1. Loads too many coefficients. Only “half” the coefficients (including center tap) are needed. Loading more or less coefficients will cause incorrect operation.
2. Improper reset of part. Both clocks must be active during reset. Both start pins high during reset and remain high until programming complete.
3. Starting part too soon. Under software control, the start pins may float momentarily before programming is complete. Once started, any writes of coefficients are ignored.
4. In DECIMATE, the designer tries to bypass the HDF by setting Hdec = 1 and Stages = 1. The correct settings are HDec = 1 and Stages = 0.
5. The designer is violating the CK_IN duty cycle requirements when HDF is bypassed. See A.C. Specifications in data sheet.
6. The designer confuses even/odd symmetry bit with even/odd length filters.
7. The designer tries to run HDF bypassed with CK_IN = FIR_CK.
8. The designer thinks that taking the start pin inactive will stop the part. Only a reset can stop the HDF Section once it has been started.
9. Has intermittent or poor results from using a low quality cheap socket or poor part insertion.
10. General - input rise/fall time to slow (>10ns), input setup/hold violations, noise.
11. System board problems are causing incorrect acquisition of outputs from DDF. i.e., in a multiplexed bus structure there is bus contention.
12. The designer does not realize data is held at outputs until next DATA_RDY.
13. The designer does not relax passband attenuation as much as possible and valuable taps are wasted.

Debug Ideas

1. Bypass the FIR or HDF Sections individually or together. If the clocks are tied together the HDF Section can be pseudo bypassed by setting HDRATE as usual, but set GROWTH = 50 and STAGES = 0. The HDF will output every Nth input sample. This will verify correct wiring of the DATA_IN bus and some of the C_BUS bits.
2. Read out coefficients as per memo.
3. Try writing F_DIS = 0 then F_DIS = 1 before loading coefficients. If this helps then poor reset procedure or floating start pins are likely.
4. Input a DC value, it should pass through a low pass filter.
5. Are DATA_RDYs at correct frequency? ($CK\_IN/(H_{dec}+F_{dec})$.

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(Rev.4.0-1 November 2017)

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