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Internal Use Only

Bat_Power_GOOD

General Description

Silego SLG7NT4953 is a low power and small form device. The SoC is housed in a 1.6 x 1.6 mm STQFN package which is optimal for using with small devices.

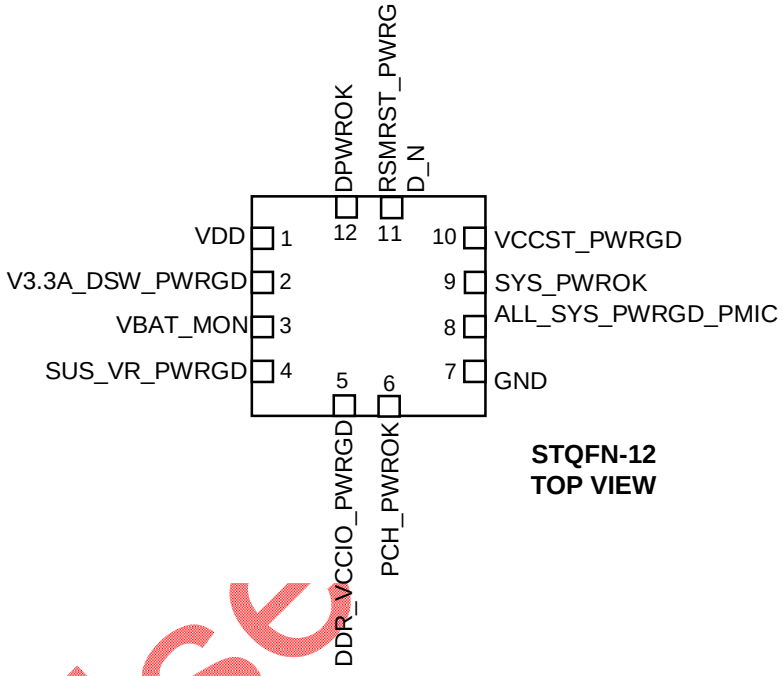
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-12 Package

Output Summary

- 3 Outputs — Push Pull 1X
- 3 Outputs — Open Drain NMOS 1X

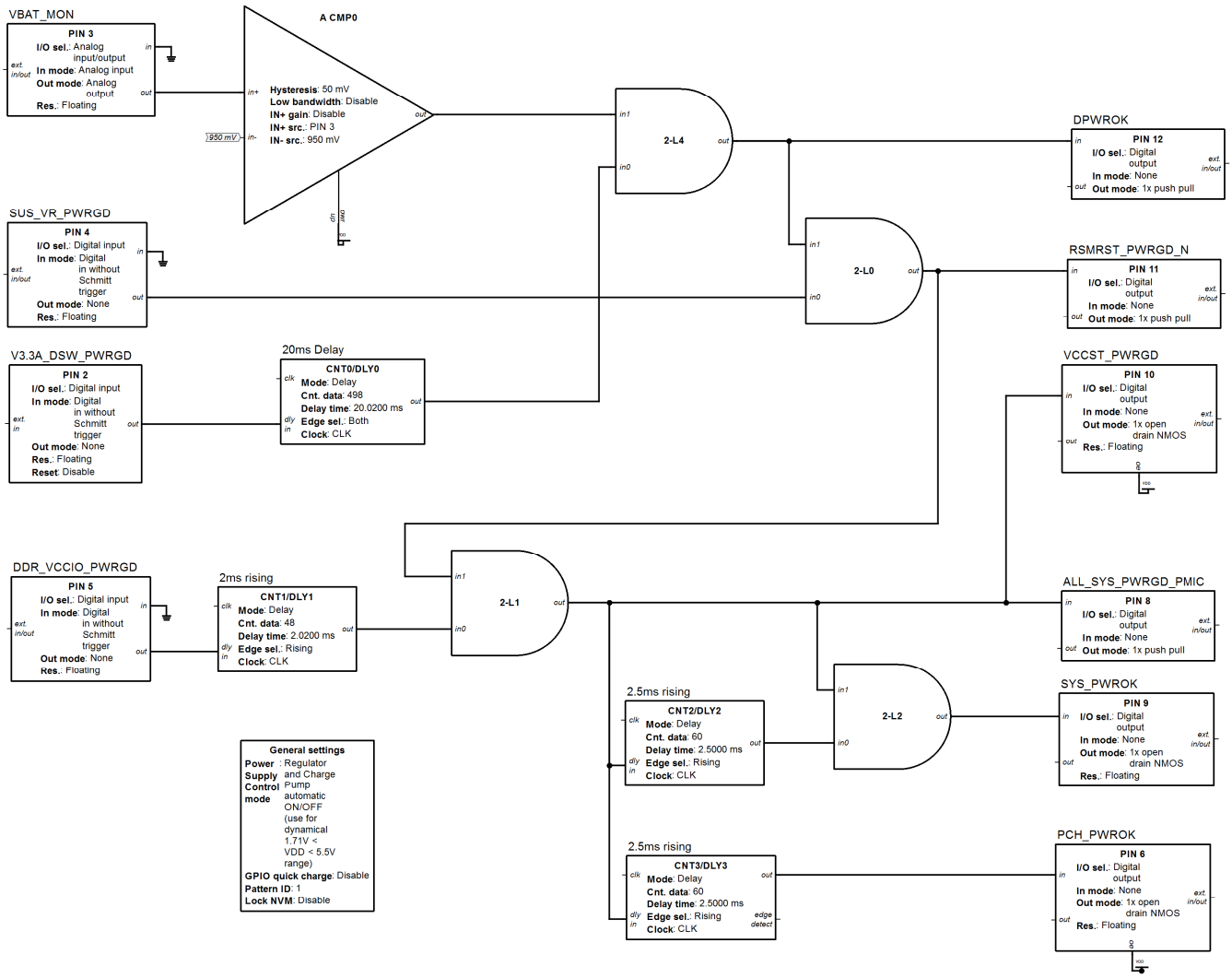
Pin Configuration



STQFN-12
TOP VIEW

Internal Use

Block Diagram



Inter

Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	V3.3A_DSW_PWRGD	Digital Input	Digital Input without Schmitt trigger
3	VBAT_MON	Analog Input/Output	Analog Input/Output
4	SUS_VR_PWRGD	Digital Input	Digital Input without Schmitt trigger
5	DDR_VCCIO_PWRGD	Digital Input	Digital Input without Schmitt trigger
6	PCH_PWROK	Digital Output	Open Drain NMOS 1X
7	GND	GND	Ground
8	ALL_SYS_PWRGD_PMIC	Digital Output	Push Pull 1X
9	SYS_PWROK	Digital Output	Open Drain NMOS 1X
10	VCCST_PWRGD	Digital Output	Open Drain NMOS 1X
11	RSMRST_PWRGD_N	Digital Output	Push Pull 1X
12	DPWROK	Digital Output	Push Pull 1X

Ordering Information

Part Number	Package Type
SLG7NT4953V	V=STQFN-12
SLG7NT4953VTR	STQFN-12 – Tape and Reel (3k units)

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Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1000	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	75	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.10	--	VDD	V
		Logic Input, at VDD=3.3V	1.78	--	VDD	
		Logic Input, at VDD=5.0V	2.64	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	--	--	0.69	V
		Logic Input, at VDD=3.3V	--	--	1.21	
		Logic Input, at VDD=5.0V	--	--	1.84	
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage (note 1)	Push Pull, I_{OH} = 100uA, 1X Driver, at VDD=1.8 V	1.68	1.79	--	V
		Push Pull & PMOS OD, I_{OH} = 3mA, 1X Driver, at VDD=3.3 V	2.71	3.09	--	
		Push Pull & PMOS OD, I_{OH} = 5mA, 1X Driver, at VDD=5.0 V	4.15	4.73	--	
V_{OL}	LOW-Level Output Voltage (note 1)	Push Pull, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.02	0.03	V
		Open Drain, I_{OL} = 100uA, 1X Driver, at VDD=1.8 V	--	0.01	0.02	
		Push Pull, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.18	0.28	
		Open Drain, I_{OL} = 3mA, 1X Driver, at VDD=3.3 V	--	0.090	0.147	

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		Push Pull, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.23	0.33	
		Open Drain, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.12	0.18	
I_{OH}	HIGH-Level Output Current (note 1)	Push Pull & PMOS OD, V_{OH} = V_{DD}-0.2, 1X Driver, at VDD=1.8 V	1.000	1.394	--	mA
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=3.3 V	5.83	10.158	--	
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	21.808	29.008	--	
I_{OL}	LOW-Level Output Current (note 1)	Push Pull, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	0.76	1.339	--	mA
		Open Drain, V_{OL} =0.15V, 1X Driver, at VDD=1.8 V	1.37	2.669	--	
		Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	4.06	6.44	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=3.3 V	7.313	12.405	--	
		Push Pull, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	6.01	9.73	--	
		Open Drain, V_{OL} =0.4V, 1X Driver, at VDD=5.0 V	11.756	17.38	--	
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, reference voltage variation and hysteresis, at temperature 25°C.	897	--	1000	mV
V_{HYST}	Analog Comparator Hysteresis Voltage (note 1)	ACMP 0	--	50	--	mV
T_{DLY0}	Delay0 Time	At temperature 25°C	18.87	20.02	20.99	ms
		At temperature -40°C +85°C (note 1)	17.02	20.02	24.85	
T_{DLY1}	Delay1 Time	At temperature 25°C	1.88	2.02	2.17	ms
		At temperature -40°C +85°C (note 1)	1.69	2.02	2.56	
T_{DLY2}	Delay2 Time	At temperature 25°C	2.33	2.5	2.67	ms
		At temperature -40°C +85°C (note 1)	2.1	2.5	3.15	
T_{DLY3}	Delay3 Time	At temperature 25°C	2.33	2.5	2.67	ms
		At temperature -40°C +85°C (note 1)	2.1	2.5	3.15	
T_{SU}	Start up Time	From VDD rising past 1.35V	--	0.31	--	ms

1. Guaranteed by Design.

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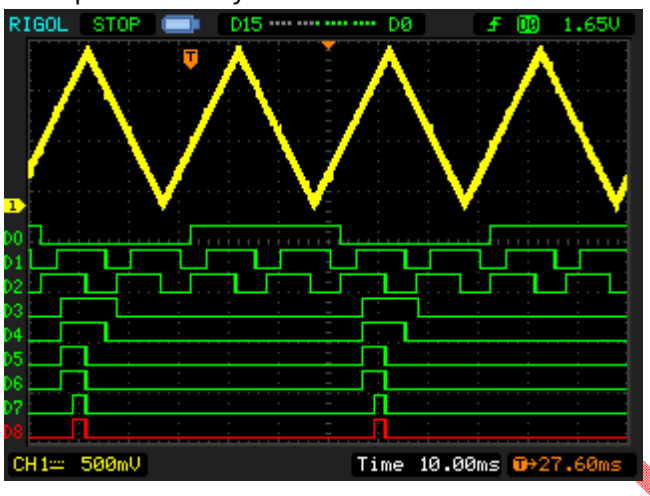
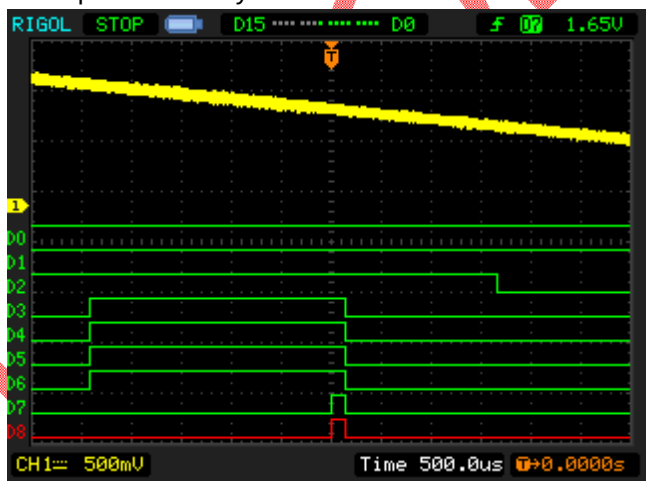
Functionality Waveforms

Channel 1 (yellow/top line) – PIN#3 (VBAT_MON)
D0 – PIN#2 (V3.3A_DSW_PWRGD)
D1 – PIN#4 (SUS_VR_PWRGD)
D2 – PIN#5 (DDR_VCCIO_PWRGD)
D3 – PIN#12 (DPWROK)
D4 – PIN#11 (RSMRST_PWRGD_N)
D5 – PIN#8 (ALL_SYS_PWRGD_PMIC)
D6 – PIN#10 (VCCST_PWRGD) with external 5kΩ pull up resistor
D7 – PIN#6 (PCH_PWROK) with external 5kΩ pull up resistor
D8 – PIN#9 (SYS_PWROK) with external 5kΩ pull up resistor

1. Chip Functionality



2. Chip Functionality



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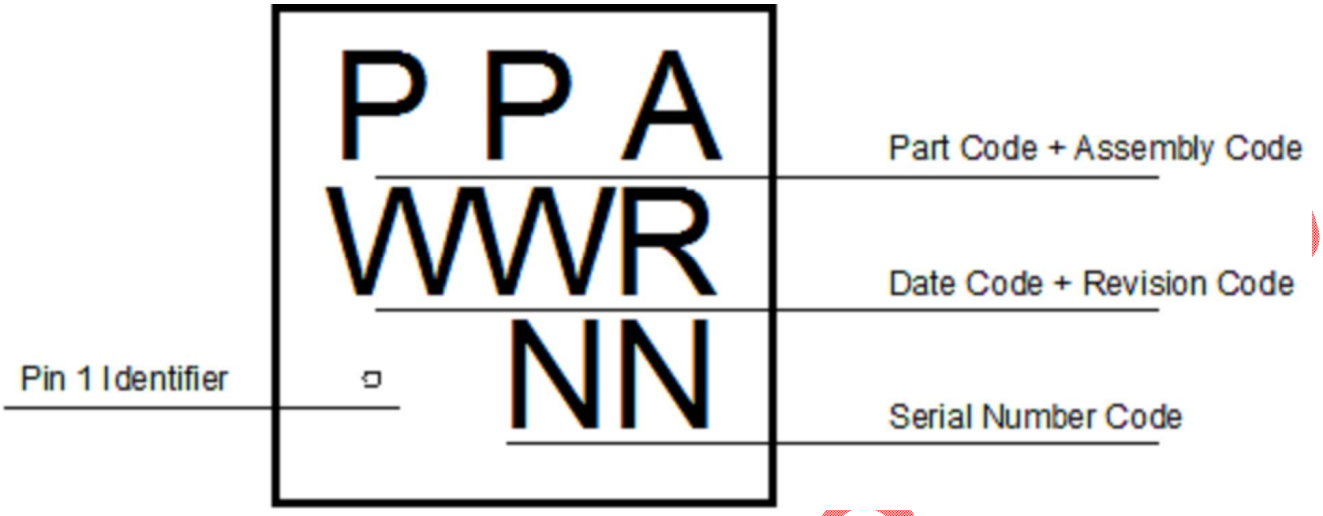
Package Top Marking



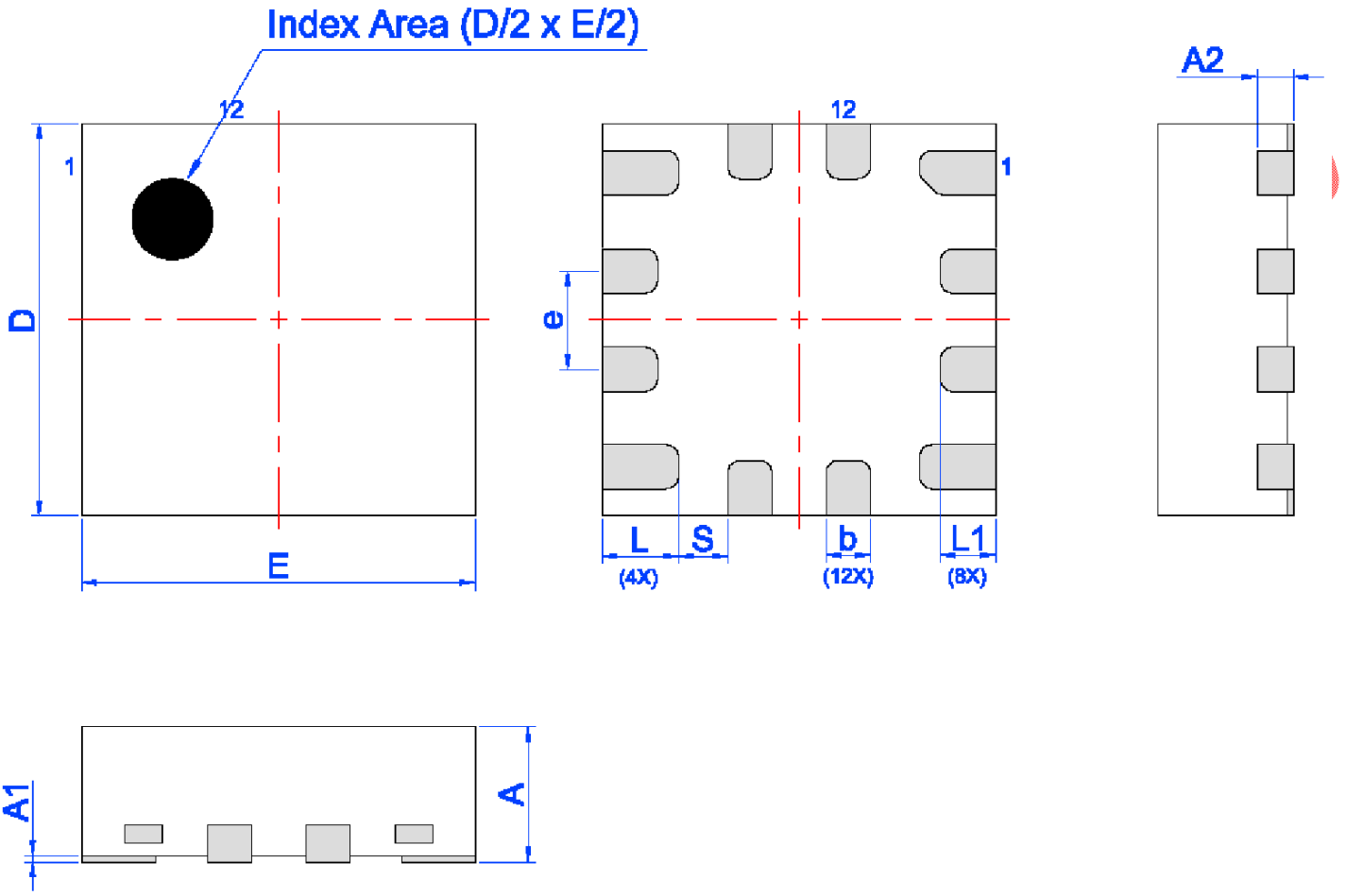
Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.12	001	U	TH	A	03/08/2015

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Internal Use

Package Drawing and Dimensions

12 Lead STQFN Package
JEDEC MO-220



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.26	0.31	0.36
b	0.13	0.18	0.23	L1	0.175	0.225	0.275
e	0.40 BSC			S	0.2 REF		

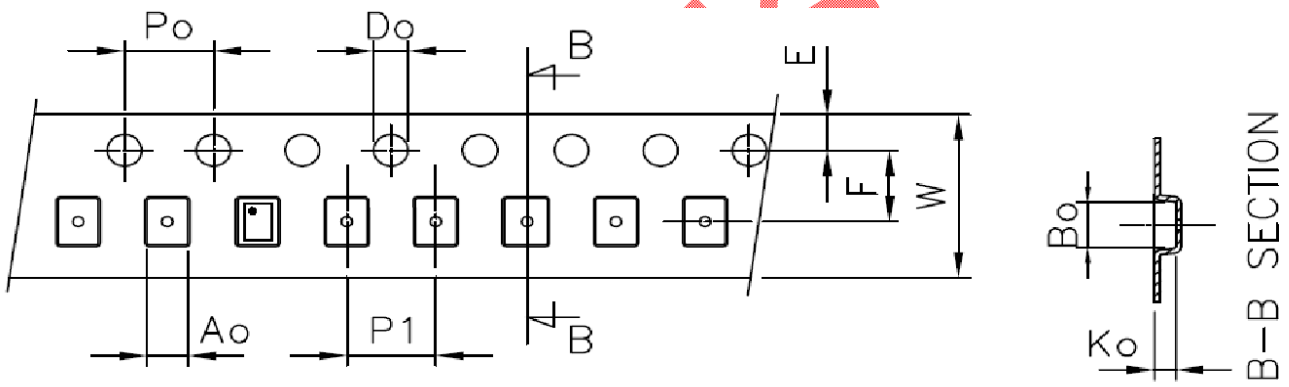
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 12L FC 0.4P Green	12	1.6x1.6x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 12L FC 0.4P Green	1.9	1.9	0.8	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm^3 (nominal). More information can be found at www.jedec.org.

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Datasheet Revision History

Date	Version	Change
10/16/2015	0.10	New design for SLG46120 chip
12/23/2015	0.11	Updated Device Revision Table
03/08/2016	0.12	Updated Title Description

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Silego Website & Support

Silego Technology Website
Silego Technology provides online support via our website at http://www.silego.com/.This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:
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http://greenpak2.silego.com/
http://greenpak3.silego.com/
http://greenfet.silego.com/
http://greenfet2.silego.com/
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