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**Phase-out/Discontinued**

**SE-17103L**

**17K SERIES**

**Phase-out/Discontinued**

**SE-17103L**

**17K SERIES**

**Phase-out/Discontinued**

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## CONTENTS

CHAPTER 1 INTRODUCTION .....	1
CHAPTER 2 SPECIFICATIONS .....	3
CHAPTER 3 BLOCK DIAGRAM .....	5
CHAPTER 4 OPERATING PROCEDURES .....	7
4.1 SETTINGS OF SE BOARD IN EACH CASE OF USING $\mu$ PD17103 AND $\mu$ PD17103L .....	7
4.2 HOW TO USE LEVEL CONVERSION CHIP ( $\mu$ PD6706GF) .....	8
4.3 HOW TO SUPPLY THE POWER TO SE BOARD .....	8
4.4 OPTION SWITCHES .....	13
4.5 ALTERATION OF OSCILLATING FREQUENCY .....	14
4.6 SETTINGS OF OTHER SWITCHES ETC. ....	15
4.7 HOW TO USE SE-17103L WITH IE-17K .....	16
4.8 HOW TO USE SE-17103L ALONE .....	21
4.9 MONITOR PINS .....	23
4.10 SETTINGS OF JUMPER SWITCHES AND SLIDE SWITCHES ETC. ....	24
CHAPTER 5 CONNECTOR PIN TABLE .....	25
CHAPTER 6 EXTERNAL FORM OF PROBE OPTION .....	26





## CHAPTER 1 INTRODUCTION

SE-17103L is a system evaluation board for 4-bit single chip microcontroller  $\mu$ PD17103 and  $\mu$ PD17103L\*. SE-17103L can be used installed with the 17K series common incircuit emulator IE-17K, and also SE-17103L can be used alone.

$\mu$ PD17103CX-00X or  $\mu$ PD17103LCX-00X (They will be called "the main chips" later on) is used as an interface with the target system. Therefore, the function of SE-17103L is the same as  $\mu$ PD17103CX or  $\mu$ PD17103LCX.

In case of connecting SE-17103L to the target system, use the option EP-17103CX (16 pin plastic DIP probe for  $\mu$ PD17103CX and  $\mu$ PD17103LCX).

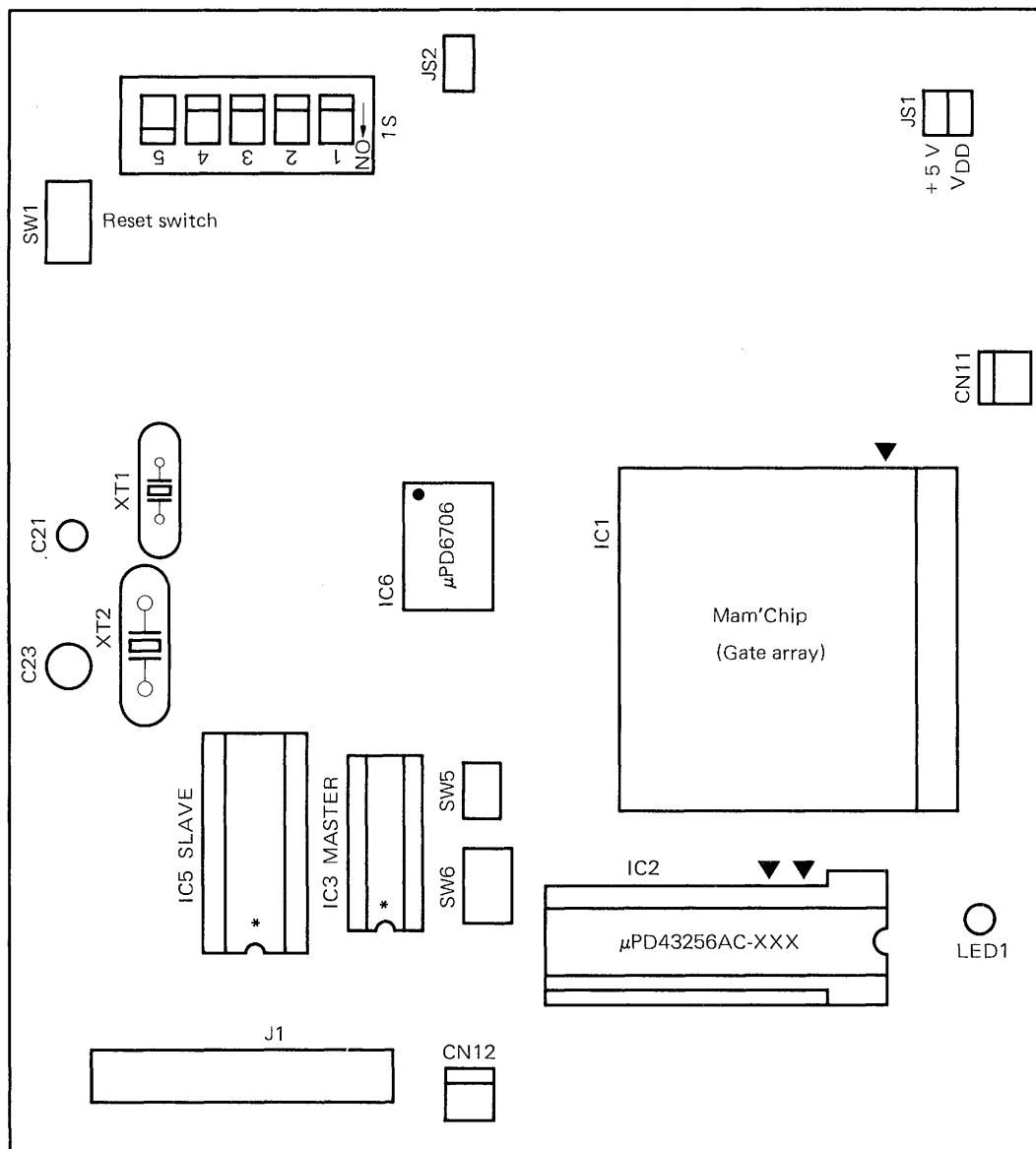
\*  $\mu$ PD17103LCX (Operating power voltage  $V_{DD} = +1.8$  to  $3.6$  V) is low voltage version of  $\mu$ PD17103CX.



## CHAPTER 2 SPECIFICATIONS

Model name	: SE-17103L
Program memory	: <ul style="list-style-type: none"><li>• In case of using SE-17103L with IE-17K, use <math>\mu</math>PD43256AC. <math>\mu</math>PD43256AC is mounted as shipped.</li><li>• In case of using SE-17103L alone, mount <math>\mu</math>PD27C256AD or <math>\mu</math>PD27C512D in which program is written.</li></ul>
Data memory	: Use the RAM built in $\mu$ PD17103CX or $\mu$ PD17103LCX (16 words x 4 bits)
Operating frequency	: 1 to 8 MHz (It is set to 1 MHz as shipped.)
Instruction cycle	: 16 $\mu$ s (When using 1 MHz crystal oscillating unit)
Operating temperature	: +10 to +40 °C
Storage temperature	: -10 to +50 °C (without condensation)
Power supply	: <ul style="list-style-type: none"><li>• Power supply for <math>\mu</math>PD17103CX (<math>V_{DD}</math>) . . . . . +2.7 to 6.0 V</li><li>Power supply for <math>\mu</math>PD17103LCX (<math>V_{DD}</math>) . . . . . +1.8 to 3.6 V</li><li>The power is supplied through the probe (EP-17103CX) or through CN12 on SE-17103L.</li><li>• Power supply for SE-17103L (<math>V_{CC}</math>) . . . . . 5 V<math>\pm</math>5 %</li><li>When using SE-17103L installed with IE-17K, the power is supplied from IE-17K.</li><li>When using SE-17103L alone, the power is supplied through CN11 on SE-17103L.</li></ul>
Current consumption	: 150 mA (MAX.) (no load, using $\mu$ PD27C256AD as a program memory)
Board dimensions	: 150 mm x 148 mm x 35 mm

Fig. 2-1 SE-17103L Component layout



\* The Main chips

- When evaluating  $\mu$ PD17103CX

Mount  $\mu$ PD17103CX-00X as IC3 and  $\mu$ PD17104CS-00X as IC5.

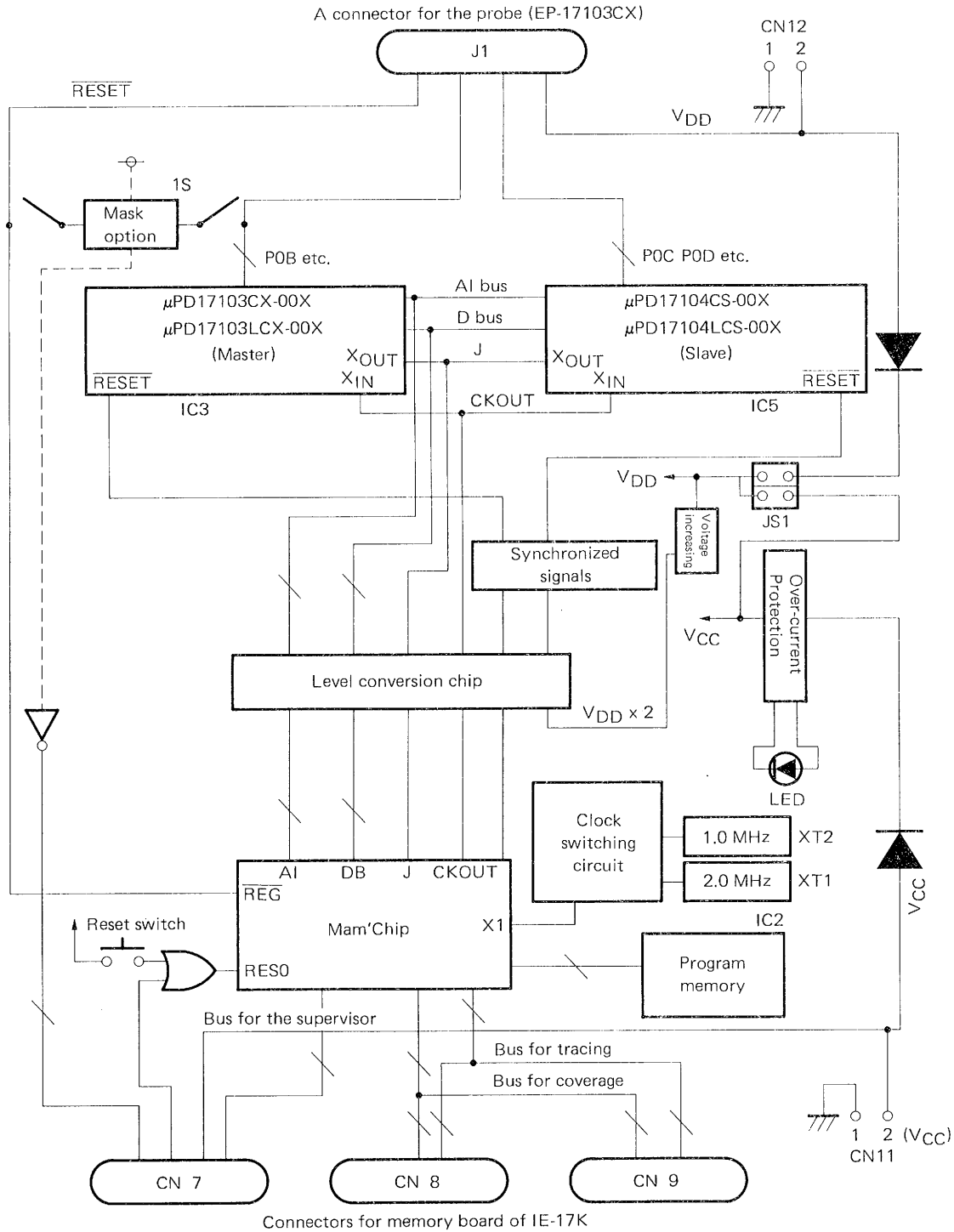
- When evaluating  $\mu$ PD17103LCX

Mount  $\mu$ PD17103LCX-00X as IC3 and  $\mu$ PD17104LCS-00X as IC5.

$\mu$ PD17103CX and  $\mu$ PD17104CS are mounted as shipped.

## CHAPTER 3 BLOCK DIAGRAM

**Fig. 3-1 Block diagram of SE-17103L**



**Phase-out/Discontinued**

## CHAPTER 4 OPERATING PROCEDURES

### 4.1 SETTINGS OF SE BOARD IN EACH CASE OF USING $\mu$ PD17103 AND $\mu$ PD17103L

SE-17103L becomes the evaluating board for the main chip by mounting the corresponding main chips which shall be evaluated as IC3 and IC5.

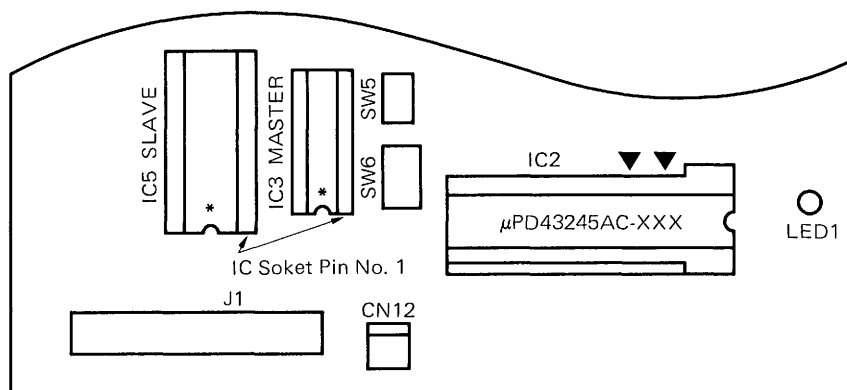
$\mu$ PD17103CX and  $\mu$ PD17104CS are mounted as IC3 and IC5 respectively so SE-17103L is set to function as the evaluation board of  $\mu$ PD17103 as shipped. It is required to exchange the main chips when evaluating  $\mu$ PD17103L referring Table 4-1 and Fig. 4-1.

**Table 4-1 The main chips to be evaluated and the corresponding main chips required to be mounted**

The main chips Chips to be evaluated	IC 3	IC5
$\mu$ PD17103	$\mu$ PD17103CX-00X	$\mu$ PD17104CS-00X
$\mu$ PD17103L	$\mu$ PD17103LCX-00X	$\mu$ PD17104LCS-00X

 : Settings as shipped.

**Fig. 4-1 Example of mounting the main chips**



\* The main chips

**Note** In case of exchanging the main chips, turn off the power, pay attention to the orientation of pin No. 1 of the main chips and insert them.



**4.2 HOW TO USE LEVEL CONVERSION CHIP ( $\mu$ PD6706GF)**

The level conversion chip is an IC that converts the voltage level to another one each other when the operating voltages differ between your target system and the SE board ( $V_{DD} \neq V_{CC}$ ,  $V_{CC} = +5$  V). Therefore, the interface between them is made smoothly by the function of the level conversion chip even in case the operating voltages are not the same between the target system and the SE board.

**Note 1.**  $V_{DD}$  is the power supply voltage of your target system.

SE-17103L is capable of supplying the power from the target system to the main chip on the SE board through CN12 or the probe. Therefore you can debug in the environment very close to the actual one.

2.  $V_{CC}$  is the power supply for operating SE board (exclusive of the main chip) and it is required to supply +5 V at any time.  $V_{CC}$  is supplied automatically from IE-17K when SE board is installed to IE-17K. In case of operating SE board alone, supply the power through CN11.

**4.3 HOW TO SUPPLY THE POWER TO SE BOARD**

The SE board requires two ways of power to be supplied with. One is the power  $V_{CC}$  to operate the SE board (exclusive of the main chip), the other is  $V_{DD}$  to operate the main chip. It is necessary to supply +5 V with  $V_{CC}$  at any time and you can supply +2.7 to 6.0 V to  $\mu$ PD17103 or +1.8 to 3.6 V to  $\mu$ PD17103L which is in the operating voltage range of the main chip.

**(1) Jumper switch JS1 for selecting the power supplying way to the SE board**

Jumper switch JS1 has the function to select the power supplying ways whether the voltage which is supplied to the SE board (+5 V) shall be applied to the main chip or whether the voltage supplied through CN12 shall be applied to the main chip. Refer to the Table 4-2 and 4-3 for its function. When your target system's power supply is +5 V, by setting JS1 to +5 V side, you would have the advantage to supply the power very easily, i.e., in case of using the SE board alone, +5 V is supplied only through CN11, and in case of using it installed with IE-17K, +5 V is supplied automatically from IE-17K.

In addition, you have the advantage to be able to do evaluation in the environment very close to the actual one because your target system's power supply can be applied to the main chip through the probe or CN12 by setting JS1 to  $V_{DD}$  side, when the power of your target system is other than +5 V.

**Notice** When evaluating  $\mu$ PD17103, supply +2.7 to 6.0 V with  $V_{DD}$  of the main chips.

When evaluating  $\mu$ PD17103L, supply +1.8 to 3.6 V with  $V_{DD}$  of the main chips.

When evaluating  $\mu$ PD17103L, set JS1 to  $V_{DD}$  at any time and supply +1.8 to 3.6 V from the target system.

If SE-17103L is operated with JS1 set to +5 V side, it may cause destructive damage in the main chips.

**Table 4-2 The function of JS1 when the SE board is installed with IE-17K**


Types of power Settings of JS1	Power supplied with the main chip ( $V_{DD}$ )	Power to operate SE board (exclusive of the main chip) ( $V_{CC}$ )
<div style="text-align: center;">JS1</div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">+5 V</div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"><math>V_{DD}</math></div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div>	The +5 V power is supplied from IE-17K.	The +5 V power is supplied from IE-17K.
<div style="text-align: center;">JS1</div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">+5 V</div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"><math>V_{DD}</math></div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div>	It is necessary to supply the power through the probe or CN12.	

**Notice** When evaluating  $\mu$ PD17103L, set JS1 to  $V_{DD}$  at any time.

**Table 4-3 The function of JS1 in case of using the SE board alone**

Types of power Settings of JS1	Power supplied with the main chip ( $V_{DD}$ )	Power to operate SE board (exclusive of the main chip) ( $V_{CC}$ )
<div style="text-align: center;">JS1</div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">+5 V</div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"><math>V_{DD}</math></div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div>	The +5 V power which is supplied through CN11 is applied.	Supply +5 V power through CN11.
<div style="text-align: center;">JS1</div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;">+5 V</div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div> <div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"><math>V_{DD}</math></div> <div style="border: 1px solid black; padding: 2px; text-align: center;">□ □</div> </div>	It is necessary to supply the power through the probe or CN12.	

**Notice** When evaluating  $\mu$ PD17103L, set JS1 to  $V_{DD}$  at any time.

**Note**  indicates the selected position of the switch.

**(2) Power supply terminals**

This SE board has three power supply terminals and it is necessary to select the way according to the evaluation environment. The terminals and their functions are mentioned in Table 4-4.

**Table 4-4 Power supply terminals and their functions**

Terminals	Types of power (Voltage range to be supplied)	Functions
CN11	$V_{CC}$ (+5 V $\pm$ 5 %)	Power supply terminal for operating SE board exclusive of the main chip in case of operating SE board alone. You need to supply +5 V at any time. In case of operating SE board installed with IE-17K, it is not necessary to supply the power through CN11. Since it is supplied from IE-17K automatically.
CN12	$V_{DD}$ • When evaluating $\mu$ PD17103 (+2.7 to 6.0 V) • When evaluating $\mu$ PD17103L (+1.8 to 3.6 V)	Power supply terminal for applying power voltage in the operating voltage range of the main chip to the main chip in case your target system's power supply voltage ( $V_{CC}$ ) is other than 5 V.
Probe (Terminal for $V_{DD}$ and GND)	$V_{DD}$ • When evaluating $\mu$ PD17103 (+2.7 to 6.0 V) • When evaluating $\mu$ PD17103L (+1.8 to 3.6 V)	The function is similar to CN12. Since in the SE board CN12 and the power pin of the probe is connected, supply the power through either one of them.

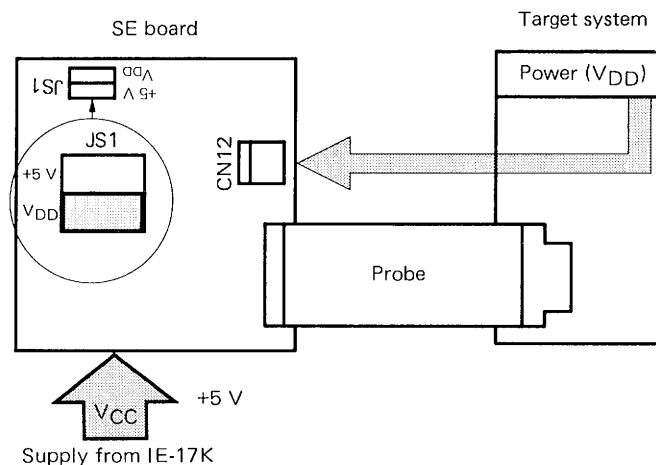
**Note** Regarding both CN11 and CN12 pin No. 1 is for GND and No. 2 is for the power. As for supplying the power we recommend you use the power supply cable attached for your convenience.

**(3) Example of practical use**

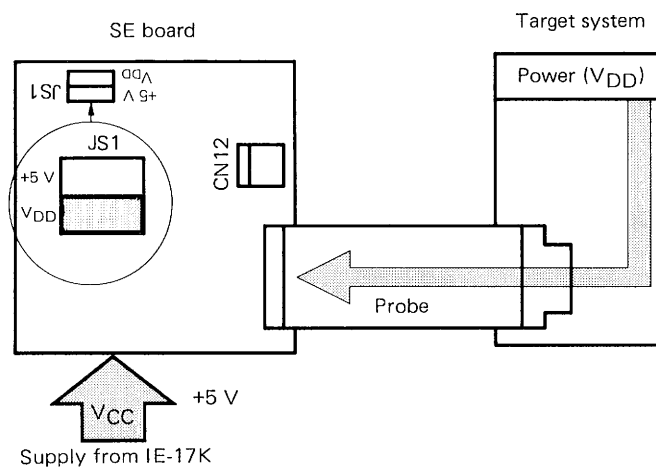
- ① In case of using the SE board installed in IE-17K

Set JS1 to  $V_{DD}$  side.  $V_{CC}$  will be supplied from IE-17K. Supply  $V_{DD}$  through CN12 or the probe.

**Fig. 4-2 Power supply method of  $V_{DD}$  through CN12 in case of installed with IE-17K**

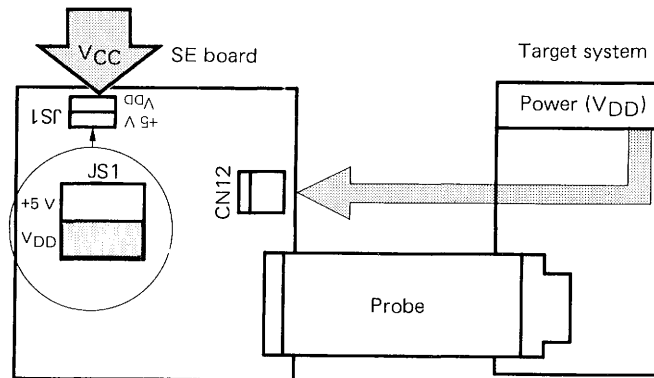


**Fig. 4-3 Power supply method of  $V_{DD}$  through the probe in case of installed with IE-17K**

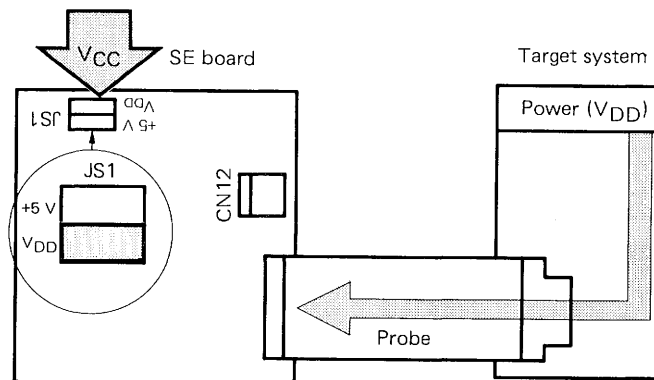


- ② In case of using the SE board alone  
Set JS1 to  $V_{DD}$  side. Supply  $V_{CC}$  through CN11, and  $V_{DD}$  through either CN12 or the probe.

**Fig. 4-4 Power supply method of  $V_{DD}$  through CN12 in case of using the SE board alone**



**Fig. 4-5 Power supply method of  $V_{DD}$  through the probe in case of using the SE board alone**



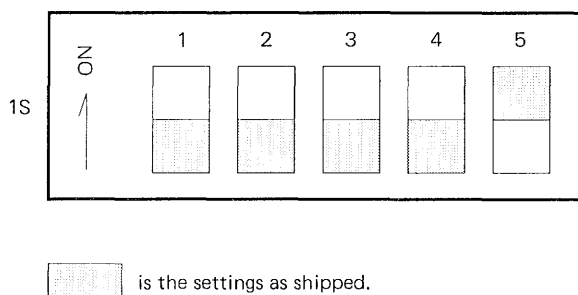
#### 4.4 OPTION SWITCHES

SE-17103L is capable of setting mask options for each pin of  $P0B_0$  to  $P0B_2$  and  $\overline{RESET}$  of  $\mu PD17103$  and  $\mu PD17103L$ .

In the debugging environment of SE-17103L, option switches (1S) are provided in order to reproduce the mask options seemingly which is described in the source program.

The appearance of option switches is as follows (refer to Fig. 2-1 as well). Set the option switches following Fig. 4-6 and Table 4-5.

**Fig. 4-6 Option switches**



**Table 4-5 Option switch settings**

Switch No.		Pin name	ON	OFF	Switch code
1S	1	P0B <sub>0</sub>	pulled up	not pulled up	0001
	2	P0B <sub>1</sub>	pulled up	not pulled up	0001
	3	P0B <sub>2</sub>	pulled up	not pulled up	0001
	4	—	—	—	—
	5	$\overline{\text{RESET}}$	pulled up	not pulled up	0000

**Note** The switch No. 1S-4 is not connected to any circuit.

In case the information of mask options described in the source program is not equivalent to that of option switch settings, IE-17K outputs the following error message

? IOS INVALID OPTION SWITCH AT XXXX

XXXX: switch code

Switch code shows the location of the option switch on the SE board whose settings is incorrect. Using the assembler (AS17K) of 17K series, the settings of mask options must be described in the source program. Just soon after the HEX file is loaded by .LP0 command or .LP1 command, IE-17K examines if the settings of option switches on SE-17103L are equivalent to the settings declared by the program. Reconfirm the settings of option switches when the error message is displayed.

**Caution** When SE-17103L is installed with IE-17K and operating without connection to the target system using the probe (EP-17103CX), or when the reset circuit of your target system is unstable, SE-17103L does not operate in some cases because the reset function may become unstable.

In this case, pull up the  $\overline{RESET}$  pin (mask option switch 1S-5) temporarily and operate SE-17103L.

#### 4.5 ALTERATION OF OSCILLATING FREQUENCY

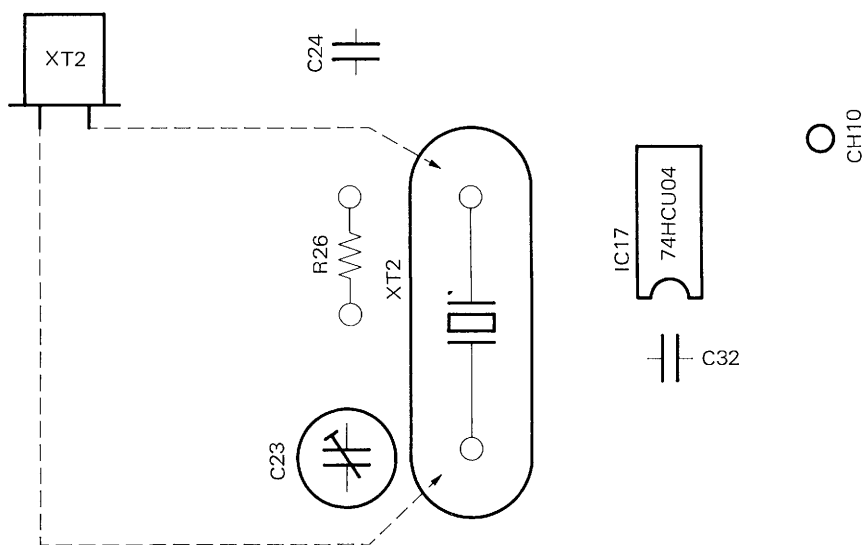
SE-17103L is capable of making alterations to the operating frequency of other than that of settings as shipped.

**Table 4-6 Settings as shipped and alterable operating frequency range**

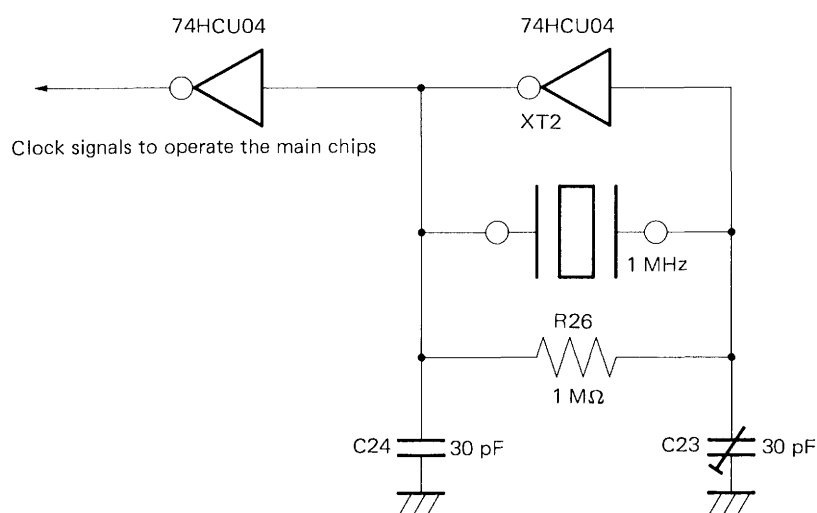
Chips to be evaluated	Settings as shipped	Alterable operating frequency range
$\mu$ PD17103	1 MHz by crystal oscillation	1 to 8 MHz
$\mu$ PD17103L		Not alterable

The oscillating circuit is implemented around XT2 as shown in Fig. 4-8.

**Fig. 4-7 Example of connecting a ceramic oscillating unit to XT2 terminals**



**Fig. 4-8 The circuit around XT2 terminals**



(1) Frequency alteration method when evaluating  $\mu$ PD17103

As shipped, the fixed 1 MHz frequency from XT2 is set to be supplied as the clock for the main chips. So the frequency can be altered by exchanging this unit connected to XT2 terminals with crystal oscillating unit or ceramic oscillating unit of 1 to 8 MHz.

#### 4.6 SETTINGS OF OTHER SWITCHES ETC.

##### (1) SW1 RESET SWITCH

SW1 is the reset switch for the case of using SE-17103L alone. For detail, refer to **"4.8 HOW TO USE SE-17103L ALONE"**.

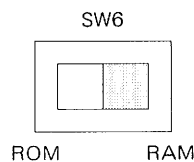
##### (2) SW5 27C256A/27C512 SELECTION SWITCH

SW5 is the selection switch of program memory type for the case of using SE-17103L alone. For detail, refer to **"4.8 HOW TO USE SE-17103L ALONE"**.

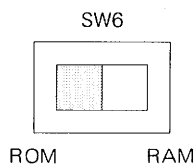
##### (3) SW6 ROM/RAM SELECTION SLIDE SWITCH


**Fig. 4-9 Settings of the ROM/RAM selection slide switch**

- ① In case of using SE-17103L installed with IE-17K



- ② In case of using SE-17103L alone



 shows the selected switch position.

##### (4) JUMPER SWITCH JS2

Use the SE board with the jumper switch JS2 connected (it is connected as shipped).

##### (5) LED1 POWER LED

LED1 lights when the power is supplied correctly. For detail, refer to **"4.7 HOW TO USE SE-17103L WITH IE-17K"** and **"4.8 HOW TO USE SE-17103L ALONE"**.



**4.7 HOW TO USE SE-17103L WITH IE-17K****(1) Mounting a RAM**

Mount the RAM ( $\mu$ PD43256AC) as a program memory. The RAM is mounted as shipped.

When using the RAM other than  $\mu$ PD43256AC, mount the RAM that accepts the following condition.

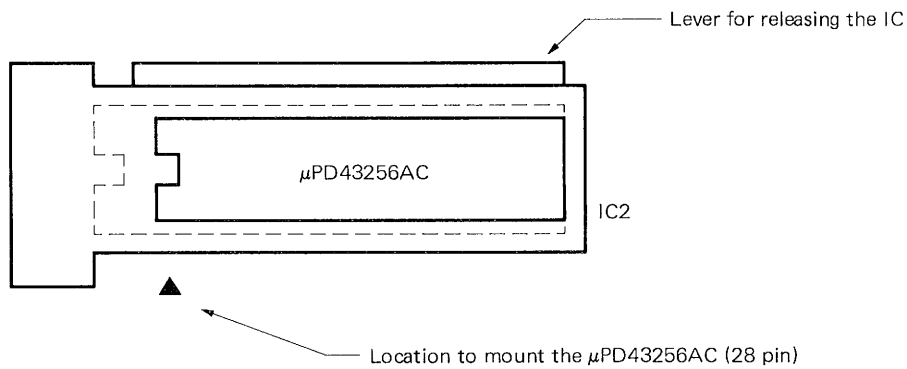
$$T_{ACC} < \text{Instruction cycle time} \div 4$$

$T_{ACC}$  : Address setting  $\rightarrow$  Data output delay time

$\mu$ PD43256AC-10, 12 and 15 are available when clock frequency is 1 MHz.

Mount the RAM paying attention to the direction and orientation of the pin No. 1 of the RAM referring Fig. 4-10.

**Fig. 4-10 How to mount the RAM**



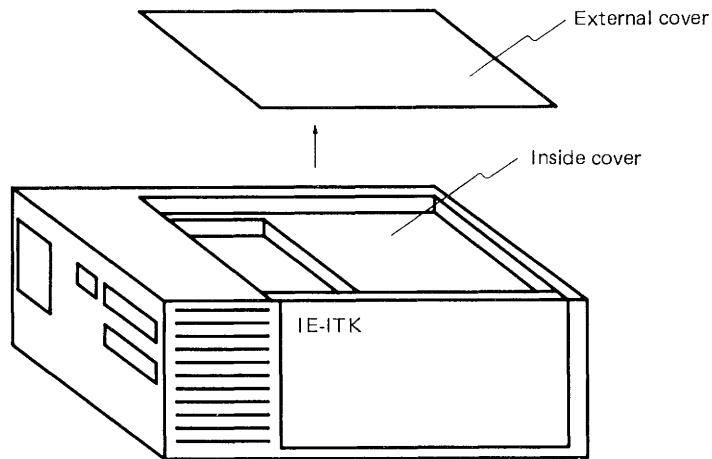
**(2) Installation and removal of SE-17103L into and from IE-17K**

To install SE-17103L into IE-17K, firstly remove the external cover and the inside cover. Fig. 4-11 shows the external view of IE-17K after removing the external cover.

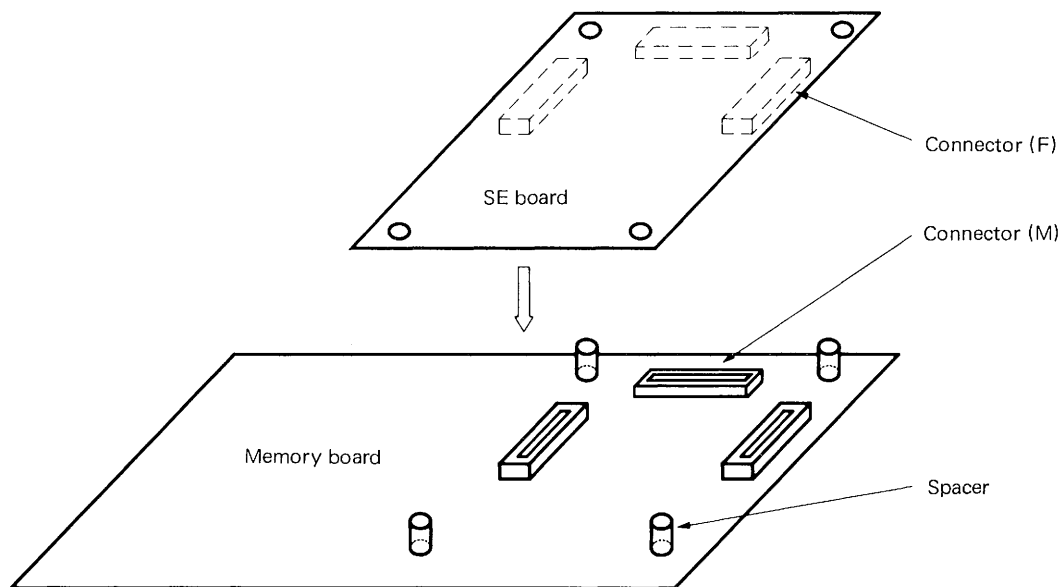
Removing the inside cover, the memory board can be seen. Three connectors are located on the memory board. SE-17103L can be installed into IE-17K by putting three connectors (CN7, 8 and 9) on SE-17103L into three connectors on IE-17K (See Fig. 4-12).

When installing SE-17103L, push it down vertically and check if three connectors are connected firmly. SE-17103L can be removed from IE-17K by lifting it up vertically (See Fig. 4-12).

**Fig. 4-11 External view of IE-17K (after removing the external cover)**



**Fig. 4-12 Installation and removal of SE-17103L**



Next, connect the probe (EP-17103CX) to the connector J1 on SE-17103L in order to connect to the target system.

Finally, install the inside cover and the external cover.

**(3) Supplying power**

After installing SE-17103L, turn on the power of IE-17K before installing the inside cover and the external cover. And check if the LED on SE-17103L lights.

In case the power voltage of target system is other than +5 V, you can apply voltage of your target system to the main chip on the SE board through CN12 or the probe. For further detail refer to **"4.2 HOW TO USE LEVEL CONVERSION CHIP ( $\mu$ PD6706GF)"** and **"4.3 HOW TO SUPPLY THE POWER TO SE BOARD"**.

The LED does not light in the following cases.

- No connection of the IE-17K power cord
- Over-current in SE-17103L (about 500 mA and more)
- Incorrect installing of SE-17103L

If the LED does not light, turn off the power of IE-17K and take out SE-17103L and then reinstall it. If it does not light yet, the trouble may exist.

**(4) Loading HEX files to IE-17K**

Connecting IE-17K to the host machine of PC-9800 series and so on. IE-17K can be used to debug the hardware and the software of the target system. With regard to the operation of IE-17K, refer to **"IE-17K USER'S MANUAL"**.

The procedure to check if SE-17103L is correctly installed is described below.

By turning on the power or pressing the RESET switch of IE-17K when the power is already supplied. IE-17K is activated and displays a prompter (@@>) which indicates the command is acceptable. Next, by .LP0 or .LP1 command load the HEX file (.HEX) of the  $\mu$ PD17103 or  $\mu$ PD17103L program made by the assembler (AS17K) or the HEX file output by .SP0 or .SP1 command. IE-17K does not operate till the HEX file is loaded. If SE-17103L is correctly installed to IE-17K, the following messages are displayed and a prompter is "BRK>".

And then IE-17K becomes the in-circuit emulator for  $\mu$ PD17103 or  $\mu$ PD17103L.

**Example** When the HEX file for  $\mu$ PD17103 is loaded.

```
OK
D17103
BRK>
```

When the above messages are not displayed, the causes seem as follows.

- In case the loaded HEX file does not correspond with the main chip mounted on SE-17103L.
- In case the SE board other than SE-17103L is installed.
- In case the HEX file of other than  $\mu$ PD17103 or  $\mu$ PD17103L is loaded.
- In case the settings of the option switches do not correspond with that declared in the program.
- In case the installation of SE-17103L with IE-17K is incomplete.

**(5) Error messages and the corresponding trouble shooting method**

IE-17K and SE-17103L has the function to display error messages in case the combination is incorrect between the mounted main chip and the loaded HEX file.

In addition, for the purpose of being able to do more reliable debugging, the SE board number is entered in SE-17103L, device numbers are entered in each of  $\mu$ PD17103CX-00X and  $\mu$ PD17103CX-00X.

The entry numbers, error messages and corresponding trouble shooting methods are described below.

**Table 4-7 The device number and the SE board number**

Devices to be evaluated	Device number	SE board number
$\mu$ PD17103	05	05
$\mu$ PD17103L	25	

**Note 1.** The device number is the entry number that each main chip has.

**Note 2.** SE board number is the entry number that the SE board has. In SE-17103L, number 05 is entered.

**Note 3.** The device number and the SE board number are embedded in the data in the HEX file to be loaded. They are used when the HEX file is loaded for the purpose of checking the development environment by IE-17K.

For instance, in the HEX file assembled by using AS17103, the device number 05 and the SE board number 05 are embedded.

- (a) The error message in case the main chip mounted on SE-17103L and the loaded HEX file does not match and the trouble shooting method.

**Error message example**

? IDI INVALID DEVICE ID NUMBER [XX- $\Delta$   $\Delta$ ]

XX indicates the device number of the actually mounted main chip and  $\Delta$   $\Delta$  is the device number embedded in the loaded HEX file.

When this error message is displayed, reconfirm the main chip on the SE board. In case incorrect main chip is mounted, turn off the power of IE-17K, exchange the main chip and reload the HEX file anew. In case the incorrect device file is chosen mistakenly when assembling, assemble the source file again using correct device file and reload this HEX file.

- (b) Error message when SE board other than SE-17103L is installed and the HEX file of the device other than  $\mu$ PD17103 or  $\mu$ PD17103L is loaded, and the trouble shooting method.

**Error message example**

? ISE INVALID SE BOARD NUMBER [ $\square$   $\square$ - $\nabla$   $\nabla$ ]

$\square$   $\square$  indicates the actually installed SE board and  $\nabla$   $\nabla$  indicates the SE board number embedded in the loaded HEX file. The SE board number  $\square$   $\square$  is 05 for SE-17103L, the SE board number  $\nabla$   $\nabla$  is 05 in case the HEX file is loaded of  $\mu$ PD17103 and  $\mu$ PD17103L.

When this error message is displayed, reconfirm the SE board and the HEX file that you have loaded.

- (c) The error message in case that the settings of option switches differ from the mask option information declared in the program and the trouble shooting method.

**Error message example**

? IOS INVALID OPTION SWITCH AT XXXX

XXXX indicates the switch code of the option switch that does not agree with the setting declared by the program.

With regard to the trouble shooting when this error message is displayed, refer to **"4.4 OPTION SWITCHES"**.

- (d) No response from IE-17K

- ① Incomplete installation of SE-17103L can be thought. Install SE-17103L firmly and correctly again.
- ② Incorrect connection of the probe (EP-17103CX) between the target system and the SE board. Confirm all connecting points again.
- ③ It can be thought that the reset circuit in your target system is not functioning correctly. At this time the reset state in the SE board is unstable in some cases so IE-17K is unable to respond.

For the purpose of check if the state is the one mentioned above, there is a way that you firstly set the mask option switch IS-5 ( $\overline{\text{RESET}}$ ) ON and activate IE-17K again. At this time the above mentioned error message ?IOS INVALID OPTION SWITCH AT XXXX can be displayed but you can load the HEX file.

When the state is found to be the one mentioned above, correct your target system or your source program so all error messages will not be displayed without delay.

**(6) CAUTION**

- When turning on the power, turn on the power to IE-17K and then the target system.
- Never use the reset switch on SE-17103L. When resetting IE-17K, use the reset switch on IE-17K.

**4.8 HOW TO USE SE-17103L ALONE****(1) Mounting a ROM**

When using SE-17103L alone, mount the PROM ( $\mu$ PD27C256AD or  $\mu$ PD27C512D) as a program memory. Mount the PROM that accepts the following condition.

ROM size

256K bit :  $\mu$ PD27C256AD-12, -15, -20 or their substitutes

512K bit :  $\mu$ PD27C512D-12, -15, -20 or their substitutes

It is required to write whichever output file as below into the PROM as a program.

- PROM file (.PRO) for  $\mu$ PD17103 or  $\mu$ PD17103L made by the assembler (AS17K) for 17K series.  
Do not write the HEX file (.HEX) made by AS17K that is output to IE-17K into the PROM.
- File for the PROM made by .XS0 or .XS1 command of IE-17K.

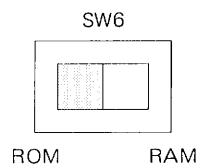
**[Note for PROM writing]**


The last program memory address of the  $\mu$ PD17103 and  $\mu$ PD17103L is 1FFH.

**(2) Settings of ROM/RAM selection slide switch**

Set the ROM/RAM selection slide switch SW6 to the ROM side as shown in Fig. 4-13.

**Fig. 4-13 Settings of ROM/RAM selection switch**

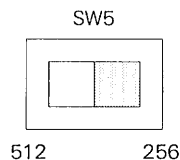
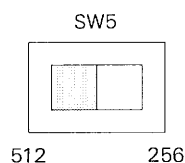



 indicates the selected switch position.

**(3) Settings of 27C256/27C512 selection slide switch (SW5)**

Set 27C256/27C512 selection switch (SW5) according to which ROM is to be used as a program memory  $\mu$ PD27C256AD or  $\mu$ PD27C512D as shown in Fig. 4-14.

**Fig. 4-14 Settings of 27C256AD/27C512D selection switch SW5**

**(a) When using  $\mu$ PD27C256AD****(b) When using  $\mu$ PD27C512D**

 indicates the selected switch position.

**(4) Supplying the power**

Supply 5 V  $\pm$  5 % ( $V_{CC}$ ) through CN11 with SE-17103L from the external power supply in any case.

In case that the power voltage of your target system is that of other than +5 V, it is possible to apply the power voltage of the target system to the main chip on the SE board through CN12 or the probe. For detail, refer **"4.2 HOW TO USE LEVEL CONVERSION CHIP ( $\mu$ PD6706GF)"** and **"4.3 HOW TO SUPPLY THE POWER TO SE BOARD"**.

When the power is supplied normally, the LED on SE-17103L lights.

The LED does not light in the following cases.

- No supplying power to SE-17103L
- Over-current in SE-17103L (approximately 500 mA or more)

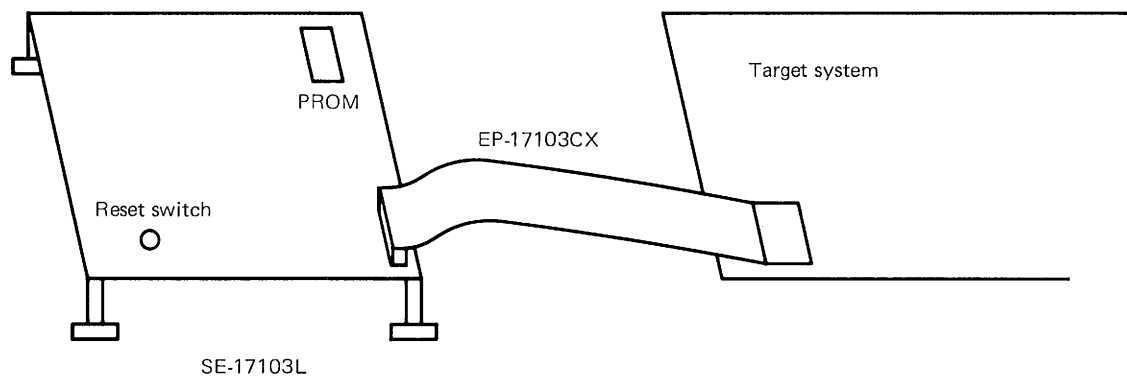
**(5) Program executing**

Connect the target system to SE-17103L as shown in Fig. 4-15.

Starting to supply the power to target system, the power is supplied to SE-17103L and the POWER-ON-RESET procedure is activated and the program written in the PROM is executed from the location 0.

By pressing the RESET switch on SE-17103L, SE-17103L is reset forcibly. As same as the POWER-ON-RESET procedure, the program written in the PROM is executed from the location 0.

**Fig. 4-15 Example of connection of SE-17103L when using it alone**



**4.9 MONITOR PINS**

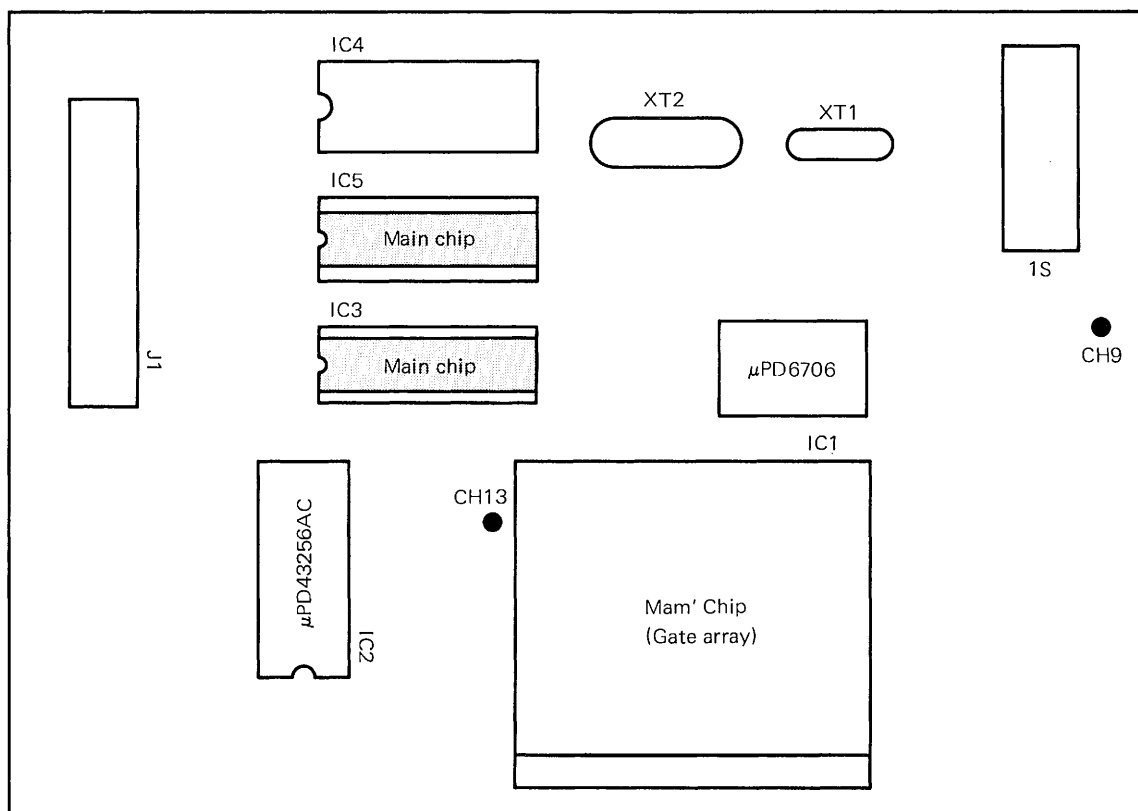
Monitor pins are provided on SE-17103L for the purpose of investigating the state of pins of the main chip. Monitor pin names and their functions are described in Table 4-8 and monitor pin location is shown in Fig. 4-16.

**Table 4-8 Monitor pin names and their functions**

Monitor pin name	Function
CH9	for monitoring $\overline{\text{RESET}}$ pin
CH13	for monitoring oscillating frequency of the main chip

**Fig. 4-16 Monitor pins location**

SE-17103L (Top View)





**4.10 SETTINGS OF JUMPER SWITCHES AND SLIDE SWITCHES ETC.**

When SE-17103L is shipped, the settings of IC2 (the program memory), the jumper switches, the slide switches, option switches and the crystal oscillating units are as below.

**(1) IC2 (Program memory)**

A RAM ( $\mu$ PD43256AC) is mounted.

**(2) Oscillating units**

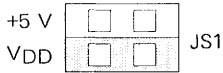

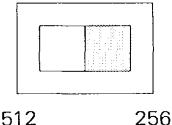
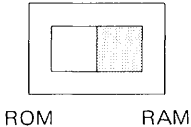
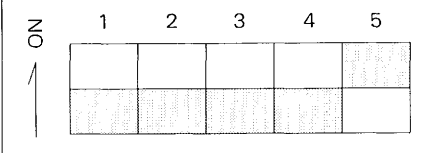
A 2 MHz crystal oscillating unit is mounted as XT1 and a 1 MHz crystal oscillating unit is mounted as XT2 as shipped.


**Note** With regard to the alteration of oscillating frequency, refer to **"4.5 ALTERATION OF OSCILLATING FREQUENCY"**.

**(3) Jumper switches and slide switches etc.**

They are set as illustrated in Table 4-9. Confirm the setting conditions before using the system.

**Table 4-9 Settings of jumper switches and slide switches etc.**

Switch No.	Jumper switches, slide switches	Setting conditions		Position
JS1		Refer to <b>"4.2 HOW TO USE LEVEL CONVERSION CHIP (<math>\mu</math>PD6706GF)"</b> and <b>"4.3 HOW TO SUPPLY THE POWER TO THE SE BOARD"</b> .		
JS2		It is connected as shipped.		Do not remove.
SW5		When installed with IE-17K for evaluation		Either side of 256 or 512 is usable.
		When SE-17103L is used alone for evaluation	Using 27C25-6A	256 side
			Using 27C512	512 side
SW6		When installed with IE-17K for evaluation.		RAM side
		When SE-17103L is used alone for evaluation. Note) Set SW5 as well.		ROM side
1S		Refer to <b>"4.4 OPTION SWITCHES"</b> .		

 is the settings as shipped.

## CHAPTER 5 CONNECTOR PIN TABLES

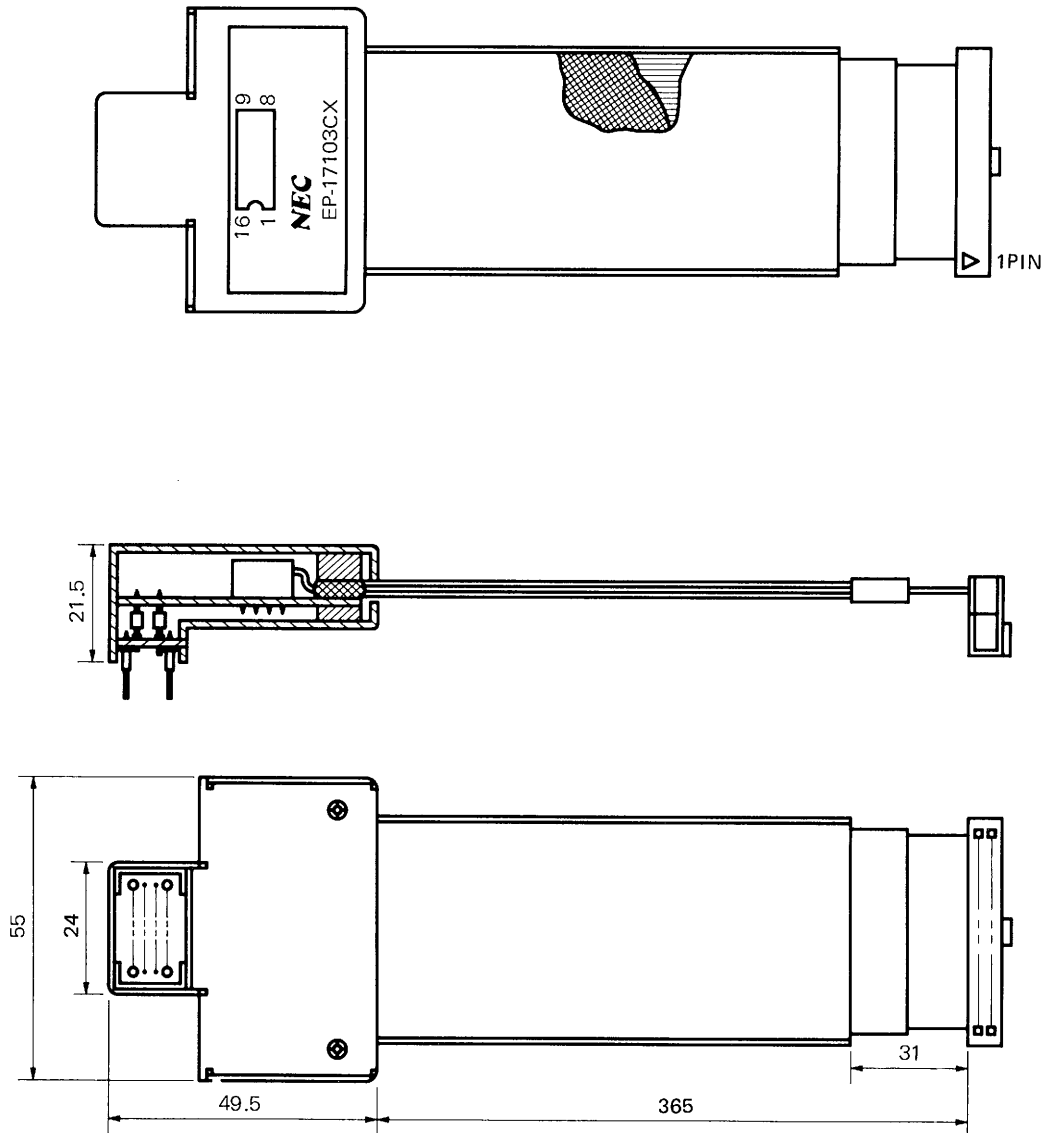
**Table 5-1 Connector (J1) for probe**

J1 Pin No.	Pin name (Pin No. of IC)	J1 Pin No.	Pin name (Pin No. of IC)	J1 Pin No.	Pin name (Pin No. of IC)
1	GND	21	GND	41	GND
2	V <sub>DD</sub> (IC3-8)	22	N.C	42	P0C <sub>0</sub> /D <sub>4</sub> (IC5-3)
3	GND	23	GND	43	GND
4	X1 (N.C)	24	N.C	44	N.C
5	GND	25	GND	45	GND
6	P0B <sub>2</sub> /MD <sub>2</sub> (IC3-15)	26	P0C <sub>3</sub> /D <sub>7</sub> (IC5-6)	46	N.C
7	GND	27	GND	47	GND
8	X2 (N.C)	28	P0D <sub>1</sub> /D <sub>1</sub> (IC5-16)	48	N.C
9	GND	29	GND	49	GND
10	N.C	30	P0C <sub>2</sub> /D <sub>0</sub> (IC5-5)	50	N.C
11	GND	31	GND	51	GND
12	N.C	32	P0D <sub>2</sub> /D <sub>2</sub> (IC5-17)	52	N.C
13	GND	33	GND	53	GND
14	P0B <sub>1</sub> /MD <sub>1</sub> (IC3-14)	34	N.C	54	N.C
15	GND	35	GND	55	GND
16	$\overline{\text{RESET}}$ (IC3-3)	36	N.C	56	N.C
17	GND	37	GND	57	GND
18	P0B <sub>0</sub> /MD <sub>0</sub> (IC3-13)	38	P0C <sub>1</sub> /D <sub>5</sub> (IC5-4)	58	N.C
19	GND	39	GND	59	GND
20	P0D <sub>0</sub> /D <sub>0</sub> (IC5-15)	40	P0D <sub>3</sub> /D <sub>3</sub> (IC5-18)	60	N.C

## CHAPTER 6 EXTERNAL FORM OF PROBE (OPTION)

Model name : EP-17103CX

Fig. 6-1 External form of probe



**Phase-out/Discontinued**

**NEC**