RL78/G22, RL78/G23

Capacitive Sensing Unit

[V3.3.0 and Earlier Versions of the QE for Capacitive Touch Tool]

Countermeasures for Limitations on the Permissible Frequency Range for SUCLK Operation

May 28, 2024

Renesas Electronics Corporation

Capacitive Sensing Unit in the RL78/G22 or RL78/G23

[V3.3.0 and Earlier Versions of the QE Tool] Countermeasures for Limitations on the Permissible Frequency Range for SUCLK Operation

As stated in the TECHNICAL UPDATE (TU) Document No: TN-RL*-A0136A/E, SUCLK is capable of operating at a frequency in the range from 16 MHz to 32 MHz.

Therefore, if you are using a V3.3.0 or earlier version of the QE tool, you need to cope with limitations related to the SUCLK setting.

Refer to the following pages and take appropriate measures according to your usage.

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Countermeasures for the Default Settings

(When the SUCLK Frequency is 32 MHz and the Drive Pulse Frequency Is 0.5 MHz, 1 MHz, 2 MHz, or 4 MHz)

Countermeasures for the Default Settings

(When the SUCLK Frequency is 32 MHz and the Drive Pulse Frequency is 0.5 MHz, 1 MHz, 2 MHz, or 4 MHz)

If you are using a QE tool with the default settings, take either of measures 1 and 2 stated below.

Measure 1

The next revision of the touch tool (QE V3.5.0) will be released around May 31, 2024.

Use a V3.5.0 or later version of the QE tool to retune and re-evaluate your product

at the time of development/update/review of your product.

Measure 2

If you are using a V3.3.0 or earlier version of the QE tool with the default settings, you can manually modify the SUCLK setting by referring to “Manually Modifying the SUCLK Setting When the Drive Pulse Frequency is xx MHz” on the

following pages.

Do this at the time of development/update/review of your product.

Manually Modifying the SUCLK Setting When the Drive Pulse Frequency is 0.5 MHz

SUCLK = STCLK × frequency multiplier setting (frequency multiplier x)

The STCLK frequency is 0.5 MHz with the default setting.

■ Modifying the SUCLK setting

SUCLK is capable of operating at a frequency in the range from 16 MHz to 32 MHz. Therefore, make the modifications as shown below.

When the SUCLK frequency is 32 MHz (the default setting in V3.3.0 and earlier versions of the QE tool) and the drive pulse frequency is 0.5 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	64	55	73
SUCLK frequency (MHz)	32.0	27.5	36.5
CTSUSO1.SDPA[7:0] bit setting	31	31	31
Frequency divisor for the drive pulse	64	64	64
Drive pulse frequency (MHz)	0.500	0.430	0.570

Setting prohibited

Modifying

Setting the SUCLK frequency to 24 MHz and the drive pulse frequency to 0.5 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	48	41	55
SUCLK frequency (MHz)	24.0	20.5	27.5
CTSUSO1.SDPA[7:0] bit setting	23	23	23
Frequency divisor for the drive pulse	48	48	48
Drive pulse frequency (MHz)	0.500	0.427	0.573

The differences between the drive pulse frequencies before and after modification for measurement 2 and measurement 3 do not create a problem because the difference values are very small.

■ Modifying the program

The project after tuning with the default settings of the QE tool requires modifications 1 and 2 below. Modify the program and build the result before use.

Modification 1

To change the frequency multiplier, modify qe_gen/qe_define.h output after tuning as follows.

#define CTSU_CFG_SUMULTI0 (0x3F) → (0x2F)

#define CTSU_CFG_SUMULTI1 (0x36) → (0x28)

#define CTSU_CFG_SUMULTI2 (0x48) → (0x36)

Modification 2

To change the setting of CTSUSO1.SDPA[7:0] bits, modify the setting of the SDPA bits in qe_gen/qe_config.c output after tuning as follows.

```
const ctsu_element_cfg_t g_qe_ctsu_element_cfg_config01[] =
{
   { .so = 0x027, .snum = 0x07, .sdpa = 0x1F }, → .sdpa = 0x17
   { .so = 0x024, .snum = 0x07, .sdpa = 0x1F }, → .sdpa = 0x17
   { .so = 0x029, .snum = 0x07, .sdpa = 0x1F }, → .sdpa = 0x17
};
```

Manually Modifying the SUCLK Setting When the Drive Pulse Frequency is 1 MHz

SUCLK = STCLK × frequency multiplier setting (frequency multiplier x)

The STCLK frequency is 0.5 MHz with the default setting.

■ Modifying the SUCLK setting

SUCLK is capable of operating at a frequency in the range from 16 MHz to 32 MHz. Therefore, make the modifications as shown below.

When the SUCLK frequency is 32 MHz (the default setting in V3.3.0 and earlier versions of the QE tool) and the drive pulse frequency is 1 MHz

—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	64	55	73
SUCLK frequency (MHz)	32.0	27.5	36.5
CTSUSO1.SDPA[7:0] bit setting	15	15	15
Frequency divisor for the drive pulse	32	32	32
Drive pulse frequency (MHz)	1.000	0.859	1.141

Setting prohibited

Modifying

Setting the SUCLK frequency to 24 MHz and the drive pulse frequency to 1 MHz

—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	48	41	55
SUCLK frequency (MHz)	24.0	20.5	27.5
CTSUSO1.SDPA[7:0] bit setting	11	11	11
Frequency divisor for the drive pulse	24	24	24
Drive pulse frequency (MHz)	1.000	0.854	1.146

The differences between the drive pulse frequencies before and after modification for measurement 2 and measurement 3 do not create a problem because the difference values are very small.

■ Modifying the program

The project after tuning with the default settings of the QE tool requires modifications 1 and 2 below. Modify the program and build the result before use.

Modification 1

To change the frequency multiplier, modify qe_gen/qe_define.h output after tuning as follows.

```
#define CTSU_CFG_SUMULTI0    (0x3F) → (0x2F)
#define CTSU_CFG_SUMULTI1    (0x36) → (0x28)
#define CTSU_CFG_SUMULTI2    (0x48) → (0x36)
```

Modification 2

To change the setting of CTSUSO1.SDPA[7:0] bits, modify the setting of the SDPA bits in qe_gen/qe_config.c output after tuning as follows.

```
const ctsu_element_cfg_t g_qe_ctsu_element_cfg_config01[] =
{
  { .so = 0x027, .snum = 0x07, .sdpa = 0x0F }, → .sdpa = 0x0B
  { .so = 0x024, .snum = 0x07, .sdpa = 0x0F }, → .sdpa = 0x0B
  { .so = 0x029, .snum = 0x07, .sdpa = 0x0F }, → .sdpa = 0x0B
};
```

Manually Modifying the SUCLK Setting When the Drive Pulse Frequency is 2 MHz

SUCLK = STCLK × frequency multiplier setting (frequency multiplier x)

The STCLK frequency is 0.5 MHz with the default setting.

■ Modifying the SUCLK setting

SUCLK is capable of operating at a frequency in the range from 16 MHz to 32 MHz. Therefore, make the modifications as shown below.

When the SUCLK frequency is 32 MHz (the default setting in V3.3.0 and earlier versions of the QE tool) and the drive pulse frequency is 2 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	64	55	73
SUCLK frequency (MHz)	32.0	27.5	36.5
CTSUSO1.SDPA[7:0] bit setting	7	7	7
Frequency divisor for the drive pulse	16	16	16
Drive pulse frequency (MHz)	2.000	1.719	2.281

Setting prohibited

Modifying

Setting the SUCLK frequency to 24 MHz and the drive pulse frequency to 2 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	48	41	55
SUCLK frequency (MHz)	24.0	20.5	27.5
CTSUSO1.SDPA[7:0] bit setting	5	5	5
Frequency divisor for the drive pulse	12	12	12
Drive pulse frequency (MHz)	2.000	1.708	2.292

The differences between the drive pulse frequencies before and after modification for measurement 2 and measurement 3 do not create a problem because the difference values are very small.

■ Modifying the program

The project after tuning with the default settings of the QE tool requires modifications 1 and 2 below. Modify the program and build the result before use.

Modification 1

To change the frequency multiplier, modify qe_gen/qe_define.h output after tuning as follows.

#define CTSU_CFG_SUMULTI0 (0x3F) → (0x2F)

#define CTSU_CFG_SUMULTI1 (0x36) → (0x28)

#define CTSU_CFG_SUMULTI2 (0x48) → (0x36)

Modification 2

To change the setting of CTSUSO1.SDPA[7:0] bits, modify the setting of the SDPA bits in qe_gen/qe_config.c output after tuning as follows.

```
const ctsu_element_cfg_t g_qe_ctsu_element_cfg_config01[] =
{
   { .so = 0x027, .snum = 0x07, .sdpa = 0x07 }, → .sdpa = 0x05
   { .so = 0x024, .snum = 0x07, .sdpa = 0x07 }, → .sdpa = 0x05
   { .so = 0x029, .snum = 0x07, .sdpa = 0x07 }, → .sdpa = 0x05
};
```

Manually Modifying the SUCLK Setting When the Drive Pulse Frequency is 4 MHz

SUCLK = STCLK × frequency multiplier setting (frequency multiplier x)

The STCLK frequency is 0.5 MHz with the default setting.

■ Modifying the SUCLK setting

SUCLK is capable of operating at a frequency in the range from 16 MHz to 32 MHz. Therefore, make the modifications as shown below.

When the SUCLK frequency is 32 MHz (the default setting in V3.3.0 and earlier versions of the QE tool) and the drive pulse frequency is 4 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	64	55	73
SUCLK frequency (MHz)	32.0	27.5	36.5
CTSUSO1.SDPA[7:0] bit setting	3	3	3
Frequency divisor for the drive pulse	8	8	8
Drive pulse frequency (MHz)	4.000	3.438	4.563

Setting prohibited

Modifying

Setting the SUCLK frequency to 24 MHz and the drive pulse frequency to 4 MHz			
—	Measurement 1	Measurement 2	Measurement 3
Frequency multiplier	48	41	55
SUCLK frequency (MHz)	24.0	20.5	27.5
CTSUSO1.SDPA[7:0] bit setting	2	2	2
Frequency divisor for the drive pulse	6	6	6
Drive pulse frequency (MHz)	4.000	3.417	4.583

The differences between the drive pulse frequencies before and after modification for measurement 2 and measurement 3 do not create a problem because the difference values are very small.

■ Modifying the program

The project after tuning with the default settings of the QE tool requires modifications 1 and 2 below. Modify the program and build the result before use.

Modification 1

To change the frequency multiplier, modify qe_gen/qe_define.h output after tuning as follows.

```
#define CTSU_CFG_SUMULTI0    (0x3F) → (0x2F)
#define CTSU_CFG_SUMULTI1    (0x36) → (0x28)
#define CTSU_CFG_SUMULTI2    (0x48) → (0x36)
```

Modification 2

To change the setting of CTSUSO1.SDPA[7:0] bits, modify the setting of the SDPA bits in qe_gen/qe_config.c output after tuning as follows.

```
const ctsu_element_cfg_t g_qe_ctsu_element_cfg_config01[] =
{
   { .so = 0x027, .snum = 0x07, .sdpa = 0x03 }, → .sdpa = 0x02
   { .so = 0x024, .snum = 0x07, .sdpa = 0x03 }, → .sdpa = 0x02
   { .so = 0x029, .snum = 0x07, .sdpa = 0x03 }, → .sdpa = 0x02
};
```

Countermeasure for the Advanced Mode of the QE Tool

(When the Drive Pulse Frequency is Changed in the Advanced Mode)

Countermeasure for the Advanced Mode of the QE Tool
(When the Drive Pulse Frequency is Changed in the Advanced Mode)

If you are using a V3.3.0 or earlier version of the QE tool to change the drive pulse frequency in the advanced mode,

take the following measure.

Measure

The next revision of the touch tool (QE V3.5.0) will be released around May 31, 2024.

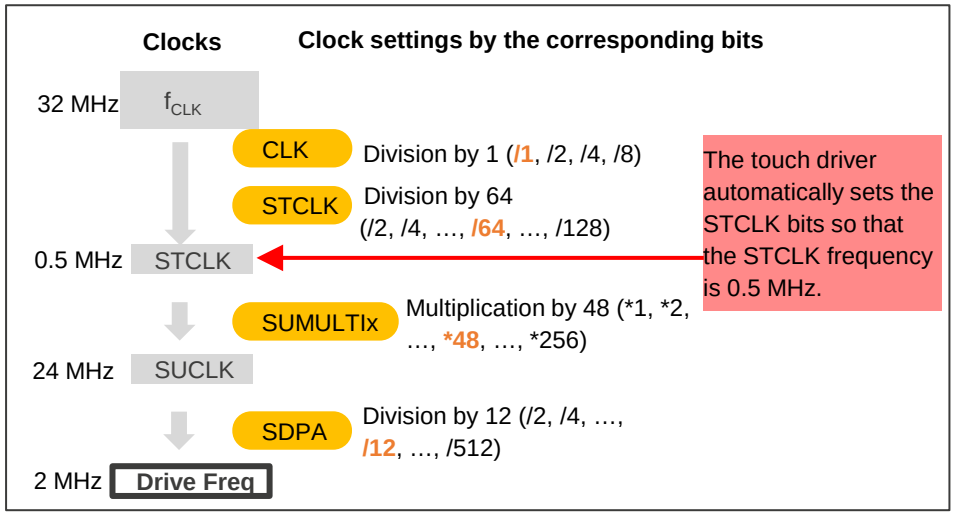
Use a V3.5.0 or later version of the QE tool to retune and re-evaluate your product

at the time of development/update/review of your product.

Appendix

[Appendix]
Sensor Drive Pulse Frequency

The following helps you understand the SUCLK and sensor drive pulse frequency settings.



The sensor drive pulse frequency is determined by the following expression.

Sensor drive pulse frequency = (f_{CLK} frequency/CLK/STCLK) × SUMULTIx/SDPA

= SUCLK/SDPA

CLK above refers to the CTSUCRAL.CLK[1:0] setting. f_{CLK} is frequency-divided by the value corresponding to this setting in setting the operating clock.

STCLK above refers to the CTSUCRAH.STCLK[5:0] setting. The operating clock is frequency-divided by the value corresponding to this setting in setting the state clock (STCLK).

SUMULTIx above refers to the CTSUSUCLK0 or CTSUSUCLK1.SUMULTIx[7:0] setting. STCLK is multiplied by the value corresponding to this setting in setting SUCLK.

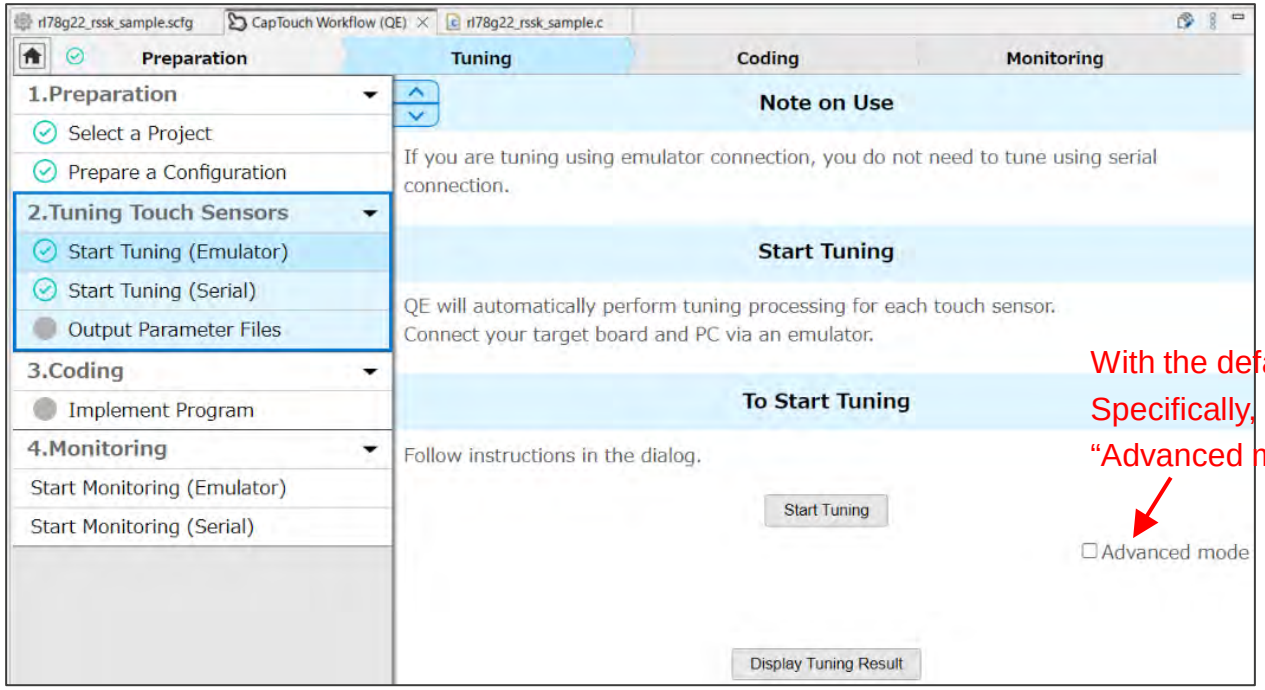
SDPA above refers to the CTSUSO1.SDPA[7:0] setting. SUCLK is frequency-divided by the value corresponding to this setting in setting the sensor drive pulse.
(If the setting of the CTSUSO1.SDPA[7:0] bits is n, the sensor drive pulse is obtained by frequency-dividing SUCLK by 2(n+1).)

[Appendix]
What Are the Default Settings?

■ Default settings

If you are using a V3.3.0 or earlier version of the QE tool with the default settings, tuning proceeds with a 32-MHz SUCLK, and the drive pulse frequency (measurement frequency) is selected from among 0.5 MHz, 1 MHz, 2 MHz, and 4 MHz.

The default settings stated in this document mean the settings with the advanced mode not in use in the QE window below.

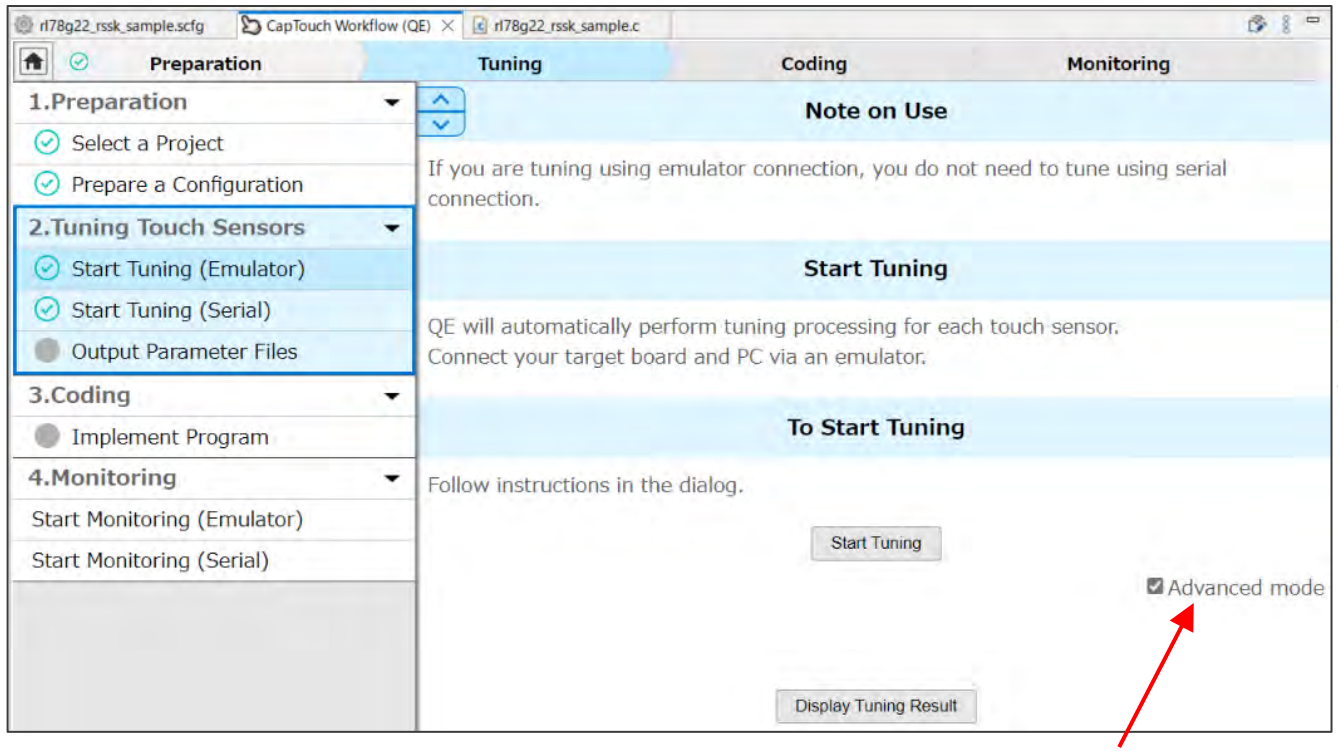


With the default settings, the advanced mode is not in use. Specifically, tuning (“Start Tuning”) is executed without checking “Advanced mode”.

[Appendix]
What Is the Advanced Mode of the QE Tool?

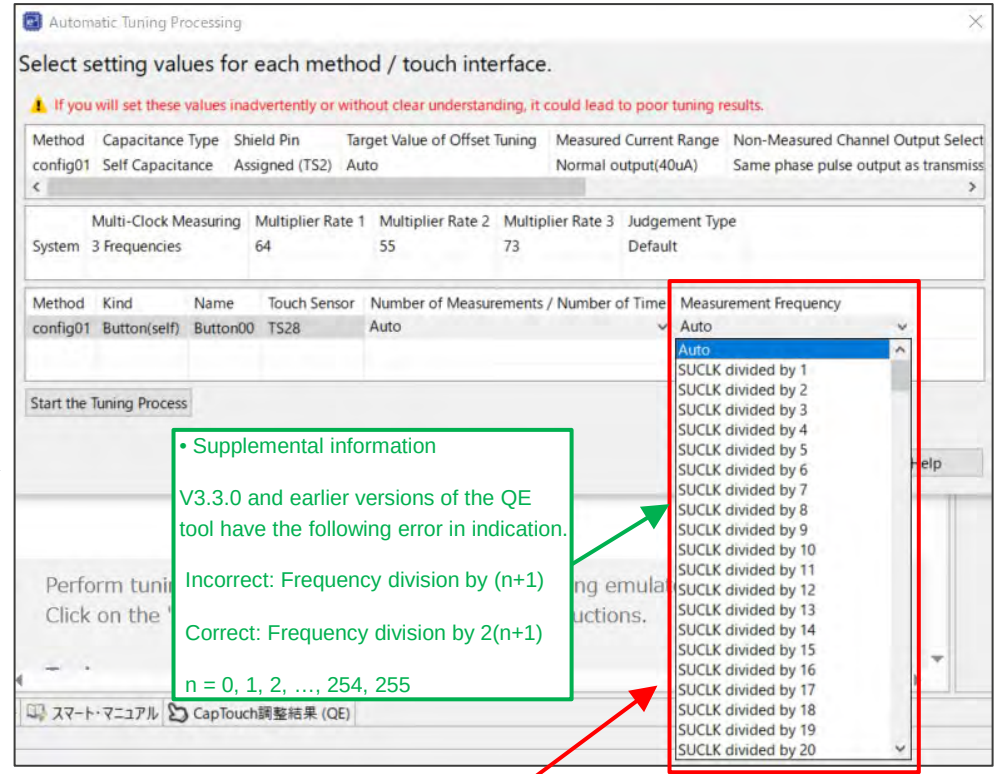
■ Advanced mode

Changing the drive pulse frequency in the advanced mode means changing the drive pulse frequency (measurement frequency) in the QE window as shown below on the right.



Check “Advanced mode” and execute tuning (“Start Tuning”).

The advanced mode setting window appears.



Setting for change to the drive pulse frequency (measurement frequency)

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