SLG4L41309

Reset IC

General Description

Silego SLG4L41309 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

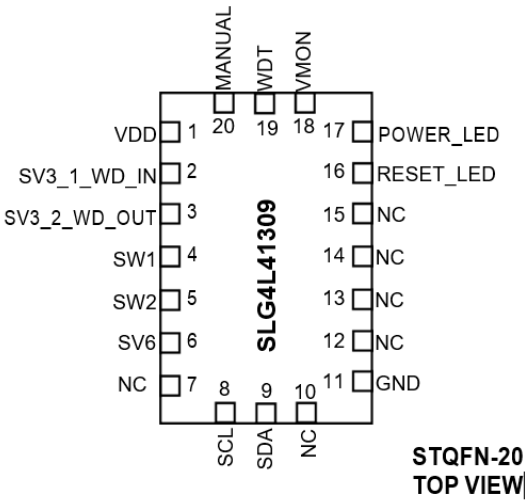
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

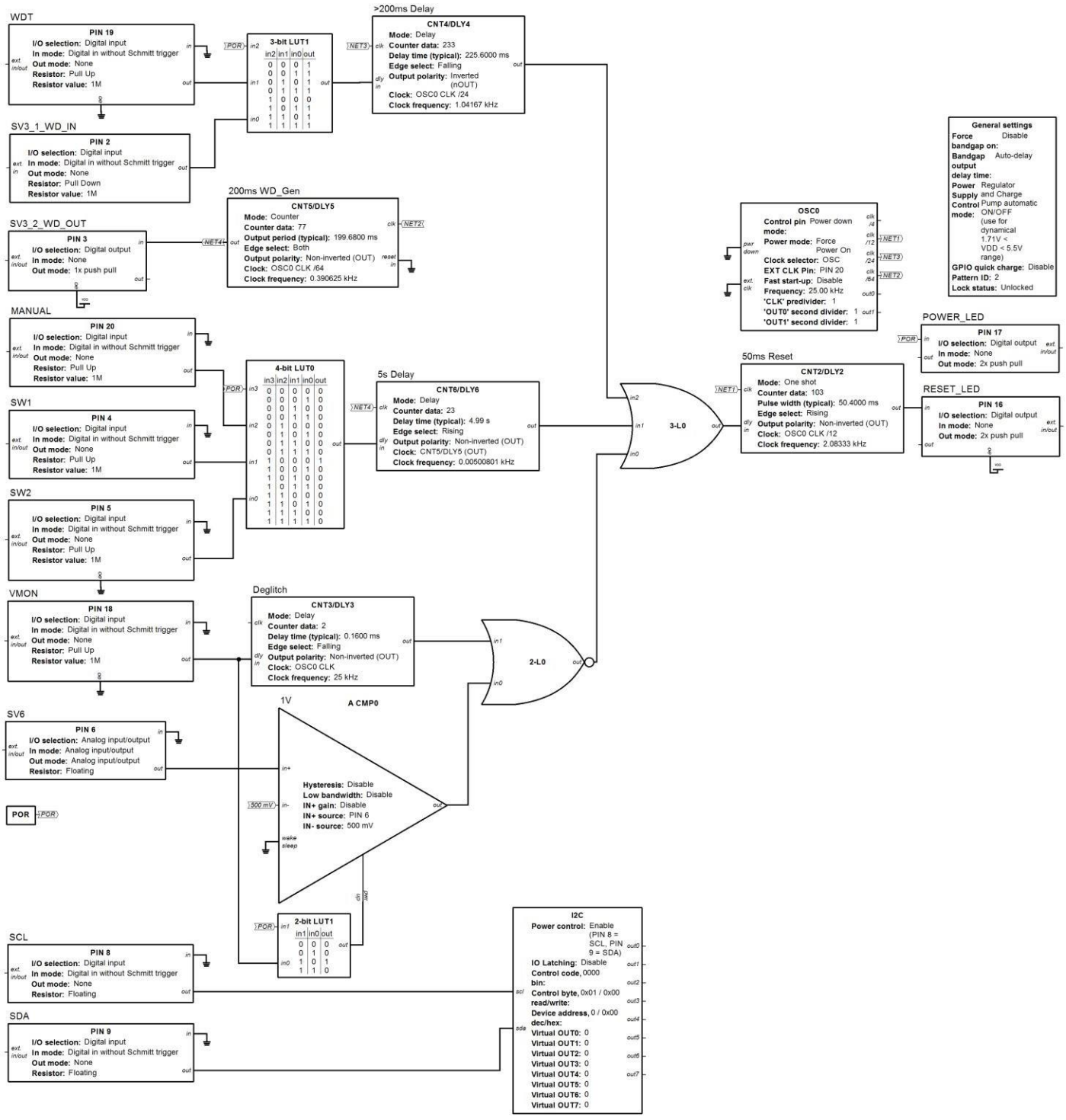
Output Summary

- 1 Output — Push Pull 1X
- 2 Outputs — Push Pull 2X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	SV3_1_WD_IN	Digital Input	Digital Input without Schmitt trigger
3	SV3_2_WD_OUT	Digital Output	Push Pull 1X
4	SW1	Digital Input	Digital Input without Schmitt trigger
5	SW2	Digital Input	Digital Input without Schmitt trigger
6	SV6	Analog Input/Output	Analog Input/Output
7	NC	--	Keep Floating or Connect to GND
8	SCL	Digital Input	Digital Input without Schmitt trigger
9	SDA	Digital Input	Digital Input without Schmitt trigger
10	NC	--	Keep Floating or Connect to GND
11	GND	GND	Ground
12	NC	--	Keep Floating or Connect to GND
13	NC	--	Keep Floating or Connect to GND
14	NC	--	Keep Floating or Connect to GND
15	NC	--	Keep Floating or Connect to GND
16	RESET_LED	Digital Output	Push Pull 2X
17	POWER_LED	Digital Output	Push Pull 2X
18	VMON	Digital Input	Digital Input without Schmitt trigger
19	WDT	Digital Input	Digital Input without Schmitt trigger
20	MANUAL	Digital Input	Digital Input without Schmitt trigger

Ordering Information

Part Number	Package Type
SLG4L41309V	V=STQFN-20
SLG4L41309VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.4	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs	--	8	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DC Current (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=5.0V	2.68	--	VDD	V
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=5.0V	0	--	1.96	V
I_{IH}	HIGH-Level Input Current	Logic Input PINs; V_{IN} = VDD	-1.0	--	1.0	µA
I_{IL}	LOW-Level Input Current	Logic Input PINs; V_{IN} = 0V	-1.0	--	1.0	µA
V_{OH}	HIGH-Level Output Voltage	Push Pull & PMOS OD, I_{OH} = 5mA, 1X Driver, at VDD=5.0 V	4.15	4.76	--	V
		Push Pull & PMOS OD, I_{OH} = 5mA, 2X Driver, at VDD=5.0 V	4.32	4.89	--	
V_{OL}	LOW-Level Output Voltage	Push Pull, I_{OL} = 5mA, 1X Driver, at VDD=5.0 V	--	0.19	0.24	V
		Push Pull, I_{OL} = 5mA, 2X Driver, at VDD=5.0 V	--	0.09	0.12	
I_{OH}	HIGH-Level Output Current	Push Pull & PMOS OD, V_{OH} = 2.4 V, 1X Driver, at VDD=5.0 V	22.08	34.04	--	mA
		Push Pull & PMOS OD, V_{OH} = 2.4 V, 2X Driver, at VDD=5.0 V	41.69	68.08	--	
I_{OL}	LOW-Level Output Current	Push Pull, V_{OL} = 0.4V, 1X Driver, at VDD=5.0 V	7.22	11.58	--	mA
		Push Pull, V_{OL} = 0.4V, 2X Driver, at VDD=5.0 V	13.83	23.16	--	
V_{ACMP0}	Analog Comparator0 Threshold Voltage	Low to High transition, at temperature 25°C.	--	500	--	mV

		Low to High transition, at temperature -40 +85°C (note 1)	--	500	--	
		High to Low transition, at temperature 25°C.	--	500	--	
		High to Low transition, at temperature -40 +85°C (note 1)	--	500	--	
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PINs 4, 5, 18, 19, 20	859	1097	1365	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	862	1097	1371	kΩ
T_{DLY2}	Delay2 Time	At temperature 25°C	--	50.38	--	ms
		At temperature -40°C +85°C (note 1)	--	50.49	--	
T_{DLY3}	Delay3 Time	At temperature 25°C	--	159.94	--	µs
		At temperature -40°C +85°C (note 1)	--	160.29	--	
T_{DLY4}	Delay4 Time	At temperature 25°C	--	225.51	--	ms
		At temperature -40°C +85°C (note 1)	--	226.01	--	
T_{DLY5}	Delay5 Time	At temperature 25°C	--	199.6	--	ms
		At temperature -40°C +85°C (note 1)	--	200.04	--	
T_{DLY6}	Delay6 Time	At temperature 25°C	--	4.99	--	s
		At temperature -40°C +85°C (note 1)	--	5	--	
T_{SU}	Start up Time	From VDD rising past 1.6 V	--	1	--	ms
F_{SCL}	Clock Frequency, SCL		--	--	400	kHz
t_{LOW}	Clock Pulse Width Low		800	--	--	ns
t_{HIGH}	Clock Pulse Width High		200	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)		--	--	168	ns
t_{AA}	Clock Low to Data Out Valid		--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	ns
t_{HD_STA}	Start Hold Time		448	--	--	ns
t_{SU_STA}	Start Set-up Time		5.8	--	--	ns
t_{HD_DAT}	Data Hold Time		0	--	--	ns
t_{SU_DAT}	Data Set-up Time		89	--	--	ns
t_R	Inputs Rise Time		--	--	300	ns
t_F	Inputs Fall Time		--	--	300	ns
t_{SU_STD}	Stop Set-up Time		9.1	--	--	ns
t_{DH}	Data Out Hold Time		444	--	--	ns
$t_{st\_out\_delay}$	State Machine Output Delay Time		67	--	275	ns
t_{st_out}	State Machine Output Transition Time		--	--	165	ns
t_{st_pulse}	State Machine Input Pulse Acceptance Time		9.2	--	--	ns
t_{st_comp}	State Machine Input Compete Time		--	--	29	ns

1. Guaranteed by Design

Chip address

HEX	BIN	DEC
0	0000000	0

Description

1.Design functionality
This design shows how using SLG46533 reset signal can be generated. Three reset modes are available: manual, voltage monitor, watchdog. For the first one, reset will be generated after 5s dual button press, the second one – when voltage on SV6 (PIN#6) is lower than 1V, third one – if there is no input signal on WD_IN (PIN#2) for longer than 200ms.Each reset mode can be activated by setting appropriate PIN (PIN#18 for voltage monitor, PIN#19 for watchdog and PIN#20 for manual reset) Low. There is an internal watchdog generator, which output can be connected directly to WD_IN (PIN#2) or external generator can be used. Reset pulse duration is 50ms, but it (and other delay's durations) canbe changed using I2C.

2.I2C Basic Command Structure
Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<xx:yy>.
The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of thedata to be read ("1") or written ("0") by the command. This Control Byte will be followed by an Acknowledge bit (ACK). With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specificdata byte to be read or written in the command. Figure 1 shows this basic command structure.

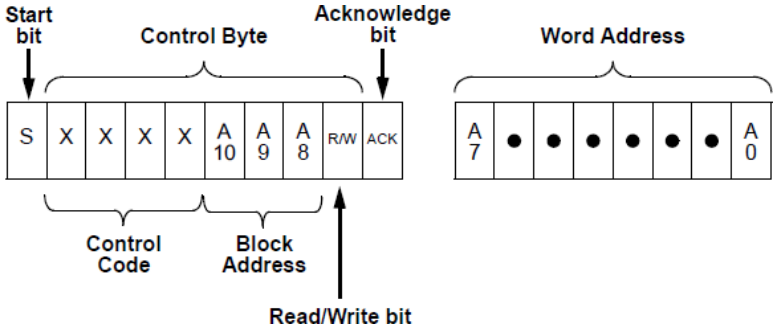


Figure 1. I2C Basic Command Structure

3.I2C Serial General Timing
Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

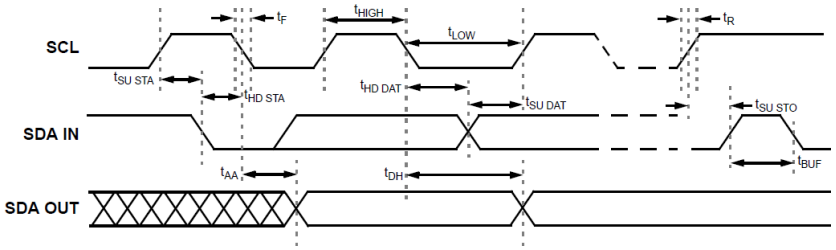


Figure 2. I2C Serial General Timing

4.I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to“0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledgebit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG46533 to the correct data byte to be written. After the SLG46533 sends another Acknowledgebit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG46533 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46533 generates the Acknowledge bit.

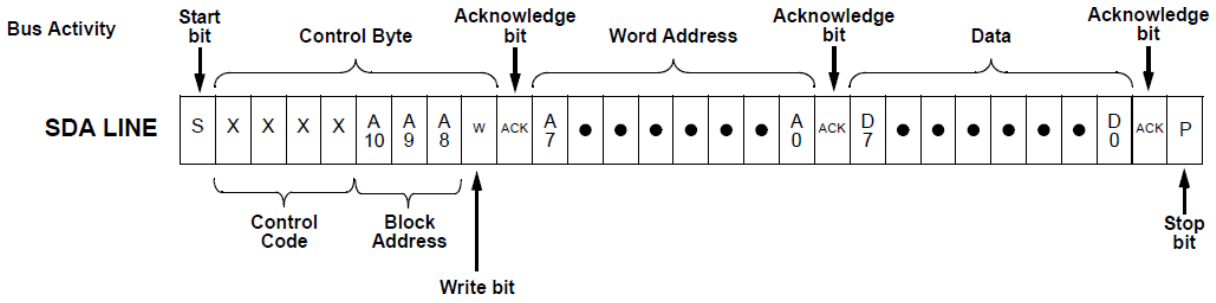


Figure 3. I2C Write Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the sameas the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46533 issues an Acknowledge bit, followed by the requested eight data bits.

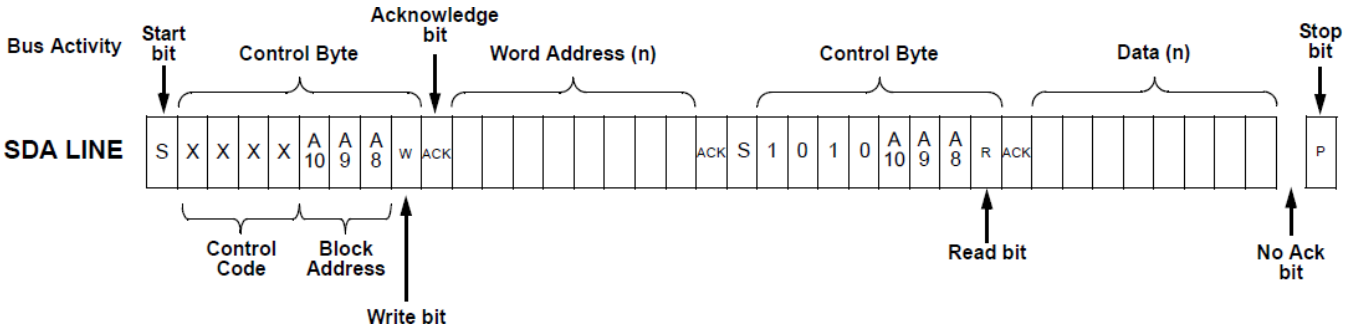
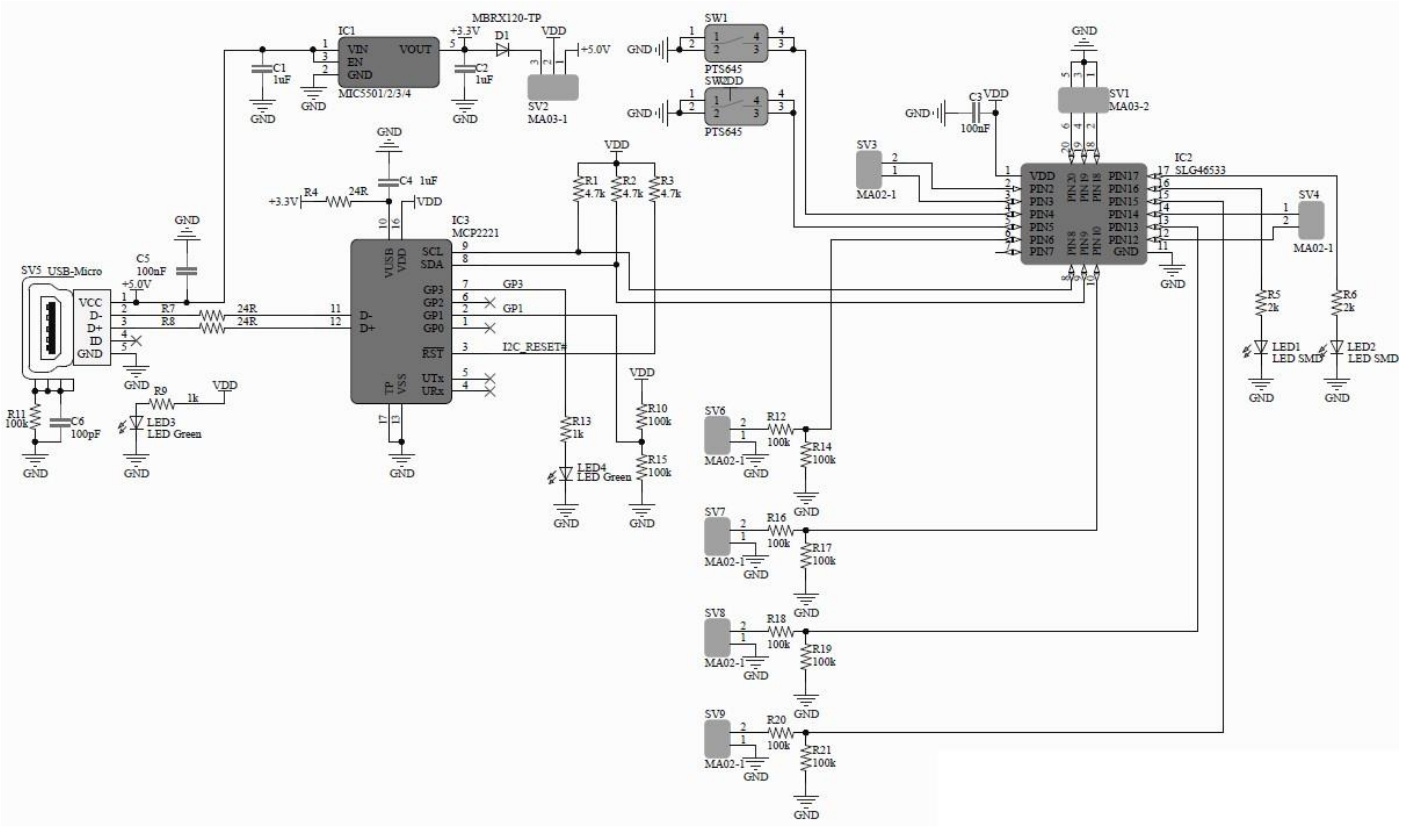


Figure 4. I2C Random Read Command

5.CNT/DLY Settings

Address Byte	Register Bit	Block	Function	Range
0xC0	reg<1543:1536>	DLY2	Counter data from 1 to 255 (default setting is 103)	0x01 to 0xFF (1 = 1.44ms; 103 = 50.4ms; 255 = 123.36ms)
0xC2	reg<1559:1552>	DLY4	Counter data from 1 to 255 (default setting is 233)	0x01 to 0xFF (1 = 2.88ms; 233 = 225.6ms; 255 = 246.72ms)
0xC3	reg<1567:1560>	CNT5	Counter data from 1 to 255 (default setting is 77)	0x01 to 0xFF (1 = 5.12ms; 77 = 199.68ms; 255 = 655.36ms)
0xC4	reg<1575:1568>	DLY6	Counter data from 1 to 255 (default setting is 23)	0x01 to 0xFF (1 = 599.04ms; 23 = 4.99s; 255 = 51.32s)

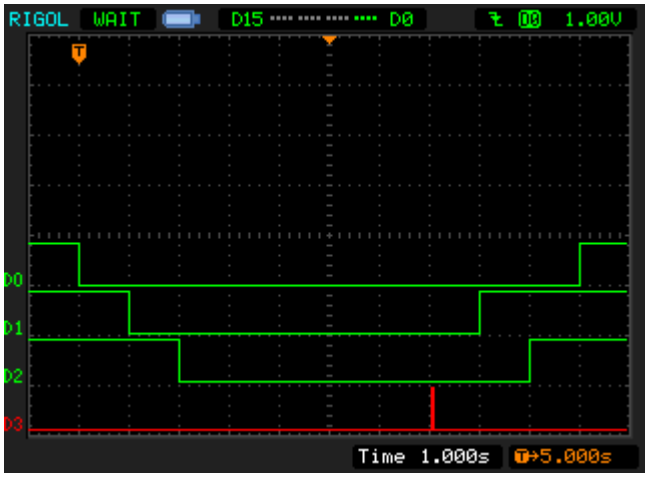
Typical Application Circuit



Functionality Waveforms

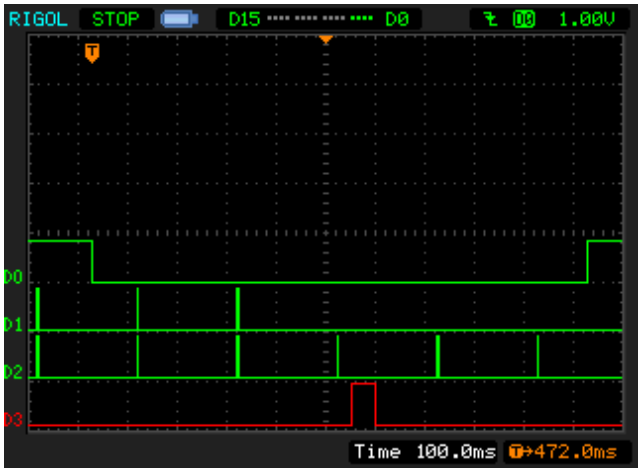
D0 – PIN#20 (MANUAL) D1 – PIN#4 (SW1)
D2 – PIN#5 (SW2)
D3 – PIN#16 (RESET_LED)

1. Manual reset functional diagram



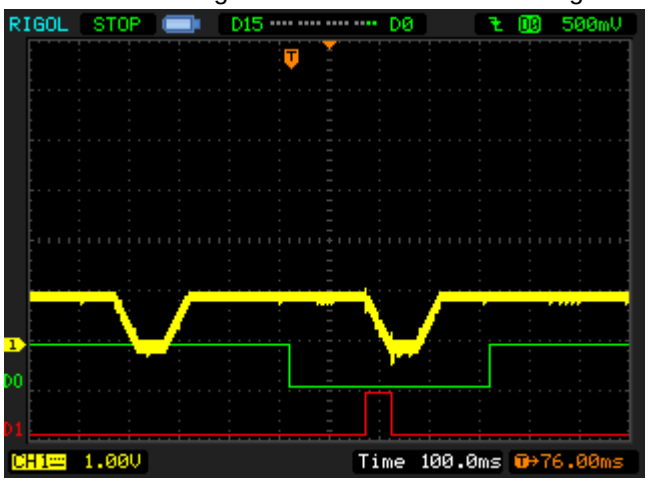
D0 – PIN#19 (WDT)
D1 – PIN#2 (WD_IN)
D2 – PIN#3 (WD_OUT)
D3 – PIN#16 (RESET_LED)

2. Watch dog reset functional diagram



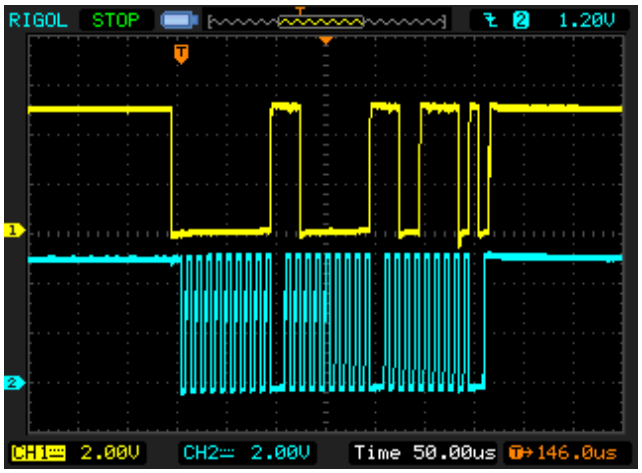
Channel 1 (yellow line) – PIN#6 (SDA)
D0 – PIN#18 (VMON)
D1 – PIN#16 (RESET_LED)

3.Voltage monitor reset functional diagram

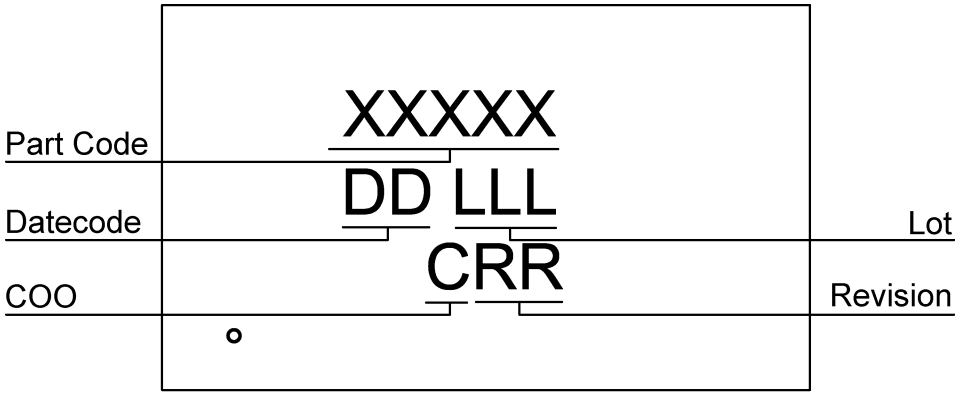


Channel 1 (yellow/top line) – PIN#9 (SDA)
Channel 2 (light blue/2nd line) – PIN#8 (SCL)

4.I2C write command (changing DLY2 counter data to 207, equal to 100 ms)



Package Top Marking



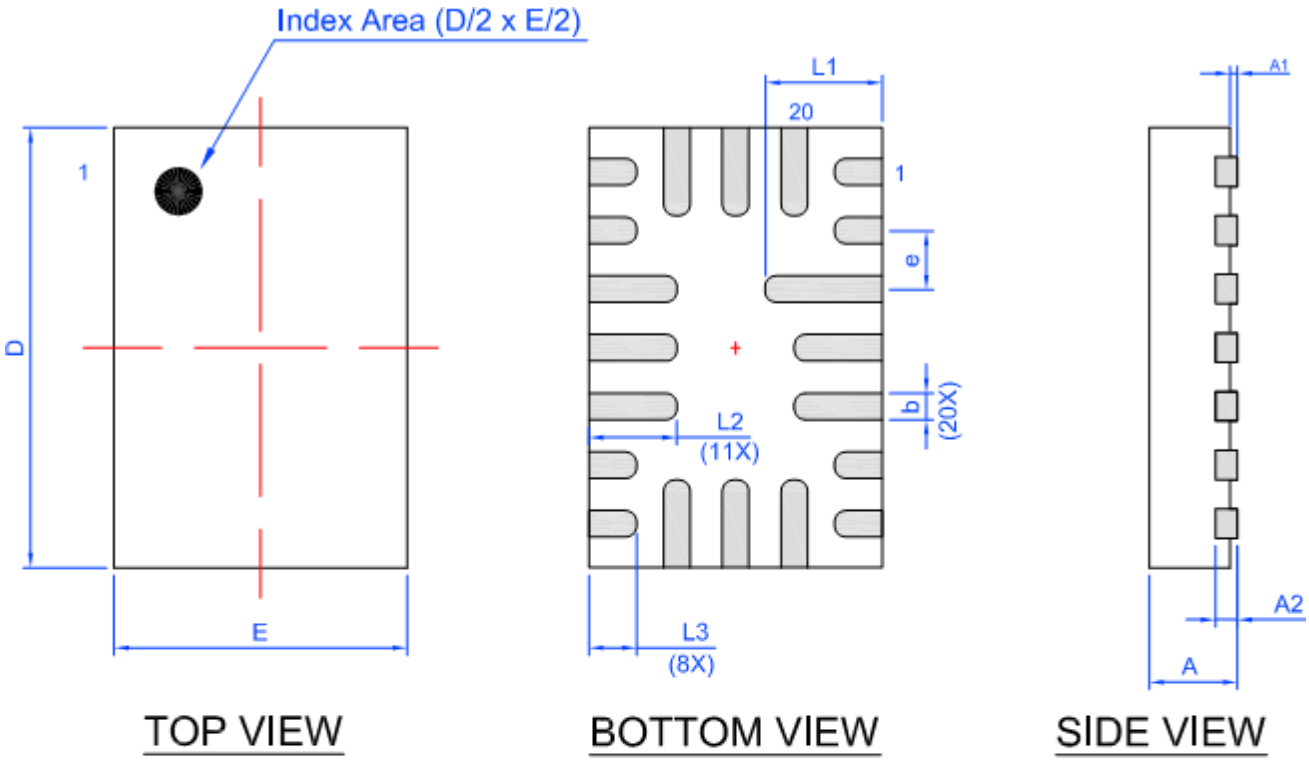
XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.10	002	U			06/29/2016

The IC security bit is locked/set for code security for production unless otherwise specified. Revisionnumber is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.015 g



TOP VIEW BOTTOM VIEW SIDE VIEW

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

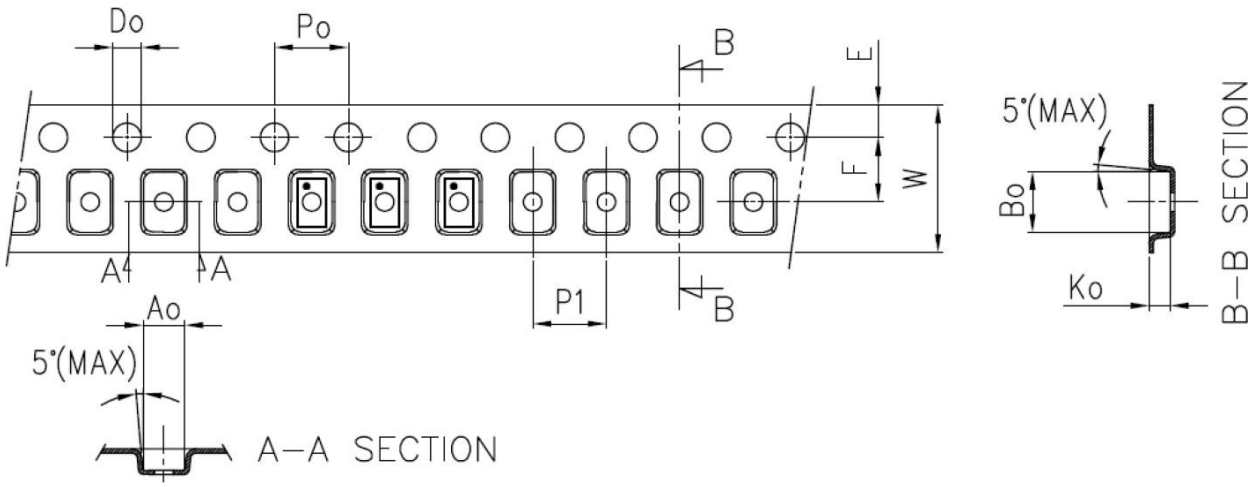
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).More information can be found at www.jedec.org.

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