QSpan II™ Debug Checklist

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6024 Silver Creek Valley Road San Jose, California 95138
Telephone: (408) 284-8200 • FAX: (408) 284-3572
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About this Document

This document describes some of the common issues customers experience when debugging boards configured with a QSpan II. The following issues are discussed:

1. Clocks

1.1 PCLK and QCLK Signals

Are PCLK and QCLK available? The PCI clock is usually available. The QBus clock must be generated.

1.1.1 Quality of Clocks

Check the quality of the clocks on an oscilloscope for jitters or skew. If there is a clock buffer in the design, then what skew will it bring to the clocks? If the design is using a Motorola 360 the design may have CLK01(clkout) from the 360 connected to the CLK input of the QSpan II, this connection could cause jitter. The clock skew of this clock must be a zero clock skew (skew < 1ns). Motorola has advised not to use the clkout of the 360 to clock the clkin of another 360. Because this will cause the clkout of the second 360 to have a substantial amount of jitter.

1.1.2 Frequency Change

Is there a change in the clock frequency during operation? If yes, is the code in section C2.1.1 implemented. If the clock speed is going to be changed during operation, the code on page 373 of the *QSpan II PCI-to-Motorola Processor Bridge Manual* must be implemented. This code inserts delay so the QSpan II can receive a stable QCLK before external bus cycles begin.

1.2 Reset

1.2.1 TMODE Signals

Check TMODE[1:0] and make sure they are 00, as per Table 49 of *QSpan II PCI-to-Motorola Processor Bridge Manual*. These two bits must be checked immediately after the device comes out of reset.

1.2.2 BDIP_ and SIZ[1]

Check BDIP_ and SIZ[1] and make sure they are the appropriate mode for the processor, as per Table 48 in *QSpan II PCI-to-Motorola Processor Bridge Manual*. These bits are pulled to the appropriate mode through the use of pull-ups and pull-downs on the board. The table resides on page 162 of the manual.

1.2.2.1 TA_, TEA_, and TRETRY_ Asserted

For the MC68040 mode, TA_, TEA_, and TRETRY_ will assert at the same time to retry, so this is a typical behavior to identify the mode. If these signals get asserted as defined, and the MC68040 processor is not being used, the QSpan II is coming out of reset in the wrong mode.

1.3 Access to QSpan II Registers Using MPC860

1.3.1 Chip Selects

How are the chip selects generated? Check BR and OR registers of the processor to make sure they are correct, including SEME and SETA. Sections C2.1.3 and C2.1.14 of the *QSpan II PCI-to-Motorola Processor Bridge Manual* gives an explanation of these settings.

1.3.2 Burst Access

The QSpan II registers do not allow burst access; therefore, BIH should be set. This bit is set in the MPC860. For more information, see section C2.1.14 of the *QSpan II PCI-to-Motorola Processor Bridge Manual*.

1.3.3 MLRC

The MLRC bits in the MPC860's SIUMCR register should be 10. For more information, see section C.2.1.14 of the *QSpan II PCI-to-Motorola Processor Bridge Manual*.

1.4 EEPROM (Optional)

1.4.1 EEPROM Used

Is a EEPROM used to program QSpan II registers at system reset? If not, then both ENID_ and SDA should be pulled low. These signals are located on the QSpan II and are defined on page 181 of the manual.

1.4.2 PCI_DIS Signal

PCI_DIS is normally pulled high for EEPROM loading. At the end of EEPROM loading, is this bit cleared to allow PCI access? Make sure this bit is cleared upon loading. This bit must be cleared before any PCI target accesses will complete successfully.

1.4.3 Check EEPROM Contents

Check the contents of the EEPROM before using. The EEPROM must be programmed. If necessary the EEPROM can be programmed by writing to EEPROM_CS at register offset 0x804. The process is explained in detail on page 133 of the manual, 2 steps.

1.5 PCI Configuration Cycles (Optional)

1.5.1 CON_ADD and CON_DATA Registers

PCI configuration cycles are generated by writing to or reading from the CON_ADD and CON_DATA registers at offsets 0x500 and 0x504.

1.5.2 IDSEL Signal

IDSEL of the PCI target should be connected to the proper address line AD[31:11] for type 0 configuration reads and writes. See the *PCI Local Bus Specification Revision 2.2* for type 1 transactions.

1.5.3 Disabling a PCI Master-Abort

To disable a PCI Master-Abort from mapping the termination to the QBus as a bus error, the MA_BE_D bit should be set. This bit is located in the MISC_CTL register at offset 0x800. When this bit is set if the QSpan II receives a PCI Master-Abort it maps this as a normal termination on the QBus.

1.5.4 Configuration Write and MAX_RTRY Bit

Configuration write does not work with MAX_RTRY set in the MISC_CTRL2 register at offset 0x802. Check the web site for the QSpan II errata. The MAX_RTRY bits must be programmed to 00.

CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
email: EHBhelp@idt.com
phone: 408-360-1538
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