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Renesas Electronics Corporation

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Low-Voltage CMOS Logic HD74LV_A/LVC Series

Precautions in System Design

1. Unused Inputs

The extremely high input impedance of the HD74LV-A/LVC/LVC-A series makes it subject to noise when used with an input open and the under fired input level causes the output logic level to be unstable.

Unused inputs must be connected to V_{CC} or GND.

Furthermore, in some cases if another gate or flip-flop in a package is not used, both p-channel MOS and n-channel MOS may conduct causing I_{CC} to flow. The same attention must be paid.

2. Output Short-Circuit

Since no protective circuitry is provided to limit the output current, an output inadvertently shorted to V_{CC} or GND on the HD74LV-A/LVC/LVC-A series IC is limited to the current determined by the pinch-off effect of the p-channel MOS and n-channel MOS for the output. Notice that such output short-circuit current, if allowed to flow for a long time, could result in increased power dissipation or in a melted wire due to excessive current density through metallization or other performance failures. For operating stability and reliability, the maximum output current should remain within the maximum rating.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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