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Low-Voltage CMOS Logic HD74LV_A/LVC Series

Application Note

1. Introduction

Notebook PCs, cellular telephones, and other portable information devices are rapidly becoming household items, and processing speeds are steadily rising. There is a need for standard logic ICs that can operate at high speeds and low voltages, with low power dissipation.

We have 3 families for 3 V operation standard logic IC's, ALVC, LVC/LVC-A and LV-A series. These families are capable of high-speed operation at 3.3 V, and like other CMOS devices, it consumes little power. This application note describes circuit characteristics of the LVC/LVC-A Series, and gives some board design guidelines. It has been written to help product designers use the performance of the LVC/LVC-A Series to reduce the voltage and power requirements of their systems.

2. Product Status

To meet the needs of a wide range of applications, Renesas has developed three families of 3-V standard logic. The ALVC Series is intended for ultra high-speed systems. The LVC/LVC-A Series is designed for high-speed systems requiring low power dissipation. The LV-A Series is for medium-speed, low-power systems.

Availability of these series is enhanced by a technology agreement with Texas Instruments Inc., which produces devices with the same specifications.

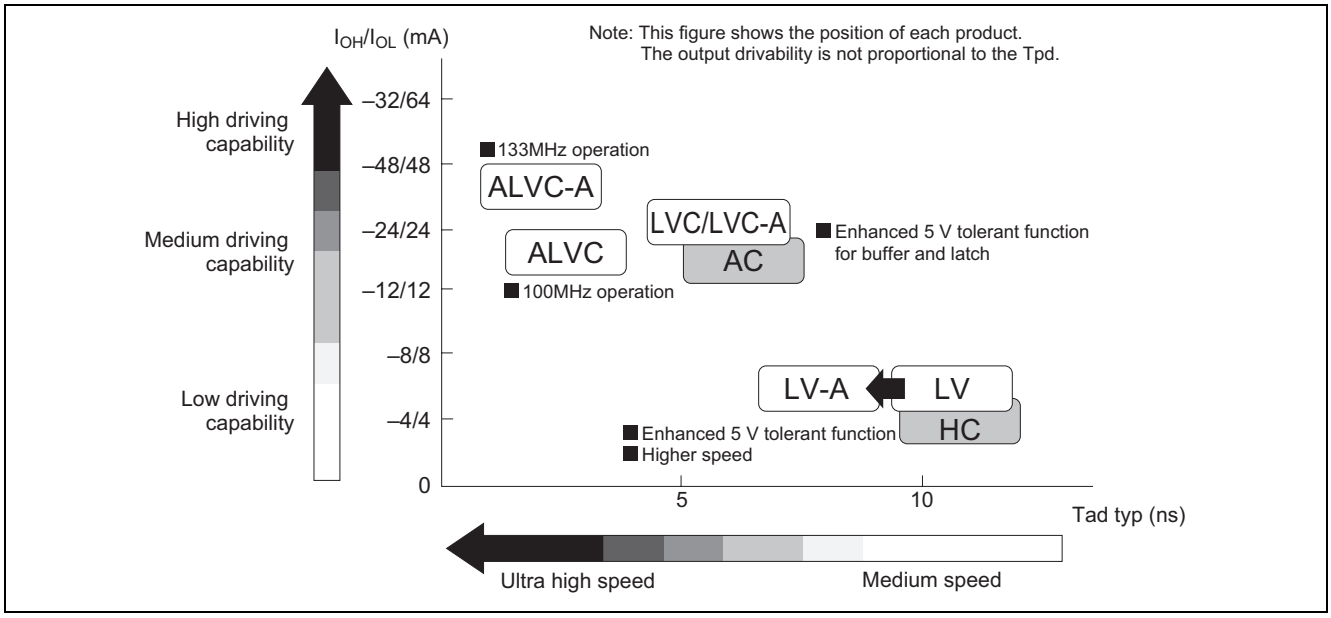


Figure 2-1 Low-Voltage Standard Logic Families

3. Performance and Features

Propagation delays increase dramatically when conventional CMOS logic, designed to operate at 5 V, is driven at a lower voltage. In battery-powered products, conventional CMOS logic is also a source of battery drain, because of current paths leading from input pins through diodes to power-supply pins. The Low voltage Series was designed to avoid these disadvantages of conventional CMOS logic and meet the following targets for low-voltage, low-power operation.

3.1 Performance and Features of Low-Voltage Standard Logic

3.1.1 Performance

- High-speed switching characteristics at low voltage
  - ALVC = 2.0 ns typ, LVC: Typical 5 ns, LV-A: 5.4 ns typ permitting high-speed operation
- High drive current
  - High output sink/source current: ALVC/LVC maximum ±24 mA; LV-A maximum ±8 mA
- Wide operating voltage
  - LVC/LVC-A series guarantees the electrical characteristics at V_{CC} = 3.3 V, 5 V and LV-A series at V_{CC} = 2.5 V, 3.3 V and 5 V. Such wide voltage range operation is possible.

3.1.2 Features

- Reduced output noise
  - V_{OLP} (output ground bounce) < 0.8 V (typical) [V_{CC} = 3.3 V, Ta = 25°C]
  - V_{OHV} (output V_{OH} undershoot) > 2 V (typical) [V_{CC} = 3.3 V, Ta = 25°C]

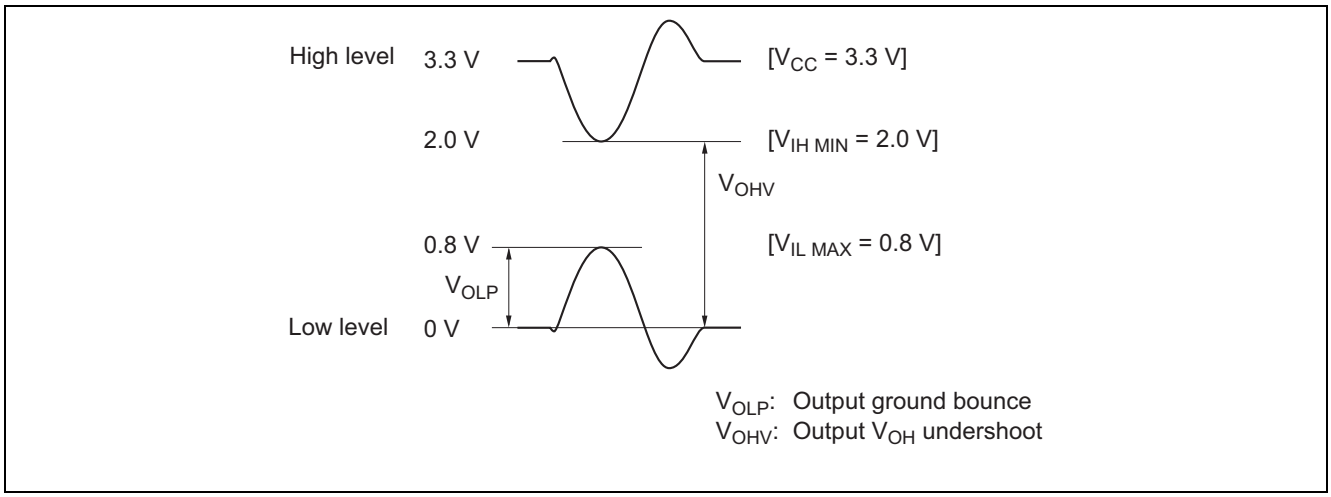


Figure 3-1 Output Noise Waveforms and Symbols

- Prevention of input current leakage when power is off [LV-A, LVC/LVC-A series]
  - Prevention of current leakage by improved input protection circuits
- Direct interface to 5-V devices [LV-A, LVC/LVC-A series]
  - Input voltage guaranteed up to 5.5 V, enabling signals from 5-V devices to be input directly during 3-V operation
- Line-up of small surface-mount packages
  - Small surface-mount packages (SOP, TSSOP) for high-density mounting

3.2 The Products to Prevent the Reflection Noise [ALVC, LVC-A]

Reflection always occurs at signal transmission paths. It causes noise to electronic devices. One of the technique to prevent the reflection noise is damping resistors.

The ALVC and LVC-A series has line-up with internal damping resistors. This damping resistors is for 50 Ω signal transmission path. Reflection noise detail is shown in 5.4

3.3 Internal Bus Hold Circuit [ALVCH]

Since the CMOS Structure is high input impedance, in case that not fixed input level voltage is given to the input or the input is not used, input should be fixed with pull-up/pull-down resistor. Bus hold circuit is like the latch circuit is put at input pin. It fixes the input level 'high' or 'low' according to the former input level. Since the level of the bus hold circuit varies due to the input level, this can be used for short time latch circuit.

3.4 The product for Hot Insertion [LVCZ]

Hot insertion means that the sub board may be taken out or inserted during the power-on status of the main system. To cope with this status, the output needs to be stable even though the V_{CC} may get lower than a certain voltage level. The representative of this application is the switch box. In the switch box application, the hot insertion may occur daily. If the stable operation is not maintained, the telephone line may get in trouble.

The TTL standard specifies the low level signal $V_{IL(max)}$ = 0.8 V, and the CMOS 5 V standard specifies the $V_{IL(max)}$ = 1.5 V.

Generally CMOS starts operation at around 0.8 V. The IC with V_{CC} = 0.8 V can output 'high' level signal up to 0.8 V. From the bus, 0.8 V is recognized as 'low' level. So, the output level should keep high impedance when being pulled-up before the V_{CC} level becomes 1.5 V.

LVCZ series output maintains high impedance level when V_{CC} is lower than 2.0 V (typ).

4. Characteristics of Input and Output Circuit

4.1 Equivalent Circuit of Input and Output

The input circuits of conventional CMOS logic have diodes for protection against electrostatic discharge, so when the logic device is powered off, if a high logic level is received at an input:

- Current will flow from the protection diode to the power-supply, causing unanticipated power dissipation.
- Coupling of the high logic-level voltage to the power-supply will cause the IC to operate and the system to malfunction.

In the LV-A and LVC/LVC-A Series, the input circuits have been improved to avoid these problems of current leakage in the power-off state. An additional result is that the input voltage rating is not dependent upon the power supply voltage, enabling the input pins to accept a maximum voltage of 5.5 V.

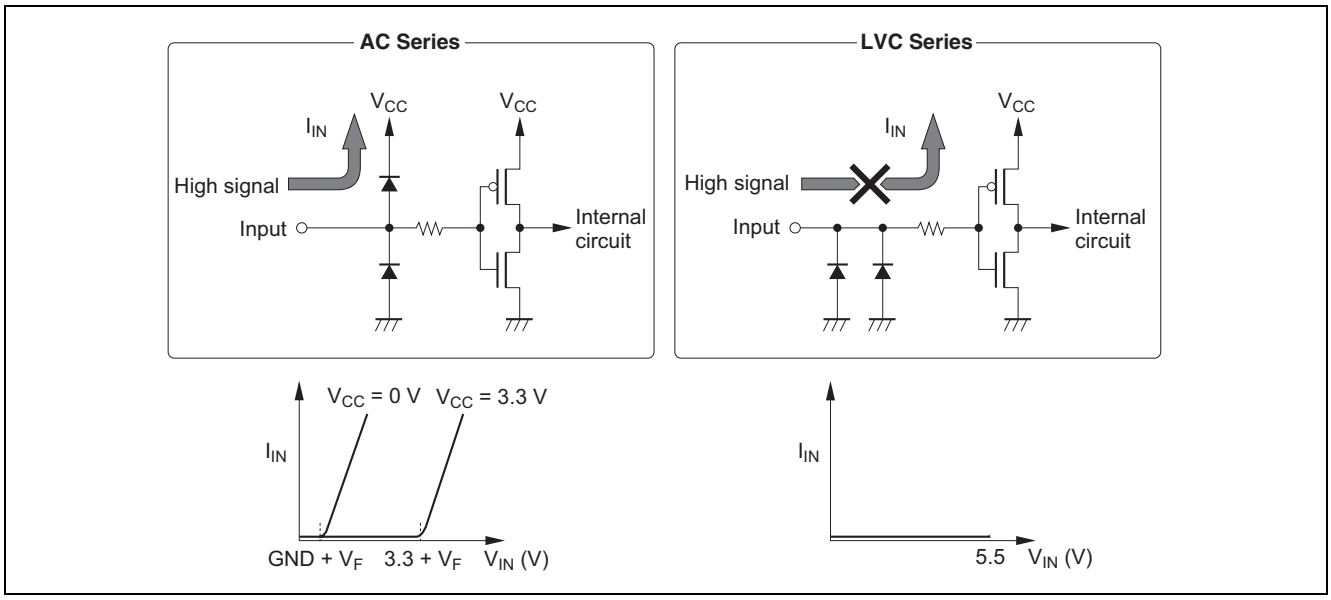


Figure 4-1 Input Protection Circuits of LV-A and LVC/LVC-A Series (Prevention of Current Leakage)

However, in case of the common terminal with input and output, the parasitic diode must be considered. CMOS output has the parasitic diode at V_{CC} side. Therefore, the terminal can be applied with the voltage up to V_{CC}.

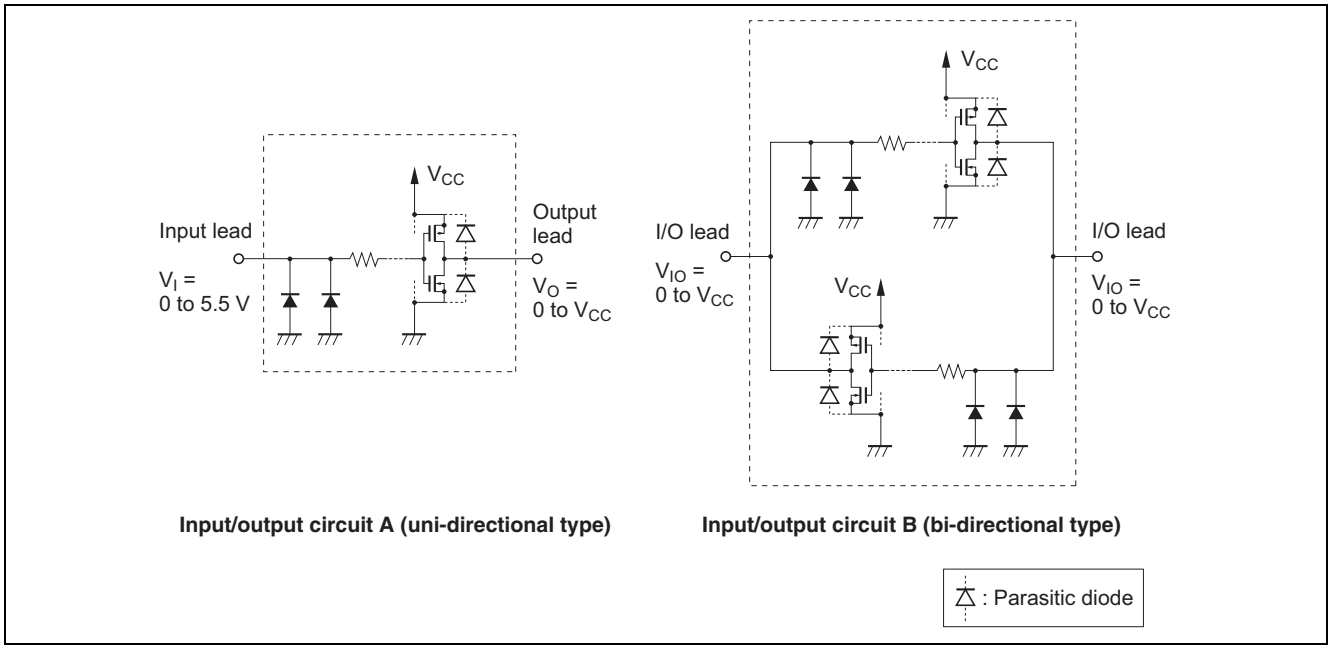


Figure 4-2 LV-A and LVC Series Input/Output Circuits

In the LVC-A version and LV-A version, the output circuit has also been improved, enabling 5 V tolerance from the input/output pins when output is disabled. As a result, 3 V to 5 V bi-directional TTL level conversion is now easily achieved with HD74LVC245A, etc..

In addition, this version is suitable for power management due to the fact that there is no leakage from either input or output pins at V_{CC} = 0 V.

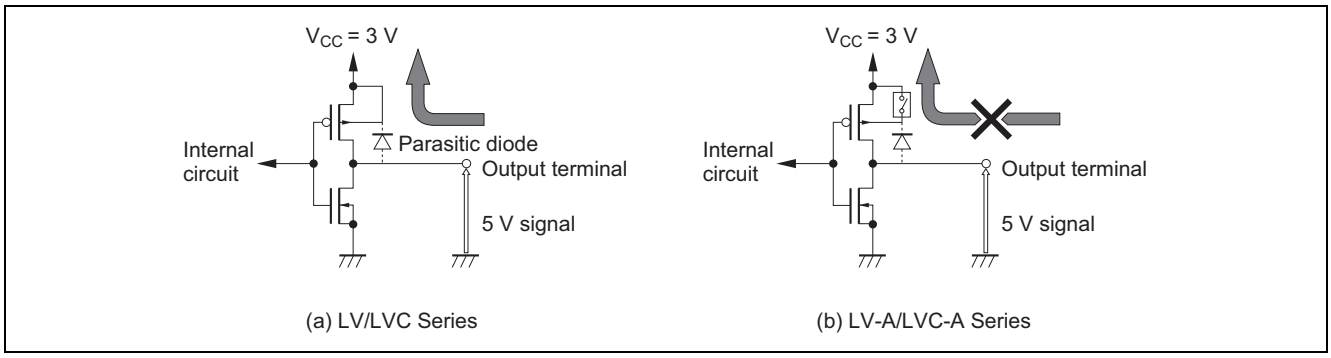


Figure 4-3 LVC-A and LV-A Series Output Circuit

The internal switch at output show in figure 4.3 prevents the current leakage. The switch becomes 'off' and prevents the current leakage,

- when the output is high impedance
- when V_{CC} is 0 V

4.2 Interface from/to 5-V Devices

LV-A and LVC/LVC-A series at V_{CC} = 3 V can interface with 5 V device, under a certain conditions.

4.2.1 Interface from 5-V Driver to 3-V Receiver

Signals from 5-V systems can be input directly, to LV-A and LVC/LVC-A series input.

When the output is applied with 5 V signal:

a) Buffer
LV-A and LVC-A can prevent the current leakage by disabling the output using OE, DIR terminal. There is no current leakage at V_{CC} = 0 V.

b) Gate
LV-A and LVC-A series can prevent the current leakage when power-supply is 0 V.

4.2.2 Interface from 3-V Driver to 5-V Receiver

When an LV-A and LVC/LVC-A output is received by a 5-V device, the device used must have TTL input levels. With a CMOS device, the LV-A and LVC/LVC-A output (V_{OH} = 2.4 V when V_{CC} = 3.0 V) would not reach the minimum valid high input level (V_{IH} = 3.5 V minimum), as shown in figure 4-4.

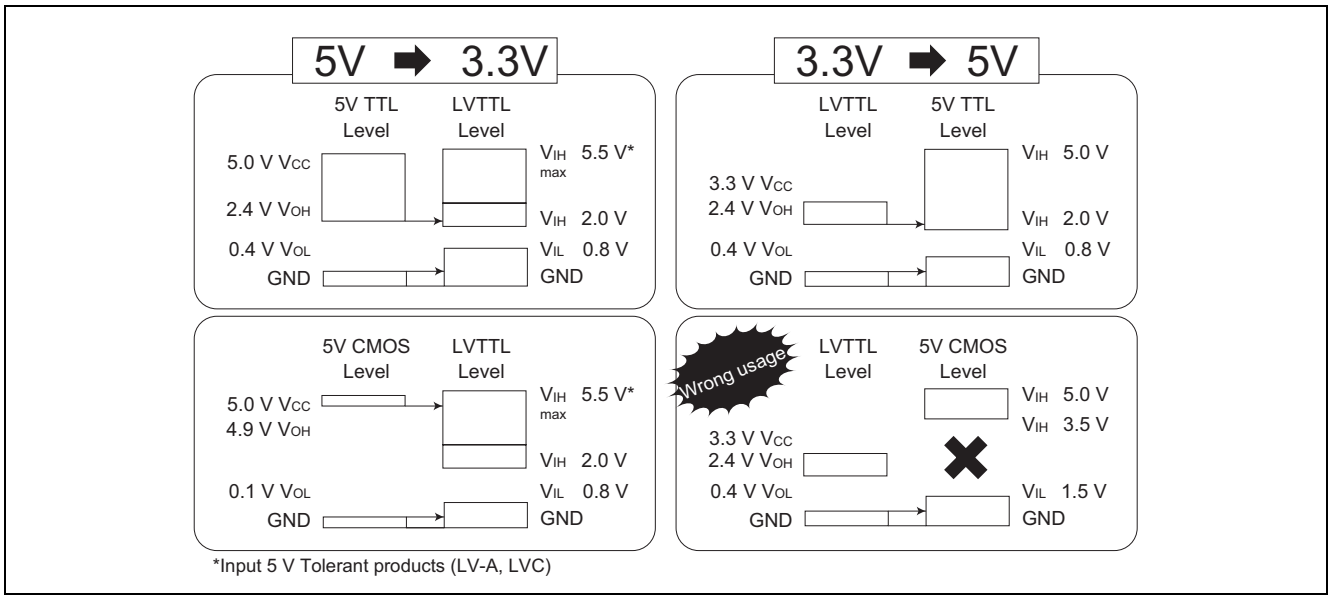


Figure 4-4 Comparison of 3.3-V and 5-V Voltage Levels

In this case, please use HD74HCT and ACT series which have TTL input level.

One possible solution in this situation is to pull up the output, but this solution cannot be recommended expect open drain output product (HD74LV05A, 06A and 07A). Because in other products current will flow through the output MOS gate to V_{CC} of IC. When CMOS outputs 'high' level signal, the output terminal and V_{CC} is connected.

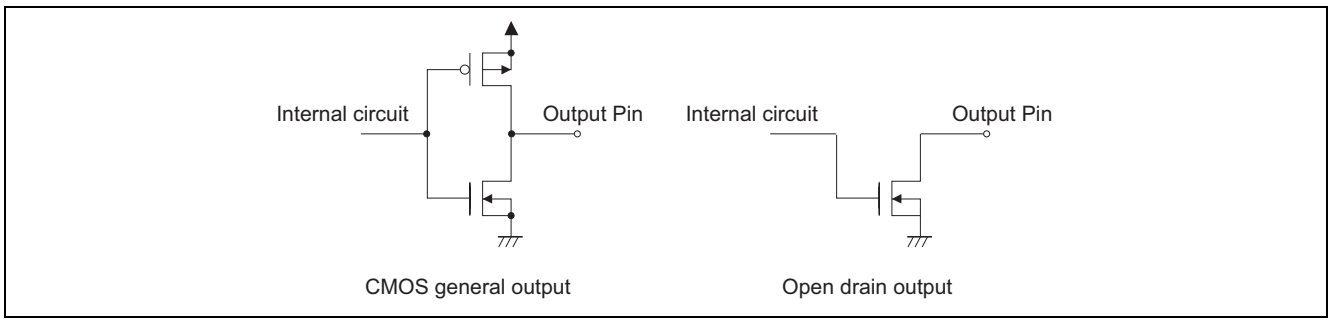


Figure 4-5 The difference in output structure between general CMOS and open drain

In other words, to pull-up the output with 5 V, 3.3 V V_{CC} is pulled-up with 5 V. The IC itself may not destroy by applying 5 V to the output.

4.2.3 Interface to Bi-directional Device (3 V to 5 V, 5 V to 3 V)

LV-A and LVC-A series can operate at V_{CC} = 5 V and can receive 5 V level signal during operation at V_{CC} = 3.3 V. However, in case of bi-directional interface with 5 V device, there is some restriction in usage regarding the output 5 V tolerant function.

For bi-directional interface,

a) To the LSI with V_{CC} = 3.3 V:
   Receives 5 V signal and transmits 3.3 V signal.
b) To the LSI with V_{CC} = 5 V:
   Receives 3.3 V signal and transmits 5 V TTL level signal.

This is basic idea. In order to transmit 3.3 V signal, the V_{CC} should be 3.3 V. In this case, 5 V CMOS ($V_{IH(min)}$ = 3.5 V) cannot be satisfied. This level can meet 5 V TTL signal ($V_{IH(min)}$ = 2.0 V). Therefore, the 5 V CMOS level bi-directional interface is not possible. However, the 5 V TTL level bi-directional interface is possible.

One possible solution in this situation is to pull up the output, but this solution is not recommended.

The output tolerant function prevents the current leakage

- When output is high impedance
- When V_{CC} is 0 V

When the output is enabled, the voltage higher than the V_{CC} cannot be applied to the output. As explained in 4.2.2, because the current flows through the output MOS gate. The IC itself may not destroy by applying 5 V when the output is enabled.

The level shifter, HD151015, which enables the bi-directional interface between 5 V CMOS level and 3.3 V, is also available.

Figure 4-6 shows whether the interface is possible or not, regarding the 3.3 V and 5 V combination.

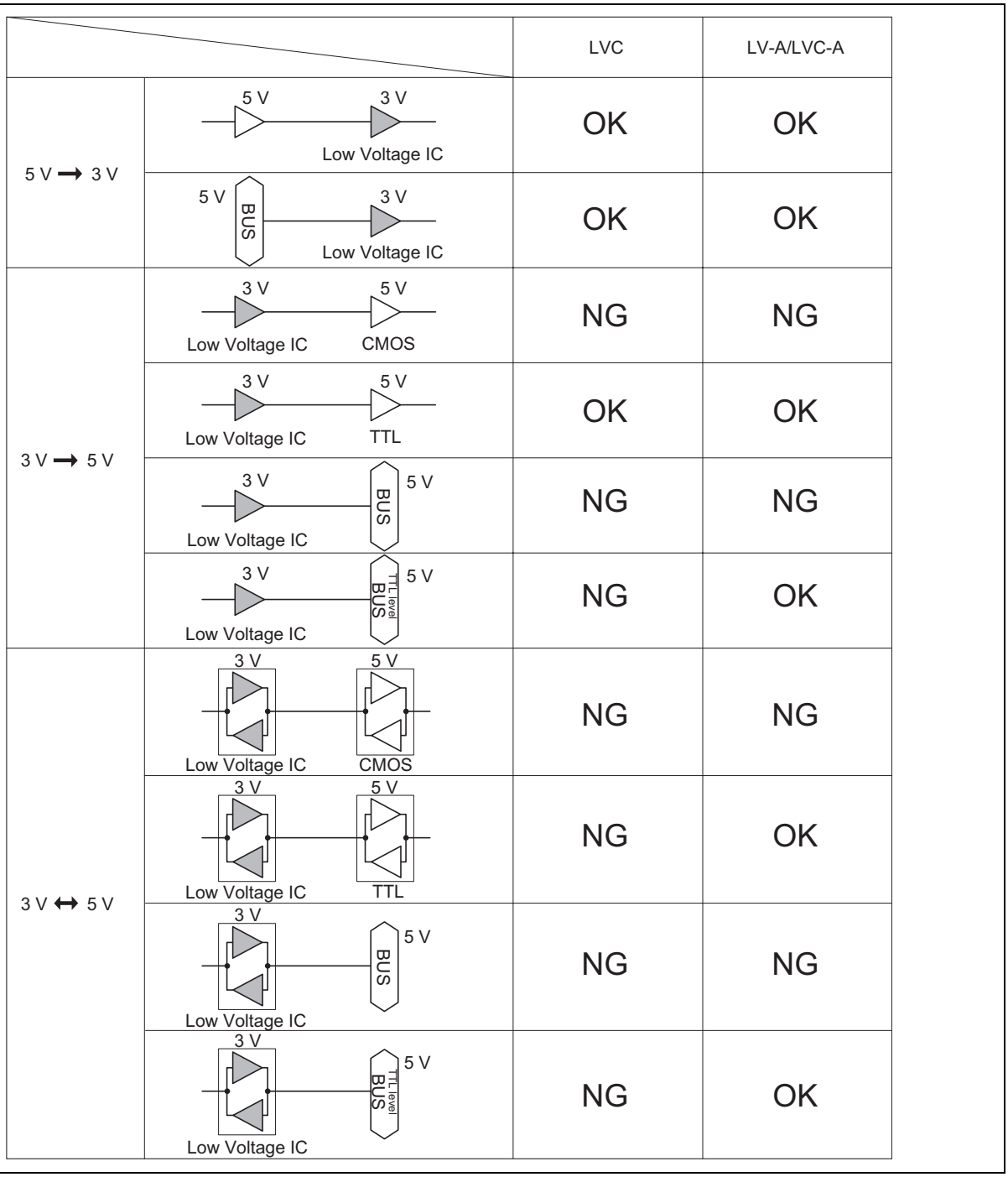


Figure 4-6 Examples of Interface between 3.3 V and 5 V System

4.3 AC Characteristics

4.3.1 Test Circuit

Figure 4-7 shows the AC test circuit used to measure switching characteristics. Figure 4-8 shows the measured waveform parameters and their symbols.

The capacitive load C_L used in the tests is 50 pF. This load is based on the assumption that the input capacitance of the ICs connected in the next stage is 5 pF and the fan-out is 10. This is close to the loads expected in typical applications.

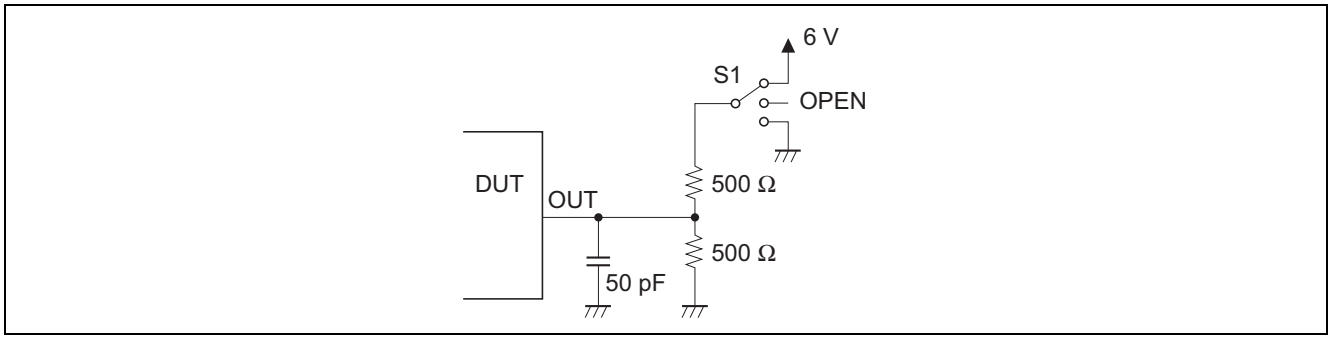


Figure 4-7 Test Circuit for AC Characteristics

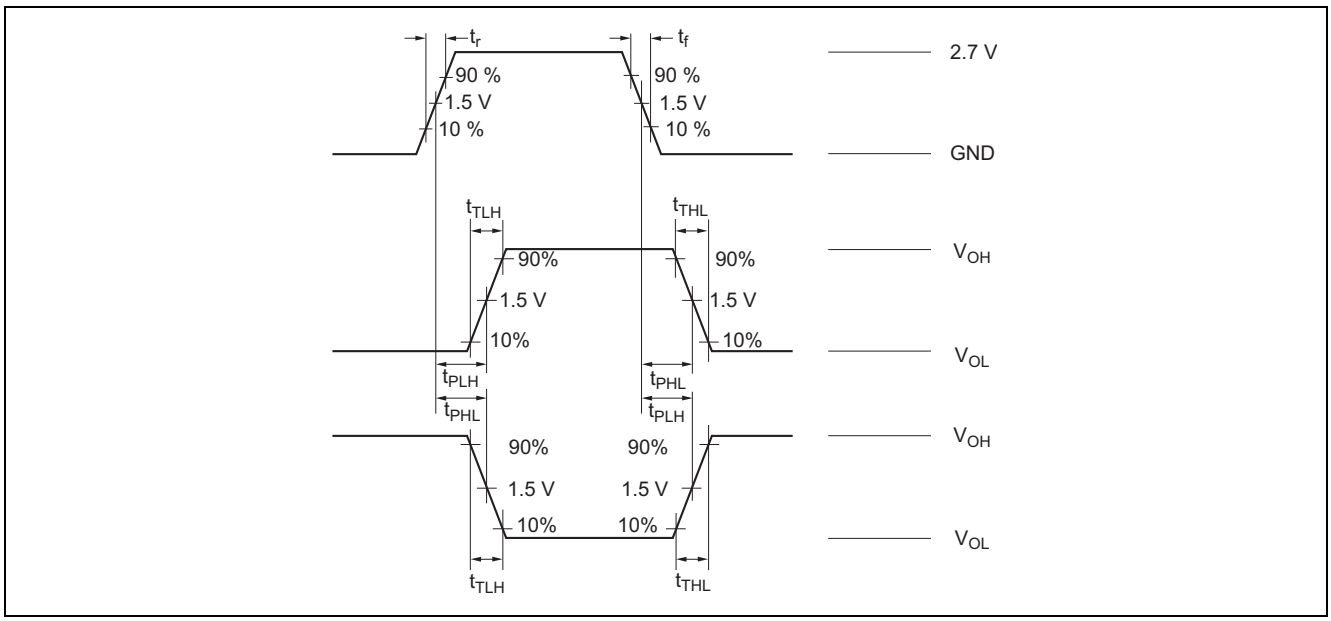


Figure 4-8 Measured Waveform Parameters and Symbols

4.3.2 Output Transition Time

Figure 4-9 shows the times required for low-to-high and high-to-low transitions of the output levels. This characteristic is referred to as the transient rate, and is an important parameter in reflection analysis.

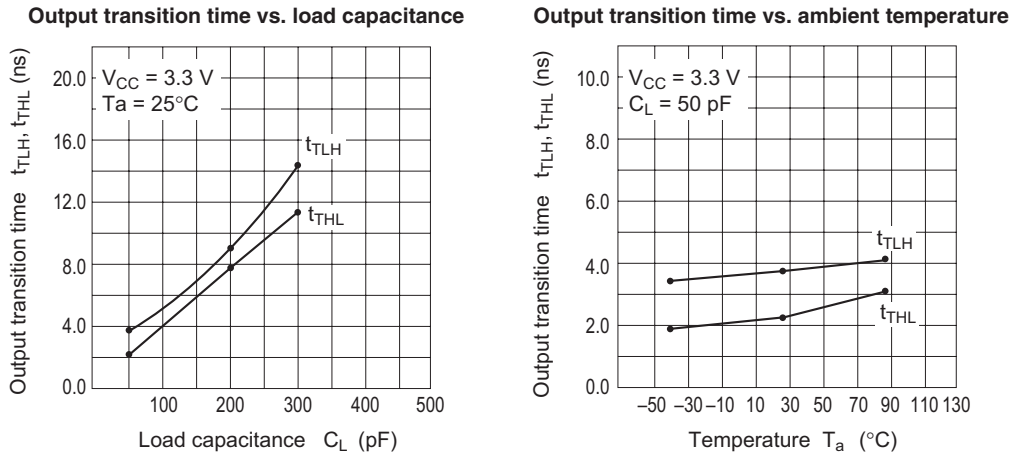


Figure 4-9 Measured Output Transition Time

4.3.3 Propagation Delay Time

Figure 4-10 shows the delay time from signal input to output.

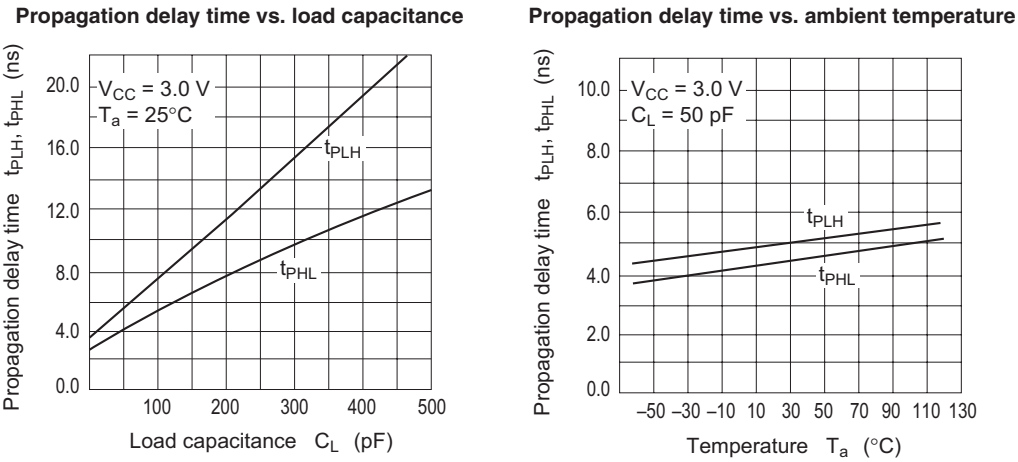


Figure 4-10 Measured Propagation Delay Time

4.3.4 Delay Due to Parasitic Load

Line Delay: Delays also exist on signal transmission paths. On a printed circuit board, signals travel at a rate of about 5.5 to 7.5 ns/m. This delay is due to the parasitic inductance and capacitance of the signal line, and is affected by the dielectric constant of the board.

Jumping wires and connectors are another source of delay, because of their large inductances. In high-speed circuits, besides delaying signals, they can also cause problems of noise and electromagnetic interference (EMI). If their use cannot be avoided, it is advisable to employ short, shielded cables.

Multiple Output Switching: Propagation delay times are affected by the number of outputs that switch simultaneously. In low-speed logic, the change in propagation delay time was negligible in relation to the delay itself, but in high-speed logic, from the AC Series on up, this effect can no longer be ignored.

In the LVC Series, when a device has two outputs or more, each additional output that switches simultaneously increases the propagation delay value listed in the data book.

The reason for this delay is that the parasitic capacitance on the output changes the power-supply and ground potentials inside the chip. This capacitive component also varies with the load capacitance on the transmission line. The larger the capacitance, the longer the switching time becomes.

One countermeasure is to reduce the load capacitance on the transmission line by one of the following methods:

- Better grounding
- Leaving more space between wiring traces

Chips with 16 circuits (16-bit devices) are better grounded inside the package than chips with 8 circuits (8-bit devices), so they are less susceptible to this effect.

Table 4-1 lists some test results of multiple output switching.

Table 4-1 Test Results of Multiple Output Switching

- HD74LVC244FP (V_{CC} = 3.3 V, Ta = 25°C)

Number of Circuits Switched	t_{PLH} (ns)	t_{PHL} (ns)
1 circuit	4.39	4.15
8 circuits	6.36	5.29

- HD74LVC16244T (V_{CC} = 3.3 V, Ta = 25°C)

Number of Circuits Switched	t_{PLH} (ns)	t_{PHL} (ns)
1 circuit	3.22	3.22
8 circuits	3.55	3.45
16 circuits	3.93	3.79

Actual Circuits and Delays: As pointed out above, propagation delays occur in on-board signal paths, and due to simultaneous switching of multiple outputs. Here, some worst-case values will be given.

Signals propagate through printed wiring traces with delays of about 5.5 to 7.5 ns/m. Assume the following values:

Propagation delay on signal path: 7 ns/m
Length of signal path: 30 cm

The propagation delay is then:

$$7 \text{ ns/m} \times 30 \text{ cm} = 2.1 \text{ ns}$$

When multiple outputs are switched simultaneously, there is an additional delay of 400 ps per output. If four outputs are switched simultaneously, then

$$400 \text{ ps/output} \times (4 - 1) \text{ outputs} = 1.2 \text{ ns}$$

When four outputs switch simultaneously, the propagation delay over 30 cm of wiring will be 3.3 ns.

These propagation delay times depend on parasitic inductance and capacitance, so they are affected by the dielectric constant of the board and the wiring method employed. The load capacitance C_L used in testing delay times assumes a fan-out of 10, with 5 pF in the next-stage ICs.

The delay can be reduced by reducing the load capacitance, using a TSSOP version of the IC, and reducing the line impedance.

4.4 Slow Input Characteristics

When an extremely slow signal is input, the input potential remains in the ambiguous state for a long time, making the output unstable. This can cause oscillation or other malfunctions.

Although the LVC/LVC-A Series has a high-speed bus interface, operation is assured at input slew rates as slow as 10 ns/V (rising and falling edges). This makes the LVC/LVC-A Series easier to use than the AC Series (8 ns/V).

4.5 Power Dissipation

CMOS logic dissipates power in proportion to the square of the voltage. A simple calculation shows that logic operating at 3 V will dissipate only 36% as much power as logic operating at 5 V.

Compared with TTL logic, at low operating frequencies CMOS logic dissipates much less power. Power dissipation rises in proportion to the operating frequency, however, because whenever switching occurs, there is a flow of current from power supply to ground.

The graph in figure 4-11 shows the relationship between operating frequency and power dissipation.

The LVC/LVC-A Series uses CMOS logic, so its power dissipation will vary according to the operating frequency.

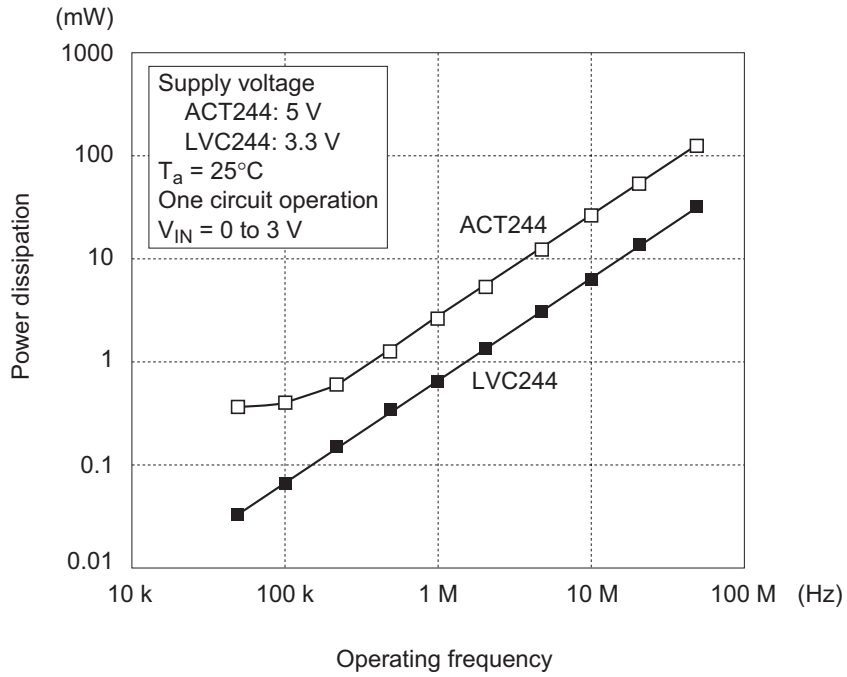


Figure 4-11 Power Dissipation in Relation to Operating Frequency

5. Noise Countermeasures

Noise may originate from the IC itself, or from external wiring. Noise originating in the IC itself, including multiple output switching noise and ringing noise, is much less of a problem in the LVC/LVC-A Series than in the previous AC Series. In the LVC/LVC-A Series:

V_{OLP} (output ground bounce) < 0.8 V (typical) [V_{CC} = 3.3 V, Ta = 25°C]
V_{OHV} (output V_{OH} undershoot) > 2 V (typical) [V_{CC} = 3.3 V, Ta = 25°C]

In most applications, these types of noise should not cause any concern.

Noise caused by wiring is a system problem rather than an IC problem. With a 3-V supply voltage, threshold voltages are lower and noise margins are reduced, increasing noise susceptibility. Systems should be designed with careful attention to power and ground lines, impedance matching, and crosstalk.

The noise waveforms discussed in this section were measured using HD74LVC244T devices. Figure 5-1 shows the noise test circuit. This circuit was used unless stated otherwise.

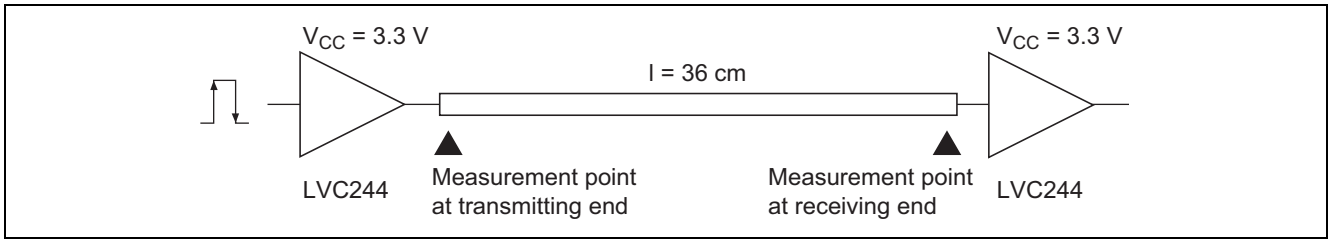


Figure 5-1 Noise Test Circuit

5.1 A Cause of Noise

In a high-speed system, digital circuit designers need to have a knowledge of high-speed analog circuit theory. There are four main causes of noise.

- Mismatching of the IC's output impedance to the characteristic impedance of the transmission line (LVC/LVC-A output impedance is approximately 25 Ω, while the impedance of a transmission line is generally about 50 Ω to 200 Ω)
  → Reflection noise
  → Ringing noise
- Parasitic inductive and capacitive components in the IC and on transmission lines, and the resulting L-C-R resonance
  → Ringing noise
- Voltages resulting from the flow of load charge/discharge current or transition current through stray inductances in the IC
  → Power- and ground-line noise
  → Multiple output switching noise
- Capacitive or inductive coupling between adjacent transmission lines
  → Crosstalk noise

In actual circuit designs there are complex and closely-interrelated factors to be considered. One way to prevent reflection noise, for example, is to shorten wiring lengths by high-density system mounting, but high-density mounting may cause crosstalk problems on other transmission lines in the system.

Designing a high-speed, low-power system requires accurate knowledge of noise.

5.2 Power- and Ground-Line Noise

Systems designed without protection from power- and ground-line noise tend to have spiky waveforms. Power- and ground-line noise includes:

- Noise originating from the AC power line
- Induction from other wiring, or effects of strong electric fields or electromagnetic radiation
- Effects of circuits connected to the power and ground lines

Here, however, we are concerned with noise generated by the operation of the IC itself.

Switching in digital circuits is accompanied by sudden changes in power-supply current. These sudden changes include many high-frequency components, and can easily generate pulse-type noise. High-speed systems also have parts that resemble high-frequency analog circuits more than digital circuits.

Specific solutions to power- and ground-line noise include:

- Use of bypass capacitors
- Reduced inductance through better grounding

5.2.1 Bypass Capacitors

The use of bypass capacitors (also called decoupling capacitors) could be described as an absolute necessity in digital circuits. Capacitors have different frequency bands, so rather than insert one large capacitor, it is more effective to insert two or more capacitors to cover the appropriate frequency bands.

Standard practice is to connect one bypass capacitor per IC, as close as possible to the IC's power and ground leads. The best type of capacitor is generally considered to be:

- 0.01 µF to 1 µF multilayer ceramic capacitor
- 0.1 µF to 10 µF tantalum capacitor

The output transition times in the LVC Series are:

- Rising edge Approx. 3.5 ns
- Falling edge Approx. 2.5 ns

The frequency band to be covered is therefore 140 MHz to 200 MHz. A multilayer ceramic capacitor with a value around 0.1 µF should be about right.

Bypass capacitors must be located close to the power and ground pins of the IC. A bypass capacitor is supposed to be a purely capacitive component, but when mounted on-board, it turns out to have a stray inductance as well. If the bypass capacitor has long leads, the inductive component may be so large that using the bypass capacitor actually does more harm than good.

The same is true if the printed wiring traces are too long. The rule for preventing noise is to use short, thick traces. When designing board patterns, it is a good idea to look at the wiring methods employed in high-frequency analog circuits. Figure 5-2 shows a recommended pattern for connecting bypass capacitors.

One aluminum electrolytic capacitor with a capacitance from 10 µF to 100 µF should be inserted near the power supply as a low-frequency filter.

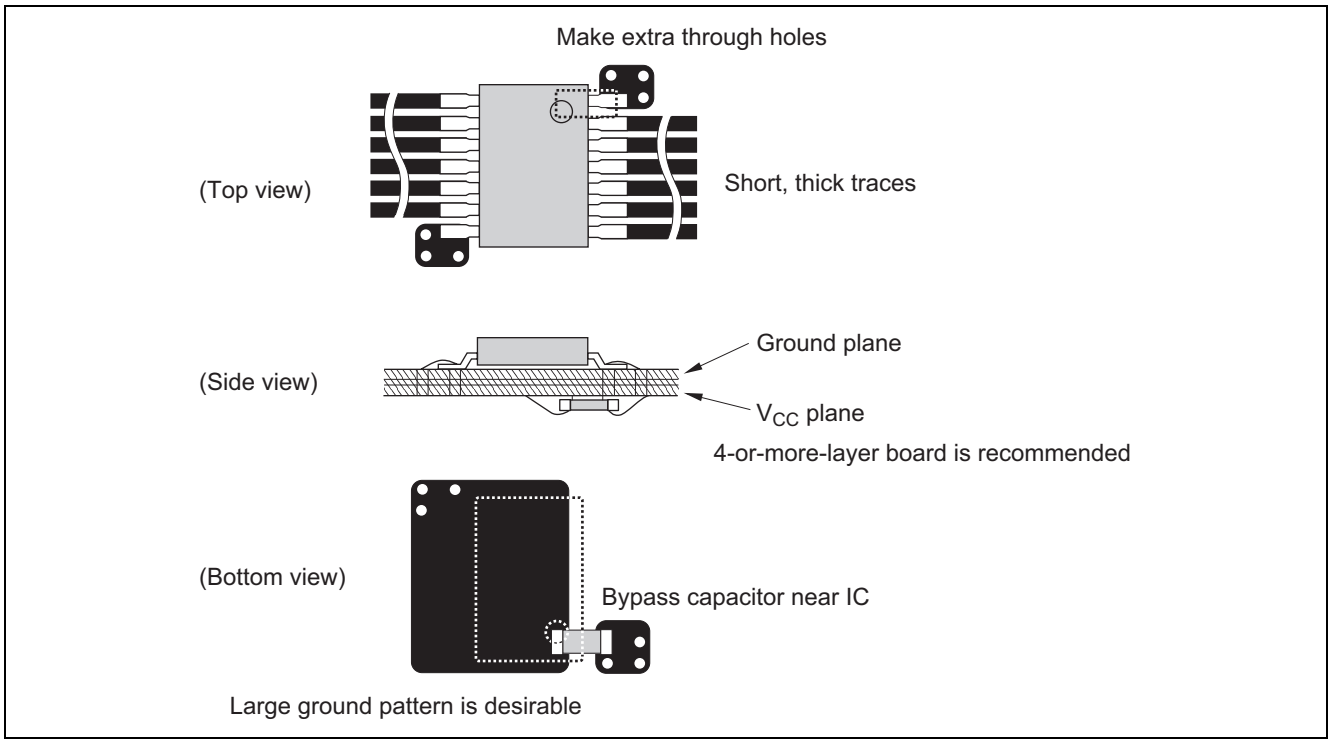


Figure 5-2 Recommended Pattern

5.2.2 Improved Grounding

Grounding can be improved by using short, wide traces on the printed circuit board (PCB), and by providing a ground plane.

For high-speed circuits in particular, the board should have at least three layers of wiring, one of which should be a ground plane. A ground plane will lower the impedance of the wiring, and can suppress ringing and crosstalk. A V_{CC} plane has the same effect in lowering impedance.

The recommended assignment of layers is:

- 3-layer board: pattern—GND—pattern
- 4-layer board: pattern—GND—V_{CC}—pattern
- 6-layer board: pattern—pattern—GND—V_{CC}—pattern—pattern

On a six-layer board, address bus and data bus lines should be routed in the layers next to the ground and VCC planes, because they will then have lower impedance. The traces on adjacent pattern layers should be laid out at right angles to each other.

The multi-wire method of making a PCB should be mentioned. This method starts from a baseboard and proceeds to embed the wiring. Besides improved grounding, this method has the following features:

- Easy impedance matching of signal lines
- Minimum-length routing of signal lines
- Easy equal-length routing of signal lines, with minimum signal-line delay

If both analog and digital circuits are placed on the same board, high-frequency signal components from the digital circuits will affect the power and ground lines of the analog circuits, so the two types of circuits must have separate V_{CC} and ground planes.

Improved grounding can dramatically reduce noise. Multilayer or multi-wire boards are recommended for high-speed circuits, and these can be made still more effective by providing large ground patterns, like the ones seen on analog boards, in appropriate places.

If the [BETA] ground and [BETA] power supply are input for each strategic point, resistance to noise can be achieved even with a double-sided board. Considered in a certain way, directionally aligning the [BETA] ground and [BETA]

power supply is equivalent to having a high-frequency bypass capacitor. Conversely, a [BETA] pattern which is not connected to either the ground or the power supply is potentially unstable, and thus susceptible to EMC noise.

5.3 Ringing Noise

Ringing refers to resonance resulting from stray L-C components in the IC or on transmission lines, or from L-C-R components, or to oscillation of output waveforms due to mismatching between the IC's output impedance and the impedance of the transmission lines.

IC's with high driving capability have particularly low output impedance. The large difference between this impedance and the impedance of the transmission lines can easily cause ringing.

The amount of ringing will differ depending on the wiring length, load capacitance, and termination method. Simply shortening the wiring traces is an effective way to suppress ringing. If long wiring traces are necessary, adding termination is effective.

In a system operating at high speed, instead of thinking of transmission lines as simple resistances, it is more accurate to regard them as an L-C-R network. Impedance effects therefore increase together with the frequency, and the longer the line is, the more susceptible it becomes to these impedance effects, resulting in more noise.

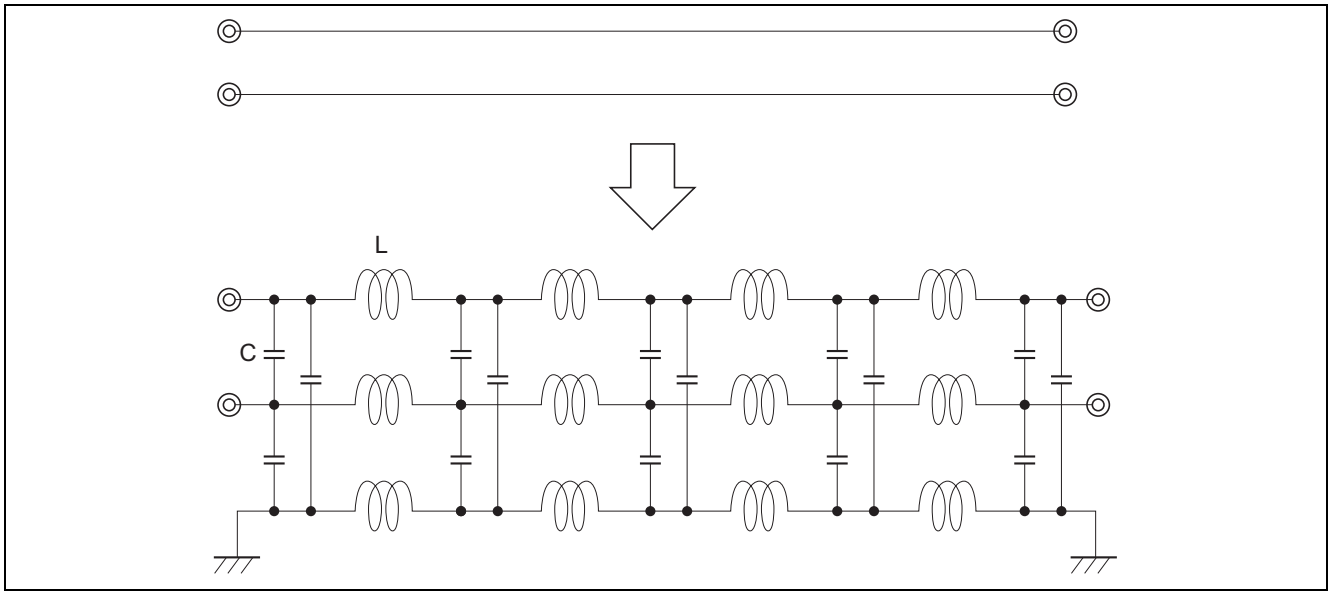


Figure 5-3 Conceptual Diagram of Transmission Lines

5.4 Reflection Noise

Reflection noise occurs inevitably as a result of mismatching of impedance between the IC and transmission line, or between different ICs (see figure 5-4). CMOS logic has only capacitive loads, so it naturally offers high impedance, and signal reflection effects require due attention.

5.4.1 Lumped-Constant and Distributed-Constant Circuits

With short transmission lines, reflection is not such a critical consideration. Short transmission lines can be treated as lumped-constant circuits.

When the propagation delay time on a transmission line is equal to or greater than the transition time of a signal pulse, the transmission line must be treated as a distributed-constant circuit and reflection effects must be considered. In general, it becomes impossible to ignore reflection when the propagation delay on the transmission line is about 1/3 greater than the IC's rise time or fall time.

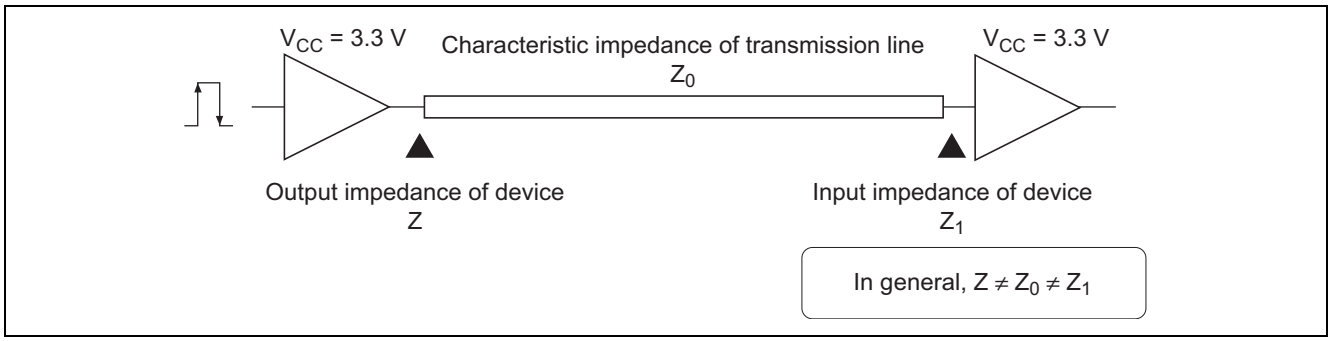


Figure 5-4 Reflection Principle

The best way to avoid reflection effects is to shorten the transmission line so that it can be treated as a lumped-constant circuit. If the transmission line cannot be made this short, then appropriate termination must be provided.

5.4.2 Reflection between Logic Devices

In terms of size alone, the effect of reflection noise from the transmission line is outweighed by the effect of the logic device at the other end of the line. The reason is that total reflection occurs at the logic device, because its input impedance is much higher than the impedance of the signal line.

The theoretical reflection waveform can be found from a Bergeron diagram, taking the impedance of the output characteristic, input characteristic, and transmission line separately. The procedure will be shown below, assuming that the transmission line has a characteristic impedance of 75 Ω.

- Output raising

1. Draw a straight line on the input/output characteristic diagram in the positive direction from 0 V, 0 A, with a slope corresponding to the impedance (75 Ω) of the transmission line.
2. When the line intersects the input/output characteristic curve, reverse direction so as to converge toward 3.3 V, 0 A, always keeping the slope equal to the impedance of the transmission line.
3. Repeat step 2 until it converges.

- Output falling

4. Draw a straight line on the input/output characteristic diagram in the negative direction from 3.3 V, 0 A, with a slope corresponding to the impedance (75 Ω) of the transmission line.
5. When the line intersects the input/output characteristic, reverse direction so as to converge toward 0 V, 0 A, always keeping the slope equal to the impedance of the transmission line.
6. Repeat step 5 until it converges.

- Transmitting and receiving ends

7. Add time-series symbols (0, T, 2T, 3T, …) to the Bergeron diagram, taking the transmitting device and receiving device in order. Figure 5-5-1 shows a completed Bergeron diagram.
8. Use the Bergeron diagram to plot a voltage time-series graph. Figure 5-5-2 shows the theoretical waveform plotted in this way.

Figure 5-5-3 compares the actual reflection waveform with the theoretical waveform for this reflection analysis. For reference, figure 5-6 shows Bergeron diagrams for 25 Ω, 50 Ω, 75 Ω, and 100 Ω. Figure 5-7 shows the corresponding reflection noise waveforms for actual interfaces.

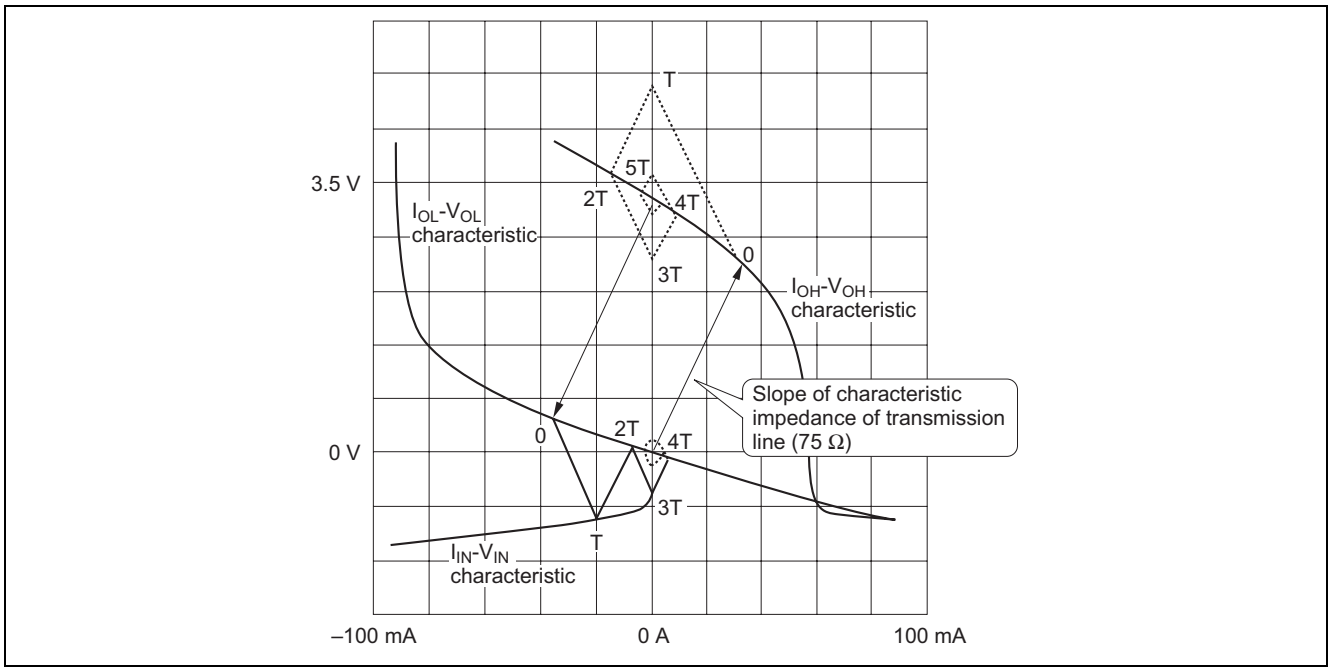


Figure 5-5-1 Analysis of Reflection Waveforms (Bergeron Diagram)

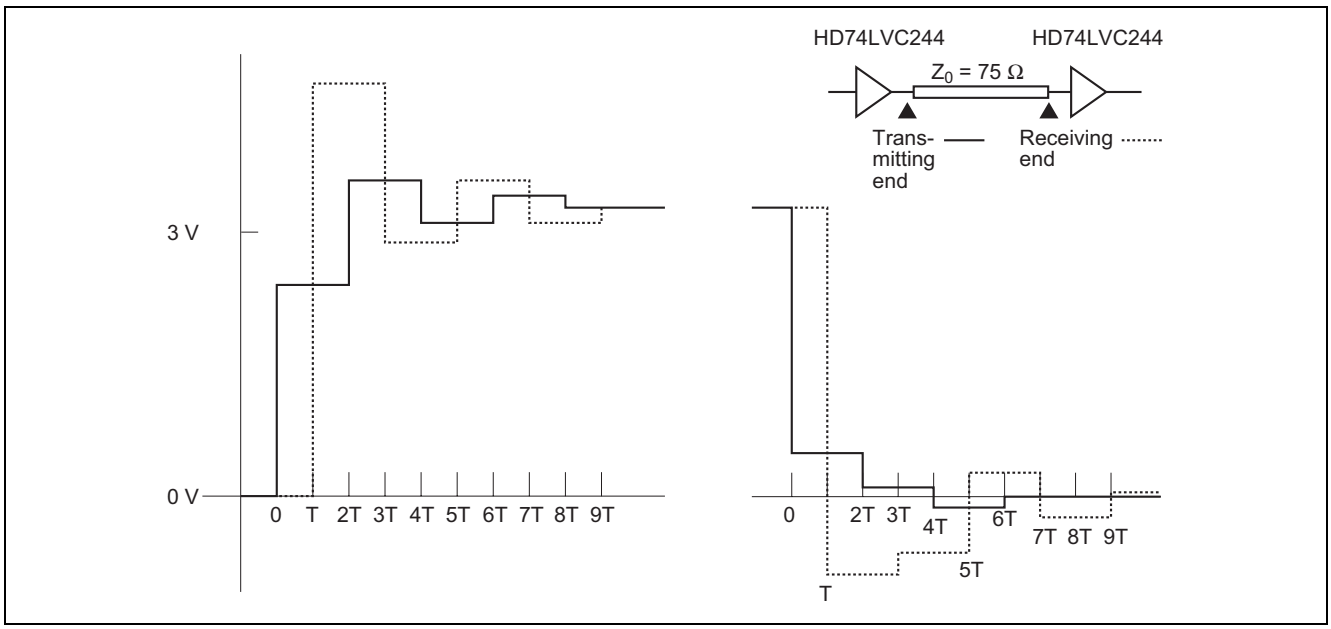


Figure 5-5-2 Analysis of Reflection Waveforms (Theoretical Waveform Plot)

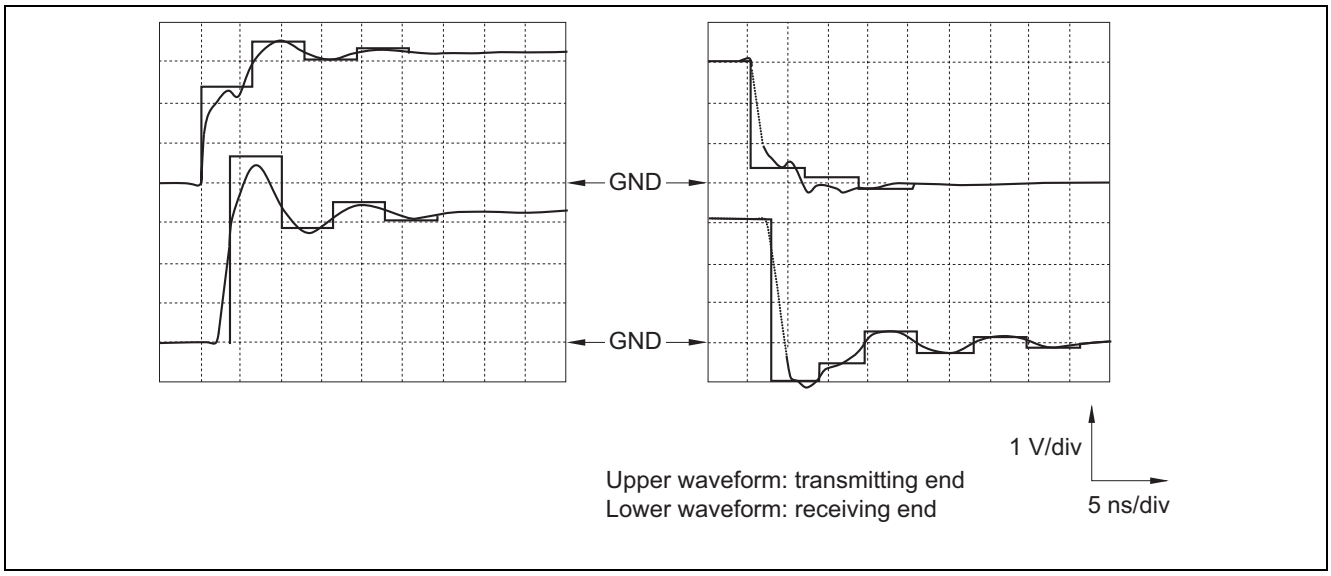


Figure 5-5-3 Analysis of Reflection Waveforms (Comparison with Actual Waveforms)

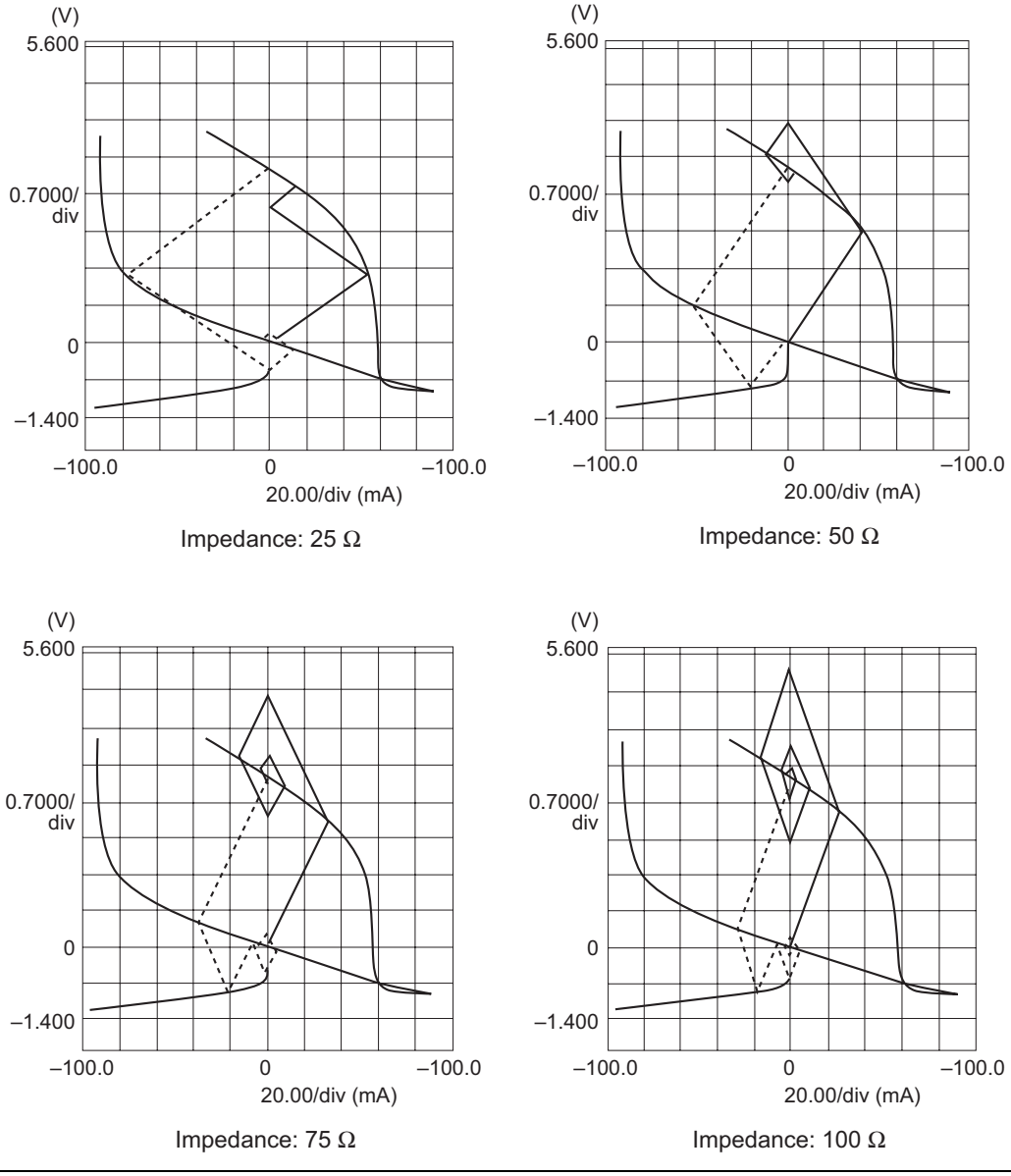


Figure 5-6 Reflection Waveform Analysis for Various Circuits

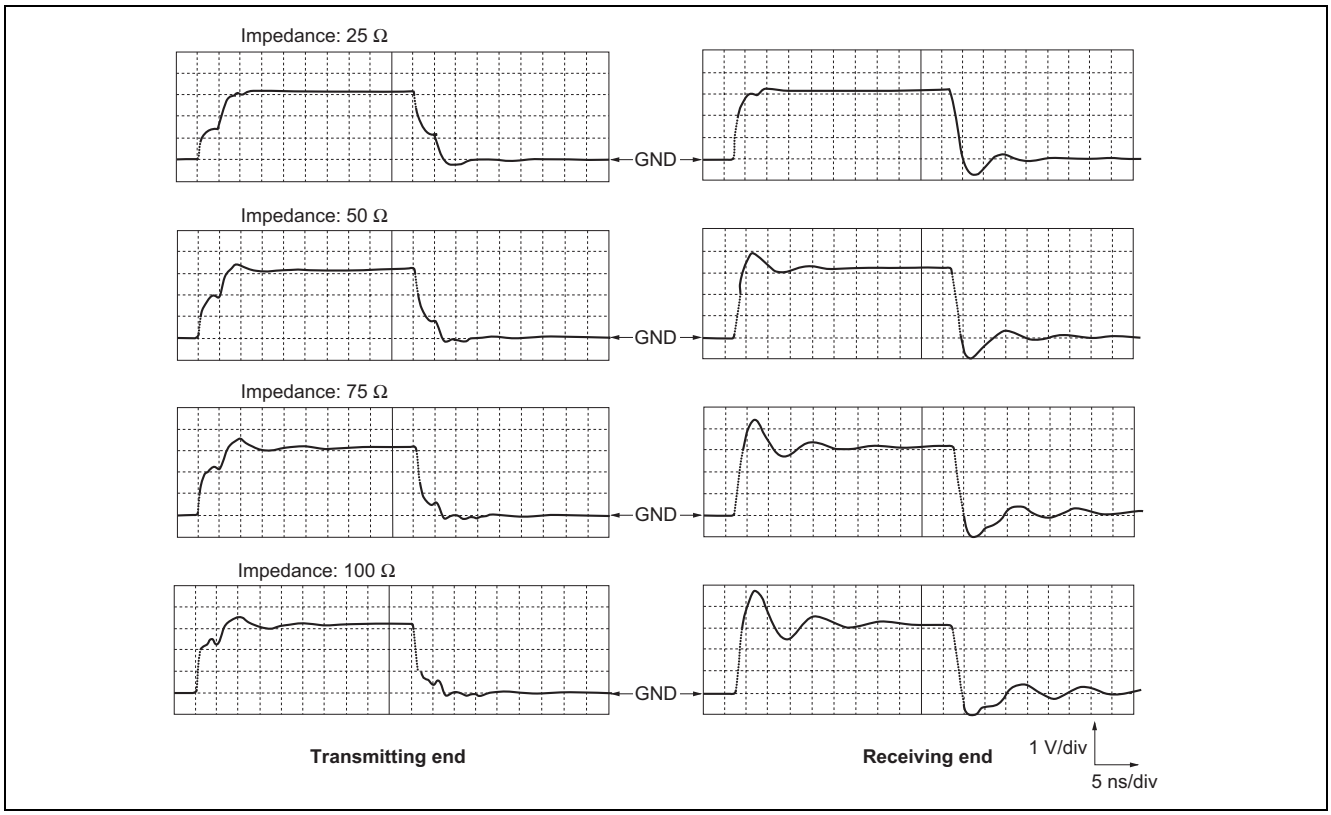


Figure 5-7 Reflection Noise Waveforms

When multiple logic devices are driven, the characteristic impedance of the transmission line will be mismatched at the branch points. Figure 5-8 shows two ways of smoothing out the impedance in this case:

- Use a single trace with no branching (terminated at the last logic device)
- Insert a damping resistor in each branch

On an expansion bus or other interface that goes through multiple connectors, the impedance on the transmission line on the expansion-bus side will normally drop to about 50 Ω.

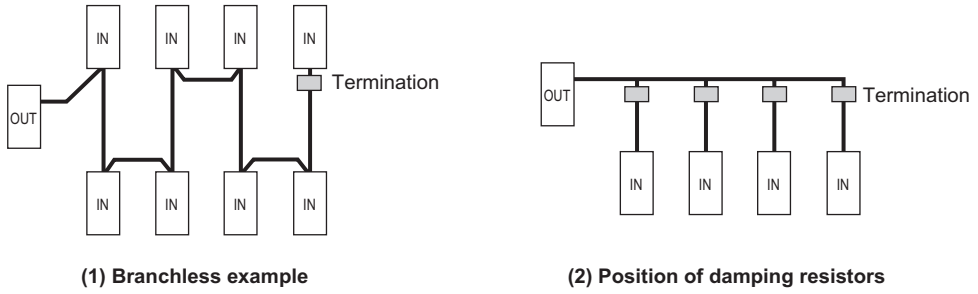


Figure 5-8 Examples of Termination

5.4.3 Termination

To suppress reflection noise, impedance must be matched between the device and transmission line. Termination is a means of impedance matching.

Different types of termination are described below (see figure 5-9).

Parallel Termination and Thevenin Termination: In parallel termination and Thevenin termination, the termination itself dissipates considerable power, which is unsuitable for low-power designs.

AC Parallel Termination and AC Thevenin Termination: These methods of termination are effective ways to reduce the power consumption of an application, because the termination does not dissipate any DC power. The resistor and

capacitor values must be selected so that the time constant of the R-C circuit equals the rise time and fall time of the signal.

Clamping Diodes: Clamping diodes are both effective and easy to use, because they do not require matching with the transmission line, unless you are considering current leakage at power-off and hot circuit insertion, or operation in mixed 3.3-V/5-V systems. Clamping diodes with a small forward voltage drop (VF equaling approximately 0.3 V) must be selected. Renesas recommends the HSM107S and HSM126S as protective diodes.

Damping Resistor: A damping resistor is an effective way to terminate a transmission line without dissipating power in the termination. A damping resistor is a resistor that is inserted in series with the transmission path, near the driver, to match its impedance to the transmission line. Damping resistors are useful when the number of added components is small and there is ample margin in timing and driving capability. They are particularly effective for an interface such as an expansion bus that passes through multiple connectors. Be careful not to insert too much resistance, however, because that can drop the voltage below the threshold level, making it impossible to drive the next stage.

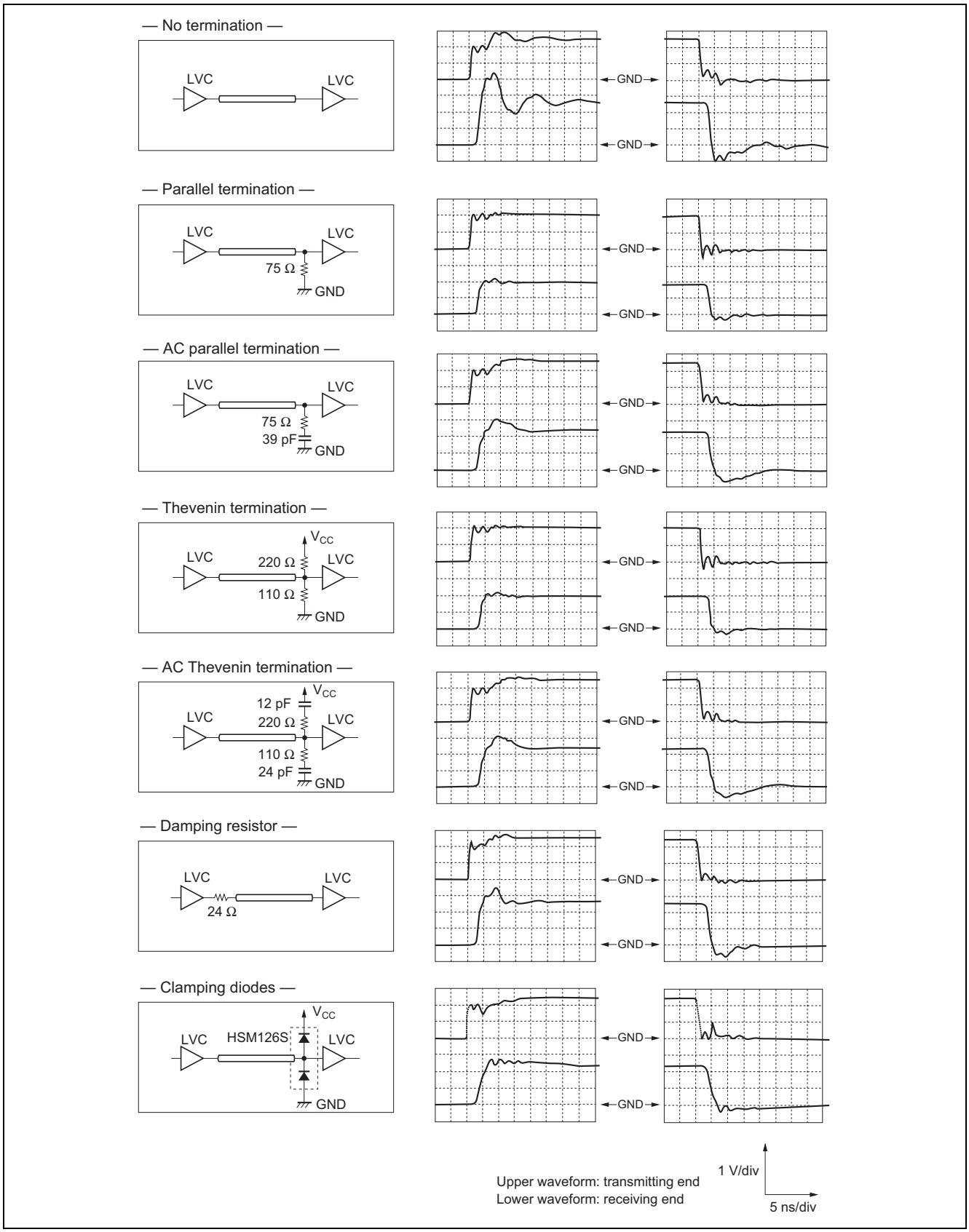


Figure 5-9 Types of Termination

5.5 Crosstalk Noise

Crosstalk noise is noise that is induced on a transmission line by a signal propagating on an adjacent transmission line, because of capacitive or inductive coupling. In the broad sense of the term, AC power-line effects, motor effects, and electrostatic noise from charged human bodies could also be classified as crosstalk noise. The following measures will help to reduce crosstalk noise:

- Make transmission lines as short as possible
- Reduce the impedance of transmission lines
- Provide better grounding
- Leave more space between pattern traces, or insert ground lines
- Avoid, or at least minimize, traces that run in parallel

The signals on parallel bus lines may travel in the same direction, which is called parallel transmission, or in opposite directions, which is called anti-parallel transmission. The causes of crosstalk differ depending on signal transition times and the characteristic impedance of the transmission lines, but in general, noise levels will be higher in anti-parallel transmission.

Figure 5-10 shows the circuits used to measure crosstalk noise. Measured waveforms are shown in figures 5-11-1, 5-11-2, and 5-11-3.

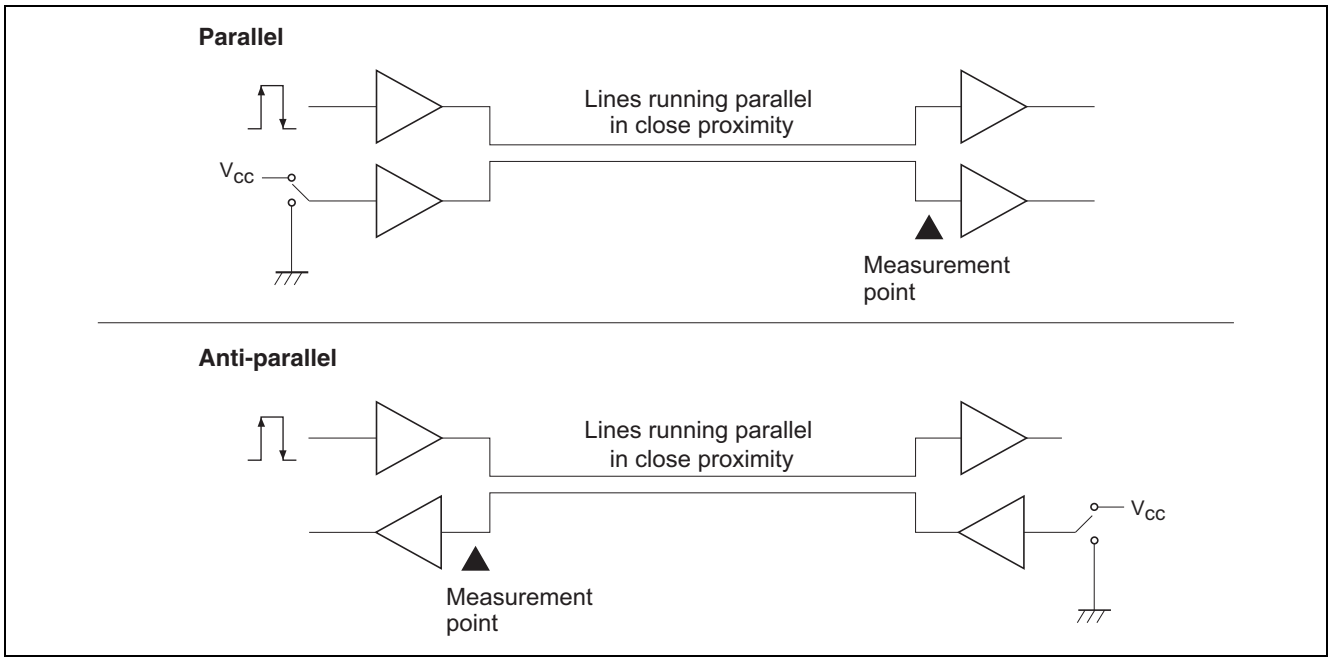


Figure 5-10 Circuits for Measuring Crosstalk Noise

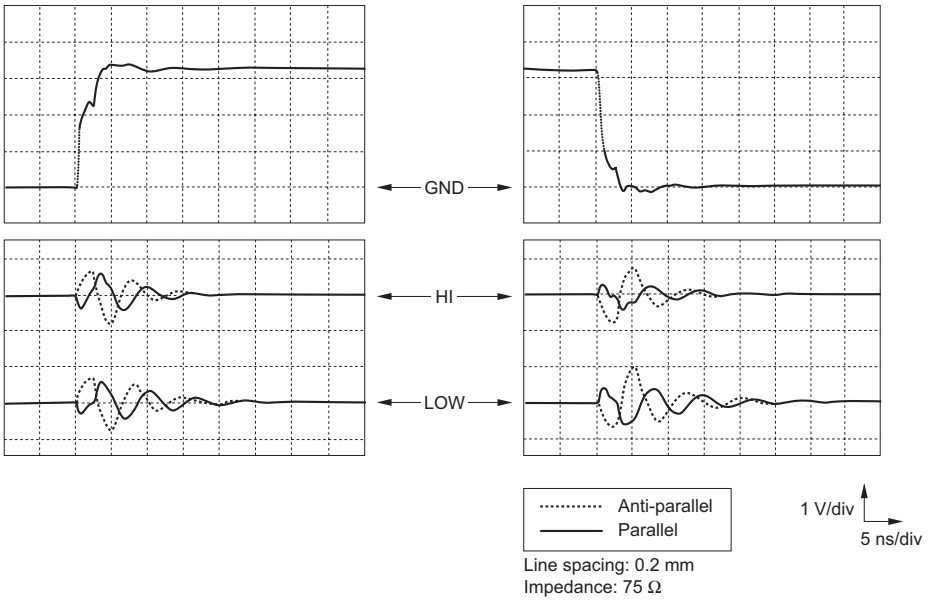


Figure 5-11-1 Crosstalk (Comparison of Parallel and Anti-Parallel Cases)

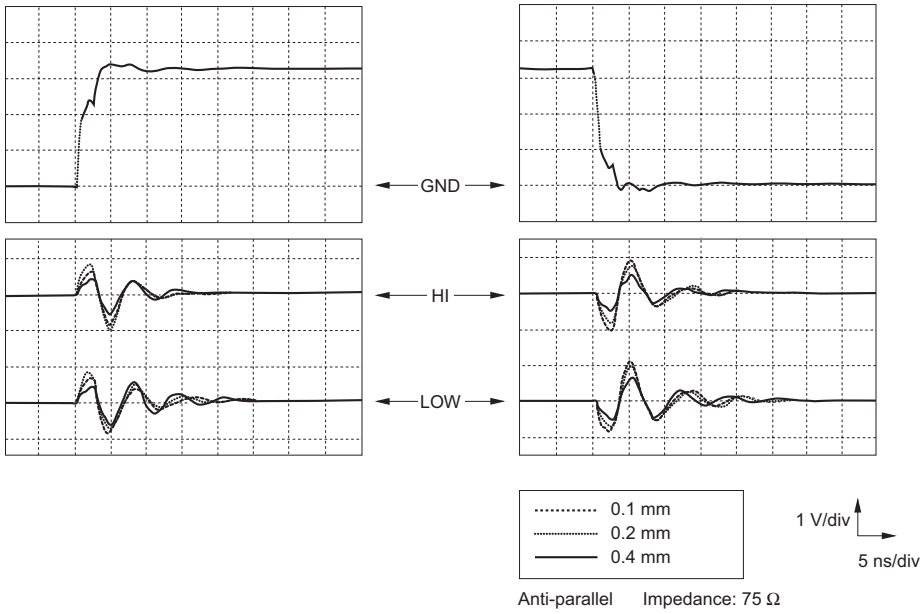


Figure 5-11-2 Crosstalk (Effect of Line Spacing)

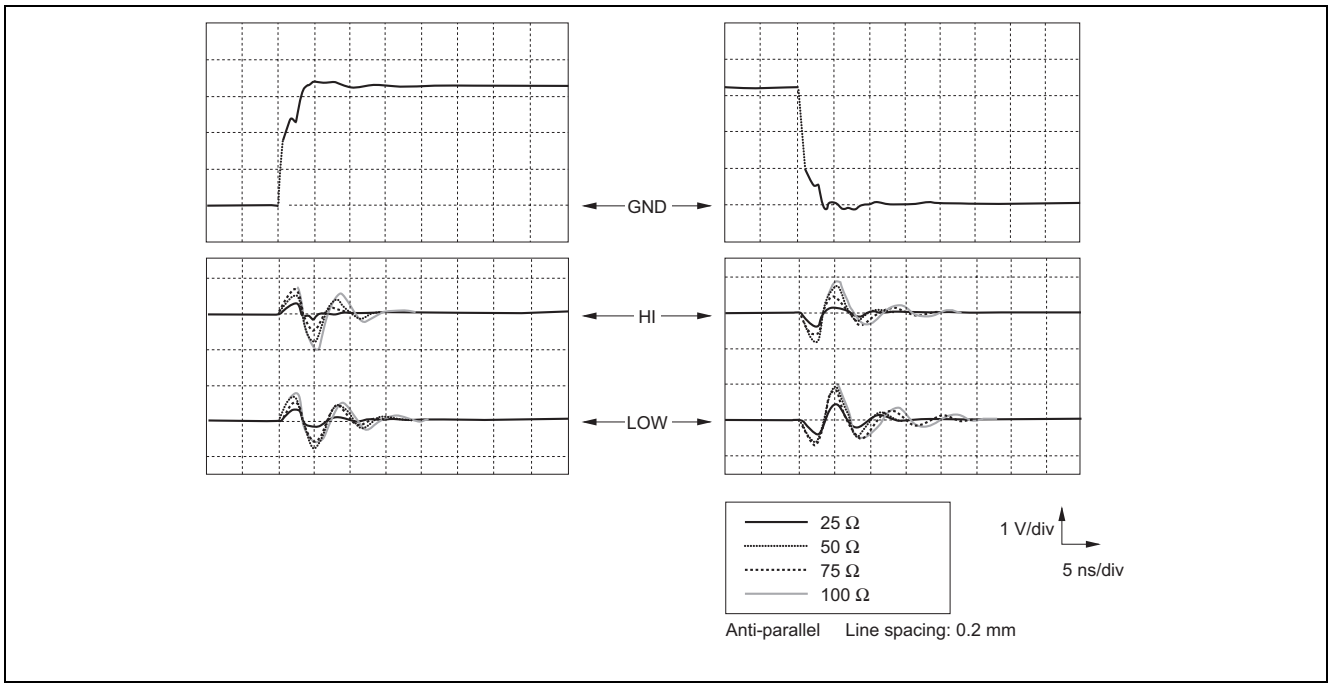


Figure 5-11-3 Crosstalk (Effect of Effect of Transmission Line Impedance)

The following guidelines relate not just to logic devices but to microprocessor systems and systems in general.

- Route the address bus as far away from the data bus as space on the board permits
- Separate the high-speed control bus
- As far as possible, avoid parallel transmission paths
- Use a board with an internal ground plane

Memory and other capacitive loads tend to increase crosstalk noise, so their transmission paths require extra attention.

5.6 Multiple Output Switching Noise

Multiple output switching noise is noise that occurs on non-switched outputs when several other outputs in the same package are switched simultaneously.

Figure 5-12 shows the principle behind multiple output switching noise. When outputs are switched, the parasitic inductance component on the common ground causes a change in the ground potential, referred to as ground bounce. This can cause malfunctions in digital circuits that are referenced to the ground potential.

Ground bounce is affected by the number of circuits that operate simultaneously, the positional relationship between the ground lead and output leads in the IC, the load capacitance, and the supply voltage.

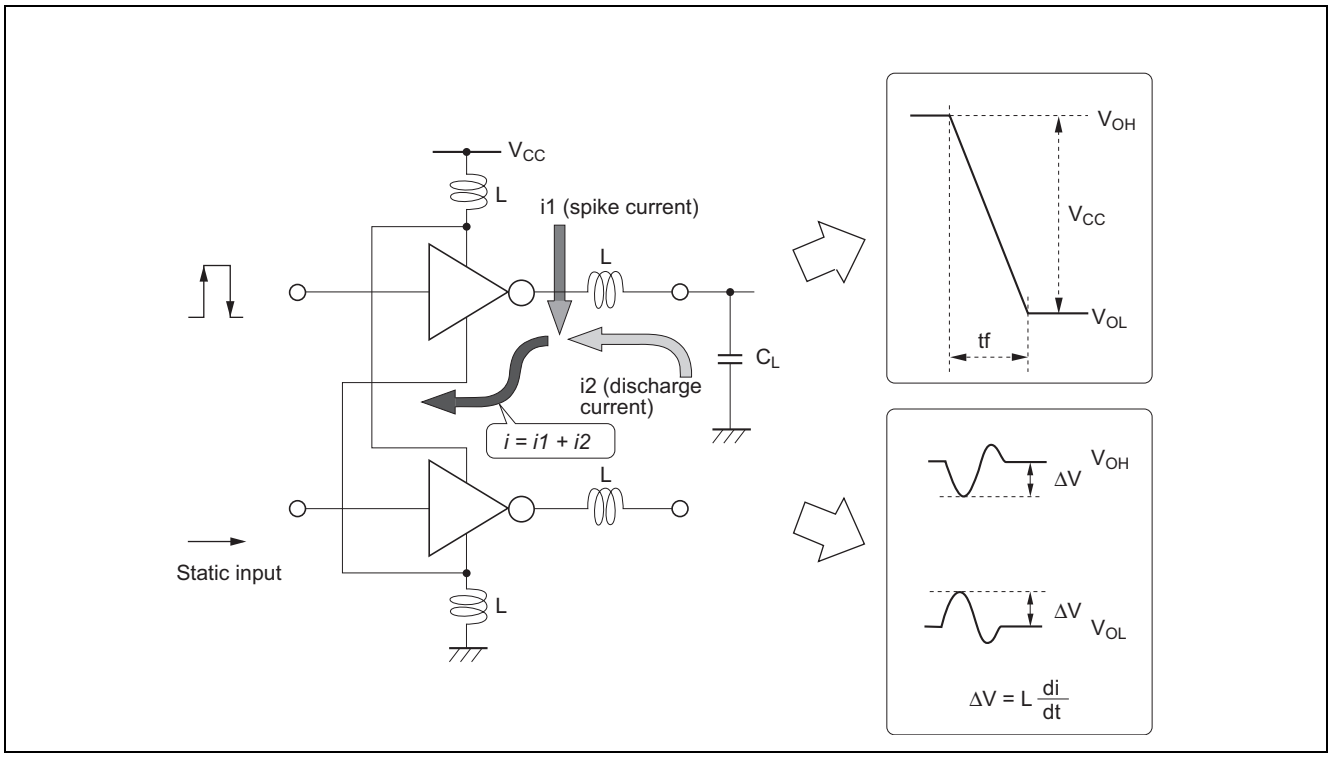


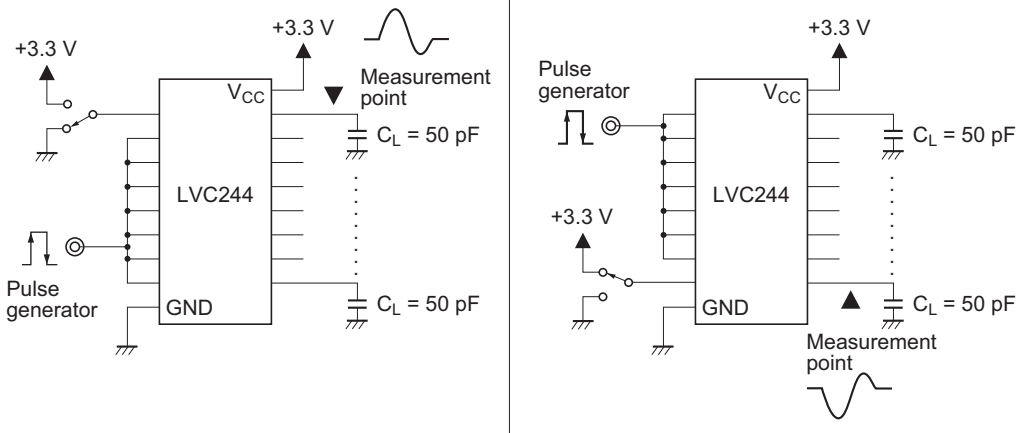
Figure 5-12 Principle of Simultaneous Switching Noise

Multiple output switching noise has the following features:

- The noise level rises with the number of circuits switched simultaneously in the same package
- Switching noise is reduced if the output levels of the driver IC are near VCC when at the high logic level and near ground at the low level
- Reducing the supply voltage also reduces switching noise

In the LVC/LVC-A Series, multiple output switching noise (V_{OLP}) is held to 0.8 V or less. Packages with 16 circuits have more V_{CC} and ground pins than packages with 8 circuits and are better grounded inside the package, so their noise levels are even lower.

Figure 5-13 shows the circuits used to measure multiple output switching noise. The measurements were performed at the point most strongly affected by multiple output switching noise. Figures 5-14-1, 5-14-2, and 5-14-3 show measured waveforms. Figure 5-15 shows a graph indicating the effect of the number of circuits switched simultaneously in the same package.



V_{OL} noise

V_{OL} noise is largest at the lead farthest from GND

V_{OH} noise

V_{OH} noise is largest at the lead farthest from V_{CC}

Figure 5-13 Circuits for Measurement of Simultaneous-Switching Noise

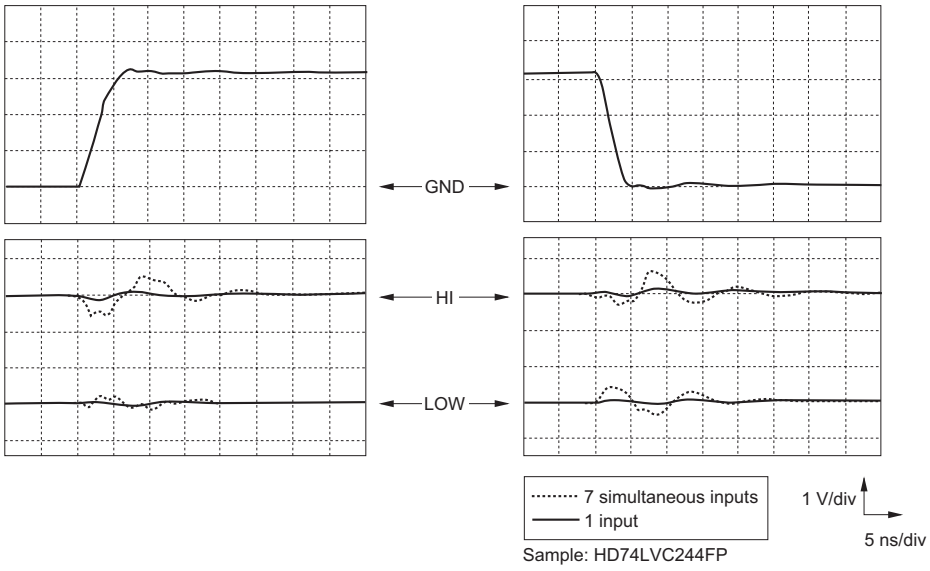


Figure 5-14-1 Multiple Output Switching Noise (Simultaneous Switching in Package with 8 Circuits)

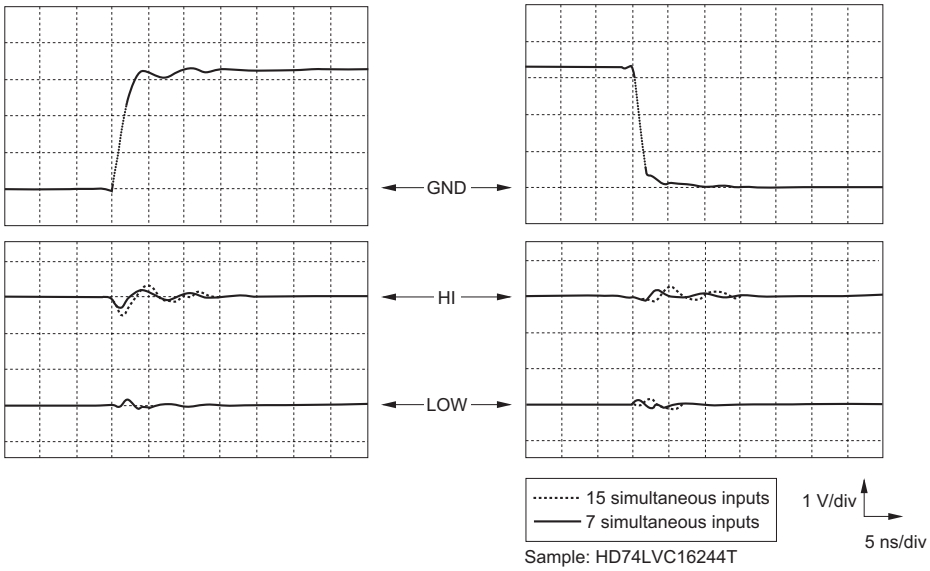


Figure 5-14-2 Multiple Output Switching Noise (Simultaneous Switching in Package with 16 Circuits)

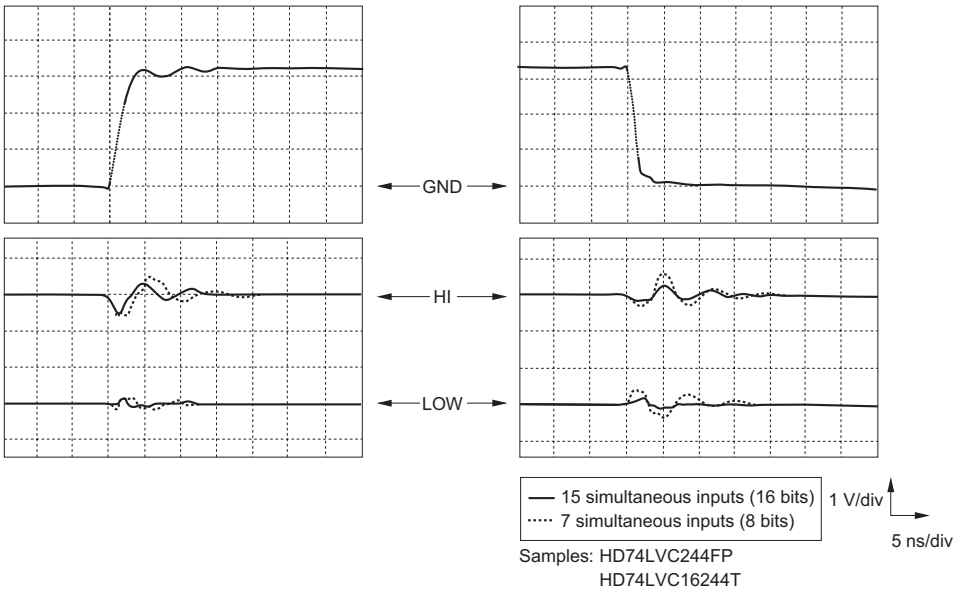


Figure 5-14-3 Multiple Output Switching Noise (Comparison of 8-Circuit and 16-Circuit Packages)

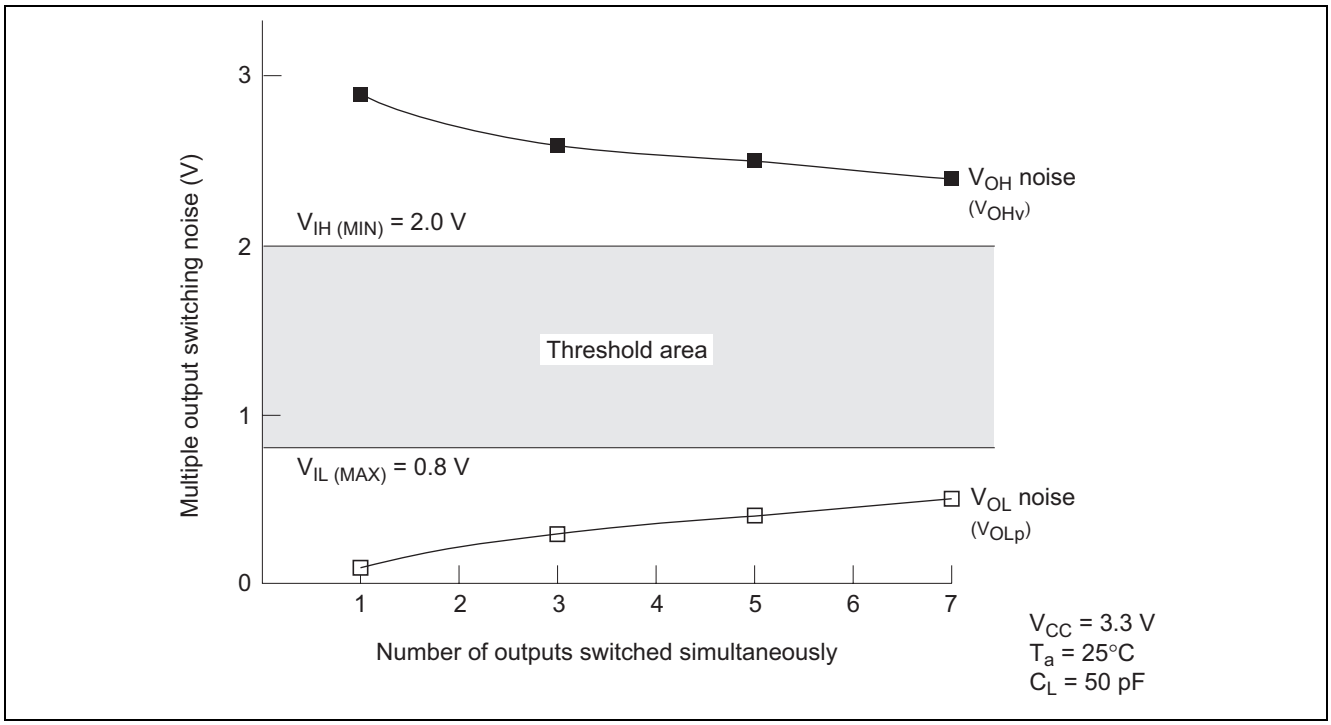


Figure 5-15 Effect of Number of Simultaneously-Switched Circuits

From a systems standpoint, multiple output switching noise can be suppressed by the following methods.

- Reduce the number of outputs that switch simultaneously in the same package
- Use separate packages for the address bus, data bus, and control bus
- Place lower address-bus bits close to ground leads
- Divide the control bus lines among several packages, so that they will not affect each other

6. Other Notes and Precautions

6.1 Grounding

The most important factor is a better ground. A well-grounded circuit should not suffer severe noise problems. Some guidelines for good grounding are:

- Ground analog circuits and digital circuits separately, and ensure that there will not be a potential difference between the two grounds
- Use a multilayer board with a ground plane, and connect devices to ground directly with large through holes
- Avoid ground loops, to avoid creating potential differences
- Ground any completely unconnected "floating island" pattern areas on the board
- Insert bypass capacitors
  - Use bypass capacitors in the board power supply to eliminate external noise
  - Use bypass capacitors near ICs to eliminate specific high-frequency components

6.2 Counter measure of Unused Inputs

a) LV-A and LVC/LVC-A series

The CMOS product has extremely high input impedance. If any inputs are left open, they can easily pick up noise, and since the input potential is undefined, the output logic level will be undefined, creating an unstable operating state.

When there are unused gates or flip-flops in the same package, if their inputs are left open, because of the structure of CMOS logic, they may draw power-supply current.

Unused inputs should therefore always be connected to ground or V_{CC}. When connecting an unused input to V_{CC}, insert a resistor of several kΩ. However, the C_{EXT}, R_{EXT} / C_{EXT} terminal of HD74LV123A is exceptional and when unused, they should be left open.

b) ALVC series

In case of ALVC series, unused countermeasures differs whether it has bus hold circuit or not.

When the ALVC dose not have the bus hold circuit, unused inputs should always be connected to ground or V_{CC}, same as LV-A and LVC/LVC-A series.

When the ALVC series has the bus hold circuit, unused inputs need not to be pulled-up or pulled-down. Compared with pulled-up with the resistor case, as shown in figure 6.2, no current flows at pull-up states in the bus hold circuit.

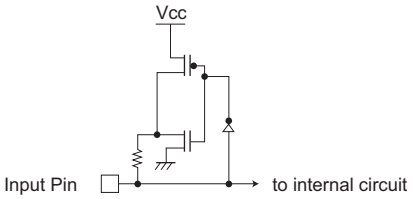


Figure 6-1 Bus hold Circuit

Figure 6-2 ALVC series Vin-Iin Characteristic with bus hold circuit

Bus hold circuit is the structure put to the input and has min.75 µA, max.500 µA drivability. The CMOS circuit which keeps high impedance in not operated status, the wiring connected with the input of ALVC series is pulled-up or pulled-down by the bus hold circuit.

Please pay attention to the following points at using the bus hold circuit.

1) Cannot select the default value as 'high' or 'low'.
2) When more than 75 µA current flows, the hold is released. If the low impedance part is connected with the input, then the bus hold circuit will not work.
3) If the input must be pulled up with the resistor, the resistor value needs to be selected in order to flow more than 500 µA current.

6.3 Bi-directional Interface with 3 V Device and 5 V Device

For bi-directional interface basic idea is as follows:

a) To the LSI with V_{CC} = 3.3 V:
   Receives 5 V signal and transmits 3.3 V signal.
b) To the LSI with V_{CC} = 5 V:
   Receives 3.3 V signal and transmits 5 V TTL level signal.

Please pay attention in this case 5 V device must have 5V TTL level input.

One possible solution in order to make signal 5 V, is to pull up the output, but this solution is not recommended. Because the current flows through the output MOS gate. The IC itself may not destroy by applying 5 V when the output is enabled.

In this case, please use the level shifter, HD151015, which enables the bi-directional interface between 5 V CMOS level and 3.3 V.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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