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April 1st, 2010
Renesas Electronics Corporation

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Low-Voltage CMOS Logic HD74ALVC Series

Definition

1. Calculating the Power Dissipation

The power dissipation PT of low-voltage CMOS logic can be calculated by (1). From this equation, the power dissipation depends on the load capacitance, frequency and supply voltage.

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 \qquad (1)$$

then,

C_L: Load capacitance, C_{pd}: Power dissipation capacitance,
f: Operating frequency, V_{CC}: Supply voltage

2. Power Dissipation Capacitance

Power dissipation capacitance (C_{pd}) can be calculated by the following equations,

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 = I_{CC} \times V_{CC} \qquad (2)$$

therefore,

$$Cpd = \frac{I_{CC}}{f \times V_{CC}} - C_L \qquad (3)$$

then,

I_{CC}: Supply current
(Test conditions)
Ta = 25°C, V_{CC} = 3.3 V, f = 10 MHz
duty = 50 %, tr = tf = 2.5 ns, C_L = 50 pF

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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