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High-Speed CMOS Logic IC HD74HC Series

Application Note

1. Input Protection Circuit

An Si-gate process is applied to Renesas's high-speed CMOS logic ICs. They have a thinner gate oxide compared to conventional Al-gate CMOS logic ICs and are composed into finer patterns.

Therefore, an input protection circuit is necessary for the gate to be protected from surges at the input pins.

Since Al-gate CMOS logic ICs use a diffusion resistor as the input protection resistor (as shown in Figure 1a), input over-current flows directly to the power supply and the destruction of the protection diode may occur.

On the other hand, using polysilicone as its input protection resistor (shown in Figure 1b), high-speed CMOS logic ICs take the role of a current limiter to counter input over voltage.

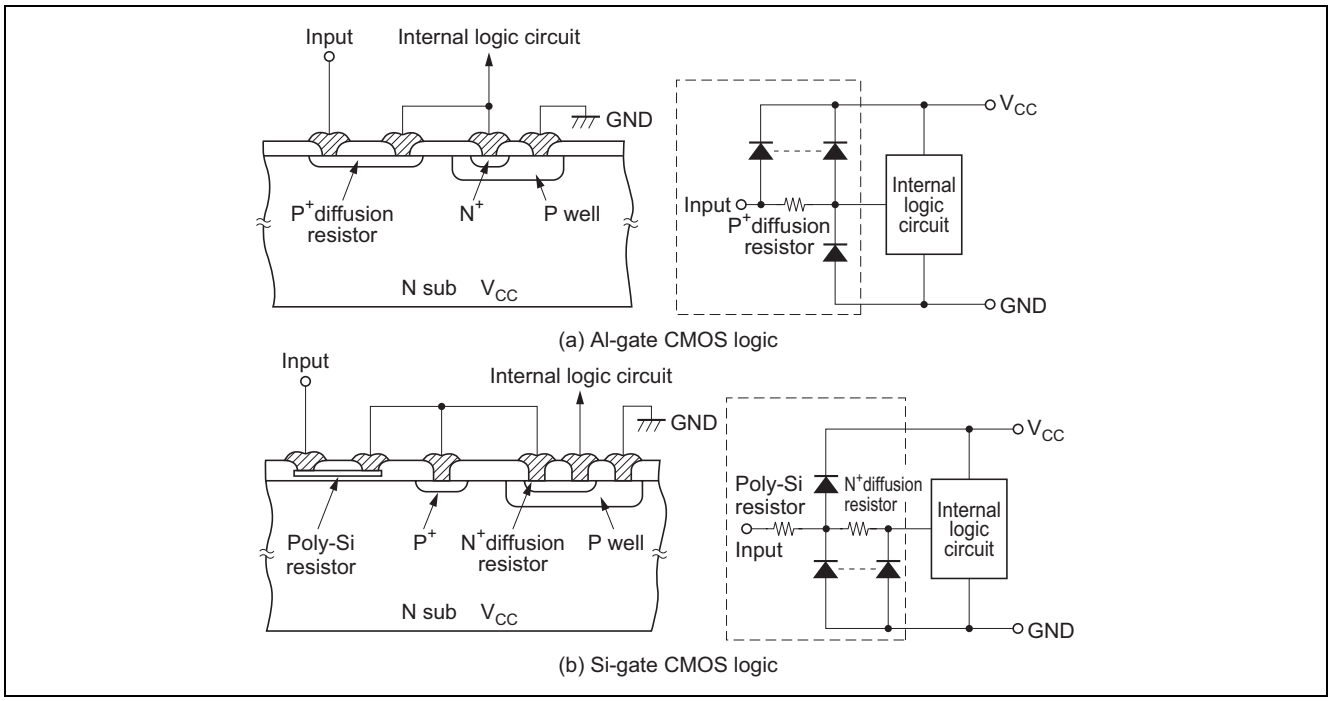


Figure 1 Input Protection Device and Equivalent Circuit

2. Electric Static Discharge Immunity (ESD Immunity)

ESD immunity is evaluated by the capacitor discharge method shown in the test circuit of Figure 2. The capacitor is 200 pF, accounting for the electrostatic capacitance of human bodies. Figure 3 shows an example of ESD immunity of integrated circuits for each products series.

The ESD for high-speed CMOS logic is over ±200 V, which is the same level or better than LS-TTL.

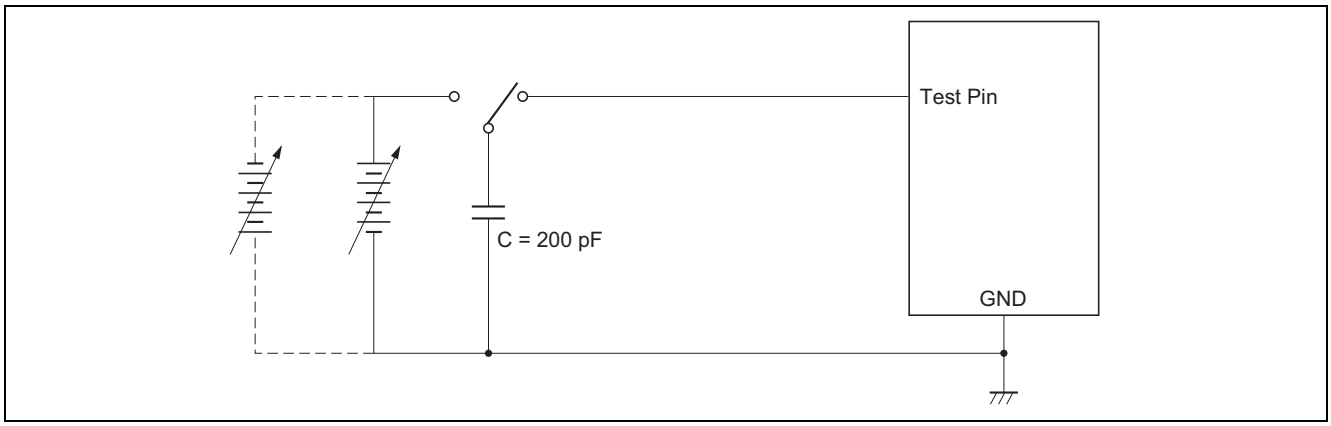


Figure 2 ESD Immunity Test Circuit

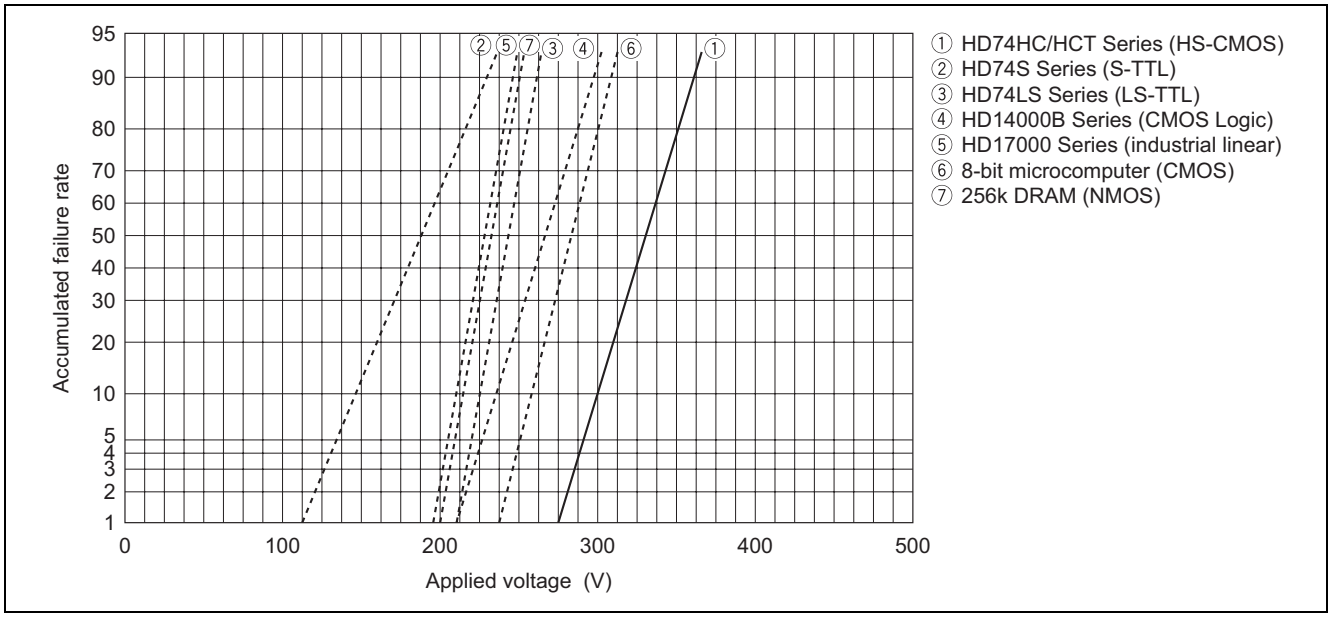


Figure 3 ESD Immunity for Each Series

3. Latch-Up

3.1 Latch-up

Latch-up is an inevitable phenomenon occurring from the basical structure of CMOS logic ICs.

Since CMOS has PMOS and NMOS on one chip, NPN and PNP transistors are made. These two types of transistors are combined into a PNPN structure, in which a parasitic thyristor is formed (see Figure 4).

If excessive noise is applied to the input or output pins when the IC is operating, the parasitic thyristor will turn on and the abnormal current will flow through the power supply pin to ground.

If the power supply is turned off, the IC will be restored to its normal state, however, the internal AI wiring of the IC may melt thus causing the IC to be destroyed.

There are countermeasures to prevent latch-up as listed below

(1) Separate PMOS from NMOS.
(2) Shut down electrical paths between PNP and NPN transistors which form parasitic thyristors by its layout pattern.
(3) Isolate each MOS transistor with an insulator to prevent the formation of parasitic thyristors.

Renesas's high-speed CMOS logic utilizes method (2)

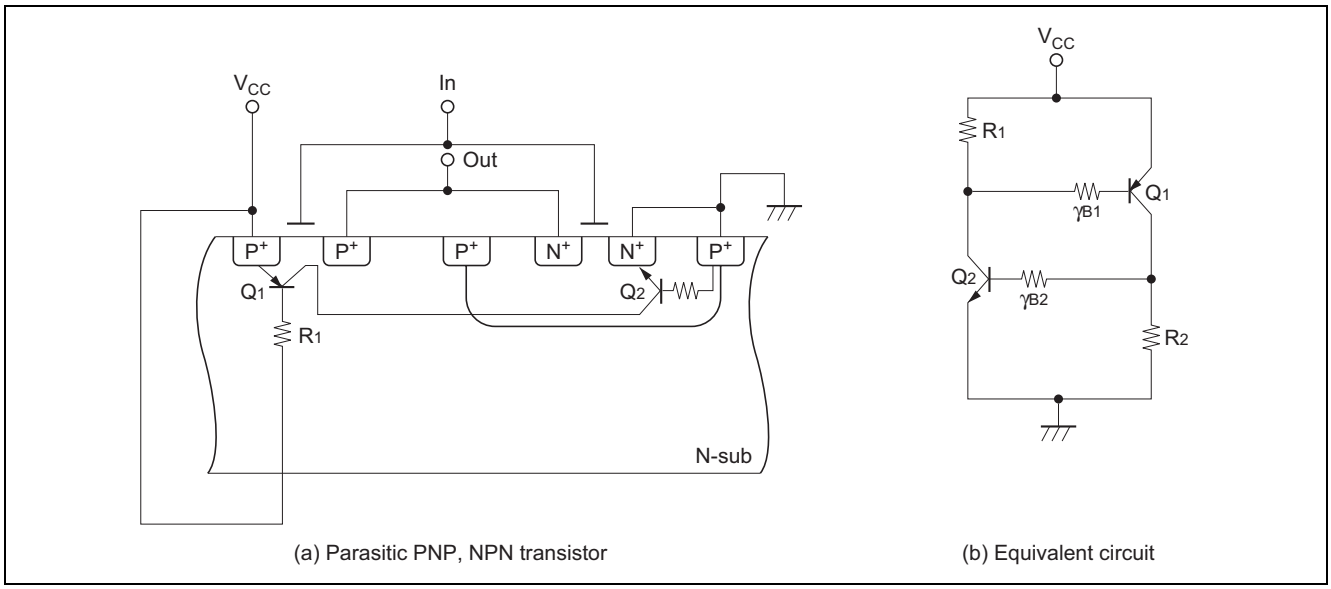


Figure 4 Parasitic Thyristor

3.2 Latch-Up immunity

Latch-up immunity is evaluated by the test circuit shown in Figure 5.

Table 1 lists the test results of latch-up immunity of Renesas's high-speed CMOS logic.

The starting voltage of high-speed CMOS logic is over ±300 V which causes almost no problems for practical use.

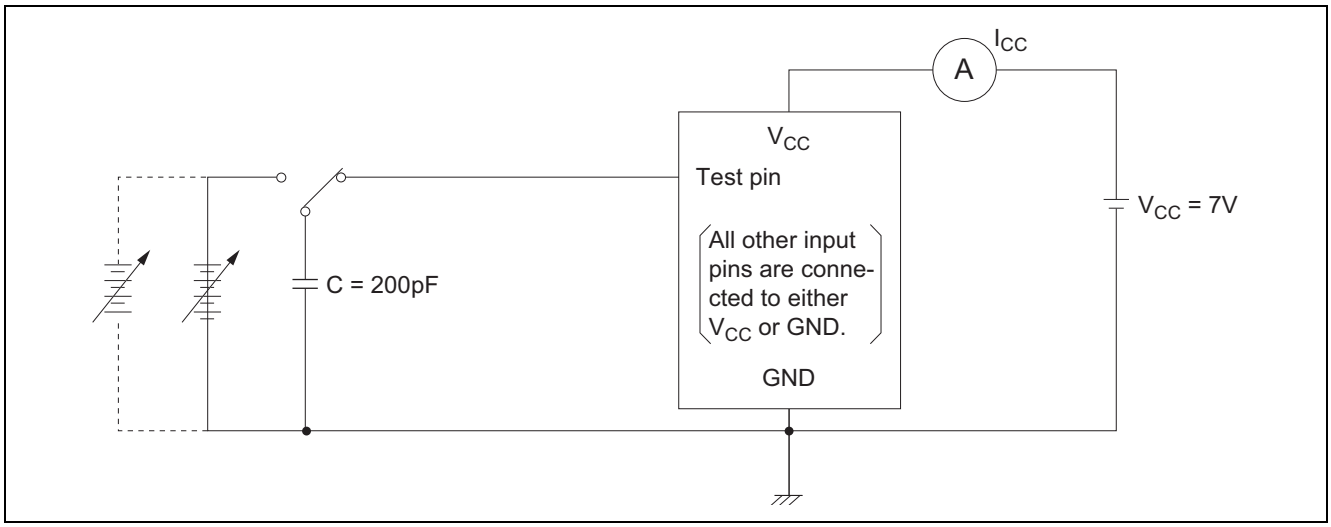


Figure 5 Latch-Up Immunity Test Circuit

Table 1 Latch-Up Starting Voltage Test Results

	Latch-up starting voltage
Positive	Over 300 V
Negative	Over 300 V

4. Electrical Characteristics

4.1 DC characteristics

(1) Logic threshold voltage (V_{TH})

The Logic threshold voltage (V_{TH}) of Renesas's high-speed CMOS logic ICs (HD74HC Series) is at half the level of V_{CC} in order to set up the widest noise margin possible.

(2) Output current characteristics

Renesas's high-speed CMOS logic ICs have symmetrical characteristics between I_{OH} and I_{OL}. Thus, the balance between t_{PLH} and t_{PHL} is mostly kept even when connecting with a comparatively large load capacitance.

Figures 7 and 8 show the output current characteristics.

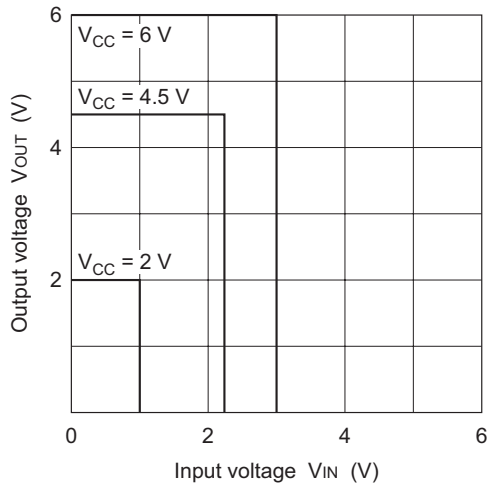


Figure 6 Output Voltage vs Input Voltage

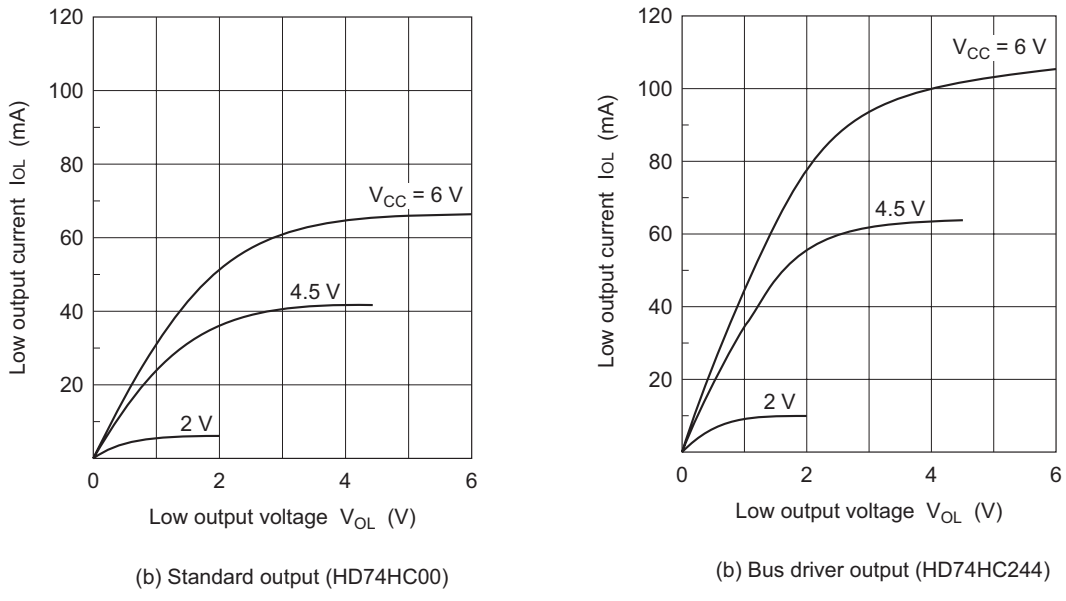
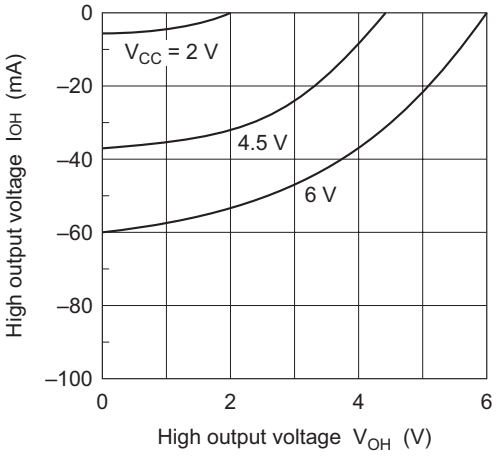
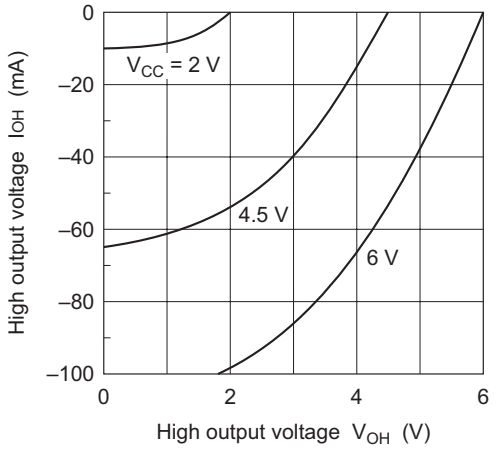


Figure 7 Output Current vs Voltage (Low Level)



(a) Standard output (HD74HC00)



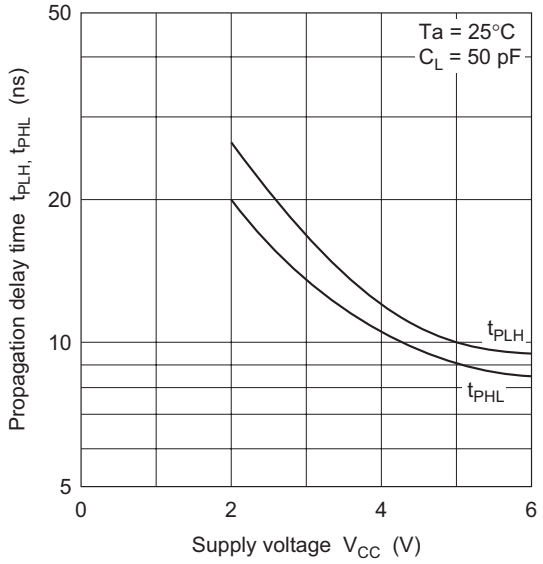
(b) Bus driver output (HD74HC244)

Figure 8 Output Current vs Voltage (High Level)

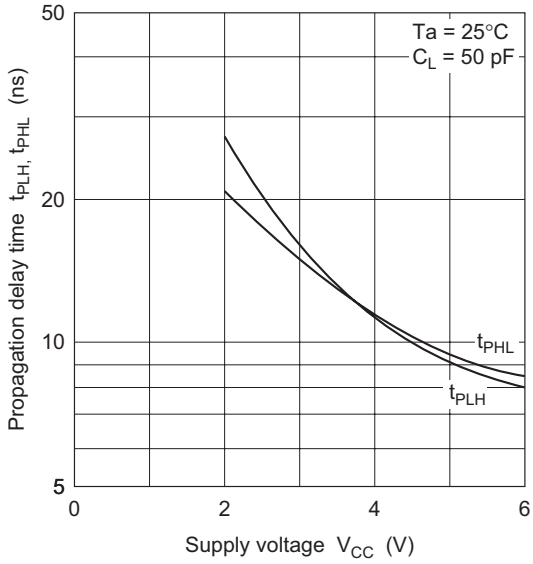
4.2 AC characteristics

t_{PLH} and t_{PHL} of Renesas's high-speed CMOS logic ICs are set up to be about the same to simplify system timing design.

(1) Propagation delay time, output rise and fall time vs supply voltage characteristics.



(a) Standard output (HD74HC00)



(b) Bus driver output (HD74HC244)

Figure 9 Propagation Delay Time vs Supply Voltage

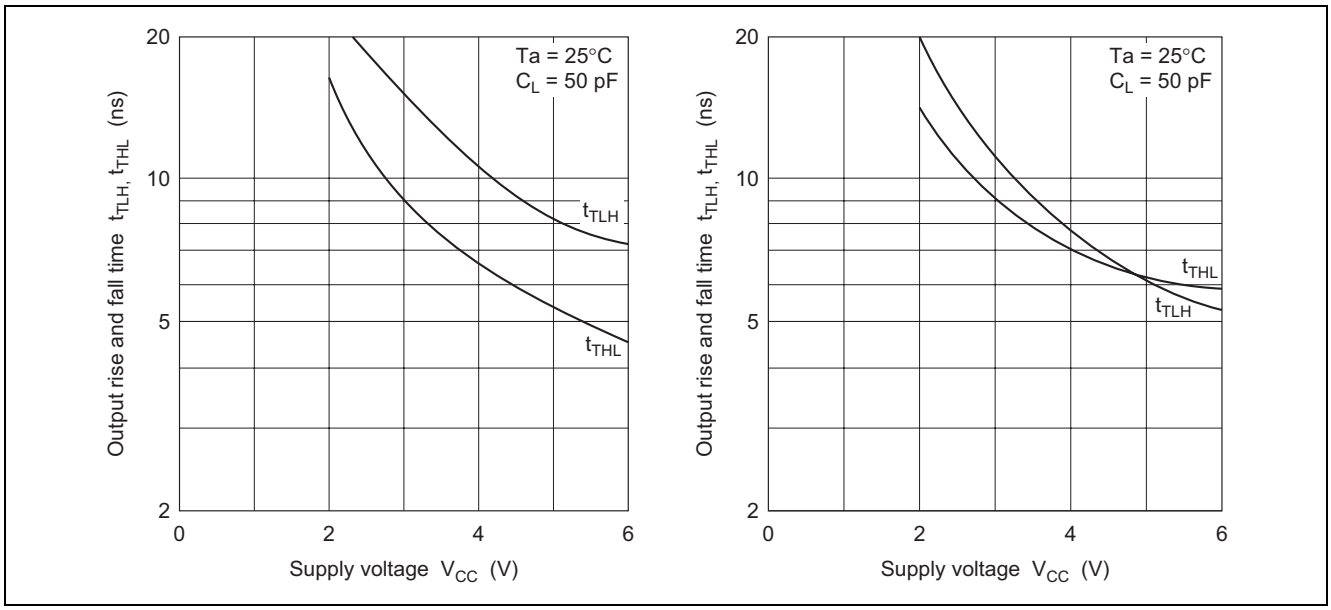


Figure 10 Output Rise and Fall Time vs Supply Voltage

(2) Propagation delay time, output rise and fall time vs load capacitance characteristics.

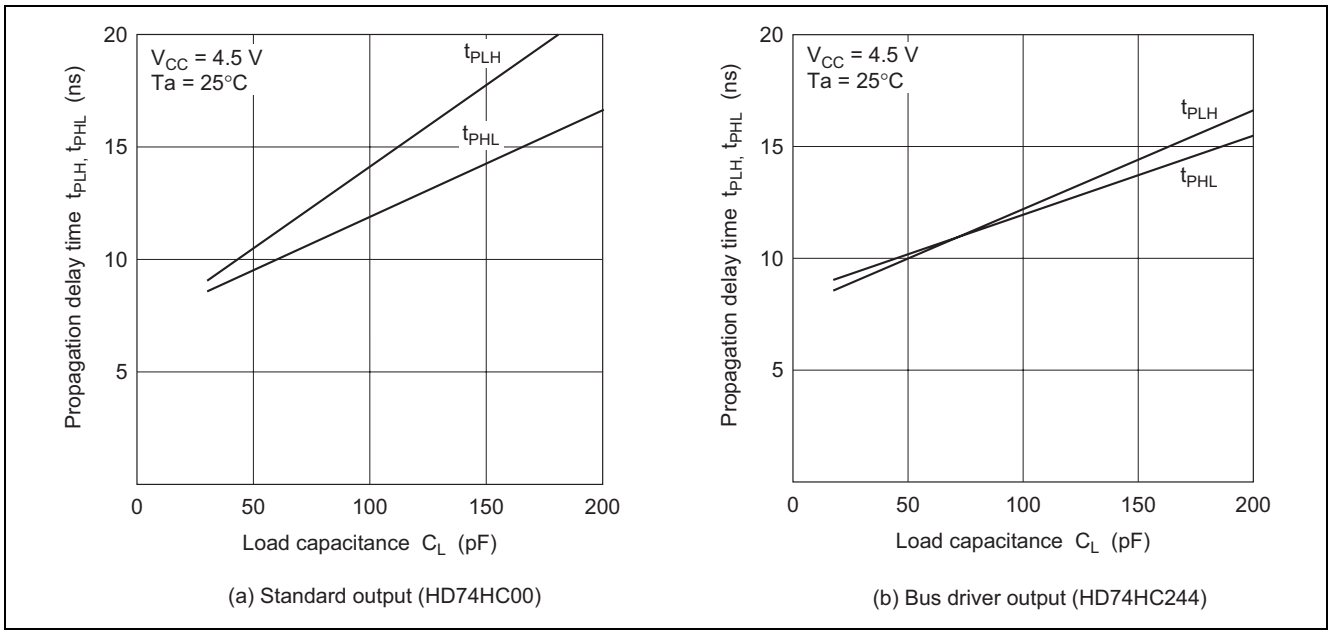


Figure 11 Propagation Delay Time vs Load Capacitance

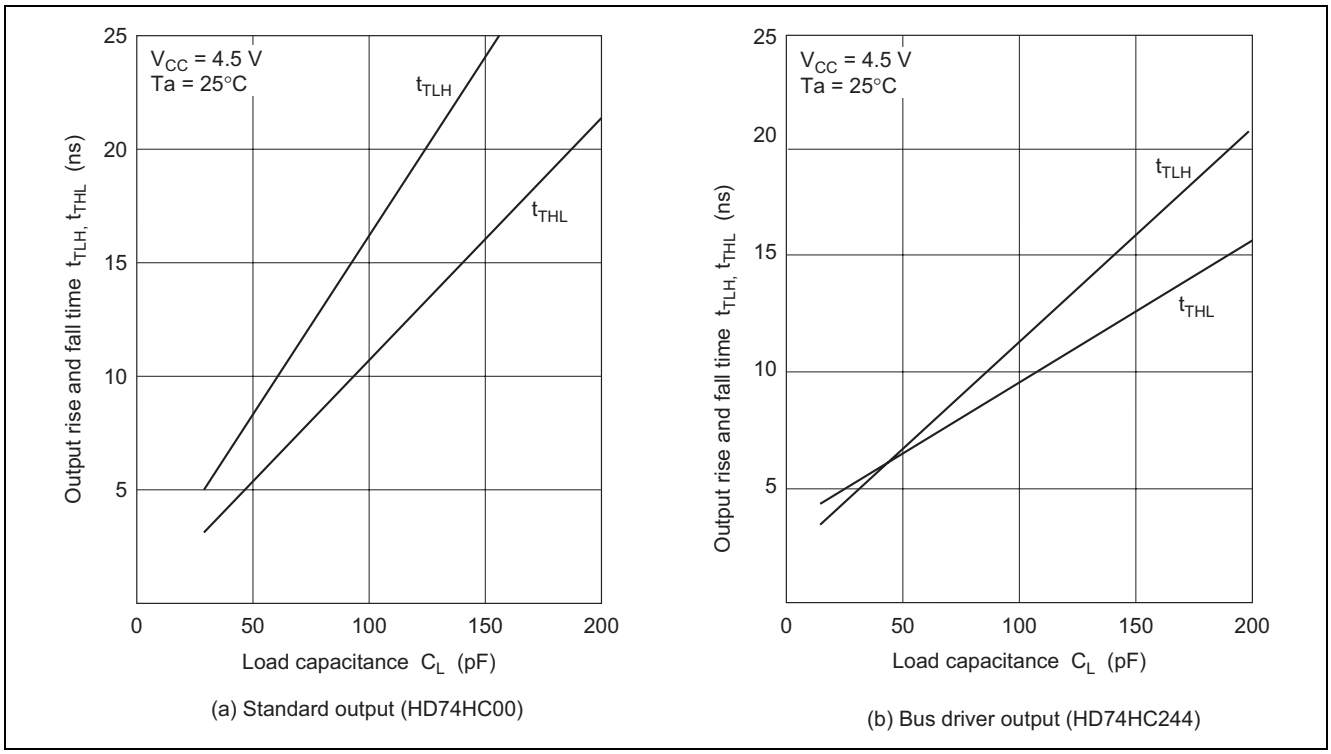


Figure 12 Output Rise and Fall Time vs Load Capacitance

5. Power Dissipation

5.1 Calculating the power dissipation

The power dissipation P_T of high-speed CMOS logic can be calculated by (1). From this equation, the power dissipation depends on the load capacitance, frequency and supply voltage.

$$P_T = (C_L + C_{PD}) \cdot f \bullet V_{CC2} \qquad (1)$$

Figure 13 shows examples of the operating frequency with the power supply current.

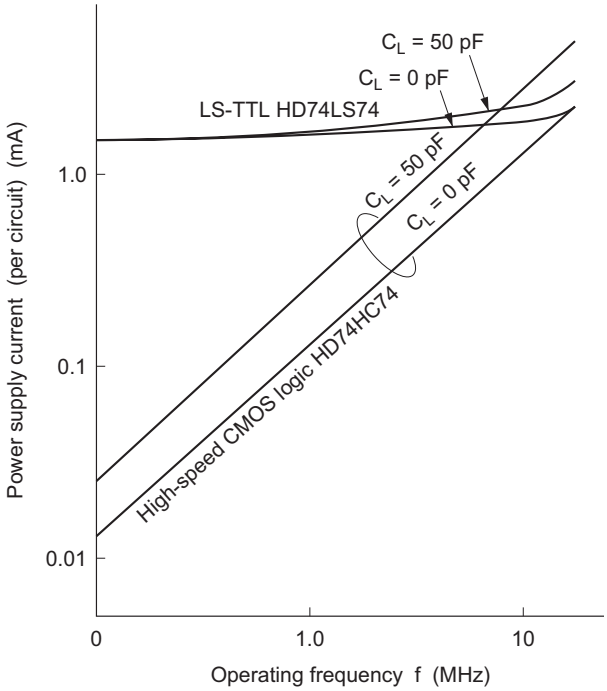


Figure 13 Operating Frequency vs Power Supply Current

5.2 Power dissipation capacitance

Power dissipation capacitance (Cpd) can be calculated by the following equations,

$$P_{T1} = C_{PD} \bullet V_{CC}^2 \bullet f_1 = I_{CC1} \cdot V_{CC} \quad (2)$$

$$P_{T2} = C_{PD} \bullet V_{CC}^2 \bullet f_2 = I_{CC2} \cdot V_{CC} \quad (3)$$

therefore,

$$C_{pd} = \frac{P_{T2} - P_{T1}}{V_{CC}^2 \times (f_2 - f_1)} = \frac{I_{CC2} - I_{CC1}}{V_{CC} \times (f_2 - f_1)} \quad (4)$$

then,

- I_{CC1} : Supply current at frequency f_1
- I_{CC2} : Supply current at frequency f_2

Table 2 lists the power dissipation capacitance of Renesas's high-speed CMOS logic.

Furthermore, the power dissipation capacitance differs according to the input conditions.

Table 3 shows typical examples.

Table 2 Power Dissipation Capacitance of High-Speed CMOS

Function		Product part no.	Note 1	Power dissipation capacitance typ. (pF)
Gate		HD74HC00	*	27
		HD74HC04	*	24
Flip-Flop	D-type	HD74HC74	*	41
	J-K-type	HD74HC76	*	49
COMPARATOR		HD74HC85	P	48
DECORDER		HD74HC138	P	90
COUNTER		HD74HC161	P	57
BUFFER		HD74HC240	*	42
MULTIPLEXER		HD74HC258	P	78
LATCH		HD74HC373	P	57

Notes: 1. *:Per circuit; P: Per package.
2. Measurement circuit is shown in figure 14.

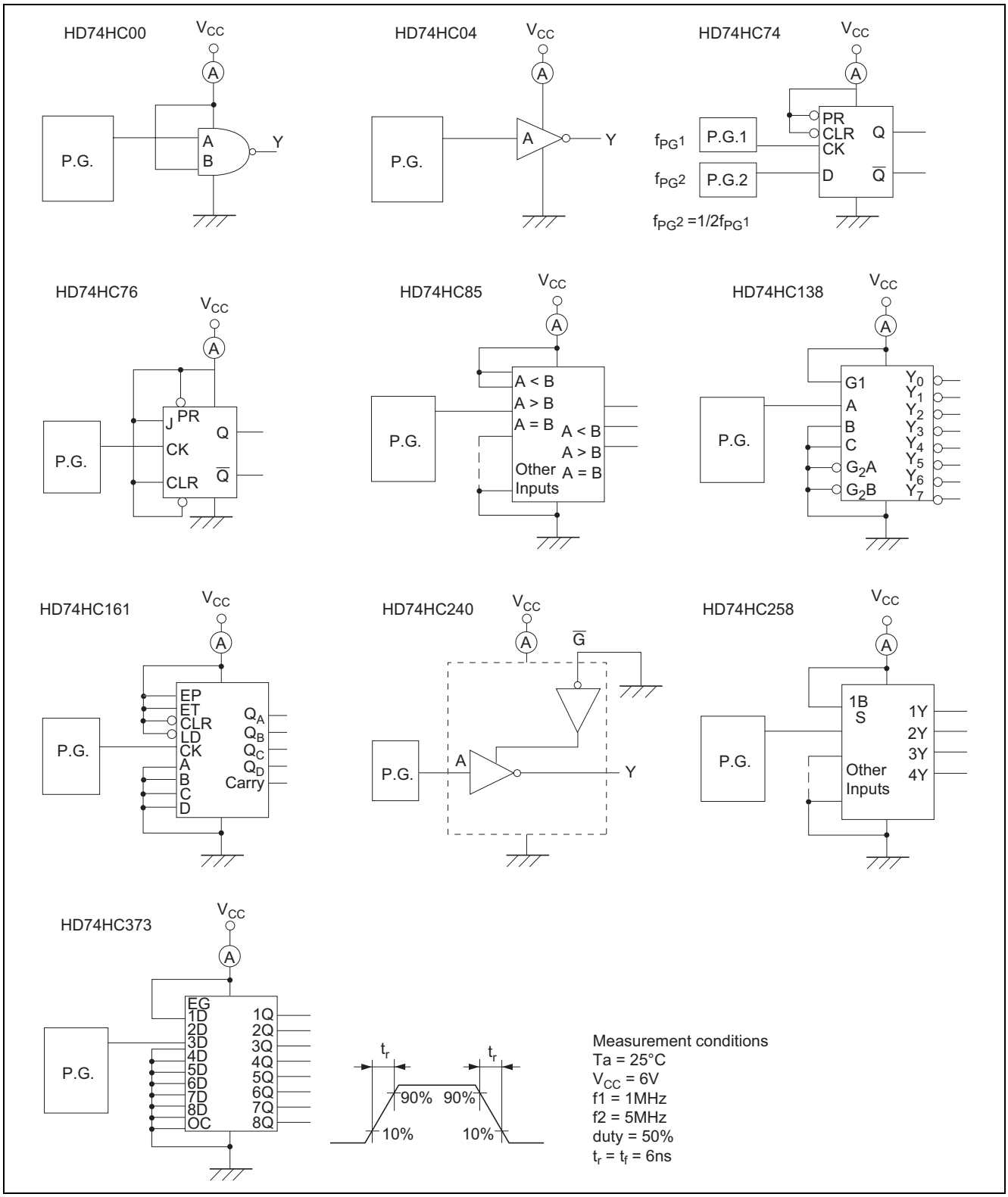
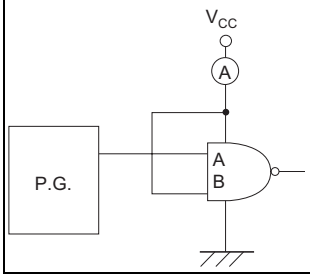
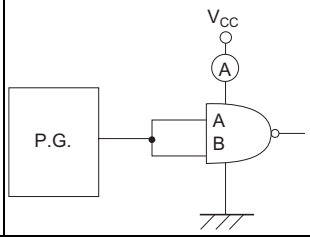
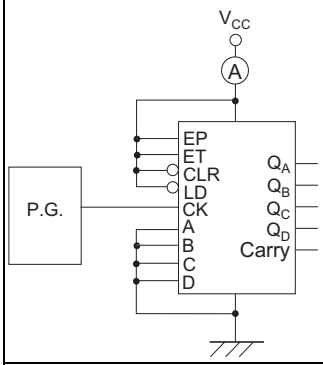
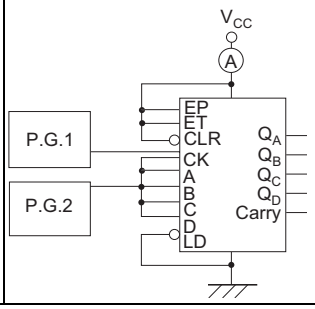


Figure 14 Measurement Circuits for Dynamic Power Supply Current

Table 3 Power Dissipation Capacitance by Input Conditions

Product part no.	Input conditions	Power dissipation capacitance (pF)
HD74HC00	Single input 	27
	Double input 	27
HD74HC161	Counting operation 	57
	Preset operation 	113

6. Decoupling

CMOS logic ICs have current spikes when switching. These spikes are produced by the repeated charging and discharging of the output capacitance when charging the output level from low to high or high to low.

Because of the current spikes the potentials of V_{CC} and GND change, and large current spikes flow when switching. Therefore ringing is produced at the output. (See Figure 15 a.)

To prevent this, decoupling capacitors must be provided externally between V_{CC} and GND.

This is proven to be useful in instantly absorbing the current and ringing at the output as shown in Figure 15 b.

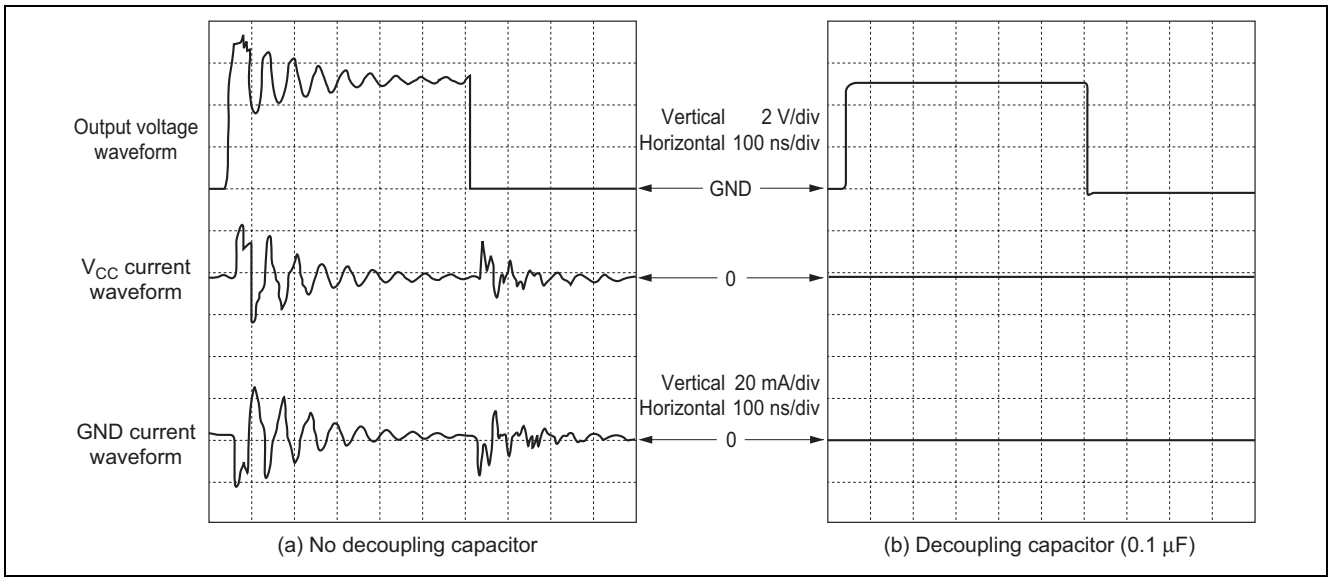


Figure 15 HD74HC00 Spike Current Waveform

7. Precautions on Board Design

High-speed CMOS logic has different electrical characteristics, such as switching speed and output current drivability, from the conventional standard logics (Al-gate CMOS, LS-TTL). The system design requires an application technique for high-speed CMOS logic.

Here an interfacing technique between high-speed CMOS logic and LS-TTL will be explained.

7.1 Transmission line reflection

(1) Analysis of transmission signals by the Bergeron diagram The Bergeron diagram is commonly used for the analysis of transmission signals in high-speed digital systems.

Figure 17 is the analysis result of an actual transmission model which is shown in Figure 16.

As for the analysis conditions, Z_0 = 125 Ω considering the standard system board, and the wiring length (l) is 1.5 m.

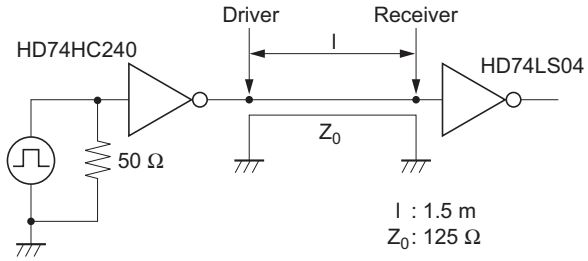
The output impedance of the HD74HC04, which operates as a driver becomes the $I_{OH} – V_{OH}$ characteristic curve when the output is high, and the input impedance of the HD74LS04 which operates as a receiver becomes the IIH - VIH characteristic curve.

On the other hand, when the output level of the HD74HC04 is low, the output impedance becomes the $I_{OL} – V_{OL}$ characteristic curve and the input impedance becomes the $I_F – V_F$ characteristic curve.

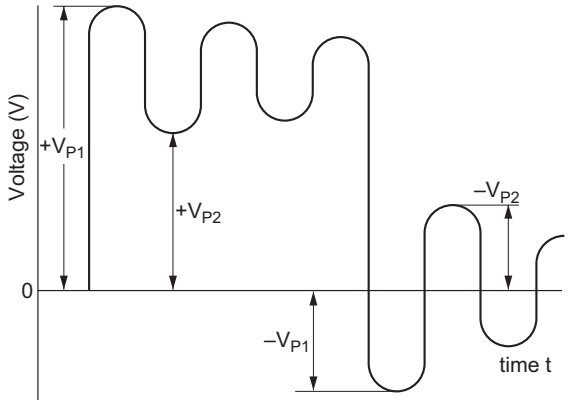
The drawing of load line Z_0 as these input/output impedance curves enables the reflection of the transmission signal to be analyzed.

The intersection coordinates in Figure 17 shows the voltage and current values at the drive end of 2T (T being the propagation delay from the driver end to the receiver end) intervals when the coordinates are even numbers (2T, 4T) or zero, or the voltage and current values at the receiver end when the coordinates are odd numbers (T, 3T, 5T).

Figure 18 shows the analysis result of the voltage waveform at the receiver end.



(a) Digiral signal transmission model circuit



(b) Receiver waveform model

Note: The model circuit above (Figure 16a) is used for analysis when the high-speed CMOS logic HD74HC240 is connected as a driver, and the LS-TTL HD74LS04 as a receiver
The waveform model for overshoot and undershoot at the receiver end is shown in Figure 16b.

Figure 16 Digital Signal Transmission

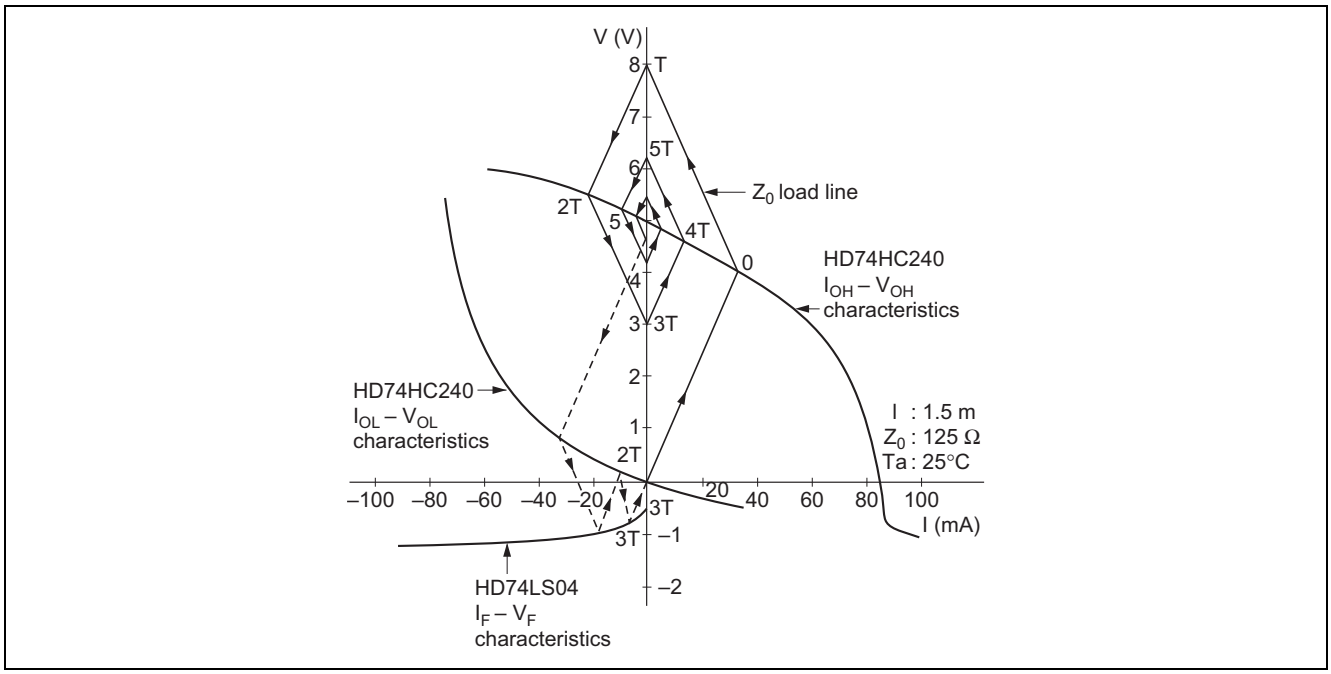


Figure 17 Bergeron Diagram Analysis of the Transmission Model

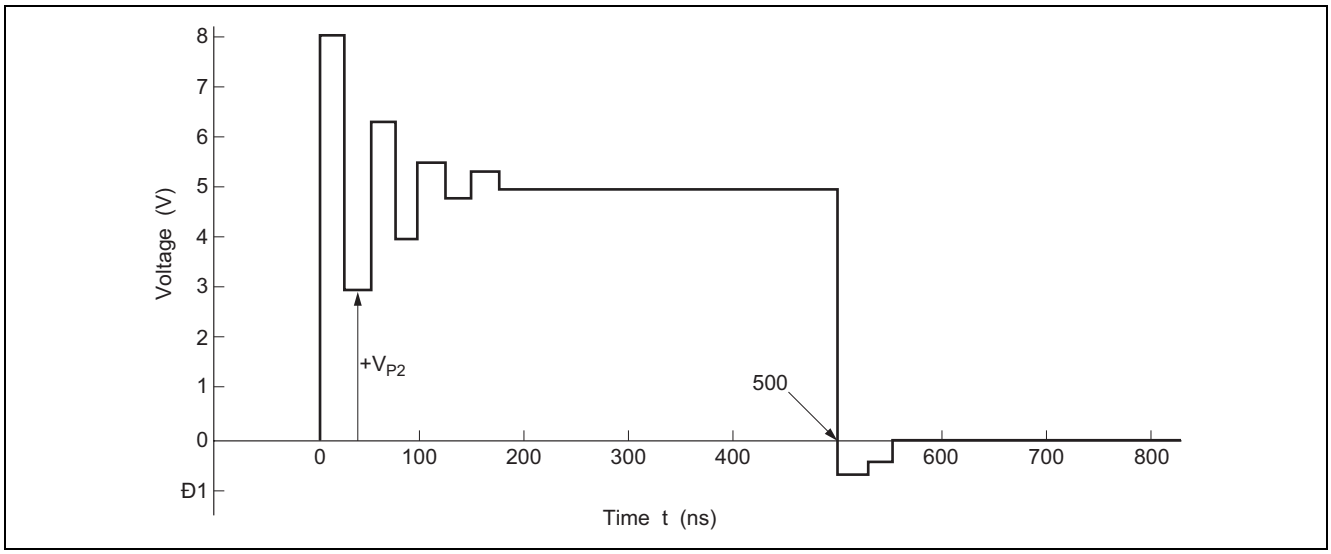
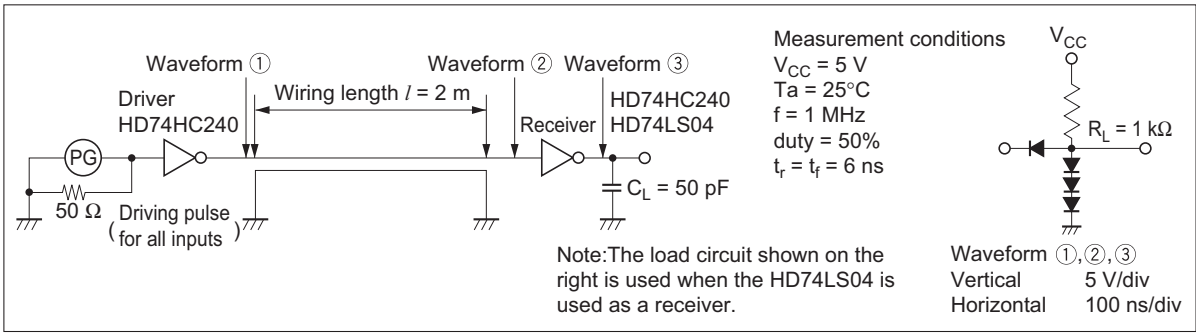


Figure 18 Analysis Results of the Waveform at the Receiver End

(2) An example for measuring the reflection on the transmission line Figure 19 shows the measured results of the reflection of the transmission line using three types of transmission line media such as 1) coaxial cable (Z_0 = 50 Ω), 2) twisted pair cable (Z_0 = 120 Ω), and 3) single lead wire (Z_0 = 150 to 200 Ω).
Figure 19 shows that the drivers and receivers operate normally with a wiring length of up to 2 m.
However, careful precautions should be taken when considering impedance in practical system designing.



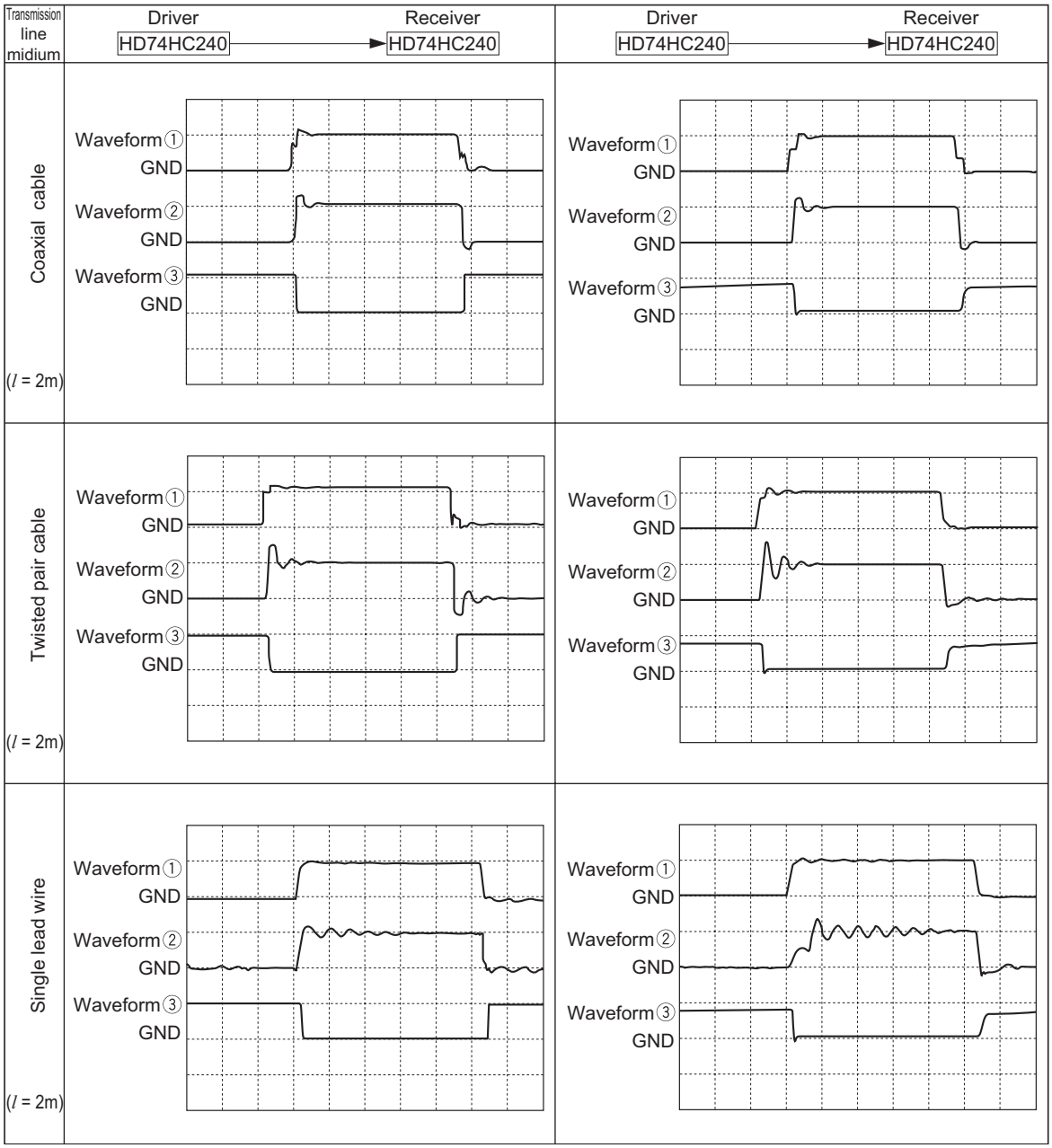


Figure 19 Reflection Ringing Waveforms (Driver: HD74HC240)

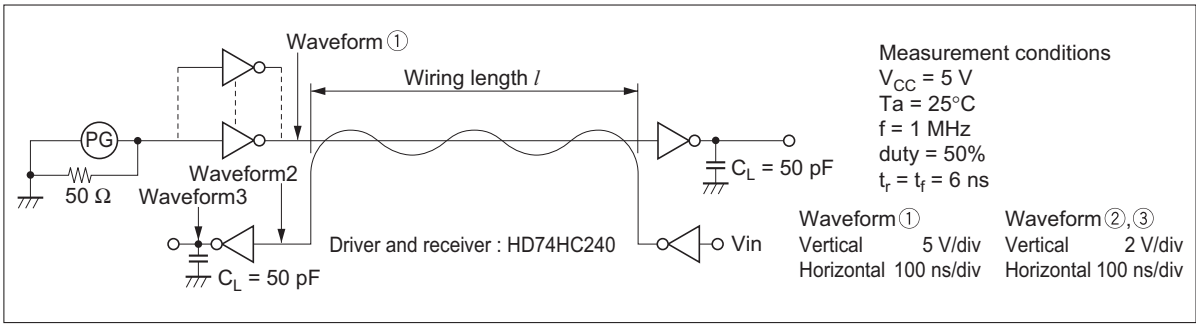
7.2 Crosstalk

Crosstalk is the capacitative coupling of signals from one line to another.

Figure 20 shows an example of crosstalk noise levels using a twisted pair cable.

Figure 20 also shows that the wiring length beyond 1 m causes malfunction.

Careful precautions should be taken especially when the spacing between circuits is narrow.



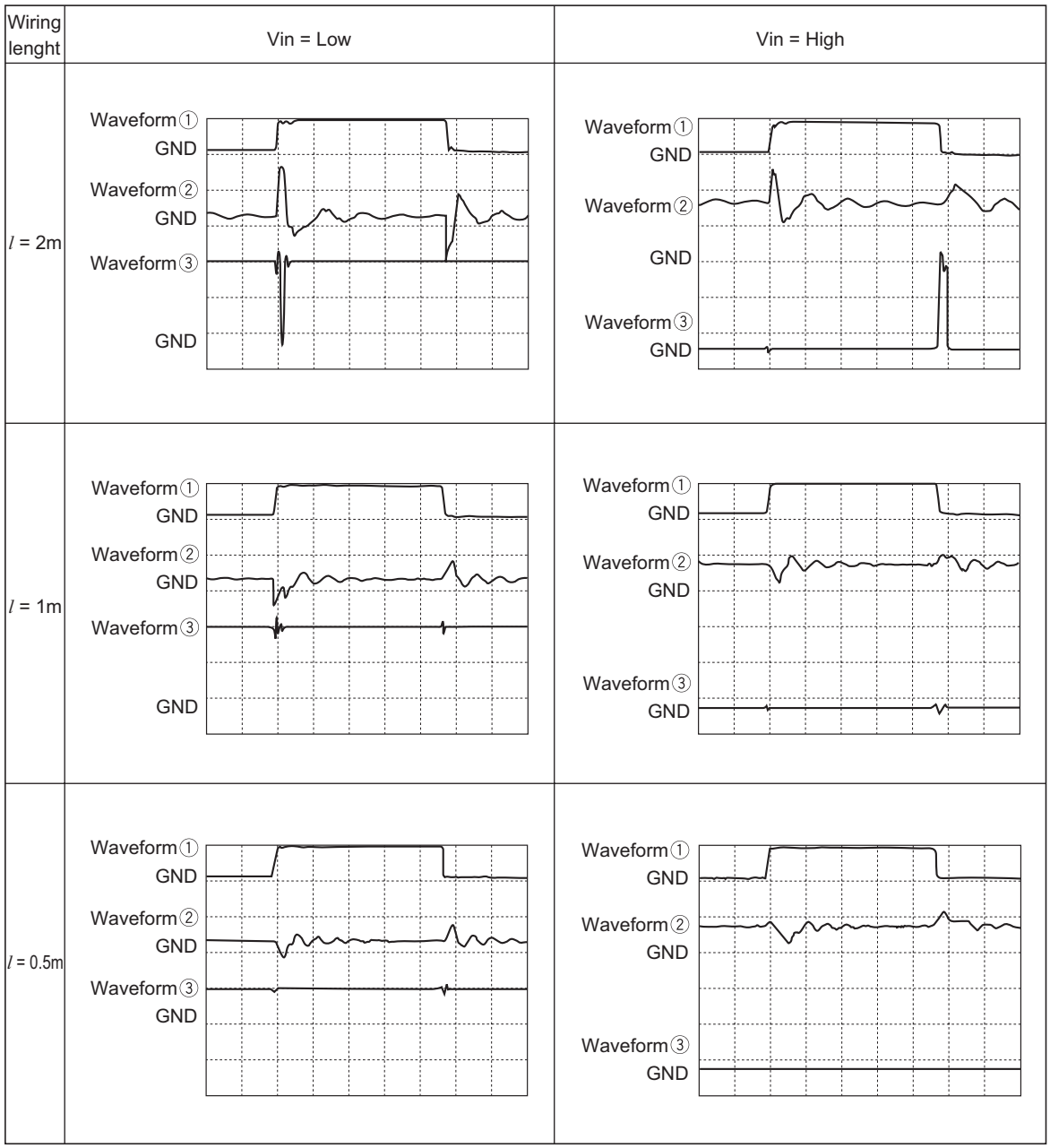


Figure 20 Crosstalk Noise Waveform (Driver: HD74HC240)

8. Interfacing

Renesas's high-speed CMOS logic has two types of input voltage levels, 74HC and 74HCT.

The 74HC has a CMOS-type input level and the 74HCT has a TTL-type input level.

Interfacing from high-speed CMOS logic to LS-TTL

Since the output level of high-speed CMOS logic is of CMOS, the use of an interfacing circuit is not necessary.

This is the same case for a microcomputer and memory IC with TTL input levels.

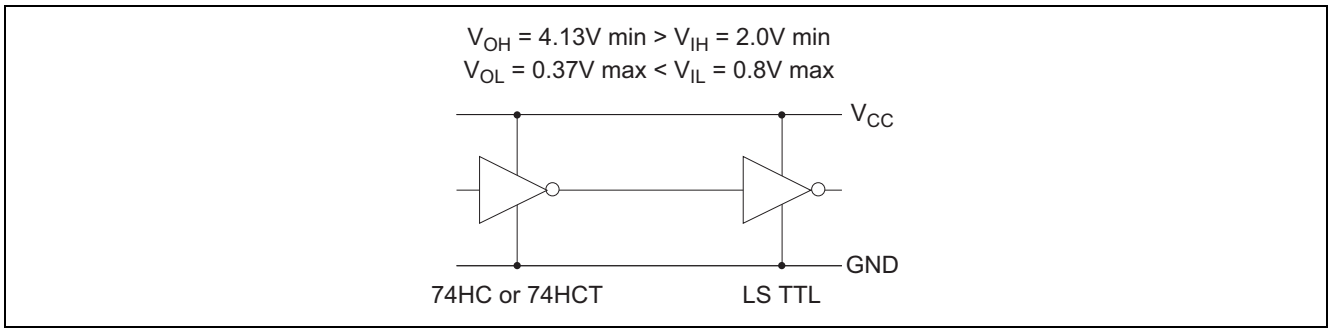


Figure 21 Interfacing HS-CMOS to LS-TTL

Interfacing from LS-TTL to high-speed CMOS logic (74HCT type)

An interfacing circuit is not necessary.

This is the same case for a microcomputer and memory IC with TTL output levels.

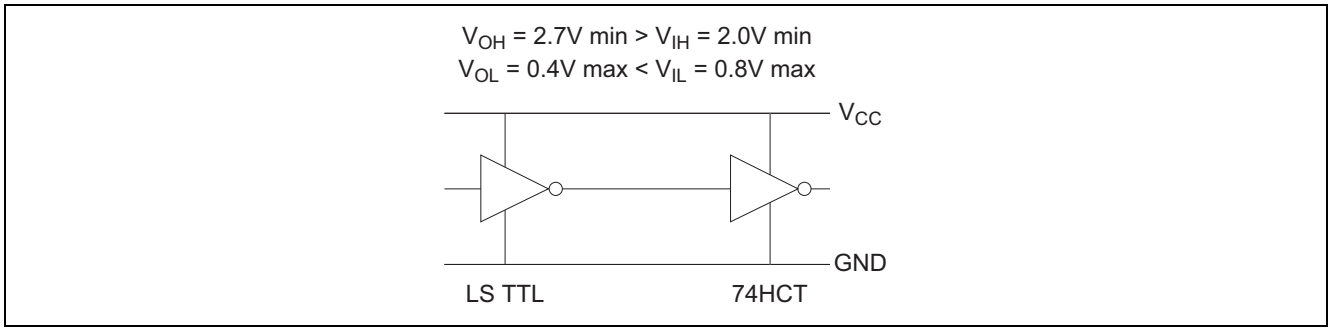


Figure 22 Interfacing LS-TTL to 74HCT

Interfacing from LS-TTL to high-speed CMOS logic (74HC type)

A pull-up resistor should be added as shown in Figure 25.

The output voltage of LS-TTL (V_{OH}) is 2.7 V (min), where as the input voltage of 74HC (V_{IH}) is 3.15 V (min.).

This implies that LS-TTL cannot drive 74HC types directly.

This is the same case for a microcomputer and memory ICs with TTL output levels.

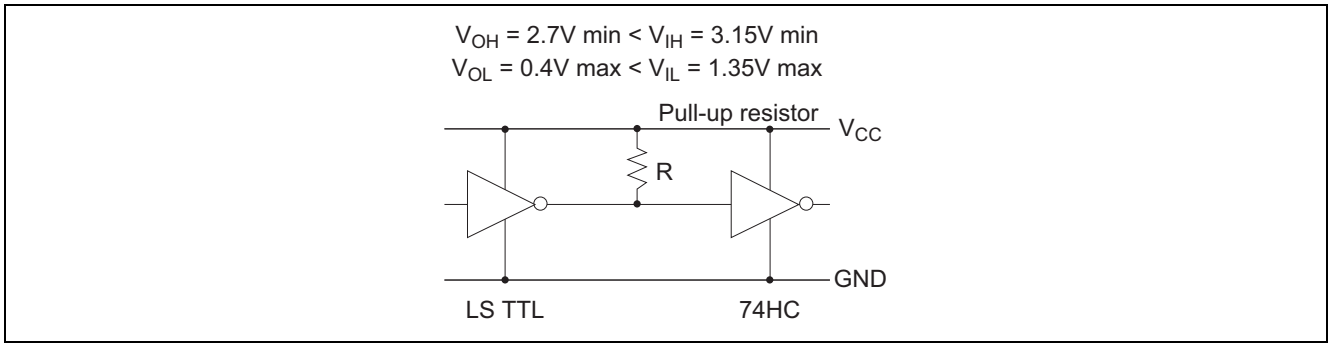


Figure 23 Interfacing LS-TTL to 74HC

Interfacing from LS-TTL with 3-state output to high-speed CMOS logic.

A pull-up or pull-down resistor should be added as shown in Figure 26.

When the output of a LS-TTL is in the high-impedance state, the input of the high-speed CMOS becomes unstable.

This is the same case for all devices with a tri-state output structure.

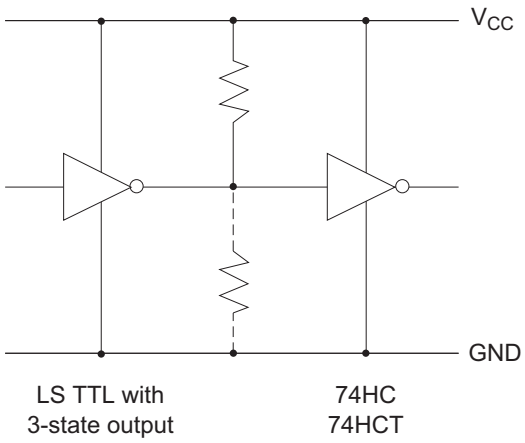


Figure 24 Interfacing LS-TTL with 3-state Output to 74HC or 74HCT

9. Surface Mount Package

9.1 Mounting small outline packages (SOP, TSSOP)

The explanation on the mounting of SOPs describes the characteristics and reliabilities of the small IC package.

(1) Dip Soldering

Initially, the package is temporarily fixed on to the board by an adhesive.

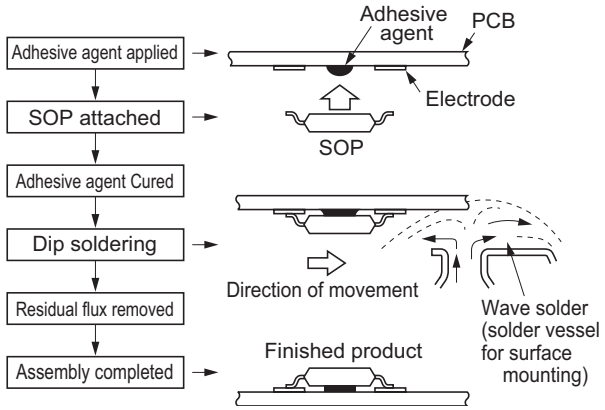


Figure 25 Process Flow for Dip Soldering SOP

With the component side of the board downward, the package is then passed through molten solder. Figure 27 depicts the process flow for dip soldering SOP. As compared with reflow methods, this method exerts an extremely high thermal stress on the semiconductor chips. The adverse effects from this thermal should be avoided by providing a preheating zone to lessen the thermal shock and by minimizing the soldering time. Figure 28 shows a typical temperature profile for dip soldering.
The dip soldering temperature is 260˚C maximum at a period of 10 seconds maximum (2 to 4 seconds is recommended).

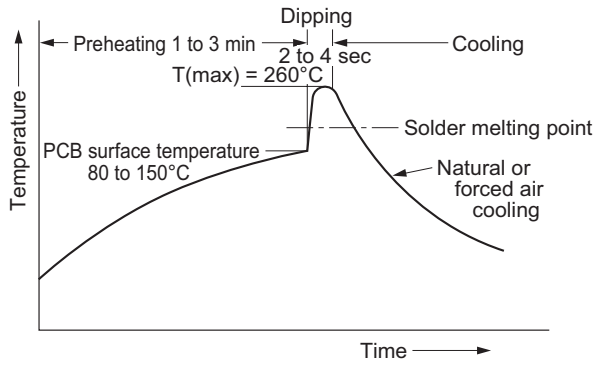


Figure 26 Temperature Profile of Dip Soldering

(2) Reflow Soldering

Reflow soldering is the basic method of mounting the SOP on to a board.

The solder composition to be used is Sn63/Pb37 or Sn62/Pb36/Ag2 with a melting point of 183°C to 193°C.

A recommended pasty flux is solder cream SP210-2 by Tamura Kaken. A pasty flux and organic solvent are also used during the process.

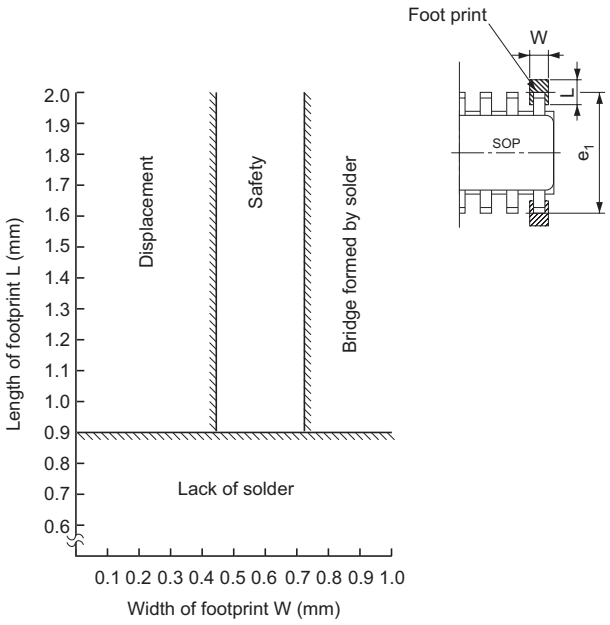
Be careful to reflow solder at a low temperature for short periods of time. The recommended conditions are shown below. The allowable board temperature is 230°C maximum and the maximum heating time is 15 sec.

(3) Footprint dimension vs solderability

The failure rate of soldering is affected by footprint dimensions. Figure 29 shows the soldering failure with the footprint dimension.

The recommended dimensions are within the safety zone of this figure.

When reflow sordering SOPs, the recommended thickness of a footprint is 0.2 mm min.



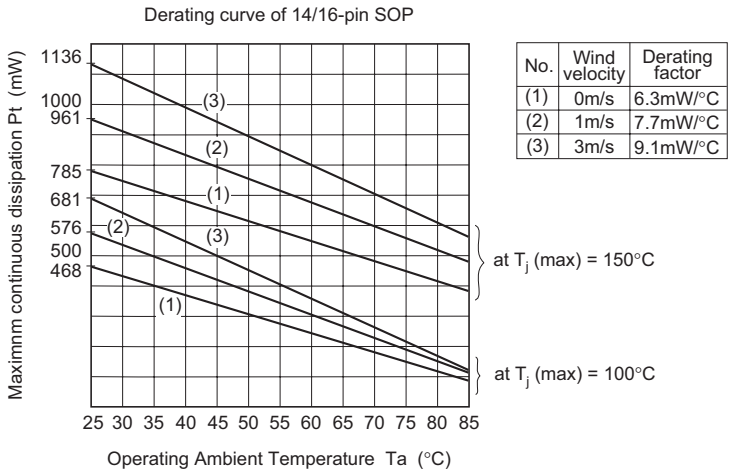
Notes: 1. Pin pitch = 1.27 mm

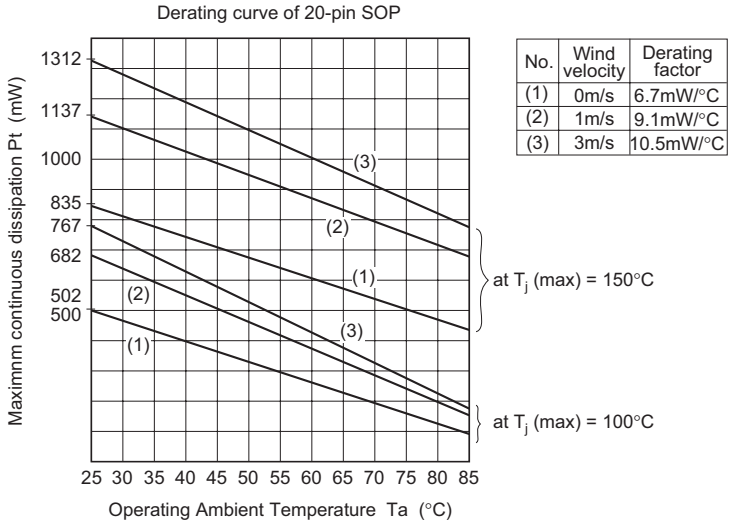
2. Recommended spacings between footprint centers.
   e_1 = 7.62 mm (SOP-14, 16)
   e_1 = 9.53 mm (SOP-20)
3. Both W and L are footprint dimensions based on the lead direction of the SOP.

Figure 27 Recommended Dimension of Footprint

(4) Thermal Resistance of SOP

Figure 30 shows the derating curves for SOPs of high-speed CMOS logic, and Table 6 lists the thermal resistance (θj-a) for SOPs.





Note: When Ta is below 25°C, P_T becomes the same value as at Ta = 25°C being independent of Ta.
The data above was measured by using the ΔV_{BE} method on a glass-epoxy board (40 × 40 × 1.0 mm) with wiring density of 10%.
Careful considerations are required for input and load conditions, Ta, cooling, etc., during actual use.

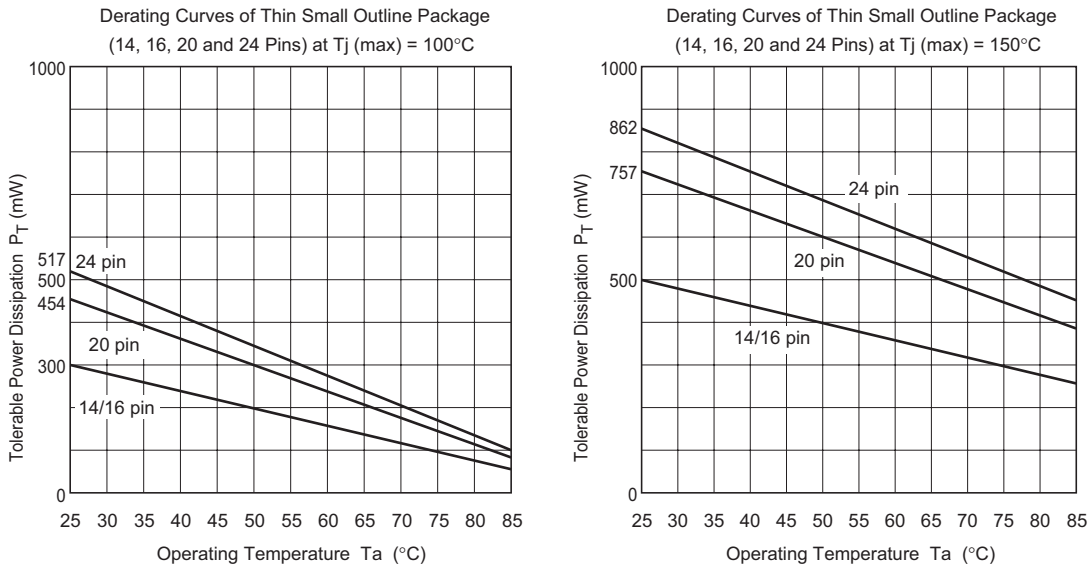
Figure 28 Derating Curves of SOP

Table 6 Thermal Resistance of SOPs

Number of pins	Wind velocity	Derating factor	Thermal resistance	Maximum continuous dissipation Ta = 25°C	
				Tj(max) = 150°C	Tj(max) = 100°C
14	0 m/s	6.3 mW/°C	160°C/W	785 mW	468 mW
16	1 m/s	7.7 mW/°C	130°C/W	961 mW	576 mW
	3 m/s	9.1 mW/°C	110°C/W	1136 mW	681 mW
20	0 m/s	6.7 mW/°C	150°C/W	835 mW	502 mW
	1 m/s	9.1 mW/°C	110°C/W	1137 mW	682 mW
	3 m/s	10.5 mW/°C	95°C/W	1312 mW	787 mW

(5) Thermal Resistance of TSSOP

Figure 29 shows the derating curve of TSSOP with HD74BC/AC/HC devices, table 7 shows the thermal resistance (θj-a) and figure 30 shows the mounting method.



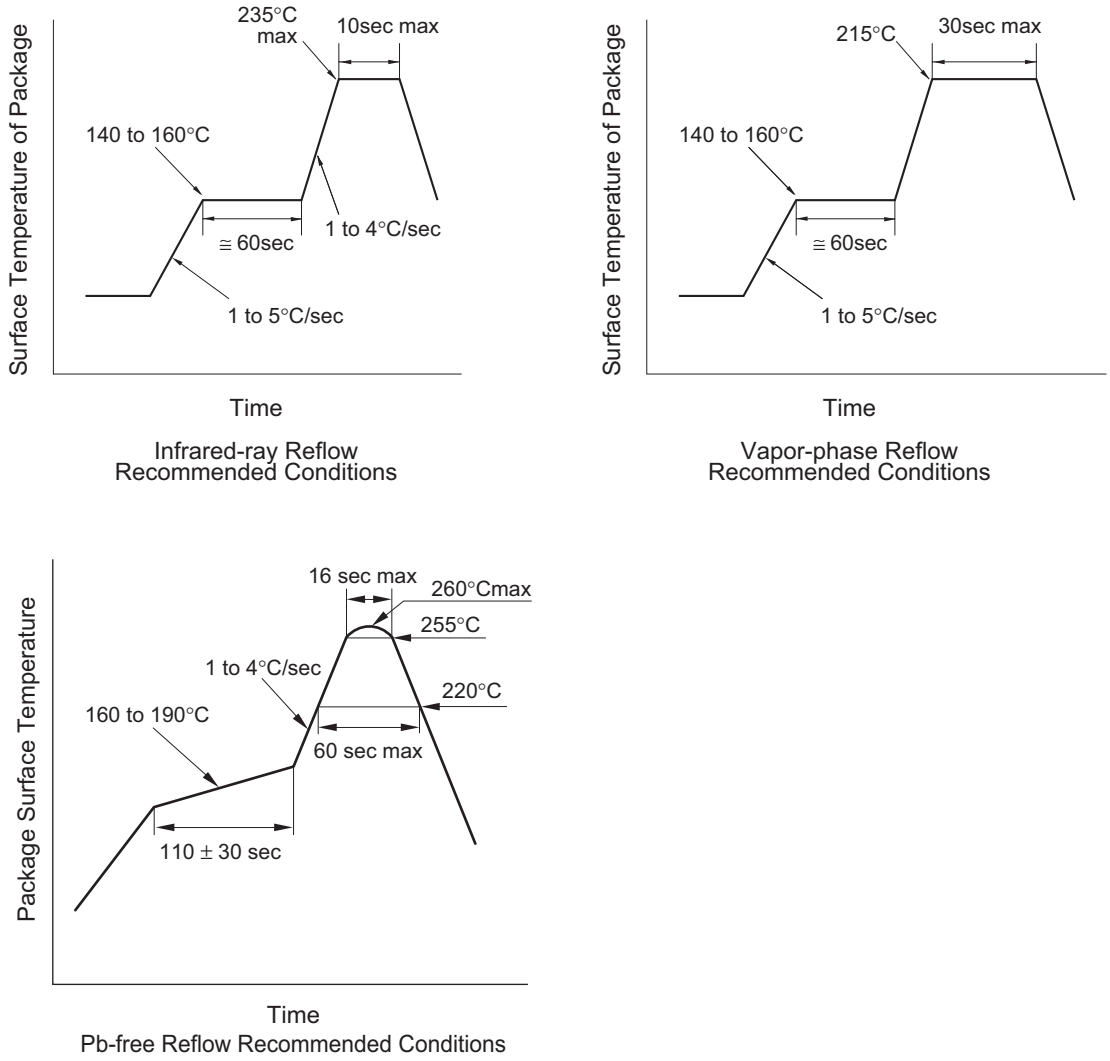
Note: Fore the ambient temperature less than 25°C, the power dissipation at 25°C is applied. The data above are measured by ΔV_{BE} method mounting on glass epoxy board (40 × 40 × 1.6 mm) with 10% of wiring density. In the actual application, using conditions, ambient temperature and forced air-cooling conditions should be sufficiently examined.

Figure 29 Derating Curve of TSSOP

Table 7 Thermal Resistance of TSSOP Package

Number of pins	Wind velocity	Derating factor	Thermal resistance	Tolerable power dissipation	
				at Tj(max) = 150°C	at Tj(max) = 100°C
14, 16	0 m/s	4.0 mW/°C	250°C/W	500 mW	300 mW
20	0 m/s	6.1 mW/°C	165°C/W	757 mW	454 mW
24	0 m/s	6.9 mW/°C	145°C/W	862 mW	517 mW

(6) TSSOP Solder Mounting

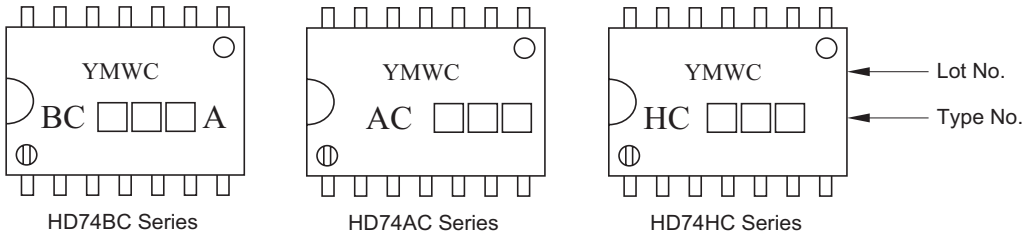


Recommended: For the whole heating on solder mounting, infrared-ray reflow and vapor-phase reflow are recommended. (Solder-dipping is not recommended.)

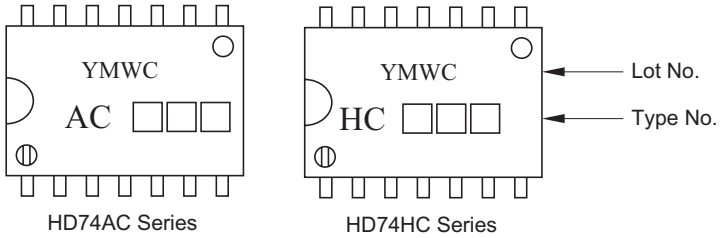
Figure 30 Mounting Method of TSSOP

(7) Marking on Package

(a) Small outline Package (EIAJ) 14, 16, 20 pins

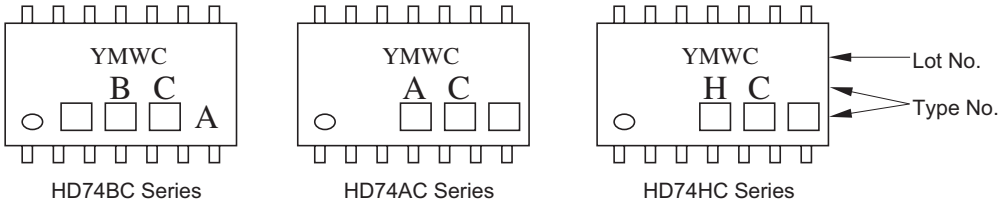


(b) Small outline Package (JEDEC) 14, 16, 20 pins



Note: Meaning of marking on package example device name:
HD74AC245RP
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (RP) from device name

(c) Thin Shrink Small outline Package 14, 16, 20 pins



Note: Meaning of marking on package example device name:
HD74BC245AT
Y: Year code (the last digit of year)
M: Month code
W: Week code
C: Control code
Type No.: delete HD74 and package code (T) from device name

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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