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CMOS Logic IC HD74AC Series (FACT)

Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Renesas's Advanced CMOS helps designers achieve these goals.

FACT (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading, and a 50 Ω transmission line drive capability to offer a complete family of SSI and MSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

There are five items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing—interboard and technology interfaces, battery backup, and power down or live insert/ extract systems require some special thought.
- Transmission line driving—FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects—As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board layout—Prudent board layout will ensure that most noise effects are minimized.
- Power supplies and decoupling—Maximize ground and V_{CC} traces to keep V_{CC}/ground impedance as low as possible; full ground/V_{CC} planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

1. Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive ALS, AS, LS, HC, and HCT devices.

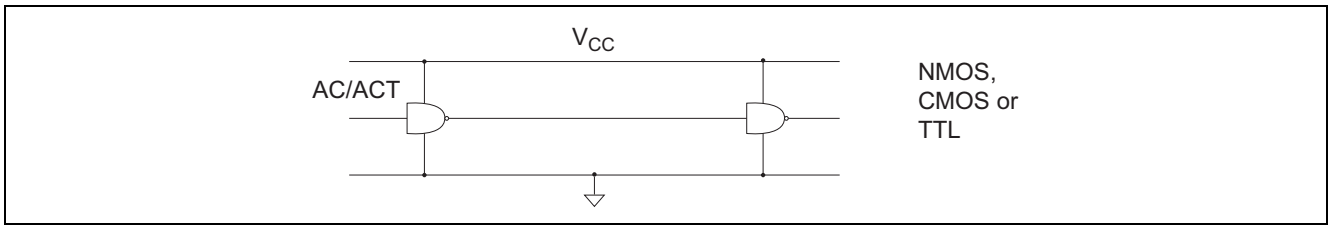


Figure 1 Interfacing FACT to NMOS, CMOS and TTL

FACT devices can be directly driven by both NMOS and CMOS families, as shown in figure 1, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 µA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4 V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be constructed employing a resistor pull-up to V_{CC} of approximately 4.7 kΩ, which is depicted in figure 2. The correct high level is seen by the CMOS device while not loading down the TTL driver.

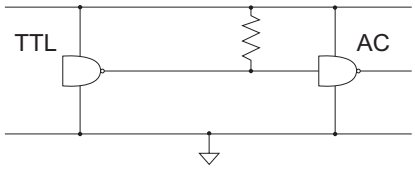


Figure 2 V_{IH} Pull-Up on TTL Outputs

Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Renesas has designed devices which offer thresholds that are TTL-compatible (figure 3). These interfaces tend to be slightly slower than their CMOS-level counter-parts due to an extra buffer stage required for level conversion.

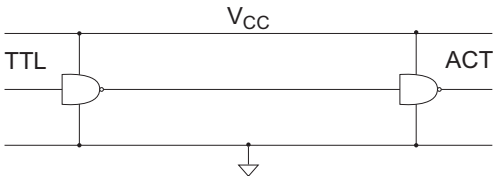


Figure 3 TTL Interfacing to HD74ACT

ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to VCC of approximately 4.7 kΩ). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in figure 4. Figures 5 and 6 show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

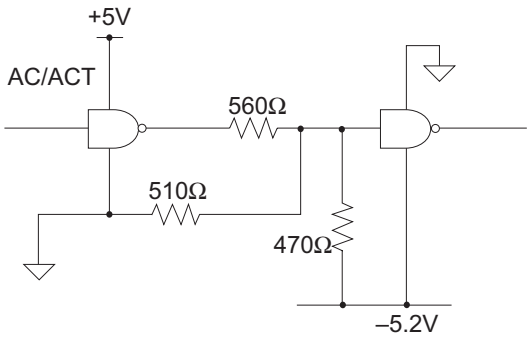


Figure 4 Resistive FACT-to-ECL Translation

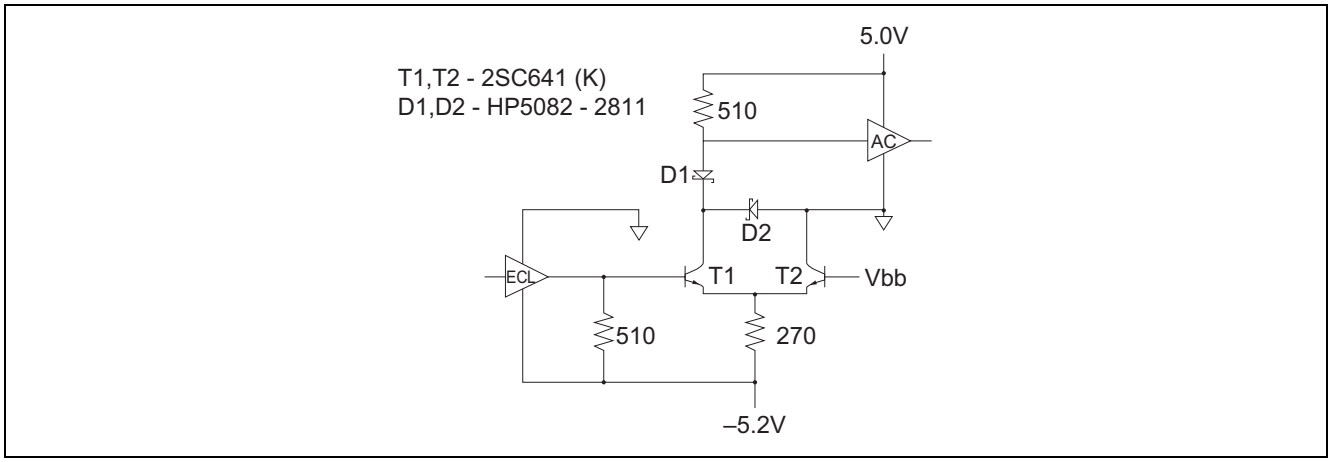


Figure 5 Single-Ended ECL-to-HD74AC Circuit

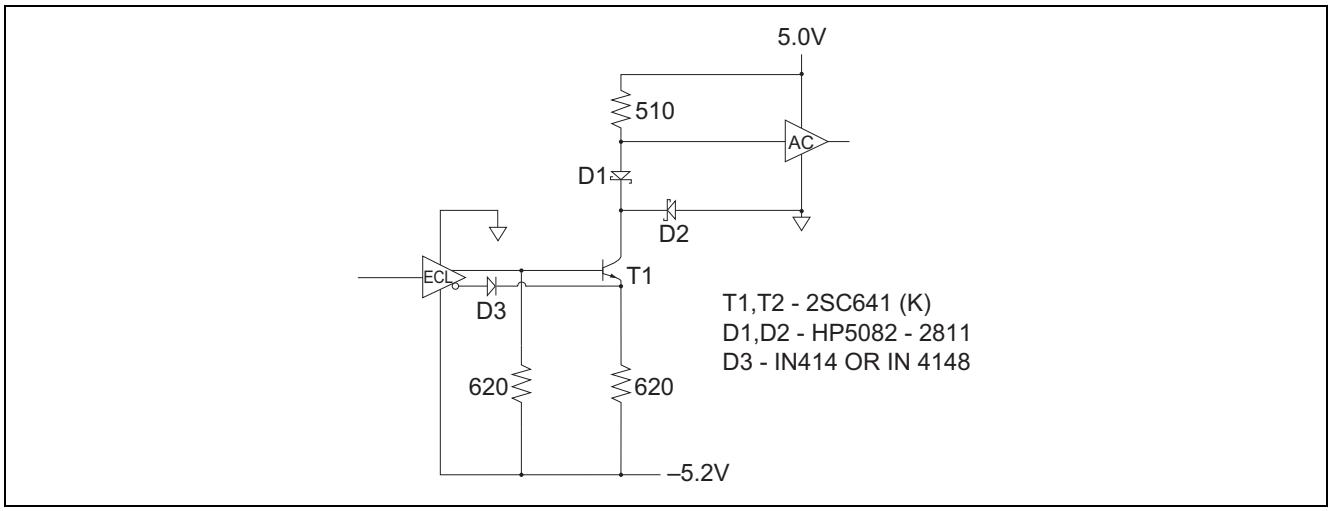


Figure 6 Differential Output ECL-to-HD74AC Circuit

It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

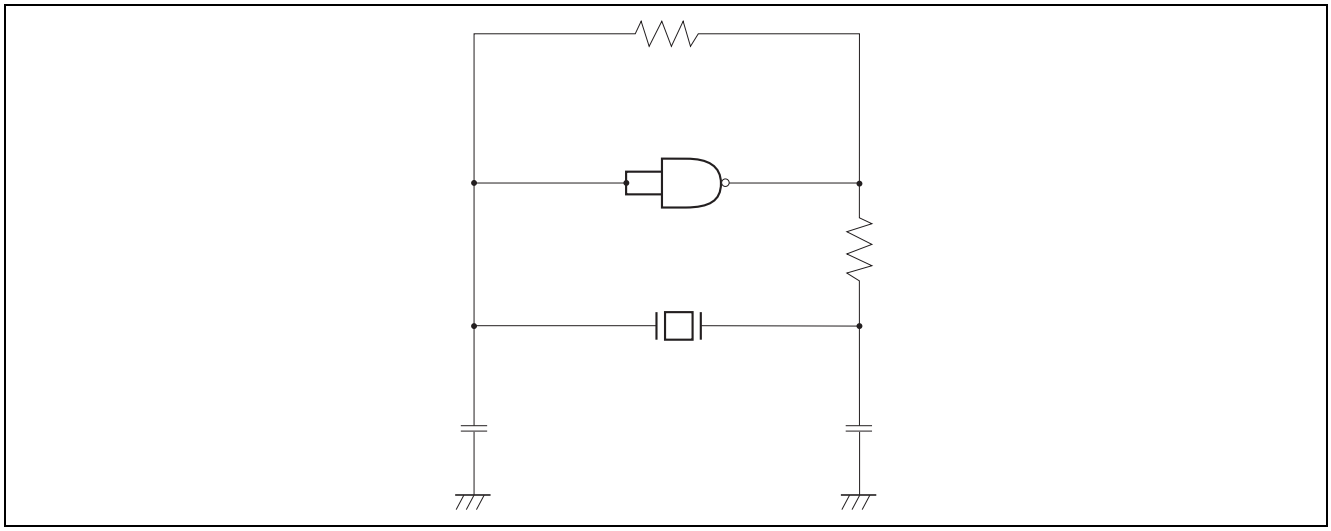


Figure 7 Crystal Oscillator Circuit Implemented with FACT HD74AC00

2. Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Zoe, the effective equivalent impedance of the line, and tpde, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_O and tpd, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Zoe and tpde can be calculated with:

$$Z_{oe} = \frac{Z_O}{\sqrt{1 + C_t / C_1}}$$

$$t_{pde} = t_{pd}\sqrt{1 + C_t / C_1}$$

where C_I = intrinsic line capacitance and Ct = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

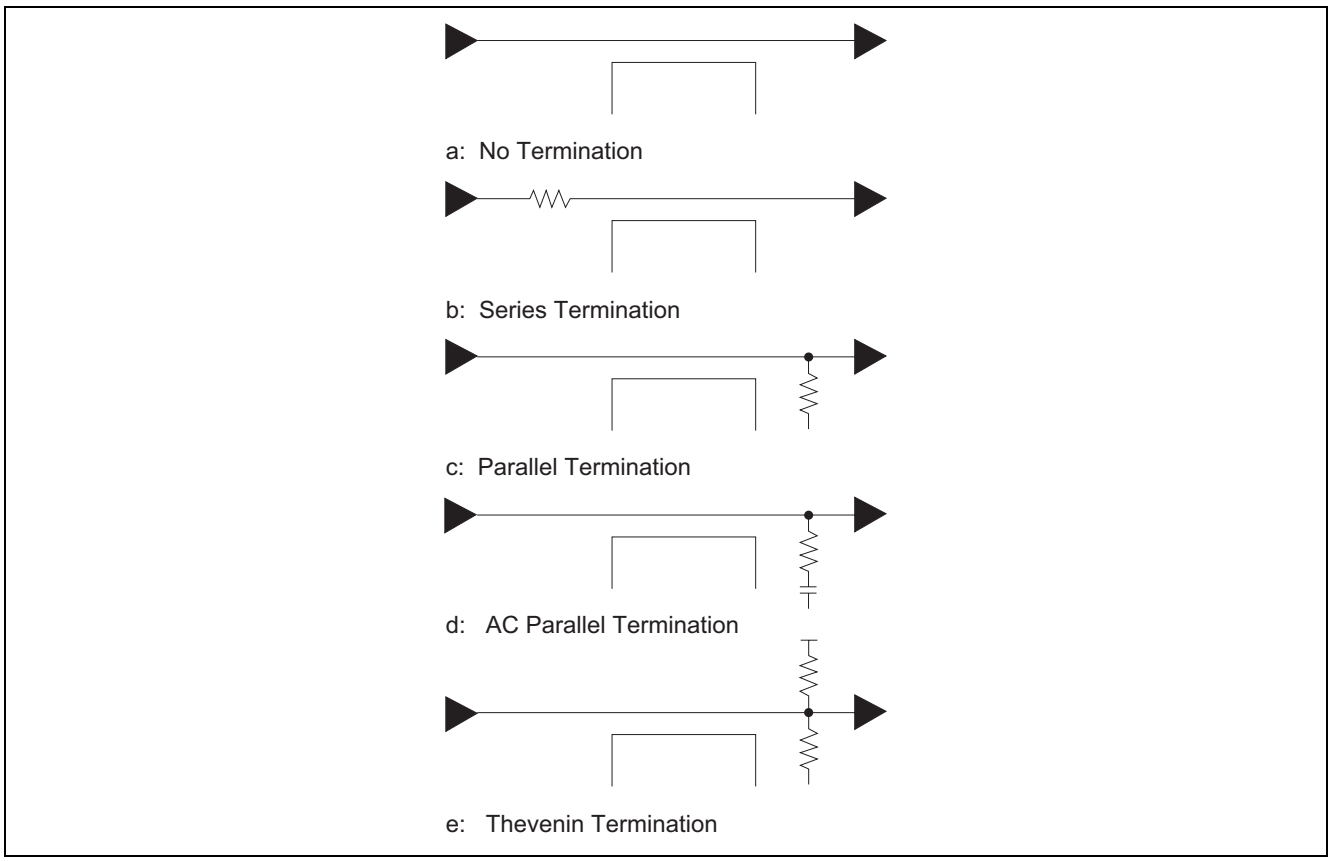


Figure 8 Termination Schemes

There are several termination schemes which may be used (figure 8). Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations cause high DC power consumption.

2.1 Series Terminations

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \bullet Zoe/(Zoe + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

2.2 Parallel Termination

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

2.3 AC Parallel Termination

AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

2.4 Thevenin Termination

Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between VCC or ground, increasing power consumption.

FACT circuits have been designed to drive 50 Ω transmission lines over the full temperature range. This is guaranteed by the FACT family's specified dynamic drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50 Ω transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, VOH and VOL, are specified to be within 0.1 V of the rails, of which the output is sourcing or sinking 50 μA or less. These noise margins are outlined in figure 9.

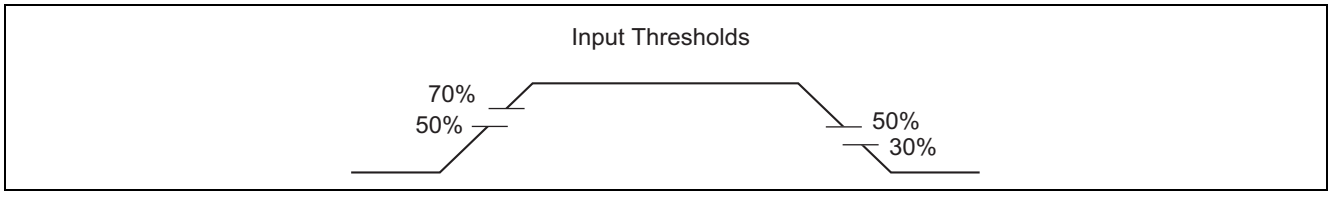


Figure 9 Input Threshold

3. CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 10 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is high. Depending upon the system, this current, IIN, can be quite high, and may not allow the bus voltage to reach a valid high state. One possible solution to eliminate this problem is to place a series resistor in the line.

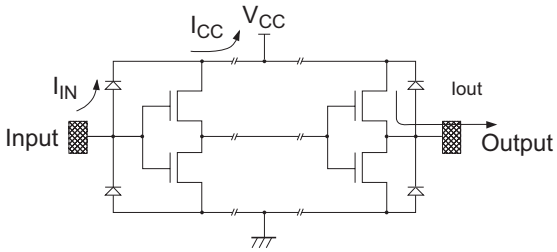


Figure 10 Clamp Diode Operation

4. Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC}. At 5 V V_{CC}, FACT's specified input and output levels give almost 1.5 V of noise margin for both ground and V_{CC}-born noise. With realistic input thresholds closer to 50% of V_{CC}, the actual margins approach 2.5 V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per ship. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

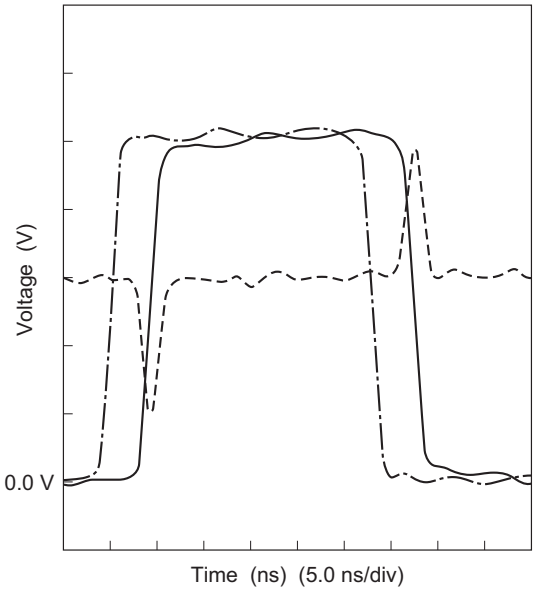
4.1 Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, figure 11, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air (Er = 1.0) and epoxy glass (Er = 4.7). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. this delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, figure 12, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

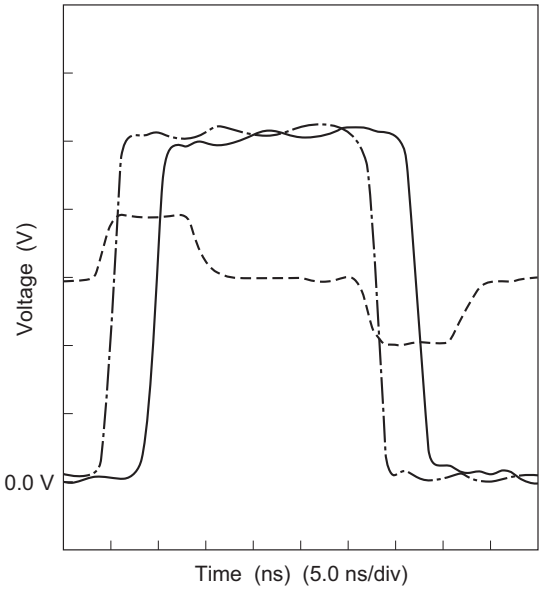
Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in figures 13 and 14, exemplify the outstanding immunity to everyday noise which can effect system reliability.



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 11 Forward Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
Active Driver	1.0 V/Div	50 ns/Div
Forward Crosstalk	0.2 V/Div	5.0 ns/Div
Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 12 Reverse Crosstalk on PCB Traces

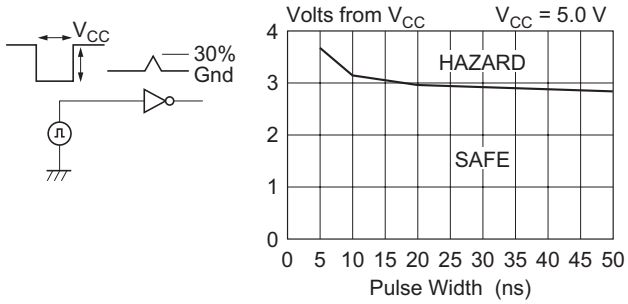


Figure 13 High Noise Margin

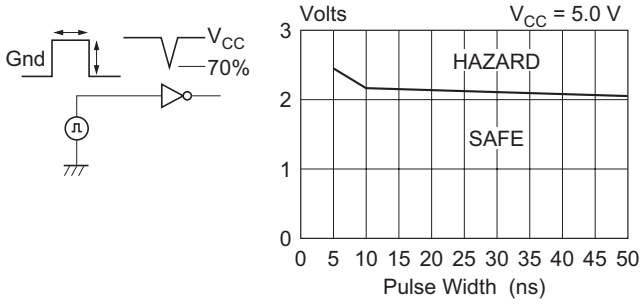


Figure 14 Low Noise Margin

With over 2.0 V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing (figure 15). Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

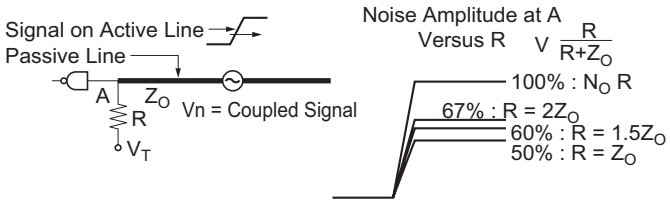


Figure 15 Effects of Termination on Crosstalk

4.2 Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 16 shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

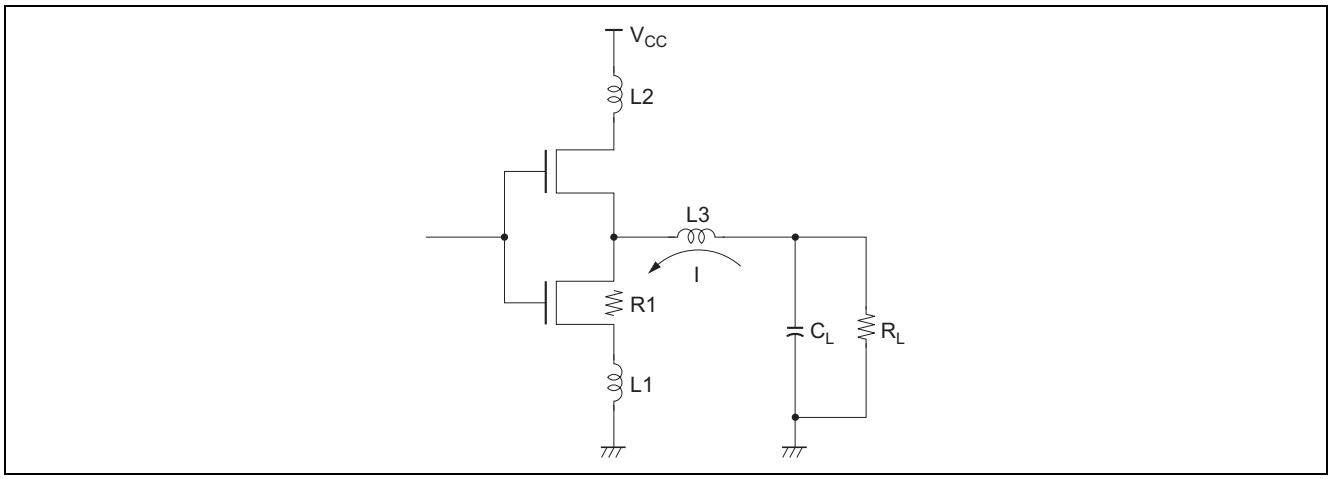
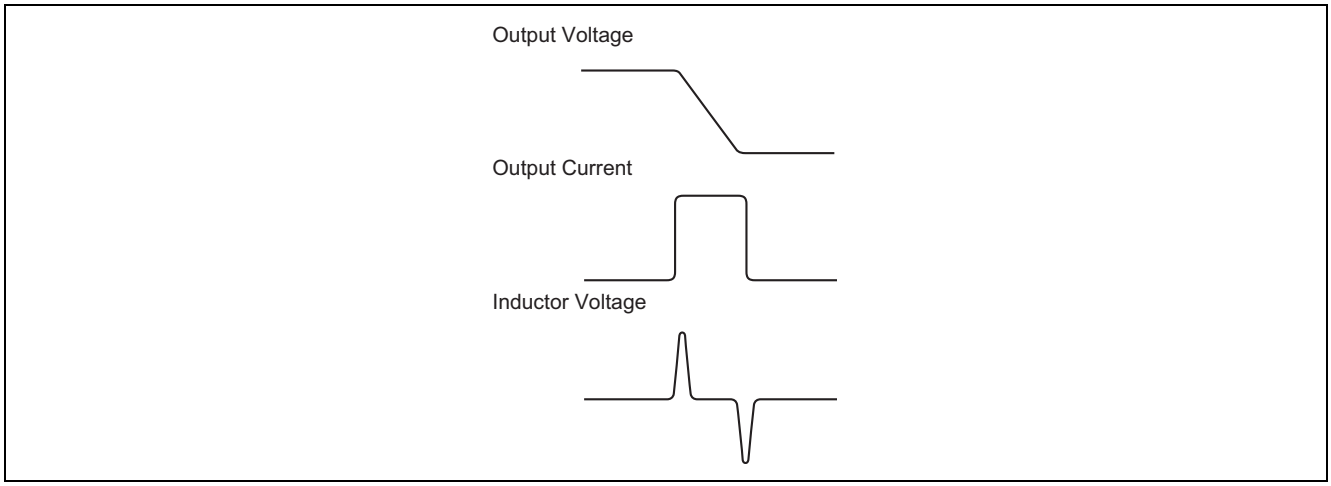


Figure 16 Ground Bounce Output Model



The three waveforms shown in figure 16 depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic high to a logic low. The output slue rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \bullet dv/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$Vgb = -L \bullet (di/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60 to 70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering VCC reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degraduation. FACT devices are characterized not to degrade more than 250 ps per additional output switching
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500 to 1100 mV in actual system applications.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

- First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or
- Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections etc.

5. Design Rules

The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 µF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Avoid sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

5.1 Decoupling Requirements

FACT, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a low to a high value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 17 displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50 and 100 Ω. This impedance appears in series with the load impedance and will cause a droop in the VCC at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used.

This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in figure 18 to calculate the amount of decoupling necessary. This circuit utilizes an HD74AC240 driving a 100 Ω bus from a point somewhere in the middle.

Being in the middle of the bus, the driver will see two 100 Ω loads in parallel, or an effective impedance of 50 Ω. To switch the line from rail to rail, a drive of 78 mA is needed; more than 624 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage with acceptable limits and keep rise and fall times to minimum. The necessary values for decoupling capacitors can be calculated with the formula given in figure 19.

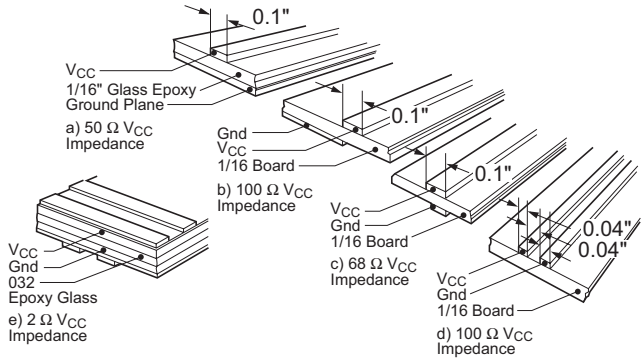


Figure 17 Power Distribution Impedances

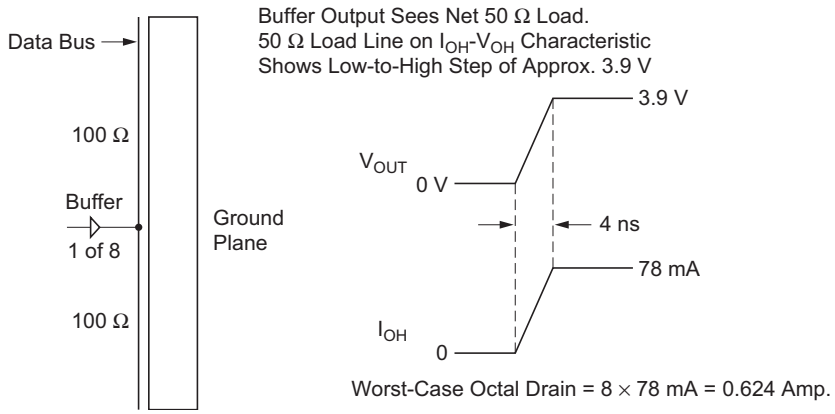
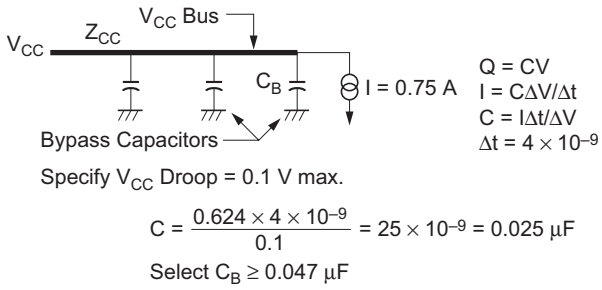


Figure 18 Octal Buffer Driving a 100 W Bus



Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly thoughout the logic. One capacitor per three packages.

Figure 19 Formula for Calculating Decoupling Capacitors

In this example, if the V_{CC} droop is to be kept below 0.1 V and the edge rate equals 4 ns, a 0.025 µF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

5.2 Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

6. TTL-Compatible CMOS Designs Require Delta I_{CC} Consideration

The FACT product line is composed of two types of advanced CMOS circuits: HD74AC and HD74ACT devices. HD74ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this HD74ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated in figure 20.

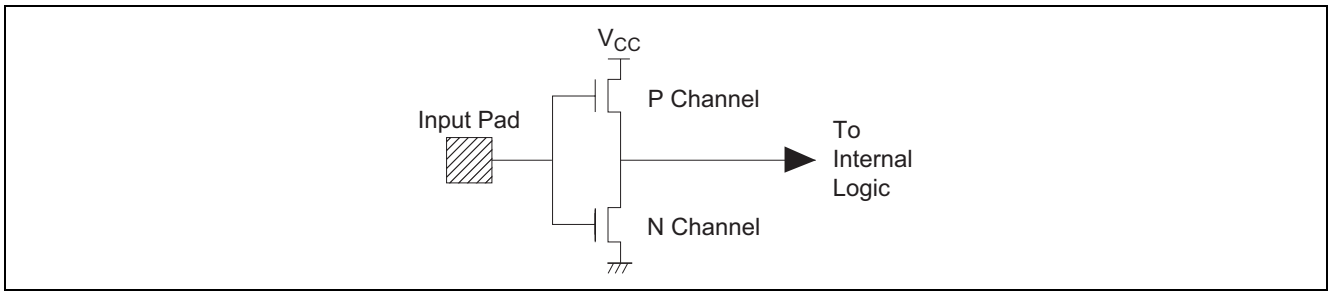


Figure 20 CMOS Input Structure

These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an on transistor is approximately 50 Ω while the resistance of an off transistor is generally greater than 5 MΩ. When the input to this structure is at either ground or V_{CC}, one transistor will be on and one will be off. The total series resistance of this pair will be the combination of the two individual resistances, greater than 5 MΩ. The leakage current will then be less than 1 µA. When the input is between ground and V_{CC}, the resistance of the on transistor will increase while the resistance of the off transistor will decrease. The net resistance will drop due to the much larger value of the off resistance. The total series resistance can be as low as 600 Ω. This reduction in series resistance of the input structure will cause a corresponding increase in I_{CC} as current flows through the input structure. Figure 21 depicts typical I_{CC} variance with input voltage for an HD74ACT device.

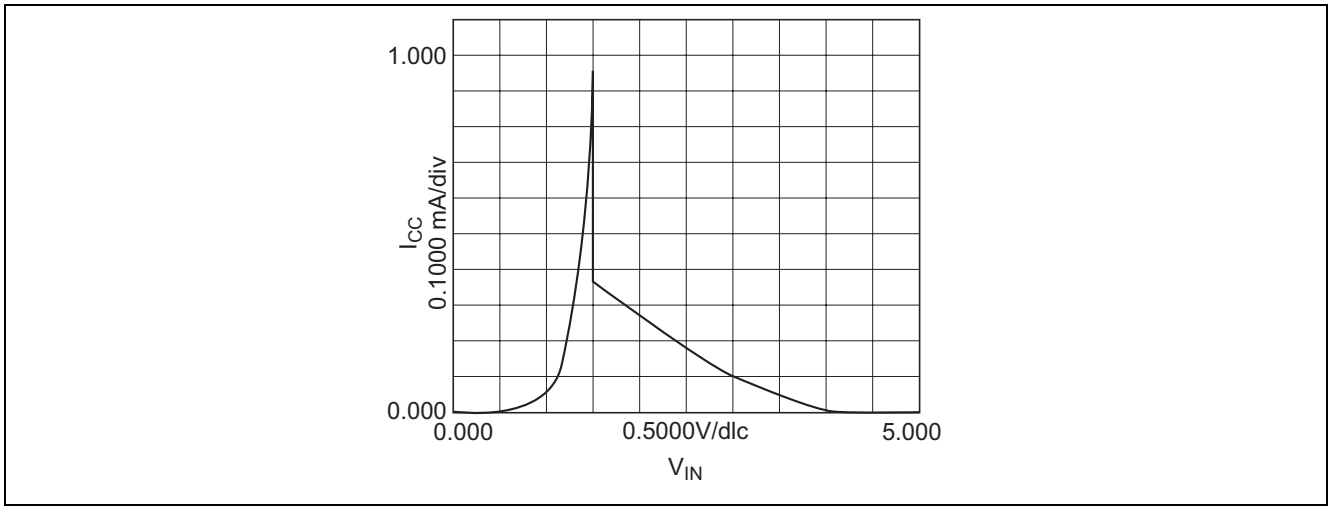


Figure 21 I_{CC} versus Input Voltage for HD74ACT Devices

The Delta I_{CC} specification is the increase in I_{CC}. For each input at V_{CC}-2.1 V, the Delta I_{CC} value should be added to the quiescent supply current to arrive at the circuit's worst-case static I_{CC} value.

Fortunately, there are several factors which tend to reduce the increase in I_{CC} per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. For example, FAST logic outputs can drive HD74ACT-type inputs down to 200 mV and up to 3.5 V. Additionally, the typical I_{CC} increase per input will be less than the specified limit. As shown in the graph above, the I_{CC} increase at V_{CC}-2.1 V is less than 200 µA in the typical system. Experiments have shown that the I_{CC} of an HD74ACT240 series device typically increases only 200 µA when all of the inputs are connected to a FAST device instead of ground or V_{CC}.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta I_{CC} specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

7. Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

Such is the case with parts that have a bidirectional pin, exemplified by the HD74AC245/HD74ACT245 octal transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for ICC and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static I_{CC} specification orders of magnitude less than standard load currents. Most CMOS I_{CC} specifications are usually less than 100 µA. When conducting an I_{CC} test, greater care must be taken so that other currents will not mask the actual I_{CC} so that other currents will not mask the actual I_{CC} of the device. These currents are usually sourced from the inputs and outputs.

Since the static I_{CC} requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an I_{CC} test. Even a standard 500 Ω load resistor will sink 10 mA at 5 V, which is more than twice the I_{CC} level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during I_{CC} tests.

Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, I_{CC} can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly on, and a conduction is created from V_{CC} to ground. This conduction path leads to the increased I_{CC} current seen in the I_{CC} vs. V_{IN} curve (figure 22). When the input is at either rail, the input structure no longer conducts. Most I_{CC} testing is done with all of the inputs tied to either V_{CC} or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual I_{CC} of the device under test which is being measured by the tester.

When testing the I_{CC} of a CMOS HD74AC245/HD74ACT245, problems can arise depending upon how the test is conducted. Note the structure of the HD74AC245/HD74ACT245's I/O pins illustrated figure 23.

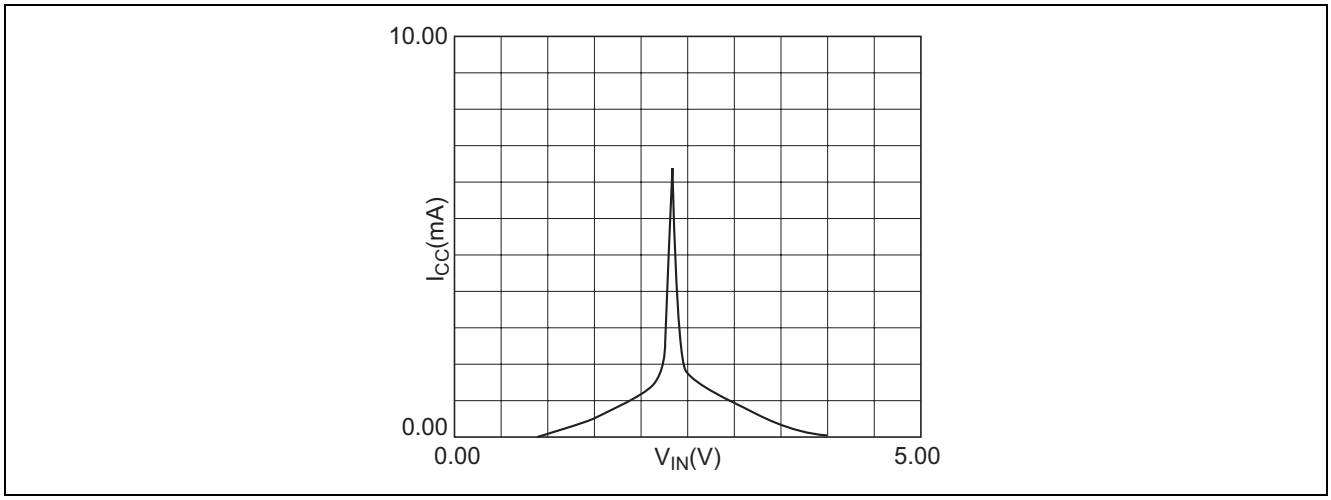


Figure 22 I_{CC} versus IIN

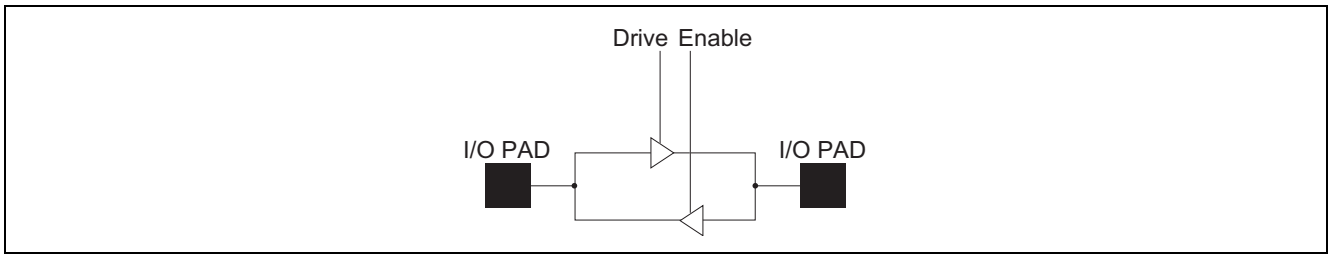


Figure 23 HD74AC245/HD74ACT245 I/O Structure

Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the I_{CC} of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from V_{CC} to ground.

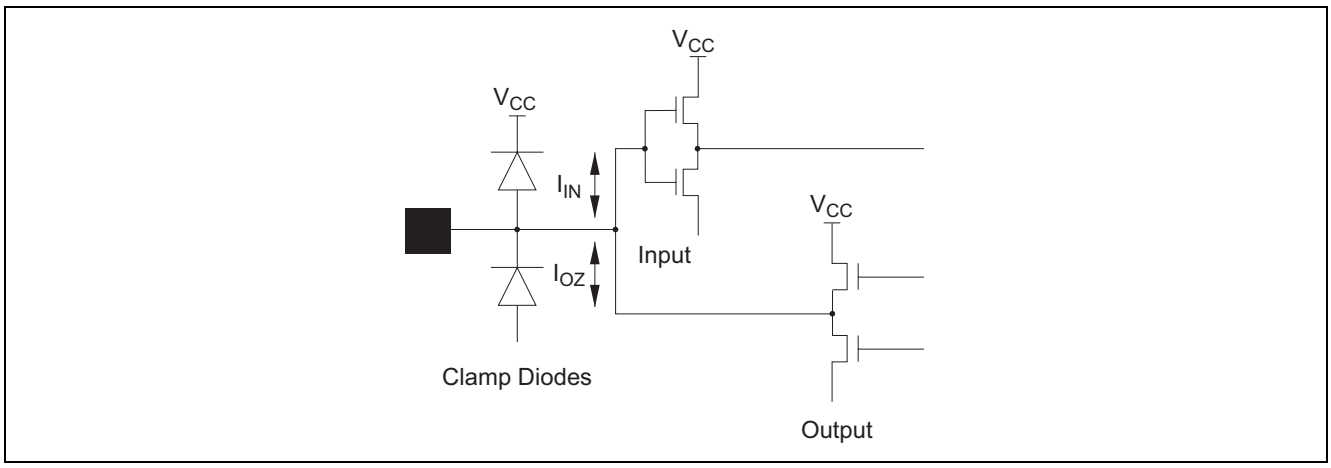


Figure 24 I/O Pin Internal Structure

A simple rule to follow is to treat any output which is disable as an input. This will help insure the integrity of an I_{CC} test.

Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted in figure 24.

The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined I_{IN} specification of the input and the I_{OZ} specification of the output. For FACT devices, I_{IN} is specified at ±1 µA while I_{OZ} is specified at ±5 µA. Combining these gives a limit of ±6 µA for I/O pins. Usually, I/O pins will show leakages that are less than the I_{OZ} specification of the output alone.

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

8. Testing Disable Times of 3-State Outputs in a Transmission Line Environment

Traditionally, the disable time of a 3-state buffer has been measured from the 50% point on the disable input, to the 10% or 90% point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown in figure 25.

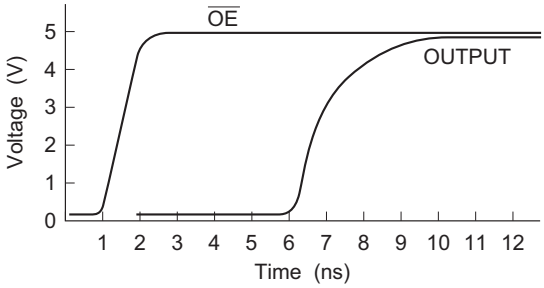


Figure 25 Typical Bench 3-State Waveform

ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. Figure 26 illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

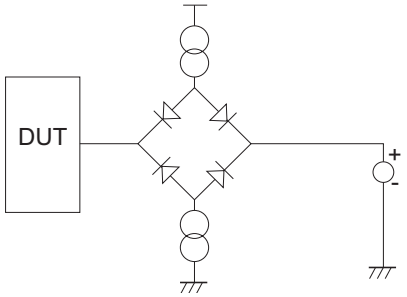


Figure 26 MCT Wheatstone Bridge Test Load

The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the 10% or 90% level. Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in figure 27.

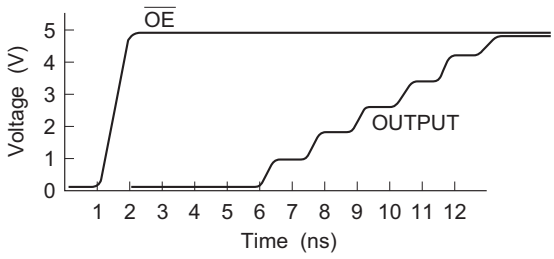


Figure 27 Typical ATE 3-State Waveform

Transmission line theory states that the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50 to 60 Ω, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the 10% point, it would be looking for a step of 550 mV at 5.5 V V_{CC}. Three reflections of the current pulse would be required before the comparator would detect the level. It is

this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customers' incoming tests, even though the device meets specifications. Figure 28 graphically shows this stepout.

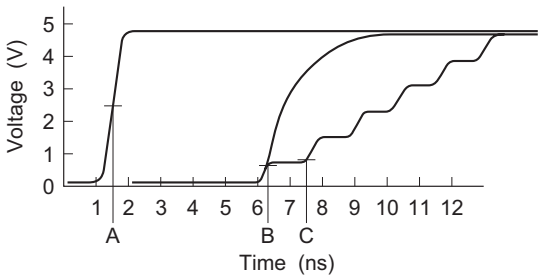


Figure 28 Measurement Stepout

Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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