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CMOS Logic IC HD74AC Series (FACT)

Definition of Specifications

1. Power Dissipation-Test Philosophy

In an erfort to reduce confusion about measuring C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted, which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5.0 V at 25°C, with 3-state outputs both enabled and disabled.

- Gates: Switch one input. Bias the remaining inputs such that the output switches.
- Latches: Switch the Enable and D inputs such that the latch toggles.
- Flip-Flops: Switch the clock pin while changing D (or bias J and K) such that the output (s) change each clock cycle. For parts with a common clock, exercise only one flip - flop.
- Decoders: Switch one address pin which changes two outputs.
- Multiplexers: Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
- Counters: Switch the clock pin with other inputs biased such that the device counts.
- Shift Registers: Switch the clock pin with other inputs biased such that the device counts.
- Transceivers: Switch one data input. For bidirectional devices enable only one direction.
- Parity Generator: Switch one input.
- Priority Encoders: Switch the lowest priority input.
- Load Capacitance: Each output which is switching should be loaded with the standard 50 pF. The equivalent load capacitance, based upon the number of outputs switching and their respective frequency, is then subtracted form the measured gross C_{PD} number to obtain the device's actual C_{PD} value.

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{PD}:

$$C_{PD} = I_{CC} / (V_{CC}) (1 \times 10^6) - \text{Equivalent Load Capacitance}$$

2. Ratings and Specifications

Table 1 Absolute Maximum Ratings[*1]

Parameter	Symbol	Limit	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7.0	V	
DC input Diode current or DC input voltage	I_{IK}	–20	mA	V_I = –0.5
		20	mA	$V_I = V_{CC}$ +0.5
	V_I	–0.5 to V_{CC} +0.5	V	
DC output Diode current or DC output voltage	I_{OK}	–50	mA	V_O = –0.5
		50	mA	$V_O = V_{CC}$ +0.5
	V_O	–0.5 to V_{CC} +0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC} or I_{GND}	±50	mA	
Storage temperature	T_{STG}	–65 to 150	°C	

Note: 1. Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the document specifications should be met, without exception to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Renesas does not recommend operation of FACT circuits outside document specifications.

Table 2 Recommended Operating Conditions

Parameter		Symbol	Limit	Unit	Condition
Supply Voltage (unless otherwise specified)	AC devices	V_{CC}	2.0 to 6.0	V	
	ACT devices		4.5 to 5.5		
Input voltage		V_I	0 to V_{CC}	V	
Output voltage		V_O	0 to V_{CC}	V	
Operating temperature		T_A	–40 to +85	°C	
Input rise and Fall time*1 (typical) (except Schmitt inputs) 'AC devices V_{IN} from 30% to 70% of V_{CC}		tr, tf	150	ns/V	V_{CC} @ 3.0V
			40	ns/V	V_{CC} @ 4.5V
			25	ns/V	V_{CC} @ 5.5V
Input rise and Fall time*1 (typical) (except schmitt inputs) 'ACT devices V_{IN} from 0.8 to 2.0 V, Vmeas from 0.8 to 2.0V		tr, tf	10	ns/V	V_{CC} @ 4.5V
			8	ns/V	V_{CC} @ 5.5V

Note: 1. See individual data sheets for those devices which differ from the typical input rise and fall times noted here.

Table 3 DC Characteristics for HD74AC Family Devices

Parameter	Symbol	V_{CC} (V)	Ta = +25°C	Ta = –40 to +85°C		Unit	Condition
			Typ	Guaranteed Limit			
Minimum High Level Input Voltage	V_{IH}	3.0	1.5	2.1	2.1	V	Vout = 0.1 V or V_{CC} –0.1 V
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
Maximum Low Level Input Voltage	V_{IL}	3.0	1.5	0.9	0.9	V	Vout = 0.1 V or V_{CC} –0.1V
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
Maximum High Level Output Voltage	V_{OH}	3.0	2.99	2.9	2.9	V	I_{OUT} = –50 µA
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.58	2.48	V	V_{IN} = V_{IL} or V_{IH} –12 mA I_{OH} –24 mA*1 –24 mA
		4.5		3.94	3.80		
		5.5		4.94	4.80		
Maximum Low Level Output Voltage	V_{OL}	3.0	0.002	0.1	0.1	V	I_{OUT} = 50 µA
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.32	0.37	V	V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA*1 24 mA
		4.5		0.32	0.37		
		5.5		0.32	0.37		
Maximum Input Leakage Current	I_{IN}	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
Maximum 3-State Current	I_{OZ}	5.5		±0.5	±5.0	µA	$V_{I\ (OE)}$ = V_{IL}, V_{IH} V_I = V_{CC}, V_{GND} V_O = V_{CC}, GND
Minimum Dynamic Output Current *2	I_{OLD}	5.5			86	mA	V_{OLD} = 1.1 V
	I_{OHD}	5.5			–75	mA	V_{OHD} = 3.85 V

Notes: 1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.

Table 4 DC Characteristics for HD74ACT Family Devices

Parameter	Symbol	V_{CC} (V)	Ta = +25°C	Ta = –40 to +85°C		Unit	Condition
			Typ	Guaranteed Limit			
Minimum High Level Input Voltage	V_{IH}	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} –0.1V
		5.5	1.5	2.0	2.0		
Maximum Low Level Input Voltage	V_{IL}	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1 V or V_{CC} –0.1V
		5.5	1.5	0.8	0.8		
Maximum High Level Output Voltage	V_{OH}	4.5	4.49	4.4	4.4	V	I_{OUT} = –50 µA
		5.5	5.49	5.4	5.4		
		4.5		3.94	3.80	V	V_{IN} = V_{IL} or V_{IH} I_{OH} –24 mA[*1], –24 mA
		5.5		4.94	4.80		
Maximum Low Level Output Voltage	V_{OL}	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 µA
		5.5	0.001	0.1	0.1		
		4.5		0.32	0.37	V	V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA[*1], 24 mA
		5.5		0.32	0.37		
Maximum Input Current	I_{IN}	5.5		±0.1	±1.0	µA	V_I = V_{CC}, GND
Maximum 3-State Current	I_{OZ}	5.5		±0.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
Maximum ICC/Input Current	I_{CCT}	5.5	0.6		1.5	mA	V_I = V_{CC} – 2.1V
Minimum Dynamic Output Current [*2]	I_{OLD}	5.5			86	mA	V_{OLD} = 1.1 V
	I_{OHD}	5.5			–75	mA	V_{OHD} = 3.85 V

Notes: 1. All outputs loaded; thresholds on input associated with output under test.
2. Maximum test duration 2.0 ms, one output loaded at a time.

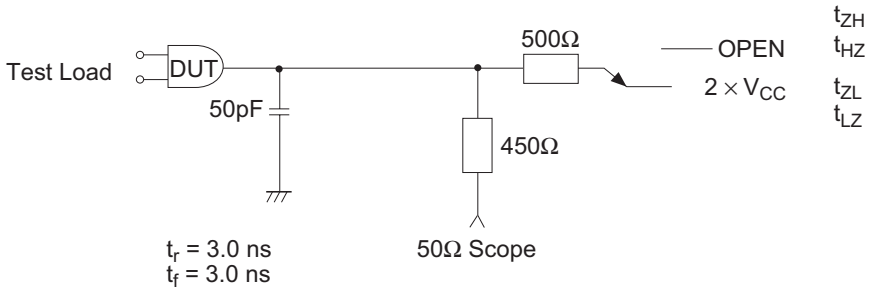


Figure 1 AC Loading Circuit

3. AC Loading and Waveforms

3.1 Loading Circuit

Figure 1 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices (HD74AC and HD74ACT) unless otherwise specified in the data sheet of a specific device.

The use of this load, differs somewhat from previous practice provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high-impedance, high-frequency scope probes. FACT circuits changed to 50 pF of capacitance, allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions.

This more closely resembles the inloading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500 Ω resistor to ground can be a high-frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high-impedance probe. Alternately, the 500 Ω resistor to ground can simply be a 450 Ω resistor feeding into a 50 Ω coaxial cable leading to a sampling scope input connector, with the internal 50 W termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See figure 1.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 Ω termination for the pulse generator that supplies the input signal.

Shown in figure 1 is a second 500 Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (low-to-off and off-to-low) of a 3-state output. With the switch closed, the pair of 500 Ω resistors and the $2 \times V_{CC}$ supply voltage establish a quiescent high level.

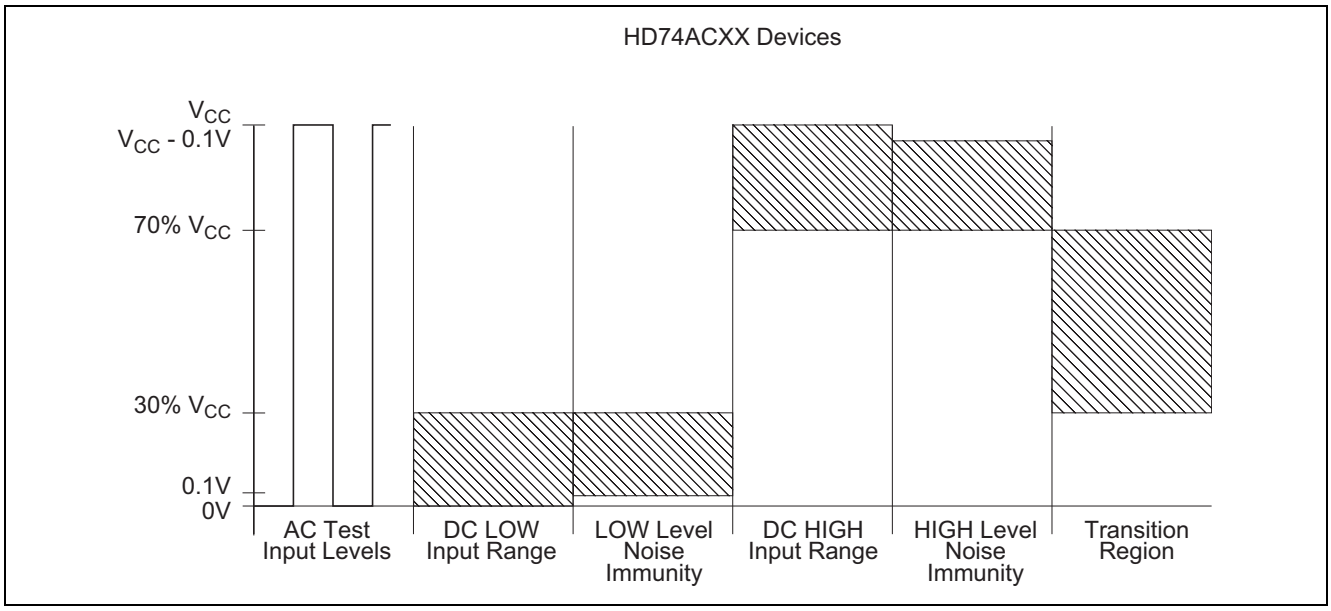


Figure 2a Test Input Signal Levels

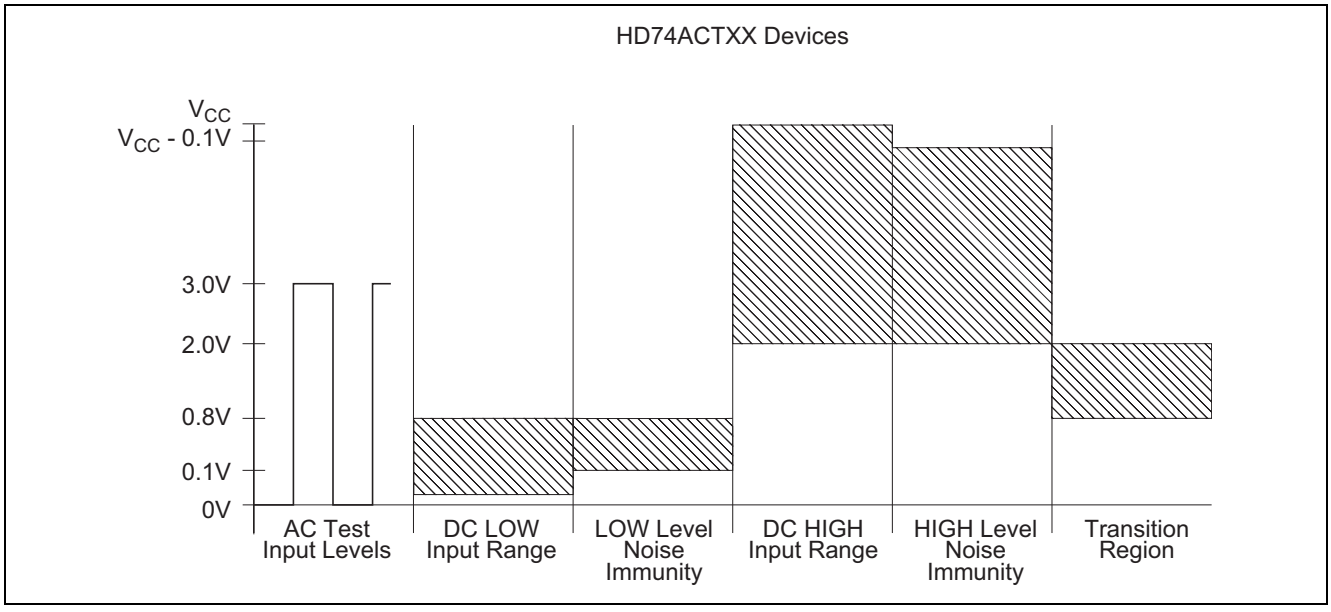


Figure 2b Test Input Signal Levels (cont)

3.2 Test Conditions

Figure 2 describes the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic low to 3.0 V for a logic high for HD74ACT devices and 0 V to V_{CC} for HD74AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is

V_{IH} to V_{IL} (see tables 3 and 4 for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handlder not specifically designed for high-speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be see in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0 V then dropping it to a level corresponding to V_{IH}, and then raising it again to the 5.0 V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning it to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high-frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

3.3 Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0 V to 3.0 V for HD74ACT devices or 0 V to V_{CC} for HD74ACT devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including, 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

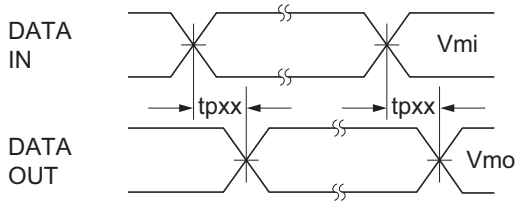
It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a high level to a low level, or from a low level to a high level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2-3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the VCC or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world become of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have V_{CC} and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5 V swing on the output.

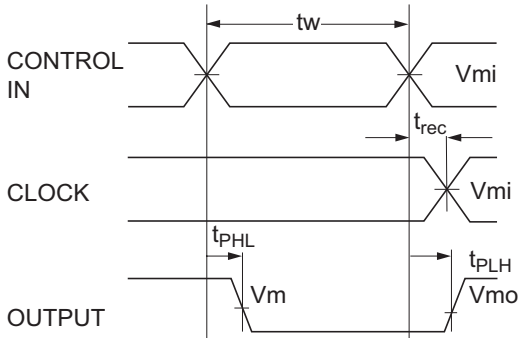
3.4 Propagation Delays, f_{max}, Set and Hold Times

A 1.0 MHz square wave is recommended for most propagation delay tests (figures 3 and 4) The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time etc.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 3 Waveform for Inverting and Non-Inverting Functions

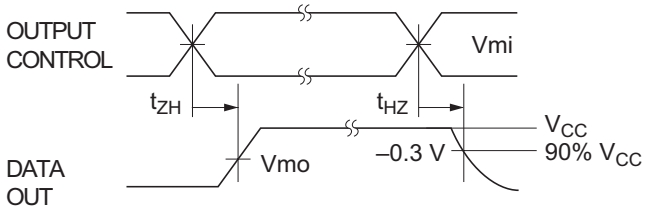


Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 4 Propagation Delay, Pulse Width, and t_{rec} Waveforms

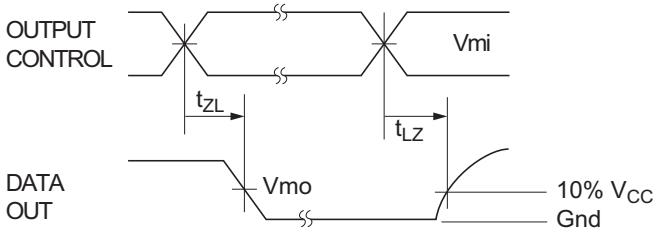
3.5 Enable and Disable Times

Figures 5 and 6 show that the disable times are measured at the point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for t_{LZ} or V_{CC} for t_{HZ}) . This change enhances the repeatability of measurements, reduces test time, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high-impedance state rising or falling waveform is RC-controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned off. Measuring to a larger change in voltage merely exaggerates the apparent Disable time and thus penalizes system performance since the designer must use the Enable and Disable times to device worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 5 3-State Output High Enable and Disable Times

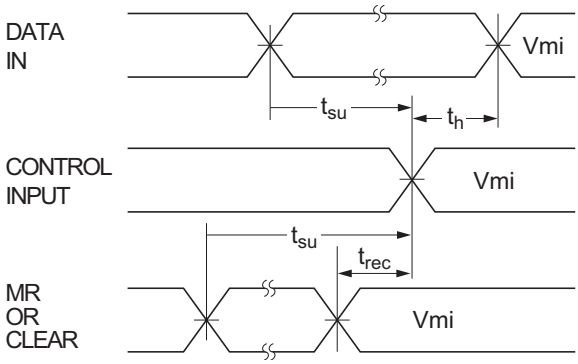


Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 6 3-State Output Low Enable and Disable Times

3.6 Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. More often, handling equipment that is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, that are near the device, are conductive and connected to ground.



Vmi = 50% V_{CC} for HD74AC devices; 1.5 V for HD74ACT devices
Vmo = 50% V_{CC} for HD74AC/HD74ACT devices

Figure 7 Setup Time, Hold Time and Recovery Time

4. Symbols and Terms Defined for HD74AC Series

Explanation of Symbols Used in Electrical Characteristics and Recommended Operating Conditions

Table 5 DC Characteristics

Symbol	Term	Description
V_{IH}	High level input voltage	High level input voltage to ensure that a logic element operates under some constraint
V_{IL}	Low level input voltage	Low level input voltage to ensure that a logic element operates under some constraint
V_{OL}	Low level output voltage	Output voltage in effect when, under the input condition for bringing the output low, the rated output current is allowed to flow to the output terminal
V_{OH}	High level output voltage	Output voltage in effect when, under the input condition for bringing the output high, the rated output current is allowed to flow to the output terminal
V_t^+	Forward input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up form a voltage level lower than the reverse input threshold voltage V_t^-
V_t^-	Reverse input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to drop up form a voltage level higher than the forward input threshold voltage V_t^+
V_h	Hysteresis voltage	Difference between forward input threshold voltage V_t^+ and reverse threshold voltage V_t^-
I_{IN}	Input leakage current	Input current that flows in when the rated maximum input voltage is applied to the input terminal
I_{OZ}	Off-state output current (high-impedance)	Current that flows to the 3-state output of an element under the input condition for bringing the output to high-impedance state
I_{CC}	Quiescent Supply current	Current that flows to the supply terminal (V_{CC}) under the rated input condition
I_{OLD}	Minimum Dynamic Output Current	Output current that flows in when, under the condition for bringing the output low, the output terminal is tied to the rated out voltage V_{OLD}.
I_{OHD}		Output current that flows out when, under the condition for bringing the output high, the output terminal is tied to the rated out voltage V_{OHD}.
I_{CCT}	Maximum I_{CC} /Input	Current that flows to the supply terminal (V_{CC}) under the rated input condition

Table 6 AC Characteristics

Symbol	Term	Description
f_{max}	Maximum clock frequency	Maximum clock frequency that maintains the stable changes in output logic level in the rated sequence under the I/O condition allowing clock pulses to change the output state
t_{TLH}	Rise (transient) time	Rated time from low level to high level of a waveform during the defined transient period changing from low level to high level
t_{THL}	Fall (transient) time	Rated time from high level to low level of a waveform during the defined transient period changing from high level to low level
t_{PLH}	Output rise propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from low level to high level
t_{PHL}	Output fall propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from high level to low level
t_{HZ}	3-state output disable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from high level to the high-impedance state
t_{LZ}	3-state output disable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from low level to the high-impedance state
t_{ZH}	3-state output enable time (high level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impedance state to high level
t_{ZL}	3-state output enable time (low level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high-impedance state to low level
t_w	Pulse width	Duration of time between the rated levels from a leading edge to a trailing edge of a pulse waveform
t_h	Hold time	Time in which to hold data at the specified input terminal after a change at another related input terminal (e.g., clock input)
t_{SU}	Setup time	Time in which to set up and keep data at the specified input terminal before a change at another related input terminal (e.g., clock input)
t_{rec}	Recovery time	Time period between the time when data at the specified input terminal is released and the time when another related input terminal (e.g., clock input) can be changed
C_{IN}	Input capacitance	Capacitance between GND terminal and an input terminal to which 0 V is applied
C_{PD}	Power Dissipation Capacitance	Equivalent device power capacitance in dynamic state

Table 7 Explanation of Symbols Used in Function Tables

Symbol	Description
H	High level (in steady state; written H or "H" level in sentences)
L	Low level (in steady state; written L or "L" level in sentences)
↑	Transition from L level to H level
↓	Transition from H level to L level
X	Either H or L
Z	3-state output off (high impedance)
a·····h	Input level of steady state for each of inputs A-H
Q0	Q level immediately before the indicated input condition is established
$\overline{Q0}$	Complement of Q_0
Qn	Q level immediately before the latest active change (↑ or ↓) occurs
⊓	Single H level pulse
⊔	Single L level pulse
TOGGLE	Each output is changed to the complement of the preceding state by an active input change (↑ or ↓)

Revision Record

Rev.	Date	Description	
		Page	Summary
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