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2010年4月1日  
瑞萨电子公司

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# 低电压 CMOS 逻辑 IC HD74LV\_A/LVC 系列

## 规格的定义

### 1. 负载电路

用于规定 HD74LV/LVC 系列的开关时间的 AC 负载电路，请参照各产品数据表。HD74LV/LVC 系列的负载电路为  $C_L=50\text{pF}$ ，在增加寄生电容的容限的同时，起输出信号上升或者下降时的负载作用。此负载电路能为系统设计提供接近于一般应用系统假设的负载并且便于使用的开关时间的数值。

连接到 HD74LVC 系列 GND 的  $500\Omega$  电阻能被视为示波器的无源探针。换言之，连接 GND 的  $500\Omega$  电阻能被视为通过  $450\Omega$  的电阻和  $50\Omega$  的同轴电缆，串联到内部连接了  $50\Omega$  终端电阻的采样示波器。器件的输入引脚通过相同阻抗的电缆连接到采样示波器的另一个输入端。相当于脉冲发生器的信号输出端连接了一个  $50\Omega$  的终端电阻。

在 HD74LV 系列的情况下，在输出 -GND 之间连接  $1\text{k}\Omega$  的电阻，并通过  $1\text{M}\Omega$  以上的阻抗探针连接到示波器。

在 HD74LV/LVC 系列的 AC 负载电路中，在测量器件的输出引脚和开关之间连接了另一个电阻（ $1\text{k}\Omega$ ：HD74LV 系列； $500\Omega$ ：HD74LVC 系列）。在测量传播延迟时间时，此开关为断开状态；在测量三态输出的允许时间和禁止时间（High→OFF、OFF→High）时，此开关连接 GND；在（Low→OFF、OFF→Low）时，此开关连接 6V 电源。

如果此开关连接 GND，输出引脚的电压就变为静态 Low 电平；如果连接 6V 电源，6V 电压就被 2 个电阻（ $1\text{k}\Omega$ ：HD74LV 系列； $500\Omega$ ：HD74LVC 系列）分压，输出引脚的电压变为静态 High 电平。

有关测量波形的定义请参照图 1～图 6。

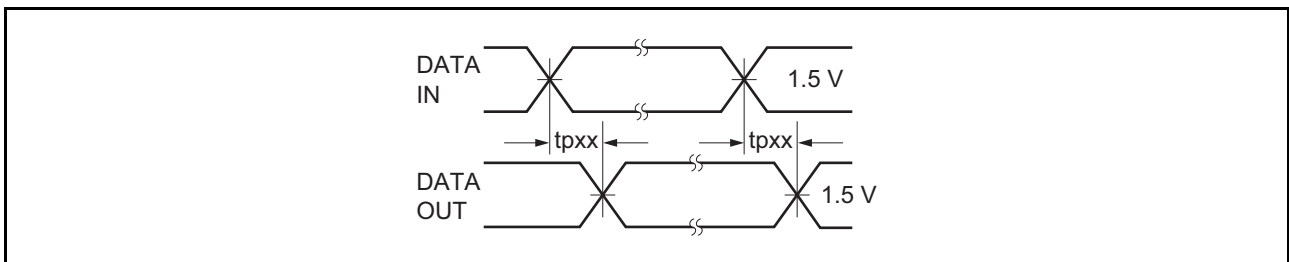


图 1 传播延迟时间

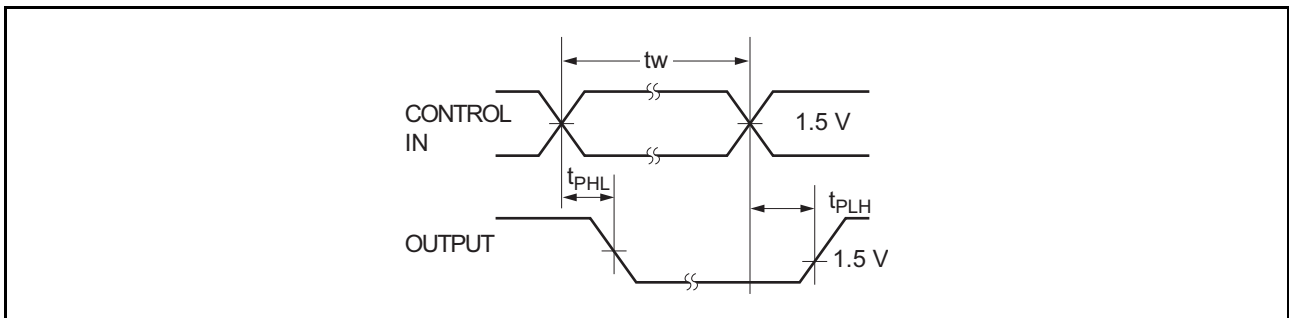


图 2 传播延迟时间和脉宽

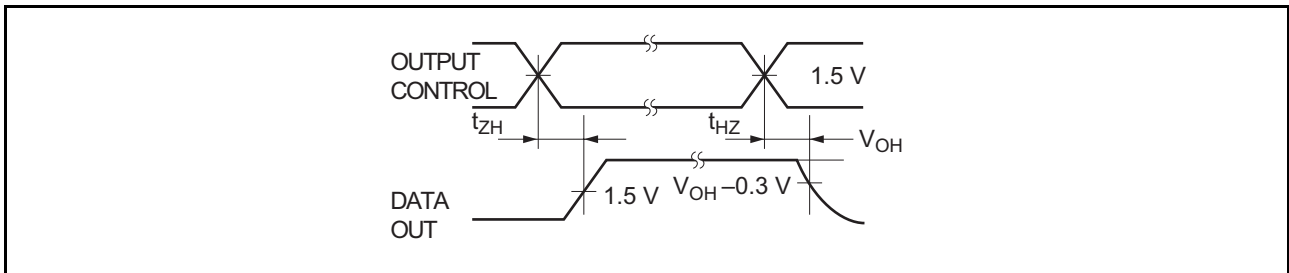


图3 三态输出  $t_{ZH}$  和  $t_{HZ}$

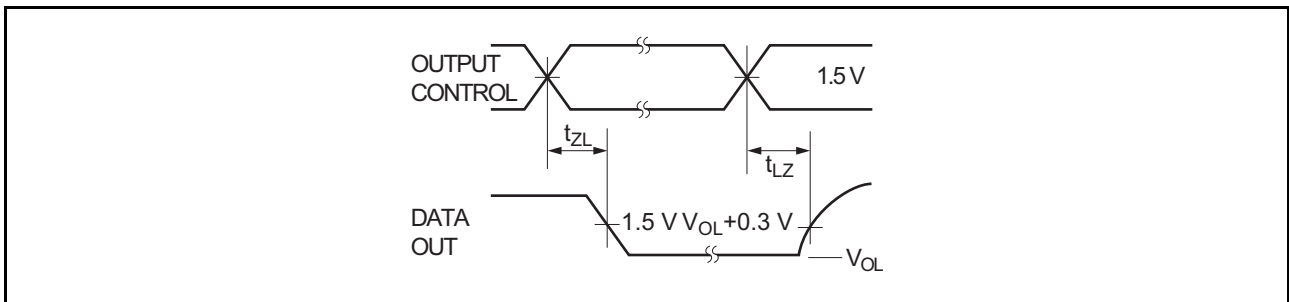


图4 三态输出  $t_{ZL}$  和  $t_{LZ}$

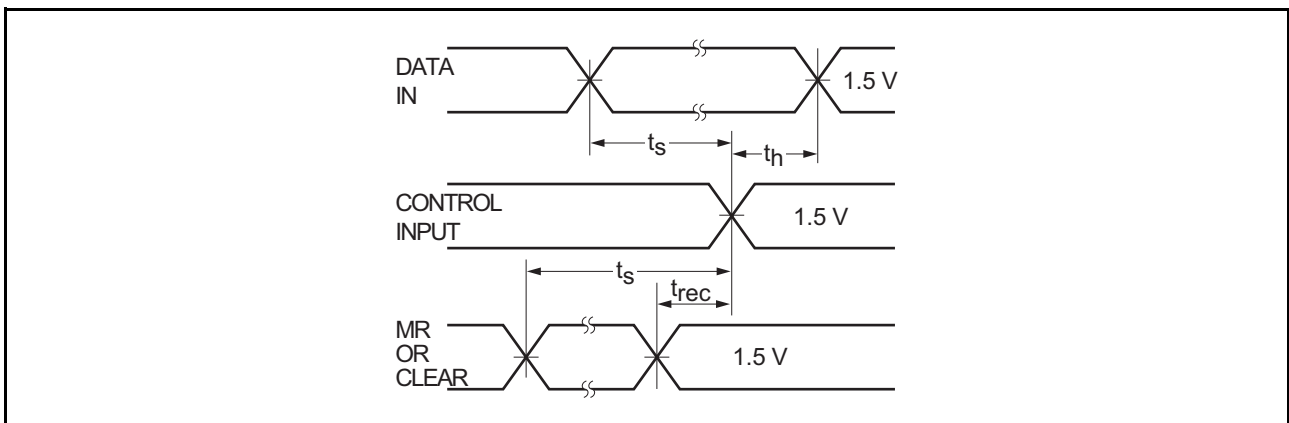


图5 准备时间和保持时间

## 2. 试验条件

有关开关特性项目的试验条件，Low 电平为  $0\text{V}$ ，High 电平为  $2.7\text{V}$ 。输入信号的上升时间和下降时间为  $2.5\text{ns}$ ，但是在测量最大时钟频率和脉宽时不超过  $1\text{ns}$ 。DC 特性项目的输入电压通常为规格中的  $V_{IH}$  和  $V_{IL}$  的值。在试验时，尤其在使用 IC 测试设备和处理设备时，必须注意：需要适当地对电源实施去耦，试验信号不能受噪声的影响。为了提高对测试设备固有噪声（在实际系统中不会发生）的噪声容限，有时需要调整输入电压电平。在试验噪声容限时，必须将输入电压先升高到和电源电压  $V_{CC}$  相同的值，然后降低到相当于  $V_{IH}$  的电平，并且再升高到  $V_{CC}$  电平。对于  $V_{IL}$ ，也需要将输入电压从  $0\text{V}$  升高到  $V_{IL}$  电平，再返回到  $0\text{V}$ 。必须确认在输入电压为  $V_{IH}$  或者  $V_{IL}$  时输出不发生变化。在制作试验夹具时，必须充分考虑高频特性的布线。为了正确地评价输出波形的波纹和负尖峰，必须尽量缩短负载电容的连线并且加宽 GND 布线（最好是地线面），还必须尽量缩短  $V_{CC}$  的旁路电容器连接到试验插座的连线。

### 3. 多个输出的同时开关

开关时间受同时变化的输出引脚数的影响。对于输出引脚数为2个以上（含2个）的器件，同时变化的输出引脚数每增加1个，开关时间就比数据手册的值慢大约200ps（HD74LV系列）或者400S（HD74LVC系列）。对于Octal系列的器件，如果同时变化的输出引脚数不超过4个，实际上此延迟值几乎可以忽略。此值适用于  $T_a = -40 \sim +85^\circ\text{C}$  和  $V_{CC} = 2.7\text{V}$ 、 $3.3 \pm 0.3\text{V}$  的全部范围。

### 4. $\Delta I_{CC}$ 特性

$\Delta I_{CC}$  的规格表示通常的  $I_{CC}$  增量。对于每个外加  $V_{CC}-0.6\text{V}$  的输入引脚，应该将  $I_{CCT}$  的值加到静态消耗电流，这样就能求出电路最坏情况下的静态消耗电流。实际上，在低电压 CMOS 逻辑的情况下，HD74LV/LVC 系列的输入在 Low 电平时能被驱动到 0V 左右，在 High 电平时能被驱动到  $V_{CC}$  左右。因此，实际上输入引脚的外加电压条件比  $\Delta I_{CC}$  的测量条件更宽，并且各输入引脚的  $I_{CC}$  增量的典型值和规格值相比是一个非常小的值。与输入电压相应的  $\Delta I_{CC}$  的变动如图6和图7所示。

因此，当使用 HD74LV/LVC 系列进行设计时，在理解  $\Delta I_{CC}$  的规格含义的同时，应该考虑到：在大部分系统中，实际值和数据手册的规格值相比是一个非常小的值。

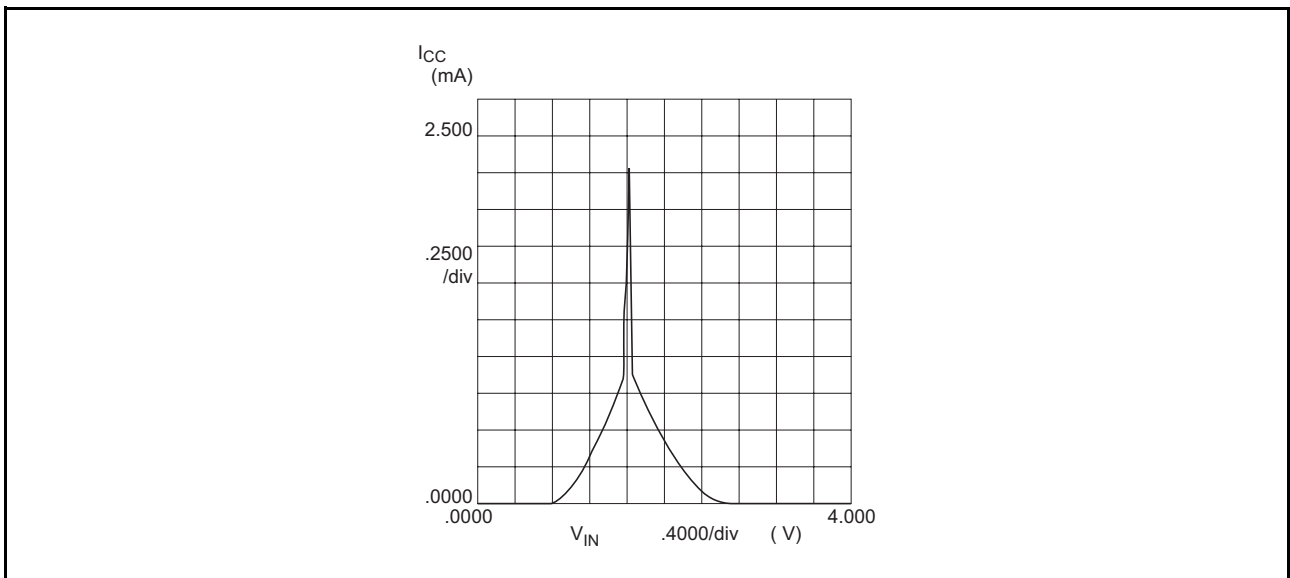


图6 HD74LVC系列的输入电压- $I_{CC}$ 特性

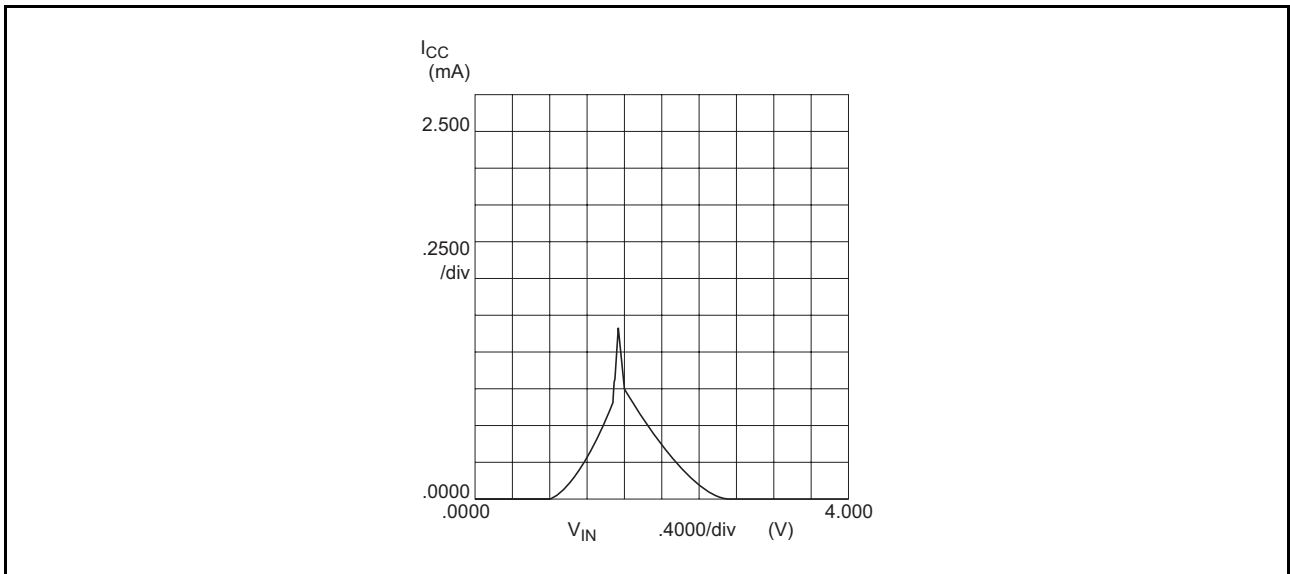


图7 HD74LV系列的输入电压-\$I\_{CC}\$特性

### 5. 功耗的计算方法

通过式(1)求出低电压CMOS标准逻辑的功耗 $P_T$ 。即，功耗取决于负载电容、内部等效电容、工作频率和电源电压。

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 \quad (1)$$

在此，

$C_L$ : 负载电容、 $C_{pd}$ : 内部等效电容

$f$ : 工作频率、 $V_{CC}$ : 电源电压

### 6. 内部等效电容

能通过下式计算内部等效电容 $C_{pd}$ :

$$P_T = (C_{pd} + C_L) \times f \times V_{CC}^2 = I_{CC} \times V_{CC} \quad (2)$$

从式(2)中得到

$$C_{pd} = \frac{I_{CC}}{f \times V_{CC}} - C_L \quad (3)$$

在此，

$I_{CC}$ : 电源电流

(测量条件)

$T_a = 25^\circ\text{C}$ 、 $V_{CC} = 3.3\text{V}$ 、 $f = 10\text{MHz}$

duty = 50%、 $t_r = t_f = 2.5\text{ns}$ 、 $C_L = 50\text{pF}$

(1) HD74LVC系列的等效内部电容Cpd

$V_{CC} = 3.3V$ 、 $T_a = 25^{\circ}C$ 、 $C_L = 50pF$ 、其他输入 =  $V_{CC}$  or GND

P1:  $f = 10MHz$ 、 $duty = 50\%$ 、P2:  $f = 5MHz$ 、 $duty = 50\%$

产品型号	测量条件		enable	disable	单位
	输入	输出	typ.	typ.	
HD74LVC00	1A: P1	1Y	17	—	pF
HD74LVC02	1A: P1	1Y	17	—	
HD74LVC04	1A: P1	1Y	13	—	
HD74LVC08	1A: P1	1Y	16	—	
HD74LVC14	1A: P1	1Y	14	—	
HD74LVC32	1A: P1	1Y	17	—	
HD74LVC74	1CK: P1、1D: P2	1Q	16	—	
HD74LVC125A	1A: P1	1Y	16	2.0	
HD74LVC138	A: P1	Y0	38	—	
HD74LVC139	1A: P1	$\overline{1Y0}$	32	—	
HD74LVC240A	1A1: P1	$\overline{1Y1}$	15	1.0	
HD74LVC244A	1A1: P1	1Y1	14	2.0	
HD74LVC245A	A0: P1	B0	17	2.0	
HD74LVC373A	1D: P1	1Q	18	3.0	
HD74LVC374A	CK: P1、1D: P2	1Q	17	9.5	
HD74LVC534	CK: P1、1D: P2	$\overline{1Q}$	16	9.5	
HD74LVC540A	A1: P1	$\overline{Y1}$	14	1.0	
HD74LVC541A	A1: P1	Y1	15	2.0	
HD74LVC573A	1D: P1	1Q	17	3.0	
HD74LVC574A	CK: P1、1D: P2	1Q	17	10.0	
HD74LVC16240A	1A1: P1	1Y1	15	1.0	
HD74LVC16244A	1A1: P1	1Y1	16	2.0	
HD74LVC16245A	1A1: P1	1B1	18	2.0	
HD74LVC16373A	1D1: P1	1Q1	16	3.0	
HD74LVC16374A	1CK: P1、1D1: P2	1Q1	17	10.0	
HD74LVC2244A	1A1: P1	1Y1	26.0	3.5	
HD74LVCR2245A	A0: P1	B0	31.0	3.5	

(2) HD74LVCZ系列的等效内部电容 Cpd

$V_{CC} = 3.3V$ 、 $T_a = 25^{\circ}C$ 、 $C_L = 50pF$ 、其他输入 =  $V_{CC}$  or GND

P1:  $f = 10MHz$ 、 $duty = 50\%$ 、P2:  $f = 5MHz$ 、 $duty = 50\%$

产品型号	测量条件		enable	disable	单位
	输入	输出	typ.	typ.	
HD74LVCZ240A	1A1: P1	1Y1	27.0	5.5	pF
HD74LVCZ244A	1A1: P1	1Y1	26.0	5.0	
HD74LVCZ245A	A0: P1	B0	31.0	5.0	
HD74LVCZ16240A	1A1: P1	1Y1	30.0	7.0	
HD74LVCZ16244A	1A1: P1	1Y1	30.0	5.0	
HD74LVCZ16245A	1A1: P1	1B1	34.0	5.5	

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8. 除上述第7项内容外,不能将本资料中记载的产品用于以下用途。如果用于以下用途而造成的损失,本公司概不负责。
  - 1) 生命维持装置。
  - 2) 植埋于人体使用的装置。
  - 3) 用于治疗(切除患处、给药等)的装置。
  - 4) 其他直接影响到人的生命的装置。
9. 在使用本资料所记载的产品时,对于最大额定值、工作电源电压的范围、放热特性、安装条件及其他条件请在本公司规定的保证范围内使用。如果超出了本公司规定的保证范围使用时,对于由此而造成的故障和出现的事故,本公司将不承担任何责任。
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11. 如果把本资料所记载的产品从其载体设备上卸下,有可能造成婴儿误吞的危险。顾客在将本公司产品安装到顾客的设备上时,请顾客自行负责将本公司产品设置为不容易剥落的安全设计。如果从顾客的设备上剥落而造成事故时,本公司将不承担任何责任。
12. 在未得到本公司的事先书面认可时,不可将本资料的一部分或者全部转载或者复制。
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