NEC

User's Manual

CMOS-8L Family

CMOS Gate Array

Block Library Ver.5.0

Document No. A12213XJ5V1UM00 (5th edition)
Date Published August 1998 NS CP(K)

[MEMO]

Summary of Contents

本製品が外国為替および外国貿易管理法の規定による戦略物資等（または役務）に該当するか否かは，ユーザ（仕様を決定した者）が判定してください。

○本資料の内容は，後日変更する場合があります。
○文書による当社の承諾なしに本資料の転載複製を禁じます。
○本資料に記載された製品の使用もしくは本資料に記載の情報の使用に際して，当社は当社もしくは第三者の知的所有権その他の権利に対する保証または実施権の許諾を行うものではありません。上記使用に起因する第三者所有の権利にかかわる問題が発生した場合，当社はその責を負うものではありませんのでご了承ください。
○当社は品質，信頼性の向上に努めていますが，半導体製品はある確率で故障が発生します。当社半導体製品の故障により結果として，人身事故，火災事故，社会的な損害等を生じさせない冗長設計，延焼対策設計，誤動作防止設計等安全設計に十分ご注意願います。
○当社は，当社製品の品質水準を「標準水準」，「特別水準」およびお客様に品質保証プログラムを指定して頂く「特定水準」に分類しております。また，各品質水準は以下に示す用途に製品が使われることを意図しておりますので，当社製品の品質水準をご確認の上ご使用願います。

標準水準：コンピュータ，OA機器，通信機器，計測機器，AV機器，家電，工作機械，パーソナル機器，産業用ロボット
特別水準：輸送機器（自動車，列車，船舶等），交通用信号機器，防災／防犯装置，各種安全装置，生命維持を直接の目的としない医療機器
特定水準：航空機器，航空宇宙機器，海底中継機器，原子力制御システム，生命維持のための医療機器，生命維持のための装置またはシステム等

当社製品のデータ・シート／データ・ブック等の資料で，特に品質水準の表示がない場合は標準水準製品であることを表します。当社製品を上記の「標準水準」の用途以外でご使用をお考えのお客様は，必ず事前に当社販売窓口までご相談頂きますようお願い致します。
○この製品は耐放射線設計をしておりません。

OPENCAD is trademark of NEC Corporation.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377
Fax: 02-2719-5951

NEC do Brasil S.A.
Electron Devices Division
Rodovia Presidente Dutra, Km 214
07210-902-Guarulhos-SP Brasil
Tel: 55-11-6465-6810
Fax: 55-11-6465-6829

本版で改訂された主な箇所

Major Revisions in this Edition

箇　所　Page	内　　容	Description
CHAPTER 4 INTERFACE BLOCK (HIGH SPEED SIGNAL TRANSMISSION)	・ファンクション名から GTL+の記述を削除 ・次のブロックを削除 FIR2, FIP2, ELTL, BL0W	・Deletion of the description of GTL+ from function names. ・Deletion of the following blocks. FIR2, FIP2, ELTL and BL0W.

巻末にアンケート・コーナを設けております。このドキュメントに対するご意見をお気軽にお寄せください。

[MEMO]

はじめに

1. 構成

このマニュアルはCMOS-8Lファミリ用ブロック・ライブラリについて記載しています。回路設計を行う際は必ず先にCMOS-8Lファミリ　ユーザーズ・マニュアル設計編（A12158J）を読んでください。

またマニュアルに記載された事項（一般事項，注意事項，制限事項）は必ずお守りください。お守りいただけない場合，LSI製品の品質や性能の低下，および動作の異常が生じることがあります。

このマニュアルは次のような構成になっています。

(1) はじめに
このマニュアルを活用されるにあたっての注意事項, 用語, 定義などを説明しています。

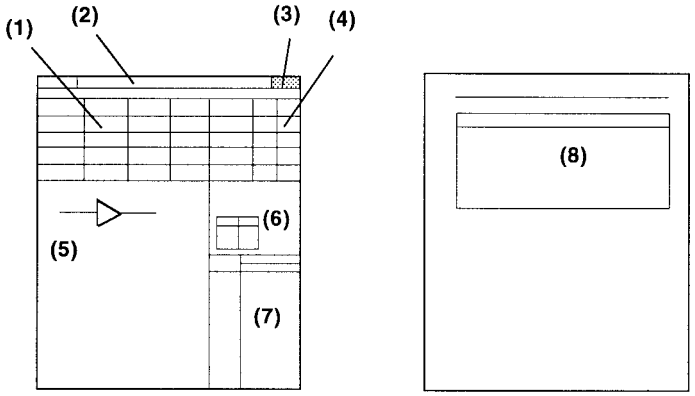
(2) CONTENTS
目次としてブロックを機能別にまとめてあります。

(3) CHAPTER 1　INTERFACE BLOCK (3.3V)
(4) CHAPTER 2　INTERFACE BLOCK (5V)
(5) CHAPTER 3　INTERFACE BLOCK (OSCILLATOR)
(6) CHAPTER 4　INTERFACE BLOCK (HIGH SPEED SIGNAL TRANSMISSION)
(7) CHAPTER 5　INTERFACE BLOCK (DIGITAL PLL)
(8) CHAPTER 6　FUNCTION BLOCK
CHAPTER 1～6は, それぞれのブロックを機能別に並べてあります。各ページには, 論理シンボル, 真理値表, 入出力データ, スイッチング・スピード（伝達遅延時間）などを2.ブロック・ライブラリ記載内容の説明に添って記載してあります。

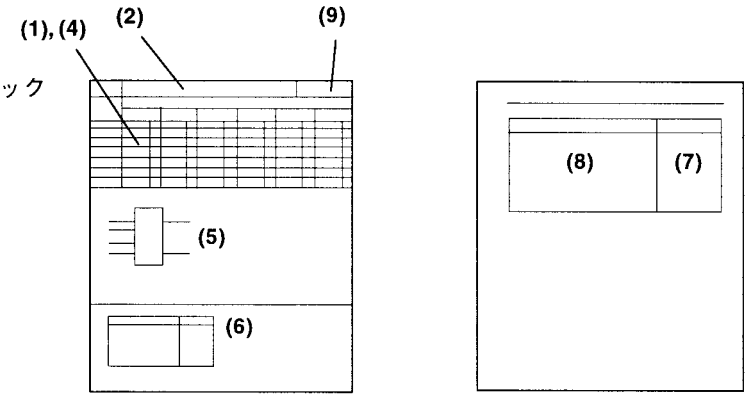
(9) INDEX
索引としてブロックをアルファベット順にまとめてあります。

2. ブロック・ライブラリ記載内容の説明

インタフェース・ブロック



ファンクション・ブロック



(1) Block Type : そのブロックの名称
(2) Function : そのブロックの機能名
(3) Interface Level : そのブロックのインタフェース・レベル
(4) No. of cells : 使用セル数
(5) Logic Diagram : そのブロックの論理シンボル（論理図）
(6) Truth Table : そのブロックの真理値表
(7) Input, Output : Input（入力端子名，Fan-in），Output（出力端子名，Fan-out）
(8) Switching Speed : そのブロックの伝達遅延時間など
(9) SSI FAMILY : 同じ機能を持つ74 (LS)シリーズ名

なお、スイッチング・スピードの記号は以下のとおりです。

A → Y (H L)
↑ ↑ ↑
(10) (11)(12)

(10) 信号のパス名（入力→出力）
(11) 入力信号の状態（H :ハイ・レベル，L : ロウ・レベル，Z :ハイ・インピーダンス）
(12) 出力信号の状態（H :ハイ・レベル，L : ロウ・レベル，Z :ハイ・インピーダンス）

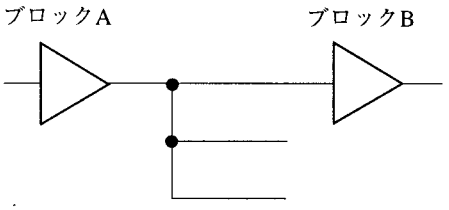
Setup time, Hold time, Release time, Removal time, Minimum pulse widthはMIN条件での最小値をMINの欄に記載しています。またMAX条件での最小値をMAXの欄に記載しています。

3. 伝達遅延時間(t_{PD})

ここで示す計算式は計算を簡易的に行うための概略計算式です。この計算式では特に負荷が次の条件を満足する範囲での算出結果が比較的精度よく求められるようになっています。負荷容量が大きいほど誤差が大きくなり，シミュレータの結果より小さい値を算出します。あらかじめ，ご承知のうえ目安としてご利用ください。

条件　遅延計算対象のブロックの前段のF/Iの合計が前段の駆動ブロックのF/O制限の15%以内である。

例



ブロックBが遅延計算対象のブロックとするとブロックAの出力に接続されるF/Iの合計がブロックAのF/O制限の15%以内のとき，簡易計算式の精度が高い。

3.1　伝達遅延時間の概算式

3.1.1　内部ファンクション・ブロックの遅延時間

内部ファンクション・ブロックの遅延時間は，メモリ・ブロックを含み，そのブロックに接続されている負荷（ファンアウト数）とその配線長（配線容量）から概算できます。

$$t_{PD} = t_{LD0} + (F/O + \ell) \times t_I \ (ns)$$

t_{LD0} ： F/O=0, ℓ =0におけるブロック自身の遅延時間
F/O： 該当出力端子のファンアウト数
ℓ ： 該当出力端子の配線容量（3.1.3 予測配線容量参照）
t_I ： 該当出力端子の遅延係数

3.1.2　出力バッファの遅延時間

出力バッファの遅延時間は，その出力端子に接続されている負荷容量によって大きく変わります。また，遅延時間の負荷容量依存性はそのバッファの駆動能力によっても変わります。

出力バッファの遅延時間(t_{PD})は，負荷容量(C_L)に対して次の式で概算できます。

$$t_{PD} = t_{LD0} + T \times C_L \ (ns)$$

t_{LD0} ： 基準遅延時間(ns)
T ： 遅延係数
C_L ： 負荷容量(pF) (ただし，$C_L \geqq 15$ pF)

なお，入出力バッファの遅延時間は，次の条件下で求められています。

3.3Vインタフェース：スレッシュホールド電圧＝1.5V スイング・レベル=0～V_{DD}

5Vインタフェース：スレッシュホールド電圧＝1.5V スイング・レベル=0～V_{DD}

ただし，5 Vインタフェースもハイ・レベルはゲートアレイの電源電圧とします。

3.1.3　予測配線容量

CMOS-8Lファミリの予測配線容量は次のようになります。

表3-1　予測配線容量（配線長をFan-in値に換算）

品名	ピン・ペア数											
	1	2	3	4	5	6	7	8	9	10	11～15	16～20
μPD65837												
μPD65839												
μPD65840/60	1.67	3.19	4.72	6.25	7.78	9.30	10.83	12.36	13.89	15.42	16.94	18.47
μPD65841/61	1.69	3.49	5.28	7.08	8.87	10.67	12.46	14.26	16.06	17.85	19.65	21.44
μPD65842/62	1.71	3.68	5.65	7.62	9.59	11.57	13.54	15.51	17.48	19.45	21.42	23.39
μPD65843/63	1.74	3.86	5.98	8.10	10.23	12.35	14.47	16.59	18.71	20.83	22.96	25.08
μPD65845/65	1.77	4.03	6.30	8.56	10.82	13.08	15.35	17.61	19.87	22.14	24.40	26.66
μPD65846/66	1.79	4.15	6.51	8.87	11.23	13.58	15.94	18.30	20.66	23.01	25.37	27.73
μPD65848/68	1.85	4.38	6.91	9.44	11.97	14.49	17.02	19.55	22.08	24.61	27.14	29.67
μPD65849/69	1.90	4.58	7.25	9.92	12.60	15.27	17.94	20.61	23.29	25.96	28.63	31.31
μPD65850/70	1.96	4.74	7.53	10.32	13.10	15.89	18.67	21.46	24.25	27.03	29.82	32.61
μPD65851/71	2.04	4.97	7.90	10.84	13.77	16.70	19.63	22.57	25.50	28.43	31.37	34.30
μPD65852/72	2.21	5.38	8.55	11.72	14.89	18.06	21.24	24.41	27.58	30.75	33.92	37.09
μPD65853/73	2.38	5.74	9.11	12.47	15.83	19.19	22.55	25.91	29.27	32.63	36.00	39.36
μPD65855/75	2.70	6.32	9.93	13.55	17.16	20.78	24.39	28.01	31.62	35.23	35.85	42.46

備考　空白：検討中

4. 入力インタフェース・レベル

次の5種類の入力インタフェース・レベルを用意してあります。用途にあわせて最適なものを選択してください。

(1) 3.3V入力
(2) 5V入力
(3) 3.3Vシュミット入力
(4) 5Vシュミット入力
(5) Failsafe機能付き3.3V入力

5. 出力駆動能力

次のような出力駆動能力が異なるバッファを多数用意していますので,用途にあわせて最適なものを選択してください。

(1) 3.3V出力(6種類) : 3.0mA, 6.0mA, 9.0mA, 12.0mA, 18.0mA, 24.0mA
(2) 5V出力(8種類) : 1.0mA, 2.0mA, 3.0mA, 6.0mA, 9.0mA, 12.0mA, 18.0mA, 24.0mA

6. 高性能バッファ

6.1 プルアップ／プルダウン抵抗付きバッファ

入力／出力／双方向バッファに次のようなプルアップ抵抗付き,プルダウン抵抗付きのものを用意しています。用途にあわせて最適なものを選択してください。

(1) プルアップ抵抗：50kΩ (TYP)
(2) プルダウン抵抗：50kΩ (TYP)
(3) プルアップ抵抗： 5kΩ (TYP)

6.2 ロウ・スルーレート・バッファ

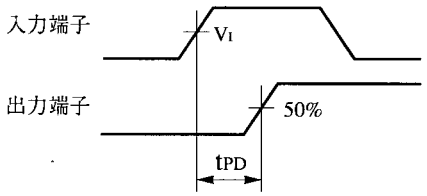
スルーレートを低くし,ロウ・ノイズ化を図った出力／双方向バッファを用意しており,ロウ・スルーレート・バッファと呼びます。なお，このマニュアルではLOW NOISEまたはLow slew-rateと表示します。

7. 伝達遅延時間の定義

入力／出力バッファの伝達遅延時間は, 次の定義による値を記載しています。

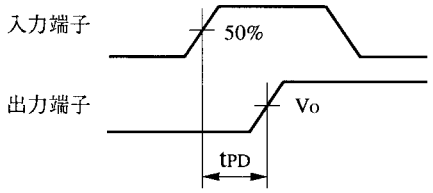
(1) 入力バッファ

V_I = 1.5V (3.3V入力)
V_I = 1.5V (5V入力)　→ (内部電圧振幅) ×50%



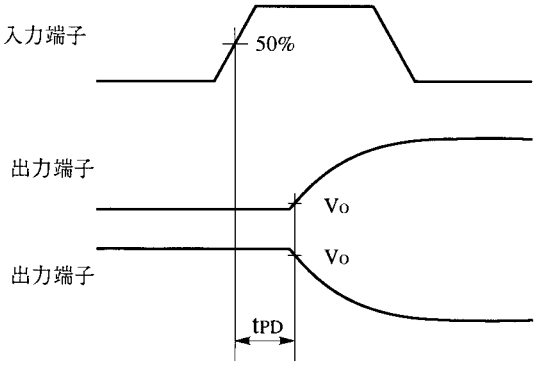
(2) 出力バッファ(L→H, H→L, Z→H(初期VO = "L"レベル), Z→L(初期VO = "H"レベル))

(内部電圧振幅) ×50% → V_O = 1.5V (3.3V出力)
V_O = 1.5V (5V出力)



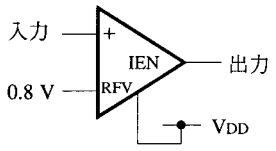
(3) 出力バッファ(L→Z, H→Z)

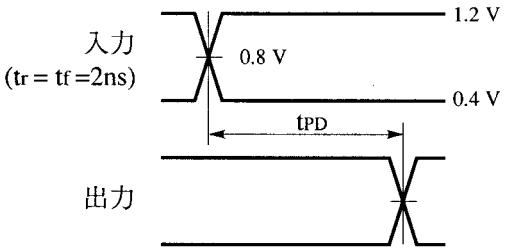
(内部電圧振幅) ×50% → $V_O = 0.1 \times V_{DD}$ (L→Z)
$V_O = 0.9 \times V_{DD}$ (H→Z)



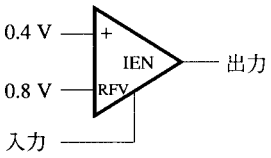
(4) GTL入力

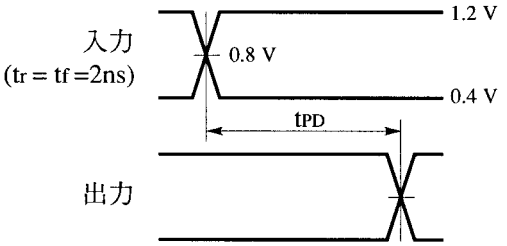
(a)



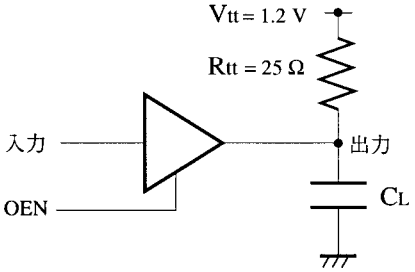


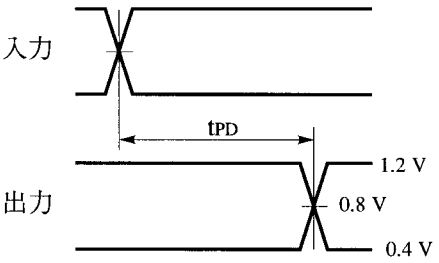
(b)





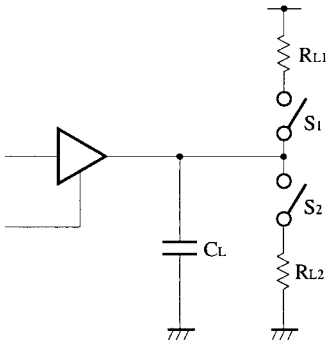
(5) GTL出力





8. 測定負荷条件

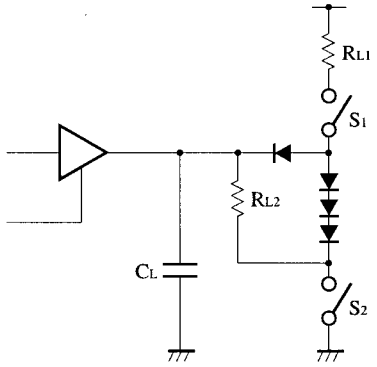
(1) CMOSレベル出力バッファ



① 通常出力バッファ
R_{L1}, R_{L2} = ∞, C_L = 15pF
(S_1, S_2 : OFF)

② 3ステート出力バッファ
R_{L1}=2kΩ, R_{L2}=2kΩ, C_L=15pF
$t_{P(HH)}$, $t_{P(LL)}$: S_1=OFF, S_2=OFF
$t_{P(ZL)}$, $t_{P(LZ)}$: S_1=ON, S_2=OFF
$t_{P(ZH)}$, $t_{P(HZ)}$: S_1=OFF, S_2=ON

(2) TTLレベル出力バッファ



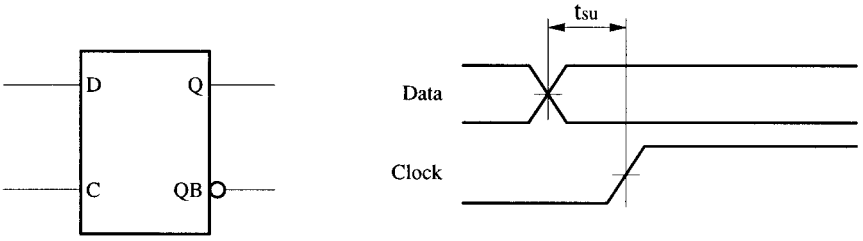
① 通常出力バッファ
R_{L1} = 500Ω, R_{L2} = ∞, C_L = 15pF
(S_1, S_2 : OFF)

② 3ステート出力バッファ
R_{L1} = 500Ω, R_{L2} = 1kΩ, C_L = 15pF
$t_{P(HH)}$, $t_{P(LL)}$: S_1 = OFF, S_2 = OFF
$t_{P(ZL)}$, $t_{P(LZ)}$: S_1 = ON, S_2 = OFF
$t_{P(ZH)}$, $t_{P(HZ)}$: S_1 = OFF, S_2 = ON

9. タイミング

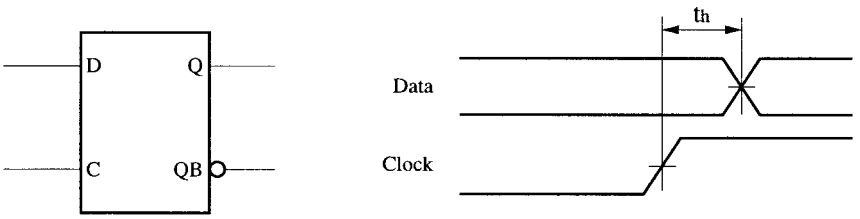
(1) セットアップ・タイム（t_{su}）

D-F/Fなどで, クロックが変化する前にデータ信号が確定していなければならない時間。



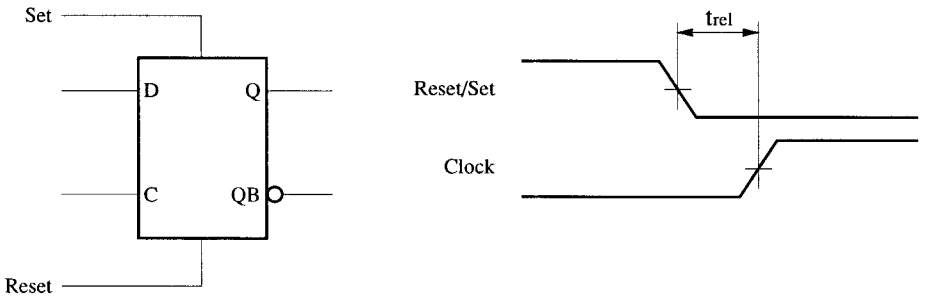
(2) ホールド・タイム（t_h）

D-F/Fなどで, クロックが変化したあとにデータ信号を保持していなければならない時間。



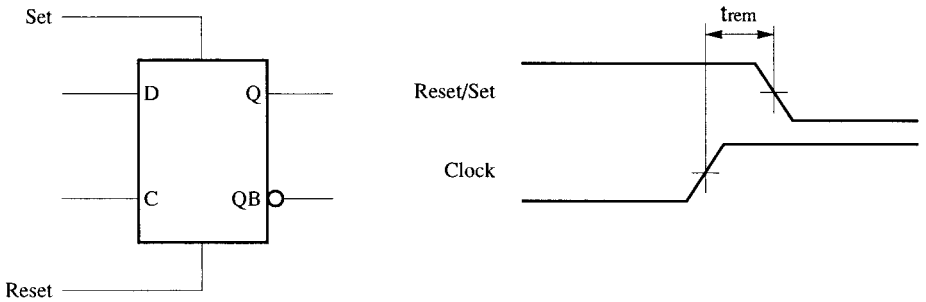
(3) リリース・タイム（t_{rel}）

D-F/Fなどで, リセットかセットが解除になってからクロックが有効になるまでの時間。



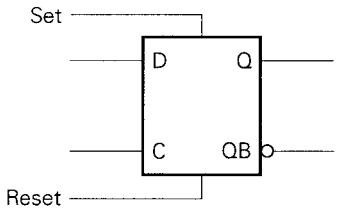
(4) リムーバル・タイム（t_{rem}）

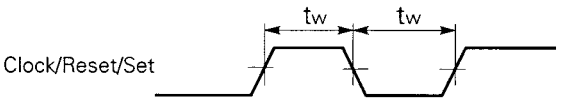
D-F/Fなどで, クロックを無効にするまでのセットまたはリセットの保持時間。



(5) 最小パルス幅（tw）

D-F/Fなどで, データを正常に読み込むために必要となるクロック，リセット，セットのパルス幅の最小時間。





関連資料

関連資料は暫定版の場合がありますが，この資料では「暫定」の表示をしておりません。あらかじめご了承ください。

・CMOS-8Lファミリ　ユーザーズ・マニュアル　設計編	(A12158J)
・CMOS-8L Family　Block Library　User's Manual	(このマニュアル)
・CMOS-8L Family　Memory Block Library　User's Manual	(A11700X)
・CMOSゲートアレイ，CMOSエンベデッドアレイ スキャンパス設計マニュアル　ユーザーズ・マニュアル	(A12212J)
・CMOSゲートアレイ，CMOSエンベデッドアレイ バウンダリ・スキャン設計マニュアル　ユーザーズ・マニュアル	(A11850J)
・CMOS-8L Family　Scan Path Block Library　User's Manual	(A11886X)
・CMOS-8L Family　Boundary Scan Block Library　User's Manual	(A11544X)

[MEMO]

PREFACE

This library contains the interface blocks and the internal function blocks of the CMOS-8L gate array family.

When carrying out circuit design, it is requested that the CMOS-8L gate array design manual(A12158E) should also be read. Furthermore, as there are occasions when this block library is changed without advance notice, please contact your local NEC ASIC design center.

Please observe all items listed in this manual(general matters,cautions,limitations).

If you don't observe these things,degradation in the quality and performance of LSI's or abnormal operation may occur.

1. Introduction

This library is composed of preface, contents, six chapters, and index as explained below.

(1) PREFACE

The usage of this library, meanings of terminologies and some information are described.

(2) CONTENTS

This CONTENTS is useful when searching a block from its function.

(3) CHAPTER 1 INTERFACE BLOCK (3.3V)
(4) CHAPTER 2 INTERFACE BLOCK (5V)
(5) CHAPTER 3 INTERFACE BLOCK (OSCILLATOR)
(6) CHAPTER 4 INTERFACE BLOCK (HIGH SPEED SIGNAL TRANSMISSION)
(7) CHAPTER 5 INTERFACE BLOCK (DIGITAL PLL)
(8) CHAPTER 6 FUNCTION BLOCK

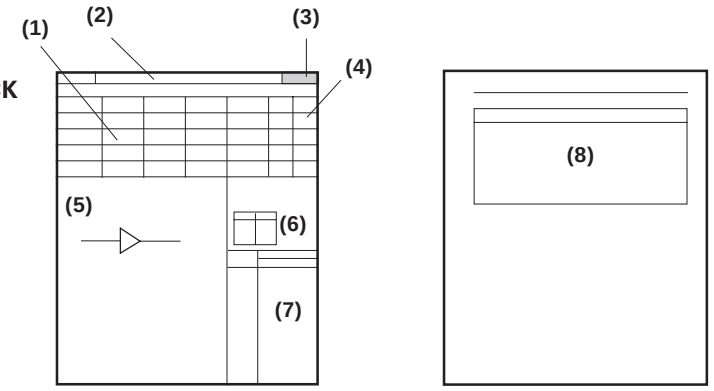
CHAPTER 1 to 6 list each block by function. Each page describes a logic symbol, a truth table, I/O data and delay time with an integrated format as explained in **2. Data Entered in the Block Library** of this PREFACE.

(9) INDEX

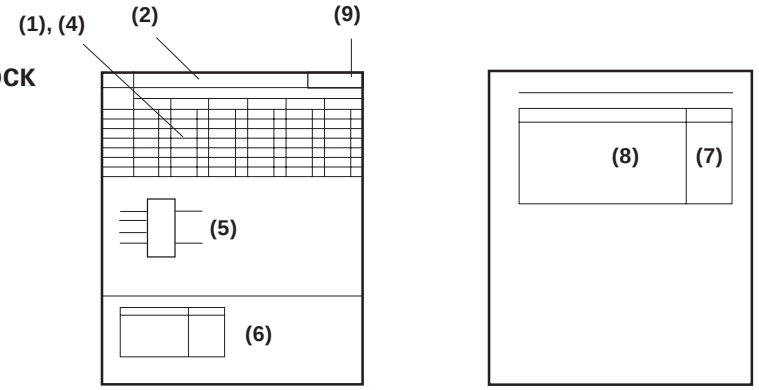
This list is useful when searching a block from its name.

2. Data Entered in the Block Library

INTERFACE BLOCK



FUNCTION BLOCK



(1) Block Type	:	Name of function block
(2) Function	:	Function of that block
(3) Interface Level	:	Interface level of that block
(4) No. of INT cells	:	No. of cells used (internal cell number)
(5) Logic Diagram	:	Symbol of that block
(6) Truth Table	:	Truth table of that block
(7) Input, Output	:	Input(Name of input pin, Fan-in)
		Output(Name of Output pin, Fan-out)
(8) Switching Speed	:	Delay time of that block
(9) SSI FAMILY	:	74(LS) series name which has the same function

Furthermore, the symbols of switching speed are as follows

$$\underset{(10)}{A \rightarrow Y} \quad \underset{(11)(12)}{(H\ L)}$$

(10) Signal path (input to output)
(11) Input signal change (H: rise L: fall Z: High impedance)
(12) Output signal change (H: rise L: fall Z: High impedance)

Setup time, Hold time, Release time, Removal time, Minimum pulse width;
MIN : The minimum result at the minimum condition
MAX : The minimum result at the maximum condition

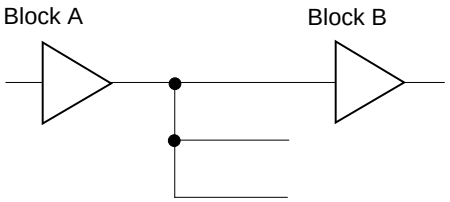
3. Propagation Delay Time (t_{PD})

The method shown here is a simplified calculation formula.This calculation method will give comparatively accurate results when the load matches the following conditions.The error becomes greater as the load capacitance increases,and the results yielded from the calculation are smaller than values obtained from the simulator.Therefore note beforehand that these values should be used mainly as a general guide.

Conditions

The total F/I of the front stage of the block for delay calculation shall be within 15% of the F/O limit of the front stage drive block.

Example



Let block B be the object of the propagation calculation. The accuracy of the simplified calculation formula is a high when the sum of the F/I connected to the output of Block A is wihthin 15% of the block A F/O limit.

3.1 Calculating Propagation Delay Time

3.1.1 Delay time of internal function block

The delay time of an internal function block can be estimated from the load (number of fan-outs) connected to the block including the memory block and its wiring length (wiring capacity).

$$t_{PD} = t_{LD0} + (F/O + \ell) \times t_1 \quad (ns)$$

t_{LD0} : Delay time of block itself when F/O = 0, ℓ= 0
F/O : Number of fan-outs of output pin
ℓ : Wiring capacitance of output pin (see **3.1.3 Estimated Wiring Capacitance**)
t_1 : Delay coefficient of output pin

3.1.2 Delay time of output buffer

The delay time of an output buffer greatly depends on the load capacitance connected to the output pin. The dependency of delay time on load capacitance varies with the drive capability of the buffer.

The delay time tPD of an output buffer can be estimated for the given load capacitance using the following formula:

$$t_{PD} = t_{LD0} + T \times C_L \quad (ns)$$

t_{LD0} : Reference delay time (ns)
T : Delay coefficient
C_L : Load capacitance (pF) ($C_L \geq 15$ pF)
t_{PD0} and T are listed in each page.

The delay time of an I/O buffer is obtained as follows:

3.3 V interface Threshold voltage = 1.5 V Swing level = 0 to V_{DD}
5 V interface Threshold voltage = 1.5 V Swing level = 0 to V_{DD}

The high level of 5 V interface is equal to the power supply of gate array.

3.1.3 Estimated Wiring Capacitance

The table 3-1 shows the values of estimated wiring capacitance of CMOS-8L family.

Table 3-1 Estimated Wiring Capacitance (Converted to Fan-in Mode)

Master	Pin Pairs											
	1	2	3	4	5	6	7	8	9	10	11 to 15	16 to 20
μPD65837												
μPD65839												
μPD65840/60	1.67	3.19	4.72	6.25	7.78	9.30	10.83	12.36	13.89	15.42	16.94	18.47
μPD65841/61	1.69	3.49	5.28	7.08	8.87	10.67	12.46	14.26	16.06	17.85	19.65	21.44
μPD65842/62	1.71	3.68	5.65	7.62	9.59	11.57	13.54	15.51	17.48	19.45	21.42	23.39
μPD65843/63	1.74	3.86	5.98	8.10	10.23	12.35	14.47	16.59	18.71	20.83	22.96	25.08
μPD65845/65	1.77	4.03	6.30	8.56	10.82	13.08	15.35	17.61	19.87	22.14	24.40	26.66
μPD65846/66	1.79	4.15	6.51	8.87	11.23	13.58	15.94	18.30	20.66	23.01	25.37	27.73
μPD65848/68	1.85	4.38	6.91	9.44	11.97	14.49	17.02	19.55	22.08	24.61	27.14	29.67
μPD65849/69	1.90	4.58	7.25	9.92	12.60	15.27	17.94	20.61	23.29	25.96	28.63	31.31
μPD65850/70	1.96	4.74	7.53	10.32	13.10	15.89	18.67	21.46	24.25	27.03	29.82	32.61
μPD65851/71	2.04	4.97	7.90	10.84	13.77	16.70	19.63	22.57	25.50	28.43	31.37	34.30
μPD65852/72	2.21	5.38	8.55	11.72	14.89	18.06	21.24	24.41	27.58	30.75	33.92	37.09
μPD65853/73	2.38	5.74	9.11	12.47	15.83	19.19	22.55	25.91	29.27	32.63	36.00	39.36
μPD65855/75	2.70	6.32	9.93	13.55	17.16	20.78	24.39	28.01	31.62	35.23	35.85	42.46

Remark Blank : Under study

4. Input Interface Levels

The CMOS-8L gate array family has the following five types of input interface levels:

(1) 3.3 V input
(2) 5 V input
(3) 3.3 V Schmitt input
(4) 5 V Schmitt input
(5) 3.3 V input with failsafe

5. Output Drive Capability

The following levels are available for output drive capability (I_{OL}):

(1) 3.3 V output : Six types (3.0 mA, 6.0 mA, 9.0 mA, 12.0 mA, 18.0 mA, 24.0 mA)
(2) 5 V output : Eight types (1.0 mA, 2.0 mA, 3.0 mA, 6.0 mA, 9.0 mA, 12.0 mA, 18.0 mA, 24.0 mA)

6. Multifunction Buffers

6.1 Buffers with Pull-up/Pull-down Resistors

The CMOS-8L family has input/output/bidirectional buffers with following on-chip pull-up/pull-down resistors. Select one suitable for the specific application.

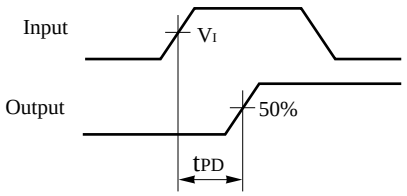
(1) Pull-up resistor : 50 kΩ (TYP)
(2) Pull-down resistor : 50 kΩ (TYP)
(3) Pull-up resistor : 5 kΩ (TYP)

6.2 Low Slew-Rate Buffers

The CMOS-8L family has special buffer which satisfies low noise requirement by fixing slew-rate low. This is called low slew-rate buffer. In this library, these buffers are described with a word "LOW NOISE" at their function description.

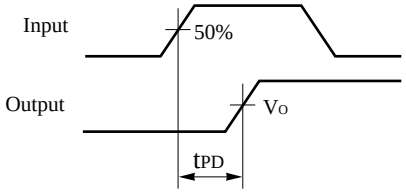
7. Definition of Propagation Delays

(1) Input Buffer



V_I = 1.5 V (3.3 V input)
V_I = 1.5 V (5 V input)

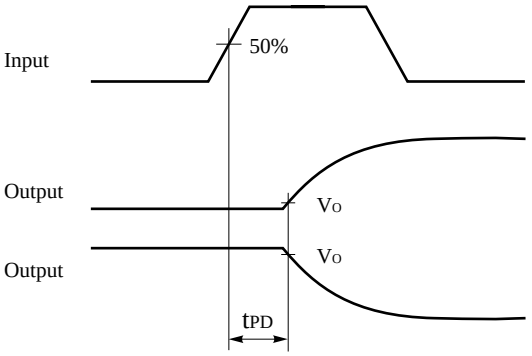
(2) Output Buffer (L → H, H → L, Z → H, Z → L)



V_O = 1.5 V (3.3 V output)
V_O = 1.5 V (5 V output)

- Z → H
  The beginning of V_O = L level
- Z → L
  The beginning of V_O = H level

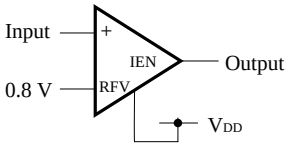
(3) Output Buffer (L → Z, H → Z)

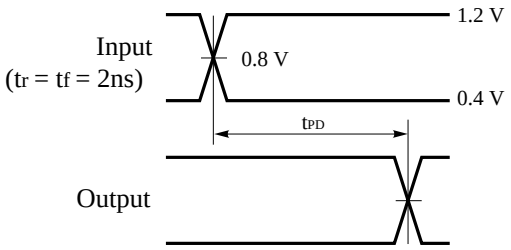


- L → Z
  The output level for high impedance
  $V_O = 0.1 \times V_{DD}$
- H → Z
  The output level for high impedance
  $V_O = 0.9 \times V_{DD}$

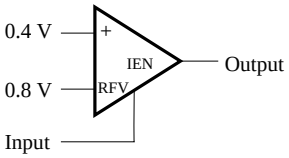
(4) GTL Input

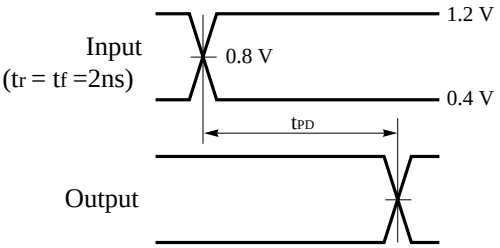
(a)



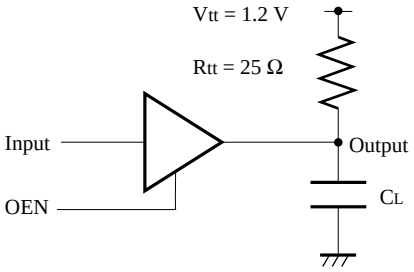


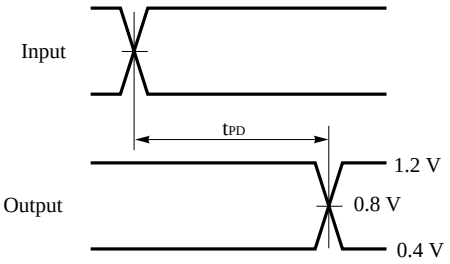
(b)





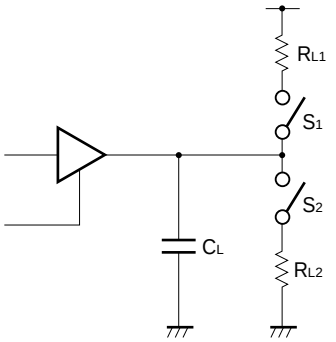
(5) GTL Output





8. Measurement Load Conditions

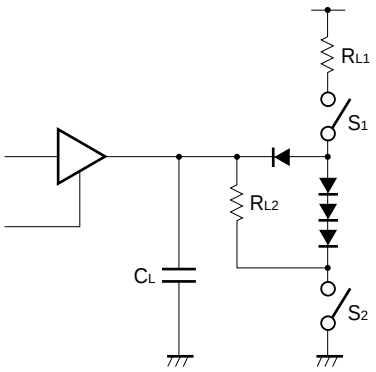
(1) CMOS level output buffer



- Normal Output Voltage
  R_{L1}, $R_{L2} = \infty$, C_L = 15 pF
  (S_1, S_2 : OFF)

- 3-State Output Buffer
  $R_{L1} = R_{L2}$ = 2 kΩ, C_L = 15 pF
  $t_{P(HH)}$, $t_{P(LL)}$: S_1 = OFF, S_2 = OFF
  $t_{P(ZL)}$, $t_{P(LZ)}$: S_1 = ON, S_2 = OFF
  $t_{P(ZH)}$, $t_{P(HZ)}$: S_1 = OFF, S_2 = ON

(2) TTL level output buffer



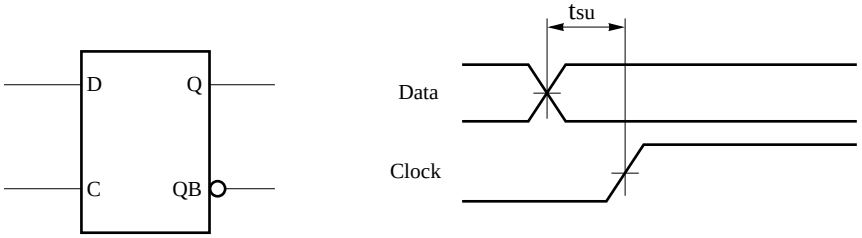
- Normal Output Voltage
  R_{L1} = 500 Ω, $R_{L2} = \infty$, C_L = 15 pF
  (S_1, S_2 : OFF)

- 3-State Output Buffer
  R_{L1} = 500 Ω, R_{L2} = 1 kΩ, C_L = 15 pF
  $t_{P(HH)}$, $t_{P(LL)}$: S_1 = OFF, S_2 = OFF
  $t_{P(ZL)}$, $t_{P(LZ)}$: S_1 = ON, S_2 = OFF
  $t_{P(ZH)}$, $t_{P(HZ)}$: S_1 = OFF, S_2 = ON

9. Timing

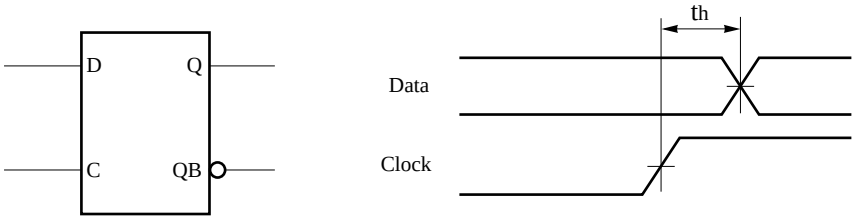
(1) Set up time(t_{su})

The data setup time required before arrival of an active edge of a clock to read data correctly.



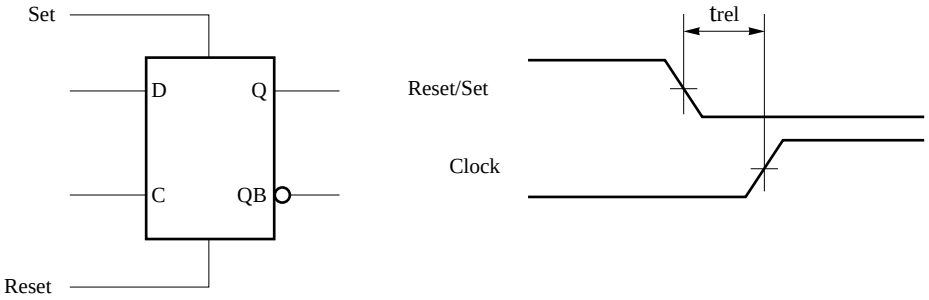
(2) Hold time(t_h)

The data hold time required after receiving an active edge of the clock to read data correctly.



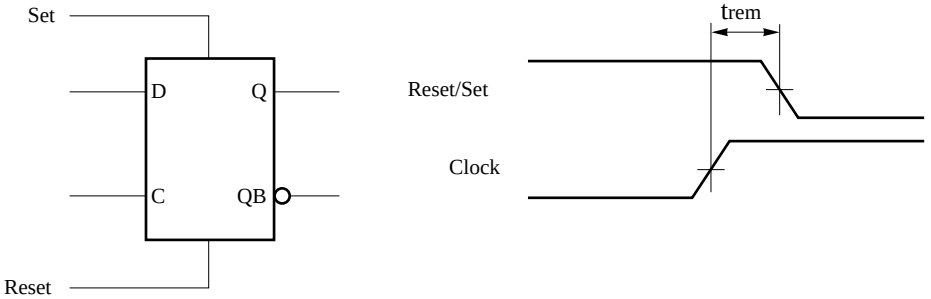
(3) Release time(t_{rel})

The time required from the release of a reset (or set) signal of a latch or flip-flop until the active edge of the next clock pulse becomes valid.



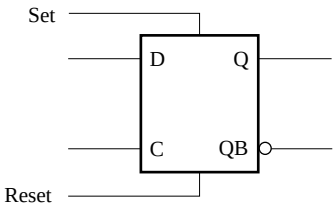
(4) Removal time(t_{rem})

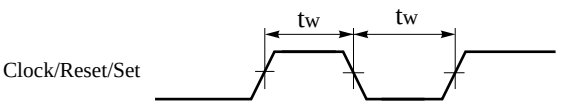
The time required to invalidate an active edge of a clock when a reset (or set) signal of a latch or flip-flop is released.



(5) Minimum Pulse Width(t_w)

The minimum pulse width of Clock/Reset/Set required to read data correctly.





CONTENTS

CHAPTER1 INTERFACE BLOCK(3.3V)

3-STATE OUTPUT BUFFER

LOW-NOISE 3-STATE OUTPUT BUFFER

HIGH SPEED 3-STATE OUTPUT BUFFER

N-CH OPEN DRAIN OUTPUT BUFFER

LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER

I/O BUFFER

LOW-NOISE I/O BUFFER

Name	Function	I/O cells	int. cells	Page
BE0C	LOW-NOISE I/O BUFFER 6mA	1	10	1-26
BEDC	LOW-NOISE I/O BUFFER 6mA 50kΩ PULL-DOWN	1	10	1-26
BEUC	LOW-NOISE I/O BUFFER 6mA 50kΩ PULL-UP	1	10	1-26
BEWC	LOW-NOISE I/O BUFFER 6mA 5kΩ PULL-UP	1	10	1-26
BE03	LOW-NOISE I/O BUFFER 9mA	1	10	1-26
BED3	LOW-NOISE I/O BUFFER 9mA 50kΩ PULL-DOWN	1	10	1-26
BEU3	LOW-NOISE I/O BUFFER 9mA 50kΩ PULL-UP	1	10	1-26
BEW3	LOW-NOISE I/O BUFFER 9mA 5kΩ PULL-UP	1	10	1-26
BE01	LOW-NOISE I/O BUFFER 12mA	1	10	1-26
BED1	LOW-NOISE I/O BUFFER 12mA 50kΩ PULL-DOWN	1	10	1-26
BEU1	LOW-NOISE I/O BUFFER 12mA 50kΩ PULL-UP	1	10	1-26
BEW1	LOW-NOISE I/O BUFFER 12mA 5kΩ PULL-UP	1	10	1-26
BE05	LOW-NOISE I/O BUFFER 18mA	1	10	1-26
BED5	LOW-NOISE I/O BUFFER 18mA 50kΩ PULL-DOWN	1	10	1-26
BEU5	LOW-NOISE I/O BUFFER 18mA 50kΩ PULL-UP	1	10	1-26
BEW5	LOW-NOISE I/O BUFFER 18mA 5kΩ PULL-UP	1	10	1-26
BE0F	LOW-NOISE I/O BUFFER 24mA	1	10	1-26
BEDF	LOW-NOISE I/O BUFFER 24mA 50kΩ PULL-DOWN	1	10	1-26
BEUF	LOW-NOISE I/O BUFFER 24mA 50kΩ PULL-UP	1	10	1-26
BEWF	LOW-NOISE I/O BUFFER 24mA 5kΩ PULL-UP	1	10	1-26

HIGH SPEED I/O BUFFER

Name	Function	I/O cells	int. cells	Page
B02U	HIGH SPEED I/O BUFFER 3mA	1	16	1-28
B03U	HIGH SPEED I/O BUFFER 3mA 50kΩ PULL-DOWN	1	16	1-28
B04U	HIGH SPEED I/O BUFFER 3mA 50kΩ PULL-UP	1	16	1-28
B05U	HIGH SPEED I/O BUFFER 3mA 5kΩ PULL-UP	1	16	1-28
B02C	HIGH SPEED I/O BUFFER 6mA	1	16	1-28
B03C	HIGH SPEED I/O BUFFER 6mA 50kΩ PULL-DOWN	1	16	1-28
B04C	HIGH SPEED I/O BUFFER 6mA 50kΩ PULL-UP	1	16	1-28
B05C	HIGH SPEED I/O BUFFER 6mA 5kΩ PULL-UP	1	16	1-28
B023	HIGH SPEED I/O BUFFER 9mA	1	16	1-28
B033	HIGH SPEED I/O BUFFER 9mA 50kΩ PULL-DOWN	1	16	1-28
B043	HIGH SPEED I/O BUFFER 9mA 50kΩ PULL-UP	1	16	1-28
B053	HIGH SPEED I/O BUFFER 9mA 5kΩ PULL-UP	1	16	1-28
B021	HIGH SPEED I/O BUFFER 12mA	1	16	1-28
B031	HIGH SPEED I/O BUFFER 12mA 50kΩ PULL-DOWN	1	16	1-28
B041	HIGH SPEED I/O BUFFER 12mA 50kΩ PULL-UP	1	16	1-28
B051	HIGH SPEED I/O BUFFER 12mA 5kΩ PULL-UP	1	16	1-28
B025	HIGH SPEED I/O BUFFER 18mA	1	20	1-28
B035	HIGH SPEED I/O BUFFER 18mA 50kΩ PULL-DOWN	1	20	1-28
B045	HIGH SPEED I/O BUFFER 18mA 50kΩ PULL-UP	1	20	1-28
B055	HIGH SPEED I/O BUFFER 18mA 5kΩ PULL-UP	1	20	1-28
B02F	HIGH SPEED I/O BUFFER 24mA	1	20	1-28
B03F	HIGH SPEED I/O BUFFER 24mA 50kΩ PULL-DOWN	1	20	1-28
B04F	HIGH SPEED I/O BUFFER 24mA 50kΩ PULL-UP	1	20	1-28
B05F	HIGH SPEED I/O BUFFER 24mA 5kΩ PULL-UP	1	20	1-28

SCHMITT I/O BUFFER

Name	Function	I/O cells	int. cells	Page
BSIU	SCHMITT I/O BUFFER 3mA	1	14	1-30
BSDU	SCHMITT I/O BUFFER 3mA 50kΩ PULL-DOWN	1	14	1-30
BSUU	SCHMITT I/O BUFFER 3mA 50kΩ PULL-UP	1	14	1-30
BSWU	SCHMITT I/O BUFFER 3mA 5kΩ PULL-UP	1	14	1-30
BSIC	SCHMITT I/O BUFFER 6mA	1	14	1-30
BSDC	SCHMITT I/O BUFFER 6mA 50kΩ PULL-DOWN	1	14	1-30
BSUC	SCHMITT I/O BUFFER 6mA 50kΩ PULL-UP	1	14	1-30
BSWC	SCHMITT I/O BUFFER 6mA 5kΩ PULL-UP	1	14	1-30
BSI3	SCHMITT I/O BUFFER 9mA	1	14	1-30
BSD3	SCHMITT I/O BUFFER 9mA 50kΩ PULL-DOWN	1	14	1-30
BSU3	SCHMITT I/O BUFFER 9mA 50kΩ PULL-UP	1	14	1-30
BSW3	SCHMITT I/O BUFFER 9mA 5kΩ PULL-UP	1	14	1-30
BSI1	SCHMITT I/O BUFFER 12mA	1	14	1-30
BSD1	SCHMITT I/O BUFFER 12mA 50kΩ PULL-DOWN	1	14	1-30
BSU1	SCHMITT I/O BUFFER 12mA 50kΩ PULL-UP	1	14	1-30
BSW1	SCHMITT I/O BUFFER 12mA 5kΩ PULL-UP	1	14	1-30
BSI5	SCHMITT I/O BUFFER 18mA	1	18	1-30
BSD5	SCHMITT I/O BUFFER 18mA 50kΩ PULL-DOWN	1	18	1-30
BSU5	SCHMITT I/O BUFFER 18mA 50kΩ PULL-UP	1	18	1-30
BSW5	SCHMITT I/O BUFFER 18mA 5kΩ PULL-UP	1	18	1-30
BSIF	SCHMITT I/O BUFFER 24mA	1	18	1-30
BSDF	SCHMITT I/O BUFFER 24mA 50kΩ PULL-DOWN	1	18	1-30
BSUF	SCHMITT I/O BUFFER 24mA 50kΩ PULL-UP	1	18	1-30
BSWF	SCHMITT I/O BUFFER 24mA 5kΩ PULL-UP	1	18	1-30

LOW-NOISE SCHMITT I/O BUFFER

Name	Function	I/O cells	int. cells	Page
BFIC	LOW-NOISE SCHMITT I/O BUFFER 6mA	1	14	1-32
BFDC	LOW-NOISE SCHMITT I/O BUFFER 6mA 50kΩ PULL-DOWN	1	14	1-32
BFUC	LOW-NOISE SCHMITT I/O BUFFER 6mA 50kΩ PULL-UP	1	14	1-32
BFWC	LOW-NOISE SCHMITT I/O BUFFER 6mA 5kΩ PULL-UP	1	14	1-32
BFI3	LOW-NOISE SCHMITT I/O BUFFER 9mA	1	14	1-32
BFD3	LOW-NOISE SCHMITT I/O BUFFER 9mA 50kΩ PULL-DOWN	1	14	1-32
BFU3	LOW-NOISE SCHMITT I/O BUFFER 9mA 50kΩ PULL-UP	1	14	1-32
BFW3	LOW-NOISE SCHMITT I/O BUFFER 9mA 5kΩ PULL-UP	1	14	1-32
BFI1	LOW-NOISE SCHMITT I/O BUFFER 12mA	1	14	1-32
BFD1	LOW-NOISE SCHMITT I/O BUFFER 12mA 50kΩ PULL-DOWN	1	14	1-32
BFU1	LOW-NOISE SCHMITT I/O BUFFER 12mA 50kΩ PULL-UP	1	14	1-32
BFW1	LOW-NOISE SCHMITT I/O BUFFER 12mA 5kΩ PULL-UP	1	14	1-32
BFI5	LOW-NOISE SCHMITT I/O BUFFER 18mA	1	14	1-32
BFD5	LOW-NOISE SCHMITT I/O BUFFER 18mA 50kΩ PULL-DOWN	1	14	1-32
BFU5	LOW-NOISE SCHMITT I/O BUFFER 18mA 50kΩ PULL-UP	1	14	1-32
BFW5	LOW-NOISE SCHMITT I/O BUFFER 18mA 5kΩ PULL-UP	1	14	1-32
BFIF	LOW-NOISE SCHMITT I/O BUFFER 24mA	1	14	1-32
BFDF	LOW-NOISE SCHMITT I/O BUFFER 24mA 50kΩ PULL-DOWN	1	14	1-32
BFUF	LOW-NOISE SCHMITT I/O BUFFER 24mA 50kΩ PULL-UP	1	14	1-32
BFWF	LOW-NOISE SCHMITT I/O BUFFER 24mA 5kΩ PULL-UP	1	14	1-32

I/O BUFFER WITH EN(OR)

LOW NOISE I/O BUFFER WITH EN(OR)

CHAPTER2 INTERFACE BLOCK(5V)

INPUT BUFFER

INPUT BUFFER WITH EN(OR)

CMOS OUTPUT BUFFER

CMOS LOW-NOISE OUTPUT BUFFER

TTL OUTPUT BUFFER

TTL LOW-NOISE OUTPUT BUFFER

TTL HIGH SPEED OUTPUT BUFFER

CMOS 3-STATE OUTPUT BUFFER

CMOS LOW-NOISE 3-STATE OUTPUT BUFFER

TTL 3-STATE OUTPUT BUFFER

TTL LOW-NOISE 3-STATE OUTPUT BUFFER

TTL HIGH SPEED 3-STATE OUTPUT BUFFER

TTL N-CH OPEN DRAIN OUTPUT BUFFER

TTL LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER

CMOS I/O BUFFER

CMOS LOW-NOISE I/O BUFFER

CMOS SCHMITT I/O BUFFER

CMOS LOW-NOISE SCHMITT I/O BUFFER

TTL I/O BUFFER

TTL LOW-NOISE I/O BUFFER

TTL HIGH SPEED I/O BUFFER

TTL SCHMITT I/O BUFFER

TTL LOW-NOISE SCHMITT I/O BUFFER

CMOS I/O BUFFER WITH EN(OR)

CMOS LOW NOISE I/O BUFFER WITH EN(OR)

TTL I/O BUFFER WITH EN(OR)

LOW NOISE I/O BUFFER WITH EN(OR)

CHAPTER3 INTERFACE BLOCK(OSCILLATOR)

CHAPTER4 INTERFACE BLOCK(HIGH SPEED SIGNALE TRANSMISSION)

3V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL

5V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL

GTL INPUT BUFFER WITH EN

GTL INPUT BUFFER FOR REFERENCE VOLTAGE

GTL OUTPUT BUFFER WITH ENB

GTL I/O BUFFER

P-ECL INPUT BUFFER WITH EN

P-ECL OUTPUT BUFFER

CHAPTER5 INTERFACE BLOCK (DIGITAL PLL)

CHAPTER6 FUNCTION BLOCK

H,L LEVEL GENERATOR

INTERFACE BLOCK FOR OSCILLATOR BUFFER

INVERTER

BUFFER

CLOCK DRIVER

CLOCK DRIVER SINGLE OUT

CLOCK TREE SYNTHESIS DRIVER

3-STATE BUFFER

3-STATE BUFFER

DELAY GATE

2-INPUT NOR

3-INPUT NOR

4-INPUT NOR

5-INPUT NOR

6-INPUT NOR

8-INPUT NOR

2-INPUT OR

3-INPUT OR

4-INPUT OR

5-INPUT OR

6-INPUT OR

8-INPUT OR

2-INPUT NAND

3-INPUT NAND

4-INPUT NAND

5-INPUT NAND

6-INPUT NAND

8-INPUT NAND

2-INPUT AND

3-INPUT AND

4-INPUT AND

5-INPUT AND

6-INPUT AND

8-INPUT AND

2-INPUT EXCLUSIVE OR

3-INPUT EXCLUSIVE OR

2-INPUT EXCLUSIVE NOR

3-INPUT EXCLUSIVE NOR

1-2-INPUT AND-OR-INVERTER

1-1-2-INPUT AND-OR-INVERTER

1-3-INPUT AND-OR-INVERTER

2-2-INPUT AND-OR-INVERTER

2-2-2-INPUT AND-OR-INVERTER

3-3-INPUT AND-OR-INVERTER

2-3-INPUT AND-OR-INVERTER

1-2-2-INPUT AND-OR-INVERTER

2-2-2-2-INPUT AND-OR-INVERTER

4-4-INPUT AND-OR-INVERTER

1-2-3-INPUT AND-OR-INVERTER

1-2-INPUT OR-AND-INVERTER

1-1-2-INPUT OR-AND-INVERTER

1-3-INPUT OR-AND-INVERTER

2-2-INPUT OR-AND-INVERTER

2-3-INPUT OR-AND-INVERTER

3-3-INPUT OR-AND-INVERTER

1-2-2-INPUT OR-AND-INVERTER

2-2-2-INPUT OR-AND-INVERTER

2-2-2-2-INPUT OR-AND-INVERTER

D-LATCH

D-LATCH HIGH SPEED

D-LATCH WITH R

D-LATCH WITH R HIGH SPEED

D-LATCH WITH RB

D-LATCH WITH RB HIGH SPEED

D-LATCH WITH SB

D-LATCH (GB)

D-LATCH (GB) HIGH SPEED

D-LATCH (GB) WITH RB

4-BIT D-LATCH

4-BIT D-LATCH HIGH SPEED

8-BIT D-LATCH

8-BIT D-LATCH HIGH SPEED

RS-LATCH

D-F/F

D-F/F WITH R

D-F/F WITH S

D-F/F WITH R,S

D-F/F WITH RB

D-F/F WITH SB

D-F/F WITH RB,SB

D-F/F (CB)

D-F/F (CB) WITH RB

D-F/F (CB) WITH SB

D-F/F (CB) WITH RB,SB

Name	Function	I/O cells	int. cells	Page
L637	D-F/F (CB) WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-252
F667	D-F/F (CB) WITH RB,SB	-	10	6-252
F637	D-F/F (CB) WITH RB,SB	-	10	6-252
F667NP	D-F/F (CB) WITH RB,SB (X2 DRIVE)	-	12	6-252
F667NQ	D-F/F (CB) WITH RB,SB Q OUT ONLY	-	9	6-252
F667NQP	D-F/F (CB) WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	10	6-252
F667NB	D-F/F (CB) WITH RB,SB QB OUT ONLY	-	9	6-252
F667NBP	D-F/F (CB) WITH RB,SB QB OUT ONLY (X2 DRIVE)	-	10	6-252

4-BIT D-F/F

Name	Function	I/O cells	int. cells	Page
F924	4-BIT D-F/F	-	28	6-256
L924	4-BIT D-F/F Q OUT ONLY (LOW POWER)	-	18	6-256

4-BIT D-F/F WITH R

Name	Function	I/O cells	int. cells	Page
F922	4-BIT D-F/F WITH R	-	33	6-258
L922	4-BIT D-F/F WITH R Q OUT ONLY (LOW POWER)	-	23	6-258

RS-F/F WITH R,S

Name	Function	I/O cells	int. cells	Page
F596	RS-F/F WITH R,S	-	11	6-262

T-F/F WITH R,S

Name	Function	I/O cells	int. cells	Page
L714	T-F/F WITH R,S Q OUT ONLY (LOW POWER)	-	7	6-264
F744	T-F/F WITH R,S	-	9	6-264
F714	T-F/F WITH R,S	-	9	6-264
F744NP	T-F/F WITH R,S (X2 DRIVE)	-	11	6-264
F744NQ	T-F/F WITH R,S Q OUT ONLY	-	8	6-264
F744NQP	T-F/F WITH R,S Q OUT ONLY (X2 DRIVE)	-	9	6-264

T-F/F WITH RB,SB

Name	Function	I/O cells	int. cells	Page
L717	T-F/F WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-268
F747	T-F/F WITH RB,SB	-	9	6-268
F717	T-F/F WITH RB,SB	-	9	6-268
F747NP	T-F/F WITH RB,SB (X2 DRIVE)	-	11	6-268
F747NQ	T-F/F WITH RB,SB Q OUT ONLY	-	8	6-268
F747NQP	T-F/F WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	9	6-268

T-F/F (TB) WITH RB,SB

Name	Function	I/O cells	int. cells	Page
L737	T-F/F (TB) WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-272
F767	T-F/F (TB) WITH RB,SB	-	9	6-272
F737	T-F/F (TB) WITH RB,SB	-	9	6-272
F767NP	T-F/F (TB) WITH RB,SB (X2 DRIVE)	-	11	6-272
F767NQ	T-F/F (TB) WITH RB,SB Q OUT ONLY	-	8	6-272
F767NQP	T-F/F (TB) WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	9	6-272

T-F/F WITH DATA-HOLD R,S

Name	Function	I/O cells	int. cells	Page
F791	T-F/F WITH DATA-HOLD R,S	-	12	6-276

T-F/F (TB) WITH DATA-HOLD RB,SB

JK-F/F

JK-F/F WITH R,S

JK-F/F WITH RB,SB

JK-F/F (CB)

JK-F/F (CB) WITH RB, SB

2 TO 1 MULTIPLEXER

QUAD 2 TO 1 MULTIPLEXER

Name	Function	I/O cells	int. cells	Page
F552	QUAD 2 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	13	6-298
F555	QUAD 2 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	9	6-298
L572	QUAD 2 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB (LOW POWER)	-	10	6-298
F572	QUAD 2 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB	-	14	6-298

4 TO 1 MULTIPLEXER

Name	Function	I/O cells	int. cells	Page
F564	4 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	8	6-302
F570	4 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB	-	10	6-302
F57A	4 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	10	6-302

QUAD 4 TO 1 MULTIPLEXER

Name	Function	I/O cells	int. cells	Page
F551	QUAD 4 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	27	6-304
F554	QUAD 4 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	31	6-304

8 TO 1 MULTIPLEXER

Name	Function	I/O cells	int. cells	Page
F563	8 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	17	6-308
F569	8 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB	-	18	6-308
F579	8 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	17	6-308

QUAD 8 TO 1 MULTIPLEXER

Name	Function	I/O cells	int. cells	Page
F550	QUAD 8 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	64	6-312
F553	QUAD 8 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	64	6-316

2 TO 4 DECODER

Name	Function	I/O cells	int. cells	Page
L560	2 TO 4 DECODER POSITIVE OUTPUT (LOW POWER)	-	6	6-320
F560	2 TO 4 DECODER POSITIVE OUTPUT	-	10	6-320
L561	2 TO 4 DECODER NEGATIVE OUTPUT (LOW POWER)	-	6	6-320
F561	2 TO 4 DECODER NEGATIVE OUTPUT	-	10	6-320
L981	2 TO 4 DECODER NEGATIVE OUTPUT WITH ENB (LOW POWER)	-	8	6-320
F981	2 TO 4 DECODER NEGATIVE OUTPUT WITH ENB	-	13	6-320

3 TO 8 DECODER

Name	Function	I/O cells	int. cells	Page
L982	3 TO 8 DECODER NEGATIVE OUTPUT WITH ENB (LOW POWER)	-	21	6-324
F982	3 TO 8 DECODER NEGATIVE OUTPUT WITH ENB	-	26	6-324

8-BIT ODD PARITY GENERATOR

Name	Function	I/O cells	int. cells	Page
F581	8-BIT ODD PARITY GENERATOR	-	19	6-328

8-BIT EVEN PARITY GENERATOR

Name	Function	I/O cells	int. cells	Page
F582	8-BIT EVEN PARITY GENERATOR	-	19	6-330

1-BIT FULL ADDER

Name	Function	I/O cells	int. cells	Page
F521	1-BIT FULL ADDER	-	9	6-332

4-BIT FULL ADDER

4-BIT LOOK AHEAD CARRY GENERATOR

1-BIT CARRY LOOK AHEAD ADDER

4-BIT MAGNITUDE COMPARATOR

4-BIT SERIAL/PARALLEL SHIFT REGISTER

4-BIT SHIFT REGISTER WITH R

4-BIT SHIFT REGISTER WITH LOAD

4-BIT SYNCHRONOUS BINARY COUNTER WITH RB

D-F/F WITH R,S,2 TO 1 SELECTOR

D-F/F WITH 2 TO 1 SELECTOR

D-F/F WITH R,S,HOLD,2 TO 1 SELECTOR

D-F/F WITH HOLD,2 TO 1 SELECTOR

JK-F/F WITH R,S,D-F/F FUNCTION

JK-F/F WITH D-F/F FUNCTION

JK-F/F WITH R,S,HOLD,D-F/F FUNCTION

JK-F/F WITH HOLD,D-F/F FUNCTION

D-LATCH WITH R,D-F/F FUNCTION

D-LATCH WITH D-F/F FUNCTION

D-LATCH WITH R,SPECIAL FUNCTION

D-LATCH WITH SPECIAL FUNCTION

2 TO 1 DATA SELECTOR

[MEMO]

[MEMO]

CHAPTER 1

INTERFACE BLOCK

(3.3V)

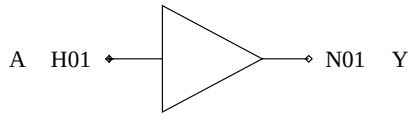
1 - 1

INTERFACE BLOCK (3.3V)

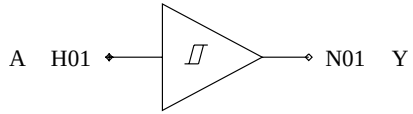
Function	INPUT BUFFER					3.3V
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FI01	FID1	FIU1	FIW1	1	4
Schmitt	FIS1	FDS1	FUS1	FWS1	1	8
Clock	FIB1	FDB1	FUB1	FWB1	1	24

Logic Diagram

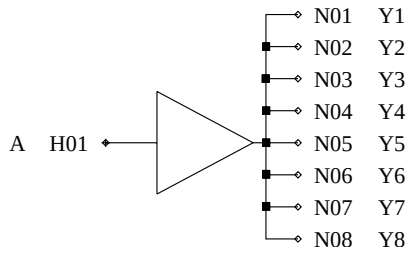
"Normal"



"Schmitt"



"Clock"



Truth Table

A	Yn
1	1
0	0

(n=1 to 8)

Block type	Input		Output	
	Symbol	Fan-In	Symbol	Fan-Out
FI01 to FIW1	A	-	Y	34
FIS1 to FWS1	A	-	Y	22
FIB1 to FWB1	A	-	Y1	34
	:	:	Y2	34
			:	:
			Y7	34
			Y8	34

INTERFACE BLOCK(3.3V)

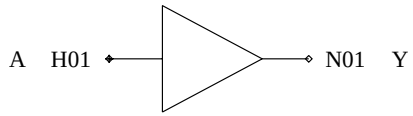
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FI01 to FIW1	A → Y	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
FIS1 to FWS1	A → Y	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
FIB1 to FWB1	A → Yn (n = 1 to 8)	(HH)	0.324	0.421	0.552	0.001	0.002	0.004			
		(LL)	0.217	0.332	0.463	0.001	0.002	0.003			

INTERFACE BLOCK (3.3V)

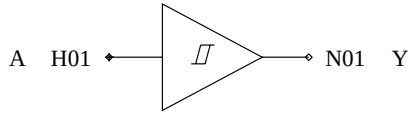
Function	INPUT BUFFER WITH FAILSAFE				3.3V	
	Block type					
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIA1	FDA1			1	4
Schmitt	FIE1	FDE1			1	8
Clock	FIH1	FDH1			1	24

Logic Diagram

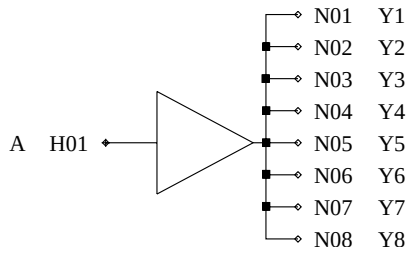
"Normal"



"Schmitt"



"Clock"



Truth Table

A	Yn
1	1
0	0

(n=1 to 8)

Block type	Input		Output	
	Symbol	Fan-In	Symbol	Fan-Out
FIA1 to FDA1	A	-	Y	34
FIE1 to FDE1	A	-	Y	22
FIH1 to FDH1	A	-	Y1	34
	:	:	Y2	34
			:	:
			Y7	34
			Y8	34

INTERFACE BLOCK(3.3V)

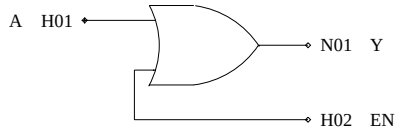
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIA1	A → Y	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
to FDA1		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
FIE1	A → Y	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
to FDE1		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
FIH1	A → Yn	(HH)	0.324	0.421	0.552	0.001	0.002	0.004			
to FDH1		(LL)	0.217	0.332	0.463	0.001	0.002	0.003			
	(n = 1 to 8)										

INTERFACE BLOCK (3.3V)

Function	INPUT BUFFER WITH EN(OR)					3.3V
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FN13	FN23			1	4
Schmitt						
Clock						

Logic Diagram

"Normal"



Truth Table

A	EN	Y
0	0	0
0	1	1
1	0	1
1	1	1

"Schmitt"

Block type	Input		Output	
	Symbol	Fan-In	Symbol	Fan-Out
FN13 to FN23	A	-	Y	33
	EN	2.1		

"Clock"

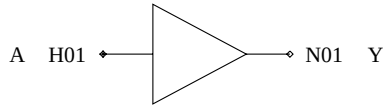
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN13 to FN23	A → Y	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
	EN → Y	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			

INTERFACE BLOCK (3.3V)

Function	OUTPUT BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	FO09				1	4
6mA	FO04				1	4
9mA	FO01				1	4
12mA	FO02				1	4
18mA	FO03				1	8
24mA	FO06				1	8

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FO09	A	8.1	Y	-
FO04	A	8.1	Y	-
FO01	A	8.1	Y	-
FO02	A	8.1	Y	-
FO03	A	16.3	Y	-
FO06	A	16.3	Y	-

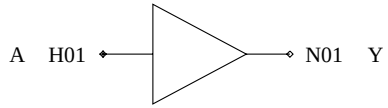
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FO09	A → Y	(HH)	0.698	1.195	2.080				0.057	0.101	0.186
		(LL)	0.717	1.166	1.960				0.073	0.102	0.159
FO04	A → Y	(HH)	0.644	1.128	1.932				0.029	0.051	0.094
		(LL)	0.580	1.017	1.775				0.037	0.051	0.081
FO01	A → Y	(HH)	0.670	1.197	2.075				0.020	0.035	0.064
		(LL)	0.574	1.053	1.894				0.025	0.035	0.055
FO02	A → Y	(HH)	0.713	1.299	2.288				0.016	0.027	0.049
		(LL)	0.594	1.124	2.078				0.019	0.028	0.043
FO03	A → Y	(HH)	0.633	1.211	2.199				0.011	0.020	0.035
		(LL)	0.521	1.054	2.016				0.013	0.019	0.030
FO06	A → Y	(HH)	0.728	1.410	2.594				0.009	0.017	0.030
		(LL)	0.613	1.274	2.463				0.010	0.016	0.025

INTERFACE BLOCK (3.3V)

Function	LOW-NOISE OUTPUT BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	FE04				1	4
9mA	FE01				1	4
12mA	FE02				1	4
18mA	FE03				1	4
24mA	FE06				1	4

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FE04	A	6.1	Y	-
FE01	A	6.1	Y	-
FE02	A	6.1	Y	-
FE03	A	6.1	Y	-
FE06	A	6.1	Y	-

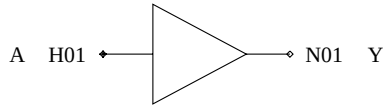
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FE04	A → Y	(HH)	1.472	2.780	5.000				0.033	0.057	0.102
		(LL)	1.439	2.828	5.019				0.039	0.058	0.091
FE01	A → Y	(HH)	1.534	2.959	5.465				0.026	0.045	0.077
		(LL)	1.445	2.905	5.276				0.029	0.044	0.070
FE02	A → Y	(HH)	1.627	3.193	5.974				0.022	0.039	0.068
		(LL)	1.468	3.013	5.560				0.025	0.038	0.061
FE03	A → Y	(HH)	1.828	3.657	6.931				0.020	0.036	0.062
		(LL)	1.575	3.296	6.220				0.020	0.034	0.056
FE06	A → Y	(HH)	2.085	4.232	8.116				0.019	0.034	0.058
		(LL)	1.765	3.750	7.140				0.018	0.031	0.051

INTERFACE BLOCK (3.3V)

Function	HIGH SPEED OUTPUT BUFFER				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	FO29				1	4
6mA	FO24				1	4
9mA	FO21				1	4
12mA	FO22				1	4
18mA	FO23				1	8
24mA	FO26				1	8

Logic Diagram



Truth Table

A	Y
0	0
1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FO29	A	7.0	Y	-
FO24	A	7.0	Y	-
FO21	A	7.0	Y	-
FO22	A	7.0	Y	-
FO23	A	15.1	Y	-
FO26	A	15.1	Y	-

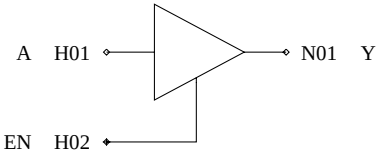
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FO29	A → Y	(HH)	0.472	0.818	1.444				0.057	0.100	0.185
		(LL)	0.595	0.900	1.440				0.072	0.101	0.159
FO24	A → Y	(HH)	0.476	0.788	1.324				0.029	0.051	0.094
		(LL)	0.570	0.963	1.596				0.036	0.051	0.080
FO21	A → Y	(HH)	0.463	0.774	1.300				0.019	0.034	0.063
		(LL)	0.549	0.959	1.609				0.024	0.035	0.054
FO22	A → Y	(HH)	0.475	0.800	1.358				0.015	0.026	0.047
		(LL)	0.561	0.999	1.699				0.019	0.027	0.042
FO23	A → Y	(HH)	0.347	0.616	1.061				0.010	0.017	0.032
		(LL)	0.409	0.721	1.239				0.012	0.018	0.028
FO26	A → Y	(HH)	0.387	0.701	1.228				0.008	0.014	0.024
		(LL)	0.455	0.810	1.416				0.010	0.014	0.023

INTERFACE BLOCK (3.3V)

Function	3-STATE OUTPUT BUFFER					3.3V
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	B00T	B0DT	B0UT	B0WT	1	6
6mA	B00E	B0DE	B0UE	B0WE	1	6
9mA	B008	B0D8	B0U8	B0W8	1	6
12mA	B007	B0D7	B0U7	B0W7	1	6
18mA	B009	B0D9	B0U9	B0W9	1	10
24mA	B00H	B0DH	B0UH	B0WH	1	10

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
B00T to B0WT	A	7.1	Y	-
	EN	3.2		
B00E to B0WE	A	7.1	Y	-
	EN	3.2		
B008 to B0W8	A	7.1	Y	-
	EN	3.2		
B007 to B0W7	A	7.1	Y	-
	EN	3.2		
B009 to B0W9	A	13.3	Y	-
	EN	3.3		
B00H to B0WH	A	13.3	Y	-
	EN	3.3		

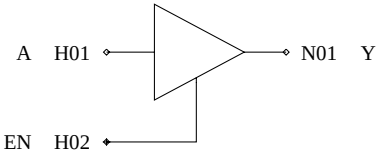
INTERFACE BLOCK(3.3V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B00T to B0WT	A → Y	(HH)	1.030	1.787	3.038				0.057	0.101	0.186
		(LL)	0.959	1.676	2.922				0.073	0.102	0.160
	EN → Y	(HZ)	0.718	1.187	1.779						
		(LZ)	0.454	0.718	1.119						
		(ZH)	0.946	1.614	2.716				0.057	0.101	0.186
		(ZL)	0.913	1.533	2.637				0.073	0.102	0.160
B00E to B0WE	A → Y	(HH)	1.023	1.829	3.121				0.030	0.053	0.095
		(LL)	0.834	1.552	2.809				0.037	0.053	0.083
	EN → Y	(HZ)	0.996	1.831	2.867						
		(LZ)	0.522	0.863	1.378						
		(ZH)	0.917	1.620	2.734				0.030	0.053	0.095
		(ZL)	0.752	1.347	2.405				0.037	0.053	0.083
B008 to B0W8	A → Y	(HH)	1.057	1.947	3.399				0.022	0.038	0.067
		(LL)	0.824	1.598	2.979				0.026	0.038	0.059
	EN → Y	(HZ)	1.212	2.319	3.699						
		(LZ)	0.595	1.004	1.610						
		(ZH)	0.933	1.705	2.943				0.022	0.038	0.067
		(ZL)	0.718	1.338	2.467				0.026	0.037	0.059
B007 to B0W7	A → Y	(HH)	1.111	2.100	3.719				0.019	0.032	0.055
		(LL)	0.841	1.672	3.201				0.021	0.031	0.049
	EN → Y	(HZ)	1.462	2.841	4.553						
		(LZ)	0.667	1.139	1.836						
		(ZH)	0.973	1.817	3.201				0.019	0.032	0.055
		(ZL)	0.705	1.353	2.568				0.021	0.031	0.048
B009 to B0W9	A → Y	(HH)	1.025	1.984	3.561				0.015	0.025	0.043
		(LL)	0.779	1.632	3.255				0.016	0.024	0.038
	EN → Y	(HZ)	2.005	3.976	6.418						
		(LZ)	0.849	1.471	2.369						
		(ZH)	1.000	1.894	3.351				0.015	0.025	0.043
		(ZL)	0.701	1.401	2.737				0.016	0.024	0.038
B00H to B0WH	A → Y	(HH)	1.164	2.292	4.143				0.013	0.023	0.039
		(LL)	0.883	1.903	3.850				0.013	0.021	0.032
	EN → Y	(HZ)	2.474	5.043	8.173						
		(LZ)	1.002	1.765	2.848						
		(ZH)	1.128	2.178	3.889				0.013	0.023	0.039
		(ZL)	0.752	1.540	3.109				0.013	0.021	0.034

INTERFACE BLOCK (3.3V)

Function	LOW-NOISE 3-STATE OUTPUT BUFFER				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	BE0E	BEDE	BEUE	BEWE	1	6
9mA	BE08	BED8	BEU8	BEW8	1	6
12mA	BE07	BED7	BEU7	BEW7	1	6
18mA	BE09	BED9	BEU9	BEW9	1	6
24mA	BE0H	BEDH	BEUH	BEWH	1	6

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BE0E to BEWE	A	6.1	Y	-
	EN	3.2		
BE08 to BEW8	A	6.1	Y	-
	EN	3.2		
BE07 to BEW7	A	6.1	Y	-
	EN	3.2		
BE09 to BEW9	A	6.1	Y	-
	EN	3.2		
BE0H to BEWH	A	6.1	Y	-
	EN	3.2		

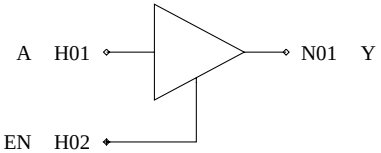
INTERFACE BLOCK(3.3V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0E to BEWE	A → Y	(HH)	1.484	2.804	5.056				0.033	0.057	0.102
		(LL)	1.446	2.847	5.070				0.039	0.058	0.091
	EN → Y	(HZ)	0.965	1.786	2.815						
		(LZ)	0.724	1.144	1.770						
		(ZH)	1.432	2.775	5.046				0.033	0.057	0.102
		(ZL)	1.480	2.940	5.224				0.039	0.058	0.091
BE08 to BEW8	A → Y	(HH)	1.543	2.980	5.502				0.026	0.045	0.077
		(LL)	1.447	2.918	5.314				0.029	0.045	0.070
	EN → Y	(HZ)	1.189	2.288	3.646						
		(LZ)	0.838	1.345	2.109						
		(ZH)	1.492	2.957	5.508				0.026	0.045	0.077
		(ZL)	1.484	3.011	5.492				0.029	0.044	0.070
BE07 to BEW7	A → Y	(HH)	1.636	3.208	6.011				0.022	0.039	0.068
		(LL)	1.470	3.024	5.605				0.025	0.039	0.061
	EN → Y	(HZ)	1.431	2.802	4.512						
		(LZ)	0.945	1.537	2.431						
		(ZH)	1.583	3.187	6.011				0.022	0.039	0.068
		(ZL)	1.506	3.118	5.756				0.025	0.039	0.061
BE09 to BEW9	A → Y	(HH)	1.836	3.669	6.952				0.020	0.036	0.062
		(LL)	1.563	3.287	6.262				0.021	0.035	0.055
	EN → Y	(HZ)	1.916	3.850	6.255						
		(LZ)	1.179	1.958	3.113						
		(ZH)	1.784	3.646	6.987				0.020	0.036	0.061
		(ZL)	1.605	3.377	6.409				0.021	0.034	0.055
BE0H to BEWH	A → Y	(HH)	2.090	4.257	8.132				0.019	0.033	0.060
		(LL)	1.772	3.750	7.178				0.018	0.031	0.051
	EN → Y	(HZ)	2.396	4.909	8.009						
		(LZ)	1.412	2.383	3.805						
		(ZH)	2.041	4.239	8.119				0.019	0.033	0.058
		(ZL)	1.783	3.822	7.275				0.019	0.031	0.051

INTERFACE BLOCK (3.3V)

Function	HIGH SPEED 3-STATE OUTPUT BUFFER				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	B02T	B03T	B04T	B05T	1	12
6mA	B02E	B03E	B04E	B05E	1	12
9mA	B028	B038	B048	B058	1	12
12mA	B027	B037	B047	B057	1	12
18mA	B029	B039	B049	B059	1	16
24mA	B02H	B03H	B04H	B05H	1	16

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
B02T to B05T	A	16.1	Y	-
	EN	1.0		
B02E to B05E	A	16.1	Y	-
	EN	1.0		
B028 to B058	A	16.1	Y	-
	EN	1.0		
B027 to B057	A	16.1	Y	-
	EN	1.0		
B029 to B059	A	32.3	Y	-
	EN	2.0		
B02H to B05H	A	32.3	Y	-
	EN	2.0		

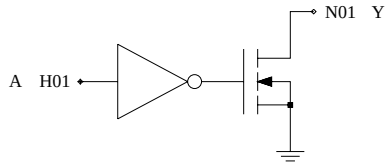
INTERFACE BLOCK(3.3V)

Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			T			
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B02T to B05T	A → Y	(HH)	0.466	0.840	1.522				0.057	0.101	0.186
		(LL)	0.597	0.960	1.561				0.072	0.101	0.159
	EN → Y	(HZ)	0.592	1.072	1.804						
		(LZ)	0.357	0.642	1.102						
		(ZH)	0.860	1.534	2.705				0.057	0.101	0.186
		(ZL)	0.800	1.239	2.003				0.072	0.102	0.159
B02E to B05E	A → Y	(HH)	0.440	0.785	1.374				0.029	0.051	0.094
		(LL)	0.538	0.969	1.626				0.036	0.051	0.080
	EN → Y	(HZ)	0.808	1.440	2.392						
		(LZ)	0.455	0.811	1.396						
		(ZH)	0.840	1.495	2.580				0.029	0.051	0.093
		(ZL)	0.749	1.262	2.087				0.036	0.051	0.080
B028 to B058	A → Y	(HH)	0.428	0.767	1.347				0.019	0.034	0.062
		(LL)	0.495	0.919	1.571				0.024	0.035	0.054
	EN → Y	(HZ)	0.881	1.579	2.613						
		(LZ)	0.478	0.851	1.468						
		(ZH)	0.824	1.475	2.541				0.019	0.034	0.063
		(ZL)	0.703	1.213	2.034				0.025	0.035	0.054
B027 to B057	A → Y	(HH)	0.438	0.793	1.396				0.015	0.026	0.047
		(LL)	0.485	0.918	1.580				0.019	0.027	0.042
	EN → Y	(HZ)	0.964	1.722	2.844						
		(LZ)	0.498	0.890	1.534						
		(ZH)	0.830	1.497	2.585				0.015	0.026	0.047
		(ZL)	0.688	1.208	2.045				0.019	0.027	0.042
B029 to B059	A → Y	(HH)	0.379	0.674	1.156				0.010	0.018	0.032
		(LL)	0.361	0.645	1.133				0.012	0.018	0.028
	EN → Y	(HZ)	0.970	1.766	2.926						
		(LZ)	0.468	0.843	1.459						
		(ZH)	0.788	1.414	2.432				0.010	0.018	0.032
		(ZL)	0.575	1.014	1.730				0.013	0.018	0.028
B02H to B05H	A → Y	(HH)	0.417	0.753	1.311				0.008	0.014	0.025
		(LL)	0.391	0.706	1.263				0.010	0.014	0.022
	EN → Y	(HZ)	1.071	1.944	3.224						
		(LZ)	0.499	0.902	1.557						
		(ZH)	0.821	1.487	2.581				0.008	0.014	0.025
		(ZL)	0.599	1.067	1.840				0.010	0.014	0.022

INTERFACE BLOCK (3.3V)

Function	N-CH OPEN DRAIN OUTPUT BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	EXTH		EXUH	EXWH	1	4
6mA	EXTJ		EXUJ	EXWJ	1	4
9mA	EXT1		EXT3	EXW3	1	4
12mA	EXT9		EXTB	EXWB	1	4
18mA	EXT5		EXT7	EXW7	1	8
24mA	EXTD		EXTF	EXWF	1	8

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
EXTH to EXWH	A	8.1	Y	-
EXTJ to EXWJ	A	8.1	Y	-
EXT1 to EXW3	A	8.1	Y	-
EXT9 to EXWB	A	8.1	Y	-
EXT5 to EXW7	A	16.3	Y	-
EXTD to EXWF	A	16.3	Y	-

Truth Table

A	Y
1	Z
0	0

Z:High Impedance

Connect a pull-up resistor to get a high level

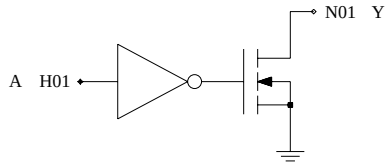
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EXTH	A → Y	(LZ)	0.270	0.390	0.562						
to EXWH		(ZL)	0.608	0.977	1.616				0.072	0.101	0.159
EXTJ	A → Y	(LZ)	0.317	0.508	0.786						
to EXWJ		(ZL)	0.439	0.769	1.324				0.036	0.051	0.080
EXT1	A → Y	(LZ)	0.367	0.618	0.970						
to EXW3		(ZL)	0.405	0.752	1.347				0.024	0.035	0.054
EXT9	A → Y	(LZ)	0.419	0.724	1.145						
to EXWB		(ZL)	0.401	0.774	1.420				0.019	0.027	0.042
EXT5	A → Y	(LZ)	0.403	0.776	1.272						
to EXW7		(ZL)	0.363	0.743	1.416				0.013	0.020	0.031
EXTD	A → Y	(LZ)	0.486	0.961	1.575						
to EXWF		(ZL)	0.391	0.821	1.601				0.011	0.017	0.027

INTERFACE BLOCK (3.3V)

Function	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	EETJ		EEUJ	EEWJ	1	2
9mA	EET1		EET3	EEW3	1	2
12mA	EET9		EETB	EEWB	1	2
18mA	EET5		EET7	EEW7	1	2
24mA	EETD		EETF	EEWF	1	2

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
EETJ to EEWJ	A	3.0	Y	-
EET1 to EEW3	A	3.0	Y	-
EET9 to EEWB	A	3.0	Y	-
EET5 to EEW7	A	3.0	Y	-
EETD to EEWF	A	3.0	Y	-

Truth Table

A	Y
1	Z
0	0

Z:High Impedance

Connect a pull-up resistor to get a high level

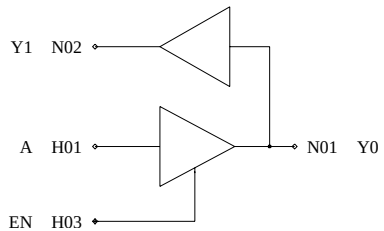
INTERFACE BLOCK(3.3V)

Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			T			
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
EETJ	A → Y	(LZ)	1.332	2.141	3.245							
to EEWJ		(ZL)	1.417	2.795	4.961				0.039	0.057	0.091	
EET1	A → Y	(LZ)	1.568	2.561	3.926							
to EEW3		(ZL)	1.426	2.878	5.201				0.029	0.044	0.071	
EET9	A → Y	(LZ)	1.794	2.963	4.588							
to EEWB		(ZL)	1.451	2.981	5.505				0.025	0.038	0.061	
EET5	A → Y	(LZ)	2.270	3.808	5.961							
to EEW7		(ZL)	1.554	3.274	6.161				0.021	0.034	0.054	
EETD	A → Y	(LZ)	2.738	4.627	7.302							
to EEWF		(ZL)	1.698	3.604	6.848				0.019	0.032	0.052	

INTERFACE BLOCK (3.3V)

Function	I/O BUFFER					3.3V
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	B00U	B0DU	B0UU	B0WU	1	10
6mA	B00C	B0DC	B0UC	B0WC	1	10
9mA	B003	B0D3	B0U3	B0W3	1	10
12mA	B001	B0D1	B0U1	B0W1	1	10
18mA	B005	B0D5	B0U5	B0W5	1	14
24mA	B00F	B0DF	B0UF	B0WF	1	14

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
B00U to B0WU	A	7.1	Y1	34
	EN	3.2		
B00C to B0WC	A	7.1	Y1	34
	EN	3.2		
B003 to B0W3	A	7.1	Y1	34
	EN	3.2		
B001 to B0W1	A	7.1	Y1	34
	EN	3.2		
B005 to B0W5	A	13.3	Y1	34
	EN	3.3		
B00F to B0WF	A	13.3	Y1	34
	EN	3.3		

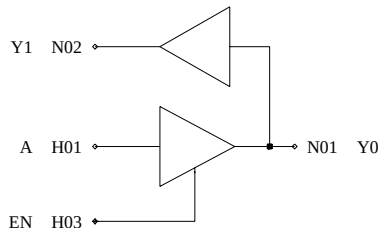
INTERFACE BLOCK(3.3V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B00U to B0WU	A → Y0	(HH)	1.030	1.787	3.038				0.057	0.101	0.186
		(LL)	0.959	1.676	2.922				0.073	0.102	0.160
	EN → Y0	(HZ)	0.718	1.187	1.779						
		(LZ)	0.454	0.718	1.119						
		(ZH)	0.946	1.614	2.716				0.057	0.101	0.186
		(ZL)	0.913	1.533	2.637				0.073	0.102	0.160
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B00C to B0WC	A → Y0	(HH)	1.023	1.829	3.121				0.030	0.053	0.095
		(LL)	0.834	1.552	2.809				0.037	0.053	0.083
	EN → Y0	(HZ)	0.996	1.831	2.867						
		(LZ)	0.522	0.863	1.378						
		(ZH)	0.917	1.620	2.734				0.030	0.053	0.095
		(ZL)	0.752	1.347	2.405				0.037	0.053	0.083
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B003 to B0W3	A → Y0	(HH)	1.057	1.947	3.399				0.022	0.038	0.067
		(LL)	0.824	1.598	2.979				0.026	0.038	0.059
	EN → Y0	(HZ)	1.212	2.319	3.699						
		(LZ)	0.595	1.004	1.610						
		(ZH)	0.933	1.705	2.943				0.022	0.038	0.067
		(ZL)	0.718	1.338	2.467				0.026	0.037	0.059
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B001 to B0W1	A → Y0	(HH)	1.111	2.100	3.719				0.019	0.032	0.055
		(LL)	0.841	1.672	3.201				0.021	0.031	0.049
	EN → Y0	(HZ)	1.462	2.841	4.553						
		(LZ)	0.667	1.139	1.836						
		(ZH)	0.973	1.817	3.201				0.019	0.032	0.055
		(ZL)	0.705	1.353	2.568				0.021	0.031	0.048
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B005 to B0W5	A → Y0	(HH)	1.025	1.984	3.561				0.015	0.025	0.043
		(LL)	0.779	1.632	3.255				0.016	0.024	0.038
	EN → Y0	(HZ)	2.005	3.976	6.418						
		(LZ)	0.849	1.471	2.369						
		(ZH)	1.000	1.894	3.351				0.015	0.025	0.043
		(ZL)	0.701	1.401	2.737				0.016	0.024	0.038
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B00F to B0WF	A → Y0	(HH)	1.164	2.292	4.143				0.013	0.023	0.039
		(LL)	0.883	1.903	3.850				0.013	0.021	0.032
	EN → Y0	(HZ)	2.474	5.043	8.173						
		(LZ)	1.002	1.765	2.848						
		(ZH)	1.128	2.178	3.889				0.013	0.023	0.039
		(ZL)	0.752	1.540	3.109				0.013	0.021	0.034
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (3.3V)

Function	LOW-NOISE I/O BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	BE0C	BEDC	BEUC	BEWC	1	10
9mA	BE03	BED3	BEU3	BEW3	1	10
12mA	BE01	BED1	BEU1	BEW1	1	10
18mA	BE05	BED5	BEU5	BEW5	1	10
24mA	BE0F	BEDF	BEUF	BEWF	1	10

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BE0C to BEWC	A	6.1	Y1	34
	EN	3.2		
BE03 to BEW3	A	6.1	Y1	34
	EN	3.2		
BE01 to BEW1	A	6.1	Y1	34
	EN	3.2		
BE05 to BEW5	A	6.1	Y1	34
	EN	3.2		
BE0F to BEWF	A	6.1	Y1	34
	EN	3.2		

Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

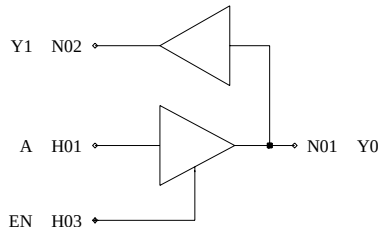
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BE0C	A → Y0	(HH)	1.484	2.804	5.056				0.033	0.057	0.102
to BEWC		(LL)	1.446	2.847	5.070				0.039	0.058	0.091
	EN → Y0	(HZ)	0.965	1.786	2.815						
		(LZ)	0.724	1.144	1.770						
		(ZH)	1.432	2.775	5.046				0.033	0.057	0.102
		(ZL)	1.480	2.940	5.224				0.039	0.058	0.091
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BE03	A → Y0	(HH)	1.543	2.980	5.502				0.026	0.045	0.077
to BEW3		(LL)	1.447	2.918	5.314				0.029	0.045	0.070
	EN → Y0	(HZ)	1.189	2.288	3.646						
		(LZ)	0.838	1.345	2.109						
		(ZH)	1.492	2.957	5.508				0.026	0.045	0.077
		(ZL)	1.484	3.011	5.492				0.029	0.044	0.070
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BE01	A → Y0	(HH)	1.636	3.208	6.011				0.022	0.039	0.068
to BEW1		(LL)	1.470	3.024	5.605				0.025	0.039	0.061
	EN → Y0	(HZ)	1.431	2.802	4.512						
		(LZ)	0.945	1.537	2.431						
		(ZH)	1.583	3.187	6.011				0.022	0.039	0.068
		(ZL)	1.506	3.118	5.756				0.025	0.039	0.061
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BE05	A → Y0	(HH)	1.836	3.669	6.952				0.020	0.036	0.062
to BEW5		(LL)	1.563	3.287	6.262				0.021	0.035	0.055
	EN → Y0	(HZ)	1.916	3.850	6.255						
		(LZ)	1.179	1.958	3.113						
		(ZH)	1.784	3.646	6.987				0.020	0.036	0.061
		(ZL)	1.605	3.377	6.409				0.021	0.034	0.055
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BE0F	A → Y0	(HH)	2.090	4.257	8.132				0.019	0.033	0.060
to BEWF		(LL)	1.772	3.750	7.178				0.018	0.031	0.051
	EN → Y0	(HZ)	2.396	4.909	8.009						
		(LZ)	1.412	2.383	3.805						
		(ZH)	2.041	4.239	8.119				0.019	0.033	0.058
		(ZL)	1.783	3.822	7.275				0.019	0.031	0.051
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (3.3V)

Function	HIGH SPEED I/O BUFFER				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	B02U	B03U	B04U	B05U	1	16
6mA	B02C	B03C	B04C	B05C	1	16
9mA	B023	B033	B043	B053	1	16
12mA	B021	B031	B041	B051	1	16
18mA	B025	B035	B045	B055	1	20
24mA	B02F	B03F	B04F	B05F	1	20

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
B02U to B05U	A	16.1	Y1	34
	EN	1.0		
B02C to B05C	A	16.1	Y1	34
	EN	1.0		
B023 to B053	A	16.1	Y1	34
	EN	1.0		
B021 to B051	A	16.1	Y1	34
	EN	1.0		
B025 to B055	A	32.3	Y1	34
	EN	2.0		
B02F to B05F	A	32.3	Y1	34
	EN	2.0		

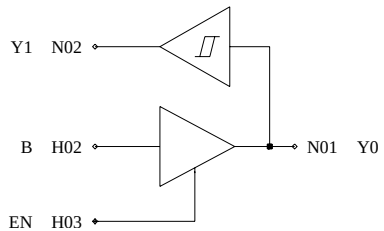
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
B02U to B05U	A → Y0	(HH)	0.466	0.840	1.522				0.057	0.101	0.186
		(LL)	0.597	0.960	1.561				0.072	0.101	0.159
	EN → Y0	(HZ)	0.592	1.072	1.804						
		(LZ)	0.357	0.642	1.102						
		(ZH)	0.860	1.534	2.705				0.057	0.101	0.186
		(ZL)	0.800	1.239	2.003				0.072	0.102	0.159
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B02C to B05C	A → Y0	(HH)	0.440	0.785	1.374				0.029	0.051	0.094
		(LL)	0.538	0.969	1.626				0.036	0.051	0.080
	EN → Y0	(HZ)	0.808	1.440	2.392						
		(LZ)	0.455	0.811	1.396						
		(ZH)	0.840	1.495	2.580				0.029	0.051	0.093
		(ZL)	0.749	1.262	2.087				0.036	0.051	0.080
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B023 to B053	A → Y0	(HH)	0.428	0.767	1.347				0.019	0.034	0.062
		(LL)	0.495	0.919	1.571				0.024	0.035	0.054
	EN → Y0	(HZ)	0.881	1.579	2.613						
		(LZ)	0.478	0.851	1.468						
		(ZH)	0.824	1.475	2.541				0.019	0.034	0.063
		(ZL)	0.703	1.213	2.034				0.025	0.035	0.054
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B021 to B051	A → Y0	(HH)	0.438	0.793	1.396				0.015	0.026	0.047
		(LL)	0.485	0.918	1.580				0.019	0.027	0.042
	EN → Y0	(HZ)	0.964	1.722	2.844						
		(LZ)	0.498	0.890	1.534						
		(ZH)	0.830	1.497	2.585				0.015	0.026	0.047
		(ZL)	0.688	1.208	2.045				0.019	0.027	0.042
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B025 to B055	A → Y0	(HH)	0.379	0.674	1.156				0.010	0.018	0.032
		(LL)	0.361	0.645	1.133				0.012	0.018	0.028
	EN → Y0	(HZ)	0.970	1.766	2.926						
		(LZ)	0.468	0.843	1.459						
		(ZH)	0.788	1.414	2.432				0.010	0.018	0.032
		(ZL)	0.575	1.014	1.730				0.013	0.018	0.028
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
B02F to B05F	A → Y0	(HH)	0.417	0.753	1.311				0.008	0.014	0.025
		(LL)	0.391	0.706	1.263				0.010	0.014	0.022
	EN → Y0	(HZ)	1.071	1.944	3.224						
		(LZ)	0.499	0.902	1.557						
		(ZH)	0.821	1.487	2.581				0.008	0.014	0.025
		(ZL)	0.599	1.067	1.840				0.010	0.014	0.022
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (3.3V)

Function	SCHMITT I/O BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BSIU	BSDU	BSUU	BSWU	1	14
6mA	BSIC	BSDC	BSUC	BSWC	1	14
9mA	BSI3	BSD3	BSU3	BSW3	1	14
12mA	BSI1	BSD1	BSU1	BSW1	1	14
18mA	BSI5	BSD5	BSU5	BSW5	1	18
24mA	BSIF	BSDF	BSUF	BSWF	1	18

Logic Diagram



Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BSIU to BSWU	B	7.1	Y1	22
	EN	3.2		
BSIC to BSWC	B	7.1	Y1	22
	EN	3.2		
BSI3 to BSW3	B	7.1	Y1	22
	EN	3.2		
BSI1 to BSW1	B	7.1	Y1	22
	EN	3.2		
BSI5 to BSW5	B	13.3	Y1	22
	EN	3.3		
BSIF to BSWF	B	13.3	Y1	22
	EN	3.3		

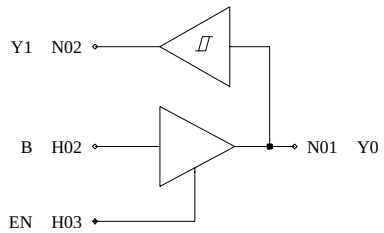
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BSIU to BSWU	B → Y0	(HH)	1.030	1.787	3.038				0.057	0.101	0.186
		(LL)	0.959	1.676	2.922				0.073	0.102	0.160
	EN → Y0	(HZ)	0.718	1.187	1.779						
		(LZ)	0.454	0.718	1.119						
		(ZH)	0.946	1.614	2.716				0.057	0.101	0.186
		(ZL)	0.913	1.533	2.637				0.073	0.102	0.160
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BSIC to BSWC	B → Y0	(HH)	1.023	1.829	3.121				0.030	0.053	0.095
		(LL)	0.834	1.552	2.809				0.037	0.053	0.083
	EN → Y0	(HZ)	0.996	1.831	2.867						
		(LZ)	0.522	0.863	1.378						
		(ZH)	0.917	1.620	2.734				0.030	0.053	0.095
		(ZL)	0.752	1.347	2.405				0.037	0.053	0.083
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BSI3 to BSW3	B → Y0	(HH)	1.057	1.947	3.399				0.022	0.038	0.067
		(LL)	0.824	1.598	2.979				0.026	0.038	0.059
	EN → Y0	(HZ)	1.212	2.319	3.699						
		(LZ)	0.595	1.004	1.610						
		(ZH)	0.933	1.705	2.943				0.022	0.038	0.067
		(ZL)	0.718	1.338	2.467				0.026	0.037	0.059
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BSI1 to BSW1	B → Y0	(HH)	1.111	2.100	3.719				0.019	0.032	0.055
		(LL)	0.841	1.672	3.201				0.021	0.031	0.049
	EN → Y0	(HZ)	1.462	2.841	4.553						
		(LZ)	0.667	1.139	1.836						
		(ZH)	0.973	1.817	3.201				0.019	0.032	0.055
		(ZL)	0.705	1.353	2.568				0.021	0.031	0.048
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BSI5 to BSW5	B → Y0	(HH)	1.025	1.984	3.561				0.015	0.025	0.043
		(LL)	0.779	1.632	3.255				0.016	0.024	0.038
	EN → Y0	(HZ)	2.005	3.976	6.418						
		(LZ)	0.849	1.471	2.369						
		(ZH)	1.000	1.894	3.351				0.015	0.025	0.043
		(ZL)	0.701	1.401	2.737				0.016	0.024	0.038
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BSIF to BSWF	B → Y0	(HH)	1.164	2.292	4.143				0.013	0.023	0.039
		(LL)	0.883	1.903	3.850				0.013	0.021	0.032
	EN → Y0	(HZ)	2.474	5.043	8.173						
		(LZ)	1.002	1.765	2.848						
		(ZH)	1.128	2.178	3.889				0.013	0.023	0.039
		(ZL)	0.752	1.540	3.109				0.013	0.021	0.034
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (3.3V)

Function	LOW-NOISE SCHMITT I/O BUFFER				3.3V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	BFIC	BFDC	BFUC	BFWC	1	14
9mA	BFI3	BFD3	BFU3	BFW3	1	14
12mA	BFI1	BFD1	BFU1	BFW1	1	14
18mA	BFI5	BFD5	BFU5	BFW5	1	14
24mA	BFIF	BFDF	BFUF	BFWF	1	14

Logic Diagram



Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BFIC to BFWC	B	6.1	Y1	22
	EN	3.2		
BFI3 to BFW3	B	6.1	Y1	22
	EN	3.2		
BFI1 to BFW1	B	6.1	Y1	22
	EN	3.2		
BFI5 to BFW5	B	6.1	Y1	22
	EN	3.2		
BFIF to BFWF	B	6.1	Y1	22
	EN	3.2		

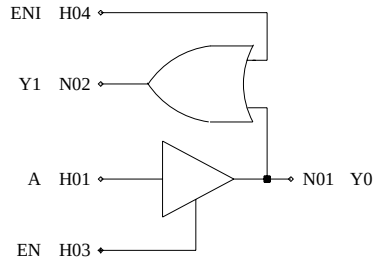
INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BFIC to BFWC	B → Y0	(HH)	1.484	2.804	5.056				0.033	0.057	0.102
		(LL)	1.446	2.847	5.070				0.039	0.058	0.091
	EN → Y0	(HZ)	0.965	1.786	2.815						
		(LZ)	0.724	1.144	1.770						
		(ZH)	1.432	2.775	5.046				0.033	0.057	0.102
		(ZL)	1.480	2.940	5.224				0.039	0.058	0.091
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BFI3 to BFW3	B → Y0	(HH)	1.543	2.980	5.502				0.026	0.045	0.077
		(LL)	1.447	2.918	5.314				0.029	0.045	0.070
	EN → Y0	(HZ)	1.189	2.288	3.646						
		(LZ)	0.838	1.345	2.109						
		(ZH)	1.492	2.957	5.508				0.026	0.045	0.077
		(ZL)	1.484	3.011	5.492				0.029	0.044	0.070
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BFI1 to BFW1	B → Y0	(HH)	1.636	3.208	6.011				0.022	0.039	0.068
		(LL)	1.470	3.024	5.605				0.025	0.039	0.061
	EN → Y0	(HZ)	1.431	2.802	4.512						
		(LZ)	0.945	1.537	2.431						
		(ZH)	1.583	3.187	6.011				0.022	0.039	0.068
		(ZL)	1.506	3.118	5.756				0.025	0.039	0.061
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BFI5 to BFW5	B → Y0	(HH)	1.836	3.669	6.952				0.020	0.036	0.062
		(LL)	1.563	3.287	6.262				0.021	0.035	0.055
	EN → Y0	(HZ)	1.916	3.850	6.255						
		(LZ)	1.179	1.958	3.113						
		(ZH)	1.784	3.646	6.987				0.020	0.036	0.061
		(ZL)	1.605	3.377	6.409				0.021	0.034	0.055
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BFIF to BFWF	B → Y0	(HH)	2.090	4.257	8.132				0.019	0.033	0.060
		(LL)	1.772	3.750	7.178				0.018	0.031	0.051
	EN → Y0	(HZ)	2.396	4.909	8.009						
		(LZ)	1.412	2.383	3.805						
		(ZH)	2.041	4.239	8.119				0.019	0.033	0.058
		(ZL)	1.783	3.822	7.275				0.019	0.031	0.051
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (3.3V)

Function	I/O BUFFER WITH EN(OR)				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BN3U33	BN5U33			1	16
6mA	BN3C33	BN5C33			1	16
9mA	BN3333	BN5333			1	16
12mA	BN3133	BN5133			1	16
18mA	BN3533	BN5533			1	20
24mA	BN3F33	BN5F33			1	20

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Y0	ENI	Y1
0	0	0
1	0	1
0	1	1
1	1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BN3U33 to BN5U33	A	16.1	Y1	33
	EN	1.0		
	ENI	2.1		
BN3C33 to BN5C33	A	16.1	Y1	33
	EN	1.0		
	ENI	2.1		
BN3333 to BN5333	A	16.1	Y1	33
	EN	1.0		
	ENI	2.1		
BN3133 to BN5133	A	16.1	Y1	33
	EN	1.0		
	ENI	2.1		
BN3533 to BN5533	A	32.3	Y1	33
	EN	2.0		
	ENI	2.1		
BN3F33 to BN5F33	A	32.3	Y1	33
	EN	2.0		
	ENI	2.1		

INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN3U33 to BN5U33	A → Y0	(HH)	0.466	0.840	1.522				0.057	0.101	0.186
		(LL)	0.597	0.960	1.561				0.072	0.101	0.159
	EN → Y0	(HZ)	0.592	1.072	1.804						
		(LZ)	0.357	0.642	1.102						
		(ZH)	0.860	1.534	2.705				0.057	0.101	0.186
		(ZL)	0.800	1.239	2.003				0.072	0.102	0.159
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN3C33 to BN5C33	A → Y0	(HH)	0.440	0.785	1.374				0.029	0.051	0.094
		(LL)	0.538	0.969	1.626				0.036	0.051	0.080
	EN → Y0	(HZ)	0.808	1.440	2.392						
		(LZ)	0.455	0.811	1.396						
		(ZH)	0.840	1.495	2.580				0.029	0.051	0.093
		(ZL)	0.749	1.262	2.087				0.036	0.051	0.080
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN3333 to BN5333	A → Y0	(HH)	0.428	0.767	1.347				0.019	0.034	0.062
		(LL)	0.495	0.919	1.571				0.024	0.035	0.054
	EN → Y0	(HZ)	0.881	1.579	2.613						
		(LZ)	0.478	0.851	1.468						
		(ZH)	0.824	1.475	2.541				0.019	0.034	0.063
		(ZL)	0.703	1.213	2.034				0.025	0.035	0.054
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN3133 to BN5133	A → Y0	(HH)	0.438	0.793	1.396				0.015	0.026	0.047
		(LL)	0.485	0.918	1.580				0.019	0.027	0.042
	EN → Y0	(HZ)	0.964	1.722	2.844						
		(LZ)	0.498	0.890	1.534						
		(ZH)	0.830	1.497	2.585				0.015	0.026	0.047
		(ZL)	0.688	1.208	2.045				0.019	0.027	0.042
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN3533 to BN5533	A → Y0	(HH)	0.379	0.674	1.156				0.010	0.018	0.032
		(LL)	0.361	0.645	1.133				0.012	0.018	0.028
	EN → Y0	(HZ)	0.970	1.766	2.926						
		(LZ)	0.468	0.843	1.459						
		(ZH)	0.788	1.414	2.432				0.010	0.018	0.032
		(ZL)	0.575	1.014	1.730				0.013	0.018	0.028
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN3F33 to BN5F33	A → Y0	(HH)	0.417	0.753	1.311				0.008	0.014	0.025
		(LL)	0.391	0.706	1.263				0.010	0.014	0.022
	EN → Y0	(HZ)	1.071	1.944	3.224						
		(LZ)	0.499	0.902	1.557						
		(ZH)	0.821	1.487	2.581				0.008	0.014	0.025
		(ZL)	0.599	1.067	1.840				0.010	0.014	0.022

INTERFACE BLOCK(3.3V)

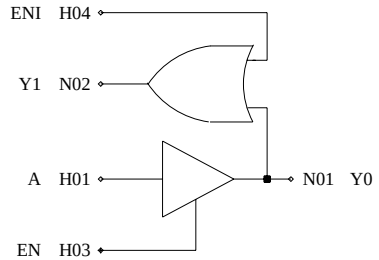
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			

[MEMO]

INTERFACE BLOCK (3.3V)

Function	LOW NOISE I/O BUFFER WITH EN(OR)				3.3V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA	BN7C33	BNBC33			1	10
9mA	BN7333	BNB333			1	10
12mA	BN7133	BNB133			1	10
18mA	BN7533	BNB533			1	10
24mA	BN7F33	BNBF33			1	10

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	ENI	Y1
0	0	0
1	0	1
0	1	1
1	1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BN7C33 to BNBC33	A	6.1	Y1	33
	EN	3.2		
	ENI	2.1		
BN7333 to BNB333	A	6.1	Y1	33
	EN	3.2		
	ENI	2.1		
BN7133 to BNB133	A	6.1	Y1	33
	EN	3.2		
	ENI	2.1		
BN7533 to BNB533	A	6.1	Y1	33
	EN	3.2		
	ENI	2.1		
BN7F33 to BNBF33	A	6.1	Y1	33
	EN	3.2		
	ENI	2.1		

INTERFACE BLOCK(3.3V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN7C33 to BNBC33	A → Y0	(HH)	1.484	2.804	5.056				0.033	0.057	0.102
		(LL)	1.446	2.847	5.070				0.039	0.058	0.091
	EN → Y0	(HZ)	0.965	1.786	2.815						
		(LZ)	0.724	1.144	1.770						
		(ZH)	1.432	2.775	5.046				0.033	0.057	0.102
		(ZL)	1.480	2.940	5.224				0.039	0.058	0.091
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN7333 to BNB333	A → Y0	(HH)	1.543	2.980	5.502				0.026	0.045	0.077
		(LL)	1.447	2.918	5.314				0.029	0.045	0.070
	EN → Y0	(HZ)	1.189	2.288	3.646						
		(LZ)	0.838	1.345	2.109						
		(ZH)	1.492	2.957	5.508				0.026	0.045	0.077
		(ZL)	1.484	3.011	5.492				0.029	0.044	0.070
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN7133 to BNB133	A → Y0	(HH)	1.636	3.208	6.011				0.022	0.039	0.068
		(LL)	1.470	3.024	5.605				0.025	0.039	0.061
	EN → Y0	(HZ)	1.431	2.802	4.512						
		(LZ)	0.945	1.537	2.431						
		(ZH)	1.583	3.187	6.011				0.022	0.039	0.068
		(ZL)	1.506	3.118	5.756				0.025	0.039	0.061
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN7533 to BNB533	A → Y0	(HH)	1.836	3.669	6.952				0.020	0.036	0.062
		(LL)	1.563	3.287	6.262				0.021	0.035	0.055
	EN → Y0	(HZ)	1.916	3.850	6.255						
		(LZ)	1.179	1.958	3.113						
		(ZH)	1.784	3.646	6.987				0.020	0.036	0.061
		(ZL)	1.605	3.377	6.409				0.021	0.034	0.055
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			
BN7F33 to BNBF33	A → Y0	(HH)	2.090	4.257	8.132				0.019	0.033	0.060
		(LL)	1.772	3.750	7.178				0.018	0.031	0.051
	EN → Y0	(HZ)	2.396	4.909	8.009						
		(LZ)	1.412	2.383	3.805						
		(ZH)	2.041	4.239	8.119				0.019	0.033	0.058
		(ZL)	1.783	3.822	7.275				0.019	0.031	0.051
	ENI → Y1	(HH)	0.206	0.300	0.437	0.008	0.015	0.025			
		(LL)	0.190	0.383	0.683	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.212	0.304	0.442	0.008	0.015	0.025			
		(LL)	0.201	0.394	0.695	0.010	0.016	0.026			

[MEMO]

CHAPTER 2

INTERFACE BLOCK

(5V)

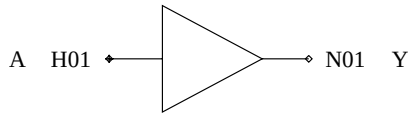
2 - 1

INTERFACE BLOCK (5V)

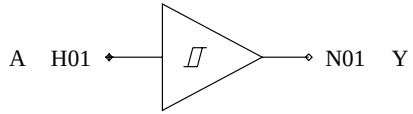
Function	INPUT BUFFER					5V
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIV1	FDV1			1	4
Schmitt	FIF1	FDF1			1	8
Clock	FIG1	FDG1			1	24

Logic Diagram

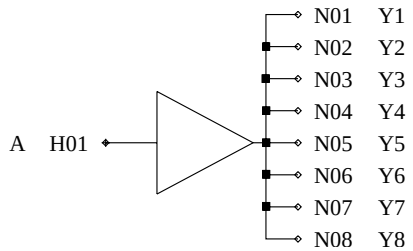
"Normal"



"Schmitt"



"Clock"



Truth Table

A	Yn
1	1
0	0

(n=1 to 8)

Block type	Input		Output	
	Symbol	Fan-In	Symbol	Fan-Out
FIV1 to FDV1	A	-	Y	32
FIF1 to FDF1	A	-	Y	22
FIG1 to FDG1	A	-	Y1	34
	:	:	Y2	34
			:	:
			Y7	34
			Y8	34

INTERFACE BLOCK(5V)

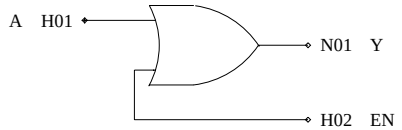
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIV1	A → Y	(HH)	0.257	0.400	0.683	0.008	0.015	0.024			
to FDV1		(LL)	0.150	0.278	0.492	0.010	0.016	0.025			
FIF1	A → Y	(HH)	0.922	1.626	2.856	0.012	0.023	0.037			
to FDF1		(LL)	0.544	1.048	1.885	0.010	0.016	0.026			
FIG1	A → Yn	(HH)	0.333	0.543	0.988	0.001	0.002	0.004			
to FDG1		(LL)	0.204	0.379	0.662	0.001	0.002	0.003			
	(n = 1 to 8)										

INTERFACE BLOCK (5V)

Function	INPUT BUFFER WITH EN(OR)					5V
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FN1335	FN2335			1	4
Schmitt						
Clock						

Logic Diagram

"Normal"



Truth Table

A	EN	Y
0	0	0
0	1	1
1	0	1
1	1	1

"Schmitt"

Block type	Input		Output	
	Symbol	Fan-In	Symbol	Fan-Out
FN1335 to FN2335	A	-	Y	34
	EN	2.1		

"Clock"

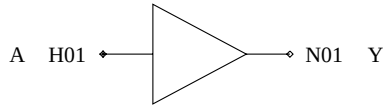
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FN1335 to FN2335	A → Y	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
	EN → Y	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	CMOS OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	FY09				1	20
6mA	FY04				1	20
9mA	FY01				1	24
12mA	FY02				1	24
18mA	FY03				2	24
24mA	FY06				2	24

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FY09	A	8.0	Y	-
FY04	A	8.0	Y	-
FY01	A	16.1	Y	-
FY02	A	16.1	Y	-
FY03	A	10.7	Y	-
FY06	A	10.7	Y	-

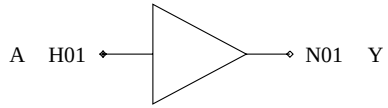
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FY09	A → Y	(HH)	0.720	1.244	2.223				0.057	0.101	0.188
		(LL)	0.836	1.225	1.953				0.073	0.103	0.162
FY04	A → Y	(HH)	0.606	1.018	1.757				0.020	0.036	0.068
		(LL)	0.696	1.179	1.973				0.026	0.037	0.060
FY01	A → Y	(HH)	0.437	0.762	1.327				0.015	0.028	0.053
		(LL)	0.509	0.845	1.421				0.020	0.029	0.048
FY02	A → Y	(HH)	0.453	0.802	1.403				0.011	0.021	0.041
		(LL)	0.519	0.896	1.541				0.015	0.022	0.036
FY03	A → Y	(HH)	0.573	1.394	1.734				0.007	0.013	0.023
		(LL)	0.709	1.436	2.133				0.009	0.015	0.022
FY06	A → Y	(HH)	0.590	1.478	1.811				0.006	0.012	0.021
		(LL)	0.738	1.528	2.262				0.008	0.014	0.020

INTERFACE BLOCK (5V)

Function	CMOS LOW-NOISE OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	FZ02				1	8
18mA	FZ03				2	8
24mA	FZ06				2	8

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FZ02	A	7.0	Y	-
FZ03	A	7.0	Y	-
FZ06	A	7.0	Y	-

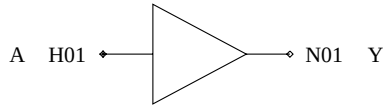
INTERFACE BLOCK(5V)

Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			T			
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
FZ02	A → Y	(HH)	1.844	3.548	6.562				0.023	0.040	0.069	
		(LL)	1.689	3.418	6.205				0.026	0.041	0.065	
FZ03	A → Y	(HH)	3.028	6.073	11.564				0.018	0.031	0.053	
		(LL)	2.725	5.808	10.780				0.019	0.032	0.052	
FZ06	A → Y	(HH)	3.248	6.558	12.558				0.017	0.030	0.053	
		(LL)	2.879	6.174	11.507				0.018	0.031	0.051	

INTERFACE BLOCK (5V)

Function	TTL OUTPUT BUFFER					5V
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA	FV0A				1	4
2mA	FV0B				1	4
3mA	FV09				1	4
6mA	FV04				1	4
9mA	FV01				1	8
12mA						
18mA						
24mA						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FV0A	A	8.1	Y	-
FV0B	A	8.1	Y	-
FV09	A	8.1	Y	-
FV04	A	8.1	Y	-
FV01	A	16.3	Y	-

Truth Table

A	Y
1	1
0	0

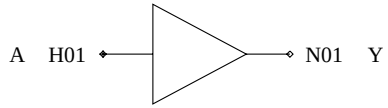
INTERFACE BLOCK(5V)

Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			T			
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
FV0A	A → Y	(HH)	0.973	1.666	2.916				0.058	0.103	0.191	
		(LL)	1.008	1.572	2.573				0.073	0.104	0.163	
FV0B	A → Y	(HH)	0.809	1.399	2.422				0.030	0.053	0.099	
		(LL)	0.745	1.264	2.163				0.038	0.054	0.086	
FV09	A → Y	(HH)	0.819	1.442	2.512				0.021	0.037	0.070	
		(LL)	0.723	1.280	2.274				0.026	0.038	0.061	
FV04	A → Y	(HH)	0.846	1.519	2.671				0.017	0.030	0.056	
		(LL)	0.724	1.340	2.430				0.021	0.031	0.051	
FV01	A → Y	(HH)	0.752	1.418	2.561				0.013	0.023	0.045	
		(LL)	0.635	1.251	2.361				0.016	0.024	0.040	

INTERFACE BLOCK (5V)

Function	TTL LOW-NOISE OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	FW02				1	4
18mA	FW03				2	4
24mA	FW06				2	4

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FW02	A	6.1	Y	-
FW03	A	6.1	Y	-
FW06	A	6.1	Y	-

Truth Table

A	Y
1	1
0	0

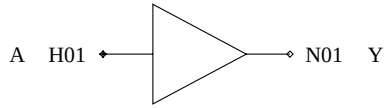
INTERFACE BLOCK(5V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FW02	A → Y	(HH)	1.726	3.468	6.619				0.016	0.029	0.054
		(LL)	1.959	4.101	7.801				0.020	0.033	0.054
FW03	A → Y	(HH)	2.326	4.657	8.989				0.013	0.024	0.043
		(LL)	2.766	5.869	11.034				0.016	0.029	0.048
FW06	A → Y	(HH)	2.630	5.337	10.382				0.013	0.023	0.043
		(LL)	3.082	6.610	12.484				0.015	0.027	0.047

INTERFACE BLOCK (5V)

Function	TTL HIGH SPEED OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	FY19				1	4
6mA	FY14				1	4
9mA	FY11				1	8
12mA	FY12				1	8
18mA	FY13				2	8
24mA	FY16				2	8

Logic Diagram



Truth Table

A	Y
0	0
1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FY19	A	8.0	Y	-
FY14	A	8.0	Y	-
FY11	A	16.1	Y	-
FY12	A	16.1	Y	-
FY13	A	16.1	Y	-
FY16	A	16.1	Y	-

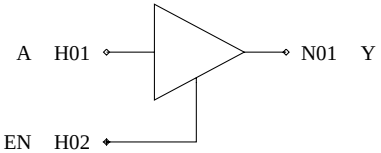
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FY19	A → Y	(HH)	0.720	1.244	2.223				0.057	0.101	0.188
		(LL)	0.836	1.225	1.953				0.073	0.103	0.162
FY14	A → Y	(HH)	0.606	1.018	1.757				0.020	0.036	0.068
		(LL)	0.696	1.179	1.973				0.026	0.037	0.060
FY11	A → Y	(HH)	0.437	0.762	1.327				0.015	0.028	0.053
		(LL)	0.509	0.845	1.421				0.020	0.029	0.048
FY12	A → Y	(HH)	0.453	0.802	1.403				0.011	0.021	0.041
		(LL)	0.519	0.896	1.541				0.015	0.022	0.036
FY13	A → Y	(HH)	0.573	0.998	1.734				0.007	0.012	0.023
		(LL)	0.709	1.247	2.133				0.009	0.013	0.022
FY16	A → Y	(HH)	0.590	1.034	1.811				0.006	0.011	0.021
		(LL)	0.738	1.314	2.262				0.008	0.012	0.020

INTERFACE BLOCK (5V)

Function	CMOS 3-STATE OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BD0T				1	32
6mA	BD0E				1	32
9mA	BD08				1	42
12mA	BD07				1	42
18mA	BD09				2	42
24mA	BD0H				2	42

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BD0T	A	20.2	Y	-
	EN	1.0		
BD0E	A	17.8	Y	-
	EN	1.0		
BD08	A	21.3	Y	-
	EN	2.0		
BD07	A	21.3	Y	-
	EN	2.0		
BD09	A	21.3	Y	-
	EN	2.0		
BD0H	A	21.3	Y	-
	EN	2.0		

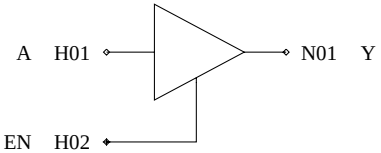
INTERFACE BLOCK(5V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BD0T	A → Y	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
BD0E	A → Y	(HH)	0.490	0.948	1.606				0.020	0.036	0.068
		(LL)	0.581	1.134	1.768				0.026	0.038	0.061
	EN → Y	(HZ)	1.120	1.798	3.569						
		(LZ)	0.667	0.971	2.174						
		(ZH)	1.098	1.824	3.493				0.020	0.035	0.068
		(ZL)	0.864	1.432	2.468				0.026	0.038	0.061
BD08	A → Y	(HH)	0.457	0.808	1.352				0.016	0.027	0.054
		(LL)	0.499	0.970	1.468				0.020	0.031	0.049
	EN → Y	(HZ)	0.986	1.613	3.100						
		(LZ)	0.529	0.830	1.728						
		(ZH)	0.964	1.608	2.938				0.015	0.027	0.054
		(ZL)	0.728	1.290	2.094				0.020	0.031	0.049
BD07	A → Y	(HH)	0.475	0.863	1.444				0.011	0.020	0.040
		(LL)	0.524	1.021	1.584				0.015	0.024	0.038
	EN → Y	(HZ)	1.069	1.787	3.366						
		(LZ)	0.561	0.891	1.830						
		(ZH)	0.989	1.657	3.049				0.011	0.020	0.041
		(ZL)	0.733	1.323	2.150				0.015	0.024	0.039
BD09	A → Y	(HH)	0.638	1.073	2.043				0.007	0.013	0.024
		(LL)	0.692	1.300	2.246				0.010	0.016	0.025
	EN → Y	(HZ)	1.346	2.107	4.176						
		(LZ)	0.679	0.988	2.160						
		(ZH)	1.132	1.868	3.593				0.008	0.012	0.024
		(ZL)	0.854	1.543	2.660				0.010	0.016	0.025
BD0H	A → Y	(HH)	0.665	1.111	2.157				0.007	0.011	0.021
		(LL)	0.725	1.364	2.391				0.009	0.015	0.023
	EN → Y	(HZ)	1.441	2.254	4.466						
		(LZ)	0.708	1.028	2.251						
		(ZH)	1.157	1.912	3.709				0.007	0.011	0.022
		(ZL)	0.862	1.573	2.719				0.009	0.015	0.024

INTERFACE BLOCK (5V)

Function	CMOS LOW-NOISE 3-STATE OUTPUT BUFFER				5V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BJ07				1	20
18mA	BJ09				2	20
24mA	BJ0H				2	20

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BJ07	A	7.1	Y	-
	EN	4.2		
BJ09	A	7.1	Y	-
	EN	4.2		
BJ0H	A	7.1	Y	-
	EN	4.2		

Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

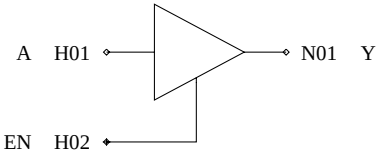
INTERFACE BLOCK(5V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BJ07	A → Y	(HH)	2.565	5.089	9.558				0.023	0.040	0.069
		(LL)	1.786	3.825	7.040				0.022	0.035	0.057
	EN → Y	(HZ)	1.833	3.131	4.762						
		(LZ)	1.210	1.903	3.016						
		(ZH)	2.539	5.105	9.601				0.023	0.040	0.069
		(ZL)	1.762	3.713	6.670				0.022	0.036	0.060
BJ09	A → Y	(HH)	3.808	7.716	14.622				0.020	0.036	0.062
		(LL)	2.564	5.821	10.808				0.020	0.032	0.052
	EN → Y	(HZ)	3.024	5.132	7.751						
		(LZ)	1.923	2.980	4.651						
		(ZH)	3.783	7.729	14.677				0.020	0.036	0.062
		(ZL)	2.555	5.554	10.116				0.019	0.033	0.055
BJ0H	A → Y	(HH)	4.095	8.344	15.878				0.020	0.035	0.061
		(LL)	2.733	6.186	11.537				0.019	0.031	0.050
	EN → Y	(HZ)	3.431	5.848	8.897						
		(LZ)	2.121	3.288	5.141						
		(ZH)	4.071	8.359	15.940				0.020	0.035	0.061
		(ZL)	2.666	5.858	10.709				0.019	0.032	0.054

INTERFACE BLOCK (5V)

Function	TTL 3-STATE OUTPUT BUFFER					5V
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA	BV0Q	BVDQ			1	16
2mA	BV0M	BVDM			1	16
3mA	BV0T	BVDT			1	16
6mA	BV0E	BVDE			1	16
9mA	BV08	BVD8			1	20
12mA						
18mA						
24mA						

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BV0Q to BVDQ	A	7.1	Y	-
	EN	4.5		
BV0M to BVDM	A	7.1	Y	-
	EN	4.5		
BV0T to BVDT	A	7.1	Y	-
	EN	4.5		
BV0E to BVDE	A	7.1	Y	-
	EN	4.5		
BV08 to BVD8	A	13.3	Y	-
	EN	4.6		

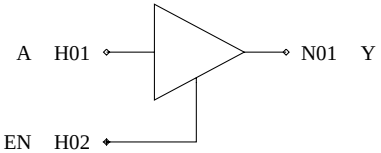
INTERFACE BLOCK(5V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BV0Q to BVDQ	A → Y	(HH)	1.184	2.056	3.557				0.059	0.104	0.191
		(LL)	1.123	1.930	3.335				0.075	0.106	0.166
	EN → Y	(HZ)	0.720	1.195	1.785						
		(LZ)	0.507	0.828	1.327						
		(ZH)	1.079	1.826	3.045				0.058	0.103	0.190
		(ZL)	1.088	1.888	3.201				0.075	0.106	0.167
BV0M to BVDM	A → Y	(HH)	1.125	2.004	3.446				0.031	0.054	0.099
		(LL)	0.985	1.808	3.212				0.040	0.058	0.092
	EN → Y	(HZ)	0.990	1.819	2.882						
		(LZ)	0.574	0.970	1.584						
		(ZH)	1.016	1.764	2.950				0.031	0.054	0.100
		(ZL)	1.014	1.830	3.161				0.040	0.059	0.094
BV0T to BVDT	A → Y	(HH)	1.165	2.134	3.735				0.023	0.039	0.071
		(LL)	1.035	1.923	3.473				0.030	0.045	0.072
	EN → Y	(HZ)	1.215	2.302	3.692						
		(LZ)	0.649	1.111	1.819						
		(ZH)	1.041	1.864	3.188				0.023	0.040	0.072
		(ZL)	1.056	1.894	3.307				0.031	0.047	0.075
BV0E to BVDE	A → Y	(HH)	1.215	2.273	4.034				0.020	0.033	0.059
		(LL)	1.063	1.975	3.458				0.027	0.041	0.064
	EN → Y	(HZ)	1.442	2.759	4.456						
		(LZ)	0.719	1.246	2.041						
		(ZH)	1.074	1.844	3.026				0.020	0.034	0.060
		(ZL)	1.057	1.871	3.265				0.028	0.043	0.068
BV08 to BVD8	A → Y	(HH)	1.136	2.187	3.929				0.016	0.027	0.047
		(LL)	1.040	2.018	3.823				0.025	0.037	0.057
	EN → Y	(HZ)	1.997	3.945	6.414						
		(LZ)	0.900	1.576	2.578						
		(ZH)	1.112	2.074	3.642				0.016	0.027	0.048
		(ZL)	1.072	1.960	3.629				0.026	0.040	0.061

INTERFACE BLOCK (5V)

Function	TTL LOW-NOISE 3-STATE OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BY07	BYD7			1	16
18mA	BY09	BYD9			2	16
24mA	BY0H	BYDH			2	16

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BY07 to BYD7	A	6.1	Y	-
	EN	4.5		
BY09 to BYD9	A	6.1	Y	-
	EN	4.5		
BY0H to BYDH	A	6.1	Y	-
	EN	4.5		

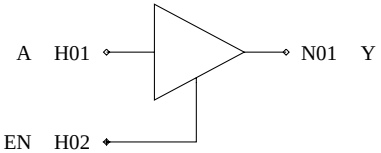
INTERFACE BLOCK(5V)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BY07 to BYD7	A → Y	(HH)	2.232	4.527	8.678				0.019	0.035	0.061
		(LL)	1.987	4.111	7.806				0.024	0.038	0.062
	EN → Y	(HZ)	2.391	4.855	7.978						
		(LZ)	1.483	2.516	4.052						
		(ZH)	2.156	4.442	8.516				0.019	0.035	0.062
		(ZL)	1.966	4.152	7.834				0.025	0.039	0.063
BY09 to BYD9	A → Y	(HH)	3.028	6.194	12.045				0.017	0.031	0.053
		(LL)	2.722	5.106	8.050				0.021	0.034	0.054
	EN → Y	(HZ)	3.374	6.267	9.976						
		(LZ)	2.122	3.379	5.355						
		(ZH)	2.932	4.361	7.918				0.017	0.032	0.055
		(ZL)	2.686	5.054	8.242				0.021	0.034	0.057
BY0H to BYDH	A → Y	(HH)	3.484	7.192	14.049				0.017	0.030	0.053
		(LL)	3.072	5.568	9.302				0.021	0.033	0.052
	EN → Y	(HZ)	4.235	7.923	12.718						
		(LZ)	2.548	4.087	6.497						
		(ZH)	3.391	4.950	9.407				0.017	0.031	0.055
		(ZL)	2.980	5.438	9.017				0.021	0.034	0.057

INTERFACE BLOCK (5V)

Function	TTL HIGH SPEED 3-STATE OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BD1T	BD2T			1	32
6mA	BD1E	BD2E			1	32
9mA	BD18	BD28			1	42
12mA	BD17	BD27			1	42
18mA	BD19	BD29			2	42
24mA	BD1H	BD2H			2	42

Logic Diagram



Truth Table

A	EN	Y
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BD1T to BD2T	A	20.2	Y	-
	EN	1.0		
BD1E to BD2E	A	20.2	Y	-
	EN	1.0		
BD18 to BD28	A	22.2	Y	-
	EN	2.0		
BD17 to BD27	A	22.2	Y	-
	EN	2.0		
BD19 to BD29	A	22.2	Y	-
	EN	2.0		
BD1H to BD2H	A	22.2	Y	-
	EN	2.0		

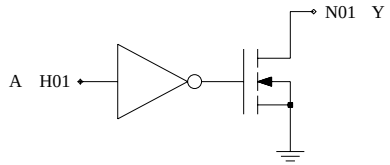
INTERFACE BLOCK(5V)

Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			T			
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
BD1T to BD2T	A → Y	(HH)	0.644	1.162	2.163				0.058	0.103	0.190	
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164	
	EN → Y	(HZ)	0.885	1.655	2.878							
		(LZ)	0.526	0.991	1.745							
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190	
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165	
BD1E to BD2E	A → Y	(HH)	0.490	0.896	1.606				0.020	0.036	0.068	
		(LL)	0.581	1.030	1.768				0.026	0.038	0.061	
	EN → Y	(HZ)	1.120	2.078	3.569							
		(LZ)	0.667	1.234	2.174							
		(ZH)	1.098	2.007	3.493				0.020	0.036	0.068	
		(ZL)	0.864	1.486	2.468				0.026	0.038	0.061	
BD18 to BD28	A → Y	(HH)	0.457	0.791	1.352				0.016	0.028	0.054	
		(LL)	0.499	0.854	1.468				0.020	0.030	0.049	
	EN → Y	(HZ)	0.986	1.818	3.100							
		(LZ)	0.529	0.979	1.728							
		(ZH)	0.964	1.717	2.938				0.015	0.028	0.054	
		(ZL)	0.728	1.251	2.094				0.020	0.030	0.049	
BD17 to BD27	A → Y	(HH)	0.475	0.839	1.444				0.011	0.021	0.040	
		(LL)	0.524	0.912	1.584				0.015	0.023	0.038	
	EN → Y	(HZ)	1.069	1.981	3.366							
		(LZ)	0.561	1.039	1.830							
		(ZH)	0.989	1.772	3.049				0.011	0.021	0.041	
		(ZL)	0.733	1.280	2.150				0.015	0.024	0.039	
BD19 to BD29	A → Y	(HH)	0.638	1.172	2.043				0.007	0.013	0.024	
		(LL)	0.692	1.247	2.246				0.010	0.015	0.025	
	EN → Y	(HZ)	1.346	2.479	4.176							
		(LZ)	0.679	1.248	2.160							
		(ZH)	1.132	2.060	3.593				0.008	0.013	0.024	
		(ZL)	0.854	1.547	2.660				0.010	0.015	0.025	
BD1H to BD2H	A → Y	(HH)	0.665	1.231	2.157				0.007	0.012	0.021	
		(LL)	0.725	1.318	2.391				0.009	0.014	0.023	
	EN → Y	(HZ)	1.441	2.648	4.466							
		(LZ)	0.708	1.302	2.251							
		(ZH)	1.157	2.120	3.709				0.007	0.012	0.022	
		(ZL)	0.862	1.576	2.719				0.009	0.015	0.024	

INTERFACE BLOCK (5V)

Function	TTL N-CH OPEN DRAIN OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	EVTH				1	4
6mA	EVTJ				1	4
9mA						
12mA	EVT9				1	8
18mA	EVT5				2	8
24mA	EVTD				2	8

Logic Diagram



Truth Table

A	Y
1	Z
0	0

Z:High Impedance

Connect a pull-up resistor to get a high level

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
EVTH	A	8.1	Y	-
EVTJ	A	8.1	Y	-
EVT9	A	16.3	Y	-
EVT5	A	16.3	Y	-
EVTD	A	16.3	Y	-

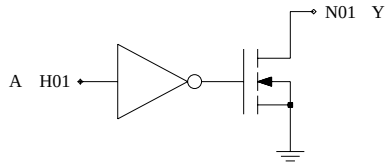
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EVTH	A → Y	(LZ)	0.272	0.394	0.568						
		(ZL)	0.528	0.901	1.560				0.114	0.183	0.318
EVTJ	A → Y	(LZ)	0.318	0.510	0.794						
		(ZL)	0.374	0.676	1.228				0.057	0.092	0.159
EVT9	A → Y	(LZ)	0.325	0.605	0.989						
		(ZL)	0.352	0.688	1.303				0.029	0.046	0.081
EVT5	A → Y	(LZ)	0.377	0.647	1.019						
		(ZL)	0.391	0.744	1.398				0.019	0.031	0.054
EVTD	A → Y	(LZ)	0.432	0.758	1.206						
		(ZL)	0.408	0.794	1.512				0.014	0.023	0.041

INTERFACE BLOCK (5V)

Function	TTL LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	EYT9				1	2
18mA	EYT5				2	2
24mA	EYTD				2	2

Logic Diagram



Truth Table

A	Y
1	Z
0	0

Z:High Impedance

Connect a pull-up resistor to get a high level

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
EYT9	A	3.0	Y	-
EYT5	A	3.0	Y	-
EYTD	A	3.0	Y	-

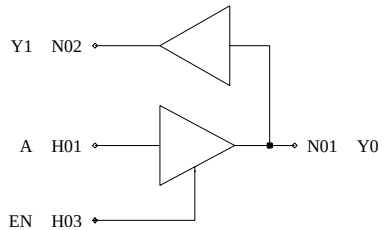
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EYT9	A → Y	(LZ)	1.837	3.033	4.685						
		(ZL)	1.399	2.890	5.347				0.032	0.053	0.092
EYT5	A → Y	(LZ)	2.939	4.783	7.353						
		(ZL)	2.004	4.159	7.762				0.025	0.043	0.073
EYTD	A → Y	(LZ)	3.416	5.594	8.670						
		(ZL)	2.155	4.539	8.524				0.022	0.037	0.064

INTERFACE BLOCK (5V)

Function	CMOS I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BM0U				1	36
6mA	BM0C				1	36
9mA	BM03				1	46
12mA	BM01				1	46
18mA	BM05				2	46
24mA	BM0F				2	46

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BM0U	A	20.2	Y1	34
	EN	1.0		
BM0C	A	17.8	Y1	34
	EN	1.0		
BM03	A	21.3	Y1	34
	EN	2.0		
BM01	A	21.3	Y1	34
	EN	2.0		
BM05	A	21.3	Y1	34
	EN	2.0		
BM0F	A	21.3	Y1	34
	EN	2.0		

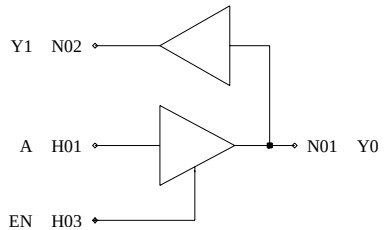
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BM0U	A → Y0	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y0	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM0C	A → Y0	(HH)	0.490	0.948	1.606				0.020	0.036	0.068
		(LL)	0.581	1.134	1.768				0.026	0.038	0.061
	EN → Y0	(HZ)	1.120	1.798	3.569						
		(LZ)	0.667	0.971	2.174						
		(ZH)	1.098	1.824	3.493				0.020	0.035	0.068
		(ZL)	0.864	1.432	2.468				0.026	0.038	0.061
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM03	A → Y0	(HH)	0.457	0.808	1.352				0.016	0.027	0.054
		(LL)	0.499	0.970	1.468				0.020	0.031	0.049
	EN → Y0	(HZ)	0.986	1.613	3.100						
		(LZ)	0.529	0.830	1.728						
		(ZH)	0.964	1.608	2.938				0.015	0.027	0.054
		(ZL)	0.728	1.290	2.094				0.020	0.031	0.049
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM01	A → Y0	(HH)	0.475	0.863	1.444				0.011	0.020	0.040
		(LL)	0.524	1.021	1.584				0.015	0.024	0.038
	EN → Y0	(HZ)	1.069	1.787	3.366						
		(LZ)	0.561	0.891	1.830						
		(ZH)	0.989	1.657	3.049				0.011	0.020	0.041
		(ZL)	0.733	1.323	2.150				0.015	0.024	0.039
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM05	A → Y0	(HH)	0.638	1.073	2.043				0.007	0.013	0.024
		(LL)	0.692	1.300	2.246				0.010	0.016	0.025
	EN → Y0	(HZ)	1.346	2.107	4.176						
		(LZ)	0.679	0.988	2.160						
		(ZH)	1.132	1.868	3.593				0.008	0.012	0.024
		(ZL)	0.854	1.543	2.660				0.010	0.016	0.025
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM0F	A → Y0	(HH)	0.665	1.111	2.157				0.007	0.011	0.021
		(LL)	0.725	1.364	2.391				0.009	0.015	0.023
	EN → Y0	(HZ)	1.441	2.254	4.466						
		(LZ)	0.708	1.028	2.251						
		(ZH)	1.157	1.912	3.709				0.007	0.011	0.022
		(ZL)	0.862	1.573	2.719				0.009	0.015	0.024
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (5V)

Function	CMOS LOW-NOISE I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BP01				1	24
18mA	BP05				2	24
24mA	BP0F				2	24

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BP01	A	7.1	Y1	34
	EN	4.2		
BP05	A	7.1	Y1	34
	EN	4.2		
BP0F	A	7.1	Y1	34
	EN	4.2		

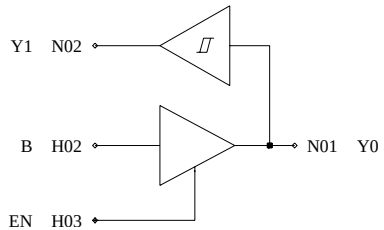
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BP01	A → Y0	(HH)	2.565	5.089	9.558				0.023	0.040	0.069
		(LL)	1.786	3.825	7.040				0.022	0.035	0.057
	EN → Y0	(HZ)	1.833	3.131	4.762						
		(LZ)	1.210	1.903	3.016						
		(ZH)	2.539	5.105	9.601				0.023	0.040	0.069
		(ZL)	1.762	3.713	6.670				0.022	0.036	0.060
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BP05	A → Y0	(HH)	3.808	7.716	14.622				0.020	0.036	0.062
		(LL)	2.564	5.821	10.808				0.020	0.032	0.052
	EN → Y0	(HZ)	3.024	5.132	7.751						
		(LZ)	1.923	2.980	4.651						
		(ZH)	3.783	7.729	14.677				0.020	0.036	0.062
		(ZL)	2.555	5.554	10.116				0.019	0.033	0.055
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BP0F	A → Y0	(HH)	4.095	8.344	15.878				0.020	0.035	0.061
		(LL)	2.733	6.186	11.537				0.019	0.031	0.050
	EN → Y0	(HZ)	3.431	5.848	8.897						
		(LZ)	2.121	3.288	5.141						
		(ZH)	4.071	8.359	15.940				0.020	0.035	0.061
		(ZL)	2.666	5.858	10.709				0.019	0.032	0.054
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (5V)

Function	CMOS SCHMITT I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BQIU				1	40
6mA	BQIC				1	40
9mA	BQI3				1	50
12mA	BQI1				1	50
18mA	BQI5				2	50
24mA	BQIF				2	50

Logic Diagram



Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BQIU	B	20.2	Y1	22
	EN	1.0		
BQIC	B	17.8	Y1	22
	EN	1.0		
BQI3	B	21.3	Y1	22
	EN	2.0		
BQI1	B	21.3	Y1	22
	EN	2.0		
BQI5	B	21.3	Y1	22
	EN	2.0		
BQIF	B	21.3	Y1	22
	EN	2.0		

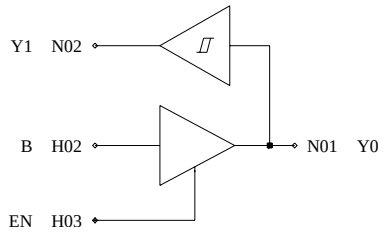
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BQIU	B → Y0	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y0	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BQIC	B → Y0	(HH)	0.490	0.948	1.606				0.020	0.036	0.068
		(LL)	0.581	1.134	1.768				0.026	0.038	0.061
	EN → Y0	(HZ)	1.120	1.798	3.569						
		(LZ)	0.667	0.971	2.174						
		(ZH)	1.098	1.824	3.493				0.020	0.035	0.068
		(ZL)	0.864	1.432	2.468				0.026	0.038	0.061
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BQI3	B → Y0	(HH)	0.457	0.808	1.352				0.016	0.027	0.054
		(LL)	0.499	0.970	1.468				0.020	0.031	0.049
	EN → Y0	(HZ)	0.986	1.613	3.100						
		(LZ)	0.529	0.830	1.728						
		(ZH)	0.964	1.608	2.938				0.015	0.027	0.054
		(ZL)	0.728	1.290	2.094				0.020	0.031	0.049
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BQI1	B → Y0	(HH)	0.475	0.863	1.444				0.011	0.020	0.040
		(LL)	0.524	1.021	1.584				0.015	0.024	0.038
	EN → Y0	(HZ)	1.069	1.787	3.366						
		(LZ)	0.561	0.891	1.830						
		(ZH)	0.989	1.657	3.049				0.011	0.020	0.041
		(ZL)	0.733	1.323	2.150				0.015	0.024	0.039
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BQI5	B → Y0	(HH)	0.638	1.073	2.043				0.007	0.013	0.024
		(LL)	0.692	1.300	2.246				0.010	0.016	0.025
	EN → Y0	(HZ)	1.346	2.107	4.176						
		(LZ)	0.679	0.988	2.160						
		(ZH)	1.132	1.868	3.593				0.008	0.012	0.024
		(ZL)	0.854	1.543	2.660				0.010	0.016	0.025
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BQIF	B → Y0	(HH)	0.665	1.111	2.157				0.007	0.011	0.021
		(LL)	0.725	1.364	2.391				0.009	0.015	0.023
	EN → Y0	(HZ)	1.441	2.254	4.466						
		(LZ)	0.708	1.028	2.251						
		(ZH)	1.157	1.912	3.709				0.007	0.011	0.022
		(ZL)	0.862	1.573	2.719				0.009	0.015	0.024
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	CMOS LOW-NOISE SCHMITT I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BUI1				1	28
18mA	BUI5				2	28
24mA	BUIF				2	28

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BUI1	B	7.1	Y1	22
	EN	4.2		
BUI5	B	7.1	Y1	22
	EN	4.2		
BUIF	B	7.1	Y1	22
	EN	4.2		

Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

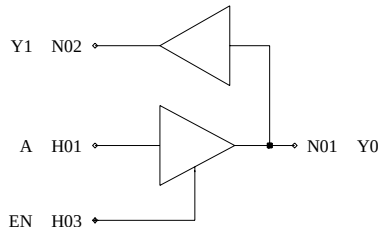
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BUI1	B → Y0	(HH)	2.565	5.089	9.558				0.023	0.040	0.069
		(LL)	1.786	3.825	7.040				0.022	0.035	0.057
	EN → Y0	(HZ)	1.833	3.131	4.762						
		(LZ)	1.210	1.903	3.016						
		(ZH)	2.539	5.105	9.601				0.023	0.040	0.069
		(ZL)	1.762	3.713	6.670				0.022	0.036	0.060
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BUI5	B → Y0	(HH)	3.808	7.716	14.622				0.020	0.036	0.062
		(LL)	2.564	5.821	10.808				0.020	0.032	0.052
	EN → Y0	(HZ)	3.024	5.132	7.751						
		(LZ)	1.923	2.980	4.651						
		(ZH)	3.783	7.729	14.677				0.020	0.036	0.062
		(ZL)	2.555	5.554	10.116				0.019	0.033	0.055
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BUIF	B → Y0	(HH)	4.095	8.344	15.878				0.020	0.035	0.061
		(LL)	2.733	6.186	11.537				0.019	0.031	0.050
	EN → Y0	(HZ)	3.431	5.848	8.897						
		(LZ)	2.121	3.288	5.141						
		(ZH)	4.071	8.359	15.940				0.020	0.035	0.061
		(ZL)	2.666	5.858	10.709				0.019	0.032	0.054
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	TTL I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA	BW0X	BWDX			1	20
2mA	BW0K	BWDK			1	20
3mA	BW0U	BWDU			1	20
6mA	BW0C	BWDC			1	20
9mA	BW03	BWD3			1	24
12mA						
18mA						
24mA						

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BW0X to BWDX	A	7.1	Y1	34
	EN	4.5		
BW0K to BWDK	A	7.1	Y1	34
	EN	4.5		
BW0U to BWDU	A	7.1	Y1	34
	EN	4.5		
BW0C to BWDC	A	7.1	Y1	34
	EN	4.5		
BW03 to BWD3	A	13.3	Y1	34
	EN	4.6		

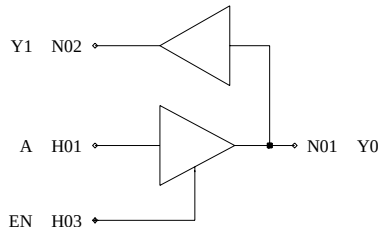
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BW0X to BWDX	A → Y0	(HH)	1.184	2.056	3.557				0.059	0.104	0.191
		(LL)	1.123	1.930	3.335				0.075	0.106	0.166
	EN → Y0	(HZ)	0.720	1.195	1.785						
		(LZ)	0.507	0.828	1.327						
		(ZH)	1.079	1.826	3.045				0.058	0.103	0.190
		(ZL)	1.088	1.888	3.201				0.075	0.106	0.167
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BW0K to BWDK	A → Y0	(HH)	1.125	2.004	3.446				0.031	0.054	0.099
		(LL)	0.985	1.808	3.212				0.040	0.058	0.092
	EN → Y0	(HZ)	0.990	1.819	2.882						
		(LZ)	0.574	0.970	1.584						
		(ZH)	1.016	1.764	2.950				0.031	0.054	0.100
		(ZL)	1.014	1.830	3.161				0.040	0.059	0.094
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BW0U to BWDU	A → Y0	(HH)	1.165	2.134	3.735				0.023	0.039	0.071
		(LL)	1.035	1.923	3.473				0.030	0.045	0.072
	EN → Y0	(HZ)	1.215	2.302	3.692						
		(LZ)	0.649	1.111	1.819						
		(ZH)	1.041	1.864	3.188				0.023	0.040	0.072
		(ZL)	1.056	1.894	3.307				0.031	0.047	0.075
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BW0C to BWDC	A → Y0	(HH)	1.215	2.273	4.034				0.020	0.033	0.059
		(LL)	1.063	1.975	3.458				0.027	0.041	0.064
	EN → Y0	(HZ)	1.442	2.759	4.456						
		(LZ)	0.719	1.246	2.041						
		(ZH)	1.074	1.844	3.026				0.020	0.034	0.060
		(ZL)	1.057	1.871	3.265				0.028	0.043	0.068
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BW03 to BWD3	A → Y0	(HH)	1.136	2.187	3.929				0.016	0.027	0.047
		(LL)	1.040	2.018	3.823				0.025	0.037	0.057
	EN → Y0	(HZ)	1.997	3.945	6.414						
		(LZ)	0.900	1.576	2.578						
		(ZH)	1.112	2.074	3.642				0.016	0.027	0.048
		(ZL)	1.072	1.960	3.629				0.026	0.040	0.061
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (5V)

Function	TTL LOW-NOISE I/O BUFFER				5V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BX01	BXD1			1	20
18mA	BX05	BXD5			2	20
24mA	BX0F	BXDF			2	20

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BX01 to BXD1	A	6.1	Y1	34
	EN	4.5		
BX05 to BXD5	A	6.1	Y1	34
	EN	4.5		
BX0F to BXDF	A	6.1	Y1	34
	EN	4.5		

Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

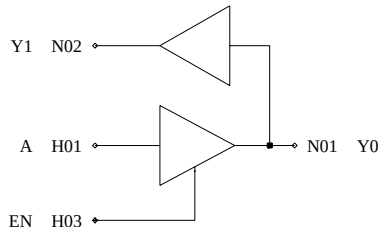
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BX01 to BXD1	A → Y0	(HH)	2.232	4.527	8.678				0.019	0.035	0.061
		(LL)	1.987	4.111	7.806				0.024	0.038	0.062
	EN → Y0	(HZ)	2.391	4.855	7.978						
		(LZ)	1.483	2.516	4.052						
		(ZH)	2.156	4.442	8.516				0.019	0.035	0.062
		(ZL)	1.966	4.152	7.834				0.025	0.039	0.063
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BX05 to BXD5	A → Y0	(HH)	3.028	6.194	12.045				0.017	0.031	0.053
		(LL)	2.722	5.106	8.050				0.021	0.034	0.054
	EN → Y0	(HZ)	3.374	6.267	9.976						
		(LZ)	2.122	3.379	5.355						
		(ZH)	2.932	4.361	7.918				0.017	0.032	0.055
		(ZL)	2.686	5.054	8.242				0.021	0.034	0.057
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BX0F to BXDF	A → Y0	(HH)	3.484	7.192	14.049				0.017	0.030	0.053
		(LL)	3.072	5.568	9.302				0.021	0.033	0.052
	EN → Y0	(HZ)	4.235	7.923	12.718						
		(LZ)	2.548	4.087	6.497						
		(ZH)	3.391	4.950	9.407				0.017	0.031	0.055
		(ZL)	2.980	5.438	9.017				0.021	0.034	0.057
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (5V)

Function	TTL HIGH SPEED I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BM1U	BM2U			1	36
6mA	BM1C	BM2C			1	36
9mA	BM13	BM23			1	46
12mA	BM11	BM21			1	46
18mA	BM15	BM25			2	46
24mA	BM1F	BM2F			2	46

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BM1U to BM2U	A	20.2	Y1	34
	EN	1.0		
BM1C to BM2C	A	17.8	Y1	34
	EN	1.0		
BM13 to BM23	A	21.3	Y1	34
	EN	2.0		
BM11 to BM21	A	21.3	Y1	34
	EN	2.0		
BM15 to BM25	A	21.3	Y1	34
	EN	2.0		
BM1F to BM2F	A	21.3	Y1	34
	EN	2.0		

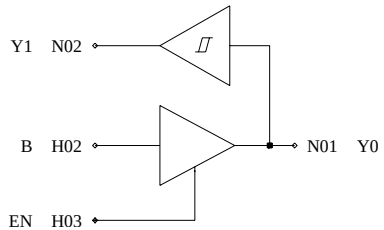
INTERFACE BLOCK(5V)

Block type	Path		Switching speed t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BM1U to BM2U	A → Y0	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y0	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM1C to BM2C	A → Y0	(HH)	0.490	0.948	1.606				0.020	0.036	0.068
		(LL)	0.581	1.134	1.768				0.026	0.038	0.061
	EN → Y0	(HZ)	1.120	1.798	3.569						
		(LZ)	0.667	0.971	2.174						
		(ZH)	1.098	1.824	3.493				0.020	0.035	0.068
		(ZL)	0.864	1.432	2.468				0.026	0.038	0.061
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM13 to BM23	A → Y0	(HH)	0.457	0.808	1.352				0.016	0.027	0.054
		(LL)	0.499	0.970	1.468				0.020	0.031	0.049
	EN → Y0	(HZ)	0.986	1.613	3.100						
		(LZ)	0.529	0.830	1.728						
		(ZH)	0.964	1.608	2.938				0.015	0.027	0.054
		(ZL)	0.728	1.290	2.094				0.020	0.031	0.049
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM11 to BM21	A → Y0	(HH)	0.475	0.863	1.444				0.011	0.020	0.040
		(LL)	0.524	1.021	1.584				0.015	0.024	0.038
	EN → Y0	(HZ)	1.069	1.787	3.366						
		(LZ)	0.561	0.891	1.830						
		(ZH)	0.989	1.657	3.049				0.011	0.020	0.041
		(ZL)	0.733	1.323	2.150				0.015	0.024	0.039
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM15 to BM25	A → Y0	(HH)	0.638	1.073	2.043				0.007	0.013	0.024
		(LL)	0.692	1.300	2.246				0.010	0.016	0.025
	EN → Y0	(HZ)	1.346	2.107	4.176						
		(LZ)	0.679	0.988	2.160						
		(ZH)	1.132	1.868	3.593				0.008	0.012	0.024
		(ZL)	0.854	1.543	2.660				0.010	0.016	0.025
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			
BM1F to BM2F	A → Y0	(HH)	0.665	1.111	2.157				0.007	0.011	0.021
		(LL)	0.725	1.364	2.391				0.009	0.015	0.023
	EN → Y0	(HZ)	1.441	2.254	4.466						
		(LZ)	0.708	1.028	2.251						
		(ZH)	1.157	1.912	3.709				0.007	0.011	0.022
		(ZL)	0.862	1.573	2.719				0.009	0.015	0.024
	Y0 → Y1	(HH)	0.223	0.312	0.446	0.008	0.015	0.024			
		(LL)	0.125	0.232	0.370	0.010	0.016	0.025			

INTERFACE BLOCK (5V)

Function	TTL SCHMITT I/O BUFFER				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA	BKIX	BKDX			1	24
2mA	BKIK	BKDK			1	24
3mA	BKIU	BKDU			1	24
6mA	BKIC	BKDC			1	24
9mA	BKI3	BKD3			1	28
12mA						
18mA						
24mA						

Logic Diagram



Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BKIX to BKDX	B	7.1	Y1	22
	EN	4.5		
BKIK to BKDK	B	7.1	Y1	22
	EN	4.5		
BKIU to BKDU	B	7.1	Y1	22
	EN	4.5		
BKIC to BKDC	B	7.1	Y1	22
	EN	4.5		
BKI3 to BKD3	B	13.3	Y1	22
	EN	4.6		

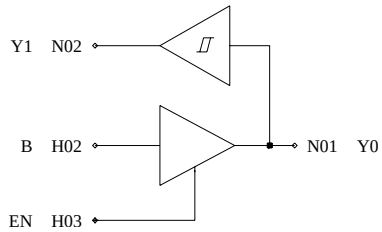
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BKIX	B → Y0	(HH)	1.184	2.056	3.557				0.059	0.104	0.191
to BKDX		(LL)	1.123	1.930	3.335				0.075	0.106	0.166
	EN → Y0	(HZ)	0.720	1.195	1.785						
		(LZ)	0.507	0.828	1.327						
		(ZH)	1.079	1.826	3.045				0.058	0.103	0.190
		(ZL)	1.088	1.888	3.201				0.075	0.106	0.167
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BKIK	B → Y0	(HH)	1.125	2.004	3.446				0.031	0.054	0.099
to BKDK		(LL)	0.985	1.808	3.212				0.040	0.058	0.092
	EN → Y0	(HZ)	0.990	1.819	2.882						
		(LZ)	0.574	0.970	1.584						
		(ZH)	1.016	1.764	2.950				0.031	0.054	0.100
		(ZL)	1.014	1.830	3.161				0.040	0.059	0.094
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BKIU	B → Y0	(HH)	1.165	2.134	3.735				0.023	0.039	0.071
to BKDU		(LL)	1.035	1.923	3.473				0.030	0.045	0.072
	EN → Y0	(HZ)	1.215	2.302	3.692						
		(LZ)	0.649	1.111	1.819						
		(ZH)	1.041	1.864	3.188				0.023	0.040	0.072
		(ZL)	1.056	1.894	3.307				0.031	0.047	0.075
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BKIC	B → Y0	(HH)	1.215	2.273	4.034				0.020	0.033	0.059
to BKDC		(LL)	1.063	1.975	3.458				0.027	0.041	0.064
	EN → Y0	(HZ)	1.442	2.759	4.456						
		(LZ)	0.719	1.246	2.041						
		(ZH)	1.074	1.844	3.026				0.020	0.034	0.060
		(ZL)	1.057	1.871	3.265				0.028	0.043	0.068
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BKI3	B → Y0	(HH)	1.136	2.187	3.929				0.016	0.027	0.047
to BKD3		(LL)	1.040	2.018	3.823				0.025	0.037	0.057
	EN → Y0	(HZ)	1.997	3.945	6.414						
		(LZ)	0.900	1.576	2.578						
		(ZH)	1.112	2.074	3.642				0.016	0.027	0.048
		(ZL)	1.072	1.960	3.629				0.026	0.040	0.061
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	TTL LOW-NOISE SCHMITT I/O BUFFER				5V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BZI1	BZD1			1	24
18mA	BZI5	BZD5			2	24
24mA	BZIF	BZDF			2	24

Logic Diagram



Truth Table

B	EN	Y0
0	1	0
1	1	1
X	0	Z

Y0	Y1
0	0
1	1

X:Irrelevant

Z:High Impedance

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BZI1 to BZD1	B	6.1	Y1	22
	EN	4.5		
BZI5 to BZD5	B	6.1	Y1	22
	EN	4.5		
BZIF to BZDF	B	6.1	Y1	22
	EN	4.5		

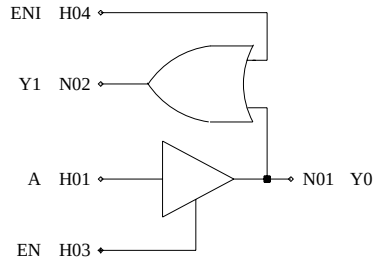
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BZI1 to BZD1	B → Y0	(HH)	2.232	4.527	8.678				0.019	0.035	0.061
		(LL)	1.987	4.111	7.806				0.024	0.038	0.062
	EN → Y0	(HZ)	2.391	4.855	7.978						
		(LZ)	1.483	2.516	4.052						
		(ZH)	2.156	4.442	8.516				0.019	0.035	0.062
		(ZL)	1.966	4.152	7.834				0.025	0.039	0.063
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BZI5 to BZD5	B → Y0	(HH)	3.028	6.194	12.045				0.017	0.031	0.053
		(LL)	2.722	5.106	8.050				0.021	0.034	0.054
	EN → Y0	(HZ)	3.374	6.267	9.976						
		(LZ)	2.122	3.379	5.355						
		(ZH)	2.932	4.361	7.918				0.017	0.032	0.055
		(ZL)	2.686	5.054	8.242				0.021	0.034	0.057
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			
BZIF to BZDF	B → Y0	(HH)	3.484	7.192	14.049				0.017	0.030	0.053
		(LL)	3.072	5.568	9.302				0.021	0.033	0.052
	EN → Y0	(HZ)	4.235	7.923	12.718						
		(LZ)	2.548	4.087	6.497						
		(ZH)	3.391	4.950	9.407				0.017	0.031	0.055
		(ZL)	2.980	5.438	9.017				0.021	0.034	0.057
	Y0 → Y1	(HH)	0.865	1.443	2.389	0.012	0.023	0.037			
		(LL)	0.539	0.994	1.723	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	CMOS I/O BUFFER WITH EN(OR)				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BN3U35				1	32
6mA	BN3C35				1	32
9mA	BN3335				1	32
12mA	BN3135				1	32
18mA	BN3535				2	36
24mA	BN3F35				2	36

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BN3U35	A	20.2	Y1	34
	EN	1.0		
	ENI	2.1		
BN3C35	A	20.2	Y1	34
	EN	1.0		
	ENI	2.1		
BN3335	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN3135	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN3535	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN3F35	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		

INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN3U35	A → Y0	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y0	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN3C35	A → Y0	(HH)	0.490	0.896	1.606				0.020	0.036	0.068
		(LL)	0.581	1.030	1.768				0.026	0.038	0.061
	EN → Y0	(HZ)	1.120	2.078	3.569						
		(LZ)	0.667	1.234	2.174						
		(ZH)	1.098	2.007	3.493				0.020	0.036	0.068
		(ZL)	0.864	1.486	2.468				0.026	0.038	0.061
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN3335	A → Y0	(HH)	0.457	0.791	1.352				0.016	0.028	0.054
		(LL)	0.499	0.854	1.468				0.020	0.030	0.049
	EN → Y0	(HZ)	0.986	1.818	3.100						
		(LZ)	0.529	0.979	1.728						
		(ZH)	0.964	1.717	2.938				0.015	0.028	0.054
		(ZL)	0.728	1.251	2.094				0.020	0.030	0.049
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN3135	A → Y0	(HH)	0.475	0.839	1.444				0.011	0.021	0.040
		(LL)	0.524	0.912	1.584				0.015	0.023	0.038
	EN → Y0	(HZ)	1.069	1.981	3.366						
		(LZ)	0.561	1.039	1.830						
		(ZH)	0.989	1.772	3.049				0.011	0.021	0.041
		(ZL)	0.733	1.280	2.150				0.015	0.024	0.039
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN3535	A → Y0	(HH)	0.638	1.172	2.043				0.007	0.013	0.024
		(LL)	0.692	1.247	2.246				0.010	0.015	0.025
	EN → Y0	(HZ)	1.346	2.479	4.176						
		(LZ)	0.679	1.248	2.160						
		(ZH)	1.132	2.060	3.593				0.008	0.013	0.024
		(ZL)	0.854	1.547	2.660				0.010	0.015	0.025
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN3F35	A → Y0	(HH)	0.665	1.231	2.157				0.007	0.012	0.021
		(LL)	0.725	1.318	2.391				0.009	0.014	0.023
	EN → Y0	(HZ)	1.441	2.648	4.466						
		(LZ)	0.708	1.302	2.251						
		(ZH)	1.157	2.120	3.709				0.007	0.012	0.022
		(ZL)	0.862	1.576	2.719				0.009	0.015	0.024

INTERFACE BLOCK(5V)

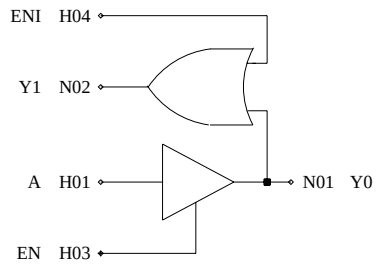
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			

[MEMO]

INTERFACE BLOCK (5V)

Function	CMOS LOW NOISE I/O BUFFER WITH EN(OR)				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BN7135				1	24
18mA	BN7535				2	24
24mA	BN7F35				2	24

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Y0	ENI	Y1
0	0	0
1	0	1
0	1	1
1	1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BN7135	A	7.1	Y1	34
	EN	4.2		
	ENI	2.1		
BN7535	A	7.1	Y1	34
	EN	4.2		
	ENI	2.1		
BN7F35	A	7.1	Y1	34
	EN	4.2		
	ENI	2.1		

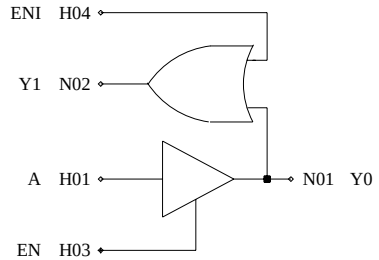
INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN7135	A → Y0	(HH)	2.565	5.089	9.558				0.023	0.040	0.069
		(LL)	1.786	3.825	7.040				0.022	0.035	0.057
	EN → Y0	(HZ)	1.833	3.131	4.762						
		(LZ)	1.210	1.903	3.016						
		(ZH)	2.539	5.105	9.601				0.023	0.040	0.069
		(ZL)	1.762	3.713	6.670				0.022	0.036	0.060
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN7535	A → Y0	(HH)	3.808	7.716	14.622				0.020	0.036	0.062
		(LL)	2.564	5.821	10.808				0.020	0.032	0.052
	EN → Y0	(HZ)	3.024	5.132	7.751						
		(LZ)	1.923	2.980	4.651						
		(ZH)	3.783	7.729	14.677				0.020	0.036	0.062
		(ZL)	2.555	5.554	10.116				0.019	0.033	0.055
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN7F35	A → Y0	(HH)	4.095	8.344	15.878				0.020	0.035	0.061
		(LL)	2.733	6.186	11.537				0.019	0.031	0.050
	EN → Y0	(HZ)	3.431	5.848	8.897						
		(LZ)	2.121	3.288	5.141						
		(ZH)	4.071	8.359	15.940				0.020	0.035	0.061
		(ZL)	2.666	5.858	10.709				0.019	0.032	0.054
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			

INTERFACE BLOCK (5V)

Function	TTL I/O BUFFER WITH EN(OR)				5V	
Block type						
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA	BN6U35	BN9U35			1	36
6mA	BN6C35	BN9C35			1	36
9mA	BN6335	BN9335			1	46
12mA	BN6135	BN9135			1	46
18mA	BN6535	BN9535			2	46
24mA	BN6F35	BN9F35			2	46

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BN6U35 to BN9U35	A	20.2	Y1	34
	EN	1.0		
	ENI	2.1		
BN6C35 to BN9C35	A	20.2	Y1	34
	EN	1.0		
	ENI	2.1		
BN6335 to BN9335	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN6135 to BN9135	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN6535 to BN9535	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		
BN6F35 to BN9F35	A	22.2	Y1	34
	EN	2.0		
	ENI	2.1		

INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BN6U35 to BN9U35	A → Y0	(HH)	0.644	1.162	2.163				0.058	0.103	0.190
		(LL)	0.775	1.179	1.916				0.074	0.104	0.164
	EN → Y0	(HZ)	0.885	1.655	2.878						
		(LZ)	0.526	0.991	1.745						
		(ZH)	1.125	2.067	3.631				0.058	0.103	0.190
		(ZL)	1.014	1.578	2.522				0.074	0.105	0.165
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN6C35 to BN9C35	A → Y0	(HH)	0.490	0.896	1.606				0.020	0.036	0.068
		(LL)	0.581	1.030	1.768				0.026	0.038	0.061
	EN → Y0	(HZ)	1.120	2.078	3.569						
		(LZ)	0.667	1.234	2.174						
		(ZH)	1.098	2.007	3.493				0.020	0.036	0.068
		(ZL)	0.864	1.486	2.468				0.026	0.038	0.061
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN6335 to BN9335	A → Y0	(HH)	0.457	0.791	1.352				0.016	0.028	0.054
		(LL)	0.499	0.854	1.468				0.020	0.030	0.049
	EN → Y0	(HZ)	0.986	1.818	3.100						
		(LZ)	0.529	0.979	1.728						
		(ZH)	0.964	1.717	2.938				0.015	0.028	0.054
		(ZL)	0.728	1.251	2.094				0.020	0.030	0.049
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN6135 to BN9135	A → Y0	(HH)	0.475	0.839	1.444				0.011	0.021	0.040
		(LL)	0.524	0.912	1.584				0.015	0.023	0.038
	EN → Y0	(HZ)	1.069	1.981	3.366						
		(LZ)	0.561	1.039	1.830						
		(ZH)	0.989	1.772	3.049				0.011	0.021	0.041
		(ZL)	0.733	1.280	2.150				0.015	0.024	0.039
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN6535 to BN9535	A → Y0	(HH)	0.638	1.172	2.043				0.007	0.013	0.024
		(LL)	0.692	1.247	2.246				0.010	0.015	0.025
	EN → Y0	(HZ)	1.346	2.479	4.176						
		(LZ)	0.679	1.248	2.160						
		(ZH)	1.132	2.060	3.593				0.008	0.013	0.024
		(ZL)	0.854	1.547	2.660				0.010	0.015	0.025
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BN6F35 to BN9F35	A → Y0	(HH)	0.665	1.231	2.157				0.007	0.012	0.021
		(LL)	0.725	1.318	2.391				0.009	0.014	0.023
	EN → Y0	(HZ)	1.441	2.648	4.466						
		(LZ)	0.708	1.302	2.251						
		(ZH)	1.157	2.120	3.709				0.007	0.012	0.022
		(ZL)	0.862	1.576	2.719				0.009	0.015	0.024

INTERFACE BLOCK(5V)

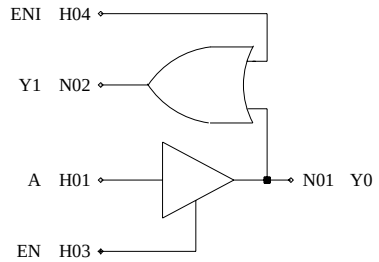
Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			

[MEMO]

INTERFACE BLOCK (5V)

Function	TTL LOW NOISE I/O BUFFER WITH EN(OR)				5V	
	Block type					
Drivability	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
1mA						
2mA						
3mA						
6mA						
9mA						
12mA	BNA135	BND135			1	20
18mA	BNA535	BND535			2	20
24mA	BNAF35	BNDF35			2	20

Logic Diagram



Truth Table

A	EN	Y0
0	1	0
1	1	1
X	0	Z

X:Irrelevant

Z:High Impedance

Y0	ENI	Y1
0	0	0
0	1	1
1	0	1
1	1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BNA135 to BND135	A	6.1	Y1	34
	EN	4.5		
	ENI	2.1		
BNA535 to BND535	A	6.1	Y1	34
	EN	4.5		
	ENI	2.1		
BNAF35 to BNDF35	A	6.1	Y1	34
	EN	4.5		
	ENI	2.1		

INTERFACE BLOCK(5V)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BNA135 to BND135	A → Y0	(HH)	2.232	4.527	8.678				0.019	0.035	0.061
		(LL)	1.987	4.111	7.806				0.024	0.038	0.062
	EN → Y0	(HZ)	2.391	4.855	7.978						
		(LZ)	1.483	2.516	4.052						
		(ZH)	2.156	4.442	8.516				0.019	0.035	0.062
		(ZL)	1.966	4.152	7.834				0.025	0.039	0.063
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BNA535 to BND535	A → Y0	(HH)	3.028	6.194	12.045				0.017	0.031	0.053
		(LL)	2.722	5.106	8.050				0.021	0.034	0.054
	EN → Y0	(HZ)	3.374	6.267	9.976						
		(LZ)	2.122	3.379	5.355						
		(ZH)	2.932	4.361	7.918				0.017	0.032	0.055
		(ZL)	2.686	5.054	8.242				0.021	0.034	0.057
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			
BNAF35 to BNDF35	A → Y0	(HH)	3.484	7.192	14.049				0.017	0.030	0.053
		(LL)	3.072	5.568	9.302				0.021	0.033	0.052
	EN → Y0	(HZ)	4.235	7.923	12.718						
		(LZ)	2.548	4.087	6.497						
		(ZH)	3.391	4.950	9.407				0.017	0.031	0.055
		(ZL)	2.980	5.438	9.017				0.021	0.034	0.057
	ENI → Y1	(HH)	0.207	0.300	0.438	0.008	0.015	0.025			
		(LL)	0.189	0.384	0.685	0.010	0.016	0.026			
	Y0 → Y1	(HH)	0.246	0.392	0.673	0.008	0.015	0.024			
		(LL)	0.230	0.455	0.817	0.010	0.016	0.026			

[MEMO]

CHAPTER 3

INTERFACE BLOCK

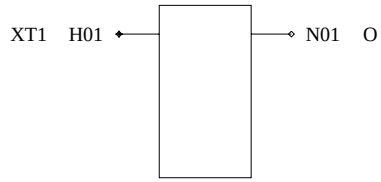
(OSCILLATOR)

3 - 1

OSCILLATION BLOCK

Function	OSCILLATOR INPUT BUFFER				
Block type					
Function				I/O cells	int. cells
Normal	OSI1			1	0
Oscillation stop function					
–					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSI1	XT1	-	O	2

Truth Table

XT1	O
0	0
1	1

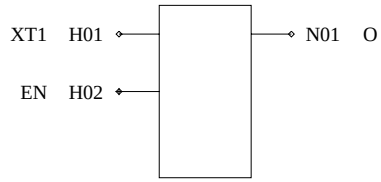
OSCILLATION BLOCK

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI1	XT1 → O (HH)	0.010	0.010	0.010	0.001	0.001	0.001			
	(LL)	0.010	0.010	0.010	0.002	0.002	0.002			

OSCILLATION BLOCK

Function	OSCILLATOR INPUT BUFFER FOR ENABLE				
Block type					
Function				I/O cells	int. cells
Normal					
Oscillation stop function	OSI2			1	0
–					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSI2	XT1	-	O	2
	EN	1.0		

Truth Table

XT1	EN	O	
0	0	0	
1	0	1	
1	1	1	
0	1	X	← Prohibition

X:Irrelevant

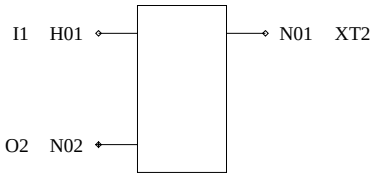
OSCILLATION BLOCK

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSI2	XT1 → O (HH)	0.010	0.010	0.010	0.001	0.001	0.001			
	(LL)	0.010	0.010	0.010	0.002	0.002	0.002			

OSCILLATION BLOCK

Function	OSCILLATOR OUTPUT BUFFER				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback					
Internal feedback	OSO1			1	4
Internal feedback Oscillation stop function					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSO1	I1	1.0	XT2	-
			O2	34

Truth Table

I1	XT2	O2
0	1	1
1	0	0

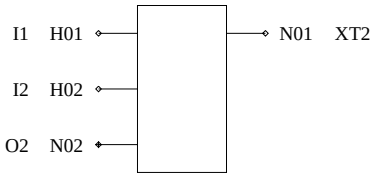
OSCILLATION BLOCK

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO1	I1 → XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
		(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1 → O2	(HL)	4.585	11.818	11.818	0.010	0.025	0.025			
		(LH)	4.582	13.548	13.548	0.008	0.025	0.025			

OSCILLATION BLOCK

Function	OSCILLATOR OUTPUT BUFFER				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback	OSO3			1	4
Internal feedback					
Internal feedback Oscillation stop function					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSO3	I1	1.0	XT2	-
	I2	1.0	O2	34

Truth Table

I1	I2	XT2	O2
0	0	1	1
1	0	0	0
X	1	0	0

X:Irrelevant

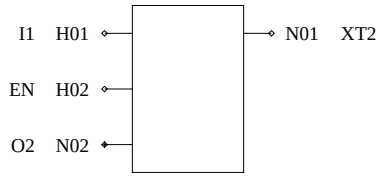
OSCILLATION BLOCK

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO3	I1 → XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
		(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1 → O2	(HL)	4.585	11.818	11.818	0.010	0.025	0.025			
		(LH)	4.582	13.548	13.548	0.008	0.025	0.025			

OSCILLATION BLOCK

Function	OSCILLATOR OUTPUT BUFFER				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback					
Internal feedback					
Internal feedback Oscillation stop function	OSO7			1	6

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSO7	I1	1.5	XT2	-
	EN	1.0	O2	34

Truth Table

I1	EN	XT2	O2	
0	0	1	1	
1	0	0	0	
1	1	0	0	
0	1	X	X	← Prohibition

X:Irrelevant

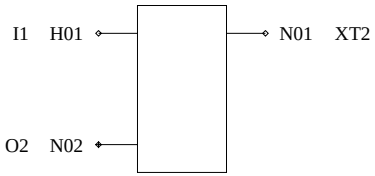
OSCILLATION BLOCK

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO7	I1 → XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
		(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1 → O2	(HL)	4.585	11.818	11.818	0.010	0.025	0.025			
		(LH)	4.582	13.548	13.548	0.008	0.025	0.025			

OSCILLATION BLOCK

Function	OSCILLATOR OUTPUT BUFFER				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback	OSO9			1	4
Internal feedback					
Internal feedback Oscillation stop function					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSO9	I1	1.0	XT2	-
			O2	34

Truth Table

I1	XT2	O2
0	1	1
1	0	0

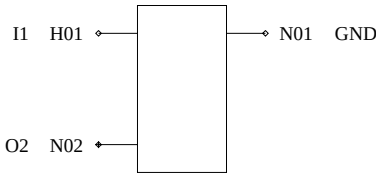
OSCILLATION BLOCK

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSO9	I1 → XT2	(HL)	0.010	0.010	0.010				0.001	0.001	0.001
		(LH)	0.010	0.010	0.010				0.001	0.001	0.001
	I1 → O2	(HL)	4.585	11.818	11.818	0.010	0.025	0.025			
		(LH)	4.582	13.548	13.548	0.008	0.025	0.025			

OSCILLATION BLOCK

Function	FEEDBACK RESISTOR FOR OSCILLATOR				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback					
Internal feedback	OSF1			1	0
Internal feedback Oscillation stop function					

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSF1	I1	1.0	GND	-
			O2	2

Truth Table

I1	O2
0	0
1	1

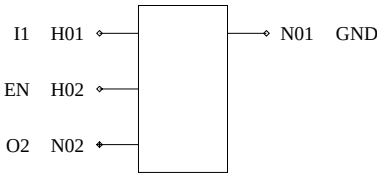
OSCILLATION BLOCK

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSF1	I1 → O2 (HH)	0.010	0.010	0.010	0.000	0.000	0.000			
	(LL)	0.010	0.010	0.010	0.000	0.000	0.000			

OSCILLATION BLOCK

Function	FEEDBACK RESISTOR FOR OSCILLATOR FOR ENABLE				
Block type					
Function	MHz range	kHz range		I/O cells	int. cells
External feedback					
Internal feedback					
Internal feedback Oscillation stop function	OSF3			1	2

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
OSF3	I1	1.5	GND	-
	EN	1.0	O2	2

Truth Table

I1	EN	O2	
0	0	0	
1	0	1	
X	1	Z	← Prohibition

X:Irrelevant

Z:High impedance

OSCILLATION BLOCK

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
OSF3	I1 → O2 (HH)	0.010	0.010	0.010	0.000	0.000	0.000			
	(LL)	0.010	0.010	0.010	0.000	0.000	0.000			

[MEMO]

CHAPTER 4

INTERFACE BLOCK

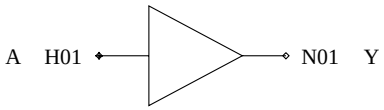
(HIGHSPEED SIGNALE TRANSMISSION)

4 - 1

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	3V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIXA		FUXA		1	24
Fail safe						
-						

Logic Diagram



Truth Table

A	Y
0	0
1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIXA to FUXA	A	-	Y	293

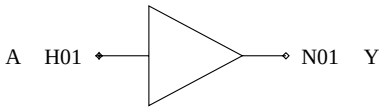
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIXA to FUXA	A → Y (HH)	0.324	0.409	0.552	0.001	0.002	0.004			
	(LL)	0.217	0.325	0.463	0.001	0.002	0.003			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	5V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIZA				1	24
Fail safe						
-						

Logic Diagram



Truth Table

A	Y
0	0
1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIZA	A	-	Y	296

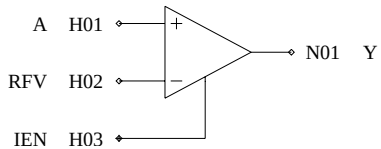
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIZA	A → Y (HH)	0.333	0.531	0.988	0.001	0.002	0.004			
	(LL)	0.204	0.370	0.662	0.001	0.002	0.003			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	GTL INPUT BUFFER WITH EN					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIR1				1	8
Fail safe						
-						

Logic Diagram



Truth Table

A	IEN	Y
1	1	1
0	1	0
X	0	1

X:Irrelevant

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIR1	A	-	Y	22
	RFV	0.0		
	IEN	1.0		

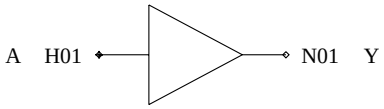
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIR1	A → Y	(HH)	0.416	0.996	2.337	0.014	0.029	0.058			
		(LL)	0.722	1.325	2.787	0.026	0.033	0.056			
	RFV → Y	(HL)	0.010	0.010	0.010	0.047	0.047	0.047			
		(LH)	0.010	0.010	0.010	0.035	0.035	0.035			
	IEN → Y	(HL)	0.383	0.781	1.644	0.023	0.027	0.043			
		(LH)	0.204	0.387	0.768	0.012	0.023	0.044			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	GTL INPUT BUFFER FOR REFERENCE VOLTAGE					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIP1				1	
Fail safe						
-						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIP1	A	-	Y	12

Truth Table

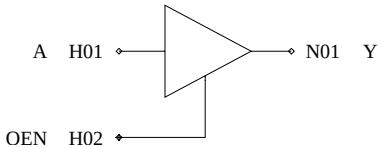
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIP1	A → Y (HH)	0.010	0.010	0.010	0.047	0.047	0.047			
	(LL)	0.010	0.010	0.010	0.035	0.035	0.035			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	GTL OUTPUT BUFFER WITH ENB					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	EGTL				2	18
Fail safe						
-						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
EGTL	A	25.7	Y	-
	OEN	1.0		

Truth Table

A	OEN	Y
0	1	0
1	1	Z*
X	0	Z*

X:Irrelevant
Z:High Impedance
*:Open drain function connect a pull-up resistor to get a high level.

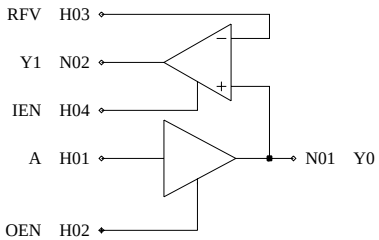
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
EGTL	A → Y	(LZ)	0.971	1.613	3.078						
		(ZL)	0.494	0.936	1.888				0.003	0.005	0.009
	OEN → Y	(LZ)	1.335	2.289	4.353						
		(ZL)	0.715	1.315	2.597				0.003	0.005	0.009

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	GTL I/O BUFFER					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	BG0W				2	26
Fail safe						
-						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
BG0W	A	25.7	Y1	22
	OEN	1.0		
	RFV	0.0		
	IEN	1.0		

Truth Table

A	OEN	Y0
0	1	0
1	1	Z*
X	0	Z*

Y0	OEN	Y1
0	1	0
1	1	1
X	0	1

X:Irrelevant
Z:High Impedance
*:Open drain function connect a pull-up resistor to get a high level.

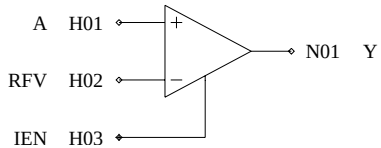
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
BG0W	A → Y0	(LZ)	0.972	1.614	3.079						
		(ZL)	0.495	0.936	1.889				0.003	0.005	0.009
	OEN → Y0	(LZ)	1.336	2.289	4.354						
		(ZL)	0.715	1.315	2.597				0.003	0.005	0.009
	RFV → Y1	(HL)	0.010	0.010	0.010	0.047	0.047	0.047			
		(LH)	0.010	0.010	0.010	0.035	0.035	0.035			
	IEN → Y1	(HL)	0.383	0.781	1.644	0.023	0.027	0.043			
		(LH)	0.204	0.387	0.768	0.012	0.023	0.044			
	Y0 → Y1	(HH)	0.425	1.009	2.344	0.014	0.029	0.058			
		(LL)	0.727	1.322	2.790	0.026	0.033	0.056			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	P-ECL INPUT BUFFER WITH EN					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIX1				1	26
Fail safe	FIX2				1	26
-						

Logic Diagram



Truth Table

A	IEN	Y
1	1	1
0	1	0
X	0	0

X:Irrelevant

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIX1	A	-	Y	56
	RFV	1.0		
	IEN	1.0		
FIX2	A	-	Y	56
	RFV	1.0		
	IEN	1.0		

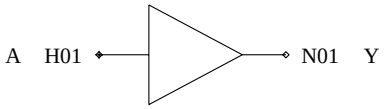
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIX1	A → Y	(HH)	0.626	1.193	2.418	0.005	0.009	0.015			
		(LL)	0.567	1.120	2.422	0.006	0.009	0.016			
	RFV → Y	(HL)	0.020	0.020	0.020	0.000	0.000	0.000			
		(LH)	0.020	0.020	0.020	0.000	0.000	0.000			
	IEN → Y	(HL)	0.993	2.157	4.172	0.006	0.009	0.016			
		(LH)	0.576	1.008	1.676	0.005	0.009	0.015			
FIX2	A → Y	(HH)	0.626	1.193	2.418	0.005	0.009	0.015			
		(LL)	0.567	1.120	2.422	0.006	0.009	0.016			
	RFV → Y	(HL)	0.020	0.020	0.020	0.000	0.000	0.000			
		(LH)	0.020	0.020	0.020	0.000	0.000	0.000			
	IEN → Y	(HL)	0.993	2.157	4.172	0.006	0.009	0.016			
		(LH)	0.576	1.008	1.676	0.005	0.009	0.015			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	P-ECL INPUT BUFFER FOR REFERENCE VOLTAGE					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FIP3				1	0
Fail safe	FIP4				1	0
-						

Logic Diagram



Truth Table

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FIP3	A	-	Y	500
FIP4	A	-	Y	500

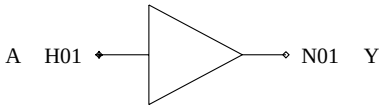
INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FIP3	A → Y	(HH)	0.020	0.020	0.020	0.000	0.000	0.000			
		(LL)	0.020	0.020	0.020	0.000	0.000	0.000			
FIP4	A → Y	(HH)	0.020	0.020	0.020	0.000	0.000	0.000			
		(LL)	0.020	0.020	0.020	0.000	0.000	0.000			

INTERFACE BLOCK (HIGH SPEED SIGNALE TRANSMISSION)

Function	P-ECL OUTPUT BUFFER					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FO0G				1	4
Fail safe						
-						

Logic Diagram



Truth Table

A	Y
0	0
1	1

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FO0G	A	8.1	Y	-

INTERFACE BLOCK(HIGHSPEED SIGNALE TRANSMISSION)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FO0G	A → Y	(HH)	0.249	0.341	0.461				0.021	0.022	0.022
		(LL)	0.229	0.345	0.461				0.023	0.031	0.042

[MEMO]

CHAPTER 5

INTERFACE BLOCK

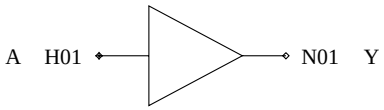
(DIGITAL PLL)

5 - 1

INTERFACE BLOCK (DIGITAL PLL)

Function	3V INPUT BUFFER REFERRENCE CLOCK					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FI0P				1	3
Fail safe						
-						

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FI0P	A	-	Y	34

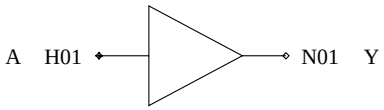
INTERFACE BLOCK(DIGITAL PLL)

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FI0P	A → Y (HH)	0.646	0.312	0.924	0.011	0.015	0.029			
	(LL)	0.010	0.232	0.641	0.012	0.016	0.030			

INTERFACE BLOCK (DIGITAL PLL)

Function	5V INPUT BUFFER REFERRENCE CLOCK					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	FI0Q				1	3
Fail safe						
-						

Logic Diagram



Truth Table

A	Y
1	1
0	0

Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
FI0Q	A	-	Y	32

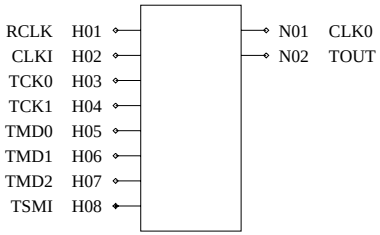
INTERFACE BLOCK(DIGITAL PLL)

Block type	Switching speed								
	Path	t_{LD0} (ns)			t_1			T		
	IN → OUT	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FI0Q	A → Y (HH)	0.280	0.400	1.022	0.008	0.015	0.028			
	(LL)	0.176	0.278	0.638	0.010	0.016	0.027			

INTERFACE BLOCK (DIGITAL PLL)

Function	DIGITAL PLL(25MHZ TO 50MHZ)					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	F9E6					1900
-						
-						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
F9E6	RCLK	1.0	CLK0	53
	CLKI	1.0	TOUT	26
	TCK0	1.0		
	TCK1	1.0		
	TMD0	1.0		
	TMD1	1.0		
	TMD2	1.0		
	TSMI	1.0		

Truth Table

RCLK	CLKI	TCK0	TCK1	TMD0	TMD1	TMD2	TSMI	CLK0	TOUT	Function	
A	A	X	X	0	0	0	X	A	LOCK	*1	
A	X	X	X	1	0	0	X	0	0	*2	
A	X	X	X	0	1	0	X	A	0	*3	
A	X	X	X	0	0	1	X	0	0	*4	
X	X	X	1	0	1	1	X	X	X		← Prohibition

X:Irrelevant
*1:PLL mode
*2:Reset mode
*3:Through Path mode
*4:Stop mode

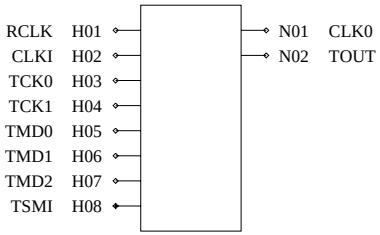
INTERFACE BLOCK(DIGITAL PLL)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
F9E6	RCLK → CLK0	(HH)	1.807	7.804	7.804	0.003	0.020	0.020			
		(LL)	1.683	6.917	6.917	0.002	0.013	0.013			

INTERFACE BLOCK (DIGITAL PLL)

Function	DIGITAL PLL(50MHZ TO 75MHZ)					
Block type						
Function	no resistor	with 50 kΩ P/D	with 50 kΩ P/U	with 5 kΩ P/U	I/O cells	int. cells
Normal	F9E8					1596
-						
-						

Logic Diagram



Block type	Input		Output	
	Symbol	Fan-in	Symbol	Fan-out
F9E8	RCLK	1.0	CLK0	53
	CLKI	1.0	TOUT	26
	TCK0	1.0		
	TCK1	1.0		
	TMD0	1.0		
	TMD1	1.0		
	TMD2	1.0		
	TSMI	1.0		

Truth Table

RCLK	CLKI	TCK0	TCK1	TMD0	TMD1	TMD2	TSMI	CLK0	TOUT	Function	
A	A	X	X	0	0	0	X	A	LOCK	*1	
A	X	X	X	1	0	0	X	0	0	*2	
A	X	X	X	0	1	0	X	A	0	*3	
A	X	X	X	0	0	1	X	0	0	*4	
X	X	X	1	0	1	1	X	X	X		← Prohibition

X:Irrelevant
*1:PLL mode
*2:Reset mode
*3:Through Path mode
*4:Stop mode

INTERFACE BLOCK(DIGITAL PLL)

Block type	Switching speed									
	Path		t_{LD0} (ns)			t_1			T		
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
F9E8	RCLK → CLK0	(HH)	1.580	6.510	6.510	0.003	0.020	0.020			
		(LL)	1.716	7.335	7.335	0.002	0.013	0.013			

[MEMO]

CHAPTER 6

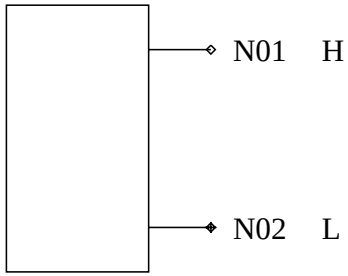
FUNCTION BLOCK

6 - 1

FUNCTION BLOCK

Function	H,L LEVEL GENERATOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
-	F091	1					
-							
-							
-							

Logic Diagram



Truth Table

H	L
1	0

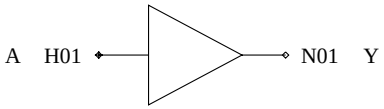
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t_{LD0} (ns)			t_1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F091											H L	103 103

FUNCTION BLOCK

Function	INTERFACE BLOCK FOR OSCILLATOR BUFFER					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
-	F093	1					
-							
-							
-							

Logic Diagram



Truth Table

A	Y
0	0
1	1

F093 is used oscillator blocks.

FUNCTION BLOCK

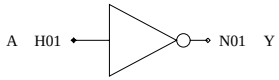
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F093	A → Y	(HH)	0.010	0.020	0.010	0.000	0.000	0.000	A	2.0	Y	4
		(LL)	0.010	0.020	0.010	0.000	0.000	0.000				

FUNCTION BLOCK

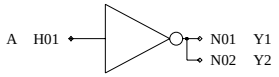
Function	INVERTER						SSI Family					
Block type	Single output type						Multi output type					
Drivability	Name	cells					Name	cells				
Low Power	L101	1										
x1	F101	1										
x2	F102	2										
x3	F143	3					F103	3				
x4	F144	4					F104	4				
x5												
x6												
x8	F148	12					F108	12				
x12												

Logic Diagram

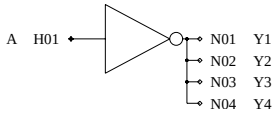
Single output type



Multi output type



Multi output type



FUNCTION BLOCK

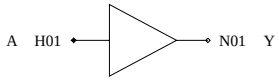
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L101	A → Y	(HL)	0.078	0.111	0.155	0.017	0.027	0.045	A	1.0	Y	11
		(LH)	0.076	0.111	0.153	0.025	0.046	0.073				
F101	A → Y	(HL)	0.073	0.106	0.143	0.010	0.016	0.025	A	2.0	Y	23
		(LH)	0.068	0.100	0.135	0.013	0.023	0.036				
F102	A → Y	(HL)	0.069	0.100	0.139	0.005	0.007	0.012	A	4.1	Y	46
		(LH)	0.065	0.094	0.127	0.006	0.011	0.018				
F143	A → Y	(HL)	0.069	0.099	0.138	0.003	0.005	0.008	A	6.1	Y	70
		(LH)	0.065	0.094	0.125	0.004	0.008	0.012				
F103	A → Yn	(HL)	0.069	0.099	0.138	0.003	0.005	0.008	A	6.1	Y0	35
		(LH)	0.065	0.094	0.125	0.004	0.008	0.012			Y1	35
	(n = 0,1)											
F144	A → Y	(HL)	0.066	0.098	0.135	0.002	0.004	0.006	A	8.1	Y	93
		(LH)	0.063	0.092	0.121	0.003	0.006	0.009				
F104	A → Yn	(HL)	0.066	0.098	0.135	0.002	0.004	0.006	A	8.1	Y0	46
		(LH)	0.063	0.092	0.121	0.003	0.006	0.009			Y1	46
	(n = 0,1)											
F148	A → Y	(HL)	0.303	0.514	0.825	0.001	0.002	0.003	A	2.0	Y	179
		(LH)	0.291	0.507	0.836	0.002	0.003	0.005				
F108	A → Yn	(HL)	0.303	0.514	0.825	0.001	0.002	0.003	A	2.0	Y0	44
		(LH)	0.291	0.507	0.836	0.002	0.003	0.005			Y1	44
	(n = 0,1,2,3)										Y2	44
											Y3	44

FUNCTION BLOCK

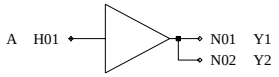
Function	BUFFER								SSI Family	
Block type	Single output type						Multi output type			
Drivability	Name	cells					Name	cells		
Low Power	L111	1								
x1	F111	2								
x2	F112	3								
x3	F153	4					F113	4		
x4	F154	5					F114	5		
x5										
x6										
x8	F158	11					F118	11		
x12										

Logic Diagram

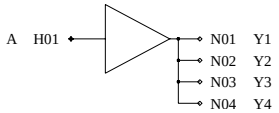
Single output type



Multi output type



Multi output type



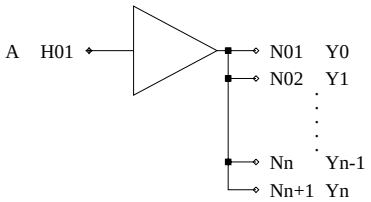
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L111	A → Y	(HH)	0.120	0.205	0.320	0.025	0.045	0.073	A	1.0	Y	11
		(LL)	0.143	0.238	0.382	0.016	0.027	0.044				
F111	A → Y	(HH)	0.122	0.206	0.307	0.012	0.023	0.036	A	2.0	Y	23
		(LL)	0.132	0.220	0.342	0.010	0.016	0.025				
F112	A → Y	(HH)	0.151	0.247	0.359	0.006	0.011	0.018	A	2.0	Y	46
		(LL)	0.163	0.278	0.438	0.005	0.008	0.013				
F153	A → Y	(HH)	0.179	0.285	0.414	0.004	0.008	0.012	A	2.0	Y	69
		(LL)	0.189	0.340	0.530	0.003	0.005	0.009				
F113	A → Yn	(HH)	0.179	0.285	0.414	0.004	0.008	0.012	A	2.0	Y0	34
		(LL)	0.189	0.340	0.530	0.003	0.005	0.009			Y1	34
	(n = 0,1)											
F154	A → Y	(HH)	0.217	0.335	0.488	0.003	0.006	0.010	A	2.0	Y	89
		(LL)	0.214	0.395	0.622	0.003	0.004	0.008				
F114	A → Yn	(HH)	0.217	0.335	0.488	0.003	0.006	0.010	A	2.0	Y0	44
		(LL)	0.214	0.395	0.622	0.003	0.004	0.008			Y1	44
	(n = 0,1)											
F158	A → Y	(HH)	0.165	0.267	0.384	0.002	0.003	0.005	A	6.1	Y	185
		(LL)	0.171	0.304	0.468	0.001	0.002	0.004				
F118	A → Yn	(HH)	0.165	0.267	0.384	0.002	0.003	0.005	A	6.1	Y0	46
		(LL)	0.171	0.304	0.468	0.001	0.002	0.004			Y1	46
	(n = 0,1,2,3)										Y2	46
											Y3	46

FUNCTION BLOCK

Function	CLOCK DRIVER						SSI Family					
Block type	Standard type (Middle scale circuit)						Double type (Large scale circuit)					
Drivability	Name	cells					Name	cells				
x1	FCK1	40										
x2	FCK2	80										
x3	FCK3	120										
x4	FCK4	160										
x5	FCK5	200										
-												
-												
-												

Logic Diagram



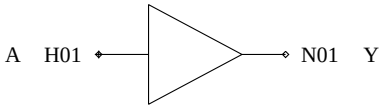
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
FCK1	A → Yn	(HH)	0.537	0.949	1.571	0.000	0.001	0.001	A	2.0	Y0	31
		(LL)	0.524	0.936	1.573	0.000	0.001	0.001			Y1	31
	(n = 0 to 17)										:	:
											Y16	31
											Y17	31
FCK2	A → Yn	(HH)	0.527	0.938	1.557	0.000	0.000	0.001	A	6.8	Y0	31
		(LL)	0.518	0.917	1.545	0.000	0.000	0.000			Y1	31
	(n = 0 to 35)										:	:
											Y34	31
											Y35	31
FCK3	A → Yn	(HH)	0.523	0.934	1.552	0.000	0.000	0.000	A	11.6	Y0	32
		(LL)	0.515	0.910	1.531	0.000	0.000	0.000			Y1	32
	(n = 0 to 53)										:	:
											Y52	32
											Y53	32
FCK4	A → Yn	(HH)	0.522	0.932	1.547	0.000	0.000	0.000	A	16.4	Y0	32
		(LL)	0.511	0.903	1.522	0.000	0.000	0.000			Y1	32
	(n = 0 to 71)										:	:
											Y70	32
											Y71	32
FCK5	A → Yn	(HH)	0.521	0.931	1.545	0.000	0.000	0.000	A	21.2	Y0	33
		(LL)	0.510	0.901	1.516	0.000	0.000	0.000			Y1	33
	(n = 0 to 89)										:	:
											Y88	33
											Y89	33

FUNCTION BLOCK

Function	CLOCK DRIVER SINGLE OUT						SSI Family					
Block type	Standard type (Middle scale circuit)						Double type (Large scale circuit)					
Drivability	Name	cells					Name	cells				
x1	FCKA	40										
x2	FCKB	80										
x3	FCKC	120										
x4	FCKD	160										
x5	FCKE	200										
-												
-												
-												

Logic Diagram



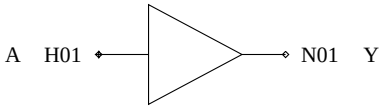
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
FCKA	A → Y	(HH)	0.537	0.949	1.571	0.000	0.001	0.001	A	2.0	Y	571
		(LL)	0.524	0.936	1.573	0.000	0.001	0.001				
FCKB	A → Y	(HH)	0.527	0.938	1.557	0.000	0.000	0.001	A	6.8	Y	1145
		(LL)	0.518	0.917	1.545	0.000	0.000	0.000				
FCKC	A → Y	(HH)	0.523	0.934	1.552	0.000	0.000	0.000	A	11.6	Y	1739
		(LL)	0.515	0.910	1.531	0.000	0.000	0.000				
FCKD	A → Y	(HH)	0.522	0.932	1.547	0.000	0.000	0.000	A	16.4	Y	2352
		(LL)	0.511	0.903	1.522	0.000	0.000	0.000				
FCKE	A → Y	(HH)	0.521	0.931	1.545	0.000	0.000	0.000	A	21.2	Y	2994
		(LL)	0.510	0.901	1.516	0.000	0.000	0.000				

FUNCTION BLOCK

Function	CLOCK TREE SYNTHESIS DRIVER						SSI Family					
Block type	Standard type (Middle scale circuit)						Double type (Large scale circuit)					
Drivability	Name	cells					Name	cells				
x1	FC42	132					FC44	340				
x2												
x3	FC82	396					FC84	1020				
x4												
x5												
-												
-												
-												

Logic Diagram



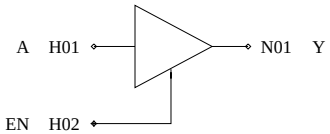
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
FC42	A → Y	(HH)	0.645	1.591	1.629	0.000	0.000	0.000	A	8.1	Y	2988
		(LL)	0.861	2.456	2.494	0.000	0.000	0.000				
FC82	A → Y	(HH)	0.535	1.033	1.640	0.000	0.000	0.000	A	2.0	Y	5747
		(LL)	0.560	1.136	1.743	0.000	0.000	0.000				
FC44	A → Y	(HH)	0.337	0.817	0.892	0.000	0.000	0.000	A	8.1	Y	5976
		(LL)	0.364	0.925	1.001	0.000	0.000	0.000				
FC84	A → Y	(HH)	0.945	1.756	2.969	0.000	0.000	0.000	A	2.0	Y	11495
		(LL)	0.949	1.769	2.983	0.000	0.000	0.000				

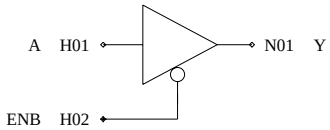
FUNCTION BLOCK

Function	3-STATE BUFFER							SSI Family					
Block type	Buffer type						Inverter type						
	with EN		with ENB				with EN		with ENB				
Drivability	Name	cells	Name	cells			Name	cells	Name	cells			
Low Power													
x1	F531	5	F532	5									
x2													
x3													
x4													

Logic Diagram
for "Buffer with EN"



Logic Diagram
for "Buffer with ENB"



Logic Diagram
for "Inverter with EN"

Logic Diagram
for "Inverter with ENB"

Truth Table

With EN

A	EN	Y	Y*
0	1	0	1
1	1	1	0
X	0	Z	Z

With ENB

A	ENB	Y	Y*
0	0	0	1
1	0	1	0
X	1	Z	Z

X:Irrelevant

Z:High Impedance

*:Inverter type

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F531	A → Y		(HH)	0.189	0.325	0.506	0.013	0.023	0.037	A	2.1	Y	22
			(LL)	0.258	0.496	0.878	0.010	0.016	0.026	EN	1.0		
	EN → Y		(HZ)	0.398	0.671	1.039				Y	1.0		
			(LZ)	0.282	0.458	0.727							
			(ZH)	0.318	0.582	0.966	0.013	0.023	0.037				
			(ZL)	0.338	0.674	1.167	0.010	0.016	0.026				
F532	A → Y		(HH)	0.189	0.324	0.506	0.013	0.023	0.037	A	2.1	Y	22
			(LL)	0.259	0.498	0.881	0.010	0.016	0.026	ENB	1.0		
	ENB → Y		(HZ)	0.324	0.527	0.763				Y	1.0		
			(LZ)	0.319	0.533	0.837							
			(ZH)	0.275	0.497	0.835	0.013	0.023	0.037				
			(ZL)	0.421	0.827	1.451	0.010	0.016	0.026				

FUNCTION BLOCK

Function	DELAY GATE										SSI Family	
Block type	Standard type											
	Normal		High speed									
Drivability	Name	cells	Name	cells								
-	F131	6										
-	F132	10										
-												
-												

Logic Diagram

Truth Table

A	Y
0	0
1	1

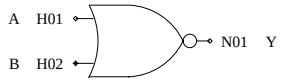
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F131	A → Y	(HH)	1.065	2.208	3.965	0.013	0.024	0.038	A	1.0	Y	21
		(LL)	1.001	2.005	3.524	0.011	0.018	0.030				
F132	A → Y	(HH)	2.084	4.390	7.931	0.013	0.024	0.038	A	1.0	Y	21
		(LL)	2.019	4.189	7.497	0.011	0.019	0.030				

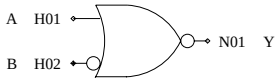
FUNCTION BLOCK

Function	2-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L202	1	L202N1	2								
x1	F202	2	F202N1	3								
x2	F222	4	F222N1	5								
x4												
x8	F282	6	F282N1	7								
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

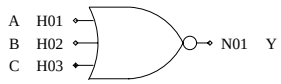
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L202	A → Y	(HL)	0.087	0.122	0.177	0.016	0.026	0.043	A	1.0	Y	5
		(LH)	0.110	0.181	0.282	0.043	0.088	0.147	B	1.0		
	B → Y	(HL)	0.095	0.134	0.191	0.016	0.026	0.043				
		(LH)	0.099	0.189	0.320	0.043	0.088	0.147				
F202	A → Y	(HL)	0.089	0.130	0.177	0.009	0.014	0.022	A	2.1	Y	10
		(LH)	0.099	0.179	0.279	0.022	0.044	0.073	B	2.1		
	B → Y	(HL)	0.089	0.130	0.177	0.009	0.014	0.022				
		(LH)	0.099	0.179	0.279	0.022	0.044	0.073				
F222	A → Y	(HL)	0.083	0.124	0.167	0.004	0.007	0.011	A	4.2	Y	22
		(LH)	0.093	0.164	0.258	0.011	0.022	0.037	B	4.2		
	B → Y	(HL)	0.083	0.124	0.167	0.004	0.007	0.011				
		(LH)	0.093	0.164	0.258	0.011	0.022	0.037				
F282	A → Y	(HL)	0.272	0.492	0.810	0.002	0.004	0.006	A	1.0	Y	91
		(LH)	0.341	0.622	1.073	0.003	0.006	0.009	B	1.0		
	B → Y	(HL)	0.277	0.496	0.820	0.002	0.004	0.006				
		(LH)	0.328	0.629	1.111	0.003	0.006	0.009				
L202N1	A → Y	(HL)	0.075	0.112	0.156	0.017	0.026	0.043	A	1.0	Y	5
		(LH)	0.093	0.148	0.221	0.044	0.088	0.147	B	1.0		
	B → Y	(HH)	0.151	0.283	0.452	0.044	0.088	0.147				
		(LL)	0.147	0.245	0.389	0.016	0.026	0.043				
F202N1	A → Y	(HL)	0.081	0.123	0.169	0.009	0.014	0.022	A	2.0	Y	11
		(LH)	0.090	0.158	0.248	0.022	0.044	0.074	B	1.0		
	B → Y	(HH)	0.170	0.306	0.478	0.022	0.044	0.074				
		(LL)	0.175	0.296	0.484	0.009	0.014	0.023				
F222N1	A → Y	(HL)	0.073	0.115	0.164	0.004	0.007	0.011	A	4.1	Y	22
		(LH)	0.090	0.149	0.232	0.011	0.022	0.037	B	1.0		
	B → Y	(HH)	0.224	0.373	0.575	0.011	0.022	0.037				
		(LL)	0.231	0.408	0.688	0.005	0.007	0.012				
F282N1	A → Y	(HL)	0.272	0.491	0.809	0.002	0.004	0.006	A	1.0	Y	90
		(LH)	0.341	0.622	1.073	0.003	0.006	0.009	B	1.0		
	B → Y	(HH)	0.388	0.751	1.301	0.003	0.006	0.009				
		(LL)	0.337	0.608	1.033	0.002	0.004	0.006				

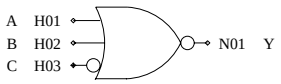
FUNCTION BLOCK

Function	3-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L203	2	L203N1	2	L203N2	3						
x1	F203	3	F203N1	4	F203N2	4						
x2	F223	6	F223N1	7	F223N2	7						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

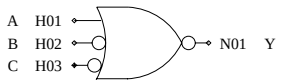
Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

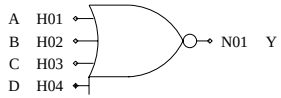
FUNCTION BLOCK

Block type	Path		Switching speed t_{LD0} (ns)			Switching speed t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L203	A → Y	(HL)	0.086	0.122	0.176	0.017	0.026	0.043	A	1.0	Y	3
		(LH)	0.135	0.226	0.366	0.065	0.134	0.225	B	1.0		
	B → Y	(HL)	0.098	0.139	0.191	0.017	0.027	0.045	C	1.0		
		(LH)	0.142	0.278	0.475	0.066	0.134	0.225				
	C → Y	(HL)	0.103	0.144	0.207	0.016	0.026	0.043				
		(LH)	0.159	0.338	0.574	0.066	0.134	0.225				
F203	A → Y	(HL)	0.100	0.138	0.199	0.008	0.013	0.022	A	2.1	Y	5
		(LH)	0.156	0.298	0.491	0.033	0.068	0.113	B	2.1		
	B → Y	(HL)	0.100	0.140	0.196	0.008	0.013	0.022	C	2.1		
		(LH)	0.150	0.298	0.495	0.033	0.068	0.113				
	C → Y	(HL)	0.101	0.141	0.198	0.009	0.014	0.022				
		(LH)	0.156	0.298	0.493	0.033	0.068	0.113				
F223	A → Y	(HL)	0.093	0.138	0.187	0.004	0.007	0.011	A	4.2	Y	12
		(LH)	0.145	0.282	0.457	0.017	0.034	0.057	B	4.2		
	B → Y	(HL)	0.095	0.141	0.189	0.004	0.007	0.011	C	4.2		
		(LH)	0.139	0.276	0.461	0.017	0.034	0.057				
	C → Y	(HL)	0.093	0.138	0.186	0.004	0.007	0.011				
		(LH)	0.145	0.282	0.455	0.017	0.034	0.057				
L203N1	A → Y	(HL)	0.082	0.124	0.175	0.017	0.026	0.043	A	1.0	Y	3
		(LH)	0.134	0.225	0.359	0.066	0.135	0.226	B	1.0		
	B → Y	(HL)	0.096	0.141	0.192	0.017	0.027	0.045	C	1.0		
		(LH)	0.140	0.281	0.472	0.066	0.135	0.226				
	C → Y	(HH)	0.217	0.437	0.725	0.066	0.134	0.225				
		(LL)	0.158	0.263	0.419	0.017	0.028	0.045				
F203N1	A → Y	(HL)	0.086	0.129	0.176	0.009	0.014	0.022	A	2.0	Y	6
		(LH)	0.126	0.242	0.390	0.032	0.067	0.113	B	2.1		
	B → Y	(HL)	0.094	0.140	0.190	0.009	0.014	0.022	C	1.0		
		(LH)	0.140	0.292	0.479	0.033	0.067	0.112				
	C → Y	(HH)	0.222	0.406	0.644	0.033	0.067	0.112				
		(LL)	0.186	0.318	0.517	0.009	0.014	0.023				
F223N1	A → Y	(HL)	0.086	0.135	0.190	0.004	0.007	0.011	A	4.2	Y	11
		(LH)	0.151	0.288	0.467	0.017	0.034	0.057	B	4.2		
	B → Y	(HL)	0.088	0.139	0.196	0.004	0.007	0.011	C	1.0		
		(LH)	0.144	0.282	0.474	0.017	0.034	0.057				
	C → Y	(HH)	0.293	0.515	0.816	0.017	0.034	0.057				
		(LL)	0.245	0.435	0.738	0.005	0.007	0.012				
L203N2	A → Y	(HL)	0.082	0.124	0.175	0.017	0.026	0.043	A	1.0	Y	3
		(LH)	0.133	0.225	0.359	0.066	0.135	0.226	B	1.0		
	B → Y	(HH)	0.209	0.408	0.668	0.066	0.135	0.226	C	1.0		
		(LL)	0.154	0.257	0.408	0.017	0.027	0.045				
	C → Y	(HH)	0.246	0.476	0.775	0.066	0.135	0.226				
		(LL)	0.167	0.276	0.443	0.017	0.028	0.045				
F203N2	A → Y	(HL)	0.085	0.128	0.176	0.009	0.014	0.022	A	2.0	Y	6
		(LH)	0.127	0.243	0.393	0.032	0.067	0.113	B	1.0		
	B → Y	(HH)	0.245	0.460	0.733	0.033	0.067	0.112	C	1.0		
		(LL)	0.192	0.327	0.533	0.009	0.014	0.023				
	C → Y	(HH)	0.223	0.409	0.647	0.033	0.067	0.113				
		(LL)	0.185	0.315	0.512	0.009	0.014	0.023				
F223N2	A → Y	(HL)	0.087	0.135	0.188	0.004	0.007	0.011	A	4.2	Y	11
		(LH)	0.152	0.290	0.470	0.017	0.034	0.057	B	1.0		
	B → Y	(HH)	0.284	0.513	0.815	0.017	0.034	0.057	C	1.0		
		(LL)	0.244	0.430	0.729	0.004	0.007	0.012				
	C → Y	(HH)	0.295	0.521	0.823	0.017	0.034	0.057				
		(LL)	0.245	0.434	0.738	0.005	0.007	0.012				

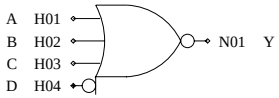
FUNCTION BLOCK

Function	4-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L204	2	L204N1	3	L204N2	3						
x1	F204	4	F204N1	5	F204N2	5						
x2	F224	8	F224N1	9	F224N2	9						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

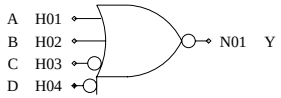
Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
L204	A → Y	(HL)	0.096	0.138	0.195	0.017	0.027	0.045	A	1.0	Y	1
		(LH)	0.177	0.319	0.541	0.084	0.177	0.299	B	1.0		
	B → Y	(HL)	0.107	0.152	0.210	0.017	0.027	0.045	C	1.0		
		(LH)	0.200	0.407	0.712	0.084	0.177	0.298	D	1.0		
	C → Y	(HL)	0.116	0.162	0.230	0.017	0.027	0.045				
		(LH)	0.249	0.536	0.923	0.085	0.177	0.298				
	D → Y	(HL)	0.113	0.160	0.227	0.016	0.026	0.044				
		(LH)	0.249	0.548	0.953	0.085	0.177	0.298				
F204	A → Y	(HL)	0.244	0.445	0.722	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.338	0.638	1.093	0.012	0.023	0.036	B	1.0		
	B → Y	(HL)	0.256	0.457	0.739	0.009	0.014	0.023	C	1.0		
		(LH)	0.325	0.645	1.130	0.012	0.023	0.036	D	1.0		
	C → Y	(HL)	0.255	0.473	0.766	0.009	0.014	0.023				
		(LH)	0.322	0.599	1.033	0.012	0.023	0.036				
	D → Y	(HL)	0.266	0.485	0.787	0.009	0.014	0.023				
		(LH)	0.309	0.605	1.070	0.012	0.023	0.036				
F224	A → Y	(HL)	0.100	0.144	0.200	0.004	0.007	0.011	A	4.3	Y	7
		(LH)	0.196	0.392	0.667	0.021	0.044	0.075	B	4.3		
	B → Y	(HL)	0.104	0.152	0.208	0.004	0.007	0.011	C	4.3		
		(LH)	0.205	0.430	0.738	0.021	0.044	0.075	D	4.3		
	C → Y	(HL)	0.104	0.152	0.208	0.004	0.007	0.011				
		(LH)	0.206	0.429	0.738	0.021	0.044	0.075				
	D → Y	(HL)	0.100	0.144	0.200	0.004	0.007	0.011				
		(LH)	0.196	0.393	0.667	0.021	0.044	0.075				
L204N1	A → Y	(HL)	0.083	0.124	0.175	0.017	0.026	0.043	A	1.0	Y	2
		(LH)	0.142	0.242	0.394	0.084	0.177	0.299	B	1.0		
	B → Y	(HL)	0.097	0.142	0.196	0.017	0.027	0.045	C	1.0		
		(LH)	0.164	0.335	0.575	0.085	0.177	0.299	D	1.0		
	C → Y	(HL)	0.105	0.151	0.207	0.017	0.027	0.045				
		(LH)	0.207	0.457	0.775	0.085	0.177	0.299				
	D → Y	(HH)	0.296	0.602	1.009	0.085	0.176	0.299				
		(LL)	0.158	0.262	0.418	0.017	0.026	0.044				
F204N1	A → Y	(HL)	0.204	0.379	0.623	0.009	0.014	0.024	A	1.0	Y	22
		(LH)	0.281	0.514	0.878	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.216	0.393	0.642	0.009	0.014	0.024	C	1.0		
		(LH)	0.268	0.526	0.916	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.220	0.413	0.683	0.009	0.015	0.024				
		(LH)	0.285	0.518	0.893	0.013	0.023	0.037				
	D → Y	(HH)	0.330	0.648	1.119	0.013	0.023	0.037				
		(LL)	0.298	0.539	0.908	0.009	0.014	0.024				
F224N1	A → Y	(HL)	0.091	0.139	0.193	0.005	0.007	0.011	A	4.3	Y	8
		(LH)	0.182	0.362	0.606	0.021	0.044	0.075	B	4.3		
	B → Y	(HL)	0.096	0.148	0.204	0.005	0.007	0.011	C	4.3		
		(LH)	0.189	0.397	0.678	0.021	0.045	0.075	D	1.0		
	C → Y	(HL)	0.096	0.147	0.205	0.005	0.007	0.011				
		(LH)	0.188	0.399	0.681	0.021	0.044	0.075				
	D → Y	(HH)	0.326	0.595	0.961	0.021	0.045	0.075				
		(LL)	0.251	0.447	0.754	0.005	0.008	0.013				
L204N2	A → Y	(HL)	0.083	0.124	0.175	0.017	0.026	0.043	A	1.0	Y	2
		(LH)	0.141	0.242	0.394	0.084	0.177	0.299	B	1.0		
	B → Y	(HL)	0.097	0.142	0.196	0.017	0.027	0.045	C	1.0		
		(LH)	0.164	0.334	0.575	0.085	0.177	0.299	D	1.0		
	C → Y	(HH)	0.293	0.588	0.979	0.085	0.177	0.299				
		(LL)	0.163	0.268	0.428	0.017	0.028	0.045				
	D → Y	(HH)	0.307	0.616	1.024	0.085	0.177	0.299				
		(LL)	0.164	0.273	0.437	0.017	0.027	0.044				

FUNCTION BLOCK

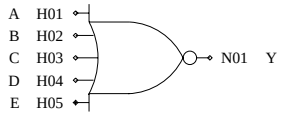
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F204N2	A → Y	(HL)	0.204	0.379	0.623	0.009	0.014	0.024	A	1.0	Y	22
		(LH)	0.281	0.514	0.878	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.216	0.393	0.642	0.009	0.014	0.024	C	1.0		
		(LH)	0.269	0.526	0.916	0.013	0.023	0.037	D	1.0		
	C → Y	(HH)	0.329	0.629	1.081	0.013	0.023	0.037				
		(LL)	0.293	0.533	0.895	0.009	0.014	0.024				
	D → Y	(HH)	0.344	0.664	1.139	0.013	0.023	0.037				
		(LL)	0.304	0.551	0.926	0.009	0.015	0.024				
F224N2	A → Y	(HL)	0.090	0.138	0.192	0.005	0.007	0.011	A	4.3	Y	8
		(LH)	0.183	0.363	0.609	0.021	0.045	0.075	B	4.3		
	B → Y	(HL)	0.096	0.147	0.203	0.005	0.007	0.011	C	1.0		
		(LH)	0.189	0.399	0.682	0.021	0.045	0.075	D	1.0		
	C → Y	(HH)	0.338	0.634	1.026	0.021	0.044	0.075				
		(LL)	0.252	0.444	0.753	0.005	0.008	0.012				
	D → Y	(HH)	0.331	0.601	0.969	0.021	0.045	0.075				
		(LL)	0.251	0.444	0.753	0.005	0.008	0.013				

[MEMO]

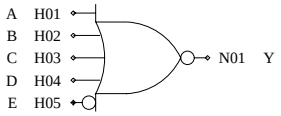
FUNCTION BLOCK

Function	5-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L205	4	L205N1	5	L205N2	5	L205N3	6				
x1	F205	5	F205N1	5	F205N2	6	F205N3	6				
x2	F225	6	F225N1	6	F225N2	7	F225N3	7				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

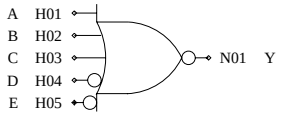
Logic Diagram for "Normal type"



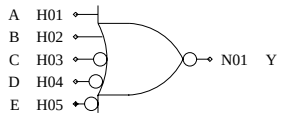
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed Path IN → OUT		t LD0 (ns) MIN.	t LD0 (ns) TYP.	t LD0 (ns) MAX.	t 1 MIN.	t 1 TYP.	t 1 MAX.	Input Symbol	Input Fanin	Output Symbol	Output Fanout
L205	A → Y	(HL)	0.211	0.386	0.629	0.017	0.026	0.044	A	1.0	Y	11
		(LH)	0.267	0.485	0.828	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.218	0.397	0.642	0.017	0.027	0.044	C	1.0		
		(LH)	0.255	0.495	0.865	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.200	0.365	0.588	0.016	0.026	0.044	E	1.0		
		(LH)	0.343	0.646	1.128	0.025	0.045	0.073				
	D → Y	(HL)	0.217	0.384	0.612	0.016	0.026	0.044				
		(LH)	0.347	0.699	1.238	0.025	0.045	0.073				
	E → Y	(HL)	0.223	0.391	0.621	0.017	0.027	0.044				
		(LH)	0.359	0.759	1.333	0.025	0.045	0.073				
F205	A → Y	(HL)	0.253	0.470	0.768	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.319	0.592	1.024	0.012	0.023	0.036	B	1.0		
	B → Y	(HL)	0.262	0.481	0.781	0.009	0.014	0.023	C	1.0		
		(LH)	0.307	0.600	1.061	0.012	0.023	0.036	D	1.0		
	C → Y	(HL)	0.251	0.453	0.736	0.009	0.014	0.023	E	1.0		
		(LH)	0.411	0.799	1.405	0.012	0.023	0.036				
	D → Y	(HL)	0.260	0.467	0.755	0.009	0.014	0.023				
		(LH)	0.416	0.850	1.515	0.012	0.023	0.036				
	E → Y	(HL)	0.267	0.477	0.769	0.009	0.014	0.023				
		(LH)	0.432	0.915	1.618	0.012	0.023	0.036				
F225	A → Y	(HL)	0.279	0.525	0.888	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.339	0.617	1.071	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.286	0.537	0.903	0.005	0.007	0.012	C	1.0		
		(LH)	0.327	0.629	1.110	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.268	0.504	0.847	0.004	0.007	0.012	E	1.0		
		(LH)	0.428	0.812	1.425	0.006	0.012	0.019				
	D → Y	(HL)	0.285	0.524	0.872	0.004	0.007	0.012				
		(LH)	0.433	0.864	1.535	0.006	0.012	0.019				
	E → Y	(HL)	0.290	0.532	0.884	0.005	0.007	0.012				
		(LH)	0.445	0.924	1.630	0.006	0.012	0.019				
L205N1	A → Y	(HL)	0.212	0.386	0.631	0.016	0.027	0.044	A	1.0	Y	11
		(LH)	0.267	0.485	0.827	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.218	0.396	0.643	0.017	0.026	0.044	C	1.0		
		(LH)	0.255	0.495	0.866	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.200	0.364	0.584	0.016	0.026	0.044	E	1.0		
		(LH)	0.343	0.646	1.128	0.025	0.045	0.073				
	D → Y	(HL)	0.217	0.384	0.612	0.016	0.026	0.044				
		(LH)	0.347	0.700	1.238	0.025	0.045	0.073				
	E → Y	(HH)	0.445	0.891	1.538	0.025	0.045	0.073				
		(LL)	0.294	0.515	0.854	0.016	0.027	0.044				
F205N1	A → Y	(HL)	0.221	0.415	0.689	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.283	0.510	0.877	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.232	0.429	0.710	0.009	0.014	0.023	C	1.0		
		(LH)	0.270	0.519	0.915	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.217	0.402	0.657	0.009	0.014	0.023	E	1.0		
		(LH)	0.366	0.692	1.216	0.012	0.023	0.037				
	D → Y	(HL)	0.234	0.421	0.683	0.009	0.014	0.023				
		(LH)	0.371	0.745	1.326	0.012	0.023	0.037				
	E → Y	(HH)	0.450	0.912	1.595	0.012	0.023	0.037				
		(LL)	0.304	0.543	0.908	0.009	0.014	0.023				
F225N1	A → Y	(HL)	0.279	0.525	0.887	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.339	0.617	1.071	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.286	0.537	0.903	0.005	0.007	0.012	C	1.0		
		(LH)	0.327	0.629	1.110	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.268	0.504	0.848	0.004	0.007	0.012	E	1.0		
		(LH)	0.429	0.814	1.427	0.006	0.012	0.019				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D → Y	(HL)	0.285	0.524	0.872	0.004	0.007	0.012				
		(LH)	0.435	0.867	1.538	0.006	0.012	0.019				
	E → Y	(HH)	0.514	1.033	1.806	0.006	0.012	0.019				
		(LL)	0.357	0.649	1.101	0.005	0.007	0.012				
L205N2	A → Y	(HL)	0.214	0.389	0.635	0.017	0.028	0.045	A	1.0	Y	11
		(LH)	0.269	0.488	0.831	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.220	0.399	0.648	0.018	0.028	0.045	C	1.0		
		(LH)	0.257	0.498	0.872	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.202	0.367	0.590	0.017	0.028	0.046	E	1.0		
		(LH)	0.344	0.648	1.133	0.025	0.045	0.073				
	D → Y	(HH)	0.413	0.833	1.445	0.025	0.045	0.073				
		(LL)	0.285	0.503	0.831	0.017	0.028	0.046				
	E → Y	(HH)	0.449	0.897	1.546	0.025	0.045	0.073				
		(LL)	0.298	0.523	0.864	0.018	0.028	0.046				
F205N2	A → Y	(HL)	0.221	0.415	0.689	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.283	0.510	0.877	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.232	0.429	0.710	0.009	0.014	0.023	C	1.0		
		(LH)	0.270	0.520	0.915	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.217	0.402	0.657	0.009	0.014	0.023	E	1.0		
		(LH)	0.366	0.692	1.216	0.012	0.023	0.037				
	D → Y	(HH)	0.444	0.886	1.543	0.012	0.023	0.037				
		(LL)	0.310	0.557	0.931	0.009	0.014	0.023				
	E → Y	(HH)	0.451	0.914	1.598	0.012	0.023	0.037				
		(LL)	0.304	0.544	0.908	0.009	0.014	0.023				
F225N2	A → Y	(HL)	0.279	0.525	0.887	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.340	0.618	1.071	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.285	0.536	0.901	0.005	0.007	0.012	C	1.0		
		(LH)	0.327	0.629	1.109	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.268	0.504	0.851	0.004	0.007	0.012	E	1.0		
		(LH)	0.429	0.815	1.427	0.006	0.012	0.019				
	D → Y	(HH)	0.497	0.995	1.736	0.006	0.012	0.019				
		(LL)	0.350	0.640	1.081	0.004	0.007	0.012				
	E → Y	(HH)	0.534	1.063	1.844	0.006	0.012	0.019				
		(LL)	0.367	0.662	1.126	0.005	0.007	0.012				
L205N3	A → Y	(HL)	0.213	0.389	0.634	0.018	0.028	0.046	A	1.0	Y	11
		(LH)	0.269	0.488	0.833	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.220	0.399	0.647	0.018	0.028	0.046	C	1.0		
		(LH)	0.257	0.498	0.871	0.025	0.045	0.073	D	1.0		
	C → Y	(HH)	0.391	0.772	1.335	0.025	0.045	0.073	E	1.0		
		(LL)	0.280	0.494	0.825	0.017	0.028	0.045				
	D → Y	(HH)	0.411	0.830	1.442	0.025	0.045	0.073				
		(LL)	0.284	0.500	0.829	0.017	0.028	0.046				
	E → Y	(HH)	0.452	0.901	1.552	0.025	0.045	0.073				
		(LL)	0.301	0.526	0.865	0.017	0.028	0.046				
F205N3	A → Y	(HL)	0.221	0.415	0.689	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.283	0.509	0.877	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.232	0.429	0.710	0.009	0.014	0.023	C	1.0		
		(LH)	0.270	0.520	0.915	0.012	0.023	0.037	D	1.0		
	C → Y	(HH)	0.416	0.818	1.424	0.012	0.023	0.037	E	1.0		
		(LL)	0.297	0.534	0.897	0.009	0.014	0.023				
	D → Y	(HH)	0.447	0.889	1.546	0.012	0.023	0.037				
		(LL)	0.310	0.553	0.928	0.009	0.014	0.023				
	E → Y	(HH)	0.453	0.917	1.602	0.012	0.023	0.037				
		(LL)	0.303	0.544	0.908	0.009	0.014	0.023				

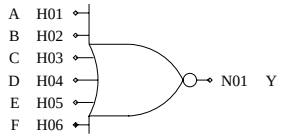
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F225N3	A → Y	(HL)	0.279	0.525	0.887	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.340	0.618	1.071	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.286	0.536	0.901	0.005	0.007	0.012	C	1.0		
		(LH)	0.327	0.629	1.109	0.006	0.012	0.019	D	1.0		
	C → Y	(HH)	0.471	0.930	1.625	0.006	0.012	0.019	E	1.0		
		(LL)	0.340	0.623	1.061	0.004	0.007	0.012				
	D → Y	(HH)	0.504	1.006	1.754	0.006	0.012	0.019				
		(LL)	0.356	0.648	1.100	0.004	0.007	0.012				
	E → Y	(HH)	0.538	1.069	1.852	0.006	0.012	0.019				
		(LL)	0.363	0.661	1.120	0.004	0.007	0.012				

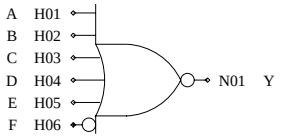
FUNCTION BLOCK

Function	6-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1	F206	5	F206N1	6	F206N2	6	F206N3	7				
x2	F226	6	F226N1	7	F226N2	7	F226N3	8				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

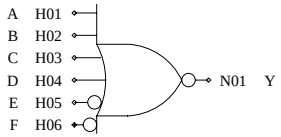
Logic Diagram for "Normal type"



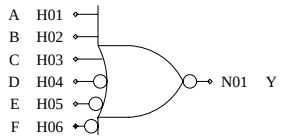
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F206	A → Y	(HL)	0.246	0.451	0.724	0.010	0.015	0.025		A	1.0	Y	22
		(LH)	0.406	0.790	1.388	0.012	0.023	0.036		B	1.0		
	B → Y	(HL)	0.257	0.463	0.740	0.010	0.015	0.025		C	1.0		
		(LH)	0.411	0.839	1.499	0.012	0.023	0.036		D	1.0		
	C → Y	(HL)	0.268	0.480	0.757	0.010	0.015	0.025		E	1.0		
		(LH)	0.427	0.906	1.603	0.012	0.023	0.036		F	1.0		
	D → Y	(HL)	0.250	0.465	0.755	0.010	0.015	0.025					
		(LH)	0.380	0.718	1.268	0.012	0.023	0.036					
	E → Y	(HL)	0.268	0.485	0.781	0.010	0.015	0.025					
		(LH)	0.383	0.771	1.381	0.012	0.023	0.036					
	F → Y	(HL)	0.280	0.501	0.803	0.010	0.015	0.025					
		(LH)	0.396	0.832	1.480	0.012	0.023	0.036					
F226	A → Y	(HL)	0.267	0.501	0.842	0.005	0.007	0.012		A	1.0	Y	44
		(LH)	0.426	0.809	1.420	0.006	0.012	0.019		B	1.0		
	B → Y	(HL)	0.283	0.521	0.865	0.005	0.007	0.012		C	1.0		
		(LH)	0.431	0.861	1.529	0.006	0.012	0.019		D	1.0		
	C → Y	(HL)	0.290	0.528	0.874	0.005	0.007	0.012		E	1.0		
		(LH)	0.445	0.924	1.630	0.006	0.012	0.019		F	1.0		
	D → Y	(HL)	0.288	0.540	0.909	0.005	0.007	0.012					
		(LH)	0.425	0.801	1.427	0.006	0.012	0.019					
	E → Y	(HL)	0.304	0.560	0.931	0.005	0.007	0.012					
		(LH)	0.430	0.857	1.541	0.006	0.012	0.019					
	F → Y	(HL)	0.311	0.567	0.944	0.005	0.007	0.012					
		(LH)	0.443	0.917	1.635	0.006	0.012	0.018					
F206N1	A → Y	(HL)	0.219	0.403	0.656	0.009	0.014	0.023		A	1.0	Y	22
		(LH)	0.377	0.720	1.263	0.013	0.023	0.037		B	1.0		
	B → Y	(HL)	0.237	0.423	0.680	0.009	0.014	0.023		C	1.0		
		(LH)	0.382	0.772	1.374	0.013	0.023	0.037		D	1.0		
	C → Y	(HL)	0.241	0.429	0.689	0.009	0.014	0.023		E	1.0		
		(LH)	0.394	0.831	1.469	0.013	0.023	0.037		F	1.0		
	D → Y	(HL)	0.229	0.426	0.699	0.009	0.014	0.023					
		(LH)	0.352	0.659	1.169	0.013	0.023	0.037					
	E → Y	(HL)	0.246	0.447	0.726	0.009	0.014	0.023					
		(LH)	0.357	0.712	1.276	0.013	0.023	0.037					
	F → Y	(HH)	0.460	0.913	1.589	0.013	0.023	0.037					
		(LL)	0.325	0.586	0.983	0.009	0.014	0.023					
F226N1	A → Y	(HL)	0.266	0.500	0.840	0.005	0.007	0.012		A	1.0	Y	44
		(LH)	0.425	0.808	1.419	0.006	0.012	0.019		B	1.0		
	B → Y	(HL)	0.283	0.521	0.864	0.005	0.007	0.012		C	1.0		
		(LH)	0.430	0.860	1.529	0.006	0.012	0.019		D	1.0		
	C → Y	(HL)	0.289	0.528	0.876	0.005	0.007	0.012		E	1.0		
		(LH)	0.444	0.924	1.628	0.006	0.012	0.019		F	1.0		
	D → Y	(HL)	0.288	0.539	0.904	0.005	0.007	0.012					
		(LH)	0.426	0.804	1.428	0.006	0.012	0.019					
	E → Y	(HL)	0.305	0.560	0.932	0.005	0.007	0.012					
		(LH)	0.431	0.858	1.541	0.006	0.012	0.019					
	F → Y	(HH)	0.531	1.052	1.844	0.006	0.012	0.018					
		(LL)	0.379	0.695	1.183	0.005	0.007	0.012					
F206N2	A → Y	(HL)	0.219	0.403	0.656	0.009	0.014	0.023		A	1.0	Y	22
		(LH)	0.377	0.720	1.263	0.013	0.023	0.037		B	1.0		
	B → Y	(HL)	0.237	0.423	0.680	0.009	0.014	0.023		C	1.0		
		(LH)	0.382	0.772	1.374	0.013	0.023	0.037		D	1.0		
	C → Y	(HL)	0.241	0.429	0.689	0.009	0.014	0.023		E	1.0		
		(LH)	0.394	0.831	1.469	0.013	0.023	0.037		F	1.0		
	D → Y	(HL)	0.227	0.426	0.702	0.009	0.014	0.023					
		(LH)	0.353	0.659	1.167	0.013	0.023	0.037					

FUNCTION BLOCK

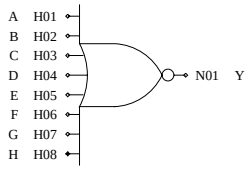
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	E → Y	(HH)	0.427	0.850	1.489	0.013	0.023	0.037				
		(LL)	0.319	0.575	0.964	0.009	0.014	0.023				
	F → Y	(HH)	0.462	0.915	1.590	0.013	0.023	0.037				
		(LL)	0.323	0.581	0.977	0.009	0.014	0.023				
F226N2	A → Y	(HL)	0.266	0.500	0.840	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.425	0.808	1.419	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.283	0.521	0.864	0.005	0.007	0.012	C	1.0		
		(LH)	0.430	0.860	1.529	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.289	0.528	0.876	0.005	0.007	0.012	E	1.0		
		(LH)	0.444	0.924	1.628	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.288	0.539	0.906	0.005	0.007	0.012				
		(LH)	0.426	0.805	1.430	0.006	0.012	0.018				
	E → Y	(HH)	0.500	0.993	1.746	0.006	0.012	0.019				
		(LL)	0.374	0.680	1.160	0.005	0.007	0.012				
	F → Y	(HH)	0.531	1.053	1.844	0.006	0.012	0.018				
		(LL)	0.377	0.690	1.172	0.005	0.007	0.012				
F206N3	A → Y	(HL)	0.220	0.403	0.657	0.009	0.014	0.023	A	1.0	Y	22
		(LH)	0.379	0.724	1.271	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.236	0.425	0.683	0.009	0.014	0.023	C	1.0		
		(LH)	0.383	0.776	1.384	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.241	0.432	0.693	0.009	0.014	0.023	E	1.0		
		(LH)	0.396	0.836	1.479	0.013	0.023	0.037	F	1.0		
	D → Y	(HH)	0.400	0.782	1.372	0.013	0.023	0.037				
		(LL)	0.306	0.552	0.932	0.009	0.014	0.023				
	E → Y	(HH)	0.431	0.854	1.494	0.013	0.023	0.037				
		(LL)	0.317	0.576	0.963	0.009	0.014	0.023				
	F → Y	(HH)	0.461	0.915	1.591	0.013	0.023	0.037				
		(LL)	0.323	0.583	0.976	0.009	0.014	0.023				
F226N3	A → Y	(HL)	0.267	0.501	0.842	0.005	0.007	0.012	A	1.0	Y	44
		(LH)	0.426	0.809	1.420	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.283	0.521	0.865	0.005	0.007	0.012	C	1.0		
		(LH)	0.431	0.861	1.529	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.289	0.528	0.874	0.005	0.007	0.012	E	1.0		
		(LH)	0.445	0.924	1.629	0.006	0.012	0.019	F	1.0		
	D → Y	(HH)	0.473	0.925	1.633	0.006	0.012	0.019				
		(LL)	0.364	0.667	1.140	0.005	0.007	0.012				
	E → Y	(HH)	0.502	0.996	1.753	0.006	0.012	0.019				
		(LL)	0.376	0.685	1.168	0.005	0.007	0.012				
	F → Y	(HH)	0.530	1.050	1.843	0.006	0.012	0.018				
		(LL)	0.374	0.682	1.162	0.005	0.007	0.012				

[MEMO]

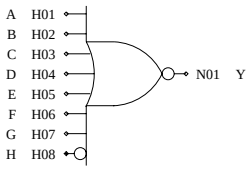
FUNCTION BLOCK

Function	8-INPUT NOR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1	F208	7	F208N1	8	F208N2	8	F208N3	9	F208N4	9		
x2	F228	8	F228N1	9	F228N2	9	F228N3	10	F228N4	10		
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

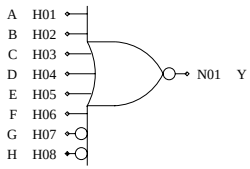
Logic Diagram for "Normal type"



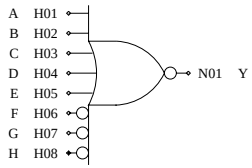
Logic Diagram for "with 1 inverter type"



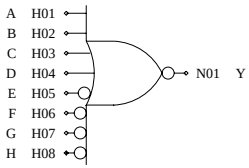
Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"



FUNCTION BLOCK

Block type	Switching speed Path IN → OUT		t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F208	A → Y	(HL)	0.255	0.468	0.768	0.010	0.016	0.025	A	1.0	Y	21
		(LH)	0.441	0.826	1.400	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.266	0.481	0.784	0.010	0.016	0.025	C	1.0		
		(LH)	0.428	0.834	1.441	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.278	0.515	0.842	0.010	0.016	0.025	E	1.0		
		(LH)	0.463	0.869	1.480	0.013	0.023	0.037	F	1.0		
	D → Y	(HL)	0.288	0.526	0.860	0.010	0.016	0.025	G	1.0		
		(LH)	0.449	0.877	1.515	0.013	0.023	0.037	H	1.0		
	E → Y	(HL)	0.295	0.556	0.912	0.010	0.016	0.026				
		(LH)	0.468	0.885	1.514	0.013	0.023	0.037				
	F → Y	(HL)	0.308	0.569	0.928	0.010	0.016	0.026				
		(LH)	0.454	0.895	1.552	0.013	0.023	0.037				
	G → Y	(HL)	0.315	0.584	0.958	0.010	0.016	0.026				
		(LH)	0.478	0.905	1.559	0.013	0.023	0.037				
	H → Y	(HL)	0.324	0.599	0.974	0.010	0.016	0.026				
		(LH)	0.465	0.915	1.596	0.013	0.023	0.037				
F228	A → Y	(HL)	0.274	0.519	0.876	0.005	0.007	0.012	A	1.0	Y	43
		(LH)	0.480	0.885	1.507	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.282	0.527	0.888	0.005	0.007	0.012	C	1.0		
		(LH)	0.468	0.896	1.543	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.287	0.549	0.935	0.005	0.007	0.012	E	1.0		
		(LH)	0.498	0.920	1.571	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.299	0.564	0.955	0.005	0.007	0.012	G	1.0		
		(LH)	0.485	0.930	1.606	0.006	0.012	0.019	H	1.0		
	E → Y	(HL)	0.317	0.605	1.027	0.005	0.007	0.012				
		(LH)	0.525	0.982	1.685	0.006	0.012	0.019				
	F → Y	(HL)	0.328	0.623	1.047	0.005	0.007	0.012				
		(LH)	0.513	0.991	1.722	0.006	0.012	0.019				
	G → Y	(HL)	0.334	0.636	1.079	0.005	0.007	0.012				
		(LH)	0.535	0.998	1.721	0.006	0.012	0.019				
	H → Y	(HL)	0.341	0.646	1.091	0.005	0.007	0.012				
		(LH)	0.521	1.007	1.759	0.006	0.012	0.019				
F208N1	A → Y	(HL)	0.219	0.408	0.673	0.009	0.014	0.023	A	1.0	Y	21
		(LH)	0.376	0.689	1.166	0.013	0.024	0.038	B	1.0		
	B → Y	(HL)	0.227	0.418	0.689	0.009	0.014	0.023	C	1.0		
		(LH)	0.363	0.700	1.202	0.013	0.024	0.038	D	1.0		
	C → Y	(HL)	0.246	0.456	0.751	0.009	0.014	0.023	E	1.0		
		(LH)	0.404	0.746	1.267	0.013	0.024	0.038	F	1.0		
	D → Y	(HL)	0.257	0.470	0.772	0.009	0.014	0.023	G	1.0		
		(LH)	0.392	0.756	1.305	0.013	0.024	0.038	H	1.0		
	E → Y	(HL)	0.265	0.498	0.827	0.009	0.015	0.024				
		(LH)	0.418	0.780	1.331	0.013	0.024	0.038				
	F → Y	(HL)	0.272	0.508	0.839	0.009	0.015	0.024				
		(LH)	0.405	0.789	1.369	0.013	0.024	0.038				
	G → Y	(HL)	0.282	0.529	0.877	0.009	0.015	0.024				
		(LH)	0.435	0.810	1.392	0.013	0.024	0.038				
	H → Y	(HH)	0.485	0.945	1.623	0.013	0.024	0.038				
		(LL)	0.355	0.655	1.103	0.009	0.015	0.024				
F228N1	A → Y	(HL)	0.274	0.519	0.876	0.005	0.007	0.012	A	1.0	Y	43
		(LH)	0.480	0.885	1.507	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.282	0.527	0.888	0.005	0.007	0.012	C	1.0		
		(LH)	0.468	0.896	1.543	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.287	0.549	0.935	0.005	0.007	0.012	E	1.0		
		(LH)	0.498	0.920	1.571	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.299	0.564	0.955	0.005	0.007	0.012	G	1.0		
		(LH)	0.485	0.930	1.606	0.006	0.012	0.019	H	1.0		

FUNCTION BLOCK

Block type	Path		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	E → Y	(HL)	0.317	0.605	1.027	0.005	0.007	0.012				
		(LH)	0.525	0.982	1.685	0.006	0.012	0.019				
	F → Y	(HL)	0.328	0.623	1.047	0.005	0.007	0.012				
		(LH)	0.513	0.991	1.722	0.006	0.012	0.019				
	G → Y	(HL)	0.328	0.629	1.070	0.005	0.007	0.012				
		(LH)	0.533	0.992	1.708	0.006	0.012	0.019				
	H → Y	(HH)	0.578	1.121	1.937	0.006	0.012	0.019				
		(LL)	0.406	0.757	1.296	0.005	0.007	0.012				
F208N2	A → Y	(HL)	0.219	0.408	0.673	0.009	0.014	0.023	A	1.0	Y	21
		(LH)	0.376	0.689	1.166	0.013	0.024	0.038	B	1.0		
	B → Y	(HL)	0.227	0.418	0.689	0.009	0.014	0.023	C	1.0		
		(LH)	0.363	0.700	1.202	0.013	0.024	0.038	D	1.0		
	C → Y	(HL)	0.246	0.456	0.751	0.009	0.014	0.023	E	1.0		
		(LH)	0.404	0.746	1.266	0.013	0.024	0.038	F	1.0		
	D → Y	(HL)	0.257	0.470	0.772	0.009	0.014	0.023	G	1.0		
		(LH)	0.392	0.756	1.305	0.013	0.024	0.038	H	1.0		
	E → Y	(HL)	0.265	0.498	0.827	0.009	0.015	0.024				
		(LH)	0.418	0.780	1.331	0.013	0.024	0.038				
	F → Y	(HL)	0.272	0.508	0.839	0.009	0.015	0.024				
		(LH)	0.405	0.789	1.369	0.013	0.024	0.038				
	G → Y	(HH)	0.479	0.922	1.577	0.013	0.024	0.038				
		(LL)	0.351	0.646	1.087	0.009	0.015	0.024				
	H → Y	(HH)	0.495	0.959	1.635	0.013	0.024	0.038				
		(LL)	0.363	0.664	1.119	0.009	0.015	0.024				
F228N2	A → Y	(HL)	0.274	0.519	0.876	0.005	0.007	0.012	A	1.0	Y	43
		(LH)	0.480	0.885	1.507	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.282	0.527	0.888	0.005	0.007	0.012	C	1.0		
		(LH)	0.468	0.896	1.543	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.287	0.549	0.935	0.005	0.007	0.012	E	1.0		
		(LH)	0.498	0.920	1.571	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.299	0.564	0.955	0.005	0.007	0.012	G	1.0		
		(LH)	0.485	0.930	1.606	0.006	0.012	0.019	H	1.0		
	E → Y	(HL)	0.317	0.605	1.027	0.005	0.007	0.012				
		(LH)	0.525	0.982	1.685	0.006	0.012	0.019				
	F → Y	(HL)	0.328	0.623	1.047	0.005	0.007	0.012				
		(LH)	0.513	0.992	1.722	0.006	0.012	0.019				
	G → Y	(HH)	0.582	1.111	1.907	0.006	0.012	0.019				
		(LL)	0.407	0.759	1.299	0.005	0.007	0.012				
	H → Y	(HH)	0.591	1.136	1.954	0.006	0.012	0.019				
		(LL)	0.408	0.761	1.302	0.005	0.007	0.012				
F208N3	A → Y	(HL)	0.219	0.408	0.673	0.009	0.014	0.023	A	1.0	Y	21
		(LH)	0.376	0.689	1.166	0.013	0.024	0.038	B	1.0		
	B → Y	(HL)	0.226	0.418	0.689	0.009	0.014	0.023	C	1.0		
		(LH)	0.363	0.700	1.202	0.013	0.024	0.038	D	1.0		
	C → Y	(HL)	0.242	0.449	0.747	0.009	0.014	0.023	E	1.0		
		(LH)	0.398	0.734	1.243	0.013	0.024	0.038	F	1.0		
	D → Y	(HL)	0.248	0.460	0.760	0.009	0.014	0.023	G	1.0		
		(LH)	0.386	0.744	1.280	0.013	0.024	0.038	H	1.0		
	E → Y	(HL)	0.269	0.504	0.832	0.009	0.015	0.024				
		(LH)	0.423	0.791	1.353	0.013	0.024	0.038				
	F → Y	(HH)	0.477	0.924	1.584	0.013	0.024	0.038				
		(LL)	0.344	0.630	1.061	0.009	0.015	0.024				
	G → Y	(HH)	0.480	0.921	1.578	0.013	0.024	0.038				
		(LL)	0.355	0.650	1.099	0.009	0.015	0.024				
	H → Y	(HH)	0.493	0.956	1.635	0.013	0.024	0.038				
		(LL)	0.366	0.669	1.128	0.009	0.015	0.024				

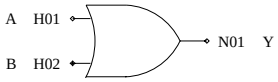
FUNCTION BLOCK

Block type	Path		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F228N3	A → Y	(HL)	0.274	0.519	0.876	0.005	0.007	0.012	A	1.0	Y	43
		(LH)	0.480	0.885	1.507	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.282	0.527	0.888	0.005	0.007	0.012	C	1.0		
		(LH)	0.468	0.896	1.543	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.287	0.549	0.935	0.005	0.007	0.012	E	1.0		
		(LH)	0.498	0.920	1.571	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.299	0.564	0.955	0.005	0.007	0.012	G	1.0		
		(LH)	0.485	0.930	1.606	0.006	0.012	0.019	H	1.0		
	E → Y	(HL)	0.316	0.605	1.031	0.005	0.007	0.012				
		(LH)	0.525	0.982	1.685	0.006	0.012	0.019				
	F → Y	(HH)	0.579	1.116	1.919	0.006	0.012	0.019				
		(LL)	0.397	0.738	1.262	0.005	0.007	0.012				
	G → Y	(HH)	0.582	1.112	1.909	0.006	0.012	0.019				
		(LL)	0.409	0.762	1.305	0.005	0.007	0.012				
	H → Y	(HH)	0.593	1.140	1.959	0.006	0.012	0.019				
		(LL)	0.415	0.774	1.323	0.005	0.007	0.012				
F208N4	A → Y	(HL)	0.219	0.408	0.673	0.009	0.014	0.023	A	1.0	Y	21
		(LH)	0.376	0.689	1.166	0.013	0.024	0.038	B	1.0		
	B → Y	(HL)	0.226	0.418	0.689	0.009	0.014	0.023	C	1.0		
		(LH)	0.363	0.700	1.202	0.013	0.024	0.038	D	1.0		
	C → Y	(HL)	0.242	0.449	0.747	0.009	0.014	0.023	E	1.0		
		(LH)	0.398	0.734	1.243	0.013	0.024	0.038	F	1.0		
	D → Y	(HL)	0.248	0.460	0.760	0.009	0.014	0.023	G	1.0		
		(LH)	0.386	0.744	1.280	0.013	0.024	0.038	H	1.0		
	E → Y	(HH)	0.474	0.911	1.550	0.013	0.024	0.038				
		(LL)	0.342	0.627	1.055	0.009	0.014	0.023				
	F → Y	(HH)	0.482	0.933	1.592	0.013	0.024	0.038				
		(LL)	0.345	0.630	1.062	0.009	0.015	0.023				
	G → Y	(HH)	0.483	0.926	1.581	0.013	0.024	0.038				
		(LL)	0.355	0.653	1.099	0.009	0.015	0.024				
	H → Y	(HH)	0.496	0.958	1.634	0.013	0.024	0.038				
		(LL)	0.365	0.667	1.119	0.009	0.015	0.024				
F228N4	A → Y	(HL)	0.274	0.519	0.876	0.005	0.007	0.012	A	1.0	Y	43
		(LH)	0.480	0.885	1.507	0.006	0.012	0.019	B	1.0		
	B → Y	(HL)	0.282	0.527	0.888	0.005	0.007	0.012	C	1.0		
		(LH)	0.468	0.896	1.543	0.006	0.012	0.019	D	1.0		
	C → Y	(HL)	0.287	0.549	0.935	0.005	0.007	0.012	E	1.0		
		(LH)	0.498	0.920	1.571	0.006	0.012	0.019	F	1.0		
	D → Y	(HL)	0.299	0.564	0.955	0.005	0.007	0.012	G	1.0		
		(LH)	0.485	0.930	1.606	0.006	0.012	0.019	H	1.0		
	E → Y	(HH)	0.576	1.102	1.880	0.006	0.012	0.019				
		(LL)	0.395	0.736	1.257	0.005	0.007	0.012				
	F → Y	(HH)	0.583	1.125	1.927	0.006	0.012	0.019				
		(LL)	0.397	0.739	1.263	0.005	0.007	0.012				
	G → Y	(HH)	0.581	1.111	1.907	0.006	0.012	0.019				
		(LL)	0.408	0.760	1.301	0.005	0.007	0.012				
	H → Y	(HH)	0.596	1.143	1.964	0.006	0.012	0.019				
		(LL)	0.414	0.773	1.323	0.005	0.007	0.012				

FUNCTION BLOCK

Function	2-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L212	2										
x1	F212	2										
x2	F232	3										
x4	F252	6										
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

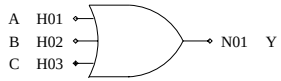
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L212	A → Y	(HH)	0.143	0.239	0.362	0.025	0.046	0.073	A	1.0	Y	11
		(LL)	0.223	0.410	0.705	0.017	0.027	0.045	B	1.0		
	B → Y	(HH)	0.154	0.250	0.380	0.025	0.046	0.073				
		(LL)	0.211	0.416	0.738	0.017	0.027	0.045				
F212	A → Y	(HH)	0.160	0.267	0.397	0.012	0.023	0.036	A	1.0	Y	22
		(LL)	0.265	0.500	0.874	0.011	0.017	0.027	B	1.0		
	B → Y	(HH)	0.169	0.277	0.411	0.012	0.023	0.037				
		(LL)	0.251	0.507	0.909	0.011	0.017	0.027				
F232	A → Y	(HH)	0.218	0.343	0.518	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.366	0.724	1.306	0.005	0.008	0.013	B	1.0		
	B → Y	(HH)	0.225	0.353	0.533	0.006	0.011	0.018				
		(LL)	0.354	0.737	1.340	0.005	0.008	0.013				
F252	A → Y	(HH)	0.196	0.306	0.458	0.003	0.006	0.009	A	2.0	Y	89
		(LL)	0.292	0.582	1.058	0.003	0.004	0.007	B	2.0		
	B → Y	(HH)	0.193	0.302	0.453	0.003	0.006	0.009				
		(LL)	0.291	0.584	1.053	0.003	0.005	0.008				

FUNCTION BLOCK

Function	3-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L213	2										
x1	F213	3										
x2	F233	4										
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

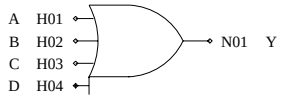
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L213	A → Y	(HH)	0.157	0.258	0.390	0.025	0.046	0.073	A	1.0	Y	11
		(LL)	0.315	0.612	1.084	0.018	0.030	0.049	B	1.0		
	B → Y	(HH)	0.167	0.271	0.406	0.025	0.046	0.073	C	1.0		
		(LL)	0.320	0.660	1.197	0.018	0.030	0.049				
	C → Y	(HH)	0.163	0.267	0.403	0.025	0.045	0.073				
		(LL)	0.341	0.733	1.304	0.018	0.030	0.049				
F213	A → Y	(HH)	0.177	0.288	0.429	0.012	0.023	0.037	A	1.0	Y	22
		(LL)	0.375	0.733	1.321	0.011	0.018	0.029	B	1.0		
	B → Y	(HH)	0.186	0.298	0.444	0.013	0.023	0.037	C	1.0		
		(LL)	0.381	0.794	1.437	0.011	0.018	0.029				
	C → Y	(HH)	0.190	0.304	0.452	0.012	0.023	0.036				
		(LL)	0.395	0.851	1.534	0.011	0.018	0.029				
F233	A → Y	(HH)	0.215	0.337	0.506	0.006	0.012	0.019	A	1.0	Y	45
		(LL)	0.458	0.929	1.702	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.224	0.348	0.525	0.006	0.012	0.019	C	1.0		
		(LL)	0.465	0.985	1.812	0.006	0.011	0.018				
	C → Y	(HH)	0.226	0.351	0.532	0.006	0.012	0.019				
		(LL)	0.481	1.051	1.908	0.006	0.011	0.018				

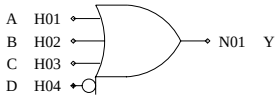
FUNCTION BLOCK

Function	4-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L214	3	L214N1	3								
x1	F214	3	F214N1	4								
x2	F234	4	F234N1	5								
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

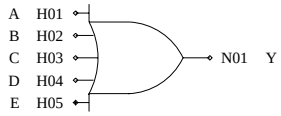
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L214	A → Y	(HH)	0.158	0.259	0.386	0.025	0.045	0.073	A	1.0	Y	11
		(LL)	0.371	0.733	1.339	0.018	0.030	0.050	B	1.0		
	B → Y	(HH)	0.168	0.272	0.408	0.025	0.045	0.073	C	1.0		
		(LL)	0.389	0.825	1.517	0.018	0.030	0.050	D	1.0		
	C → Y	(HH)	0.179	0.286	0.426	0.025	0.045	0.072				
		(LL)	0.434	0.953	1.724	0.018	0.030	0.050				
	D → Y	(HH)	0.174	0.280	0.420	0.025	0.045	0.072				
		(LL)	0.435	0.963	1.758	0.018	0.030	0.050				
F214	A → Y	(HH)	0.177	0.289	0.429	0.012	0.023	0.037	A	1.0	Y	22
		(LL)	0.438	0.880	1.607	0.012	0.019	0.031	B	1.0		
	B → Y	(HH)	0.187	0.300	0.445	0.012	0.023	0.037	C	1.0		
		(LL)	0.457	0.976	1.788	0.012	0.019	0.031	D	1.0		
	C → Y	(HH)	0.198	0.314	0.465	0.013	0.023	0.037				
		(LL)	0.504	1.099	2.000	0.012	0.019	0.031				
	D → Y	(HH)	0.193	0.309	0.458	0.012	0.023	0.037				
		(LL)	0.503	1.119	2.027	0.012	0.019	0.031				
F234	A → Y	(HH)	0.225	0.354	0.534	0.006	0.011	0.018	A	1.0	Y	44
		(LL)	0.597	1.259	2.328	0.006	0.010	0.017	B	1.0		
	B → Y	(HH)	0.234	0.365	0.553	0.006	0.011	0.018	C	1.0		
		(LL)	0.619	1.355	2.501	0.006	0.010	0.017	D	1.0		
	C → Y	(HH)	0.245	0.379	0.575	0.006	0.011	0.018				
		(LL)	0.670	1.476	2.708	0.006	0.010	0.017				
	D → Y	(HH)	0.239	0.372	0.566	0.006	0.011	0.018				
		(LL)	0.670	1.492	2.750	0.006	0.010	0.017				
L214N1	A → Y	(HH)	0.136	0.237	0.354	0.025	0.045	0.073	A	1.0	Y	11
		(LL)	0.324	0.621	1.120	0.018	0.029	0.049	B	1.0		
	B → Y	(HH)	0.152	0.256	0.378	0.025	0.045	0.073	C	1.0		
		(LL)	0.341	0.707	1.296	0.018	0.029	0.049	D	1.0		
	C → Y	(HH)	0.164	0.269	0.397	0.025	0.045	0.073				
		(LL)	0.382	0.833	1.494	0.018	0.029	0.049				
	D → Y	(HL)	0.469	0.976	1.741	0.018	0.029	0.049				
		(LH)	0.222	0.375	0.602	0.025	0.045	0.073				
F214N1	A → Y	(HH)	0.150	0.248	0.366	0.013	0.023	0.037	A	1.0	Y	22
		(LL)	0.368	0.734	1.352	0.010	0.017	0.028	B	1.0		
	B → Y	(HH)	0.165	0.267	0.396	0.013	0.023	0.037	C	1.0		
		(LL)	0.389	0.828	1.526	0.010	0.017	0.028	D	1.0		
	C → Y	(HH)	0.177	0.282	0.412	0.013	0.023	0.037				
		(LL)	0.433	0.953	1.736	0.010	0.017	0.028				
	D → Y	(HL)	0.524	1.105	1.979	0.010	0.017	0.028				
		(LH)	0.229	0.389	0.626	0.013	0.023	0.037				
F234N1	A → Y	(HH)	0.201	0.317	0.474	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.515	1.077	2.003	0.006	0.009	0.016	B	1.0		
	B → Y	(HH)	0.211	0.329	0.495	0.006	0.011	0.018	C	1.0		
		(LL)	0.538	1.174	2.174	0.006	0.009	0.016	D	1.0		
	C → Y	(HH)	0.222	0.344	0.517	0.006	0.011	0.018				
		(LL)	0.584	1.299	2.381	0.006	0.009	0.016				
	D → Y	(HL)	0.671	1.442	2.617	0.006	0.009	0.016				
		(LH)	0.265	0.447	0.725	0.006	0.011	0.018				

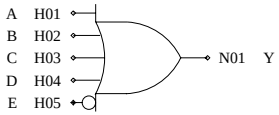
FUNCTION BLOCK

Function	5-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L215	4	L215N1	4								
x1	F215	5	F215N1	5								
x2	F235	7	F235N1	7								
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L215	A → Y	(HH)	0.121	0.217	0.332	0.025	0.045	0.072	A	1.0	Y	11
		(LL)	0.192	0.351	0.587	0.025	0.044	0.077	B	1.0		
	B → Y	(HH)	0.133	0.230	0.348	0.025	0.045	0.073	C	1.0		
		(LL)	0.180	0.360	0.629	0.025	0.044	0.077	D	1.0		
	C → Y	(HH)	0.150	0.265	0.407	0.025	0.045	0.072	E	1.0		
		(LL)	0.281	0.525	0.937	0.024	0.044	0.078				
	D → Y	(HH)	0.167	0.285	0.432	0.024	0.045	0.072				
		(LL)	0.284	0.579	1.051	0.025	0.044	0.078				
	E → Y	(HH)	0.173	0.293	0.442	0.024	0.045	0.072				
		(LL)	0.295	0.638	1.145	0.024	0.044	0.078				
F215	A → Y	(HH)	0.171	0.283	0.423	0.012	0.023	0.037	A	1.0	Y	21
		(LL)	0.270	0.513	0.891	0.013	0.023	0.040	B	1.0		
	B → Y	(HH)	0.180	0.293	0.438	0.013	0.023	0.037	C	1.0		
		(LL)	0.257	0.521	0.927	0.013	0.023	0.040	D	1.0		
	C → Y	(HH)	0.180	0.305	0.465	0.012	0.023	0.036	E	1.0		
		(LL)	0.351	0.682	1.229	0.013	0.023	0.040				
	D → Y	(HH)	0.196	0.324	0.491	0.012	0.023	0.036				
		(LL)	0.355	0.738	1.343	0.013	0.023	0.040				
	E → Y	(HH)	0.200	0.330	0.500	0.012	0.023	0.036				
		(LL)	0.370	0.794	1.440	0.013	0.023	0.040				
F235	A → Y	(HH)	0.294	0.542	0.900	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.365	0.678	1.188	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.302	0.552	0.913	0.006	0.011	0.018	C	1.0		
		(LL)	0.353	0.690	1.222	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.283	0.519	0.855	0.006	0.011	0.018	E	1.0		
		(LL)	0.446	0.855	1.513	0.004	0.007	0.011				
	D → Y	(HH)	0.299	0.539	0.881	0.006	0.011	0.018				
		(LL)	0.449	0.908	1.623	0.004	0.007	0.011				
	E → Y	(HH)	0.304	0.547	0.890	0.006	0.011	0.018				
		(LL)	0.462	0.967	1.719	0.004	0.007	0.011				
L215N1	A → Y	(HH)	0.121	0.217	0.332	0.025	0.045	0.072	A	1.0	Y	11
		(LL)	0.192	0.351	0.587	0.025	0.044	0.077	B	1.0		
	B → Y	(HH)	0.133	0.230	0.348	0.025	0.045	0.073	C	1.0		
		(LL)	0.180	0.360	0.629	0.025	0.044	0.077	D	1.0		
	C → Y	(HH)	0.149	0.265	0.406	0.025	0.045	0.072	E	1.0		
		(LL)	0.281	0.527	0.934	0.025	0.044	0.078				
	D → Y	(HH)	0.167	0.285	0.432	0.024	0.045	0.072				
		(LL)	0.287	0.584	1.053	0.024	0.044	0.078				
	E → Y	(HL)	0.366	0.747	1.317	0.024	0.044	0.078				
		(LH)	0.238	0.409	0.660	0.025	0.045	0.072				
F215N1	A → Y	(HH)	0.157	0.270	0.408	0.012	0.023	0.036	A	1.0	Y	21
		(LL)	0.241	0.449	0.782	0.013	0.023	0.040	B	1.0		
	B → Y	(HH)	0.168	0.282	0.425	0.012	0.023	0.036	C	1.0		
		(LL)	0.229	0.458	0.820	0.013	0.023	0.040	D	1.0		
	C → Y	(HH)	0.173	0.293	0.441	0.013	0.023	0.037	E	1.0		
		(LL)	0.356	0.695	1.241	0.013	0.023	0.041				
	D → Y	(HH)	0.189	0.311	0.468	0.013	0.023	0.037				
		(LL)	0.362	0.751	1.355	0.013	0.023	0.041				
	E → Y	(HL)	0.439	0.911	1.617	0.013	0.023	0.041				
		(LH)	0.254	0.435	0.702	0.013	0.023	0.037				
F235N1	A → Y	(HH)	0.288	0.535	0.891	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.363	0.672	1.177	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.300	0.550	0.910	0.006	0.011	0.018	C	1.0		
		(LL)	0.350	0.683	1.212	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.283	0.520	0.856	0.006	0.011	0.018	E	1.0		
		(LL)	0.447	0.857	1.518	0.004	0.007	0.011				

FUNCTION BLOCK

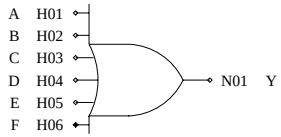
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D → Y	(HH)	0.300	0.539	0.882	0.006	0.011	0.018				
		(LL)	0.452	0.911	1.628	0.004	0.007	0.011				
	E → Y	(HL)	0.531	1.076	1.894	0.004	0.007	0.011				
		(LH)	0.370	0.663	1.107	0.006	0.011	0.018				

[MEMO]

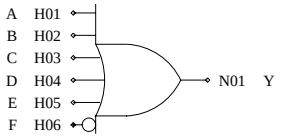
FUNCTION BLOCK

Function	6-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1	F216	5	F216N1	6	F216N2	6						
x2	F236	7	F236N1	8	F236N2	8						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

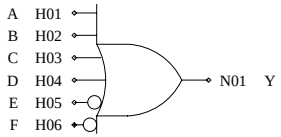
Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F216	A → Y	(HH)	0.181	0.298	0.448	0.013	0.023	0.037	A	1.0	Y	21
		(LL)	0.385	0.761	1.365	0.013	0.024	0.042	B	1.0		
	B → Y	(HH)	0.191	0.311	0.463	0.013	0.023	0.037	C	1.0		
		(LL)	0.391	0.818	1.473	0.013	0.024	0.042	D	1.0		
	C → Y	(HH)	0.203	0.325	0.482	0.013	0.023	0.037	E	1.0		
		(LL)	0.409	0.881	1.581	0.013	0.024	0.041	F	1.0		
	D → Y	(HH)	0.180	0.307	0.466	0.012	0.023	0.036				
		(LL)	0.354	0.685	1.245	0.013	0.023	0.041				
	E → Y	(HH)	0.196	0.326	0.492	0.012	0.023	0.036				
		(LL)	0.358	0.741	1.353	0.013	0.023	0.041				
	F → Y	(HH)	0.208	0.339	0.511	0.012	0.023	0.036				
		(LL)	0.373	0.806	1.456	0.013	0.023	0.041				
F236	A → Y	(HH)	0.286	0.520	0.853	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.458	0.881	1.562	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.303	0.540	0.879	0.006	0.011	0.018	C	1.0		
		(LL)	0.462	0.936	1.674	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.307	0.547	0.887	0.006	0.011	0.018	E	1.0		
		(LL)	0.475	0.995	1.771	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.296	0.546	0.900	0.006	0.011	0.018				
		(LL)	0.435	0.823	1.469	0.004	0.007	0.011				
	E → Y	(HH)	0.314	0.566	0.926	0.006	0.011	0.018				
		(LL)	0.439	0.876	1.578	0.004	0.007	0.011				
	F → Y	(HH)	0.319	0.574	0.936	0.006	0.011	0.018				
		(LL)	0.452	0.940	1.678	0.004	0.007	0.011				
F216N1	A → Y	(HH)	0.163	0.276	0.413	0.013	0.023	0.037	A	1.0	Y	21
		(LL)	0.365	0.707	1.260	0.016	0.027	0.044	B	1.0		
	B → Y	(HH)	0.179	0.293	0.438	0.013	0.023	0.037	C	1.0		
		(LL)	0.370	0.764	1.371	0.016	0.027	0.044	D	1.0		
	C → Y	(HH)	0.179	0.295	0.439	0.012	0.023	0.037	E	1.0		
		(LL)	0.383	0.824	1.465	0.016	0.027	0.044	F	1.0		
	D → Y	(HH)	0.184	0.316	0.483	0.012	0.023	0.036				
		(LL)	0.350	0.686	1.238	0.015	0.026	0.044				
	E → Y	(HH)	0.201	0.336	0.510	0.012	0.023	0.036				
		(LL)	0.355	0.738	1.351	0.015	0.026	0.044				
	F → Y	(HL)	0.458	0.935	1.658	0.015	0.026	0.044				
		(LH)	0.264	0.463	0.758	0.012	0.023	0.036				
F236N1	A → Y	(HH)	0.286	0.520	0.853	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.458	0.881	1.561	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.303	0.540	0.878	0.006	0.011	0.018	C	1.0		
		(LL)	0.462	0.935	1.675	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.307	0.547	0.887	0.006	0.011	0.018	E	1.0		
		(LL)	0.475	0.995	1.770	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.296	0.546	0.899	0.006	0.011	0.018				
		(LL)	0.435	0.823	1.471	0.004	0.007	0.011				
	E → Y	(HH)	0.314	0.565	0.925	0.006	0.011	0.018				
		(LL)	0.439	0.876	1.578	0.004	0.007	0.011				
	F → Y	(HL)	0.542	1.077	1.890	0.004	0.007	0.011				
		(LH)	0.392	0.706	1.183	0.006	0.011	0.018				
F216N2	A → Y	(HH)	0.163	0.276	0.413	0.013	0.023	0.037	A	1.0	Y	21
		(LL)	0.365	0.707	1.260	0.016	0.027	0.044	B	1.0		
	B → Y	(HH)	0.179	0.293	0.438	0.013	0.023	0.037	C	1.0		
		(LL)	0.370	0.764	1.371	0.016	0.027	0.044	D	1.0		
	C → Y	(HH)	0.179	0.295	0.439	0.012	0.023	0.037	E	1.0		
		(LL)	0.383	0.824	1.465	0.016	0.027	0.044	F	1.0		
	D → Y	(HH)	0.185	0.317	0.485	0.012	0.023	0.036				
		(LL)	0.351	0.685	1.241	0.015	0.026	0.044				

FUNCTION BLOCK

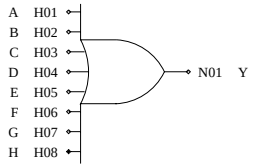
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	E → Y	(HL)	0.426	0.874	1.562	0.015	0.026	0.044				
		(LH)	0.259	0.449	0.734	0.012	0.023	0.036				
	F → Y	(HL)	0.462	0.940	1.664	0.015	0.026	0.044				
		(LH)	0.263	0.460	0.752	0.012	0.023	0.036				
F236N2	A → Y	(HH)	0.286	0.521	0.853	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.458	0.882	1.563	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.303	0.541	0.879	0.006	0.011	0.018	C	1.0		
		(LL)	0.462	0.936	1.676	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.307	0.547	0.888	0.006	0.011	0.018	E	1.0		
		(LL)	0.476	0.996	1.772	0.005	0.007	0.012	F	1.0		
	D → Y	(HH)	0.296	0.547	0.900	0.006	0.011	0.018				
		(LL)	0.436	0.824	1.469	0.005	0.007	0.012				
	E → Y	(HL)	0.510	1.015	1.791	0.005	0.007	0.012				
		(LH)	0.387	0.695	1.161	0.006	0.011	0.018				
	F → Y	(HL)	0.544	1.079	1.892	0.005	0.007	0.012				
		(LH)	0.391	0.701	1.176	0.006	0.011	0.018				

[MEMO]

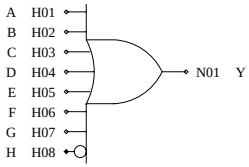
FUNCTION BLOCK

Function	8-INPUT OR										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1	F218	8	F218N1	9	F218N2	9	F218N3	10				
x2	F238	9	F238N1	10	F238N2	10	F238N3	11				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

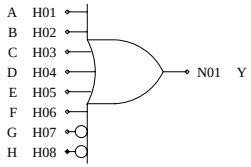
Logic Diagram for "Normal type"



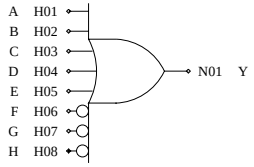
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F218	A → Y	(HH)	0.261	0.485	0.801	0.012	0.023	0.037	A	1.0	Y	23
		(LL)	0.427	0.790	1.360	0.009	0.014	0.022	B	1.0		
	B → Y	(HH)	0.269	0.494	0.814	0.012	0.023	0.037	C	1.0		
		(LL)	0.415	0.802	1.397	0.009	0.014	0.022	D	1.0		
	C → Y	(HH)	0.293	0.536	0.886	0.012	0.023	0.037	E	1.0		
		(LL)	0.464	0.865	1.492	0.009	0.014	0.022	F	1.0		
	D → Y	(HH)	0.299	0.545	0.899	0.012	0.023	0.037	G	1.0		
		(LL)	0.451	0.874	1.527	0.009	0.014	0.022	H	1.0		
	E → Y	(HH)	0.306	0.572	0.951	0.012	0.023	0.037				
		(LL)	0.469	0.882	1.526	0.009	0.014	0.022				
	F → Y	(HH)	0.313	0.582	0.963	0.012	0.023	0.037				
		(LL)	0.457	0.890	1.566	0.009	0.014	0.022				
	G → Y	(HH)	0.319	0.595	0.992	0.012	0.023	0.036				
		(LL)	0.480	0.897	1.561	0.009	0.014	0.022				
	H → Y	(HH)	0.331	0.610	1.010	0.012	0.023	0.036				
		(LL)	0.467	0.908	1.600	0.009	0.014	0.022				
F238	A → Y	(HH)	0.288	0.529	0.878	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.460	0.863	1.488	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.296	0.539	0.888	0.006	0.011	0.018	C	1.0		
		(LL)	0.448	0.874	1.524	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.310	0.571	0.947	0.006	0.011	0.018	E	1.0		
		(LL)	0.483	0.906	1.565	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.318	0.581	0.961	0.006	0.011	0.018	G	1.0		
		(LL)	0.472	0.917	1.602	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.338	0.626	1.038	0.006	0.011	0.018				
		(LL)	0.508	0.964	1.672	0.004	0.007	0.011				
	F → Y	(HH)	0.350	0.641	1.054	0.006	0.011	0.018				
		(LL)	0.495	0.974	1.711	0.004	0.007	0.011				
	G → Y	(HH)	0.352	0.652	1.080	0.006	0.011	0.018				
		(LL)	0.520	0.983	1.711	0.004	0.007	0.011				
	H → Y	(HH)	0.358	0.661	1.092	0.006	0.011	0.018				
		(LL)	0.506	0.993	1.753	0.004	0.007	0.011				
F218N1	A → Y	(HH)	0.262	0.485	0.801	0.012	0.023	0.037	A	1.0	Y	23
		(LL)	0.427	0.790	1.360	0.009	0.014	0.022	B	1.0		
	B → Y	(HH)	0.269	0.494	0.815	0.012	0.023	0.037	C	1.0		
		(LL)	0.415	0.802	1.397	0.009	0.014	0.022	D	1.0		
	C → Y	(HH)	0.283	0.525	0.870	0.012	0.023	0.037	E	1.0		
		(LL)	0.450	0.835	1.438	0.009	0.014	0.022	F	1.0		
	D → Y	(HH)	0.291	0.535	0.884	0.012	0.023	0.037	G	1.0		
		(LL)	0.438	0.845	1.475	0.009	0.014	0.022	H	1.0		
	E → Y	(HH)	0.310	0.577	0.958	0.012	0.023	0.037				
		(LL)	0.475	0.892	1.545	0.009	0.014	0.022				
	F → Y	(HH)	0.322	0.592	0.976	0.012	0.023	0.037				
		(LL)	0.462	0.902	1.584	0.009	0.014	0.022				
	G → Y	(HH)	0.324	0.602	1.000	0.012	0.023	0.036				
		(LL)	0.487	0.911	1.587	0.009	0.014	0.022				
	H → Y	(HL)	0.541	1.055	1.829	0.009	0.014	0.022				
		(LH)	0.404	0.739	1.245	0.012	0.023	0.037				
F238N1	A → Y	(HH)	0.288	0.529	0.878	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.460	0.863	1.488	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.296	0.539	0.888	0.006	0.011	0.018	C	1.0		
		(LL)	0.448	0.874	1.524	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.310	0.571	0.947	0.006	0.011	0.018	E	1.0		
		(LL)	0.483	0.906	1.565	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.318	0.581	0.961	0.006	0.011	0.018	G	1.0		
		(LL)	0.472	0.917	1.602	0.004	0.007	0.011	H	1.0		

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	E → Y	(HH)	0.338	0.626	1.038	0.006	0.011	0.018				
		(LL)	0.508	0.964	1.672	0.004	0.007	0.011				
	F → Y	(HH)	0.350	0.641	1.054	0.006	0.011	0.018				
		(LL)	0.495	0.974	1.711	0.004	0.007	0.011				
	G → Y	(HH)	0.352	0.652	1.081	0.006	0.011	0.018				
		(LL)	0.520	0.984	1.715	0.004	0.007	0.011				
	H → Y	(HL)	0.569	1.119	1.946	0.004	0.007	0.011				
		(LH)	0.425	0.778	1.306	0.006	0.011	0.018				
F218N2	A → Y	(HH)	0.262	0.485	0.801	0.012	0.023	0.037	A	1.0	Y	23
		(LL)	0.427	0.790	1.360	0.009	0.014	0.022	B	1.0		
	B → Y	(HH)	0.269	0.494	0.815	0.012	0.023	0.037	C	1.0		
		(LL)	0.415	0.802	1.397	0.009	0.014	0.022	D	1.0		
	C → Y	(HH)	0.283	0.525	0.870	0.012	0.023	0.037	E	1.0		
		(LL)	0.450	0.835	1.438	0.009	0.014	0.022	F	1.0		
	D → Y	(HH)	0.291	0.535	0.884	0.012	0.023	0.037	G	1.0		
		(LL)	0.438	0.845	1.475	0.009	0.014	0.022	H	1.0		
	E → Y	(HH)	0.310	0.577	0.958	0.012	0.023	0.037				
		(LL)	0.475	0.892	1.545	0.009	0.014	0.022				
	F → Y	(HH)	0.322	0.592	0.976	0.012	0.023	0.037				
		(LL)	0.462	0.902	1.583	0.009	0.014	0.022				
	G → Y	(HL)	0.535	1.029	1.779	0.009	0.014	0.022				
		(LH)	0.398	0.727	1.228	0.012	0.023	0.037				
	H → Y	(HL)	0.546	1.057	1.830	0.009	0.014	0.022				
		(LH)	0.401	0.735	1.239	0.012	0.023	0.037				
F238N2	A → Y	(HH)	0.288	0.529	0.876	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.460	0.863	1.488	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.296	0.539	0.888	0.006	0.011	0.018	C	1.0		
		(LL)	0.448	0.874	1.524	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.310	0.571	0.947	0.006	0.011	0.018	E	1.0		
		(LL)	0.483	0.906	1.565	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.318	0.581	0.961	0.006	0.011	0.018	G	1.0		
		(LL)	0.472	0.917	1.602	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.338	0.626	1.038	0.006	0.011	0.018				
		(LL)	0.508	0.964	1.672	0.004	0.007	0.011				
	F → Y	(HH)	0.350	0.641	1.054	0.006	0.011	0.018				
		(LL)	0.495	0.974	1.711	0.004	0.007	0.011				
	G → Y	(HL)	0.564	1.096	1.901	0.004	0.007	0.011				
		(LH)	0.421	0.769	1.291	0.006	0.011	0.018				
	H → Y	(HL)	0.581	1.132	1.957	0.004	0.007	0.011				
		(LH)	0.432	0.787	1.322	0.006	0.011	0.018				
F218N3	A → Y	(HH)	0.262	0.485	0.801	0.012	0.023	0.037	A	1.0	Y	23
		(LL)	0.427	0.790	1.360	0.009	0.014	0.022	B	1.0		
	B → Y	(HH)	0.269	0.494	0.815	0.012	0.023	0.037	C	1.0		
		(LL)	0.415	0.802	1.397	0.009	0.014	0.022	D	1.0		
	C → Y	(HH)	0.283	0.525	0.870	0.012	0.023	0.037	E	1.0		
		(LL)	0.450	0.835	1.438	0.009	0.014	0.022	F	1.0		
	D → Y	(HH)	0.291	0.535	0.884	0.012	0.023	0.037	G	1.0		
		(LL)	0.438	0.845	1.475	0.009	0.014	0.022	H	1.0		
	E → Y	(HH)	0.310	0.577	0.958	0.012	0.023	0.037				
		(LL)	0.475	0.893	1.549	0.009	0.014	0.022				
	F → Y	(HL)	0.533	1.037	1.789	0.009	0.014	0.022				
		(LH)	0.393	0.718	1.205	0.012	0.023	0.037				
	G → Y	(HL)	0.537	1.029	1.780	0.009	0.014	0.022				
		(LH)	0.402	0.735	1.238	0.012	0.023	0.036				
	H → Y	(HL)	0.545	1.056	1.827	0.009	0.014	0.022				
		(LH)	0.404	0.741	1.249	0.012	0.023	0.036				

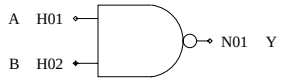
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F238N3	A → Y	(HH)	0.288	0.529	0.878	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.460	0.863	1.489	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.296	0.539	0.888	0.006	0.011	0.018	C	1.0		
		(LL)	0.448	0.874	1.524	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.310	0.571	0.947	0.006	0.011	0.018	E	1.0		
		(LL)	0.483	0.906	1.566	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.318	0.581	0.961	0.006	0.011	0.018	G	1.0		
		(LL)	0.472	0.917	1.602	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.338	0.626	1.036	0.006	0.011	0.018				
		(LL)	0.508	0.964	1.676	0.004	0.007	0.011				
	F → Y	(HL)	0.561	1.096	1.906	0.004	0.007	0.011				
		(LH)	0.413	0.753	1.263	0.006	0.011	0.018				
	G → Y	(HL)	0.564	1.093	1.895	0.004	0.007	0.011				
		(LH)	0.424	0.773	1.300	0.006	0.011	0.018				
	H → Y	(HL)	0.576	1.126	1.948	0.004	0.007	0.011				
		(LH)	0.434	0.791	1.326	0.006	0.011	0.018				

FUNCTION BLOCK

Function	2-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L302	1	L302N1	2								
x1	F302	2	F302N1	3								
x2	F322	4	F322N1	5								
x4	F382	6	F382N1	7								
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

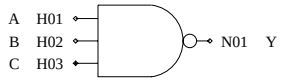
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t LD0 (ns)			t 1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L302	A → Y	(HL)	0.092	0.133	0.188	0.024	0.044	0.076	A	1.0	Y	11
		(LH)	0.074	0.112	0.150	0.024	0.045	0.073	B	1.0		
	B → Y	(HL)	0.076	0.119	0.195	0.024	0.044	0.076				
		(LH)	0.089	0.139	0.197	0.024	0.045	0.072				
F302	A → Y	(HL)	0.081	0.127	0.187	0.012	0.022	0.038	A	2.1	Y	22
		(LH)	0.083	0.126	0.178	0.012	0.023	0.036	B	2.1		
	B → Y	(HL)	0.082	0.128	0.189	0.012	0.022	0.038				
		(LH)	0.083	0.126	0.178	0.012	0.023	0.036				
F322	A → Y	(HL)	0.082	0.130	0.190	0.006	0.011	0.019	A	4.2	Y	45
		(LH)	0.082	0.126	0.179	0.006	0.011	0.018	B	4.2		
	B → Y	(HL)	0.081	0.128	0.190	0.006	0.011	0.019				
		(LH)	0.082	0.126	0.179	0.006	0.011	0.018				
F382	A → Y	(HL)	0.308	0.559	0.931	0.002	0.004	0.006	A	1.0	Y	90
		(LH)	0.273	0.468	0.765	0.003	0.006	0.009	B	1.0		
	B → Y	(HL)	0.295	0.548	0.934	0.002	0.004	0.006				
		(LH)	0.291	0.501	0.822	0.003	0.006	0.009				
L302N1	A → Y	(HL)	0.094	0.131	0.184	0.025	0.045	0.078	A	1.0	Y	11
		(LH)	0.072	0.111	0.155	0.024	0.045	0.072	B	1.0		
	B → Y	(HH)	0.136	0.240	0.370	0.025	0.045	0.073				
		(LL)	0.143	0.243	0.389	0.025	0.045	0.079				
F302N1	A → Y	(HL)	0.080	0.127	0.189	0.012	0.022	0.038	A	2.0	Y	22
		(LH)	0.081	0.123	0.173	0.012	0.023	0.036	B	1.0		
	B → Y	(HH)	0.158	0.267	0.404	0.012	0.023	0.036				
		(LL)	0.174	0.298	0.488	0.012	0.022	0.038				
F322N1	A → Y	(HL)	0.079	0.128	0.191	0.006	0.011	0.019	A	4.1	Y	44
		(LH)	0.080	0.122	0.172	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.219	0.351	0.534	0.006	0.011	0.018				
		(LL)	0.239	0.418	0.704	0.006	0.011	0.020				
F382N1	A → Y	(HL)	0.309	0.560	0.932	0.002	0.004	0.006	A	1.0	Y	90
		(LH)	0.273	0.468	0.764	0.003	0.006	0.009	B	1.0		
	B → Y	(HH)	0.334	0.602	0.996	0.003	0.006	0.009				
		(LL)	0.361	0.667	1.144	0.002	0.004	0.006				

FUNCTION BLOCK

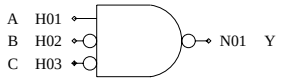
Function	3-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L303	2	L303N1	2	L303N2	3						
x1	F303	3	F303N1	4	F303N2	4						
x2	F323	6	F323N1	7	F323N2	7						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

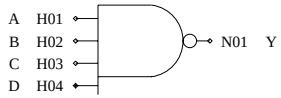
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L303	A → Y	(HL)	0.127	0.178	0.262	0.038	0.068	0.117		A	1.0	Y	8
		(LH)	0.083	0.132	0.189	0.025	0.045	0.073		B	1.0		
	B → Y	(HL)	0.121	0.192	0.305	0.038	0.068	0.117		C	1.0		
		(LH)	0.101	0.163	0.235	0.024	0.045	0.072					
	C → Y	(HL)	0.119	0.211	0.362	0.038	0.068	0.117					
		(LH)	0.122	0.200	0.301	0.024	0.045	0.073					
F303	A → Y	(HL)	0.116	0.189	0.294	0.020	0.035	0.060		A	2.1	Y	16
		(LH)	0.098	0.157	0.228	0.012	0.023	0.036		B	2.1		
	B → Y	(HL)	0.119	0.186	0.287	0.020	0.035	0.060		C	2.1		
		(LH)	0.095	0.155	0.225	0.012	0.022	0.036					
	C → Y	(HL)	0.116	0.189	0.294	0.020	0.035	0.060					
		(LH)	0.098	0.157	0.228	0.012	0.023	0.036					
F323	A → Y	(HL)	0.117	0.191	0.295	0.010	0.018	0.030		A	4.2	Y	32
		(LH)	0.098	0.158	0.227	0.006	0.011	0.018		B	4.2		
	B → Y	(HL)	0.120	0.187	0.289	0.010	0.018	0.030		C	4.2		
		(LH)	0.095	0.157	0.226	0.006	0.011	0.018					
	C → Y	(HL)	0.117	0.191	0.295	0.010	0.018	0.030					
		(LH)	0.098	0.158	0.227	0.006	0.011	0.018					
L303N1	A → Y	(HL)	0.123	0.177	0.262	0.039	0.069	0.118		A	1.0	Y	8
		(LH)	0.082	0.132	0.184	0.025	0.045	0.072		B	1.0		
	B → Y	(HL)	0.122	0.193	0.304	0.039	0.069	0.118		C	1.0		
		(LH)	0.099	0.160	0.233	0.025	0.046	0.073					
	C → Y	(HH)	0.160	0.291	0.458	0.025	0.046	0.073					
		(LL)	0.191	0.333	0.556	0.039	0.069	0.118					
F303N1	A → Y	(HL)	0.107	0.174	0.265	0.019	0.034	0.057		A	2.0	Y	17
		(LH)	0.091	0.147	0.211	0.012	0.023	0.037		B	2.1		
	B → Y	(HL)	0.109	0.189	0.297	0.019	0.034	0.057		C	1.0		
		(LH)	0.099	0.162	0.233	0.013	0.023	0.037					
	C → Y	(HH)	0.181	0.303	0.459	0.012	0.023	0.037					
		(LL)	0.206	0.358	0.584	0.019	0.034	0.057					
F323N1	A → Y	(HL)	0.124	0.206	0.320	0.010	0.018	0.030		A	4.2	Y	31
		(LH)	0.100	0.162	0.235	0.006	0.011	0.018		B	4.2		
	B → Y	(HL)	0.128	0.201	0.319	0.010	0.018	0.030		C	1.0		
		(LH)	0.097	0.159	0.232	0.006	0.011	0.018					
	C → Y	(HH)	0.243	0.397	0.605	0.006	0.011	0.018					
		(LL)	0.279	0.496	0.841	0.010	0.018	0.030					
L303N2	A → Y	(HL)	0.125	0.182	0.258	0.039	0.069	0.119		A	1.0	Y	8
		(LH)	0.083	0.133	0.186	0.025	0.045	0.072		B	1.0		
	B → Y	(HH)	0.146	0.259	0.403	0.024	0.045	0.072		C	1.0		
		(LL)	0.182	0.312	0.511	0.039	0.069	0.118					
	C → Y	(HH)	0.175	0.308	0.479	0.025	0.046	0.073					
		(LL)	0.201	0.349	0.577	0.039	0.069	0.118					
F303N2	A → Y	(HL)	0.107	0.175	0.268	0.019	0.034	0.057		A	2.0	Y	17
		(LH)	0.090	0.147	0.209	0.012	0.023	0.037		B	1.0		
	B → Y	(HH)	0.191	0.322	0.490	0.013	0.023	0.037		C	1.0		
		(LL)	0.215	0.378	0.626	0.019	0.034	0.058					
	C → Y	(HH)	0.179	0.301	0.456	0.012	0.023	0.037					
		(LL)	0.206	0.357	0.585	0.019	0.034	0.058					
F323N2	A → Y	(HL)	0.125	0.208	0.323	0.010	0.018	0.030		A	4.2	Y	31
		(LH)	0.100	0.161	0.233	0.006	0.011	0.018		B	1.0		
	B → Y	(HH)	0.239	0.390	0.599	0.006	0.011	0.018		C	1.0		
		(LL)	0.278	0.489	0.820	0.010	0.018	0.030					
	C → Y	(HH)	0.241	0.392	0.599	0.006	0.011	0.018					
		(LL)	0.278	0.496	0.837	0.010	0.018	0.030					

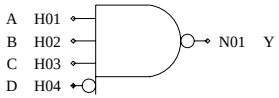
FUNCTION BLOCK

Function	4-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L304	2	L304N1	3	L304N2	3						
x1	F304	4	F304N1	5	F304N2	5						
x2	F324	8	F324N1	9	F324N2	9						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

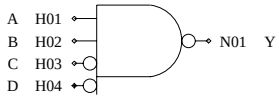
Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Path		Switching speed t_{LD0} (ns)			Switching speed t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L304	A → Y	(HL)	0.131	0.191	0.282	0.045	0.085	0.147	A	1.0	Y	6
		(LH)	0.085	0.137	0.191	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.136	0.219	0.351	0.045	0.085	0.147	C	1.0		
		(LH)	0.100	0.165	0.242	0.025	0.045	0.072	D	1.0		
	C → Y	(HL)	0.146	0.273	0.454	0.045	0.085	0.147				
		(LH)	0.123	0.203	0.307	0.024	0.045	0.073				
	D → Y	(HL)	0.146	0.268	0.470	0.045	0.085	0.147				
		(LH)	0.131	0.217	0.334	0.025	0.045	0.073				
F304	A → Y	(HL)	0.139	0.242	0.376	0.023	0.042	0.073	A	2.2	Y	12
		(LH)	0.108	0.178	0.261	0.012	0.023	0.036	B	2.1		
	B → Y	(HL)	0.143	0.255	0.404	0.023	0.042	0.073	C	2.1		
		(LH)	0.112	0.185	0.273	0.012	0.023	0.036	D	2.1		
	C → Y	(HL)	0.146	0.257	0.409	0.023	0.042	0.073				
		(LH)	0.113	0.185	0.277	0.012	0.023	0.036				
	D → Y	(HL)	0.141	0.241	0.382	0.023	0.042	0.073				
		(LH)	0.109	0.179	0.263	0.012	0.023	0.036				
F324	A → Y	(HL)	0.139	0.238	0.380	0.011	0.021	0.037	A	4.4	Y	25
		(LH)	0.107	0.176	0.256	0.006	0.011	0.018	B	4.4		
	B → Y	(HL)	0.142	0.251	0.408	0.011	0.021	0.037	C	4.4		
		(LH)	0.112	0.184	0.274	0.006	0.011	0.018	D	4.4		
	C → Y	(HL)	0.144	0.252	0.409	0.011	0.021	0.037				
		(LH)	0.112	0.185	0.273	0.006	0.011	0.018				
	D → Y	(HL)	0.140	0.240	0.380	0.011	0.021	0.037				
		(LH)	0.108	0.177	0.257	0.006	0.011	0.018				
L304N1	A → Y	(HL)	0.129	0.186	0.274	0.045	0.084	0.147	A	1.0	Y	6
		(LH)	0.083	0.133	0.190	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.133	0.218	0.346	0.045	0.084	0.147	C	1.0		
		(LH)	0.099	0.164	0.240	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.140	0.265	0.431	0.045	0.084	0.147				
		(LH)	0.121	0.201	0.298	0.025	0.046	0.073				
	D → Y	(HH)	0.174	0.314	0.496	0.025	0.045	0.073				
		(LL)	0.219	0.394	0.659	0.045	0.084	0.147				
F304N1	A → Y	(HL)	0.140	0.241	0.383	0.023	0.042	0.074	A	2.1	Y	12
		(LH)	0.108	0.175	0.258	0.012	0.023	0.037	B	2.1		
	B → Y	(HL)	0.143	0.251	0.409	0.023	0.042	0.074	C	2.1		
		(LH)	0.112	0.184	0.275	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.143	0.253	0.408	0.023	0.042	0.074				
		(LH)	0.112	0.184	0.274	0.012	0.023	0.037				
	D → Y	(HH)	0.199	0.336	0.511	0.012	0.023	0.037				
		(LL)	0.241	0.428	0.708	0.023	0.042	0.074				
F324N1	A → Y	(HL)	0.141	0.242	0.389	0.011	0.021	0.037	A	4.3	Y	25
		(LH)	0.109	0.177	0.258	0.006	0.011	0.018	B	4.3		
	B → Y	(HL)	0.145	0.255	0.415	0.011	0.021	0.037	C	4.3		
		(LH)	0.113	0.185	0.275	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.144	0.255	0.415	0.011	0.021	0.037				
		(LH)	0.112	0.184	0.274	0.006	0.011	0.018				
	D → Y	(HH)	0.255	0.417	0.639	0.006	0.012	0.018				
		(LL)	0.300	0.545	0.921	0.011	0.021	0.037				
L304N2	A → Y	(HL)	0.129	0.188	0.274	0.045	0.084	0.147	A	1.0	Y	6
		(LH)	0.083	0.133	0.190	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.134	0.218	0.344	0.045	0.085	0.147	C	1.0		
		(LH)	0.099	0.164	0.240	0.025	0.045	0.073	D	1.0		
	C → Y	(HH)	0.174	0.308	0.481	0.025	0.046	0.073				
		(LL)	0.214	0.384	0.641	0.045	0.084	0.147				
	D → Y	(HH)	0.182	0.324	0.506	0.025	0.045	0.073				
		(LL)	0.223	0.405	0.671	0.045	0.084	0.147				

FUNCTION BLOCK

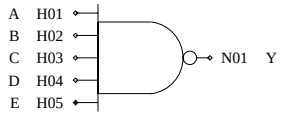
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F304N2	A → Y	(HL)	0.140	0.242	0.387	0.023	0.042	0.074	A	2.1	Y	12
		(LH)	0.107	0.175	0.257	0.012	0.023	0.037	B	2.1		
	B → Y	(HL)	0.144	0.254	0.409	0.023	0.042	0.074	C	1.0		
		(LH)	0.112	0.184	0.274	0.013	0.023	0.037	D	1.0		
	C → Y	(HH)	0.204	0.346	0.529	0.013	0.023	0.037				
		(LL)	0.246	0.439	0.733	0.023	0.042	0.074				
	D → Y	(HH)	0.196	0.331	0.505	0.012	0.023	0.037				
		(LL)	0.238	0.425	0.701	0.023	0.042	0.074				
F324N2	A → Y	(HL)	0.142	0.245	0.392	0.011	0.021	0.037	A	4.3	Y	24
		(LH)	0.108	0.176	0.257	0.006	0.011	0.018	B	4.3		
	B → Y	(HL)	0.145	0.257	0.418	0.011	0.021	0.037	C	1.0		
		(LH)	0.112	0.184	0.273	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.253	0.415	0.640	0.006	0.011	0.018				
		(LL)	0.297	0.538	0.911	0.011	0.021	0.037				
	D → Y	(HH)	0.252	0.413	0.633	0.006	0.012	0.018				
		(LL)	0.299	0.544	0.919	0.011	0.021	0.037				

[MEMO]

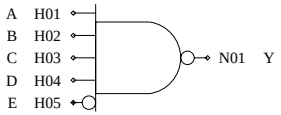
FUNCTION BLOCK

Function	5-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L305	3	L305N1	3	L305N2	4	L305N3	4				
x1	F305	5	F305N1	5	F305N2	6	F305N3	6				
x2	F325	6	F325N1	6	F325N2	7	F325N3	7				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

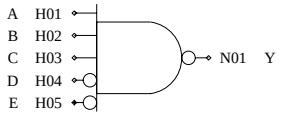
Logic Diagram for "Normal type"



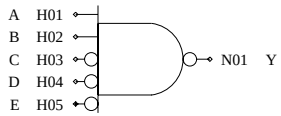
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L305	A → Y	(HL)	0.162	0.245	0.371	0.059	0.108	0.186	A	1.0	Y	4
		(LH)	0.094	0.155	0.219	0.025	0.045	0.073	B	1.0		
	B → Y	(HL)	0.178	0.291	0.474	0.059	0.108	0.186	C	1.0		
		(LH)	0.112	0.184	0.275	0.025	0.046	0.073	D	1.0		
	C → Y	(HL)	0.209	0.381	0.625	0.059	0.109	0.186	E	1.0		
		(LH)	0.135	0.221	0.340	0.025	0.046	0.073				
	D → Y	(HL)	0.219	0.408	0.670	0.059	0.109	0.186				
		(LH)	0.144	0.240	0.370	0.025	0.046	0.074				
	E → Y	(HL)	0.226	0.432	0.723	0.059	0.109	0.186				
		(LH)	0.153	0.260	0.398	0.025	0.046	0.074				
F305	A → Y	(HL)	0.346	0.678	1.157	0.009	0.015	0.024	A	1.0	Y	22
		(LH)	0.230	0.397	0.637	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.335	0.665	1.165	0.009	0.015	0.024	C	1.0		
		(LH)	0.250	0.431	0.696	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.420	0.805	1.368	0.009	0.015	0.024	E	1.0		
		(LH)	0.257	0.454	0.736	0.013	0.023	0.037				
	D → Y	(HL)	0.422	0.816	1.412	0.009	0.015	0.024				
		(LH)	0.278	0.490	0.797	0.013	0.023	0.037				
	E → Y	(HL)	0.417	0.836	1.460	0.009	0.015	0.024				
		(LH)	0.307	0.541	0.875	0.013	0.023	0.037				
F325	A → Y	(HL)	0.384	0.763	1.338	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.243	0.418	0.677	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.373	0.756	1.348	0.005	0.008	0.013	C	1.0		
		(LH)	0.265	0.454	0.736	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.454	0.878	1.529	0.005	0.008	0.013	E	1.0		
		(LH)	0.269	0.469	0.763	0.006	0.011	0.018				
	D → Y	(HL)	0.456	0.892	1.569	0.005	0.008	0.013				
		(LH)	0.293	0.509	0.833	0.006	0.011	0.018				
	E → Y	(HL)	0.447	0.910	1.612	0.005	0.008	0.013				
		(LH)	0.318	0.557	0.905	0.006	0.011	0.018				
L305N1	A → Y	(HL)	0.161	0.237	0.364	0.060	0.110	0.188	A	1.0	Y	3
		(LH)	0.094	0.153	0.221	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.180	0.287	0.462	0.060	0.110	0.188	C	1.0		
		(LH)	0.110	0.183	0.270	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.210	0.375	0.618	0.060	0.110	0.188	E	1.0		
		(LH)	0.133	0.222	0.336	0.025	0.046	0.073				
	D → Y	(HL)	0.221	0.405	0.666	0.060	0.110	0.188				
		(LH)	0.142	0.239	0.366	0.025	0.046	0.074				
	E → Y	(HH)	0.194	0.355	0.566	0.025	0.046	0.074				
		(LL)	0.303	0.552	0.916	0.060	0.110	0.188				
F305N1	A → Y	(HL)	0.296	0.575	0.989	0.009	0.015	0.025	A	1.0	Y	22
		(LH)	0.207	0.355	0.570	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.288	0.567	0.993	0.009	0.015	0.025	C	1.0		
		(LH)	0.226	0.389	0.626	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.373	0.695	1.185	0.009	0.015	0.025	E	1.0		
		(LH)	0.227	0.398	0.648	0.012	0.023	0.037				
	D → Y	(HL)	0.375	0.709	1.231	0.010	0.015	0.025				
		(LH)	0.249	0.438	0.717	0.012	0.023	0.037				
	E → Y	(HH)	0.317	0.585	0.967	0.012	0.023	0.036				
		(LL)	0.444	0.859	1.485	0.009	0.015	0.025				
F325N1	A → Y	(HL)	0.384	0.763	1.338	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.243	0.418	0.677	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.373	0.756	1.348	0.005	0.008	0.013	C	1.0		
		(LH)	0.265	0.454	0.736	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.458	0.881	1.531	0.005	0.008	0.013	E	1.0		
		(LH)	0.269	0.469	0.763	0.006	0.011	0.018				

FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	D → Y	(HL)	0.460	0.896	1.574	0.005	0.008	0.013				
		(LH)	0.293	0.510	0.833	0.006	0.011	0.018				
	E → Y	(HH)	0.362	0.658	1.081	0.006	0.011	0.018				
		(LL)	0.527	1.042	1.827	0.005	0.008	0.013				
L305N2	A → Y	(HL)	0.161	0.237	0.362	0.060	0.109	0.188	A	1.0	Y	3
		(LH)	0.094	0.152	0.218	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.178	0.287	0.461	0.060	0.110	0.188	C	1.0		
		(LH)	0.110	0.183	0.270	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.210	0.374	0.618	0.060	0.110	0.188	E	1.0		
		(LH)	0.133	0.222	0.336	0.025	0.046	0.073				
	D → Y	(HH)	0.203	0.358	0.560	0.025	0.046	0.074				
		(LL)	0.301	0.539	0.898	0.060	0.110	0.188				
	E → Y	(HH)	0.194	0.354	0.564	0.025	0.046	0.074				
		(LL)	0.307	0.554	0.919	0.060	0.110	0.188				
F305N2	A → Y	(HL)	0.296	0.575	0.989	0.009	0.015	0.025	A	1.0	Y	22
		(LH)	0.207	0.355	0.570	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.288	0.567	0.993	0.009	0.015	0.025	C	1.0		
		(LH)	0.226	0.389	0.626	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.372	0.696	1.186	0.010	0.015	0.025	E	1.0		
		(LH)	0.227	0.398	0.648	0.012	0.023	0.037				
	D → Y	(HH)	0.307	0.554	0.908	0.012	0.023	0.037				
		(LL)	0.437	0.842	1.460	0.010	0.015	0.025				
	E → Y	(HH)	0.316	0.586	0.966	0.012	0.023	0.036				
		(LL)	0.445	0.861	1.496	0.010	0.015	0.025				
F325N2	A → Y	(HL)	0.384	0.763	1.338	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.243	0.418	0.677	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.373	0.756	1.348	0.005	0.008	0.013	C	1.0		
		(LH)	0.265	0.454	0.736	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.456	0.881	1.530	0.005	0.008	0.013	E	1.0		
		(LH)	0.269	0.469	0.762	0.006	0.011	0.018				
	D → Y	(HH)	0.338	0.609	1.003	0.006	0.011	0.018				
		(LL)	0.518	1.018	1.780	0.005	0.008	0.013				
	E → Y	(HH)	0.376	0.675	1.102	0.006	0.011	0.018				
		(LL)	0.538	1.057	1.855	0.005	0.008	0.013				
L305N3	A → Y	(HL)	0.160	0.236	0.362	0.060	0.110	0.188	A	1.0	Y	3
		(LH)	0.094	0.153	0.218	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.177	0.286	0.462	0.060	0.110	0.188	C	1.0		
		(LH)	0.110	0.183	0.269	0.025	0.045	0.073	D	1.0		
	C → Y	(HH)	0.191	0.336	0.526	0.025	0.046	0.073	E	1.0		
		(LL)	0.282	0.505	0.836	0.060	0.110	0.188				
	D → Y	(HH)	0.200	0.354	0.555	0.025	0.046	0.074				
		(LL)	0.303	0.540	0.896	0.060	0.110	0.188				
	E → Y	(HH)	0.193	0.354	0.563	0.025	0.046	0.074				
		(LL)	0.308	0.557	0.926	0.060	0.110	0.188				
F305N3	A → Y	(HL)	0.296	0.575	0.989	0.009	0.015	0.025	A	1.0	Y	22
		(LH)	0.207	0.355	0.571	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.288	0.567	0.993	0.009	0.015	0.025	C	1.0		
		(LH)	0.226	0.389	0.626	0.012	0.023	0.037	D	1.0		
	C → Y	(HH)	0.284	0.509	0.835	0.013	0.023	0.037	E	1.0		
		(LL)	0.425	0.814	1.413	0.010	0.015	0.025				
	D → Y	(HH)	0.293	0.536	0.888	0.013	0.023	0.036				
		(LL)	0.432	0.833	1.446	0.010	0.015	0.025				
	E → Y	(HH)	0.328	0.598	0.982	0.012	0.023	0.036				
		(LL)	0.454	0.874	1.510	0.009	0.015	0.025				

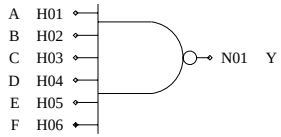
FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F325N3	A → Y	(HL)	0.384	0.763	1.338	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.243	0.418	0.677	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.373	0.756	1.348	0.005	0.008	0.013	C	1.0		
		(LH)	0.265	0.454	0.736	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.327	0.581	0.954	0.006	0.011	0.018	E	1.0		
		(LL)	0.511	1.006	1.760	0.005	0.008	0.013				
	D → Y	(HH)	0.337	0.609	1.003	0.006	0.011	0.018				
		(LL)	0.517	1.019	1.788	0.005	0.008	0.013				
	E → Y	(HH)	0.375	0.675	1.102	0.006	0.011	0.018				
		(LL)	0.540	1.059	1.861	0.005	0.008	0.013				

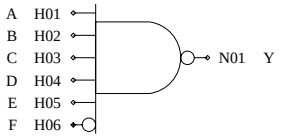
FUNCTION BLOCK

Function	6-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L306	3	L306N1	4	L306N2	4	L306N3	5				
x1	F306	6	F306N1	6	F306N2	6	F306N3	7				
x2	F326	6	F326N1	7	F326N2	7	F326N3	8				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

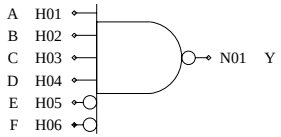
Logic Diagram for "Normal type"



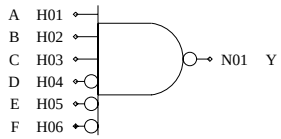
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L306	A → Y	(HL)	0.167	0.247	0.382	0.066	0.125	0.215		A	1.0	Y	3
		(LH)	0.095	0.158	0.223	0.025	0.045	0.073		B	1.0		
	B → Y	(HL)	0.190	0.308	0.507	0.067	0.125	0.215		C	1.0		
		(LH)	0.113	0.186	0.276	0.025	0.046	0.073		D	1.0		
	C → Y	(HL)	0.231	0.423	0.703	0.067	0.125	0.215		E	1.0		
		(LH)	0.136	0.226	0.346	0.025	0.046	0.073		F	1.0		
	D → Y	(HL)	0.249	0.464	0.769	0.067	0.125	0.215					
		(LH)	0.145	0.244	0.376	0.025	0.046	0.074					
	E → Y	(HL)	0.267	0.518	0.866	0.067	0.125	0.215					
		(LH)	0.157	0.265	0.410	0.025	0.046	0.074					
	F → Y	(HL)	0.269	0.519	0.878	0.067	0.125	0.215					
		(LH)	0.157	0.267	0.417	0.025	0.046	0.074					
F306	A → Y	(HL)	0.421	0.793	1.344	0.010	0.016	0.026		A	1.0	Y	22
		(LH)	0.243	0.430	0.697	0.012	0.023	0.036		B	1.0		
	B → Y	(HL)	0.425	0.805	1.383	0.010	0.016	0.026		C	1.0		
		(LH)	0.264	0.465	0.756	0.012	0.023	0.036		D	1.0		
	C → Y	(HL)	0.417	0.827	1.440	0.010	0.016	0.026		E	1.0		
		(LH)	0.293	0.517	0.838	0.012	0.023	0.036		F	1.0		
	D → Y	(HL)	0.429	0.811	1.390	0.010	0.016	0.026					
		(LH)	0.260	0.456	0.747	0.012	0.023	0.036					
	E → Y	(HL)	0.428	0.829	1.429	0.010	0.016	0.026					
		(LH)	0.279	0.492	0.803	0.012	0.023	0.036					
	F → Y	(HL)	0.425	0.846	1.479	0.010	0.016	0.026					
		(LH)	0.307	0.544	0.883	0.012	0.023	0.036					
F326	A → Y	(HL)	0.456	0.874	1.504	0.005	0.008	0.013		A	1.0	Y	45
		(LH)	0.257	0.448	0.731	0.006	0.011	0.018		B	1.0		
	B → Y	(HL)	0.459	0.884	1.544	0.005	0.008	0.013		C	1.0		
		(LH)	0.281	0.489	0.798	0.006	0.011	0.018		D	1.0		
	C → Y	(HL)	0.450	0.903	1.596	0.005	0.008	0.013		E	1.0		
		(LH)	0.308	0.537	0.874	0.006	0.011	0.018		F	1.0		
	D → Y	(HL)	0.460	0.888	1.538	0.005	0.008	0.013					
		(LH)	0.264	0.463	0.759	0.006	0.011	0.018					
	E → Y	(HL)	0.463	0.904	1.581	0.005	0.008	0.013					
		(LH)	0.288	0.503	0.826	0.006	0.011	0.018					
	F → Y	(HL)	0.454	0.922	1.628	0.005	0.008	0.013					
		(LH)	0.313	0.550	0.899	0.006	0.011	0.018					
L306N1	A → Y	(HL)	0.164	0.240	0.368	0.066	0.125	0.215		A	1.0	Y	3
		(LH)	0.095	0.155	0.223	0.025	0.045	0.072		B	1.0		
	B → Y	(HL)	0.184	0.302	0.492	0.066	0.125	0.215		C	1.0		
		(LH)	0.112	0.185	0.272	0.025	0.045	0.073		D	1.0		
	C → Y	(HL)	0.228	0.413	0.684	0.066	0.125	0.215		E	1.0		
		(LH)	0.133	0.225	0.341	0.025	0.046	0.073		F	1.0		
	D → Y	(HL)	0.247	0.456	0.756	0.066	0.125	0.215					
		(LH)	0.143	0.243	0.371	0.025	0.046	0.074					
	E → Y	(HL)	0.263	0.507	0.846	0.066	0.125	0.215					
		(LH)	0.154	0.263	0.405	0.025	0.046	0.074					
	F → Y	(HH)	0.216	0.385	0.608	0.025	0.046	0.074					
		(LL)	0.357	0.654	1.096	0.066	0.125	0.215					
F306N1	A → Y	(HL)	0.366	0.684	1.152	0.010	0.015	0.025		A	1.0	Y	22
		(LH)	0.218	0.384	0.620	0.012	0.023	0.037		B	1.0		
	B → Y	(HL)	0.370	0.697	1.192	0.009	0.015	0.025		C	1.0		
		(LH)	0.240	0.420	0.683	0.012	0.023	0.037		D	1.0		
	C → Y	(HL)	0.360	0.711	1.240	0.010	0.015	0.025		E	1.0		
		(LH)	0.263	0.464	0.754	0.012	0.023	0.037		F	1.0		
	D → Y	(HL)	0.373	0.701	1.190	0.010	0.015	0.025					
		(LH)	0.227	0.398	0.655	0.012	0.023	0.036					

FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed: t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	E → Y	(HL)	0.375	0.713	1.233	0.009	0.015	0.025				
		(LH)	0.250	0.438	0.720	0.012	0.023	0.036				
	F → Y	(HH)	0.329	0.600	0.984	0.012	0.023	0.036				
		(LL)	0.451	0.868	1.505	0.010	0.015	0.025				
F326N1	A → Y	(HL)	0.456	0.874	1.504	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.257	0.448	0.731	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.459	0.884	1.544	0.005	0.008	0.013	C	1.0		
		(LH)	0.281	0.489	0.798	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.450	0.903	1.596	0.005	0.008	0.013	E	1.0		
		(LH)	0.308	0.537	0.874	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.460	0.890	1.538	0.005	0.008	0.013				
		(LH)	0.264	0.463	0.759	0.006	0.011	0.018				
	E → Y	(HL)	0.462	0.904	1.581	0.005	0.008	0.013				
		(LH)	0.288	0.503	0.825	0.006	0.011	0.018				
	F → Y	(HH)	0.369	0.667	1.093	0.006	0.011	0.018				
		(LL)	0.540	1.055	1.858	0.005	0.008	0.013				
L306N2	A → Y	(HL)	0.164	0.239	0.367	0.066	0.125	0.215	A	1.0	Y	3
		(LH)	0.095	0.155	0.223	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.184	0.302	0.492	0.066	0.125	0.215	C	1.0		
		(LH)	0.112	0.185	0.272	0.025	0.045	0.073	D	1.0		
	C → Y	(HL)	0.228	0.413	0.683	0.066	0.125	0.215	E	1.0		
		(LH)	0.133	0.225	0.341	0.025	0.046	0.073	F	1.0		
	D → Y	(HL)	0.247	0.456	0.758	0.066	0.125	0.215				
		(LH)	0.143	0.243	0.371	0.025	0.046	0.074				
	E → Y	(HH)	0.213	0.379	0.597	0.025	0.046	0.074				
		(LL)	0.349	0.640	1.068	0.066	0.125	0.215				
	F → Y	(HH)	0.214	0.383	0.605	0.025	0.046	0.074				
		(LL)	0.358	0.656	1.099	0.066	0.125	0.215				
F306N2	A → Y	(HL)	0.366	0.684	1.152	0.010	0.015	0.025	A	1.0	Y	22
		(LH)	0.218	0.384	0.620	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.370	0.697	1.192	0.009	0.015	0.025	C	1.0		
		(LH)	0.240	0.420	0.683	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.360	0.711	1.240	0.010	0.015	0.025	E	1.0		
		(LH)	0.263	0.464	0.754	0.012	0.023	0.037	F	1.0		
	D → Y	(HL)	0.374	0.701	1.191	0.009	0.015	0.025				
		(LH)	0.228	0.399	0.657	0.012	0.023	0.036				
	E → Y	(HH)	0.303	0.547	0.901	0.012	0.023	0.037				
		(LL)	0.433	0.835	1.445	0.009	0.015	0.025				
	F → Y	(HH)	0.328	0.598	0.983	0.012	0.023	0.036				
		(LL)	0.453	0.872	1.511	0.009	0.015	0.025				
F326N2	A → Y	(HL)	0.456	0.874	1.504	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.257	0.448	0.731	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.459	0.884	1.544	0.005	0.008	0.013	C	1.0		
		(LH)	0.281	0.489	0.798	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.450	0.903	1.596	0.005	0.008	0.013	E	1.0		
		(LH)	0.308	0.537	0.874	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.459	0.890	1.538	0.005	0.008	0.013				
		(LH)	0.264	0.463	0.759	0.006	0.011	0.018				
	E → Y	(HH)	0.344	0.616	1.015	0.006	0.011	0.018				
		(LL)	0.525	1.032	1.804	0.005	0.008	0.013				
	F → Y	(HH)	0.366	0.661	1.087	0.006	0.011	0.018				
		(LL)	0.538	1.055	1.851	0.005	0.008	0.013				
L306N3	A → Y	(HL)	0.164	0.238	0.368	0.066	0.125	0.215	A	1.0	Y	3
		(LH)	0.095	0.155	0.221	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.183	0.302	0.491	0.066	0.125	0.215	C	1.0		
		(LH)	0.111	0.185	0.272	0.025	0.045	0.073	D	1.0		

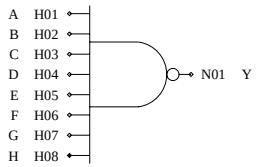
FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed: t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	C → Y	(HL)	0.228	0.413	0.683	0.066	0.125	0.215	E	1.0		
		(LH)	0.133	0.225	0.341	0.025	0.046	0.073	F	1.0		
	D → Y	(HH)	0.198	0.352	0.552	0.025	0.046	0.074				
		(LL)	0.317	0.578	0.965	0.066	0.125	0.215				
	E → Y	(HH)	0.213	0.379	0.596	0.025	0.046	0.074				
		(LL)	0.351	0.644	1.077	0.066	0.125	0.215				
	F → Y	(HH)	0.212	0.381	0.601	0.025	0.046	0.074				
		(LL)	0.357	0.655	1.100	0.066	0.125	0.215				
F306N3	A → Y	(HL)	0.366	0.684	1.152	0.010	0.015	0.025	A	1.0	Y	22
		(LH)	0.218	0.384	0.620	0.012	0.023	0.037	B	1.0		
	B → Y	(HL)	0.370	0.697	1.192	0.009	0.015	0.025	C	1.0		
		(LH)	0.240	0.420	0.683	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.360	0.711	1.240	0.010	0.015	0.025	E	1.0		
		(LH)	0.263	0.464	0.754	0.012	0.023	0.037	F	1.0		
	D → Y	(HH)	0.281	0.506	0.833	0.012	0.023	0.037				
		(LL)	0.421	0.811	1.405	0.009	0.015	0.025				
	E → Y	(HH)	0.306	0.553	0.909	0.012	0.023	0.037				
		(LL)	0.441	0.847	1.469	0.009	0.015	0.025				
	F → Y	(HH)	0.329	0.599	0.986	0.012	0.023	0.036				
		(LL)	0.456	0.878	1.523	0.009	0.015	0.025				
F326N3	A → Y	(HL)	0.456	0.874	1.504	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.257	0.448	0.731	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.459	0.884	1.544	0.005	0.008	0.013	C	1.0		
		(LH)	0.281	0.489	0.798	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.450	0.903	1.595	0.005	0.008	0.013	E	1.0		
		(LH)	0.308	0.538	0.874	0.006	0.011	0.018	F	1.0		
	D → Y	(HH)	0.317	0.566	0.936	0.006	0.011	0.018				
		(LL)	0.506	0.997	1.749	0.005	0.008	0.013				
	E → Y	(HH)	0.344	0.616	1.015	0.006	0.011	0.018				
		(LL)	0.528	1.034	1.817	0.005	0.008	0.013				
	F → Y	(HH)	0.370	0.668	1.097	0.006	0.011	0.018				
		(LL)	0.541	1.064	1.874	0.005	0.008	0.013				

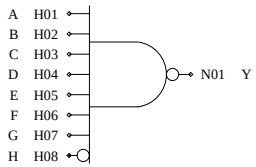
FUNCTION BLOCK

Function	8-INPUT NAND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1	F308	6	F308N1	7	F308N2	7	F308N3	8	F308N4	8		
x2	F328	7	F328N1	8	F328N2	8	F328N3	9	F328N4	9		
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

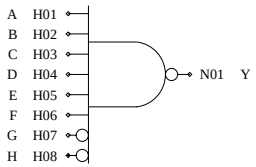
Logic Diagram for "Normal type"



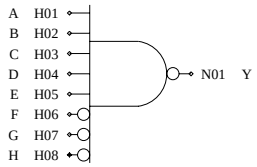
Logic Diagram for "with 1 inverter type"



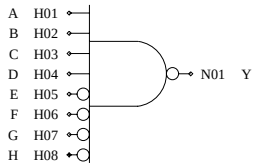
Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"



FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F308	A → Y	(HL)	0.450	0.844	1.437	0.010	0.016	0.026	A	1.0	Y	22
		(LH)	0.245	0.432	0.709	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.458	0.869	1.501	0.010	0.016	0.026	C	1.0		
		(LH)	0.265	0.469	0.770	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.465	0.926	1.605	0.010	0.016	0.026	E	1.0		
		(LH)	0.294	0.523	0.854	0.013	0.023	0.037	F	1.0		
	D → Y	(HL)	0.464	0.931	1.616	0.010	0.016	0.026	G	1.0		
		(LH)	0.304	0.542	0.888	0.013	0.023	0.037	H	1.0		
	E → Y	(HL)	0.430	0.815	1.398	0.010	0.016	0.026				
		(LH)	0.247	0.433	0.707	0.013	0.023	0.037				
	F → Y	(HL)	0.437	0.843	1.459	0.010	0.016	0.026				
		(LH)	0.268	0.470	0.769	0.013	0.023	0.037				
	G → Y	(HL)	0.446	0.897	1.565	0.010	0.016	0.026				
		(LH)	0.297	0.525	0.856	0.013	0.023	0.037				
	H → Y	(HL)	0.444	0.900	1.578	0.010	0.016	0.026				
		(LH)	0.308	0.547	0.891	0.013	0.023	0.037				
F328	A → Y	(HL)	0.487	0.936	1.617	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.256	0.451	0.737	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.497	0.962	1.682	0.005	0.008	0.013	C	1.0		
		(LH)	0.280	0.489	0.800	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.500	1.009	1.776	0.005	0.008	0.013	E	1.0		
		(LH)	0.309	0.543	0.881	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.498	1.011	1.793	0.005	0.008	0.013	G	1.0		
		(LH)	0.316	0.561	0.912	0.006	0.011	0.018	H	1.0		
	E → Y	(HL)	0.477	0.927	1.609	0.005	0.008	0.013				
		(LH)	0.262	0.459	0.749	0.006	0.011	0.018				
	F → Y	(HL)	0.485	0.954	1.676	0.005	0.008	0.013				
		(LH)	0.287	0.501	0.820	0.006	0.011	0.018				
	G → Y	(HL)	0.490	0.999	1.769	0.005	0.008	0.013				
		(LH)	0.316	0.555	0.902	0.006	0.011	0.018				
	H → Y	(HL)	0.490	1.007	1.787	0.005	0.008	0.013				
		(LH)	0.326	0.573	0.935	0.006	0.011	0.018				
F308N1	A → Y	(HL)	0.398	0.740	1.251	0.009	0.015	0.024	A	1.0	Y	23
		(LH)	0.219	0.388	0.632	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.407	0.766	1.318	0.009	0.015	0.024	C	1.0		
		(LH)	0.240	0.425	0.693	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.411	0.812	1.409	0.009	0.015	0.024	E	1.0		
		(LH)	0.266	0.475	0.770	0.012	0.023	0.037	F	1.0		
	D → Y	(HL)	0.409	0.815	1.428	0.009	0.015	0.024	G	1.0		
		(LH)	0.274	0.490	0.802	0.012	0.023	0.036	H	1.0		
	E → Y	(HL)	0.381	0.716	1.218	0.009	0.015	0.024				
		(LH)	0.222	0.391	0.634	0.012	0.023	0.037				
	F → Y	(HL)	0.388	0.744	1.296	0.009	0.015	0.024				
		(LH)	0.243	0.427	0.698	0.012	0.023	0.037				
	G → Y	(HL)	0.394	0.791	1.378	0.009	0.015	0.024				
		(LH)	0.271	0.478	0.775	0.012	0.023	0.037				
	H → Y	(HH)	0.324	0.597	0.985	0.012	0.023	0.036				
		(LL)	0.471	0.920	1.599	0.009	0.015	0.024				
F328N1	A → Y	(HL)	0.487	0.936	1.617	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.256	0.451	0.737	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.497	0.962	1.682	0.005	0.008	0.013	C	1.0		
		(LH)	0.280	0.489	0.800	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.500	1.009	1.776	0.005	0.008	0.013	E	1.0		
		(LH)	0.309	0.543	0.881	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.498	1.011	1.793	0.005	0.008	0.013	G	1.0		
		(LH)	0.316	0.561	0.912	0.006	0.011	0.018	H	1.0		

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	E → Y	(HL)	0.477	0.925	1.609	0.005	0.008	0.013				
		(LH)	0.262	0.459	0.749	0.006	0.011	0.018				
	F → Y	(HL)	0.485	0.954	1.676	0.005	0.008	0.013				
		(LH)	0.287	0.501	0.820	0.006	0.011	0.018				
	G → Y	(HL)	0.491	0.999	1.768	0.005	0.008	0.013				
		(LH)	0.316	0.555	0.902	0.006	0.011	0.018				
	H → Y	(HH)	0.377	0.682	1.120	0.006	0.011	0.018				
		(LL)	0.570	1.131	1.998	0.005	0.008	0.013				
F308N2	A → Y	(HL)	0.398	0.740	1.251	0.009	0.015	0.024	A	1.0	Y	23
		(LH)	0.219	0.388	0.632	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.407	0.766	1.318	0.009	0.015	0.024	C	1.0		
		(LH)	0.240	0.425	0.693	0.013	0.023	0.037	D	1.0		
	C → Y	(HL)	0.411	0.812	1.409	0.009	0.015	0.024	E	1.0		
		(LH)	0.266	0.475	0.770	0.012	0.023	0.037	F	1.0		
	D → Y	(HL)	0.409	0.815	1.428	0.009	0.015	0.024	G	1.0		
		(LH)	0.274	0.490	0.802	0.012	0.023	0.036	H	1.0		
	E → Y	(HL)	0.381	0.715	1.224	0.009	0.015	0.024				
		(LH)	0.222	0.391	0.634	0.012	0.023	0.037				
	F → Y	(HL)	0.389	0.744	1.296	0.009	0.015	0.024				
		(LH)	0.243	0.429	0.698	0.012	0.023	0.037				
	G → Y	(HH)	0.322	0.587	0.960	0.012	0.023	0.037				
		(LL)	0.467	0.910	1.586	0.009	0.015	0.024				
	H → Y	(HH)	0.332	0.606	0.995	0.012	0.023	0.036				
		(LL)	0.477	0.932	1.617	0.009	0.015	0.024				
F328N2	A → Y	(HL)	0.487	0.936	1.617	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.256	0.451	0.737	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.497	0.962	1.682	0.005	0.008	0.013	C	1.0		
		(LH)	0.280	0.489	0.800	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.500	1.009	1.776	0.005	0.008	0.013	E	1.0		
		(LH)	0.309	0.543	0.881	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.498	1.011	1.793	0.005	0.008	0.013	G	1.0		
		(LH)	0.316	0.561	0.912	0.006	0.011	0.018	H	1.0		
	E → Y	(HL)	0.479	0.926	1.614	0.005	0.008	0.013				
		(LH)	0.262	0.459	0.749	0.006	0.011	0.018				
	F → Y	(HL)	0.490	0.956	1.680	0.005	0.008	0.013				
		(LH)	0.287	0.501	0.820	0.006	0.011	0.018				
	G → Y	(HH)	0.367	0.663	1.086	0.006	0.011	0.018				
		(LL)	0.569	1.125	1.983	0.005	0.008	0.013				
	H → Y	(HH)	0.382	0.689	1.128	0.006	0.011	0.018				
		(LL)	0.580	1.144	2.015	0.005	0.008	0.013				
F308N3	A → Y	(HL)	0.398	0.740	1.251	0.009	0.015	0.024	A	1.0	Y	23
		(LH)	0.219	0.388	0.632	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.407	0.766	1.318	0.009	0.015	0.024	C	1.0		
		(LH)	0.240	0.425	0.693	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.411	0.812	1.409	0.009	0.015	0.024	E	1.0		
		(LH)	0.266	0.475	0.770	0.012	0.023	0.037	F	1.0		
	D → Y	(HL)	0.409	0.813	1.428	0.009	0.015	0.024	G	1.0		
		(LH)	0.274	0.491	0.802	0.012	0.023	0.037	H	1.0		
	E → Y	(HL)	0.382	0.718	1.220	0.009	0.015	0.024				
		(LH)	0.221	0.389	0.634	0.012	0.023	0.037				
	F → Y	(HH)	0.296	0.535	0.877	0.012	0.023	0.037				
		(LL)	0.446	0.864	1.512	0.009	0.015	0.024				
	G → Y	(HH)	0.325	0.590	0.967	0.012	0.023	0.036				
		(LL)	0.476	0.927	1.613	0.009	0.015	0.024				
	H → Y	(HH)	0.335	0.611	1.002	0.012	0.023	0.036				
		(LL)	0.483	0.940	1.633	0.009	0.015	0.024				

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F328N3	A → Y	(HL)	0.487	0.936	1.617	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.257	0.451	0.737	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.497	0.962	1.682	0.005	0.008	0.013	C	1.0		
		(LH)	0.280	0.489	0.800	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.500	1.009	1.776	0.005	0.008	0.013	E	1.0		
		(LH)	0.309	0.543	0.881	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.498	1.011	1.793	0.005	0.008	0.013	G	1.0		
		(LH)	0.316	0.561	0.912	0.006	0.011	0.018	H	1.0		
	E → Y	(HL)	0.480	0.930	1.619	0.005	0.008	0.013				
		(LH)	0.263	0.461	0.752	0.006	0.011	0.018				
	F → Y	(HH)	0.338	0.607	0.999	0.006	0.011	0.018				
		(LL)	0.544	1.077	1.898	0.005	0.008	0.013				
	G → Y	(HH)	0.368	0.664	1.089	0.006	0.011	0.018				
		(LL)	0.576	1.140	2.000	0.005	0.008	0.013				
	H → Y	(HH)	0.386	0.694	1.136	0.006	0.011	0.018				
		(LL)	0.586	1.156	2.033	0.005	0.008	0.013				
F308N4	A → Y	(HL)	0.398	0.740	1.251	0.009	0.015	0.024	A	1.0	Y	23
		(LH)	0.219	0.388	0.632	0.013	0.023	0.037	B	1.0		
	B → Y	(HL)	0.407	0.766	1.318	0.009	0.015	0.024	C	1.0		
		(LH)	0.240	0.425	0.693	0.012	0.023	0.037	D	1.0		
	C → Y	(HL)	0.411	0.812	1.409	0.009	0.015	0.024	E	1.0		
		(LH)	0.266	0.475	0.770	0.012	0.023	0.037	F	1.0		
	D → Y	(HL)	0.409	0.813	1.428	0.009	0.015	0.024	G	1.0		
		(LH)	0.274	0.491	0.802	0.012	0.023	0.037	H	1.0		
	E → Y	(HH)	0.277	0.497	0.815	0.012	0.023	0.037				
		(LL)	0.429	0.831	1.440	0.009	0.015	0.024				
	F → Y	(HH)	0.299	0.538	0.884	0.012	0.023	0.037				
		(LL)	0.452	0.876	1.527	0.009	0.015	0.024				
	G → Y	(HH)	0.324	0.591	0.967	0.012	0.023	0.037				
		(LL)	0.478	0.931	1.615	0.009	0.015	0.024				
	H → Y	(HH)	0.334	0.610	1.002	0.012	0.023	0.037				
		(LL)	0.483	0.943	1.644	0.009	0.015	0.024				
F328N4	A → Y	(HL)	0.487	0.936	1.617	0.005	0.008	0.013	A	1.0	Y	45
		(LH)	0.257	0.451	0.737	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.497	0.962	1.682	0.005	0.008	0.013	C	1.0		
		(LH)	0.280	0.489	0.800	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.500	1.009	1.776	0.005	0.008	0.013	E	1.0		
		(LH)	0.309	0.543	0.881	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.498	1.011	1.793	0.005	0.008	0.013	G	1.0		
		(LH)	0.316	0.561	0.912	0.006	0.011	0.018	H	1.0		
	E → Y	(HH)	0.323	0.574	0.943	0.006	0.011	0.018				
		(LL)	0.533	1.050	1.849	0.005	0.008	0.013				
	F → Y	(HH)	0.338	0.606	0.999	0.006	0.011	0.018				
		(LL)	0.547	1.080	1.905	0.005	0.008	0.013				
	G → Y	(HH)	0.370	0.666	1.093	0.006	0.011	0.018				
		(LL)	0.579	1.148	2.016	0.005	0.008	0.013				
	H → Y	(HH)	0.384	0.695	1.136	0.006	0.011	0.018				
		(LL)	0.587	1.158	2.037	0.005	0.008	0.013				

FUNCTION BLOCK

Function	2-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L312	2										
x1	F312	2										
x2	F332	3										
x4	F352	6										
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"

Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L312	A → Y	(HH)	0.165	0.279	0.426	0.025	0.045	0.072	A	1.0	Y	11
		(LL)	0.144	0.244	0.392	0.017	0.028	0.045	B	1.0		
	B → Y	(HH)	0.156	0.267	0.435	0.025	0.045	0.072				
		(LL)	0.169	0.282	0.450	0.017	0.028	0.046				
F312	A → Y	(HH)	0.196	0.331	0.509	0.013	0.023	0.037	A	1.0	Y	22
		(LL)	0.175	0.301	0.493	0.010	0.016	0.026	B	1.0		
	B → Y	(HH)	0.184	0.317	0.517	0.013	0.023	0.037				
		(LL)	0.196	0.339	0.553	0.010	0.016	0.026				
F332	A → Y	(HH)	0.250	0.417	0.666	0.006	0.012	0.019	A	1.0	Y	44
		(LL)	0.225	0.399	0.671	0.005	0.008	0.013	B	1.0		
	B → Y	(HH)	0.229	0.401	0.671	0.006	0.012	0.019				
		(LL)	0.241	0.429	0.725	0.005	0.008	0.014				
F352	A → Y	(HH)	0.229	0.384	0.625	0.003	0.006	0.009	A	2.0	Y	89
		(LL)	0.218	0.387	0.646	0.002	0.004	0.007	B	2.0		
	B → Y	(HH)	0.227	0.383	0.624	0.003	0.006	0.009				
		(LL)	0.217	0.386	0.645	0.002	0.004	0.006				

FUNCTION BLOCK

Function	3-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L313	2										
x1	F313	3										
x2	F333	4										
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"

Logic Diagram for "with 1 inverter type"

Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

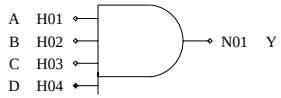
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L313	A → Y	(HH)	0.221	0.368	0.574	0.025	0.046	0.074	A	1.0	Y	10
		(LL)	0.155	0.270	0.438	0.018	0.028	0.046	B	1.0		
	B → Y	(HH)	0.220	0.377	0.611	0.025	0.046	0.074	C	1.0		
		(LL)	0.175	0.305	0.493	0.018	0.028	0.046				
	C → Y	(HH)	0.215	0.397	0.669	0.025	0.046	0.073				
		(LL)	0.205	0.360	0.580	0.018	0.028	0.046				
F313	A → Y	(HH)	0.269	0.444	0.703	0.013	0.024	0.037	A	1.0	Y	21
		(LL)	0.187	0.326	0.538	0.010	0.016	0.026	B	1.0		
	B → Y	(HH)	0.267	0.458	0.742	0.013	0.024	0.038	C	1.0		
		(LL)	0.206	0.364	0.598	0.010	0.016	0.026				
	C → Y	(HH)	0.258	0.476	0.791	0.013	0.024	0.038				
		(LL)	0.231	0.410	0.672	0.010	0.016	0.026				
F333	A → Y	(HH)	0.351	0.587	0.953	0.007	0.012	0.020	A	1.0	Y	44
		(LL)	0.237	0.426	0.722	0.005	0.008	0.014	B	1.0		
	B → Y	(HH)	0.347	0.601	0.995	0.007	0.013	0.020	C	1.0		
		(LL)	0.252	0.460	0.778	0.005	0.009	0.014				
	C → Y	(HH)	0.341	0.625	1.053	0.007	0.013	0.020				
		(LL)	0.279	0.510	0.862	0.005	0.009	0.014				

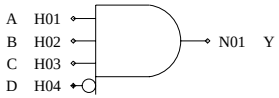
FUNCTION BLOCK

Function	4-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L314	3	L314N1	3								
x1	F314	3	F314N1	4								
x2	F334	4	F334N1	5								
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

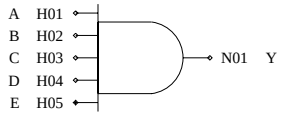
FUNCTION BLOCK

Block type	Switching speed Path IN → OUT		t LD0 (ns) MIN.	t LD0 (ns) TYP.	t LD0 (ns) MAX.	t 1 MIN.	t 1 TYP.	t 1 MAX.	Input Symbol	Input Fanin	Output Symbol	Output Fanout
L314	A → Y	(HH)	0.258	0.433	0.675	0.025	0.046	0.074	A	1.0	Y	10
		(LL)	0.159	0.280	0.455	0.017	0.027	0.044	B	1.0		
	B → Y	(HH)	0.265	0.457	0.747	0.025	0.046	0.073	C	1.0		
		(LL)	0.180	0.316	0.515	0.017	0.027	0.044	D	1.0		
	C → Y	(HH)	0.274	0.509	0.846	0.025	0.046	0.074				
		(LL)	0.208	0.366	0.600	0.017	0.027	0.044				
	D → Y	(HH)	0.271	0.506	0.859	0.025	0.046	0.074				
		(LL)	0.220	0.389	0.633	0.017	0.027	0.045				
F314	A → Y	(HH)	0.302	0.510	0.816	0.013	0.024	0.038	A	1.0	Y	21
		(LL)	0.190	0.331	0.545	0.010	0.016	0.026	B	1.0		
	B → Y	(HH)	0.307	0.536	0.882	0.013	0.024	0.038	C	1.0		
		(LL)	0.207	0.368	0.605	0.010	0.016	0.026	D	1.0		
	C → Y	(HH)	0.312	0.587	0.979	0.013	0.024	0.038				
		(LL)	0.234	0.420	0.688	0.010	0.016	0.026				
	D → Y	(HH)	0.310	0.589	0.993	0.013	0.024	0.038				
		(LL)	0.244	0.438	0.717	0.010	0.016	0.026				
F334	A → Y	(HH)	0.395	0.680	1.122	0.007	0.013	0.021	A	1.0	Y	43
		(LL)	0.238	0.429	0.725	0.005	0.008	0.014	B	1.0		
	B → Y	(HH)	0.397	0.710	1.191	0.007	0.013	0.021	C	1.0		
		(LL)	0.254	0.464	0.787	0.005	0.009	0.014	D	1.0		
	C → Y	(HH)	0.408	0.765	1.295	0.007	0.013	0.021				
		(LL)	0.280	0.516	0.872	0.005	0.009	0.014				
	D → Y	(HH)	0.405	0.768	1.309	0.007	0.013	0.021				
		(LL)	0.291	0.538	0.910	0.005	0.009	0.014				
L314N1	A → Y	(HH)	0.250	0.422	0.660	0.025	0.046	0.074	A	1.0	Y	10
		(LL)	0.154	0.272	0.437	0.017	0.027	0.044	B	1.0		
	B → Y	(HH)	0.259	0.450	0.724	0.025	0.046	0.074	C	1.0		
		(LL)	0.178	0.313	0.505	0.017	0.027	0.044	D	1.0		
	C → Y	(HH)	0.264	0.496	0.816	0.025	0.046	0.074				
		(LL)	0.205	0.363	0.582	0.017	0.027	0.044				
	D → Y	(HL)	0.260	0.484	0.794	0.017	0.027	0.045				
		(LH)	0.341	0.626	1.037	0.025	0.046	0.074				
F314N1	A → Y	(HH)	0.282	0.472	0.752	0.013	0.024	0.038	A	1.0	Y	21
		(LL)	0.172	0.304	0.493	0.009	0.015	0.024	B	1.0		
	B → Y	(HH)	0.287	0.500	0.817	0.013	0.024	0.038	C	1.0		
		(LL)	0.193	0.341	0.565	0.009	0.015	0.024	D	1.0		
	C → Y	(HH)	0.293	0.549	0.914	0.013	0.024	0.038				
		(LL)	0.219	0.394	0.644	0.009	0.015	0.024				
	D → Y	(HL)	0.278	0.518	0.857	0.009	0.015	0.024				
		(LH)	0.371	0.680	1.140	0.013	0.024	0.038				
F334N1	A → Y	(HH)	0.378	0.647	1.061	0.006	0.012	0.019	A	1.0	Y	42
		(LL)	0.227	0.412	0.689	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.380	0.678	1.130	0.006	0.012	0.019	C	1.0		
		(LL)	0.243	0.446	0.752	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.385	0.724	1.222	0.006	0.012	0.019				
		(LL)	0.268	0.493	0.832	0.005	0.008	0.012				
	D → Y	(HL)	0.323	0.614	1.042	0.005	0.008	0.012				
		(LH)	0.463	0.854	1.444	0.006	0.012	0.019				

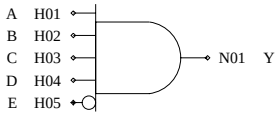
FUNCTION BLOCK

Function	5-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L315	4	L315N1	4								
x1	F315	5	F315N1	5								
x2	F335	7	F335N1	7								
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"

Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L315	A → Y	(HH)	0.167	0.319	0.523	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.163	0.277	0.443	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.175	0.327	0.517	0.044	0.088	0.147	C	1.0		
		(LL)	0.142	0.243	0.386	0.016	0.026	0.043	D	1.0		
	C → Y	(HH)	0.253	0.475	0.788	0.044	0.088	0.147	E	1.0		
		(LL)	0.214	0.382	0.619	0.017	0.027	0.045				
	D → Y	(HH)	0.260	0.474	0.772	0.044	0.088	0.147				
		(LL)	0.201	0.355	0.574	0.017	0.027	0.044				
	E → Y	(HH)	0.263	0.445	0.696	0.044	0.088	0.147				
		(LL)	0.167	0.296	0.479	0.017	0.027	0.044				
F315	A → Y	(HH)	0.206	0.383	0.628	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.199	0.345	0.563	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.220	0.395	0.625	0.022	0.044	0.074	C	1.0		
		(LL)	0.180	0.309	0.505	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.283	0.539	0.902	0.022	0.045	0.074	E	1.0		
		(LL)	0.239	0.426	0.698	0.009	0.014	0.023				
	D → Y	(HH)	0.290	0.520	0.851	0.022	0.045	0.074				
		(LL)	0.214	0.378	0.623	0.009	0.014	0.023				
	E → Y	(HH)	0.292	0.506	0.811	0.022	0.045	0.074				
		(LL)	0.195	0.342	0.564	0.009	0.014	0.023				
F335	A → Y	(HH)	0.364	0.694	1.190	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.287	0.512	0.857	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.354	0.686	1.195	0.006	0.011	0.018	C	1.0		
		(LL)	0.306	0.548	0.912	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.436	0.811	1.380	0.006	0.011	0.018	E	1.0		
		(LL)	0.307	0.556	0.931	0.005	0.007	0.012				
	D → Y	(HH)	0.438	0.825	1.421	0.006	0.011	0.018				
		(LL)	0.330	0.597	1.000	0.005	0.007	0.012				
	E → Y	(HH)	0.431	0.845	1.473	0.006	0.011	0.018				
		(LL)	0.353	0.645	1.075	0.005	0.007	0.012				
L315N1	A → Y	(HH)	0.167	0.319	0.523	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.163	0.277	0.443	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.175	0.327	0.517	0.044	0.088	0.147	C	1.0		
		(LL)	0.142	0.243	0.386	0.016	0.026	0.043	D	1.0		
	C → Y	(HH)	0.261	0.488	0.805	0.044	0.088	0.147	E	1.0		
		(LL)	0.212	0.380	0.616	0.017	0.027	0.045				
	D → Y	(HH)	0.268	0.465	0.755	0.044	0.088	0.147				
		(LL)	0.188	0.329	0.540	0.017	0.027	0.044				
	E → Y	(HL)	0.220	0.400	0.656	0.017	0.027	0.044				
		(LH)	0.316	0.567	0.927	0.044	0.088	0.147				
F315N1	A → Y	(HH)	0.193	0.356	0.586	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.192	0.334	0.546	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.205	0.369	0.580	0.022	0.044	0.074	C	1.0		
		(LL)	0.173	0.299	0.487	0.008	0.014	0.023	D	1.0		
	C → Y	(HH)	0.299	0.563	0.940	0.022	0.044	0.074	E	1.0		
		(LL)	0.246	0.442	0.737	0.009	0.014	0.023				
	D → Y	(HH)	0.308	0.541	0.888	0.022	0.044	0.074				
		(LL)	0.220	0.396	0.659	0.009	0.014	0.023				
	E → Y	(HL)	0.253	0.468	0.778	0.009	0.014	0.023				
		(LH)	0.355	0.643	1.063	0.022	0.044	0.074				
F335N1	A → Y	(HH)	0.364	0.694	1.190	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.287	0.512	0.857	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.354	0.686	1.195	0.006	0.011	0.018	C	1.0		
		(LL)	0.306	0.548	0.912	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.440	0.814	1.384	0.006	0.011	0.018	E	1.0		
		(LL)	0.307	0.557	0.931	0.005	0.007	0.012				

FUNCTION BLOCK

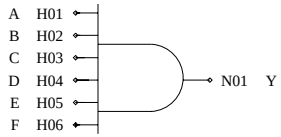
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D → Y	(HH)	0.442	0.828	1.429	0.006	0.011	0.018				
		(LL)	0.330	0.597	1.000	0.005	0.007	0.012				
	E → Y	(HL)	0.397	0.742	1.252	0.005	0.007	0.012				
		(LH)	0.510	0.976	1.685	0.006	0.011	0.018				

[MEMO]

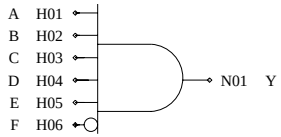
FUNCTION BLOCK

Function	6-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L316	4	L316N1	5	L316N2	5						
x1	F316	6	F316N1	6	F316N2	6						
x2	F336	7	F336N1	8	F336N2	8						
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

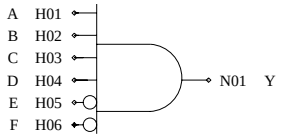
Logic Diagram for "Normal type"



Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"

Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L316	A → Y	(HH)	0.246	0.419	0.655	0.044	0.088	0.147		A	1.0	Y	5
		(LL)	0.157	0.275	0.440	0.016	0.027	0.044		B	1.0		
	B → Y	(HH)	0.249	0.432	0.693	0.044	0.088	0.147		C	1.0		
		(LL)	0.179	0.312	0.505	0.017	0.027	0.044		D	1.0		
	C → Y	(HH)	0.240	0.449	0.741	0.044	0.088	0.147		E	1.0		
		(LL)	0.203	0.359	0.578	0.017	0.027	0.044		F	1.0		
	D → Y	(HH)	0.235	0.411	0.647	0.044	0.088	0.147					
		(LL)	0.156	0.274	0.443	0.016	0.026	0.044					
	E → Y	(HH)	0.238	0.425	0.688	0.044	0.088	0.147					
		(LL)	0.181	0.313	0.507	0.016	0.026	0.044					
	F → Y	(HH)	0.231	0.445	0.740	0.044	0.088	0.147					
		(LL)	0.206	0.360	0.581	0.017	0.027	0.044					
F316	A → Y	(HH)	0.295	0.510	0.813	0.022	0.044	0.074		A	1.0	Y	10
		(LL)	0.192	0.338	0.560	0.009	0.014	0.023		B	1.0		
	B → Y	(HH)	0.294	0.524	0.853	0.022	0.044	0.074		C	1.0		
		(LL)	0.214	0.378	0.624	0.009	0.014	0.023		D	1.0		
	C → Y	(HH)	0.285	0.543	0.906	0.022	0.044	0.074		E	1.0		
		(LL)	0.238	0.427	0.699	0.009	0.014	0.023		F	1.0		
	D → Y	(HH)	0.303	0.522	0.836	0.022	0.044	0.074					
		(LL)	0.201	0.353	0.584	0.009	0.014	0.023					
	E → Y	(HH)	0.300	0.535	0.876	0.022	0.044	0.074					
		(LL)	0.217	0.386	0.640	0.009	0.014	0.023					
	F → Y	(HH)	0.294	0.558	0.932	0.022	0.044	0.074					
		(LL)	0.244	0.436	0.722	0.009	0.014	0.023					
F336	A → Y	(HH)	0.434	0.801	1.351	0.006	0.011	0.018		A	1.0	Y	45
		(LL)	0.299	0.543	0.906	0.005	0.007	0.012		B	1.0		
	B → Y	(HH)	0.437	0.814	1.392	0.006	0.011	0.018		C	1.0		
		(LL)	0.321	0.579	0.968	0.005	0.007	0.012		D	1.0		
	C → Y	(HH)	0.428	0.830	1.439	0.006	0.011	0.018		E	1.0		
		(LL)	0.344	0.622	1.040	0.005	0.007	0.012		F	1.0		
	D → Y	(HH)	0.441	0.818	1.390	0.006	0.011	0.018					
		(LL)	0.307	0.558	0.938	0.005	0.007	0.012					
	E → Y	(HH)	0.442	0.832	1.431	0.006	0.011	0.018					
		(LL)	0.331	0.597	1.002	0.005	0.007	0.012					
	F → Y	(HH)	0.435	0.851	1.484	0.006	0.011	0.018					
		(LL)	0.355	0.643	1.076	0.005	0.007	0.012					
L316N1	A → Y	(HH)	0.246	0.419	0.655	0.044	0.088	0.147		A	1.0	Y	5
		(LL)	0.157	0.275	0.440	0.016	0.027	0.044		B	1.0		
	B → Y	(HH)	0.249	0.432	0.693	0.044	0.088	0.147		C	1.0		
		(LL)	0.178	0.312	0.505	0.017	0.027	0.044		D	1.0		
	C → Y	(HH)	0.240	0.449	0.741	0.044	0.088	0.147		E	1.0		
		(LL)	0.203	0.359	0.578	0.017	0.027	0.044		F	1.0		
	D → Y	(HH)	0.235	0.411	0.647	0.044	0.088	0.147					
		(LL)	0.156	0.274	0.443	0.016	0.026	0.044					
	E → Y	(HH)	0.238	0.425	0.687	0.044	0.088	0.147					
		(LL)	0.181	0.313	0.507	0.016	0.026	0.044					
	F → Y	(HL)	0.264	0.479	0.779	0.017	0.027	0.044					
		(LH)	0.320	0.586	0.978	0.044	0.088	0.147					
F316N1	A → Y	(HH)	0.288	0.486	0.769	0.023	0.046	0.076		A	1.0	Y	10
		(LL)	0.183	0.325	0.532	0.009	0.015	0.024		B	1.0		
	B → Y	(HH)	0.287	0.499	0.810	0.023	0.046	0.076		C	1.0		
		(LL)	0.204	0.361	0.599	0.009	0.015	0.024		D	1.0		
	C → Y	(HH)	0.276	0.516	0.858	0.023	0.046	0.076		E	1.0		
		(LL)	0.225	0.406	0.667	0.009	0.015	0.024		F	1.0		
	D → Y	(HH)	0.296	0.523	0.841	0.023	0.046	0.076					
		(LL)	0.196	0.349	0.575	0.008	0.013	0.022					

FUNCTION BLOCK

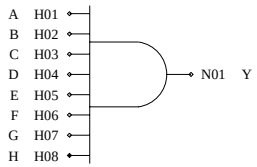
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	E → Y	(HH)	0.294	0.536	0.886	0.023	0.046	0.076				
		(LL)	0.217	0.387	0.642	0.008	0.014	0.022				
	F → Y	(HL)	0.297	0.549	0.909	0.008	0.014	0.023				
		(LH)	0.368	0.693	1.165	0.023	0.046	0.076				
F336N1	A → Y	(HH)	0.434	0.801	1.351	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.299	0.543	0.906	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.437	0.814	1.392	0.006	0.011	0.018	C	1.0		
		(LL)	0.321	0.579	0.968	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.428	0.830	1.439	0.006	0.011	0.018	E	1.0		
		(LL)	0.344	0.622	1.040	0.005	0.007	0.012	F	1.0		
	D → Y	(HH)	0.441	0.818	1.390	0.006	0.011	0.018				
		(LL)	0.307	0.557	0.938	0.005	0.007	0.012				
	E → Y	(HH)	0.442	0.831	1.431	0.006	0.011	0.018				
		(LL)	0.330	0.596	1.003	0.005	0.007	0.012				
	F → Y	(HL)	0.411	0.757	1.265	0.005	0.007	0.012				
		(LH)	0.519	0.986	1.703	0.006	0.011	0.018				
L316N2	A → Y	(HH)	0.246	0.419	0.655	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.157	0.275	0.440	0.016	0.027	0.044	B	1.0		
	B → Y	(HH)	0.249	0.432	0.693	0.044	0.088	0.147	C	1.0		
		(LL)	0.178	0.312	0.505	0.017	0.027	0.044	D	1.0		
	C → Y	(HH)	0.240	0.449	0.741	0.044	0.088	0.147	E	1.0		
		(LL)	0.203	0.359	0.578	0.017	0.027	0.044	F	1.0		
	D → Y	(HH)	0.235	0.411	0.645	0.044	0.088	0.147				
		(LL)	0.156	0.274	0.443	0.016	0.026	0.044				
	E → Y	(HL)	0.238	0.428	0.696	0.016	0.026	0.044				
		(LH)	0.303	0.554	0.917	0.044	0.088	0.147				
	F → Y	(HL)	0.263	0.475	0.774	0.017	0.027	0.044				
		(LH)	0.319	0.586	0.977	0.044	0.088	0.147				
F316N2	A → Y	(HH)	0.288	0.485	0.769	0.023	0.046	0.076	A	1.0	Y	10
		(LL)	0.183	0.325	0.532	0.009	0.015	0.024	B	1.0		
	B → Y	(HH)	0.287	0.498	0.810	0.023	0.046	0.076	C	1.0		
		(LL)	0.204	0.361	0.599	0.009	0.015	0.024	D	1.0		
	C → Y	(HH)	0.276	0.516	0.858	0.023	0.046	0.076	E	1.0		
		(LL)	0.225	0.406	0.667	0.009	0.015	0.024	F	1.0		
	D → Y	(HH)	0.298	0.524	0.843	0.023	0.046	0.076				
		(LL)	0.197	0.350	0.578	0.008	0.013	0.022				
	E → Y	(HL)	0.274	0.502	0.832	0.008	0.014	0.022				
		(LH)	0.356	0.665	1.113	0.023	0.046	0.076				
	F → Y	(HL)	0.292	0.543	0.901	0.008	0.014	0.023				
		(LH)	0.367	0.690	1.158	0.023	0.046	0.076				
F336N2	A → Y	(HH)	0.434	0.801	1.351	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.299	0.543	0.906	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.437	0.814	1.392	0.006	0.011	0.018	C	1.0		
		(LL)	0.321	0.579	0.968	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.428	0.830	1.439	0.006	0.011	0.018	E	1.0		
		(LL)	0.344	0.622	1.040	0.005	0.007	0.012	F	1.0		
	D → Y	(HH)	0.441	0.819	1.390	0.006	0.011	0.018				
		(LL)	0.307	0.558	0.940	0.005	0.007	0.012				
	E → Y	(HL)	0.383	0.706	1.184	0.005	0.007	0.012				
		(LH)	0.501	0.953	1.645	0.006	0.011	0.018				
	F → Y	(HL)	0.408	0.755	1.267	0.005	0.007	0.012				
		(LH)	0.520	0.990	1.710	0.006	0.011	0.018				

[MEMO]

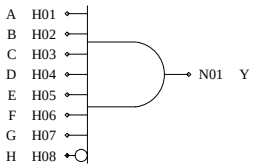
FUNCTION BLOCK

Function	8-INPUT AND										SSI Family	
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L318	5	L318N1	6	L318N2	6	L318N3	7				
x1	F318	6	F318N1	7	F318N2	7	F318N3	8				
x2	F338	8	F338N1	9	F338N2	9	F338N3	10				
x4												
x8												
Block type	Normal		with 1 inverter		with 2 inverter		with 3 inverter		with 4 inverter			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power												
x1												
x2												
x4												
x8												

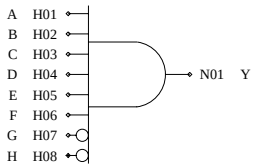
Logic Diagram for "Normal type"



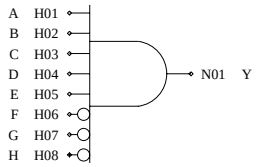
Logic Diagram for "with 1 inverter type"



Logic Diagram for "with 2 inverter type"



Logic Diagram for "with 3 inverter type"



Logic Diagram for "with 4 inverter type"

FUNCTION BLOCK

Block type	Switching speed Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L318	A → Y	(HH)	0.252	0.444	0.702	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.159	0.281	0.451	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.261	0.471	0.772	0.044	0.088	0.147	C	1.0		
		(LL)	0.182	0.317	0.512	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.265	0.516	0.859	0.044	0.088	0.147	E	1.0		
		(LL)	0.209	0.367	0.590	0.017	0.027	0.044	F	1.0		
	D → Y	(HH)	0.264	0.519	0.880	0.044	0.088	0.147	G	1.0		
		(LL)	0.217	0.385	0.623	0.017	0.027	0.044	H	1.0		
	E → Y	(HH)	0.261	0.449	0.707	0.044	0.088	0.148				
		(LL)	0.151	0.269	0.428	0.017	0.028	0.046				
	F → Y	(HH)	0.270	0.477	0.770	0.044	0.088	0.148				
		(LL)	0.175	0.305	0.496	0.018	0.028	0.046				
	G → Y	(HH)	0.276	0.525	0.864	0.044	0.088	0.148				
		(LL)	0.203	0.359	0.572	0.018	0.028	0.046				
	H → Y	(HH)	0.274	0.528	0.880	0.044	0.088	0.148				
		(LL)	0.210	0.374	0.601	0.018	0.028	0.046				
F318	A → Y	(HH)	0.306	0.531	0.854	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074	C	1.0		
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074	E	1.0		
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023	F	1.0		
	D → Y	(HH)	0.314	0.607	1.028	0.022	0.044	0.074	G	1.0		
		(LL)	0.240	0.432	0.716	0.009	0.014	0.023	H	1.0		
	E → Y	(HH)	0.306	0.531	0.854	0.022	0.044	0.074				
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023				
	F → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074				
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023				
	G → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074				
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023				
	H → Y	(HH)	0.314	0.607	1.029	0.022	0.044	0.074				
		(LL)	0.240	0.435	0.716	0.009	0.014	0.023				
F338	A → Y	(HH)	0.467	0.861	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.301	0.550	0.926	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.476	0.888	1.524	0.006	0.011	0.018	C	1.0		
		(LL)	0.323	0.588	0.987	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.479	0.933	1.615	0.006	0.011	0.018	E	1.0		
		(LL)	0.348	0.636	1.066	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.477	0.936	1.633	0.006	0.011	0.018	G	1.0		
		(LL)	0.357	0.653	1.094	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.449	0.837	1.427	0.006	0.011	0.018				
		(LL)	0.304	0.554	0.929	0.004	0.007	0.011				
	F → Y	(HH)	0.458	0.866	1.495	0.006	0.011	0.018				
		(LL)	0.325	0.591	0.991	0.004	0.007	0.011				
	G → Y	(HH)	0.462	0.912	1.585	0.006	0.011	0.018				
		(LL)	0.353	0.641	1.069	0.004	0.007	0.011				
	H → Y	(HH)	0.460	0.915	1.605	0.006	0.011	0.018				
		(LL)	0.361	0.657	1.099	0.004	0.007	0.011				
L318N1	A → Y	(HH)	0.252	0.444	0.702	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.159	0.281	0.451	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.261	0.471	0.772	0.044	0.088	0.147	C	1.0		
		(LL)	0.182	0.317	0.512	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.265	0.516	0.859	0.044	0.088	0.147	E	1.0		
		(LL)	0.209	0.367	0.590	0.017	0.027	0.044	F	1.0		
	D → Y	(HH)	0.264	0.519	0.880	0.044	0.088	0.147	G	1.0		
		(LL)	0.217	0.385	0.623	0.017	0.027	0.044	H	1.0		

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
	E → Y	(HH)	0.261	0.449	0.707	0.044	0.088	0.148				
		(LL)	0.151	0.268	0.431	0.018	0.028	0.045				
	F → Y	(HH)	0.270	0.477	0.770	0.044	0.088	0.148				
		(LL)	0.175	0.305	0.496	0.018	0.028	0.046				
	G → Y	(HH)	0.276	0.525	0.864	0.044	0.088	0.148				
		(LL)	0.203	0.358	0.572	0.018	0.028	0.046				
	H → Y	(HL)	0.262	0.484	0.788	0.018	0.028	0.046				
		(LH)	0.355	0.656	1.092	0.044	0.088	0.148				
F318N1	A → Y	(HH)	0.306	0.531	0.854	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074	C	1.0		
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074	E	1.0		
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023	F	1.0		
	D → Y	(HH)	0.314	0.607	1.028	0.022	0.044	0.074	G	1.0		
		(LL)	0.240	0.432	0.716	0.009	0.014	0.023	H	1.0		
	E → Y	(HH)	0.307	0.531	0.854	0.022	0.044	0.074				
		(LL)	0.188	0.332	0.544	0.009	0.014	0.023				
	F → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074				
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023				
	G → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074				
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023				
	H → Y	(HL)	0.286	0.537	0.895	0.009	0.014	0.023				
		(LH)	0.393	0.735	1.235	0.022	0.044	0.074				
F338N1	A → Y	(HH)	0.467	0.861	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.301	0.550	0.926	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.476	0.888	1.524	0.006	0.011	0.018	C	1.0		
		(LL)	0.323	0.588	0.987	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.479	0.933	1.615	0.006	0.011	0.018	E	1.0		
		(LL)	0.348	0.636	1.066	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.477	0.936	1.633	0.006	0.011	0.018	G	1.0		
		(LL)	0.357	0.652	1.091	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.449	0.837	1.427	0.006	0.011	0.018				
		(LL)	0.303	0.554	0.929	0.004	0.007	0.011				
	F → Y	(HH)	0.458	0.865	1.499	0.006	0.011	0.018				
		(LL)	0.326	0.591	0.992	0.004	0.007	0.011				
	G → Y	(HH)	0.462	0.911	1.583	0.006	0.011	0.018				
		(LL)	0.353	0.641	1.069	0.004	0.007	0.011				
	H → Y	(HL)	0.407	0.760	1.275	0.004	0.007	0.011				
		(LH)	0.540	1.041	1.808	0.006	0.011	0.018				
L318N2	A → Y	(HH)	0.253	0.444	0.702	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.159	0.281	0.451	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.261	0.471	0.772	0.044	0.088	0.147	C	1.0		
		(LL)	0.182	0.317	0.512	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.265	0.517	0.860	0.044	0.088	0.147	E	1.0		
		(LL)	0.209	0.367	0.590	0.017	0.027	0.044	F	1.0		
	D → Y	(HH)	0.264	0.519	0.880	0.044	0.088	0.147	G	1.0		
		(LL)	0.217	0.385	0.623	0.017	0.027	0.044	H	1.0		
	E → Y	(HH)	0.264	0.452	0.709	0.044	0.088	0.148				
		(LL)	0.152	0.268	0.431	0.017	0.028	0.045				
	F → Y	(HH)	0.274	0.481	0.775	0.044	0.088	0.148				
		(LL)	0.175	0.306	0.496	0.018	0.028	0.046				
	G → Y	(HL)	0.254	0.465	0.757	0.018	0.028	0.046				
		(LH)	0.354	0.652	1.079	0.044	0.088	0.148				
	H → Y	(HL)	0.267	0.489	0.795	0.018	0.028	0.046				
		(LH)	0.365	0.671	1.111	0.044	0.088	0.148				

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F318N2	A → Y	(HH)	0.306	0.531	0.854	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074	C	1.0		
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074	E	1.0		
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023	F	1.0		
	D → Y	(HH)	0.314	0.607	1.028	0.022	0.044	0.074	G	1.0		
		(LL)	0.240	0.432	0.716	0.009	0.014	0.023	H	1.0		
	E → Y	(HH)	0.306	0.531	0.853	0.022	0.044	0.074				
		(LL)	0.187	0.332	0.543	0.009	0.014	0.023				
	F → Y	(HH)	0.313	0.559	0.920	0.022	0.044	0.074				
		(LL)	0.207	0.368	0.608	0.009	0.014	0.023				
	G → Y	(HL)	0.285	0.526	0.870	0.009	0.014	0.023				
		(LH)	0.390	0.726	1.222	0.022	0.044	0.074				
	H → Y	(HL)	0.294	0.546	0.905	0.009	0.014	0.023				
		(LH)	0.400	0.746	1.252	0.022	0.044	0.074				
F338N2	A → Y	(HH)	0.467	0.861	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.301	0.550	0.926	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.476	0.888	1.524	0.006	0.011	0.018	C	1.0		
		(LL)	0.323	0.588	0.987	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.479	0.933	1.615	0.006	0.011	0.018	E	1.0		
		(LL)	0.348	0.636	1.066	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.477	0.936	1.633	0.006	0.011	0.018	G	1.0		
		(LL)	0.357	0.652	1.091	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.449	0.838	1.428	0.006	0.011	0.018				
		(LL)	0.303	0.554	0.929	0.004	0.007	0.011				
	F → Y	(HH)	0.458	0.865	1.498	0.006	0.011	0.018				
		(LL)	0.326	0.591	0.991	0.004	0.007	0.011				
	G → Y	(HL)	0.404	0.749	1.253	0.004	0.007	0.011				
		(LH)	0.536	1.032	1.792	0.006	0.011	0.018				
	H → Y	(HL)	0.414	0.767	1.288	0.004	0.007	0.011				
		(LH)	0.547	1.053	1.825	0.006	0.011	0.018				
L318N3	A → Y	(HH)	0.253	0.444	0.702	0.044	0.088	0.147	A	1.0	Y	5
		(LL)	0.159	0.281	0.451	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.261	0.471	0.772	0.044	0.088	0.147	C	1.0		
		(LL)	0.182	0.317	0.512	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.265	0.517	0.860	0.044	0.088	0.147	E	1.0		
		(LL)	0.209	0.367	0.590	0.017	0.027	0.044	F	1.0		
	D → Y	(HH)	0.264	0.519	0.880	0.044	0.088	0.147	G	1.0		
		(LL)	0.217	0.385	0.623	0.017	0.027	0.044	H	1.0		
	E → Y	(HH)	0.264	0.452	0.708	0.044	0.088	0.148				
		(LL)	0.153	0.268	0.428	0.017	0.028	0.046				
	F → Y	(HL)	0.228	0.415	0.673	0.018	0.028	0.046				
		(LH)	0.329	0.599	0.986	0.044	0.088	0.148				
	G → Y	(HL)	0.257	0.467	0.760	0.018	0.028	0.046				
		(LH)	0.360	0.663	1.093	0.044	0.088	0.148				
	H → Y	(HL)	0.270	0.494	0.799	0.018	0.028	0.046				
		(LH)	0.369	0.680	1.126	0.044	0.088	0.148				
F318N3	A → Y	(HH)	0.306	0.531	0.854	0.022	0.044	0.074	A	1.0	Y	10
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.313	0.559	0.922	0.022	0.044	0.074	C	1.0		
		(LL)	0.207	0.368	0.606	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.316	0.604	1.012	0.022	0.044	0.074	E	1.0		
		(LL)	0.232	0.419	0.686	0.009	0.014	0.023	F	1.0		
	D → Y	(HH)	0.314	0.607	1.028	0.022	0.044	0.074	G	1.0		
		(LL)	0.240	0.432	0.716	0.009	0.014	0.023	H	1.0		

FUNCTION BLOCK

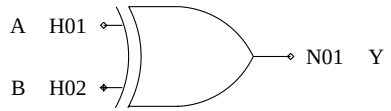
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	E → Y	(HH)	0.306	0.530	0.852	0.022	0.044	0.074				
		(LL)	0.187	0.332	0.544	0.009	0.014	0.023				
	F → Y	(HL)	0.259	0.476	0.788	0.009	0.014	0.023				
		(LH)	0.367	0.678	1.134	0.022	0.044	0.074				
	G → Y	(HL)	0.288	0.533	0.878	0.009	0.014	0.023				
		(LH)	0.397	0.741	1.244	0.022	0.044	0.074				
	H → Y	(HL)	0.296	0.549	0.910	0.009	0.014	0.023				
		(LH)	0.402	0.753	1.266	0.022	0.044	0.074				
F338N3	A → Y	(HH)	0.467	0.861	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.301	0.550	0.926	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.476	0.888	1.524	0.006	0.011	0.018	C	1.0		
		(LL)	0.323	0.588	0.987	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.479	0.933	1.615	0.006	0.011	0.018	E	1.0		
		(LL)	0.348	0.636	1.066	0.004	0.007	0.011	F	1.0		
	D → Y	(HH)	0.477	0.936	1.633	0.006	0.011	0.018	G	1.0		
		(LL)	0.357	0.652	1.091	0.004	0.007	0.011	H	1.0		
	E → Y	(HH)	0.449	0.839	1.424	0.006	0.011	0.018				
		(LL)	0.303	0.554	0.929	0.004	0.007	0.011				
	F → Y	(HL)	0.379	0.698	1.172	0.004	0.007	0.011				
		(LH)	0.513	0.984	1.710	0.006	0.011	0.018				
	G → Y	(HL)	0.409	0.756	1.260	0.004	0.007	0.011				
		(LH)	0.543	1.047	1.814	0.006	0.011	0.018				
	H → Y	(HL)	0.417	0.771	1.291	0.004	0.007	0.011				
		(LH)	0.549	1.059	1.836	0.006	0.011	0.018				

[MEMO]

FUNCTION BLOCK

Function	2-INPUT EXCLUSIVE OR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power	L511	3					
x1	F511	4					
x2							
x4							

Logic Diagram



Truth Table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

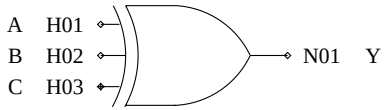
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L511	A → Y	(HH)	0.184	0.328	0.537	0.025	0.045	0.073	A	2.1	Y	11
		(HL)	0.223	0.403	0.654	0.016	0.026	0.044	B	2.1		
		(LH)	0.222	0.396	0.647	0.025	0.045	0.073				
		(LL)	0.261	0.535	0.929	0.017	0.027	0.045				
	B → Y	(HH)	0.167	0.292	0.476	0.025	0.045	0.072				
		(HL)	0.214	0.390	0.661	0.016	0.026	0.044				
		(LH)	0.271	0.474	0.766	0.025	0.045	0.073				
		(LL)	0.263	0.490	0.833	0.017	0.027	0.045				
F511	A → Y	(HH)	0.223	0.391	0.631	0.013	0.023	0.037	A	2.1	Y	22
		(HL)	0.258	0.469	0.765	0.010	0.016	0.026	B	2.1		
		(LH)	0.253	0.455	0.745	0.013	0.023	0.037				
		(LL)	0.306	0.629	1.106	0.011	0.017	0.027				
	B → Y	(HH)	0.192	0.337	0.548	0.013	0.023	0.037				
		(HL)	0.247	0.455	0.773	0.010	0.016	0.026				
		(LH)	0.316	0.545	0.881	0.013	0.023	0.037				
		(LL)	0.307	0.581	1.007	0.011	0.017	0.027				

FUNCTION BLOCK

Function	3-INPUT EXCLUSIVE OR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power	L516	6					
x1	F516	8					
x2							
x4							

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

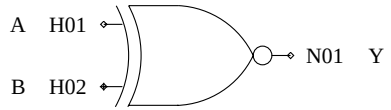
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t_{LD0} (ns)			t_1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L516	A → Y	(HH)	0.319	0.562	0.939	0.025	0.046	0.074	A	1.0	Y	10
		(HL)	0.524	1.005	1.877	0.017	0.028	0.046	B	3.1		
		(LH)	0.508	0.929	1.591	0.025	0.046	0.074	C	2.1		
		(LL)	0.395	0.787	1.546	0.017	0.028	0.046				
	B → Y	(HH)	0.254	0.458	0.752	0.025	0.046	0.074				
		(HL)	0.288	0.582	1.187	0.017	0.028	0.046				
		(LH)	0.297	0.555	0.935	0.025	0.046	0.074				
		(LL)	0.315	0.638	1.228	0.017	0.028	0.046				
	C → Y	(HH)	0.171	0.300	0.457	0.025	0.046	0.074				
		(HL)	0.220	0.395	0.745	0.016	0.027	0.046				
		(LH)	0.222	0.395	0.630	0.025	0.046	0.074				
		(LL)	0.204	0.368	0.633	0.016	0.027	0.045				
F516	A → Y	(HH)	0.351	0.660	1.105	0.013	0.023	0.037	A	1.9	Y	22
		(HL)	0.316	0.611	1.041	0.010	0.016	0.026	B	2.9		
		(LH)	0.330	0.604	1.033	0.013	0.023	0.037	C	1.0		
		(LL)	0.345	0.696	1.248	0.010	0.016	0.026				
	B → Y	(HH)	0.278	0.508	0.841	0.013	0.023	0.037				
		(HL)	0.255	0.511	0.893	0.010	0.016	0.026				
		(LH)	0.270	0.483	0.790	0.013	0.023	0.037				
		(LL)	0.266	0.548	1.003	0.010	0.016	0.026				
	C → Y	(HH)	0.283	0.457	0.728	0.013	0.023	0.037				
		(HL)	0.300	0.537	0.929	0.009	0.015	0.025				
		(LH)	0.319	0.553	0.917	0.013	0.023	0.037				
		(LL)	0.312	0.586	1.094	0.010	0.016	0.026				

FUNCTION BLOCK

Function	2-INPUT EXCLUSIVE NOR												SSI Family	
Block type	Standard type													
	Normal		High speed											
Drivability	Name	cells	Name	cells										
Low Power	L512	3												
x1	F512	4												
x2														
x4														

Logic Diagram



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

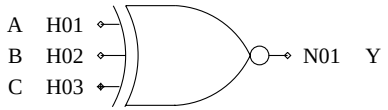
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L512	A → Y	(HH)	0.185	0.329	0.530	0.024	0.045	0.072	A	2.1	Y	11
		(HL)	0.249	0.481	0.815	0.017	0.027	0.045	B	2.1		
		(LH)	0.269	0.489	0.842	0.025	0.045	0.072				
		(LL)	0.262	0.544	0.932	0.017	0.027	0.045				
	B → Y	(HH)	0.203	0.329	0.497	0.025	0.045	0.073				
		(HL)	0.312	0.607	1.033	0.017	0.027	0.045				
		(LH)	0.255	0.498	0.876	0.025	0.045	0.073				
		(LL)	0.202	0.414	0.722	0.017	0.027	0.045				
F512	A → Y	(HH)	0.260	0.413	0.634	0.013	0.023	0.037	A	2.1	Y	21
		(HL)	0.362	0.724	1.266	0.010	0.016	0.026	B	2.1		
		(LH)	0.311	0.571	0.979	0.013	0.023	0.037				
		(LL)	0.276	0.571	1.006	0.010	0.016	0.026				
	B → Y	(HH)	0.240	0.415	0.672	0.013	0.023	0.037				
		(HL)	0.342	0.654	1.124	0.010	0.016	0.026				
		(LH)	0.299	0.579	1.021	0.013	0.023	0.037				
		(LL)	0.323	0.677	1.194	0.010	0.016	0.026				

FUNCTION BLOCK

Function	3-INPUT EXCLUSIVE NOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power	L517	6					
x1	F517	8					
x2							
x4							

Logic Diagram



Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

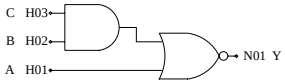
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L517	A → Y	(HH)	0.319	0.557	0.929	0.025	0.046	0.074	A	1.0	Y	10
		(HL)	0.525	1.009	1.881	0.017	0.028	0.046	B	3.1		
		(LH)	0.509	0.931	1.596	0.025	0.046	0.074	C	2.1		
		(LL)	0.392	0.786	1.539	0.017	0.028	0.046				
	B → Y	(HH)	0.253	0.453	0.742	0.025	0.046	0.074				
		(HL)	0.285	0.579	1.185	0.017	0.028	0.046				
		(LH)	0.297	0.553	0.934	0.025	0.046	0.074				
		(LL)	0.313	0.635	1.215	0.017	0.028	0.046				
	C → Y	(HH)	0.170	0.299	0.455	0.025	0.046	0.074				
		(HL)	0.221	0.394	0.742	0.016	0.027	0.046				
		(LH)	0.223	0.393	0.634	0.025	0.046	0.074				
		(LL)	0.204	0.370	0.637	0.016	0.027	0.045				
F517	A → Y	(HH)	0.352	0.653	1.094	0.013	0.023	0.037	A	1.9	Y	22
		(HL)	0.315	0.616	1.050	0.010	0.016	0.026	B	2.9		
		(LH)	0.330	0.602	1.031	0.013	0.023	0.037	C	1.0		
		(LL)	0.345	0.694	1.241	0.010	0.016	0.026				
	B → Y	(HH)	0.277	0.505	0.836	0.013	0.023	0.037				
		(HL)	0.251	0.515	0.905	0.010	0.016	0.026				
		(LH)	0.269	0.482	0.791	0.013	0.023	0.037				
		(LL)	0.269	0.541	0.990	0.010	0.016	0.026				
	C → Y	(HH)	0.282	0.457	0.729	0.013	0.023	0.037				
		(HL)	0.300	0.536	0.929	0.009	0.015	0.025				
		(LH)	0.320	0.553	0.916	0.013	0.023	0.037				
		(LL)	0.313	0.586	1.094	0.010	0.016	0.026				

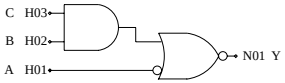
FUNCTION BLOCK

Function	1-2-INPUT AND-OR-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L421	2	L421NA	2	L421NB	3	L421NC	3	L421ND	2	L421NE	3		
x1	F421	3	F421NA	4	F421NB	4	F421NC	5	F421ND	4	F421NE	4		
x2	F421NP	5	F421NAP	5	F421NBP	6	F421NCP	6	F421NDP	5	F421NEP	6		
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

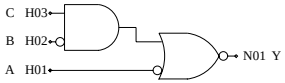
Logic Diagram for "Normal type"



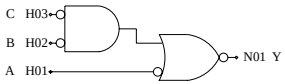
Logic Diagram for "with inv. A type"



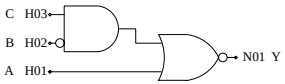
Logic Diagram for "with inv. B type"



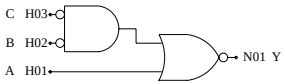
Logic Diagram for "with inv. C type"



Logic Diagram for "with inv. D type"



Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L421	A → Y	(HL)	0.085	0.131	0.178	0.017	0.027	0.045	A	1.0	Y	5
		(LH)	0.104	0.242	0.392	0.036	0.092	0.151	B	1.0		
	B → Y	(HL)	0.121	0.180	0.260	0.024	0.044	0.076	C	1.0		
		(LH)	0.119	0.239	0.389	0.047	0.092	0.151				
	C → Y	(HL)	0.103	0.163	0.270	0.024	0.044	0.076				
		(LH)	0.144	0.290	0.488	0.046	0.091	0.150				
F421	A → Y	(HL)	0.074	0.116	0.161	0.009	0.014	0.022	A	2.0	Y	12
		(LH)	0.090	0.183	0.283	0.018	0.045	0.075	B	2.1		
	B → Y	(HL)	0.103	0.162	0.246	0.012	0.022	0.038	C	2.1		
		(LH)	0.124	0.248	0.401	0.023	0.045	0.075				
	C → Y	(HL)	0.104	0.164	0.248	0.012	0.022	0.038				
		(LH)	0.123	0.250	0.400	0.023	0.045	0.075				
F421NP	A → Y	(HL)	0.223	0.424	0.675	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.255	0.673	1.157	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.310	0.524	0.843	0.004	0.007	0.011	C	1.0		
		(LH)	0.294	0.587	1.030	0.006	0.011	0.018				
	C → Y	(HL)	0.288	0.522	0.877	0.004	0.007	0.011				
		(LH)	0.351	0.711	1.238	0.006	0.011	0.018				
L421NA	A → Y	(HH)	0.138	0.359	0.580	0.034	0.092	0.151	A	1.0	Y	6
		(LL)	0.144	0.250	0.388	0.017	0.028	0.045	B	1.0		
	B → Y	(HL)	0.122	0.175	0.245	0.030	0.051	0.085	C	1.0		
		(LH)	0.097	0.200	0.312	0.044	0.089	0.148				
	C → Y	(HL)	0.105	0.180	0.282	0.030	0.051	0.085				
		(LH)	0.141	0.290	0.476	0.047	0.092	0.151				
F421NA	A → Y	(HH)	0.171	0.333	0.520	0.018	0.046	0.076	A	1.0	Y	12
		(LL)	0.176	0.302	0.487	0.009	0.014	0.024	B	2.0		
	B → Y	(HL)	0.103	0.161	0.242	0.012	0.022	0.039	C	2.0		
		(LH)	0.121	0.246	0.396	0.023	0.046	0.076				
	C → Y	(HL)	0.101	0.160	0.241	0.012	0.022	0.039				
		(LH)	0.120	0.245	0.395	0.023	0.046	0.075				
F421NAP	A → Y	(HH)	0.306	0.784	1.341	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.290	0.545	0.900	0.004	0.007	0.011	B	1.0		
	B → Y	(HL)	0.312	0.526	0.847	0.004	0.007	0.011	C	1.0		
		(LH)	0.293	0.587	1.028	0.006	0.011	0.018				
	C → Y	(HL)	0.293	0.527	0.881	0.004	0.007	0.011				
		(LH)	0.354	0.713	1.242	0.006	0.011	0.018				
L421NB	A → Y	(HH)	0.127	0.345	0.565	0.034	0.092	0.151	A	1.0	Y	6
		(LL)	0.139	0.238	0.366	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.163	0.311	0.495	0.044	0.088	0.148	C	1.0		
		(LL)	0.173	0.289	0.458	0.030	0.051	0.086				
	C → Y	(HL)	0.108	0.184	0.292	0.030	0.051	0.085				
		(LH)	0.141	0.287	0.476	0.046	0.092	0.151				
F421NB	A → Y	(HH)	0.173	0.339	0.529	0.018	0.046	0.076	A	1.0	Y	12
		(LL)	0.178	0.307	0.494	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.229	0.412	0.646	0.023	0.046	0.076	C	2.0		
		(LL)	0.196	0.339	0.558	0.012	0.022	0.039				
	C → Y	(HL)	0.104	0.164	0.248	0.012	0.022	0.039				
		(LH)	0.121	0.246	0.397	0.023	0.046	0.076				
F421NBP	A → Y	(HH)	0.298	0.780	1.348	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.282	0.527	0.876	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.360	0.710	1.225	0.006	0.011	0.018	C	1.0		
		(LL)	0.365	0.644	1.071	0.005	0.007	0.012				
	C → Y	(HL)	0.301	0.541	0.904	0.005	0.007	0.012				
		(LH)	0.356	0.721	1.260	0.006	0.011	0.018				

FUNCTION BLOCK

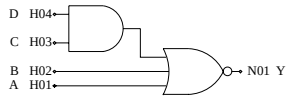
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L421NC	A → Y	(HH)	0.132	0.349	0.569	0.034	0.092	0.151	A	1.0	Y	6
		(LL)	0.139	0.241	0.370	0.017	0.026	0.044	B	1.0		
	B → Y	(HH)	0.181	0.332	0.522	0.044	0.089	0.148	C	1.0		
		(LL)	0.178	0.298	0.475	0.030	0.051	0.086				
	C → Y	(HH)	0.202	0.391	0.643	0.046	0.091	0.151				
		(LL)	0.179	0.305	0.493	0.030	0.051	0.086				
F421NC	A → Y	(HH)	0.170	0.331	0.518	0.018	0.046	0.076	A	1.0	Y	12
		(LL)	0.174	0.300	0.485	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.232	0.415	0.649	0.023	0.046	0.076	C	1.0		
		(LL)	0.203	0.351	0.575	0.012	0.022	0.039				
	C → Y	(HH)	0.223	0.405	0.636	0.023	0.046	0.076				
		(LL)	0.197	0.341	0.563	0.012	0.022	0.039				
F421NCP	A → Y	(HH)	0.307	0.793	1.362	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.291	0.542	0.899	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.361	0.710	1.226	0.006	0.011	0.018	C	1.0		
		(LL)	0.364	0.643	1.069	0.005	0.007	0.012				
	C → Y	(HH)	0.435	0.849	1.457	0.006	0.011	0.018				
		(LL)	0.373	0.664	1.117	0.005	0.007	0.012				
L421ND	A → Y	(HL)	0.077	0.125	0.163	0.018	0.027	0.045	A	1.0	Y	6
		(LH)	0.086	0.246	0.394	0.034	0.092	0.151	B	1.0		
	B → Y	(HH)	0.162	0.309	0.490	0.044	0.088	0.148	C	1.0		
		(LL)	0.173	0.290	0.461	0.031	0.051	0.086				
	C → Y	(HL)	0.109	0.189	0.297	0.030	0.051	0.086				
		(LH)	0.140	0.290	0.480	0.047	0.092	0.151				
F421ND	A → Y	(HL)	0.074	0.116	0.158	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.089	0.180	0.280	0.018	0.046	0.076	B	1.0		
	B → Y	(HH)	0.222	0.402	0.634	0.023	0.046	0.076	C	2.0		
		(LL)	0.197	0.342	0.563	0.012	0.022	0.039				
	C → Y	(HL)	0.102	0.162	0.245	0.012	0.022	0.039				
		(LH)	0.118	0.239	0.386	0.023	0.046	0.076				
F421NDP	A → Y	(HL)	0.223	0.421	0.672	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.256	0.675	1.158	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.356	0.700	1.209	0.006	0.011	0.018	C	1.0		
		(LL)	0.362	0.641	1.066	0.004	0.007	0.011				
	C → Y	(HL)	0.297	0.536	0.898	0.004	0.007	0.011				
		(LH)	0.353	0.713	1.243	0.006	0.011	0.018				
L421NE	A → Y	(HL)	0.077	0.125	0.164	0.018	0.027	0.045	A	1.0	Y	6
		(LH)	0.086	0.249	0.395	0.034	0.092	0.152	B	1.0		
	B → Y	(HH)	0.163	0.310	0.492	0.044	0.088	0.148	C	1.0		
		(LL)	0.174	0.291	0.462	0.031	0.051	0.086				
	C → Y	(HH)	0.222	0.421	0.680	0.047	0.092	0.151				
		(LL)	0.190	0.322	0.526	0.031	0.051	0.086				
F421NE	A → Y	(HL)	0.074	0.116	0.158	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.089	0.179	0.279	0.018	0.046	0.076	B	1.0		
	B → Y	(HH)	0.222	0.404	0.635	0.023	0.046	0.076	C	1.0		
		(LL)	0.202	0.349	0.576	0.013	0.023	0.039				
	C → Y	(HH)	0.218	0.399	0.628	0.023	0.046	0.076				
		(LL)	0.198	0.340	0.560	0.013	0.023	0.039				
F421NEP	A → Y	(HL)	0.225	0.423	0.674	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.258	0.686	1.182	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.361	0.711	1.229	0.006	0.011	0.018	C	1.0		
		(LL)	0.364	0.645	1.073	0.005	0.007	0.012				
	C → Y	(HH)	0.437	0.854	1.466	0.006	0.011	0.018				
		(LL)	0.381	0.677	1.137	0.005	0.007	0.012				

[MEMO]

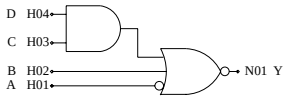
FUNCTION BLOCK

Function	1-1-2-INPUT AND-OR-INVERTER										SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L422	2	L422NA	3	L422NB	3	L422NC	4	L422ND	4	L422NE	3
x1	F422	4	F422NA	5	F422NB	5	F422NC	6	F422ND	6	F422NE	5
x2	F422NP	5	F422NAP	6	F422NBP	6	F422NCP	7	F422NDP	7	F422NEP	6
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power	L422NF	4	L422NG	3	L422NH	3						
x1	F422NF	6	F422NG	5	F422NH	5						
x2	F422NFP	7	F422NGP	6	F422NHP	6						
x4												
x8												

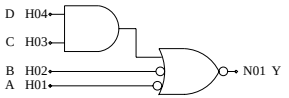
Logic Diagram for "Normal type"



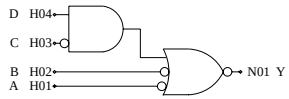
Logic Diagram for "with inv. A type"



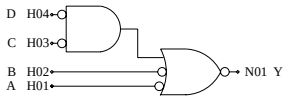
Logic Diagram for "with inv. B type"



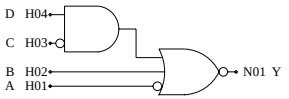
Logic Diagram for "with inv. C type"



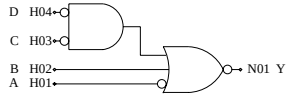
Logic Diagram for "with inv. D type"



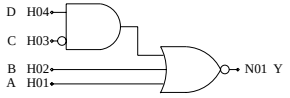
Logic Diagram for "with inv. E type"



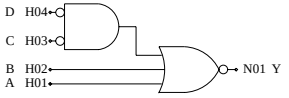
Logic Diagram for "with inv. F type"



Logic Diagram for "with inv. G type"



Logic Diagram for "with inv. H type"



FUNCTION BLOCK

Block type	Switching speed Path IN → OUT		t LD0 (ns) MIN.	t LD0 (ns) TYP.	t LD0 (ns) MAX.	t 1 MIN.	t 1 TYP.	t 1 MAX.	Input Symbol	Input Fanin	Output Symbol	Output Fanout
L422	A → Y	(HL)	0.090	0.133	0.183	0.017	0.027	0.045	A	1.0	Y	3
		(LH)	0.129	0.329	0.551	0.055	0.135	0.226	B	1.0		
	B → Y	(HL)	0.099	0.150	0.200	0.017	0.027	0.045	C	1.0		
		(LH)	0.127	0.378	0.663	0.055	0.135	0.226	D	1.0		
	C → Y	(HL)	0.126	0.192	0.279	0.024	0.044	0.076				
		(LH)	0.168	0.362	0.610	0.066	0.135	0.226				
	D → Y	(HL)	0.107	0.175	0.290	0.024	0.044	0.077				
		(LH)	0.203	0.440	0.756	0.066	0.134	0.225				
F422	A → Y	(HL)	0.079	0.123	0.171	0.009	0.014	0.022	A	2.0	Y	6
		(LH)	0.121	0.251	0.409	0.029	0.069	0.115	B	2.0		
	B → Y	(HL)	0.093	0.145	0.193	0.009	0.013	0.022	C	2.1		
		(LH)	0.134	0.359	0.602	0.029	0.069	0.115	D	2.1		
	C → Y	(HL)	0.113	0.183	0.279	0.012	0.022	0.039				
		(LH)	0.198	0.426	0.709	0.035	0.069	0.115				
	D → Y	(HL)	0.114	0.182	0.280	0.012	0.022	0.039				
		(LH)	0.198	0.426	0.709	0.035	0.069	0.115				
F422NP	A → Y	(HL)	0.229	0.423	0.680	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.351	0.857	1.537	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.245	0.442	0.705	0.004	0.007	0.011	C	1.0		
		(LH)	0.348	0.910	1.644	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.299	0.525	0.866	0.004	0.007	0.011				
		(LH)	0.410	0.866	1.548	0.006	0.011	0.018				
	D → Y	(HL)	0.282	0.513	0.873	0.004	0.007	0.011				
		(LH)	0.452	0.964	1.733	0.006	0.011	0.018				
L422NA	A → Y	(HH)	0.166	0.429	0.719	0.056	0.135	0.226	A	1.0	Y	3
		(LL)	0.146	0.246	0.388	0.016	0.026	0.044	B	1.0		
	B → Y	(HL)	0.095	0.148	0.198	0.017	0.027	0.045	C	1.0		
		(LH)	0.123	0.372	0.638	0.055	0.135	0.226	D	1.0		
	C → Y	(HL)	0.123	0.187	0.274	0.024	0.044	0.076				
		(LH)	0.161	0.349	0.579	0.066	0.135	0.226				
	D → Y	(HL)	0.106	0.175	0.284	0.024	0.044	0.076				
		(LH)	0.196	0.429	0.727	0.066	0.134	0.225				
F422NA	A → Y	(HH)	0.198	0.401	0.645	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.181	0.314	0.505	0.009	0.014	0.023	B	2.0		
	B → Y	(HL)	0.094	0.144	0.195	0.009	0.014	0.023	C	2.0		
		(LH)	0.132	0.352	0.591	0.030	0.070	0.115	D	2.0		
	C → Y	(HL)	0.113	0.181	0.276	0.012	0.022	0.039				
		(LH)	0.199	0.423	0.702	0.035	0.070	0.115				
	D → Y	(HL)	0.115	0.182	0.277	0.012	0.022	0.039				
		(LH)	0.199	0.425	0.704	0.035	0.070	0.115				
F422NAP	A → Y	(HH)	0.395	0.973	1.741	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.291	0.534	0.891	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.247	0.440	0.702	0.005	0.007	0.012	C	1.0		
		(LH)	0.352	0.921	1.666	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.301	0.528	0.869	0.005	0.007	0.012				
		(LH)	0.415	0.878	1.574	0.006	0.011	0.018				
	D → Y	(HL)	0.284	0.516	0.877	0.005	0.007	0.012				
		(LH)	0.456	0.977	1.756	0.006	0.011	0.018				
L422NB	A → Y	(HH)	0.171	0.435	0.724	0.056	0.135	0.226	A	1.0	Y	3
		(LL)	0.147	0.248	0.393	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.199	0.509	0.849	0.056	0.135	0.226	C	1.0		
		(LL)	0.160	0.273	0.431	0.017	0.027	0.045	D	1.0		
	C → Y	(HL)	0.123	0.186	0.274	0.024	0.044	0.076				
		(LH)	0.163	0.355	0.584	0.066	0.135	0.226				
	D → Y	(HL)	0.106	0.176	0.284	0.024	0.044	0.077				
		(LH)	0.197	0.430	0.731	0.066	0.134	0.225				

FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F422NB	A → Y	(HH)	0.197	0.400	0.644	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.180	0.309	0.499	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.239	0.521	0.842	0.030	0.070	0.115	C	2.0		
		(LL)	0.191	0.331	0.533	0.009	0.014	0.023	D	2.0		
	C → Y	(HL)	0.113	0.180	0.275	0.012	0.022	0.039				
		(LH)	0.201	0.428	0.708	0.035	0.070	0.115				
	D → Y	(HL)	0.114	0.181	0.277	0.012	0.022	0.039				
		(LH)	0.202	0.429	0.711	0.035	0.070	0.115				
F422NBP	A → Y	(HH)	0.405	0.984	1.754	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.297	0.541	0.906	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.425	1.051	1.868	0.006	0.011	0.018	C	1.0		
		(LL)	0.303	0.556	0.924	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.301	0.527	0.869	0.005	0.007	0.012				
		(LH)	0.416	0.881	1.576	0.006	0.011	0.018				
	D → Y	(HL)	0.284	0.515	0.880	0.005	0.007	0.012				
		(LH)	0.457	0.980	1.759	0.006	0.011	0.018				
L422NC	A → Y	(HH)	0.171	0.432	0.723	0.056	0.135	0.226	A	1.0	Y	3
		(LL)	0.147	0.247	0.393	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.201	0.509	0.848	0.056	0.135	0.226	C	1.0		
		(LL)	0.162	0.276	0.437	0.017	0.027	0.045	D	1.0		
	C → Y	(HH)	0.254	0.489	0.791	0.066	0.135	0.226				
		(LL)	0.184	0.317	0.517	0.024	0.044	0.077				
	D → Y	(HL)	0.107	0.179	0.291	0.024	0.044	0.077				
		(LH)	0.196	0.429	0.729	0.066	0.134	0.225				
F422NC	A → Y	(HH)	0.202	0.407	0.652	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.186	0.320	0.515	0.009	0.014	0.024	B	1.0		
	B → Y	(HH)	0.242	0.526	0.849	0.030	0.070	0.115	C	1.0		
		(LL)	0.195	0.339	0.547	0.009	0.014	0.023	D	2.0		
	C → Y	(HH)	0.307	0.585	0.948	0.035	0.069	0.115				
		(LL)	0.204	0.353	0.589	0.013	0.022	0.039				
	D → Y	(HL)	0.115	0.184	0.281	0.013	0.022	0.039				
		(LH)	0.201	0.428	0.708	0.035	0.070	0.115				
F422NCP	A → Y	(HH)	0.406	0.978	1.739	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.299	0.550	0.920	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.423	1.040	1.848	0.006	0.011	0.018	C	1.0		
		(LL)	0.305	0.555	0.928	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.505	1.010	1.766	0.006	0.011	0.018				
		(LL)	0.358	0.653	1.106	0.004	0.007	0.011				
	D → Y	(HL)	0.282	0.518	0.885	0.004	0.007	0.011				
		(LH)	0.454	0.969	1.737	0.006	0.011	0.018				
L422ND	A → Y	(HH)	0.171	0.431	0.719	0.055	0.134	0.225	A	1.0	Y	3
		(LL)	0.147	0.247	0.393	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.196	0.505	0.843	0.055	0.134	0.225	C	1.0		
		(LL)	0.161	0.274	0.434	0.017	0.027	0.045	D	1.0		
	C → Y	(HH)	0.255	0.494	0.795	0.066	0.134	0.225				
		(LL)	0.183	0.315	0.512	0.024	0.044	0.077				
	D → Y	(HH)	0.289	0.563	0.935	0.066	0.134	0.225				
		(LL)	0.182	0.314	0.521	0.024	0.044	0.077				
F422ND	A → Y	(HH)	0.198	0.401	0.644	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.181	0.312	0.501	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.242	0.524	0.845	0.030	0.070	0.115	C	1.0		
		(LL)	0.194	0.336	0.543	0.009	0.014	0.023	D	1.0		
	C → Y	(HH)	0.316	0.595	0.958	0.035	0.069	0.115				
		(LL)	0.211	0.369	0.611	0.013	0.023	0.039				
	D → Y	(HH)	0.317	0.597	0.962	0.035	0.070	0.115				
		(LL)	0.214	0.372	0.615	0.013	0.023	0.039				

FUNCTION BLOCK

Block type	Path IN → OUT		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F422NDP	A → Y	(HH)	0.404	0.976	1.736	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.298	0.545	0.912	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.423	1.042	1.848	0.006	0.011	0.018	C	1.0		
		(LL)	0.305	0.556	0.925	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.503	1.008	1.763	0.006	0.011	0.018				
		(LL)	0.357	0.648	1.103	0.004	0.007	0.011				
	D → Y	(HH)	0.542	1.099	1.940	0.006	0.011	0.018				
		(LL)	0.358	0.651	1.109	0.004	0.007	0.011				
L422NE	A → Y	(HH)	0.170	0.430	0.717	0.056	0.135	0.226	A	1.0	Y	3
		(LL)	0.147	0.247	0.393	0.016	0.026	0.044	B	1.0		
	B → Y	(HL)	0.095	0.147	0.197	0.017	0.027	0.045	C	1.0		
		(LH)	0.123	0.369	0.636	0.055	0.135	0.226	D	1.0		
	C → Y	(HH)	0.252	0.488	0.785	0.066	0.135	0.226				
		(LL)	0.181	0.312	0.508	0.024	0.044	0.077				
	D → Y	(HL)	0.107	0.179	0.292	0.024	0.044	0.076				
		(LH)	0.195	0.428	0.725	0.066	0.134	0.225				
F422NE	A → Y	(HH)	0.198	0.401	0.645	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.181	0.312	0.504	0.009	0.014	0.023	B	2.0		
	B → Y	(HL)	0.095	0.144	0.195	0.009	0.014	0.023	C	1.0		
		(LH)	0.131	0.352	0.591	0.030	0.070	0.115	D	2.0		
	C → Y	(HH)	0.315	0.592	0.955	0.035	0.069	0.115				
		(LL)	0.210	0.365	0.606	0.013	0.022	0.039				
	D → Y	(HL)	0.115	0.184	0.282	0.013	0.022	0.039				
		(LH)	0.199	0.423	0.702	0.035	0.070	0.115				
F422NEP	A → Y	(HH)	0.400	0.975	1.744	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.291	0.537	0.891	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.247	0.440	0.703	0.005	0.007	0.012	C	1.0		
		(LH)	0.352	0.919	1.667	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.507	1.017	1.782	0.006	0.011	0.018				
		(LL)	0.356	0.652	1.103	0.005	0.007	0.012				
	D → Y	(HL)	0.283	0.520	0.887	0.005	0.007	0.012				
		(LH)	0.455	0.976	1.755	0.006	0.011	0.018				
L422NF	A → Y	(HH)	0.171	0.431	0.718	0.056	0.135	0.226	A	1.0	Y	3
		(LL)	0.147	0.247	0.393	0.016	0.026	0.044	B	1.0		
	B → Y	(HL)	0.095	0.147	0.197	0.017	0.027	0.045	C	1.0		
		(LH)	0.123	0.369	0.635	0.055	0.135	0.226	D	1.0		
	C → Y	(HH)	0.254	0.489	0.788	0.066	0.135	0.226				
		(LL)	0.183	0.314	0.512	0.024	0.044	0.077				
	D → Y	(HH)	0.287	0.561	0.931	0.066	0.134	0.225				
		(LL)	0.184	0.319	0.530	0.024	0.044	0.077				
F422NF	A → Y	(HH)	0.198	0.400	0.643	0.030	0.070	0.115	A	1.0	Y	6
		(LL)	0.181	0.312	0.505	0.009	0.014	0.023	B	2.0		
	B → Y	(HL)	0.094	0.144	0.194	0.009	0.014	0.023	C	1.0		
		(LH)	0.131	0.352	0.591	0.030	0.070	0.115	D	1.0		
	C → Y	(HH)	0.313	0.592	0.955	0.035	0.069	0.115				
		(LL)	0.212	0.371	0.617	0.013	0.023	0.039				
	D → Y	(HH)	0.315	0.593	0.955	0.035	0.070	0.115				
		(LL)	0.212	0.368	0.613	0.013	0.022	0.039				
F422NFP	A → Y	(HH)	0.400	0.971	1.732	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.298	0.547	0.916	0.004	0.007	0.011	B	1.0		
	B → Y	(HL)	0.245	0.441	0.703	0.004	0.007	0.011	C	1.0		
		(LH)	0.349	0.911	1.649	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.494	0.996	1.750	0.006	0.011	0.018				
		(LL)	0.349	0.638	1.081	0.004	0.007	0.011				
	D → Y	(HH)	0.541	1.097	1.937	0.006	0.011	0.018				
		(LL)	0.356	0.650	1.110	0.004	0.007	0.011				

FUNCTION BLOCK

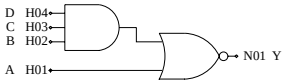
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L422NG	A → Y	(HL)	0.083	0.130	0.177	0.017	0.026	0.043	A	1.0	Y	3
		(LH)	0.123	0.312	0.521	0.055	0.135	0.226	B	1.0		
	B → Y	(HL)	0.095	0.147	0.197	0.017	0.027	0.045	C	1.0		
		(LH)	0.121	0.368	0.633	0.055	0.135	0.226	D	1.0		
	C → Y	(HH)	0.241	0.475	0.770	0.066	0.135	0.226				
		(LL)	0.174	0.299	0.488	0.024	0.044	0.077				
	D → Y	(HL)	0.107	0.179	0.292	0.024	0.044	0.076				
		(LH)	0.194	0.423	0.723	0.066	0.134	0.225				
F422NG	A → Y	(HL)	0.079	0.124	0.170	0.009	0.014	0.023	A	2.0	Y	6
		(LH)	0.118	0.243	0.397	0.030	0.070	0.115	B	2.0		
	B → Y	(HL)	0.095	0.143	0.194	0.009	0.014	0.023	C	1.0		
		(LH)	0.130	0.348	0.586	0.030	0.070	0.115	D	2.0		
	C → Y	(HH)	0.301	0.576	0.935	0.035	0.069	0.115				
		(LL)	0.204	0.353	0.587	0.013	0.022	0.039				
	D → Y	(HL)	0.115	0.183	0.282	0.013	0.022	0.039				
		(LH)	0.196	0.418	0.696	0.035	0.070	0.115				
F422NGP	A → Y	(HL)	0.231	0.422	0.677	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.357	0.868	1.565	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.248	0.442	0.703	0.005	0.007	0.012	C	1.0		
		(LH)	0.353	0.923	1.674	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.498	1.009	1.775	0.006	0.011	0.018				
		(LL)	0.351	0.641	1.087	0.005	0.007	0.012				
	D → Y	(HL)	0.285	0.521	0.893	0.005	0.007	0.012				
		(LH)	0.457	0.979	1.762	0.006	0.011	0.018				
L422NH	A → Y	(HL)	0.083	0.130	0.177	0.017	0.026	0.043	A	1.0	Y	3
		(LH)	0.124	0.312	0.521	0.055	0.135	0.226	B	1.0		
	B → Y	(HL)	0.095	0.147	0.197	0.017	0.027	0.045	C	1.0		
		(LH)	0.121	0.368	0.633	0.055	0.135	0.226	D	1.0		
	C → Y	(HH)	0.245	0.479	0.775	0.066	0.135	0.226				
		(LL)	0.177	0.301	0.493	0.024	0.044	0.077				
	D → Y	(HH)	0.281	0.553	0.921	0.066	0.134	0.225				
		(LL)	0.182	0.313	0.513	0.024	0.044	0.077				
F422NH	A → Y	(HL)	0.079	0.123	0.170	0.009	0.014	0.023	A	2.0	Y	6
		(LH)	0.119	0.242	0.395	0.029	0.070	0.115	B	2.0		
	B → Y	(HL)	0.095	0.142	0.194	0.009	0.014	0.023	C	1.0		
		(LH)	0.130	0.347	0.584	0.030	0.070	0.115	D	1.0		
	C → Y	(HH)	0.305	0.580	0.939	0.035	0.069	0.115				
		(LL)	0.207	0.358	0.595	0.013	0.023	0.039				
	D → Y	(HH)	0.309	0.586	0.947	0.035	0.070	0.115				
		(LL)	0.212	0.369	0.612	0.013	0.023	0.039				
F422NHP	A → Y	(HL)	0.231	0.422	0.677	0.005	0.007	0.012	A	1.0	Y	46
		(LH)	0.356	0.868	1.565	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.248	0.442	0.705	0.005	0.007	0.012	C	1.0		
		(LH)	0.353	0.923	1.674	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.502	1.013	1.780	0.006	0.011	0.018				
		(LL)	0.352	0.643	1.090	0.005	0.007	0.012				
	D → Y	(HH)	0.543	1.108	1.962	0.006	0.011	0.018				
		(LL)	0.358	0.654	1.113	0.005	0.007	0.012				

[MEMO]

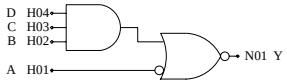
FUNCTION BLOCK

Function	1-3-INPUT AND-OR-INVERTER											SSI Family
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L423	2	L423NA	3	L423NB	3	L423NC	4	L423ND	4	L423NE	3
x1	F423	4	F423NA	5	F423NB	5	F423NC	6	F423ND	6	F423NE	5
x2	F423NP	5	F423NAP	6	F423NBP	6	F423NCP	7	F423NDP	7	F423NEP	6
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power	L423NF	3	L423NG	4								
x1	F423NF	5	F423NG	6								
x2	F423NFP	6	F423NGP	7								
x4												
x8												

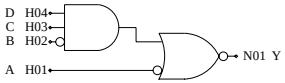
Logic Diagram for "Normal type"



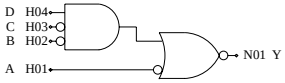
Logic Diagram for "with inv. A type"



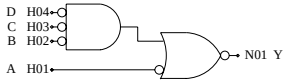
Logic Diagram for "with inv. B type"



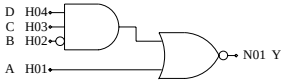
Logic Diagram for "with inv. C type"



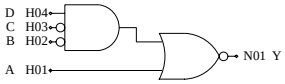
Logic Diagram for "with inv. D type"



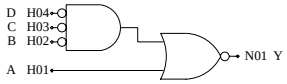
Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"



Logic Diagram for "with inv. G type"



Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L423	A → Y	(HL)	0.086	0.135	0.184	0.017	0.027	0.044	A	1.0	Y	5
		(LH)	0.095	0.332	0.553	0.031	0.091	0.150	B	1.0		
	B → Y	(HL)	0.154	0.231	0.351	0.038	0.068	0.117	C	1.0		
		(LH)	0.125	0.252	0.409	0.046	0.091	0.151	D	1.0		
	C → Y	(HL)	0.154	0.244	0.395	0.038	0.068	0.117				
		(LH)	0.155	0.309	0.516	0.046	0.091	0.150				
	D → Y	(HL)	0.151	0.268	0.456	0.038	0.068	0.117				
		(LH)	0.192	0.393	0.667	0.043	0.088	0.147				
F423	A → Y	(HL)	0.086	0.134	0.180	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.097	0.256	0.408	0.016	0.046	0.076	B	2.1		
	B → Y	(HL)	0.157	0.259	0.405	0.020	0.035	0.060	C	2.1		
		(LH)	0.165	0.333	0.543	0.023	0.046	0.076	D	2.1		
	C → Y	(HL)	0.160	0.254	0.399	0.020	0.035	0.060				
		(LH)	0.160	0.322	0.523	0.023	0.046	0.076				
	D → Y	(HL)	0.156	0.259	0.405	0.020	0.035	0.060				
		(LH)	0.165	0.332	0.541	0.023	0.046	0.076				
F423NP	A → Y	(HL)	0.224	0.432	0.684	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.245	0.745	1.278	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.347	0.598	0.978	0.004	0.007	0.011	C	1.0		
		(LH)	0.296	0.591	1.036	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.342	0.627	1.056	0.004	0.007	0.011				
		(LH)	0.356	0.720	1.256	0.006	0.011	0.018				
	D → Y	(HL)	0.334	0.628	1.072	0.004	0.007	0.011				
		(LH)	0.381	0.780	1.356	0.006	0.011	0.018				
L423NA	A → Y	(HH)	0.125	0.397	0.660	0.031	0.092	0.151	A	1.0	Y	6
		(LL)	0.139	0.240	0.367	0.016	0.026	0.044	B	1.0		
	B → Y	(HL)	0.131	0.195	0.281	0.037	0.066	0.114	C	1.0		
		(LH)	0.100	0.205	0.327	0.044	0.089	0.148	D	1.0		
	C → Y	(HL)	0.131	0.228	0.363	0.037	0.066	0.114				
		(LH)	0.145	0.296	0.490	0.046	0.092	0.151				
	D → Y	(HL)	0.123	0.229	0.378	0.037	0.066	0.115				
		(LH)	0.164	0.343	0.573	0.046	0.091	0.150				
F423NA	A → Y	(HH)	0.162	0.384	0.608	0.016	0.046	0.076	A	1.0	Y	12
		(LL)	0.173	0.305	0.481	0.009	0.014	0.024	B	2.0		
	B → Y	(HL)	0.143	0.231	0.354	0.020	0.035	0.060	C	2.1		
		(LH)	0.145	0.297	0.476	0.023	0.046	0.076	D	2.1		
	C → Y	(HL)	0.143	0.244	0.383	0.020	0.035	0.060				
		(LH)	0.157	0.319	0.519	0.023	0.046	0.076				
	D → Y	(HL)	0.143	0.230	0.351	0.020	0.035	0.060				
		(LH)	0.144	0.296	0.475	0.023	0.046	0.076				
F423NAP	A → Y	(HH)	0.289	0.847	1.461	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.281	0.535	0.890	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.351	0.601	0.985	0.005	0.007	0.012	C	1.0		
		(LH)	0.299	0.601	1.053	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.344	0.631	1.065	0.005	0.007	0.012				
		(LH)	0.360	0.729	1.274	0.006	0.011	0.018				
	D → Y	(HL)	0.338	0.633	1.080	0.005	0.007	0.012				
		(LH)	0.383	0.788	1.374	0.006	0.011	0.018				
L423NB	A → Y	(HH)	0.130	0.400	0.663	0.031	0.092	0.151	A	1.0	Y	6
		(LL)	0.139	0.243	0.372	0.017	0.026	0.044	B	1.0		
	B → Y	(HH)	0.182	0.335	0.525	0.044	0.089	0.148	C	1.0		
		(LL)	0.187	0.317	0.511	0.037	0.067	0.115	D	1.0		
	C → Y	(HL)	0.132	0.232	0.372	0.037	0.066	0.115				
		(LH)	0.143	0.296	0.489	0.047	0.092	0.151				
	D → Y	(HL)	0.125	0.235	0.389	0.037	0.066	0.115				
		(LH)	0.164	0.342	0.573	0.046	0.091	0.150				

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F423NB	A → Y	(HH)	0.165	0.387	0.612	0.016	0.046	0.076	A	1.0	Y	12
		(LL)	0.177	0.310	0.497	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.253	0.459	0.723	0.023	0.046	0.076	C	2.1		
		(LL)	0.239	0.406	0.664	0.020	0.035	0.060	D	2.1		
	C → Y	(HL)	0.144	0.246	0.389	0.020	0.035	0.060				
		(LH)	0.157	0.317	0.518	0.023	0.046	0.076				
	D → Y	(HL)	0.145	0.232	0.357	0.020	0.035	0.060				
		(LH)	0.143	0.295	0.474	0.023	0.046	0.076				
F423NBP	A → Y	(HH)	0.294	0.851	1.468	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.282	0.538	0.888	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.379	0.734	1.255	0.006	0.011	0.018	C	1.0		
		(LL)	0.400	0.724	1.215	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.346	0.635	1.073	0.005	0.007	0.012				
		(LH)	0.359	0.729	1.277	0.006	0.011	0.018				
	D → Y	(HL)	0.340	0.638	1.092	0.005	0.007	0.012				
		(LH)	0.383	0.788	1.377	0.006	0.011	0.018				
L423NC	A → Y	(HH)	0.130	0.399	0.662	0.031	0.092	0.151	A	1.0	Y	6
		(LL)	0.139	0.243	0.373	0.016	0.026	0.044	B	1.0		
	B → Y	(HH)	0.184	0.337	0.528	0.044	0.089	0.148	C	1.0		
		(LL)	0.188	0.319	0.512	0.037	0.067	0.115	D	1.0		
	C → Y	(HH)	0.228	0.428	0.691	0.046	0.092	0.151				
		(LL)	0.207	0.363	0.600	0.037	0.067	0.115				
	D → Y	(HL)	0.126	0.236	0.391	0.037	0.066	0.115				
		(LH)	0.163	0.341	0.571	0.046	0.091	0.150				
F423NC	A → Y	(HH)	0.165	0.387	0.613	0.016	0.046	0.076	A	1.0	Y	12
		(LL)	0.177	0.310	0.498	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.252	0.457	0.720	0.023	0.046	0.076	C	1.0		
		(LL)	0.240	0.407	0.667	0.020	0.035	0.060	D	2.1		
	C → Y	(HH)	0.265	0.488	0.773	0.023	0.046	0.076				
		(LL)	0.249	0.431	0.713	0.020	0.035	0.060				
	D → Y	(HL)	0.144	0.233	0.359	0.020	0.035	0.060				
		(LH)	0.143	0.294	0.473	0.023	0.046	0.076				
F423NCP	A → Y	(HH)	0.295	0.847	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.288	0.548	0.907	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.378	0.729	1.245	0.006	0.011	0.018	C	1.0		
		(LL)	0.399	0.722	1.212	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.440	0.857	1.463	0.006	0.011	0.018				
		(LL)	0.419	0.766	1.294	0.004	0.007	0.011				
	D → Y	(HL)	0.336	0.636	1.088	0.004	0.007	0.011				
		(LH)	0.381	0.783	1.360	0.006	0.011	0.018				
L423ND	A → Y	(HH)	0.133	0.406	0.673	0.031	0.092	0.151	A	1.0	Y	6
		(LL)	0.143	0.249	0.385	0.017	0.028	0.046	B	1.0		
	B → Y	(HH)	0.185	0.339	0.532	0.044	0.089	0.148	C	1.0		
		(LL)	0.188	0.321	0.516	0.037	0.067	0.115	D	1.0		
	C → Y	(HH)	0.229	0.429	0.695	0.046	0.092	0.151				
		(LL)	0.210	0.367	0.600	0.037	0.067	0.115				
	D → Y	(HH)	0.245	0.470	0.773	0.046	0.091	0.150				
		(LL)	0.215	0.375	0.617	0.037	0.066	0.114				
F423ND	A → Y	(HH)	0.164	0.386	0.612	0.016	0.046	0.076	A	1.0	Y	12
		(LL)	0.177	0.310	0.497	0.009	0.014	0.023	B	1.0		
	B → Y	(HH)	0.250	0.458	0.724	0.023	0.046	0.076	C	1.0		
		(LL)	0.244	0.420	0.684	0.020	0.035	0.060	D	1.0		
	C → Y	(HH)	0.264	0.485	0.770	0.023	0.046	0.076				
		(LL)	0.250	0.435	0.715	0.020	0.035	0.060				
	D → Y	(HH)	0.253	0.459	0.724	0.023	0.046	0.076				
		(LL)	0.243	0.414	0.677	0.020	0.035	0.060				

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F423NDP	A → Y	(HH)	0.295	0.847	1.457	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.288	0.549	0.905	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.378	0.727	1.244	0.006	0.011	0.018	C	1.0		
		(LL)	0.397	0.721	1.208	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.439	0.855	1.460	0.006	0.011	0.018				
		(LL)	0.418	0.763	1.289	0.004	0.007	0.011				
	D → Y	(HH)	0.462	0.909	1.556	0.006	0.011	0.018				
		(LL)	0.424	0.773	1.312	0.004	0.007	0.011				
L423NE	A → Y	(HL)	0.078	0.126	0.162	0.018	0.028	0.045	A	1.0	Y	6
		(LH)	0.082	0.294	0.486	0.031	0.092	0.151	B	1.0		
	B → Y	(HH)	0.170	0.321	0.505	0.044	0.089	0.148	C	1.0		
		(LL)	0.183	0.311	0.500	0.037	0.066	0.115	D	1.0		
	C → Y	(HL)	0.133	0.236	0.378	0.037	0.066	0.115				
		(LH)	0.146	0.300	0.489	0.046	0.092	0.151				
	D → Y	(HL)	0.127	0.238	0.394	0.037	0.066	0.115				
		(LH)	0.165	0.341	0.576	0.046	0.091	0.150				
F423NE	A → Y	(HL)	0.069	0.114	0.152	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.078	0.226	0.363	0.016	0.046	0.076	B	1.0		
	B → Y	(HH)	0.239	0.444	0.705	0.023	0.046	0.076	C	2.1		
		(LL)	0.237	0.403	0.661	0.020	0.035	0.060	D	2.1		
	C → Y	(HL)	0.144	0.245	0.387	0.020	0.035	0.060				
		(LH)	0.153	0.312	0.511	0.023	0.046	0.076				
	D → Y	(HL)	0.145	0.231	0.355	0.020	0.035	0.060				
		(LH)	0.141	0.290	0.467	0.023	0.046	0.076				
F423NEP	A → Y	(HL)	0.227	0.433	0.682	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.247	0.754	1.302	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.377	0.734	1.259	0.006	0.011	0.018	C	1.0		
		(LL)	0.405	0.729	1.225	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.348	0.639	1.078	0.005	0.007	0.012				
		(LH)	0.360	0.731	1.281	0.006	0.011	0.018				
	D → Y	(HL)	0.341	0.641	1.096	0.005	0.007	0.012				
		(LH)	0.384	0.790	1.380	0.006	0.011	0.018				
L423NF	A → Y	(HL)	0.078	0.126	0.163	0.018	0.028	0.045	A	1.0	Y	6
		(LH)	0.083	0.293	0.485	0.031	0.092	0.151	B	1.0		
	B → Y	(HH)	0.174	0.328	0.512	0.044	0.089	0.148	C	1.0		
		(LL)	0.184	0.312	0.502	0.037	0.066	0.115	D	1.0		
	C → Y	(HH)	0.226	0.425	0.687	0.046	0.092	0.151				
		(LL)	0.209	0.365	0.596	0.037	0.066	0.115				
	D → Y	(HL)	0.128	0.239	0.398	0.037	0.066	0.115				
		(LH)	0.164	0.340	0.573	0.046	0.091	0.150				
F423NF	A → Y	(HL)	0.069	0.114	0.151	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.077	0.226	0.364	0.016	0.046	0.076	B	1.0		
	B → Y	(HH)	0.244	0.447	0.710	0.023	0.046	0.076	C	1.0		
		(LL)	0.239	0.407	0.667	0.020	0.035	0.060	D	2.1		
	C → Y	(HH)	0.259	0.478	0.762	0.023	0.046	0.076				
		(LL)	0.247	0.429	0.704	0.020	0.035	0.060				
	D → Y	(HL)	0.145	0.232	0.357	0.020	0.035	0.060				
		(LH)	0.141	0.289	0.465	0.023	0.046	0.076				
F423NFP	A → Y	(HL)	0.228	0.435	0.687	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.249	0.759	1.312	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.376	0.734	1.262	0.006	0.011	0.018	C	1.0		
		(LL)	0.401	0.723	1.215	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.443	0.868	1.490	0.006	0.011	0.018				
		(LL)	0.425	0.776	1.309	0.005	0.007	0.012				
	D → Y	(HL)	0.345	0.648	1.110	0.005	0.007	0.012				
		(LH)	0.386	0.793	1.393	0.006	0.011	0.018				

FUNCTION BLOCK

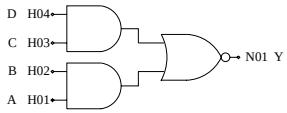
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L423NG	A → Y	(HL)	0.077	0.125	0.162	0.018	0.028	0.045	A	1.0	Y	6
		(LH)	0.081	0.291	0.485	0.031	0.092	0.151	B	1.0		
	B → Y	(HH)	0.174	0.329	0.519	0.044	0.089	0.148	C	1.0		
		(LL)	0.184	0.313	0.502	0.037	0.066	0.115	D	1.0		
	C → Y	(HH)	0.226	0.426	0.690	0.046	0.092	0.151				
		(LL)	0.211	0.367	0.603	0.037	0.066	0.115				
	D → Y	(HH)	0.245	0.468	0.771	0.046	0.091	0.150				
		(LL)	0.216	0.377	0.623	0.037	0.067	0.115				
F423NG	A → Y	(HL)	0.069	0.113	0.151	0.009	0.014	0.023	A	2.0	Y	12
		(LH)	0.078	0.225	0.363	0.016	0.046	0.076	B	1.0		
	B → Y	(HH)	0.248	0.453	0.719	0.023	0.046	0.076	C	1.0		
		(LL)	0.245	0.422	0.688	0.020	0.035	0.060	D	1.0		
	C → Y	(HH)	0.260	0.478	0.762	0.023	0.046	0.076				
		(LL)	0.249	0.433	0.710	0.020	0.035	0.060				
	D → Y	(HH)	0.244	0.449	0.711	0.023	0.046	0.076				
		(LL)	0.242	0.414	0.677	0.020	0.035	0.060				
F423NGP	A → Y	(HL)	0.223	0.429	0.681	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.245	0.744	1.280	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.368	0.715	1.229	0.006	0.011	0.018	C	1.0		
		(LL)	0.393	0.710	1.192	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.436	0.852	1.456	0.006	0.011	0.018				
		(LL)	0.419	0.765	1.294	0.004	0.007	0.011				
	D → Y	(HH)	0.461	0.907	1.554	0.006	0.011	0.018				
		(LL)	0.424	0.775	1.314	0.004	0.007	0.011				

[MEMO]

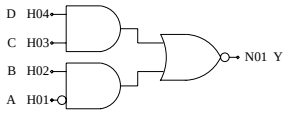
FUNCTION BLOCK

Function	2-2-INPUT AND-OR-INVERTER										SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L424	2	L424NA	3	L424NB	3	L424NC	4	L424ND	3	L424NE	4
x1	F424	4	F424NA	5	F424NB	5	F424NC	6	F424ND	5	F424NE	6
x2	F424NP	5	F424NAP	6	F424NBP	6	F424NCP	7	F424NDP	6	F424NEP	7
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												

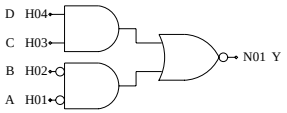
Logic Diagram for "Normal type"



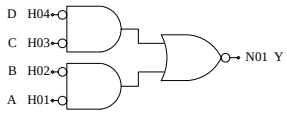
Logic Diagram for "with inv. A type"



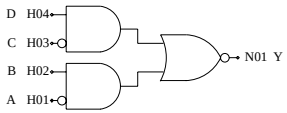
Logic Diagram for "with inv. B type"



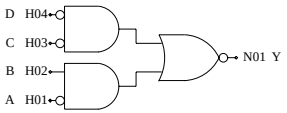
Logic Diagram for "with inv. C type"



Logic Diagram for "with inv. D type"



Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L424	A → Y	(HL)	0.105	0.167	0.235	0.024	0.044	0.076	A	1.0	Y	5
		(LH)	0.108	0.255	0.412	0.036	0.091	0.151	B	1.0		
	B → Y	(HL)	0.089	0.152	0.238	0.024	0.044	0.076	C	1.0		
		(LH)	0.128	0.306	0.512	0.036	0.091	0.150	D	1.0		
	C → Y	(HL)	0.142	0.219	0.330	0.024	0.044	0.076				
		(LH)	0.123	0.343	0.567	0.035	0.091	0.151				
	D → Y	(HL)	0.124	0.203	0.337	0.024	0.044	0.077				
		(LH)	0.142	0.397	0.668	0.035	0.091	0.150				
F424	A → Y	(HL)	0.097	0.159	0.234	0.012	0.022	0.039	A	2.1	Y	10
		(LH)	0.117	0.249	0.401	0.018	0.046	0.076	B	2.1		
	B → Y	(HL)	0.096	0.159	0.233	0.012	0.022	0.039	C	2.1		
		(LH)	0.117	0.248	0.402	0.018	0.046	0.076	D	2.1		
	C → Y	(HL)	0.126	0.213	0.332	0.012	0.022	0.039				
		(LH)	0.135	0.345	0.561	0.018	0.046	0.076				
	D → Y	(HL)	0.129	0.216	0.334	0.012	0.022	0.039				
		(LH)	0.136	0.346	0.563	0.018	0.046	0.076				
F424NP	A → Y	(HL)	0.279	0.518	0.842	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.286	0.685	1.195	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.266	0.508	0.849	0.004	0.007	0.011	C	1.0		
		(LH)	0.310	0.753	1.318	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.312	0.556	0.912	0.004	0.007	0.011				
		(LH)	0.297	0.768	1.339	0.006	0.011	0.018				
	D → Y	(HL)	0.293	0.544	0.918	0.004	0.007	0.011				
		(LH)	0.318	0.836	1.457	0.006	0.011	0.018				
L424NA	A → Y	(HH)	0.152	0.359	0.590	0.036	0.091	0.150	A	1.0	Y	5
		(LL)	0.156	0.279	0.433	0.025	0.045	0.078	B	1.0		
	B → Y	(HL)	0.092	0.162	0.247	0.025	0.045	0.078	C	1.0		
		(LH)	0.125	0.301	0.504	0.036	0.091	0.150	D	1.0		
	C → Y	(HL)	0.137	0.213	0.321	0.024	0.044	0.076				
		(LH)	0.121	0.332	0.549	0.035	0.092	0.151				
	D → Y	(HL)	0.119	0.204	0.327	0.024	0.044	0.076				
		(LH)	0.138	0.384	0.646	0.035	0.091	0.150				
F424NA	A → Y	(HH)	0.204	0.419	0.670	0.018	0.046	0.076	A	1.0	Y	10
		(LL)	0.199	0.349	0.570	0.012	0.022	0.039	B	2.0		
	B → Y	(HL)	0.099	0.167	0.248	0.012	0.022	0.039	C	2.0		
		(LH)	0.119	0.258	0.419	0.018	0.046	0.076	D	2.0		
	C → Y	(HL)	0.126	0.214	0.333	0.012	0.022	0.039				
		(LH)	0.132	0.337	0.554	0.018	0.046	0.075				
	D → Y	(HL)	0.128	0.216	0.334	0.012	0.022	0.039				
		(LH)	0.134	0.338	0.555	0.018	0.046	0.076				
F424NAP	A → Y	(HH)	0.328	0.787	1.370	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.326	0.623	1.051	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.265	0.509	0.856	0.005	0.007	0.012	C	1.0		
		(LH)	0.307	0.749	1.317	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.312	0.552	0.904	0.005	0.007	0.012				
		(LH)	0.296	0.764	1.334	0.006	0.011	0.018				
	D → Y	(HL)	0.291	0.540	0.910	0.005	0.007	0.012				
		(LH)	0.317	0.831	1.454	0.006	0.011	0.018				
L424NB	A → Y	(HH)	0.158	0.363	0.595	0.036	0.091	0.150	A	1.0	Y	5
		(LL)	0.158	0.280	0.436	0.025	0.045	0.079	B	1.0		
	B → Y	(HH)	0.178	0.419	0.697	0.036	0.091	0.150	C	1.0		
		(LL)	0.167	0.297	0.475	0.025	0.045	0.078	D	1.0		
	C → Y	(HL)	0.137	0.215	0.321	0.024	0.044	0.076				
		(LH)	0.123	0.335	0.552	0.035	0.092	0.151				
	D → Y	(HL)	0.119	0.203	0.328	0.024	0.044	0.076				
		(LH)	0.138	0.387	0.649	0.035	0.091	0.150				

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F424NB	A → Y	(HH)	0.201	0.412	0.662	0.018	0.046	0.076		A	1.0	Y	10
		(LL)	0.198	0.347	0.572	0.012	0.022	0.039		B	1.0		
	B → Y	(HH)	0.201	0.414	0.663	0.018	0.046	0.076		C	2.0		
		(LL)	0.198	0.348	0.570	0.012	0.022	0.039		D	2.0		
	C → Y	(HL)	0.126	0.214	0.332	0.012	0.022	0.039					
		(LH)	0.133	0.342	0.561	0.018	0.046	0.075					
	D → Y	(HL)	0.128	0.215	0.333	0.012	0.022	0.039					
		(LH)	0.134	0.343	0.562	0.018	0.046	0.076					
F424NBP	A → Y	(HH)	0.333	0.792	1.373	0.006	0.011	0.018		A	1.0	Y	46
		(LL)	0.329	0.626	1.054	0.005	0.007	0.012		B	1.0		
	B → Y	(HH)	0.362	0.862	1.504	0.006	0.011	0.018		C	1.0		
		(LL)	0.340	0.643	1.086	0.005	0.007	0.012		D	1.0		
	C → Y	(HL)	0.311	0.552	0.905	0.005	0.007	0.012					
		(LH)	0.296	0.767	1.338	0.006	0.011	0.018					
	D → Y	(HL)	0.292	0.540	0.910	0.005	0.007	0.012					
		(LH)	0.318	0.834	1.457	0.006	0.011	0.018					
L424NC	A → Y	(HH)	0.164	0.371	0.603	0.036	0.091	0.150		A	1.0	Y	5
		(LL)	0.167	0.292	0.462	0.025	0.045	0.079		B	1.0		
	B → Y	(HH)	0.175	0.413	0.689	0.036	0.091	0.150		C	1.0		
		(LL)	0.163	0.286	0.463	0.025	0.045	0.078		D	1.0		
	C → Y	(HH)	0.198	0.463	0.753	0.035	0.092	0.151					
		(LL)	0.195	0.342	0.555	0.024	0.044	0.077					
	D → Y	(HH)	0.212	0.508	0.843	0.035	0.091	0.150					
		(LL)	0.194	0.342	0.565	0.024	0.044	0.077					
F424NC	A → Y	(HH)	0.201	0.412	0.661	0.018	0.046	0.076		A	1.0	Y	10
		(LL)	0.196	0.348	0.570	0.012	0.022	0.039		B	1.0		
	B → Y	(HH)	0.205	0.419	0.669	0.018	0.046	0.076		C	1.0		
		(LL)	0.203	0.355	0.585	0.012	0.022	0.039		D	1.0		
	C → Y	(HH)	0.235	0.504	0.807	0.018	0.046	0.075					
		(LL)	0.223	0.404	0.669	0.012	0.022	0.039					
	D → Y	(HH)	0.236	0.507	0.811	0.018	0.046	0.076					
		(LL)	0.225	0.407	0.671	0.012	0.022	0.039					
F424NCP	A → Y	(HH)	0.342	0.800	1.386	0.006	0.011	0.018		A	1.0	Y	45
		(LL)	0.338	0.642	1.079	0.004	0.007	0.011		B	1.0		
	B → Y	(HH)	0.360	0.858	1.498	0.006	0.011	0.018		C	1.0		
		(LL)	0.336	0.636	1.077	0.004	0.007	0.011		D	1.0		
	C → Y	(HH)	0.378	0.896	1.540	0.006	0.011	0.018					
		(LL)	0.368	0.680	1.145	0.004	0.007	0.011					
	D → Y	(HH)	0.398	0.955	1.653	0.006	0.011	0.018					
		(LL)	0.370	0.682	1.153	0.004	0.007	0.011					
L424ND	A → Y	(HH)	0.157	0.362	0.593	0.036	0.091	0.150		A	1.0	Y	5
		(LL)	0.158	0.279	0.435	0.025	0.045	0.079		B	1.0		
	B → Y	(HL)	0.093	0.160	0.245	0.025	0.045	0.078		C	1.0		
		(LH)	0.125	0.299	0.503	0.036	0.091	0.150		D	1.0		
	C → Y	(HH)	0.197	0.459	0.749	0.035	0.092	0.151					
		(LL)	0.192	0.341	0.552	0.024	0.044	0.076					
	D → Y	(HL)	0.121	0.209	0.337	0.024	0.044	0.077					
		(LH)	0.138	0.383	0.644	0.035	0.091	0.150					
F424ND	A → Y	(HH)	0.201	0.414	0.664	0.018	0.046	0.076		A	1.0	Y	10
		(LL)	0.197	0.343	0.563	0.012	0.022	0.039		B	2.0		
	B → Y	(HL)	0.099	0.165	0.247	0.012	0.022	0.039		C	1.0		
		(LH)	0.119	0.258	0.418	0.018	0.046	0.076		D	2.0		
	C → Y	(HH)	0.234	0.497	0.800	0.018	0.046	0.075					
		(LL)	0.221	0.398	0.661	0.012	0.022	0.039					
	D → Y	(HL)	0.128	0.217	0.337	0.012	0.022	0.039					
		(LH)	0.133	0.337	0.553	0.018	0.046	0.076					

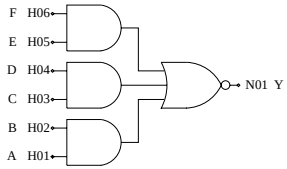
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F424NDP	A → Y	(HH)	0.334	0.790	1.374	0.006	0.011	0.018		A	1.0	Y	46
		(LL)	0.328	0.626	1.053	0.005	0.007	0.012		B	1.0		
	B → Y	(HL)	0.265	0.508	0.854	0.005	0.007	0.012		C	1.0		
		(LH)	0.307	0.748	1.315	0.006	0.011	0.018		D	1.0		
	C → Y	(HH)	0.376	0.888	1.535	0.006	0.011	0.018					
		(LL)	0.366	0.677	1.137	0.005	0.007	0.012					
	D → Y	(HL)	0.294	0.544	0.920	0.005	0.007	0.012					
		(LH)	0.317	0.830	1.453	0.006	0.011	0.018					
L424NE	A → Y	(HH)	0.165	0.374	0.607	0.036	0.091	0.150		A	1.0	Y	5
		(LL)	0.169	0.300	0.467	0.025	0.045	0.078		B	1.0		
	B → Y	(HL)	0.093	0.160	0.246	0.025	0.045	0.078		C	1.0		
		(LH)	0.124	0.299	0.503	0.036	0.091	0.150		D	1.0		
	C → Y	(HH)	0.192	0.454	0.740	0.035	0.092	0.151					
		(LL)	0.188	0.329	0.538	0.024	0.044	0.077					
	D → Y	(HH)	0.211	0.507	0.840	0.035	0.091	0.150					
		(LL)	0.194	0.343	0.565	0.024	0.044	0.077					
F424NE	A → Y	(HH)	0.201	0.415	0.665	0.018	0.046	0.076		A	1.0	Y	10
		(LL)	0.197	0.344	0.563	0.012	0.022	0.039		B	2.0		
	B → Y	(HL)	0.099	0.166	0.248	0.012	0.022	0.039		C	1.0		
		(LH)	0.118	0.258	0.419	0.018	0.046	0.076		D	1.0		
	C → Y	(HH)	0.234	0.500	0.802	0.018	0.046	0.075					
		(LL)	0.223	0.405	0.672	0.012	0.022	0.039					
	D → Y	(HH)	0.236	0.501	0.803	0.018	0.046	0.076					
		(LL)	0.225	0.406	0.671	0.012	0.022	0.039					
F424NEP	A → Y	(HH)	0.344	0.804	1.390	0.006	0.011	0.018		A	1.0	Y	45
		(LL)	0.341	0.648	1.085	0.004	0.007	0.011		B	1.0		
	B → Y	(HL)	0.266	0.511	0.857	0.004	0.007	0.011		C	1.0		
		(LH)	0.309	0.751	1.316	0.006	0.011	0.018		D	1.0		
	C → Y	(HH)	0.372	0.886	1.528	0.006	0.011	0.018					
		(LL)	0.361	0.669	1.126	0.004	0.007	0.011					
	D → Y	(HH)	0.398	0.953	1.649	0.006	0.011	0.018					
		(LL)	0.369	0.682	1.154	0.004	0.007	0.011					

FUNCTION BLOCK

Function	2-2-2-INPUT AND-OR-INVERTER											SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L425	3											
x1	F425	6											
x2	F425NP	6											
x4													
x8													
Block type	with inv. F		with inv. G		with inv. H								
Drivability	Name	cells	Name	cells	Name	cells							
Low Power													
x1													
x2													
x4													
x8													

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

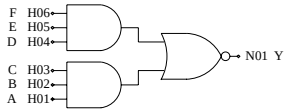
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L425	A → Y	(HL)	0.127	0.221	0.305	0.025	0.045	0.078	A	1.0	Y	2
		(LH)	0.148	0.511	0.889	0.047	0.137	0.228	B	1.0		
	B → Y	(HL)	0.114	0.209	0.312	0.025	0.045	0.078	C	1.0		
		(LH)	0.172	0.591	1.040	0.047	0.137	0.228	D	1.0		
	C → Y	(HL)	0.160	0.259	0.383	0.025	0.045	0.078	E	1.0		
		(LH)	0.179	0.670	1.159	0.047	0.137	0.228	F	1.0		
	D → Y	(HL)	0.141	0.247	0.394	0.025	0.045	0.078				
		(LH)	0.204	0.754	1.306	0.047	0.137	0.228				
	E → Y	(HL)	0.180	0.279	0.451	0.024	0.044	0.077				
		(LH)	0.220	0.771	1.322	0.047	0.138	0.229				
	F → Y	(HL)	0.157	0.264	0.459	0.024	0.044	0.077				
		(LH)	0.242	0.845	1.464	0.046	0.137	0.228				
F425	A → Y	(HL)	0.108	0.185	0.267	0.012	0.022	0.039	A	2.1	Y	5
		(LH)	0.147	0.402	0.691	0.024	0.069	0.115	B	2.1		
	B → Y	(HL)	0.108	0.185	0.265	0.012	0.022	0.039	C	2.1		
		(LH)	0.146	0.400	0.691	0.024	0.069	0.115	D	2.1		
	C → Y	(HL)	0.146	0.238	0.377	0.013	0.023	0.039	E	2.1		
		(LH)	0.189	0.615	1.044	0.023	0.069	0.115	F	2.1		
	D → Y	(HL)	0.148	0.240	0.375	0.013	0.022	0.039				
		(LH)	0.190	0.616	1.044	0.023	0.069	0.115				
	E → Y	(HL)	0.156	0.271	0.436	0.013	0.023	0.040				
		(LH)	0.229	0.714	1.204	0.023	0.069	0.114				
	F → Y	(HL)	0.159	0.272	0.438	0.013	0.023	0.040				
		(LH)	0.231	0.717	1.207	0.023	0.069	0.115				
F425NP	A → Y	(HL)	0.288	0.556	0.903	0.005	0.007	0.012	A	1.0	Y	46
		(LH)	0.339	1.025	1.857	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.271	0.544	0.907	0.005	0.007	0.012	C	1.0		
		(LH)	0.370	1.122	2.048	0.006	0.011	0.018	D	1.1		
	C → Y	(HL)	0.337	0.617	1.003	0.005	0.007	0.012	E	1.0		
		(LH)	0.380	1.233	2.206	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.320	0.606	1.013	0.005	0.007	0.012				
		(LH)	0.413	1.333	2.395	0.006	0.011	0.018				
	E → Y	(HL)	0.356	0.632	1.033	0.005	0.007	0.012				
		(LH)	0.414	1.323	2.353	0.006	0.011	0.018				
	F → Y	(HL)	0.336	0.621	1.043	0.004	0.007	0.012				
		(LH)	0.442	1.416	2.534	0.006	0.011	0.018				

FUNCTION BLOCK

Function	3-3-INPUT AND-OR-INVERTER											SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L426	3											
x1	F426	6											
x2	F426NP	6											
x4													
x8													
Block type	with inv. F		with inv. G		with inv. H								
Drivability	Name	cells	Name	cells	Name	cells							
Low Power													
x1													
x2													
x4													
x8													

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

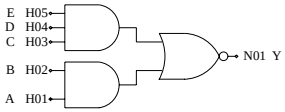
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L426	A → Y	(HL)	0.148	0.253	0.349	0.038	0.068	0.117	A	1.0	Y	4
		(LH)	0.118	0.394	0.659	0.032	0.092	0.152	B	1.0		
	B → Y	(HL)	0.144	0.266	0.389	0.038	0.068	0.117	C	1.0		
		(LH)	0.137	0.451	0.764	0.032	0.092	0.152	D	1.0		
	C → Y	(HL)	0.138	0.282	0.440	0.038	0.068	0.117	E	1.0		
		(LH)	0.159	0.520	0.892	0.031	0.092	0.152	F	1.0		
	D → Y	(HL)	0.211	0.363	0.575	0.038	0.068	0.118				
		(LH)	0.146	0.516	0.857	0.031	0.091	0.151				
	E → Y	(HL)	0.194	0.378	0.619	0.038	0.068	0.118				
		(LH)	0.166	0.579	0.967	0.032	0.092	0.152				
	F → Y	(HL)	0.185	0.396	0.671	0.038	0.068	0.118				
		(LH)	0.190	0.648	1.099	0.031	0.092	0.151				
F426	A → Y	(HL)	0.136	0.254	0.358	0.021	0.037	0.062	A	2.1	Y	10
		(LH)	0.125	0.364	0.606	0.016	0.045	0.075	B	2.1		
	B → Y	(HL)	0.137	0.248	0.352	0.021	0.037	0.062	C	2.1		
		(LH)	0.121	0.347	0.582	0.016	0.045	0.075	D	2.1		
	C → Y	(HL)	0.137	0.254	0.358	0.021	0.037	0.062	E	2.1		
		(LH)	0.125	0.363	0.605	0.016	0.045	0.075	F	2.1		
	D → Y	(HL)	0.206	0.375	0.602	0.019	0.034	0.059				
		(LH)	0.165	0.494	0.813	0.016	0.045	0.075				
	E → Y	(HL)	0.206	0.393	0.636	0.019	0.034	0.059				
		(LH)	0.173	0.520	0.859	0.016	0.045	0.075				
	F → Y	(HL)	0.204	0.372	0.597	0.019	0.034	0.059				
		(LH)	0.165	0.495	0.812	0.015	0.045	0.075				
F426NP	A → Y	(HL)	0.339	0.670	1.063	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.264	0.790	1.374	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.335	0.703	1.145	0.005	0.007	0.012	C	1.0		
		(LH)	0.305	0.911	1.587	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.327	0.703	1.159	0.005	0.007	0.012	E	1.0		
		(LH)	0.322	0.969	1.694	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.421	0.770	1.226	0.004	0.007	0.012				
		(LH)	0.294	0.917	1.584	0.006	0.011	0.018				
	E → Y	(HL)	0.391	0.802	1.304	0.005	0.007	0.012				
		(LH)	0.332	1.032	1.789	0.006	0.011	0.018				
	F → Y	(HL)	0.384	0.803	1.320	0.005	0.007	0.012				
		(LH)	0.347	1.091	1.891	0.006	0.011	0.018				

FUNCTION BLOCK

Function	2-3-INPUT AND-OR-INVERTER										SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L427	3										
x1	F427	5										
x2	F427NP	6										
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

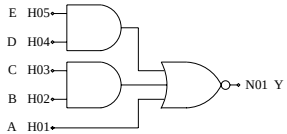
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L427	A → Y	(HL)	0.153	0.271	0.407	0.029	0.050	0.084	A	1.0	Y	4
		(LH)	0.127	0.409	0.661	0.031	0.092	0.152	B	1.0		
	B → Y	(HL)	0.132	0.271	0.443	0.029	0.050	0.084	C	1.0		
		(LH)	0.153	0.491	0.817	0.031	0.091	0.150	D	1.0		
	C → Y	(HL)	0.129	0.219	0.289	0.037	0.066	0.115	E	1.0		
		(LH)	0.101	0.285	0.464	0.034	0.091	0.150				
	D → Y	(HL)	0.126	0.256	0.374	0.037	0.066	0.115				
		(LH)	0.138	0.378	0.634	0.035	0.091	0.150				
	E → Y	(HL)	0.119	0.256	0.392	0.037	0.066	0.115				
		(LH)	0.151	0.426	0.722	0.035	0.091	0.150				
F427	A → Y	(HL)	0.139	0.251	0.391	0.012	0.022	0.039	A	2.0	Y	10
		(LH)	0.138	0.439	0.725	0.016	0.046	0.075	B	2.0		
	B → Y	(HL)	0.138	0.252	0.392	0.012	0.022	0.039	C	2.1		
		(LH)	0.137	0.439	0.725	0.016	0.046	0.075	D	2.1		
	C → Y	(HL)	0.140	0.239	0.356	0.022	0.037	0.061	E	2.0		
		(LH)	0.132	0.300	0.495	0.018	0.045	0.075				
	D → Y	(HL)	0.135	0.250	0.383	0.022	0.037	0.061				
		(LH)	0.139	0.319	0.529	0.018	0.045	0.075				
	E → Y	(HL)	0.141	0.239	0.355	0.022	0.037	0.061				
		(LH)	0.131	0.299	0.492	0.018	0.045	0.075				
F427NP	A → Y	(HL)	0.352	0.634	1.006	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.292	0.846	1.458	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.326	0.634	1.041	0.005	0.007	0.012	C	1.0		
		(LH)	0.327	0.954	1.653	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.339	0.645	1.040	0.005	0.007	0.012	E	1.0		
		(LH)	0.275	0.722	1.254	0.006	0.011	0.018				
	D → Y	(HL)	0.336	0.678	1.120	0.005	0.007	0.012				
		(LH)	0.320	0.841	1.465	0.006	0.011	0.018				
	E → Y	(HL)	0.327	0.679	1.135	0.005	0.007	0.012				
		(LH)	0.340	0.899	1.570	0.006	0.011	0.018				

FUNCTION BLOCK

Function	1-2-2-INPUT AND-OR-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L428	3												
x1	F428	5												
x2	F428NP	6												
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

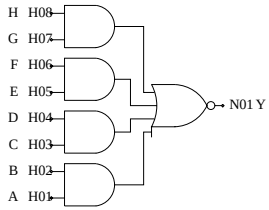
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L428	A → Y	(HL)	0.094	0.153	0.200	0.016	0.026	0.043		A	1.0	Y	2
		(LH)	0.129	0.444	0.770	0.047	0.137	0.228		B	1.0		
	B → Y	(HL)	0.137	0.221	0.317	0.025	0.045	0.078		C	1.1		
		(LH)	0.177	0.511	0.865	0.058	0.137	0.228		D	1.0		
	C → Y	(HL)	0.121	0.211	0.327	0.025	0.045	0.078		E	1.0		
		(LH)	0.209	0.593	1.016	0.058	0.137	0.228					
	D → Y	(HL)	0.149	0.241	0.348	0.024	0.044	0.077					
		(LH)	0.218	0.602	1.012	0.058	0.138	0.229					
	E → Y	(HL)	0.130	0.228	0.354	0.024	0.044	0.077					
		(LH)	0.248	0.679	1.159	0.057	0.137	0.228					
F428	A → Y	(HL)	0.087	0.141	0.188	0.009	0.013	0.022		A	2.0	Y	6
		(LH)	0.126	0.333	0.560	0.024	0.069	0.115		B	2.0		
	B → Y	(HL)	0.120	0.197	0.297	0.012	0.022	0.039		C	2.0		
		(LH)	0.179	0.474	0.804	0.030	0.070	0.115		D	2.0		
	C → Y	(HL)	0.119	0.197	0.297	0.012	0.022	0.039		E	2.0		
		(LH)	0.179	0.475	0.804	0.030	0.070	0.115					
	D → Y	(HL)	0.132	0.213	0.330	0.012	0.023	0.039					
		(LH)	0.219	0.558	0.937	0.029	0.069	0.115					
	E → Y	(HL)	0.133	0.214	0.331	0.012	0.023	0.039					
		(LH)	0.221	0.559	0.940	0.030	0.070	0.115					
F428NP	A → Y	(HL)	0.237	0.449	0.717	0.005	0.007	0.012		A	1.0	Y	46
		(LH)	0.337	1.023	1.849	0.006	0.011	0.018		B	1.0		
	B → Y	(HL)	0.316	0.576	0.943	0.005	0.007	0.012		C	1.1		
		(LH)	0.409	1.064	1.901	0.006	0.011	0.018		D	1.0		
	C → Y	(HL)	0.299	0.564	0.951	0.005	0.007	0.012		E	1.0		
		(LH)	0.447	1.164	2.092	0.006	0.011	0.018					
	D → Y	(HL)	0.331	0.593	0.977	0.005	0.007	0.012					
		(LH)	0.447	1.156	2.051	0.006	0.011	0.018					
	E → Y	(HL)	0.312	0.583	0.983	0.005	0.007	0.012					
		(LH)	0.483	1.252	2.231	0.006	0.011	0.018					

FUNCTION BLOCK

Function	2-2-2-2-INPUT AND-OR-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L429	4												
x1	F429	8												
x2														
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

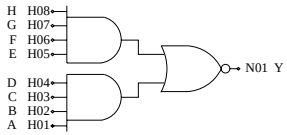
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L429	A → Y	(HL)	0.130	0.237	0.309	0.025	0.045	0.078	A	1.0	Y	0
		(LH)	0.149	0.682	1.237	0.058	0.183	0.306	B	1.0		
	B → Y	(HL)	0.113	0.222	0.319	0.025	0.045	0.078	C	1.0		
		(LH)	0.177	0.784	1.433	0.058	0.183	0.305	D	1.0		
	C → Y	(HL)	0.175	0.296	0.428	0.025	0.045	0.078	E	1.0		
		(LH)	0.244	1.102	1.928	0.059	0.183	0.305	F	1.0		
	D → Y	(HL)	0.158	0.282	0.439	0.025	0.045	0.079	G	1.0		
		(LH)	0.275	1.207	2.123	0.058	0.183	0.305	H	1.0		
	E → Y	(HL)	0.195	0.318	0.487	0.025	0.045	0.079				
		(LH)	0.293	1.260	2.192	0.058	0.183	0.305				
	F → Y	(HL)	0.173	0.304	0.500	0.025	0.045	0.079				
		(LH)	0.326	1.364	2.392	0.058	0.183	0.305				
	G → Y	(HL)	0.202	0.320	0.513	0.025	0.045	0.079				
		(LH)	0.339	1.360	2.353	0.058	0.184	0.306				
	H → Y	(HL)	0.178	0.306	0.524	0.025	0.045	0.079				
		(LH)	0.367	1.458	2.543	0.057	0.183	0.305				
F429	A → Y	(HL)	0.119	0.209	0.303	0.012	0.022	0.038	A	2.1	Y	1
		(LH)	0.175	0.590	1.052	0.029	0.092	0.153	B	2.1		
	B → Y	(HL)	0.121	0.210	0.303	0.012	0.022	0.038	C	2.1		
		(LH)	0.176	0.590	1.053	0.029	0.092	0.153	D	2.1		
	C → Y	(HL)	0.156	0.258	0.410	0.012	0.022	0.038	E	2.1		
		(LH)	0.246	0.930	1.613	0.029	0.091	0.153	F	2.1		
	D → Y	(HL)	0.157	0.260	0.410	0.012	0.022	0.038	G	2.1		
		(LH)	0.250	0.935	1.615	0.030	0.092	0.153	H	2.1		
	E → Y	(HL)	0.172	0.293	0.480	0.012	0.022	0.039				
		(LH)	0.314	1.143	1.960	0.029	0.092	0.153				
	F → Y	(HL)	0.175	0.292	0.478	0.012	0.022	0.039				
		(LH)	0.313	1.143	1.957	0.029	0.092	0.153				
	G → Y	(HL)	0.178	0.306	0.506	0.013	0.023	0.040				
		(LH)	0.355	1.233	2.108	0.029	0.092	0.153				
	H → Y	(HL)	0.178	0.306	0.505	0.012	0.023	0.040				
		(LH)	0.355	1.233	2.109	0.029	0.092	0.153				

FUNCTION BLOCK

Function	4-4-INPUT AND-OR-INVERTER											SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L442	4											
x1	F442	8											
x2													
x4													
x8													
Block type	with inv. F		with inv. G		with inv. H								
Drivability	Name	cells	Name	cells	Name	cells							
Low Power													
x1													
x2													
x4													
x8													

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

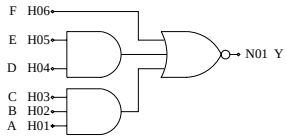
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t LD0 (ns)			t 1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L442	A → Y	(HL)	0.157	0.297	0.394	0.046	0.085	0.148	A	1.0	Y	2
		(LH)	0.112	0.437	0.729	0.031	0.091	0.151	B	1.0		
	B → Y	(HL)	0.163	0.327	0.462	0.046	0.085	0.148	C	1.0		
		(LH)	0.133	0.495	0.839	0.030	0.091	0.151	D	1.0		
	C → Y	(HL)	0.172	0.380	0.556	0.046	0.085	0.148	E	1.0		
		(LH)	0.157	0.591	1.009	0.030	0.091	0.151	F	1.0		
	D → Y	(HL)	0.172	0.383	0.577	0.046	0.085	0.148	G	1.0		
		(LH)	0.167	0.635	1.092	0.030	0.091	0.151	H	1.0		
	E → Y	(HL)	0.238	0.510	0.831	0.045	0.086	0.149				
		(LH)	0.163	0.626	1.029	0.030	0.091	0.151				
	F → Y	(HL)	0.241	0.542	0.901	0.045	0.086	0.149				
		(LH)	0.180	0.681	1.144	0.030	0.091	0.151				
	G → Y	(HL)	0.251	0.592	0.993	0.045	0.086	0.149				
		(LH)	0.206	0.779	1.309	0.030	0.091	0.151				
	H → Y	(HL)	0.250	0.595	1.010	0.045	0.086	0.149				
		(LH)	0.218	0.826	1.396	0.030	0.091	0.151				
F442	A → Y	(HL)	0.169	0.333	0.499	0.023	0.043	0.074	A	2.2	Y	7
		(LH)	0.144	0.443	0.746	0.015	0.046	0.076	B	2.1		
	B → Y	(HL)	0.175	0.346	0.526	0.023	0.043	0.074	C	2.1		
		(LH)	0.147	0.449	0.762	0.015	0.046	0.076	D	2.1		
	C → Y	(HL)	0.176	0.348	0.530	0.023	0.043	0.074	E	2.1		
		(LH)	0.148	0.452	0.765	0.015	0.046	0.076	F	2.1		
	D → Y	(HL)	0.172	0.335	0.504	0.023	0.043	0.074	G	2.1		
		(LH)	0.143	0.444	0.750	0.015	0.046	0.076	H	2.1		
	E → Y	(HL)	0.283	0.558	0.934	0.023	0.043	0.075				
		(LH)	0.193	0.638	1.056	0.015	0.046	0.076				
	F → Y	(HL)	0.287	0.571	0.958	0.023	0.043	0.075				
		(LH)	0.198	0.647	1.073	0.015	0.046	0.076				
	G → Y	(HL)	0.287	0.571	0.958	0.023	0.043	0.075				
		(LH)	0.198	0.647	1.072	0.015	0.046	0.076				
	H → Y	(HL)	0.283	0.558	0.934	0.023	0.043	0.075				
		(LH)	0.195	0.641	1.058	0.015	0.046	0.076				

FUNCTION BLOCK

Function	1-2-3-INPUT AND-OR-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L462	3												
x1	F462	6												
x2														
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

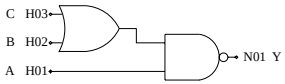
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L462	A → Y	(HL)	0.171	0.310	0.535	0.037	0.067	0.116	A	1.0	Y	3
		(LH)	0.283	0.679	1.150	0.055	0.136	0.227	B	1.0		
	B → Y	(HL)	0.175	0.313	0.522	0.037	0.067	0.116	C	1.0		
		(LH)	0.255	0.604	1.011	0.055	0.136	0.227	D	1.0		
	C → Y	(HL)	0.181	0.283	0.435	0.037	0.067	0.116	E	1.0		
		(LH)	0.198	0.453	0.742	0.054	0.134	0.224	F	1.0		
	D → Y	(HL)	0.119	0.228	0.339	0.029	0.050	0.084				
		(LH)	0.184	0.713	1.255	0.051	0.134	0.225				
	E → Y	(HL)	0.137	0.228	0.301	0.029	0.050	0.084				
		(LH)	0.134	0.588	1.013	0.052	0.136	0.227				
	F → Y	(HL)	0.085	0.144	0.181	0.017	0.026	0.044				
		(LH)	0.108	0.595	1.045	0.040	0.136	0.227				
F462	A → Y	(HL)	0.182	0.306	0.475	0.019	0.034	0.059	A	2.1	Y	7
		(LH)	0.253	0.634	1.057	0.029	0.069	0.115	B	2.1		
	B → Y	(HL)	0.185	0.322	0.509	0.019	0.034	0.059	C	2.1		
		(LH)	0.267	0.667	1.121	0.029	0.069	0.115	D	2.1		
	C → Y	(HL)	0.181	0.304	0.474	0.019	0.034	0.059	E	2.1		
		(LH)	0.252	0.632	1.056	0.029	0.069	0.115	F	2.0		
	D → Y	(HL)	0.109	0.193	0.275	0.012	0.022	0.039				
		(LH)	0.154	0.544	0.931	0.027	0.069	0.115				
	E → Y	(HL)	0.111	0.194	0.275	0.012	0.022	0.039				
		(LH)	0.155	0.544	0.931	0.027	0.069	0.115				
	F → Y	(HL)	0.081	0.134	0.178	0.009	0.014	0.022				
		(LH)	0.108	0.397	0.681	0.022	0.069	0.115				

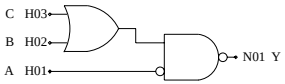
FUNCTION BLOCK

Function	1-2-INPUT OR-AND-INVERTER											SSI Family
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L431	2	L431NA	2	L431NB	3	L431NC	3	L431ND	2	L431NE	3
x1	F431	3	F431NA	4	F431NB	4	F431NC	5	F431ND	4	F431NE	4
x2	F431NP	5	F431NAP	5	F431NBP	6	F431NCP	6	F431NDP	5	F431NEP	6
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												

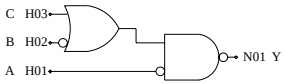
Logic Diagram for "Normal type"



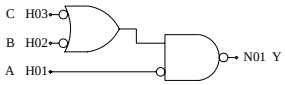
Logic Diagram for "with inv. A type"



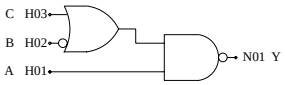
Logic Diagram for "with inv. B type"



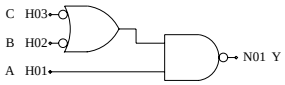
Logic Diagram for "with inv. C type"



Logic Diagram for "with inv. D type"



Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L431	A → Y	(HL)	0.107	0.183	0.263	0.024	0.049	0.083	A	1.0	Y	7
		(LH)	0.083	0.132	0.187	0.025	0.046	0.073	B	1.0		
	B → Y	(HL)	0.099	0.168	0.273	0.029	0.049	0.083	C	1.0		
		(LH)	0.157	0.283	0.462	0.043	0.088	0.147				
	C → Y	(HL)	0.112	0.184	0.303	0.029	0.049	0.083				
		(LH)	0.144	0.292	0.500	0.043	0.088	0.147				
F431	A → Y	(HL)	0.105	0.170	0.232	0.013	0.026	0.043	A	2.0	Y	15
		(LH)	0.078	0.123	0.173	0.012	0.023	0.036	B	2.1		
	B → Y	(HL)	0.096	0.168	0.264	0.016	0.026	0.043	C	2.1		
		(LH)	0.136	0.259	0.431	0.022	0.044	0.073				
	C → Y	(HL)	0.096	0.168	0.264	0.016	0.026	0.043				
		(LH)	0.136	0.259	0.431	0.022	0.044	0.073				
F431NP	A → Y	(HL)	0.242	0.526	0.853	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.228	0.409	0.673	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.261	0.473	0.795	0.004	0.007	0.011	C	1.0		
		(LH)	0.353	0.666	1.151	0.006	0.011	0.018				
	C → Y	(HL)	0.287	0.524	0.875	0.004	0.007	0.011				
		(LH)	0.351	0.714	1.243	0.006	0.011	0.018				
L431NA	A → Y	(HH)	0.127	0.223	0.339	0.024	0.045	0.072	A	1.0	Y	8
		(LL)	0.147	0.300	0.476	0.021	0.051	0.086	B	1.0		
	B → Y	(HL)	0.088	0.146	0.228	0.025	0.045	0.078	C	1.0		
		(LH)	0.139	0.237	0.384	0.046	0.092	0.151				
	C → Y	(HL)	0.108	0.185	0.292	0.031	0.051	0.086				
		(LH)	0.140	0.285	0.477	0.046	0.092	0.151				
F431NA	A → Y	(HH)	0.163	0.271	0.402	0.013	0.023	0.037	A	1.0	Y	15
		(LL)	0.189	0.342	0.554	0.013	0.026	0.043	B	2.0		
	B → Y	(HL)	0.098	0.173	0.272	0.016	0.026	0.043	C	2.0		
		(LH)	0.130	0.247	0.408	0.022	0.044	0.074				
	C → Y	(HL)	0.097	0.171	0.270	0.015	0.026	0.043				
		(LH)	0.130	0.246	0.408	0.022	0.044	0.074				
F431NAP	A → Y	(HH)	0.273	0.510	0.845	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.302	0.648	1.081	0.004	0.007	0.011	B	1.0		
	B → Y	(HL)	0.260	0.475	0.806	0.004	0.007	0.011	C	1.0		
		(LH)	0.353	0.665	1.148	0.006	0.011	0.018				
	C → Y	(HL)	0.296	0.536	0.896	0.004	0.007	0.011				
		(LH)	0.352	0.710	1.242	0.006	0.011	0.018				
L431NB	A → Y	(HH)	0.123	0.215	0.332	0.025	0.045	0.072	A	1.0	Y	7
		(LL)	0.141	0.286	0.457	0.021	0.051	0.086	B	1.0		
	B → Y	(HH)	0.188	0.351	0.570	0.047	0.092	0.151	C	1.0		
		(LL)	0.156	0.269	0.439	0.025	0.045	0.078				
	C → Y	(HL)	0.106	0.183	0.288	0.030	0.051	0.085				
		(LH)	0.140	0.289	0.480	0.047	0.092	0.151				
F431NB	A → Y	(HH)	0.162	0.270	0.400	0.013	0.023	0.037	A	1.0	Y	15
		(LL)	0.188	0.340	0.551	0.013	0.026	0.043	B	1.0		
	B → Y	(HH)	0.220	0.404	0.651	0.022	0.044	0.074	C	2.0		
		(LL)	0.206	0.353	0.577	0.016	0.026	0.043				
	C → Y	(HL)	0.098	0.173	0.273	0.016	0.026	0.043				
		(LH)	0.131	0.248	0.411	0.022	0.044	0.074				
F431NBP	A → Y	(HH)	0.272	0.510	0.849	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.297	0.639	1.068	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.403	0.785	1.356	0.006	0.011	0.018	C	1.0		
		(LL)	0.328	0.601	1.017	0.005	0.007	0.012				
	C → Y	(HL)	0.297	0.536	0.898	0.005	0.007	0.012				
		(LH)	0.356	0.722	1.265	0.006	0.011	0.018				

FUNCTION BLOCK

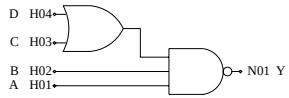
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L431NC	A → Y	(HH)	0.128	0.219	0.331	0.024	0.045	0.073	A	1.0	Y	7
		(LL)	0.141	0.288	0.458	0.021	0.051	0.086	B	1.0		
	B → Y	(HH)	0.187	0.351	0.570	0.047	0.092	0.151	C	1.0		
		(LL)	0.157	0.268	0.440	0.025	0.045	0.078				
	C → Y	(HH)	0.222	0.419	0.678	0.047	0.092	0.151				
		(LL)	0.188	0.320	0.513	0.030	0.051	0.086				
F431NC	A → Y	(HH)	0.162	0.269	0.400	0.013	0.023	0.037	A	1.0	Y	15
		(LL)	0.188	0.340	0.551	0.013	0.026	0.043	B	1.0		
	B → Y	(HH)	0.221	0.406	0.652	0.022	0.044	0.074	C	1.0		
		(LL)	0.206	0.353	0.577	0.016	0.026	0.043				
	C → Y	(HH)	0.227	0.415	0.663	0.022	0.044	0.074				
		(LL)	0.210	0.363	0.595	0.016	0.026	0.043				
F431NCP	A → Y	(HH)	0.275	0.514	0.854	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.299	0.644	1.076	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.404	0.788	1.362	0.006	0.011	0.018	C	1.0		
		(LL)	0.328	0.603	1.017	0.005	0.007	0.012				
	C → Y	(HH)	0.437	0.854	1.469	0.006	0.011	0.018				
		(LL)	0.379	0.674	1.127	0.005	0.007	0.012				
L431ND	A → Y	(HL)	0.088	0.183	0.253	0.021	0.051	0.085	A	1.0	Y	7
		(LH)	0.073	0.117	0.161	0.025	0.046	0.073	B	1.0		
	B → Y	(HH)	0.192	0.355	0.578	0.046	0.092	0.151	C	1.0		
		(LL)	0.155	0.266	0.434	0.025	0.045	0.078				
	C → Y	(HL)	0.106	0.181	0.283	0.031	0.051	0.085				
		(LH)	0.143	0.293	0.489	0.046	0.092	0.151				
F431ND	A → Y	(HL)	0.095	0.155	0.215	0.013	0.026	0.043	A	2.0	Y	15
		(LH)	0.072	0.112	0.155	0.013	0.023	0.037	B	1.0		
	B → Y	(HH)	0.223	0.410	0.657	0.022	0.044	0.074	C	2.0		
		(LL)	0.202	0.344	0.564	0.016	0.026	0.043				
	C → Y	(HL)	0.094	0.161	0.252	0.015	0.025	0.042				
		(LH)	0.131	0.251	0.413	0.022	0.044	0.074				
F431NDP	A → Y	(HL)	0.242	0.528	0.861	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.227	0.408	0.672	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.402	0.782	1.344	0.006	0.011	0.018	C	1.0		
		(LL)	0.325	0.594	1.005	0.004	0.007	0.011				
	C → Y	(HL)	0.294	0.530	0.884	0.004	0.007	0.011				
		(LH)	0.356	0.718	1.253	0.006	0.011	0.018				
L431NE	A → Y	(HL)	0.084	0.181	0.251	0.021	0.051	0.085	A	1.0	Y	7
		(LH)	0.073	0.114	0.156	0.025	0.046	0.074	B	1.0		
	B → Y	(HH)	0.190	0.359	0.577	0.047	0.092	0.151	C	1.0		
		(LL)	0.157	0.264	0.434	0.025	0.045	0.078				
	C → Y	(HH)	0.226	0.426	0.690	0.047	0.092	0.151				
		(LL)	0.187	0.317	0.513	0.030	0.051	0.085				
F431NE	A → Y	(HL)	0.094	0.155	0.215	0.013	0.026	0.043	A	2.0	Y	15
		(LH)	0.072	0.112	0.155	0.013	0.023	0.037	B	1.0		
	B → Y	(HH)	0.230	0.420	0.669	0.022	0.044	0.074	C	1.0		
		(LL)	0.204	0.348	0.568	0.016	0.026	0.043				
	C → Y	(HH)	0.225	0.413	0.662	0.022	0.044	0.074				
		(LL)	0.200	0.338	0.554	0.016	0.026	0.043				
F431NEP	A → Y	(HL)	0.246	0.535	0.868	0.005	0.007	0.012	A	1.0	Y	46
		(LH)	0.230	0.413	0.678	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.407	0.792	1.365	0.006	0.011	0.018	C	1.0		
		(LL)	0.327	0.598	1.014	0.005	0.007	0.012				
	C → Y	(HH)	0.441	0.862	1.476	0.006	0.011	0.018				
		(LL)	0.377	0.671	1.125	0.005	0.007	0.012				

[MEMO]

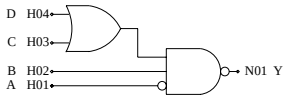
FUNCTION BLOCK

Function	1-1-2-INPUT OR-AND-INVERTER											
									SSI Family			
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L432	2	L432NA	3	L432NB	3	L432NC	4	L432ND	4	L432NE	3
x1	F432	5	F432NA	5	F432NB	5	F432NC	6	F432ND	6	F432NE	5
x2	F432NP	5	F432NAP	6	F432NBP	6	F432NCP	7	F432NDP	7	F432NEP	6
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power	L432NF	4	L432NG	3	L432NH	3						
x1	F432NF	6	F432NG	5	F432NH	5						
x2	F432NFP	7	F432NGP	6	F432NHP	6						
x4												
x8												

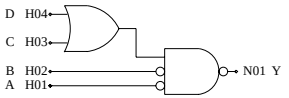
Logic Diagram for "Normal type"



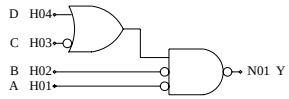
Logic Diagram for "with inv. A type"



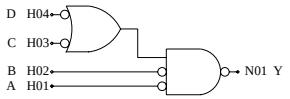
Logic Diagram for "with inv. B type"



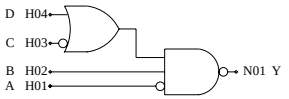
Logic Diagram for "with inv. C type"



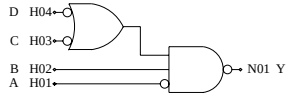
Logic Diagram for "with inv. D type"



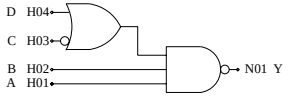
Logic Diagram for "with inv. E type"



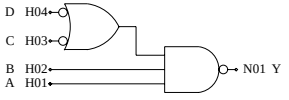
Logic Diagram for "with inv. F type"



Logic Diagram for "with inv. G type"



Logic Diagram for "with inv. H type"



FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L432	A → Y	(HL)	0.116	0.213	0.315	0.033	0.068	0.117	A	1.0	Y	7
		(LH)	0.083	0.134	0.191	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.113	0.225	0.362	0.033	0.068	0.117	C	1.0		
		(LH)	0.099	0.161	0.235	0.024	0.045	0.072	D	1.0		
	C → Y	(HL)	0.120	0.210	0.369	0.038	0.068	0.116				
		(LH)	0.175	0.330	0.553	0.044	0.088	0.147				
	D → Y	(HL)	0.135	0.241	0.411	0.038	0.068	0.117				
		(LH)	0.164	0.342	0.593	0.044	0.088	0.147				
F432	A → Y	(HL)	0.141	0.222	0.314	0.022	0.039	0.065	A	2.0	Y	14
		(LH)	0.083	0.137	0.193	0.012	0.023	0.036	B	2.0		
	B → Y	(HL)	0.119	0.235	0.366	0.022	0.040	0.065	C	2.1		
		(LH)	0.100	0.167	0.244	0.012	0.023	0.036	D	2.1		
	C → Y	(HL)	0.147	0.266	0.422	0.024	0.039	0.065				
		(LH)	0.169	0.341	0.582	0.022	0.044	0.074				
	D → Y	(HL)	0.147	0.266	0.422	0.024	0.039	0.065				
		(LH)	0.169	0.341	0.583	0.022	0.044	0.074				
F432NP	A → Y	(HL)	0.313	0.615	1.015	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.238	0.428	0.705	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.309	0.627	1.056	0.004	0.007	0.011	C	1.0		
		(LH)	0.259	0.467	0.773	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.330	0.621	1.057	0.004	0.007	0.011				
		(LH)	0.383	0.756	1.325	0.006	0.011	0.018				
	D → Y	(HL)	0.340	0.644	1.099	0.004	0.007	0.011				
		(LH)	0.372	0.768	1.363	0.006	0.011	0.018				
L432NA	A → Y	(HH)	0.133	0.235	0.357	0.024	0.045	0.072	A	1.0	Y	7
		(LL)	0.163	0.321	0.519	0.033	0.069	0.119	B	1.0		
	B → Y	(HL)	0.114	0.229	0.358	0.033	0.069	0.119	C	1.0		
		(LH)	0.097	0.159	0.231	0.025	0.046	0.073	D	1.0		
	C → Y	(HL)	0.120	0.224	0.362	0.039	0.069	0.119				
		(LH)	0.170	0.317	0.531	0.043	0.088	0.147				
	D → Y	(HL)	0.131	0.247	0.406	0.038	0.068	0.117				
		(LH)	0.158	0.329	0.567	0.043	0.088	0.147				
F432NA	A → Y	(HH)	0.179	0.309	0.472	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.217	0.406	0.657	0.022	0.040	0.066	B	2.0		
	B → Y	(HL)	0.127	0.203	0.283	0.022	0.040	0.066	C	2.0		
		(LH)	0.076	0.126	0.175	0.013	0.023	0.037	D	2.0		
	C → Y	(HL)	0.147	0.262	0.415	0.025	0.040	0.066				
		(LH)	0.163	0.328	0.555	0.022	0.044	0.074				
	D → Y	(HL)	0.145	0.260	0.412	0.025	0.040	0.066				
		(LH)	0.162	0.328	0.555	0.022	0.044	0.074				
F432NAP	A → Y	(HH)	0.285	0.531	0.888	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.361	0.730	1.236	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.312	0.637	1.077	0.005	0.007	0.012	C	1.0		
		(LH)	0.258	0.467	0.778	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.335	0.633	1.076	0.005	0.007	0.012				
		(LH)	0.386	0.762	1.345	0.006	0.011	0.018				
	D → Y	(HL)	0.347	0.655	1.117	0.005	0.007	0.012				
		(LH)	0.374	0.774	1.382	0.006	0.011	0.018				
L432NB	A → Y	(HH)	0.139	0.240	0.363	0.024	0.045	0.072	A	1.0	Y	7
		(LL)	0.164	0.320	0.518	0.033	0.069	0.119	B	1.0		
	B → Y	(HH)	0.155	0.271	0.418	0.025	0.046	0.073	C	1.0		
		(LL)	0.180	0.358	0.590	0.033	0.069	0.118	D	1.0		
	C → Y	(HL)	0.120	0.227	0.369	0.039	0.069	0.119				
		(LH)	0.169	0.315	0.529	0.043	0.088	0.147				
	D → Y	(HL)	0.131	0.248	0.411	0.038	0.068	0.117				
		(LH)	0.157	0.327	0.565	0.043	0.088	0.147				

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F432NB	A → Y	(HH)	0.184	0.313	0.474	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.220	0.418	0.679	0.022	0.041	0.066	B	1.0		
	B → Y	(HH)	0.171	0.285	0.423	0.013	0.023	0.037	C	2.0		
		(LL)	0.215	0.389	0.629	0.022	0.040	0.066	D	2.0		
	C → Y	(HL)	0.152	0.273	0.436	0.025	0.040	0.066				
		(LH)	0.161	0.325	0.554	0.022	0.044	0.074				
	D → Y	(HL)	0.149	0.271	0.432	0.025	0.040	0.066				
		(LH)	0.161	0.325	0.553	0.022	0.044	0.074				
F432NBP	A → Y	(HH)	0.289	0.536	0.893	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.362	0.732	1.237	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.313	0.582	0.967	0.006	0.011	0.018	C	1.0		
		(LL)	0.378	0.767	1.298	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.336	0.635	1.082	0.005	0.007	0.012				
		(LH)	0.385	0.761	1.343	0.006	0.011	0.018				
	D → Y	(HL)	0.347	0.657	1.124	0.005	0.007	0.012				
		(LH)	0.373	0.773	1.380	0.006	0.011	0.018				
L432NC	A → Y	(HH)	0.139	0.240	0.363	0.024	0.045	0.072	A	1.0	Y	7
		(LL)	0.164	0.320	0.518	0.033	0.069	0.119	B	1.0		
	B → Y	(HH)	0.157	0.274	0.420	0.025	0.046	0.073	C	1.0		
		(LL)	0.181	0.359	0.598	0.033	0.069	0.118	D	1.0		
	C → Y	(HH)	0.230	0.440	0.731	0.043	0.088	0.147				
		(LL)	0.207	0.364	0.597	0.039	0.069	0.119				
	D → Y	(HL)	0.131	0.249	0.411	0.038	0.068	0.117				
		(LH)	0.158	0.329	0.569	0.043	0.088	0.147				
F432NC	A → Y	(HH)	0.183	0.312	0.474	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.220	0.418	0.679	0.022	0.040	0.066	B	1.0		
	B → Y	(HH)	0.171	0.285	0.423	0.013	0.023	0.037	C	1.0		
		(LL)	0.213	0.387	0.629	0.022	0.040	0.066	D	2.0		
	C → Y	(HH)	0.258	0.492	0.808	0.022	0.044	0.074				
		(LL)	0.267	0.461	0.753	0.025	0.040	0.066				
	D → Y	(HL)	0.148	0.270	0.434	0.025	0.040	0.066				
		(LH)	0.161	0.325	0.557	0.022	0.044	0.074				
F432NCP	A → Y	(HH)	0.295	0.543	0.899	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.368	0.742	1.253	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.308	0.574	0.953	0.006	0.011	0.018	C	1.0		
		(LL)	0.370	0.754	1.279	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.443	0.878	1.527	0.006	0.011	0.018				
		(LL)	0.419	0.768	1.301	0.004	0.007	0.011				
	D → Y	(HL)	0.343	0.651	1.112	0.004	0.007	0.011				
		(LH)	0.372	0.768	1.366	0.006	0.011	0.018				
L432ND	A → Y	(HH)	0.144	0.246	0.376	0.025	0.045	0.072	A	1.0	Y	7
		(LL)	0.173	0.334	0.548	0.033	0.069	0.118	B	1.0		
	B → Y	(HH)	0.152	0.267	0.412	0.025	0.046	0.073	C	1.0		
		(LL)	0.176	0.349	0.578	0.033	0.069	0.119	D	1.0		
	C → Y	(HH)	0.230	0.439	0.729	0.044	0.088	0.147				
		(LL)	0.206	0.359	0.594	0.039	0.069	0.118				
	D → Y	(HH)	0.241	0.465	0.773	0.044	0.088	0.147				
		(LL)	0.217	0.385	0.635	0.038	0.068	0.117				
F432ND	A → Y	(HH)	0.183	0.311	0.474	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.220	0.418	0.679	0.022	0.040	0.066	B	1.0		
	B → Y	(HH)	0.171	0.285	0.423	0.013	0.023	0.037	C	1.0		
		(LL)	0.213	0.387	0.628	0.022	0.040	0.066	D	1.0		
	C → Y	(HH)	0.261	0.496	0.812	0.022	0.044	0.074				
		(LL)	0.267	0.459	0.749	0.025	0.040	0.066				
	D → Y	(HH)	0.259	0.493	0.808	0.022	0.044	0.074				
		(LL)	0.264	0.454	0.741	0.025	0.040	0.066				

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F432NDP	A → Y	(HH)	0.293	0.541	0.896	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.366	0.739	1.245	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.308	0.574	0.953	0.006	0.011	0.018	C	1.0		
		(LL)	0.370	0.753	1.280	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.442	0.878	1.527	0.006	0.011	0.018				
		(LL)	0.418	0.765	1.296	0.004	0.007	0.011				
	D → Y	(HH)	0.454	0.905	1.570	0.006	0.011	0.018				
		(LL)	0.429	0.787	1.339	0.004	0.007	0.011				
L432NE	A → Y	(HH)	0.139	0.240	0.362	0.024	0.045	0.072	A	1.0	Y	7
		(LL)	0.164	0.321	0.521	0.033	0.069	0.119	B	1.0		
	B → Y	(HL)	0.113	0.229	0.359	0.033	0.069	0.119	C	1.0		
		(LH)	0.097	0.159	0.231	0.025	0.046	0.073	D	1.0		
	C → Y	(HH)	0.228	0.437	0.728	0.043	0.088	0.147				
		(LL)	0.206	0.359	0.588	0.039	0.069	0.118				
	D → Y	(HL)	0.131	0.247	0.406	0.038	0.068	0.117				
		(LH)	0.159	0.331	0.571	0.043	0.088	0.147				
F432NE	A → Y	(HH)	0.189	0.320	0.486	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.219	0.415	0.673	0.022	0.040	0.066	B	2.0		
	B → Y	(HL)	0.127	0.202	0.283	0.022	0.040	0.066	C	1.0		
		(LH)	0.076	0.126	0.175	0.013	0.023	0.037	D	2.0		
	C → Y	(HH)	0.256	0.485	0.796	0.022	0.044	0.074				
		(LL)	0.259	0.441	0.717	0.025	0.040	0.066				
	D → Y	(HL)	0.144	0.260	0.413	0.025	0.040	0.066				
		(LH)	0.163	0.329	0.557	0.022	0.044	0.074				
F432NEP	A → Y	(HH)	0.289	0.536	0.892	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.362	0.732	1.238	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.312	0.637	1.077	0.005	0.007	0.012	C	1.0		
		(LH)	0.259	0.466	0.778	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.444	0.883	1.543	0.006	0.011	0.018				
		(LL)	0.422	0.770	1.299	0.005	0.007	0.012				
	D → Y	(HL)	0.346	0.656	1.119	0.005	0.007	0.012				
		(LH)	0.375	0.777	1.385	0.006	0.011	0.018				
L432NF	A → Y	(HH)	0.145	0.247	0.377	0.025	0.045	0.072	A	1.0	Y	7
		(LL)	0.175	0.337	0.548	0.033	0.069	0.119	B	1.0		
	B → Y	(HL)	0.113	0.229	0.360	0.033	0.069	0.119	C	1.0		
		(LH)	0.097	0.159	0.231	0.025	0.046	0.073	D	1.0		
	C → Y	(HH)	0.225	0.431	0.721	0.043	0.088	0.147				
		(LL)	0.202	0.351	0.573	0.039	0.069	0.119				
	D → Y	(HH)	0.240	0.465	0.773	0.043	0.088	0.147				
		(LL)	0.218	0.383	0.633	0.038	0.068	0.117				
F432NF	A → Y	(HH)	0.184	0.314	0.478	0.013	0.023	0.037	A	1.0	Y	14
		(LL)	0.216	0.407	0.663	0.022	0.040	0.066	B	2.0		
	B → Y	(HL)	0.128	0.202	0.282	0.022	0.040	0.066	C	1.0		
		(LH)	0.075	0.123	0.174	0.013	0.023	0.037	D	1.0		
	C → Y	(HH)	0.261	0.496	0.810	0.022	0.044	0.074				
		(LL)	0.262	0.450	0.732	0.025	0.040	0.066				
	D → Y	(HH)	0.258	0.493	0.806	0.022	0.044	0.074				
		(LL)	0.260	0.445	0.725	0.025	0.040	0.066				
F432NFP	A → Y	(HH)	0.296	0.544	0.900	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.369	0.741	1.254	0.004	0.007	0.011	B	1.0		
	B → Y	(HL)	0.309	0.631	1.065	0.004	0.007	0.011	C	1.0		
		(LH)	0.258	0.464	0.772	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.436	0.870	1.517	0.006	0.011	0.018				
		(LL)	0.413	0.754	1.279	0.004	0.007	0.011				
	D → Y	(HH)	0.453	0.905	1.571	0.006	0.011	0.018				
		(LL)	0.429	0.785	1.334	0.004	0.007	0.011				

FUNCTION BLOCK

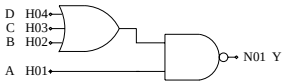
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L432NG	A → Y	(HL)	0.117	0.212	0.315	0.033	0.069	0.118	A	1.0	Y	7
		(LH)	0.081	0.133	0.186	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.112	0.222	0.354	0.033	0.069	0.118	C	1.0		
		(LH)	0.098	0.161	0.234	0.025	0.046	0.073	D	1.0		
	C → Y	(HH)	0.220	0.428	0.716	0.043	0.088	0.147				
		(LL)	0.197	0.342	0.565	0.039	0.069	0.118				
	D → Y	(HL)	0.129	0.242	0.397	0.038	0.068	0.117				
		(LH)	0.159	0.331	0.571	0.043	0.088	0.147				
F432NG	A → Y	(HL)	0.121	0.233	0.357	0.022	0.040	0.066	A	2.0	Y	14
		(LH)	0.098	0.162	0.236	0.013	0.023	0.037	B	2.0		
	B → Y	(HL)	0.130	0.203	0.284	0.022	0.040	0.066	C	1.0		
		(LH)	0.076	0.126	0.175	0.013	0.023	0.037	D	2.0		
	C → Y	(HH)	0.252	0.483	0.795	0.022	0.044	0.074				
		(LL)	0.254	0.432	0.705	0.025	0.040	0.066				
	D → Y	(HL)	0.144	0.256	0.406	0.025	0.040	0.066				
		(LH)	0.164	0.331	0.561	0.022	0.044	0.074				
F432NGP	A → Y	(HL)	0.319	0.625	1.035	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.240	0.433	0.714	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.314	0.637	1.075	0.005	0.007	0.012	C	1.0		
		(LH)	0.260	0.470	0.783	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.437	0.878	1.537	0.006	0.011	0.018				
		(LL)	0.414	0.757	1.282	0.005	0.007	0.012				
	D → Y	(HL)	0.347	0.652	1.114	0.005	0.007	0.012				
		(LH)	0.377	0.781	1.391	0.006	0.011	0.018				
L432NH	A → Y	(HL)	0.117	0.211	0.315	0.033	0.069	0.118	A	1.0	Y	7
		(LH)	0.081	0.133	0.186	0.025	0.045	0.072	B	1.0		
	B → Y	(HL)	0.111	0.222	0.354	0.033	0.069	0.118	C	1.0		
		(LH)	0.098	0.161	0.234	0.025	0.046	0.073	D	1.0		
	C → Y	(HH)	0.227	0.434	0.723	0.043	0.088	0.147				
		(LL)	0.197	0.342	0.568	0.039	0.069	0.118				
	D → Y	(HH)	0.242	0.466	0.774	0.043	0.088	0.147				
		(LL)	0.211	0.374	0.616	0.038	0.068	0.117				
F432NH	A → Y	(HL)	0.121	0.233	0.357	0.022	0.040	0.066	A	2.0	Y	14
		(LH)	0.098	0.162	0.237	0.013	0.023	0.037	B	2.0		
	B → Y	(HL)	0.130	0.202	0.284	0.022	0.040	0.066	C	1.0		
		(LH)	0.076	0.126	0.175	0.013	0.023	0.037	D	1.0		
	C → Y	(HH)	0.262	0.496	0.808	0.022	0.044	0.074				
		(LL)	0.256	0.434	0.708	0.025	0.040	0.066				
	D → Y	(HH)	0.264	0.499	0.813	0.022	0.044	0.074				
		(LL)	0.257	0.438	0.715	0.025	0.040	0.066				
F432NHP	A → Y	(HL)	0.319	0.625	1.036	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.240	0.433	0.714	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.314	0.637	1.074	0.005	0.007	0.012	C	1.0		
		(LH)	0.260	0.470	0.783	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.443	0.884	1.544	0.006	0.011	0.018				
		(LL)	0.414	0.758	1.283	0.005	0.007	0.012				
	D → Y	(HH)	0.459	0.916	1.594	0.006	0.011	0.018				
		(LL)	0.429	0.785	1.334	0.005	0.007	0.012				

[MEMO]

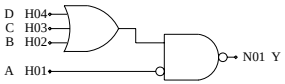
FUNCTION BLOCK

Function	1-3-INPUT OR-AND-INVERTER										SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L433	2	L433NA	3	L433NB	3	L433NC	4	L433ND	4	L433NE	3
x1	F433	4	F433NA	5	F433NB	5	F433NC	6	F433ND	6	F433NE	5
x2	F433NP	5	F433NAP	6	F433NBP	6	F433NCP	7	F433NDP	7	F433NEP	6
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power	L433NF	3	L433NG	4								
x1	F433NF	5	F433NG	6								
x2	F433NFP	6	F433NGP	7								
x4												
x8												

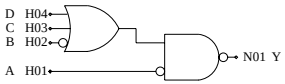
Logic Diagram for "Normal type"



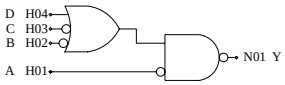
Logic Diagram for "with inv. A type"



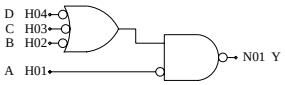
Logic Diagram for "with inv. B type"



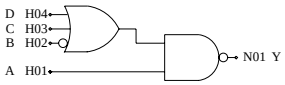
Logic Diagram for "with inv. C type"



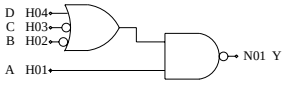
Logic Diagram for "with inv. D type"



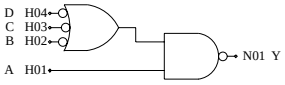
Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"



Logic Diagram for "with inv. G type"



Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L433	A → Y	(HL)	0.093	0.185	0.267	0.019	0.049	0.083	A	1.0	Y	6
		(LH)	0.083	0.132	0.187	0.025	0.046	0.073	B	1.0		
	B → Y	(HL)	0.102	0.170	0.277	0.029	0.049	0.083	C	1.0		
		(LH)	0.201	0.381	0.646	0.066	0.135	0.226	D	1.0		
	C → Y	(HL)	0.112	0.186	0.306	0.029	0.049	0.083				
		(LH)	0.210	0.436	0.756	0.066	0.135	0.226				
	D → Y	(HL)	0.124	0.199	0.327	0.024	0.044	0.077				
		(LH)	0.238	0.512	0.873	0.066	0.135	0.226				
F433	A → Y	(HL)	0.095	0.187	0.258	0.013	0.027	0.044	A	2.0	Y	13
		(LH)	0.073	0.116	0.162	0.012	0.023	0.036	B	2.1		
	B → Y	(HL)	0.106	0.183	0.284	0.016	0.026	0.044	C	2.1		
		(LH)	0.196	0.401	0.686	0.033	0.067	0.112	D	2.1		
	C → Y	(HL)	0.118	0.200	0.309	0.016	0.027	0.044				
		(LH)	0.214	0.452	0.773	0.033	0.067	0.112				
	D → Y	(HL)	0.106	0.184	0.284	0.016	0.026	0.044				
		(LH)	0.195	0.402	0.686	0.032	0.067	0.112				
F433NP	A → Y	(HL)	0.237	0.544	0.884	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.228	0.409	0.674	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.262	0.476	0.799	0.004	0.007	0.011	C	1.0		
		(LH)	0.426	0.840	1.499	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.297	0.534	0.891	0.004	0.007	0.011				
		(LH)	0.452	0.950	1.704	0.006	0.011	0.018				
	D → Y	(HL)	0.298	0.540	0.903	0.004	0.007	0.011				
		(LH)	0.450	0.968	1.738	0.006	0.011	0.018				
L433NA	A → Y	(HH)	0.123	0.216	0.334	0.025	0.045	0.072	A	1.0	Y	6
		(LL)	0.139	0.295	0.472	0.020	0.051	0.086	B	1.0		
	B → Y	(HL)	0.089	0.150	0.233	0.025	0.045	0.078	C	1.0		
		(LH)	0.163	0.299	0.502	0.065	0.133	0.224	D	1.0		
	C → Y	(HL)	0.108	0.188	0.294	0.030	0.051	0.086				
		(LH)	0.192	0.413	0.704	0.065	0.133	0.224				
	D → Y	(HL)	0.111	0.193	0.305	0.030	0.050	0.084				
		(LH)	0.190	0.427	0.740	0.065	0.133	0.224				
F433NA	A → Y	(HH)	0.158	0.260	0.387	0.013	0.023	0.037	A	1.0	Y	13
		(LL)	0.179	0.359	0.580	0.012	0.027	0.044	B	2.0		
	B → Y	(HL)	0.109	0.191	0.294	0.016	0.026	0.044	C	2.1		
		(LH)	0.191	0.395	0.677	0.033	0.067	0.113	D	2.1		
	C → Y	(HL)	0.122	0.209	0.324	0.016	0.027	0.044				
		(LH)	0.211	0.451	0.770	0.033	0.067	0.113				
	D → Y	(HL)	0.113	0.194	0.300	0.016	0.027	0.044				
		(LH)	0.195	0.400	0.687	0.033	0.067	0.113				
F433NAP	A → Y	(HH)	0.271	0.510	0.851	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.293	0.655	1.095	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.263	0.483	0.812	0.005	0.007	0.012	C	1.0		
		(LH)	0.428	0.849	1.523	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.300	0.542	0.907	0.005	0.007	0.012				
		(LH)	0.455	0.964	1.728	0.006	0.011	0.018				
	D → Y	(HL)	0.303	0.549	0.922	0.005	0.007	0.012				
		(LH)	0.453	0.977	1.762	0.006	0.011	0.018				
L433NB	A → Y	(HH)	0.127	0.220	0.336	0.025	0.045	0.072	A	1.0	Y	6
		(LL)	0.141	0.298	0.475	0.020	0.051	0.086	B	1.0		
	B → Y	(HH)	0.217	0.421	0.702	0.065	0.133	0.224	C	1.0		
		(LL)	0.165	0.280	0.456	0.025	0.045	0.078	D	1.0		
	C → Y	(HL)	0.108	0.188	0.294	0.030	0.051	0.086				
		(LH)	0.193	0.415	0.707	0.065	0.133	0.224				
	D → Y	(HL)	0.111	0.193	0.305	0.030	0.050	0.084				
		(LH)	0.192	0.429	0.742	0.065	0.133	0.224				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F433NB	A → Y	(HH)	0.160	0.265	0.394	0.013	0.023	0.037	A	1.0	Y	13
		(LL)	0.181	0.366	0.595	0.013	0.027	0.044	B	1.0		
	B → Y	(HH)	0.286	0.557	0.922	0.033	0.067	0.113	C	2.1		
		(LL)	0.218	0.370	0.603	0.016	0.026	0.044	D	2.1		
	C → Y	(HL)	0.121	0.209	0.324	0.016	0.027	0.044				
		(LH)	0.211	0.454	0.775	0.033	0.067	0.113				
	D → Y	(HL)	0.112	0.194	0.300	0.016	0.027	0.044				
		(LH)	0.195	0.404	0.688	0.033	0.067	0.113				
F433NBP	A → Y	(HH)	0.275	0.515	0.854	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.295	0.659	1.097	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.480	0.972	1.725	0.006	0.011	0.018	C	1.0		
		(LL)	0.338	0.615	1.039	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.302	0.544	0.908	0.005	0.007	0.012				
		(LH)	0.456	0.966	1.730	0.006	0.011	0.018				
	D → Y	(HL)	0.303	0.549	0.920	0.005	0.007	0.012				
		(LH)	0.454	0.979	1.765	0.006	0.011	0.018				
L433NC	A → Y	(HH)	0.131	0.226	0.340	0.025	0.046	0.074	A	1.0	Y	6
		(LL)	0.144	0.304	0.489	0.020	0.051	0.086	B	1.0		
	B → Y	(HH)	0.222	0.428	0.712	0.065	0.133	0.224	C	1.0		
		(LL)	0.169	0.285	0.464	0.025	0.045	0.078	D	1.0		
	C → Y	(HH)	0.278	0.553	0.923	0.065	0.133	0.224				
		(LL)	0.193	0.327	0.530	0.030	0.051	0.086				
	D → Y	(HL)	0.113	0.195	0.308	0.030	0.050	0.084				
		(LH)	0.194	0.438	0.753	0.065	0.133	0.224				
F433NC	A → Y	(HH)	0.163	0.269	0.396	0.013	0.023	0.037	A	1.0	Y	13
		(LL)	0.186	0.370	0.602	0.012	0.027	0.044	B	1.0		
	B → Y	(HH)	0.290	0.560	0.927	0.033	0.067	0.113	C	1.0		
		(LL)	0.215	0.366	0.598	0.016	0.026	0.044	D	2.1		
	C → Y	(HH)	0.321	0.623	1.030	0.033	0.067	0.112				
		(LL)	0.231	0.396	0.644	0.016	0.027	0.044				
	D → Y	(HL)	0.113	0.194	0.300	0.016	0.027	0.044				
		(LH)	0.196	0.403	0.691	0.033	0.067	0.113				
F433NCP	A → Y	(HH)	0.278	0.518	0.857	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.296	0.659	1.100	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.478	0.963	1.703	0.006	0.011	0.018	C	1.0		
		(LL)	0.337	0.614	1.040	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.535	1.088	1.915	0.006	0.011	0.018				
		(LL)	0.380	0.678	1.137	0.004	0.007	0.011				
	D → Y	(HL)	0.300	0.545	0.913	0.004	0.007	0.011				
		(LH)	0.451	0.972	1.745	0.006	0.011	0.018				
L433ND	A → Y	(HH)	0.131	0.226	0.340	0.025	0.046	0.074	A	1.0	Y	6
		(LL)	0.144	0.304	0.488	0.020	0.051	0.086	B	1.0		
	B → Y	(HH)	0.221	0.426	0.710	0.065	0.133	0.224	C	1.0		
		(LL)	0.167	0.282	0.459	0.025	0.045	0.078	D	1.0		
	C → Y	(HH)	0.277	0.553	0.923	0.065	0.133	0.224				
		(LL)	0.191	0.327	0.528	0.030	0.051	0.086				
	D → Y	(HH)	0.289	0.576	0.960	0.065	0.133	0.224				
		(LL)	0.193	0.328	0.532	0.030	0.050	0.084				
F433ND	A → Y	(HH)	0.160	0.265	0.393	0.013	0.023	0.037	A	1.0	Y	13
		(LL)	0.183	0.365	0.595	0.012	0.027	0.044	B	1.0		
	B → Y	(HH)	0.295	0.567	0.937	0.033	0.067	0.113	C	1.0		
		(LL)	0.218	0.375	0.613	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.322	0.625	1.032	0.033	0.067	0.113				
		(LL)	0.231	0.394	0.643	0.016	0.027	0.044				
	D → Y	(HH)	0.293	0.567	0.939	0.033	0.067	0.113				
		(LL)	0.220	0.376	0.613	0.016	0.027	0.044				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F433NDP	A → Y	(HH)	0.278	0.519	0.857	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.296	0.659	1.099	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.477	0.961	1.703	0.006	0.011	0.018	C	1.0		
		(LL)	0.337	0.612	1.035	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.534	1.088	1.915	0.006	0.011	0.018				
		(LL)	0.379	0.677	1.132	0.004	0.007	0.011				
	D → Y	(HH)	0.545	1.111	1.953	0.006	0.011	0.018				
		(LL)	0.380	0.680	1.140	0.004	0.007	0.011				
L433NE	A → Y	(HL)	0.085	0.187	0.267	0.020	0.051	0.085	A	1.0	Y	6
		(LH)	0.073	0.113	0.161	0.025	0.046	0.073	B	1.0		
	B → Y	(HH)	0.213	0.418	0.701	0.065	0.133	0.224	C	1.0		
		(LL)	0.158	0.269	0.437	0.025	0.045	0.078	D	1.0		
	C → Y	(HL)	0.109	0.187	0.290	0.031	0.051	0.086				
		(LH)	0.197	0.419	0.715	0.065	0.133	0.224				
	D → Y	(HL)	0.111	0.190	0.298	0.030	0.050	0.084				
		(LH)	0.195	0.434	0.750	0.065	0.133	0.224				
F433NE	A → Y	(HL)	0.087	0.176	0.239	0.012	0.027	0.044	A	2.0	Y	13
		(LH)	0.068	0.105	0.143	0.013	0.023	0.037	B	1.0		
	B → Y	(HH)	0.283	0.555	0.921	0.033	0.067	0.113	C	2.1		
		(LL)	0.209	0.353	0.578	0.016	0.026	0.044	D	2.1		
	C → Y	(HL)	0.120	0.200	0.304	0.016	0.027	0.044				
		(LH)	0.213	0.457	0.776	0.033	0.067	0.113				
	D → Y	(HL)	0.110	0.183	0.280	0.016	0.027	0.044				
		(LH)	0.197	0.407	0.692	0.033	0.067	0.113				
F433NEP	A → Y	(HL)	0.241	0.551	0.899	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.231	0.416	0.684	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.479	0.976	1.738	0.006	0.011	0.018	C	1.0		
		(LL)	0.331	0.604	1.023	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.304	0.543	0.905	0.005	0.007	0.012				
		(LH)	0.462	0.980	1.752	0.006	0.011	0.018				
	D → Y	(HL)	0.305	0.549	0.918	0.005	0.007	0.012				
		(LH)	0.460	0.993	1.787	0.006	0.011	0.018				
L433NF	A → Y	(HL)	0.085	0.187	0.265	0.020	0.051	0.085	A	1.0	Y	6
		(LH)	0.073	0.113	0.161	0.025	0.046	0.073	B	1.0		
	B → Y	(HH)	0.219	0.424	0.707	0.065	0.133	0.224	C	1.0		
		(LL)	0.158	0.270	0.438	0.025	0.045	0.078	D	1.0		
	C → Y	(HH)	0.279	0.552	0.918	0.065	0.133	0.224				
		(LL)	0.187	0.318	0.513	0.031	0.051	0.085				
	D → Y	(HL)	0.111	0.190	0.298	0.030	0.050	0.084				
		(LH)	0.195	0.438	0.752	0.065	0.133	0.224				
F433NF	A → Y	(HL)	0.087	0.174	0.240	0.012	0.027	0.044	A	2.0	Y	13
		(LH)	0.068	0.105	0.143	0.013	0.023	0.037	B	1.0		
	B → Y	(HH)	0.292	0.565	0.930	0.033	0.067	0.113	C	1.0		
		(LL)	0.210	0.355	0.581	0.016	0.026	0.044	D	2.1		
	C → Y	(HH)	0.321	0.627	1.031	0.033	0.067	0.113				
		(LL)	0.224	0.382	0.621	0.016	0.027	0.044				
	D → Y	(HL)	0.110	0.183	0.282	0.016	0.027	0.044				
		(LH)	0.197	0.408	0.695	0.033	0.067	0.113				
F433NFP	A → Y	(HL)	0.241	0.551	0.900	0.005	0.007	0.012	A	1.0	Y	45
		(LH)	0.232	0.417	0.685	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.484	0.982	1.744	0.006	0.011	0.018	C	1.0		
		(LL)	0.332	0.604	1.024	0.005	0.007	0.012	D	1.0		
	C → Y	(HH)	0.545	1.111	1.957	0.006	0.011	0.018				
		(LL)	0.379	0.675	1.130	0.005	0.007	0.012				
	D → Y	(HL)	0.305	0.549	0.917	0.005	0.007	0.012				
		(LH)	0.461	0.997	1.790	0.006	0.011	0.018				

FUNCTION BLOCK

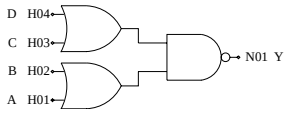
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L433NG	A → Y	(HL)	0.083	0.187	0.262	0.020	0.051	0.085	A	1.0	Y	6
		(LH)	0.073	0.115	0.156	0.025	0.046	0.074	B	1.0		
	B → Y	(HH)	0.218	0.425	0.709	0.065	0.133	0.224	C	1.0		
		(LL)	0.160	0.268	0.434	0.025	0.045	0.079	D	1.0		
	C → Y	(HH)	0.281	0.555	0.924	0.065	0.133	0.224				
		(LL)	0.188	0.320	0.520	0.030	0.051	0.086				
	D → Y	(HH)	0.290	0.578	0.963	0.065	0.133	0.224				
		(LL)	0.193	0.326	0.526	0.030	0.050	0.084				
F433NG	A → Y	(HL)	0.085	0.174	0.240	0.012	0.027	0.044	A	2.0	Y	13
		(LH)	0.067	0.105	0.145	0.013	0.023	0.037	B	1.0		
	B → Y	(HH)	0.296	0.569	0.939	0.033	0.067	0.112	C	1.0		
		(LL)	0.216	0.368	0.598	0.016	0.026	0.044	D	1.0		
	C → Y	(HH)	0.324	0.629	1.036	0.033	0.067	0.112				
		(LL)	0.226	0.385	0.626	0.016	0.027	0.044				
	D → Y	(HH)	0.298	0.574	0.946	0.033	0.067	0.112				
		(LL)	0.214	0.362	0.591	0.016	0.027	0.044				
F433NGP	A → Y	(HL)	0.237	0.543	0.883	0.004	0.007	0.011	A	1.0	Y	46
		(LH)	0.228	0.408	0.673	0.006	0.011	0.018	B	1.0		
	B → Y	(HH)	0.475	0.960	1.698	0.006	0.011	0.018	C	1.0		
		(LL)	0.328	0.597	1.009	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.537	1.090	1.914	0.006	0.011	0.018				
		(LL)	0.375	0.670	1.120	0.004	0.007	0.011				
	D → Y	(HH)	0.546	1.112	1.953	0.006	0.011	0.018				
		(LL)	0.379	0.676	1.135	0.004	0.007	0.011				

[MEMO]

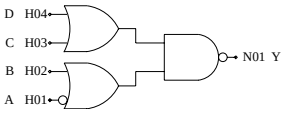
FUNCTION BLOCK

Function	2-2-INPUT OR-AND-INVERTER										SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L434	2	L434NA	3	L434NB	3	L434NC	4	L434ND	3	L434NE	4
x1	F434	4	F434NA	5	F434NB	5	F434NC	6	F434ND	5	F434NE	6
x2	F434NP	5	F434NAP	6	F434NBP	6	F434NCP	7	F434NDP	6	F434NEP	7
x4												
x8												
Block type	with inv. F		with inv. G		with inv. H							
Drivability	Name	cells	Name	cells	Name	cells						
Low Power												
x1												
x2												
x4												
x8												

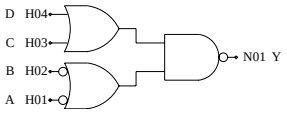
Logic Diagram for "Normal type"



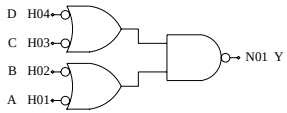
Logic Diagram for "with inv. A type"



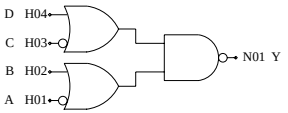
Logic Diagram for "with inv. B type"



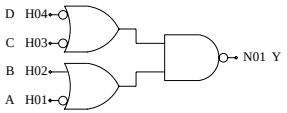
Logic Diagram for "with inv. C type"



Logic Diagram for "with inv. D type"



Logic Diagram for "with inv. E type"



Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L434	A → Y	(HL)	0.115	0.204	0.299	0.024	0.049	0.083	A	1.0	Y	4
		(LH)	0.130	0.229	0.352	0.043	0.088	0.147	B	1.0		
	B → Y	(HL)	0.127	0.222	0.329	0.024	0.049	0.083	C	1.0		
		(LH)	0.116	0.233	0.388	0.043	0.088	0.147	D	1.0		
	C → Y	(HL)	0.113	0.210	0.340	0.022	0.049	0.083				
		(LH)	0.176	0.356	0.598	0.043	0.088	0.147				
	D → Y	(HL)	0.120	0.229	0.375	0.022	0.049	0.083				
		(LH)	0.165	0.365	0.638	0.043	0.088	0.147				
F434	A → Y	(HL)	0.115	0.194	0.279	0.012	0.024	0.041	A	2.1	Y	8
		(LH)	0.117	0.217	0.351	0.022	0.044	0.074	B	2.1		
	B → Y	(HL)	0.116	0.195	0.280	0.012	0.024	0.041	C	2.1		
		(LH)	0.117	0.217	0.352	0.022	0.044	0.074	D	2.1		
	C → Y	(HL)	0.118	0.220	0.343	0.011	0.024	0.041				
		(LH)	0.175	0.374	0.636	0.022	0.044	0.074				
	D → Y	(HL)	0.118	0.220	0.343	0.011	0.024	0.041				
		(LH)	0.175	0.374	0.636	0.022	0.044	0.074				
F434NP	A → Y	(HL)	0.279	0.544	0.880	0.004	0.007	0.011	A	1.0	Y	45
		(LH)	0.313	0.603	1.060	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.292	0.564	0.917	0.004	0.007	0.011	C	1.0		
		(LH)	0.300	0.614	1.097	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.276	0.576	0.948	0.004	0.007	0.011				
		(LH)	0.390	0.782	1.377	0.006	0.011	0.018				
	D → Y	(HL)	0.277	0.590	0.976	0.004	0.007	0.011				
		(LH)	0.377	0.792	1.414	0.006	0.011	0.018				
L434NA	A → Y	(HH)	0.160	0.300	0.476	0.044	0.088	0.147	A	1.0	Y	4
		(LL)	0.160	0.304	0.487	0.025	0.050	0.084	B	1.0		
	B → Y	(HL)	0.118	0.209	0.303	0.025	0.050	0.084	C	1.0		
		(LH)	0.099	0.206	0.335	0.044	0.088	0.147	D	1.0		
	C → Y	(HL)	0.113	0.215	0.335	0.023	0.051	0.085				
		(LH)	0.169	0.343	0.577	0.043	0.088	0.147				
	D → Y	(HL)	0.119	0.230	0.363	0.022	0.050	0.084				
		(LH)	0.156	0.354	0.614	0.043	0.088	0.147				
F434NA	A → Y	(HH)	0.202	0.366	0.580	0.022	0.044	0.074	A	1.0	Y	8
		(LL)	0.205	0.376	0.612	0.013	0.026	0.044	B	2.0		
	B → Y	(HL)	0.123	0.203	0.290	0.014	0.027	0.045	C	2.0		
		(LH)	0.114	0.212	0.342	0.022	0.044	0.074	D	2.0		
	C → Y	(HL)	0.114	0.215	0.337	0.012	0.027	0.044				
		(LH)	0.162	0.345	0.590	0.022	0.044	0.074				
	D → Y	(HL)	0.116	0.217	0.339	0.012	0.027	0.045				
		(LH)	0.163	0.346	0.591	0.022	0.044	0.074				
F434NAP	A → Y	(HH)	0.360	0.718	1.251	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.334	0.660	1.106	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.293	0.566	0.920	0.005	0.007	0.012	C	1.0		
		(LH)	0.300	0.615	1.100	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.277	0.575	0.949	0.005	0.007	0.012				
		(LH)	0.387	0.779	1.379	0.006	0.011	0.018				
	D → Y	(HL)	0.279	0.588	0.975	0.005	0.007	0.012				
		(LH)	0.374	0.790	1.415	0.006	0.011	0.018				
L434NB	A → Y	(HH)	0.170	0.314	0.490	0.044	0.088	0.147	A	1.0	Y	4
		(LL)	0.166	0.313	0.501	0.025	0.050	0.084	B	1.0		
	B → Y	(HH)	0.177	0.333	0.529	0.044	0.088	0.147	C	1.0		
		(LL)	0.169	0.321	0.517	0.025	0.050	0.084	D	1.0		
	C → Y	(HL)	0.112	0.222	0.346	0.023	0.051	0.085				
		(LH)	0.168	0.342	0.575	0.043	0.088	0.147				
	D → Y	(HL)	0.118	0.237	0.374	0.022	0.050	0.084				
		(LH)	0.156	0.353	0.612	0.043	0.088	0.147				

FUNCTION BLOCK

Block type	Path		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F434NB	A → Y	(HH)	0.210	0.377	0.591	0.022	0.044	0.074	A	1.0	Y	8
		(LL)	0.207	0.379	0.619	0.013	0.026	0.044	B	1.0		
	B → Y	(HH)	0.215	0.384	0.601	0.022	0.044	0.074	C	2.0		
		(LL)	0.216	0.395	0.641	0.014	0.027	0.045	D	2.0		
	C → Y	(HL)	0.113	0.227	0.357	0.012	0.027	0.044				
		(LH)	0.161	0.343	0.587	0.022	0.044	0.074				
	D → Y	(HL)	0.115	0.230	0.361	0.012	0.027	0.045				
		(LH)	0.161	0.343	0.588	0.022	0.044	0.074				
F434NBP	A → Y	(HH)	0.366	0.725	1.259	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.336	0.663	1.109	0.005	0.007	0.012	B	1.0		
	B → Y	(HH)	0.374	0.747	1.300	0.006	0.011	0.018	C	1.0		
		(LL)	0.339	0.673	1.127	0.005	0.007	0.012	D	1.0		
	C → Y	(HL)	0.275	0.581	0.958	0.005	0.007	0.012				
		(LH)	0.387	0.779	1.379	0.006	0.011	0.018				
	D → Y	(HL)	0.277	0.595	0.984	0.005	0.007	0.012				
		(LH)	0.373	0.789	1.415	0.006	0.011	0.018				
L434NC	A → Y	(HH)	0.166	0.309	0.485	0.044	0.088	0.147	A	1.0	Y	4
		(LL)	0.162	0.305	0.489	0.025	0.050	0.084	B	1.0		
	B → Y	(HH)	0.184	0.342	0.542	0.044	0.088	0.147	C	1.0		
		(LL)	0.177	0.337	0.541	0.025	0.050	0.084	D	1.0		
	C → Y	(HH)	0.228	0.466	0.777	0.044	0.088	0.147				
		(LL)	0.185	0.352	0.571	0.023	0.051	0.085				
	D → Y	(HH)	0.239	0.492	0.819	0.044	0.088	0.147				
		(LL)	0.191	0.367	0.599	0.022	0.050	0.084				
F434NC	A → Y	(HH)	0.210	0.377	0.589	0.022	0.044	0.074	A	1.0	Y	8
		(LL)	0.208	0.379	0.619	0.013	0.026	0.044	B	1.0		
	B → Y	(HH)	0.215	0.384	0.597	0.022	0.044	0.074	C	1.0		
		(LL)	0.216	0.394	0.640	0.014	0.027	0.045	D	1.0		
	C → Y	(HH)	0.258	0.512	0.844	0.022	0.044	0.074				
		(LL)	0.218	0.409	0.675	0.012	0.027	0.044				
	D → Y	(HH)	0.260	0.515	0.848	0.022	0.044	0.074				
		(LL)	0.222	0.414	0.679	0.012	0.027	0.045				
F434NCP	A → Y	(HH)	0.363	0.721	1.252	0.006	0.011	0.018	A	1.0	Y	46
		(LL)	0.332	0.656	1.099	0.004	0.007	0.011	B	1.0		
	B → Y	(HH)	0.380	0.756	1.309	0.006	0.011	0.018	C	1.0		
		(LL)	0.347	0.687	1.148	0.004	0.007	0.011	D	1.0		
	C → Y	(HH)	0.447	0.904	1.580	0.006	0.011	0.018				
		(LL)	0.357	0.707	1.182	0.004	0.007	0.011				
	D → Y	(HH)	0.458	0.931	1.626	0.006	0.011	0.018				
		(LL)	0.360	0.719	1.207	0.004	0.007	0.011				
L434ND	A → Y	(HH)	0.165	0.305	0.483	0.044	0.088	0.147	A	1.0	Y	4
		(LL)	0.162	0.305	0.489	0.025	0.050	0.084	B	1.0		
	B → Y	(HL)	0.119	0.208	0.303	0.025	0.050	0.084	C	1.0		
		(LH)	0.100	0.206	0.335	0.044	0.088	0.147	D	1.0		
	C → Y	(HH)	0.225	0.466	0.774	0.044	0.088	0.147				
		(LL)	0.184	0.344	0.559	0.023	0.051	0.085				
	D → Y	(HL)	0.119	0.230	0.362	0.022	0.050	0.084				
		(LH)	0.158	0.355	0.617	0.043	0.088	0.147				
F434ND	A → Y	(HH)	0.206	0.371	0.585	0.022	0.044	0.074	A	1.0	Y	8
		(LL)	0.207	0.380	0.620	0.013	0.026	0.044	B	2.0		
	B → Y	(HL)	0.123	0.203	0.289	0.014	0.027	0.045	C	1.0		
		(LH)	0.114	0.212	0.343	0.022	0.044	0.074	D	2.0		
	C → Y	(HH)	0.254	0.508	0.841	0.022	0.044	0.074				
		(LL)	0.219	0.395	0.655	0.012	0.027	0.044				
	D → Y	(HL)	0.116	0.217	0.340	0.012	0.027	0.045				
		(LH)	0.164	0.347	0.594	0.022	0.044	0.074				

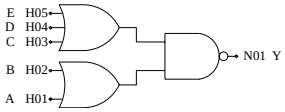
FUNCTION BLOCK

Block type	Path		Switching speed t LD0 (ns) MIN.	TYP.	MAX.	t 1 MIN.	TYP.	MAX.	Input Symbol	Fanin	Output Symbol	Fanout
F434NDP	A → Y	(HH)	0.364	0.724	1.260	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.333	0.659	1.101	0.005	0.007	0.012	B	1.0		
	B → Y	(HL)	0.293	0.567	0.919	0.005	0.007	0.012	C	1.0		
		(LH)	0.302	0.621	1.110	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.446	0.905	1.586	0.006	0.011	0.018				
		(LL)	0.356	0.701	1.176	0.005	0.007	0.012				
	D → Y	(HL)	0.281	0.592	0.977	0.005	0.007	0.012				
		(LH)	0.378	0.798	1.428	0.006	0.011	0.018				
L434NE	A → Y	(HH)	0.165	0.304	0.482	0.044	0.088	0.147	A	1.0	Y	4
		(LL)	0.162	0.305	0.489	0.025	0.050	0.084	B	1.0		
	B → Y	(HL)	0.119	0.208	0.302	0.025	0.050	0.084	C	1.0		
		(LH)	0.100	0.206	0.335	0.044	0.088	0.147	D	1.0		
	C → Y	(HH)	0.227	0.464	0.776	0.044	0.088	0.147				
		(LL)	0.186	0.345	0.562	0.023	0.051	0.085				
	D → Y	(HH)	0.237	0.491	0.820	0.044	0.088	0.147				
		(LL)	0.192	0.363	0.592	0.022	0.050	0.084				
F434NE	A → Y	(HH)	0.206	0.371	0.586	0.022	0.044	0.074	A	1.0	Y	8
		(LL)	0.207	0.379	0.619	0.013	0.026	0.044	B	2.0		
	B → Y	(HL)	0.123	0.202	0.289	0.014	0.027	0.045	C	1.0		
		(LH)	0.114	0.213	0.342	0.022	0.044	0.074	D	1.0		
	C → Y	(HH)	0.257	0.512	0.847	0.022	0.044	0.074				
		(LL)	0.220	0.399	0.657	0.012	0.027	0.044				
	D → Y	(HH)	0.259	0.514	0.850	0.022	0.044	0.074				
		(LL)	0.222	0.404	0.663	0.012	0.027	0.045				
F434NEP	A → Y	(HH)	0.362	0.719	1.250	0.006	0.011	0.018	A	1.0	Y	45
		(LL)	0.332	0.656	1.096	0.004	0.007	0.011	B	1.0		
	B → Y	(HL)	0.292	0.565	0.916	0.004	0.007	0.011	C	1.0		
		(LH)	0.301	0.617	1.100	0.006	0.011	0.018	D	1.0		
	C → Y	(HH)	0.447	0.903	1.579	0.006	0.011	0.018				
		(LL)	0.357	0.701	1.175	0.004	0.007	0.011				
	D → Y	(HH)	0.457	0.930	1.624	0.006	0.011	0.018				
		(LL)	0.360	0.714	1.199	0.004	0.007	0.011				

FUNCTION BLOCK

Function	2-3-INPUT OR-AND-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L435	3												
x1	F435	5												
x2	F435NP	6												
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

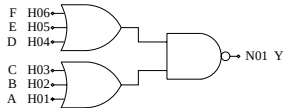
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L435	A → Y	(HL)	0.109	0.228	0.332	0.021	0.049	0.083		A	1.0	Y	2
		(LH)	0.130	0.226	0.354	0.043	0.088	0.147		B	1.0		
	B → Y	(HL)	0.120	0.245	0.366	0.021	0.049	0.083		C	1.0		
		(LH)	0.116	0.236	0.384	0.043	0.088	0.147		D	1.0		
	C → Y	(HL)	0.124	0.238	0.369	0.022	0.049	0.083		E	1.0		
		(LH)	0.264	0.563	0.971	0.065	0.134	0.225					
	D → Y	(HL)	0.132	0.260	0.407	0.022	0.049	0.083					
		(LH)	0.274	0.620	1.087	0.065	0.134	0.225					
	E → Y	(HL)	0.143	0.283	0.445	0.022	0.049	0.083					
		(LH)	0.293	0.682	1.186	0.066	0.134	0.225					
F435	A → Y	(HL)	0.104	0.197	0.279	0.011	0.024	0.042		A	2.1	Y	6
		(LH)	0.109	0.202	0.326	0.022	0.044	0.074		B	2.1		
	B → Y	(HL)	0.106	0.197	0.281	0.011	0.025	0.042		C	2.1		
		(LH)	0.110	0.203	0.325	0.022	0.044	0.074		D	2.1		
	C → Y	(HL)	0.127	0.233	0.362	0.011	0.025	0.042		E	2.1		
		(LH)	0.253	0.576	1.005	0.033	0.067	0.112					
	D → Y	(HL)	0.137	0.250	0.387	0.011	0.025	0.042					
		(LH)	0.271	0.628	1.092	0.033	0.067	0.112					
	E → Y	(HL)	0.128	0.234	0.360	0.011	0.025	0.042					
		(LH)	0.253	0.576	1.007	0.032	0.067	0.112					
F435NP	A → Y	(HL)	0.283	0.610	0.996	0.005	0.007	0.012		A	1.0	Y	46
		(LH)	0.345	0.675	1.192	0.006	0.011	0.018		B	1.0		
	B → Y	(HL)	0.295	0.634	1.031	0.005	0.007	0.012		C	1.0		
		(LH)	0.333	0.688	1.229	0.006	0.011	0.018		D	1.0		
	C → Y	(HL)	0.299	0.615	1.014	0.005	0.007	0.012		E	1.0		
		(LH)	0.544	1.148	2.085	0.006	0.011	0.018					
	D → Y	(HL)	0.311	0.638	1.055	0.005	0.007	0.012					
		(LH)	0.553	1.199	2.195	0.006	0.011	0.018					
	E → Y	(HL)	0.316	0.660	1.091	0.005	0.007	0.012					
		(LH)	0.573	1.268	2.297	0.006	0.011	0.018					

FUNCTION BLOCK

Function	3-3-INPUT OR-AND-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L436	3												
x1	F436	6												
x2	F436NP	6												
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

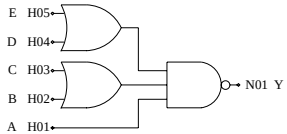
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L436	A → Y	(HL)	0.105	0.235	0.350	0.020	0.050	0.084	A	1.0	Y	1
		(LH)	0.160	0.298	0.488	0.065	0.134	0.224	B	1.0		
	B → Y	(HL)	0.130	0.270	0.413	0.022	0.050	0.084	C	1.0		
		(LH)	0.194	0.413	0.696	0.065	0.134	0.224	D	1.0		
	C → Y	(HL)	0.135	0.281	0.436	0.022	0.050	0.084	E	1.0		
		(LH)	0.191	0.426	0.733	0.065	0.134	0.224	F	1.0		
	D → Y	(HL)	0.122	0.253	0.413	0.018	0.050	0.084				
		(LH)	0.250	0.601	1.051	0.065	0.133	0.224				
	E → Y	(HL)	0.137	0.293	0.476	0.020	0.050	0.084				
		(LH)	0.284	0.717	1.265	0.065	0.133	0.224				
	F → Y	(HL)	0.140	0.306	0.499	0.020	0.050	0.084				
		(LH)	0.282	0.730	1.300	0.065	0.133	0.224				
F436	A → Y	(HL)	0.117	0.230	0.340	0.011	0.026	0.043	A	2.1	Y	2
		(LH)	0.159	0.322	0.530	0.033	0.067	0.113	B	2.1		
	B → Y	(HL)	0.127	0.248	0.366	0.012	0.026	0.043	C	2.1		
		(LH)	0.178	0.376	0.621	0.033	0.067	0.113	D	2.1		
	C → Y	(HL)	0.119	0.233	0.343	0.012	0.026	0.043	E	2.1		
		(LH)	0.159	0.320	0.528	0.033	0.067	0.113	F	2.1		
	D → Y	(HL)	0.140	0.286	0.444	0.010	0.026	0.043				
		(LH)	0.285	0.706	1.243	0.033	0.067	0.113				
	E → Y	(HL)	0.149	0.305	0.470	0.011	0.026	0.044				
		(LH)	0.304	0.759	1.331	0.033	0.067	0.113				
	F → Y	(HL)	0.143	0.292	0.450	0.011	0.026	0.044				
		(LH)	0.286	0.706	1.244	0.033	0.067	0.113				
F436NP	A → Y	(HL)	0.267	0.612	0.995	0.005	0.007	0.012	A	1.0	Y	46
		(LH)	0.426	0.870	1.565	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.304	0.655	1.069	0.005	0.007	0.012	C	1.0		
		(LH)	0.459	0.990	1.778	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.311	0.669	1.096	0.005	0.007	0.012	E	1.0		
		(LH)	0.456	1.003	1.814	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.277	0.656	1.070	0.005	0.007	0.012				
		(LH)	0.527	1.194	2.189	0.006	0.011	0.018				
	E → Y	(HL)	0.303	0.695	1.145	0.004	0.007	0.012				
		(LH)	0.557	1.311	2.394	0.006	0.011	0.018				
	F → Y	(HL)	0.298	0.700	1.157	0.005	0.007	0.012				
		(LH)	0.555	1.325	2.428	0.006	0.011	0.018				

FUNCTION BLOCK

Function	1-2-2-INPUT OR-AND-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L437	3												
x1	F437	5												
x2	F437NP	6												
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

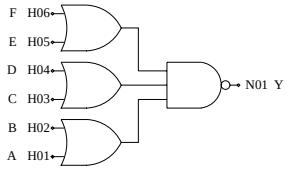
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L437	A → Y	(HL)	0.107	0.278	0.429	0.026	0.068	0.117		A	1.0	Y	6
		(LH)	0.085	0.137	0.184	0.025	0.045	0.073		B	1.0		
	B → Y	(HL)	0.116	0.296	0.467	0.033	0.073	0.123		C	1.0		
		(LH)	0.165	0.304	0.491	0.046	0.091	0.151		D	1.0		
	C → Y	(HL)	0.150	0.337	0.537	0.032	0.068	0.117		E	1.0		
		(LH)	0.173	0.359	0.591	0.046	0.091	0.151					
	D → Y	(HL)	0.145	0.328	0.530	0.032	0.069	0.119					
		(LH)	0.224	0.443	0.742	0.046	0.091	0.151					
	E → Y	(HL)	0.164	0.373	0.606	0.033	0.068	0.117					
		(LH)	0.230	0.493	0.831	0.046	0.091	0.151					
F437	A → Y	(HL)	0.131	0.243	0.357	0.018	0.039	0.064		A	2.0	Y	13
		(LH)	0.090	0.144	0.205	0.013	0.023	0.037		B	2.0		
	B → Y	(HL)	0.147	0.292	0.457	0.020	0.039	0.064		C	2.0		
		(LH)	0.160	0.314	0.524	0.022	0.044	0.074		D	2.0		
	C → Y	(HL)	0.147	0.292	0.458	0.020	0.039	0.064		E	2.0		
		(LH)	0.160	0.314	0.523	0.022	0.044	0.074					
	D → Y	(HL)	0.166	0.328	0.523	0.020	0.038	0.064					
		(LH)	0.202	0.438	0.746	0.022	0.044	0.074					
	E → Y	(HL)	0.169	0.331	0.525	0.020	0.039	0.064					
		(LH)	0.203	0.438	0.747	0.022	0.044	0.074					
F437NP	A → Y	(HL)	0.279	0.691	1.146	0.005	0.007	0.012		A	1.0	Y	46
		(LH)	0.239	0.439	0.732	0.006	0.011	0.018		B	1.0		
	B → Y	(HL)	0.312	0.717	1.190	0.005	0.007	0.012		C	1.0		
		(LH)	0.379	0.754	1.307	0.006	0.011	0.018		D	1.0		
	C → Y	(HL)	0.347	0.745	1.250	0.005	0.007	0.012		E	1.0		
		(LH)	0.385	0.806	1.407	0.006	0.011	0.018					
	D → Y	(HL)	0.329	0.744	1.244	0.005	0.007	0.012					
		(LH)	0.459	0.908	1.575	0.006	0.011	0.018					
	E → Y	(HL)	0.362	0.786	1.321	0.005	0.007	0.012					
		(LH)	0.462	0.959	1.666	0.006	0.011	0.018					

FUNCTION BLOCK

Function	2-2-2-INPUT OR-AND-INVERTER												SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power	L438	3												
x1	F438	6												
x2	F438NP	6												
x4														
x8														
Block type	with inv. F		with inv. G		with inv. H									
Drivability	Name	cells	Name	cells	Name	cells								
Low Power														
x1														
x2														
x4														
x8														

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

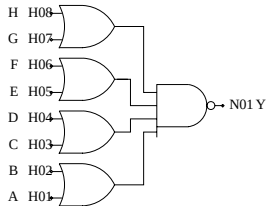
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L438	A → Y	(HL)	0.132	0.286	0.434	0.033	0.076	0.127	A	1.0	Y	3
		(LH)	0.125	0.227	0.347	0.044	0.088	0.147	B	1.0		
	B → Y	(HL)	0.144	0.316	0.486	0.033	0.076	0.127	C	1.0		
		(LH)	0.112	0.236	0.385	0.044	0.088	0.147	D	1.0		
	C → Y	(HL)	0.153	0.355	0.563	0.031	0.073	0.123	E	1.0		
		(LH)	0.191	0.389	0.654	0.044	0.089	0.148	F	1.0		
	D → Y	(HL)	0.178	0.404	0.634	0.034	0.077	0.127				
		(LH)	0.181	0.401	0.692	0.044	0.089	0.148				
	E → Y	(HL)	0.165	0.412	0.658	0.032	0.078	0.129				
		(LH)	0.238	0.532	0.915	0.043	0.088	0.147				
	F → Y	(HL)	0.173	0.437	0.702	0.030	0.077	0.127				
		(LH)	0.225	0.544	0.950	0.044	0.088	0.147				
F438	A → Y	(HL)	0.143	0.270	0.413	0.016	0.037	0.062	A	2.0	Y	5
		(LH)	0.133	0.250	0.406	0.022	0.044	0.074	B	2.0		
	B → Y	(HL)	0.143	0.271	0.413	0.016	0.037	0.062	C	2.0		
		(LH)	0.131	0.250	0.406	0.022	0.044	0.074	D	2.0		
	C → Y	(HL)	0.166	0.357	0.562	0.016	0.037	0.062	E	2.0		
		(LH)	0.194	0.421	0.717	0.022	0.044	0.074	F	2.0		
	D → Y	(HL)	0.166	0.357	0.562	0.016	0.037	0.062				
		(LH)	0.194	0.421	0.717	0.022	0.044	0.074				
	E → Y	(HL)	0.171	0.385	0.619	0.015	0.037	0.062				
		(LH)	0.238	0.558	0.966	0.022	0.044	0.074				
	F → Y	(HL)	0.174	0.389	0.624	0.016	0.037	0.062				
		(LH)	0.238	0.560	0.965	0.022	0.044	0.074				
F438NP	A → Y	(HL)	0.333	0.731	1.191	0.005	0.007	0.012	A	1.0	Y	46
		(LH)	0.329	0.658	1.156	0.006	0.011	0.018	B	1.0		
	B → Y	(HL)	0.350	0.766	1.248	0.004	0.007	0.012	C	1.0		
		(LH)	0.317	0.668	1.191	0.006	0.011	0.018	D	1.0		
	C → Y	(HL)	0.347	0.792	1.308	0.004	0.007	0.012	E	1.0		
		(LH)	0.419	0.835	1.475	0.006	0.011	0.018	F	1.0		
	D → Y	(HL)	0.386	0.853	1.398	0.005	0.007	0.012				
		(LH)	0.407	0.849	1.518	0.006	0.011	0.018				
	E → Y	(HL)	0.362	0.865	1.420	0.005	0.007	0.012				
		(LH)	0.476	1.007	1.780	0.006	0.011	0.018				
	F → Y	(HL)	0.368	0.889	1.464	0.004	0.007	0.012				
		(LH)	0.464	1.019	1.815	0.006	0.011	0.018				

FUNCTION BLOCK

Function	2-2-2-2-INPUT OR-AND-INVERTER											SSI Family	
Block type	Normal		with inv. A		with inv. B		with inv. C		with inv. D		with inv. E		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power	L454	5											
x1	F454	8											
x2													
x4													
x8													
Block type	with inv. F		with inv. G		with inv. H								
Drivability	Name	cells	Name	cells	Name	cells							
Low Power													
x1													
x2													
x4													
x8													

Logic Diagram for "Normal type"



Logic Diagram for "with inv. A type"

Logic Diagram for "with inv. B type"

Logic Diagram for "with inv. C type"

Logic Diagram for "with inv. D type"

Logic Diagram for "with inv. E type"

Logic Diagram for "with inv. F type"

Logic Diagram for "with inv. G type"

Logic Diagram for "with inv. H type"

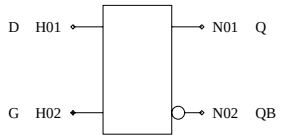
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L454	A → Y	(HL)	0.171	0.444	0.721	0.039	0.095	0.159	A	1.0	Y	1
		(LH)	0.164	0.306	0.495	0.044	0.088	0.147	B	1.0		
	B → Y	(HL)	0.186	0.483	0.787	0.039	0.095	0.159	C	1.0		
		(LH)	0.152	0.316	0.527	0.044	0.088	0.147	D	1.0		
	C → Y	(HL)	0.194	0.531	0.881	0.038	0.095	0.159	E	1.0		
		(LH)	0.219	0.441	0.741	0.043	0.088	0.147	F	1.0		
	D → Y	(HL)	0.210	0.571	0.952	0.038	0.095	0.159	G	1.0		
		(LH)	0.208	0.452	0.779	0.043	0.088	0.147	H	1.0		
	E → Y	(HL)	0.223	0.623	1.031	0.038	0.096	0.160				
		(LH)	0.273	0.592	1.027	0.043	0.088	0.147				
	F → Y	(HL)	0.233	0.655	1.089	0.037	0.095	0.159				
		(LH)	0.261	0.604	1.057	0.043	0.088	0.147				
	G → Y	(HL)	0.241	0.657	1.099	0.037	0.095	0.159				
		(LH)	0.319	0.738	1.280	0.044	0.089	0.148				
	H → Y	(HL)	0.256	0.698	1.168	0.037	0.095	0.159				
		(LH)	0.309	0.753	1.322	0.044	0.089	0.148				
F454	A → Y	(HL)	0.168	0.368	0.585	0.020	0.049	0.082	A	2.1	Y	3
		(LH)	0.150	0.291	0.468	0.022	0.044	0.074	B	2.1		
	B → Y	(HL)	0.168	0.367	0.585	0.020	0.049	0.082	C	2.1		
		(LH)	0.150	0.290	0.468	0.022	0.044	0.074	D	2.1		
	C → Y	(HL)	0.204	0.489	0.790	0.020	0.049	0.082	E	2.1		
		(LH)	0.210	0.450	0.765	0.022	0.044	0.074	F	2.1		
	D → Y	(HL)	0.204	0.489	0.790	0.020	0.049	0.082	G	2.1		
		(LH)	0.210	0.450	0.765	0.022	0.044	0.074	H	2.1		
	E → Y	(HL)	0.242	0.591	0.950	0.020	0.049	0.082				
		(LH)	0.266	0.616	1.058	0.022	0.045	0.074				
	F → Y	(HL)	0.242	0.591	0.950	0.020	0.049	0.082				
		(LH)	0.266	0.616	1.058	0.022	0.045	0.074				
	G → Y	(HL)	0.257	0.632	1.023	0.019	0.049	0.081				
		(LH)	0.305	0.758	1.317	0.022	0.045	0.075				
	H → Y	(HL)	0.262	0.637	1.030	0.020	0.049	0.082				
		(LH)	0.305	0.757	1.320	0.022	0.045	0.075				

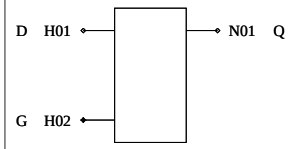
FUNCTION BLOCK

Function	D-LATCH							SSI Family				
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L601	3		
x1	F601	6	F601NQ	5	F601NB	5						
x2	F601NP	8	F601NQP	6	F601NBP	6						
x4												

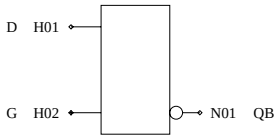
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	G	Q	QB
0	1	0	1
1	1	1	0
X	0	Latch	

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F601	D → Q	(HH)	0.435	0.776	1.298	0.012	0.023	0.036	D	1.0	Q	22
		(LL)	0.448	0.843	1.493	0.009	0.015	0.024	G	1.0	QB	23
	D → QB	(HL)	0.339	0.599	0.995	0.010	0.015	0.025				
		(LH)	0.331	0.602	1.056	0.012	0.023	0.036				
	G → Q	(HH)	0.497	0.919	1.547	0.012	0.023	0.036				
		(HL)	0.467	0.883	1.522	0.009	0.015	0.024				
	G → QB	(HH)	0.351	0.643	1.085	0.012	0.023	0.036				
		(HL)	0.401	0.742	1.245	0.009	0.015	0.024				
	Set up time	D	0.511		0.836							
	Hold time	D	0.114		0.010							
	Min Pulse	G	1.021		2.131							
F601NP	D → Q	(HH)	0.318	0.531	0.852	0.006	0.012	0.019	D	1.0	Q	45
		(LL)	0.336	0.649	1.237	0.005	0.008	0.014	G	1.0	QB	45
	D → QB	(HL)	0.517	0.927	1.560	0.005	0.007	0.012				
		(LH)	0.507	0.981	1.826	0.006	0.011	0.018				
	G → Q	(HH)	0.376	0.670	1.087	0.006	0.012	0.019				
		(HL)	0.351	0.707	1.344	0.005	0.008	0.014				
	G → QB	(HH)	0.522	1.039	1.935	0.006	0.011	0.018				
		(HL)	0.575	1.066	1.796	0.005	0.007	0.012				
	Set up time	D	0.540		1.470							
	Hold time	D	0.260		0.040							
	Min Pulse	G	1.000		2.345							
L601	D → Q	(HH)	0.167	0.315	0.535	0.024	0.045	0.072	D	3.1	Q	10
		(LL)	0.189	0.321	0.539	0.016	0.026	0.043	G	1.0		
	G → Q	(HH)	0.279	0.500	0.810	0.024	0.045	0.073				
		(HL)	0.319	0.581	0.974	0.016	0.026	0.043				
	Set up time	D	0.482		0.653							
	Hold time	D	0.388		0.400							
	Min Pulse	G	1.028		2.083							
F601NQ	D → Q	(HH)	0.256	0.428	0.678	0.013	0.023	0.037	D	1.0	Q	22
		(LL)	0.281	0.533	0.992	0.009	0.016	0.025	G	1.0		
	G → Q	(HH)	0.318	0.570	0.924	0.013	0.023	0.037				
		(HL)	0.301	0.597	1.086	0.009	0.015	0.025				
	Set up time	D	0.410		0.950							
	Hold time	D	0.320		0.180							
	Min Pulse	G	0.743		1.339							
F601NQP	D → Q	(HH)	0.316	0.528	0.845	0.006	0.012	0.019	D	1.0	Q	44
		(LL)	0.335	0.649	1.235	0.005	0.008	0.014	G	1.0		
	G → Q	(HH)	0.374	0.666	1.082	0.006	0.012	0.019				
		(HL)	0.350	0.707	1.342	0.005	0.008	0.014				
	Set up time	D	0.470		1.210							
	Hold time	D	0.260		0.050							
	Min Pulse	G	0.794		1.560							
F601NB	D → QB	(HL)	0.316	0.572	0.951	0.009	0.014	0.023	D	1.0	QB	23
		(LH)	0.313	0.572	1.002	0.012	0.023	0.037	G	1.0		
	G → QB	(HH)	0.336	0.616	1.033	0.012	0.023	0.037				
		(HL)	0.382	0.717	1.204	0.009	0.014	0.023				
	Set up time	D	0.370		0.780							
	Hold time	D	0.330		0.160							
	Min Pulse	G	0.806		1.525							
F601NBP	D → QB	(HL)	0.370	0.672	1.129	0.005	0.008	0.012	D	1.0	QB	44
		(LH)	0.356	0.645	1.123	0.006	0.011	0.018	G	1.0		
	G → QB	(HH)	0.376	0.687	1.152	0.006	0.011	0.018				
		(HL)	0.434	0.818	1.384	0.005	0.007	0.012				
	Set up time	D	0.400		0.830							
	Hold time	D	0.290		0.050							

FUNCTION BLOCK

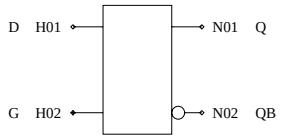
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Min Pulse	G	0.851		1.680							

[MEMO]

FUNCTION BLOCK

Function	D-LATCH HIGH SPEED							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F6R1	6											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

D	G	Q	QB
0	1	0	1
1	1	1	0
X	0	Latch	

X:Irrelevant

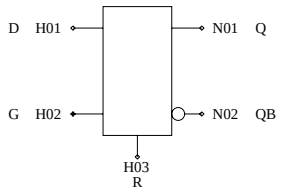
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F6R1	D → Q	(HH)	0.276	0.455	0.724	0.013	0.023	0.037		D	1.0	Q	22
		(LL)	0.301	0.563	1.037	0.010	0.016	0.027		G	1.0	QB	22
	D → QB	(HL)	0.412	0.724	1.206	0.009	0.015	0.024					
		(LH)	0.401	0.759	1.380	0.012	0.022	0.036					
	G → Q	(HH)	0.334	0.592	0.962	0.013	0.023	0.037					
		(HL)	0.316	0.615	1.119	0.010	0.016	0.027					
	G → QB	(HH)	0.416	0.808	1.462	0.012	0.022	0.036					
		(HL)	0.469	0.862	1.444	0.009	0.015	0.024					
	Set up time	D	1.558		2.103								
	Hold time	D	0.059		0.010								
	Min Pulse	G	0.921		2.002								

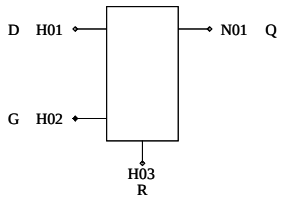
FUNCTION BLOCK

Function	D-LATCH WITH R							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L602	4		
x1	F602	6	F602NQ	6	F602NB	5						
x2	F602NP	9	F602NQP	7	F602NBP	6						
x4												

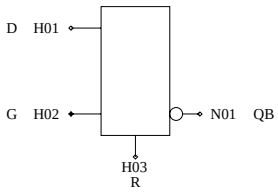
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	G	R	Q	QB
1	1	0	1	0
0	1	0	0	1
X	0	0	Latch	
X	X	1	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F602	D → Q	(HH)	0.562	1.055	1.831	0.012	0.022	0.036	D	1.0	Q	22
		(LL)	0.471	0.882	1.554	0.009	0.015	0.024	G	1.0	QB	22
	D → QB	(HL)	0.448	0.847	1.468	0.010	0.016	0.027	R	1.0		
		(LH)	0.340	0.621	1.089	0.012	0.023	0.036				
	G → Q	(HH)	0.620	1.193	2.068	0.012	0.022	0.036				
		(HL)	0.492	0.924	1.588	0.009	0.015	0.024				
	G → QB	(HH)	0.360	0.664	1.123	0.012	0.023	0.036				
		(HL)	0.506	0.984	1.705	0.010	0.016	0.027				
	R → Q	(HL)	0.322	0.692	1.141	0.009	0.016	0.026				
		(LH)	0.407	0.810	1.456	0.012	0.022	0.036				
	R → QB	(HH)	0.191	0.303	0.459	0.012	0.023	0.036				
		(LL)	0.295	0.601	1.093	0.010	0.016	0.027				
	Set up time	D	0.521		0.925							
	Hold time	D	0.045		0.010							
	Release time	R	1.450		1.990							
	Removal time	R	0.253		0.020							
	Min Pulse	G	1.118		2.541							
	Min Pulse	R	1.001		2.437							
F602NP	D → Q	(HH)	0.476	0.790	1.270	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.350	0.684	1.301	0.005	0.008	0.014	G	1.0	QB	45
	D → QB	(HL)	0.698	1.232	2.068	0.005	0.007	0.012	R	1.0		
		(LH)	0.533	1.037	1.926	0.006	0.011	0.018				
	G → Q	(HH)	0.478	0.836	1.350	0.007	0.013	0.020				
		(HL)	0.360	0.727	1.392	0.005	0.008	0.014				
	G → QB	(HH)	0.543	1.081	2.020	0.006	0.011	0.018				
		(HL)	0.699	1.279	2.151	0.005	0.007	0.012				
	R → Q	(HL)	0.359	0.759	1.301	0.005	0.008	0.013				
		(LH)	0.521	0.911	1.515	0.007	0.013	0.020				
	R → QB	(HH)	0.538	1.090	1.855	0.006	0.011	0.018				
		(LL)	0.744	1.356	2.316	0.005	0.007	0.012				
	Set up time	D	0.580		1.550							
	Hold time	D	0.060		0.000							
	Release time	R	0.500		1.390							
	Removal time	R	0.000		0.000							
	Min Pulse	G	1.126		2.469							
	Min Pulse	R	1.185		2.695							
L602	D → Q	(HH)	0.220	0.408	0.672	0.025	0.045	0.073	D	3.1	Q	10
		(LL)	0.205	0.353	0.589	0.020	0.031	0.050	G	1.0		
	G → Q	(HH)	0.336	0.594	0.970	0.025	0.045	0.073	R	1.0		
		(HL)	0.342	0.621	1.031	0.020	0.031	0.050				
	R → Q	(HL)	0.262	0.507	0.809	0.020	0.031	0.050				
		(LH)	0.254	0.451	0.740	0.024	0.045	0.073				
	Set up time	D	0.470		0.779							
	Hold time	D	0.319		0.351							
	Release time	R	1.238		1.519							
	Removal time	R	0.424		0.393							
	Min Pulse	G	0.983		2.067							
	Min Pulse	R	1.019		2.319							
F602NQ	D → Q	(HH)	0.404	0.664	1.055	0.014	0.025	0.039	D	1.0	Q	22
		(LL)	0.299	0.574	1.071	0.010	0.016	0.026	G	1.0		
	G → Q	(HH)	0.406	0.717	1.150	0.014	0.025	0.039	R	1.0		
		(HL)	0.314	0.625	1.158	0.010	0.016	0.026				
	R → Q	(HL)	0.308	0.659	1.120	0.009	0.015	0.025				
		(LH)	0.450	0.786	1.300	0.014	0.025	0.039				
	Set up time	D	0.420		1.050							
	Hold time	D	0.150		0.000							

FUNCTION BLOCK

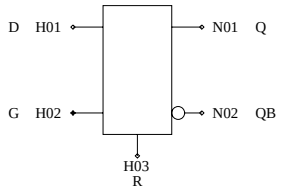
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	R	0.300		0.860							
	Removal time	R	0.000		0.000							
	Min Pulse	G	0.810		1.422							
	Min Pulse	R	0.869		1.632							
F602NQP	D → Q	(HH)	0.486	0.805	1.292	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.353	0.688	1.311	0.005	0.008	0.014	G	1.0		
	G → Q	(HH)	0.487	0.852	1.375	0.007	0.013	0.020	R	1.0		
		(HL)	0.362	0.734	1.403	0.005	0.008	0.014				
	R → Q	(HL)	0.360	0.762	1.307	0.005	0.008	0.013				
		(LH)	0.532	0.927	1.538	0.007	0.013	0.020				
	Set up time	D	0.480		1.320							
	Hold time	D	0.060		0.000							
	Release time	R	0.400		1.120							
	Removal time	R	0.000		0.000							
	Min Pulse	G	0.888		1.623							
	Min Pulse	R	0.947		1.848							
F602NB	D → QB	(HL)	0.406	0.781	1.351	0.009	0.015	0.025	D	1.0	QB	23
		(LH)	0.317	0.578	1.013	0.012	0.023	0.037	G	1.0		
	G → QB	(HH)	0.340	0.623	1.042	0.012	0.023	0.037	R	1.0		
		(HL)	0.473	0.927	1.602	0.009	0.015	0.025				
	R → QB	(HH)	0.184	0.289	0.428	0.012	0.023	0.037				
		(LL)	0.268	0.555	1.004	0.009	0.015	0.025				
	Set up time	D	0.380		0.790							
	Hold time	D	0.250		0.000							
	Release time	R	0.010		0.200							
	Removal time	R	0.000		0.000							
	Min Pulse	G	0.878		1.860							
	Min Pulse	R	0.719		1.351							
F602NBP	D → QB	(HL)	0.490	0.961	1.690	0.005	0.008	0.014	D	1.0	QB	45
		(LH)	0.360	0.653	1.135	0.006	0.011	0.018	G	1.0		
	G → QB	(HH)	0.382	0.694	1.163	0.006	0.011	0.018	R	1.0		
		(HL)	0.556	1.106	1.940	0.005	0.008	0.014				
	R → QB	(HH)	0.227	0.351	0.531	0.006	0.012	0.018				
		(LL)	0.349	0.734	1.342	0.005	0.008	0.014				
	Set up time	D	0.410		1.000							
	Hold time	D	0.180		0.000							
	Release time	R	0.080		0.480							
	Removal time	R	0.000		0.000							
	Min Pulse	G	0.954		2.162							
	Min Pulse	R	0.793		1.651							

[MEMO]

FUNCTION BLOCK

Function	D-LATCH WITH R HIGH SPEED											SSI Family	
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F6R2	7											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

D	G	R	Q	QB
1	1	0	1	0
0	1	0	0	1
X	0	0	Latch	
X	X	1	0	1

X:Irrelevant

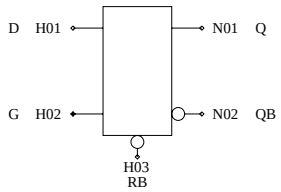
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F6R2	D → Q	(HH)	0.411	0.678	1.081	0.014	0.025	0.039		D	1.0	Q	21
		(LL)	0.311	0.594	1.101	0.010	0.017	0.027		G	1.0	QB	22
	D → QB	(HL)	0.528	0.934	1.565	0.009	0.015	0.024		R	1.0		
		(LH)	0.419	0.802	1.464	0.012	0.022	0.036					
	G → Q	(HH)	0.416	0.734	1.180	0.014	0.025	0.039					
		(HL)	0.328	0.649	1.196	0.010	0.017	0.027					
	G → QB	(HH)	0.437	0.855	1.559	0.012	0.022	0.036					
		(HL)	0.534	0.992	1.665	0.009	0.015	0.024					
	R → Q	(HL)	0.345	0.712	1.191	0.010	0.016	0.027					
		(LH)	0.475	0.830	1.372	0.014	0.025	0.039					
	R → QB	(HH)	0.458	0.919	1.534	0.012	0.023	0.036					
		(LL)	0.591	1.086	1.855	0.009	0.015	0.024					
	Set up time	D	1.828		2.491								
	Hold time	D	0.030		0.010								
	Release time	R	1.855		2.782								
	Removal time	R	0.010		0.010								
	Min Pulse	G	0.993		2.204								
	Min Pulse	R	1.190		2.865								

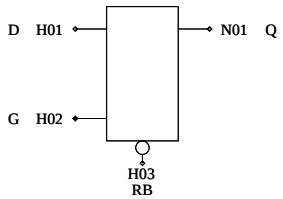
FUNCTION BLOCK

Function	D-LATCH WITH RB							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L603	4		
x1	F603	7	F603NQ	5	F603NB	6						
x2	F603NP	8	F603NQP	6	F603NBP	7						
x4												

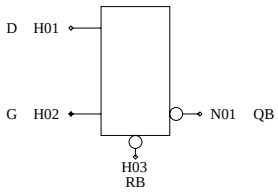
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	G	RB	Q	QB
1	1	1	1	0
0	1	1	0	1
X	0	1	Latch	
X	X	0	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F603	D → Q	(HH)	0.567	1.066	1.850	0.012	0.022	0.036	D	1.0	Q	22
		(LL)	0.477	0.888	1.565	0.009	0.015	0.024	G	1.0	QB	22
	D → QB	(HL)	0.451	0.853	1.480	0.010	0.016	0.027	RB	1.0		
		(LH)	0.342	0.624	1.094	0.012	0.023	0.036				
	G → Q	(HH)	0.625	1.203	2.087	0.012	0.022	0.036				
		(HL)	0.495	0.931	1.599	0.009	0.015	0.024				
	G → QB	(HH)	0.362	0.667	1.127	0.012	0.023	0.036				
		(HL)	0.509	0.990	1.717	0.010	0.016	0.027				
	RB → Q	(HH)	0.486	0.953	1.676	0.012	0.022	0.036				
		(LL)	0.386	0.826	1.390	0.009	0.016	0.026				
	RB → QB	(HL)	0.370	0.740	1.306	0.010	0.016	0.027				
		(LH)	0.253	0.432	0.701	0.012	0.023	0.036				
	Set up time	D	0.516		1.006							
	Hold time	D	0.042		0.010							
	Release time	RB	1.516		2.227							
	Removal time	RB	0.198		0.010							
	Min Pulse	G	1.120		2.554							
	Min Pulse	RB	1.048		2.648							
F603NP	D → Q	(HH)	0.461	0.769	1.238	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.349	0.679	1.293	0.005	0.008	0.014	G	1.0	QB	46
	D → QB	(HL)	0.665	1.193	2.016	0.004	0.007	0.012	RB	1.0		
		(LH)	0.524	1.022	1.906	0.006	0.011	0.018				
	G → Q	(HH)	0.468	0.822	1.330	0.007	0.013	0.020				
		(HL)	0.359	0.724	1.387	0.005	0.008	0.014				
	G → QB	(HH)	0.535	1.067	2.001	0.006	0.011	0.018				
		(HL)	0.672	1.248	2.107	0.004	0.007	0.012				
	RB → Q	(HH)	0.433	0.767	1.274	0.007	0.013	0.020				
		(LL)	0.314	0.658	1.124	0.005	0.008	0.013				
	RB → QB	(HL)	0.636	1.191	2.048	0.004	0.007	0.012				
		(LH)	0.482	0.976	1.661	0.006	0.011	0.018				
	Set up time	D	0.540		1.530							
	Hold time	D	0.080		0.000							
	Release time	RB	0.260		1.020							
	Removal time	RB	0.000		0.000							
	Min Pulse	G	1.098		2.424							
	Min Pulse	RB	1.086		2.393							
L603	D → Q	(HH)	0.210	0.390	0.644	0.024	0.045	0.073	D	3.1	Q	10
		(LL)	0.189	0.330	0.553	0.016	0.026	0.043	G	1.0		
	G → Q	(HH)	0.325	0.581	0.942	0.024	0.045	0.073	RB	1.0		
		(HL)	0.327	0.598	0.995	0.016	0.026	0.043				
	RB → Q	(HH)	0.170	0.302	0.490	0.024	0.045	0.073				
		(LL)	0.178	0.349	0.554	0.016	0.026	0.044				
	Set up time	D	0.482		0.773							
	Hold time	D	0.337		0.382							
	Release time	RB	1.123		1.301							
	Removal time	RB	0.521		0.568							
	Min Pulse	G	0.985		2.079							
	Min Pulse	RB	0.940		2.099							
F603NQ	D → Q	(HH)	0.396	0.652	1.037	0.013	0.025	0.039	D	1.0	Q	22
		(LL)	0.297	0.572	1.065	0.010	0.016	0.026	G	1.0		
	G → Q	(HH)	0.402	0.711	1.141	0.013	0.025	0.039	RB	1.0		
		(HL)	0.313	0.625	1.157	0.010	0.016	0.026				
	RB → Q	(HH)	0.370	0.651	1.072	0.013	0.025	0.039				
		(LL)	0.264	0.561	0.943	0.009	0.015	0.025				
	Set up time	D	0.410		1.030							
	Hold time	D	0.160		0.000							

FUNCTION BLOCK

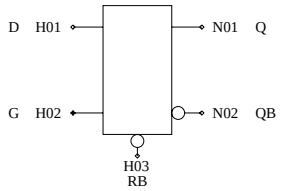
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	RB	0.070		0.510							
	Removal time	RB	0.000		0.000							
	Min Pulse	G	0.806		1.416							
	Min Pulse	RB	0.797		1.373							
F603NQP	D → Q	(HH)	0.477	0.790	1.269	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.351	0.685	1.304	0.005	0.008	0.014	G	1.0		
	G → Q	(HH)	0.482	0.843	1.360	0.007	0.013	0.020	RB	1.0		
		(HL)	0.362	0.732	1.400	0.005	0.008	0.014				
	RB → Q	(HH)	0.450	0.790	1.305	0.007	0.013	0.020				
		(LL)	0.314	0.662	1.130	0.005	0.008	0.013				
	Set up time	D	0.480		1.300							
	Hold time	D	0.070		0.000							
	Release time	RB	0.160		0.760							
	Removal time	RB	0.000		0.000							
	Min Pulse	G	0.883		1.612							
	Min Pulse	RB	0.874		1.583							
F603NB	D → QB	(HL)	0.406	0.781	1.351	0.009	0.015	0.025	D	1.0	QB	22
		(LH)	0.317	0.579	1.013	0.012	0.023	0.037	G	1.0		
	G → QB	(HH)	0.340	0.623	1.042	0.012	0.023	0.037	RB	1.0		
		(HL)	0.473	0.927	1.604	0.009	0.015	0.025				
	RB → QB	(HL)	0.334	0.678	1.194	0.009	0.015	0.025				
		(LH)	0.230	0.392	0.635	0.012	0.023	0.037				
	Set up time	D	0.380		0.790							
	Hold time	D	0.250		0.000							
	Release time	RB	0.000		0.340							
	Removal time	RB	0.100		0.000							
	Min Pulse	G	0.878		1.860							
	Min Pulse	RB	0.755		1.457							
F603NBP	D → QB	(HL)	0.491	0.964	1.695	0.005	0.008	0.014	D	1.0	QB	45
		(LH)	0.361	0.654	1.138	0.006	0.011	0.018	G	1.0		
	G → QB	(HH)	0.382	0.695	1.166	0.006	0.011	0.018	RB	1.0		
		(HL)	0.558	1.109	1.946	0.005	0.008	0.014				
	RB → QB	(HL)	0.418	0.860	1.538	0.005	0.008	0.014				
		(LH)	0.268	0.454	0.739	0.006	0.012	0.018				
	Set up time	D	0.410		1.010							
	Hold time	D	0.180		0.000							
	Release time	RB	0.000		0.610							
	Removal time	RB	0.030		0.000							
	Min Pulse	G	0.955		2.167							
	Min Pulse	RB	0.831		1.767							

[MEMO]

FUNCTION BLOCK

Function	D-LATCH WITH RB HIGH SPEED										SSI Family	
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F6R5	6										
x2												
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

D	G	RB	Q	QB
1	1	1	1	0
0	1	1	0	1
X	0	1	Latch	
X	X	0	0	1

X:Irrelevant

FUNCTION BLOCK

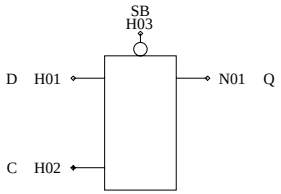
Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F6R5	D → Q	(HH)	0.411	0.676	1.081	0.014	0.025	0.039		D	1.0	Q	21
		(LL)	0.311	0.593	1.100	0.010	0.017	0.027		G	1.0	QB	22
	D → QB	(HL)	0.528	0.931	1.564	0.009	0.015	0.024		RB	1.0		
		(LH)	0.419	0.800	1.463	0.012	0.022	0.036					
	G → Q	(HH)	0.416	0.731	1.180	0.014	0.025	0.039					
		(HL)	0.328	0.645	1.196	0.010	0.017	0.027					
	G → QB	(HH)	0.437	0.851	1.559	0.012	0.022	0.036					
		(HL)	0.534	0.988	1.664	0.009	0.015	0.024					
	RB → Q	(HH)	0.395	0.686	1.136	0.014	0.025	0.039					
		(LL)	0.289	0.595	0.999	0.010	0.016	0.027					
	RB → QB	(HL)	0.512	0.942	1.619	0.009	0.015	0.024					
		(LH)	0.403	0.801	1.341	0.012	0.023	0.036					
	Set up time	D	1.828		2.491								
	Hold time	D	0.030		0.010								
	Release time	RB	1.786		2.550								
	Removal time	RB	0.010		0.010								
	Min Pulse	G	0.993		2.203								
	Min Pulse	RB	1.124		2.648								

FUNCTION BLOCK

Function	D-LATCH WITH SB							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L606	4		
x1												
x2												
x4												

Logic Diagram for "Normal"

Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

D	GB	SB	Q
1	0	1	1
0	0	1	0
X	1	1	Latch
X	X	0	1

X:Irrelevant

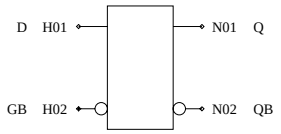
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L606	D → Q		(HH)	0.211	0.370	0.610	0.025	0.045	0.072	D	3.1	Q	9
			(LL)	0.246	0.477	0.856	0.020	0.032	0.050	C	1.0		
	C → Q		(HH)	0.320	0.551	0.892	0.025	0.045	0.073	SB	1.0		
			(HL)	0.394	0.748	1.285	0.020	0.031	0.050				
	SB → Q		(HL)	0.284	0.516	0.875	0.020	0.031	0.050				
			(LH)	0.217	0.463	0.753	0.024	0.045	0.072				
	Set up time	D		1.216		1.844							
	Hold time	D		0.477		0.520							
	Release time	SB		1.278		1.880							
	Removal time	SB		0.369		0.205							
	Min Pulse	C		5.000		5.000							
	Min Pulse	SB		5.000		5.000							

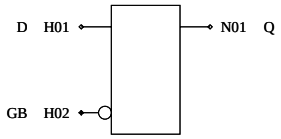
FUNCTION BLOCK

Function	D-LATCH (GB)							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power									L604	3			
x1	F604	6	F604NQ	5	F604NB	5							
x2	F604NP	8	F604NQP	6	F604NBP	6							
x4													

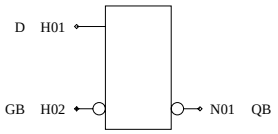
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	GB	Q	QB
1	0	1	0
0	0	0	1
X	1	Latch	

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F604	D → Q	(HH)	0.435	0.776	1.297	0.012	0.023	0.036	D	1.0	Q	23
		(LL)	0.449	0.843	1.494	0.009	0.015	0.024	GB	1.0	QB	22
	D → QB	(HL)	0.339	0.598	0.994	0.009	0.015	0.024				
		(LH)	0.332	0.602	1.056	0.012	0.023	0.036				
	GB → Q	(LH)	0.487	0.884	1.497	0.012	0.023	0.036				
		(LL)	0.496	0.947	1.689	0.009	0.015	0.024				
	GB → QB	(LH)	0.380	0.707	1.252	0.012	0.023	0.036				
		(LL)	0.390	0.707	1.194	0.009	0.015	0.024				
	Set up time	D	0.638		0.714							
	Hold time	D	0.110		0.010							
	Min Pulse	GB	1.002		2.179							
F604NP	D → Q	(HH)	0.318	0.531	0.852	0.006	0.012	0.019	D	1.0	Q	45
		(LL)	0.335	0.649	1.236	0.005	0.008	0.014	GB	1.0	QB	45
	D → QB	(HL)	0.517	0.927	1.560	0.005	0.007	0.012				
		(LH)	0.507	0.981	1.826	0.006	0.011	0.018				
	GB → Q	(LH)	0.379	0.664	1.093	0.006	0.012	0.019				
		(LL)	0.370	0.732	1.413	0.005	0.008	0.014				
	GB → QB	(LH)	0.542	1.064	2.002	0.006	0.011	0.018				
		(LL)	0.577	1.060	1.801	0.005	0.007	0.012				
	Set up time	D	0.680		1.410							
	Hold time	D	0.000		0.000							
	Min Pulse	GB	1.011		2.476							
L604	D → Q	(HH)	0.169	0.319	0.549	0.024	0.045	0.072	D	3.1	Q	10
		(LL)	0.187	0.323	0.538	0.016	0.026	0.043	GB	1.0		
	GB → Q	(LH)	0.315	0.581	1.001	0.024	0.044	0.072				
		(LL)	0.309	0.548	0.926	0.016	0.026	0.044				
	Set up time	D	0.454		0.663							
	Hold time	D	0.388		0.356							
	Min Pulse	GB	1.016		2.025							
F604NQ	D → Q	(HH)	0.256	0.427	0.677	0.013	0.023	0.037	D	1.0	Q	22
		(LL)	0.281	0.533	0.990	0.009	0.016	0.025	GB	1.0		
	GB → Q	(LH)	0.317	0.554	0.909	0.013	0.023	0.037				
		(LL)	0.324	0.630	1.178	0.009	0.015	0.025				
	Set up time	D	0.550		0.890							
	Hold time	D	0.050		0.000							
	Min Pulse	GB	0.751		1.492							
F604NQP	D → Q	(HH)	0.316	0.528	0.845	0.006	0.012	0.019	D	1.0	Q	44
		(LL)	0.335	0.649	1.235	0.005	0.008	0.014	GB	1.0		
	GB → Q	(LH)	0.377	0.660	1.086	0.006	0.012	0.019				
		(LL)	0.371	0.733	1.413	0.005	0.008	0.014				
	Set up time	D	0.620		1.160							
	Hold time	D	0.000		0.000							
	Min Pulse	GB	0.805		1.694							
F604NB	D → QB	(HL)	0.316	0.571	0.948	0.009	0.014	0.023	D	1.0	QB	23
		(LH)	0.314	0.571	1.002	0.012	0.023	0.037	GB	1.0		
	GB → QB	(LH)	0.365	0.680	1.199	0.012	0.023	0.037				
		(LL)	0.372	0.680	1.148	0.009	0.014	0.023				
	Set up time	D	0.500		0.760							
	Hold time	D	0.090		0.000							
	Min Pulse	GB	0.809		1.634							
F604NBP	D → QB	(HL)	0.369	0.671	1.129	0.005	0.008	0.012	D	1.0	QB	44
		(LH)	0.356	0.645	1.125	0.006	0.011	0.018	GB	1.0		
	GB → QB	(LH)	0.406	0.751	1.317	0.006	0.011	0.018				
		(LL)	0.425	0.781	1.325	0.005	0.008	0.012				
	Set up time	D	0.520		0.840							
	Hold time	D	0.070		0.000							

FUNCTION BLOCK

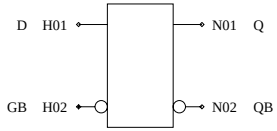
Block type	Switching speed										
	Path		t LD0 (ns)			t 1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Min Pulse	GB	0.850		1.742							

[MEMO]

FUNCTION BLOCK

Function	D-LATCH (GB) HIGH SPEED							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F6R8	6											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

D	GB	Q	QB
1	0	1	0
0	0	0	1
X	1	Latch	

X:Irrelevant

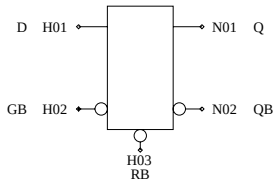
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F6R8	D → Q		(HH)	0.276	0.454	0.723	0.013	0.023	0.037	D	1.0	Q	22
			(LL)	0.301	0.563	1.037	0.010	0.016	0.027	GB	1.0	QB	22
	D → QB		(HL)	0.412	0.723	1.204	0.009	0.015	0.024				
			(LH)	0.401	0.758	1.380	0.012	0.022	0.036				
	GB → Q		(LH)	0.331	0.579	0.945	0.013	0.023	0.037				
			(LL)	0.338	0.652	1.218	0.010	0.016	0.027				
	GB → QB		(LH)	0.439	0.847	1.561	0.012	0.022	0.036				
			(LL)	0.466	0.847	1.427	0.009	0.015	0.024				
	Set up time	D		1.582		2.101							
	Hold time	D		0.055		0.010							
	Min Pulse	GB		0.933		1.994							

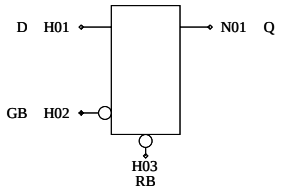
FUNCTION BLOCK

Function	D-LATCH (GB) WITH RB							SSI Family				
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L605	4		
x1	F605	7	F605NQ	5	F605NB	6						
x2	F605NP	8	F605NQP	6	F605NBP	7						
x4												

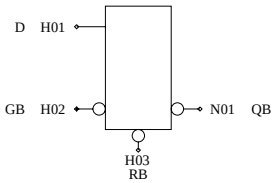
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	GB	RB	Q	QB
1	0	1	1	0
0	0	1	0	1
X	1	1	Latch	
X	X	0	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F605	D → Q	(HH)	0.567	1.066	1.849	0.012	0.022	0.036	D	1.0	Q	22
		(LL)	0.476	0.889	1.566	0.009	0.015	0.024	GB	1.0	QB	22
	D → QB	(HL)	0.451	0.853	1.479	0.010	0.016	0.027	RB	1.0		
		(LH)	0.342	0.624	1.094	0.012	0.023	0.036				
	GB → Q	(LH)	0.617	1.173	2.039	0.012	0.022	0.036				
		(LL)	0.522	0.990	1.751	0.009	0.015	0.024				
	GB → QB	(LH)	0.389	0.726	1.279	0.012	0.023	0.036				
		(LL)	0.501	0.960	1.669	0.010	0.016	0.027				
	RB → Q	(HH)	0.486	0.953	1.676	0.012	0.022	0.036				
		(LL)	0.386	0.826	1.389	0.009	0.016	0.026				
	RB → QB	(HL)	0.370	0.740	1.306	0.010	0.016	0.027				
		(LH)	0.253	0.432	0.701	0.012	0.023	0.036				
	Set up time	D	0.600		1.122							
	Hold time	D	0.033		0.010							
	Release time	RB	1.537		2.224							
	Removal time	RB	0.189		0.010							
	Min Pulse	GB	1.087		2.487							
	Min Pulse	RB	1.039		2.648							
F605NP	D → Q	(HH)	0.466	0.774	1.246	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.348	0.679	1.292	0.005	0.008	0.014	GB	1.0	QB	45
	D → QB	(HL)	0.666	1.196	2.018	0.004	0.007	0.012	RB	1.0		
		(LH)	0.529	1.028	1.912	0.006	0.011	0.018				
	GB → Q	(LH)	0.475	0.824	1.350	0.007	0.013	0.020				
		(LL)	0.378	0.749	1.451	0.005	0.008	0.014				
	GB → QB	(LH)	0.559	1.098	2.072	0.006	0.011	0.018				
		(LL)	0.675	1.247	2.123	0.004	0.007	0.012				
	RB → Q	(HH)	0.439	0.774	1.282	0.007	0.013	0.020				
		(LL)	0.314	0.658	1.124	0.005	0.008	0.013				
	RB → QB	(HL)	0.639	1.196	2.056	0.004	0.007	0.012				
		(LH)	0.487	0.982	1.670	0.006	0.011	0.018				
	Set up time	D	0.760		1.540							
	Hold time	D	0.000		0.000							
	Release time	RB	0.480		1.340							
	Removal time	RB	0.000		0.000							
	Min Pulse	GB	1.109		2.537							
	Min Pulse	RB	1.088		2.397							
L605	D → Q	(HH)	0.210	0.390	0.645	0.024	0.045	0.073	D	3.1	Q	10
		(LL)	0.189	0.329	0.552	0.016	0.026	0.043	GB	1.0		
	GB → Q	(LH)	0.347	0.645	1.104	0.024	0.045	0.072	RB	1.0		
		(LL)	0.315	0.559	0.942	0.016	0.026	0.044				
	RB → Q	(HH)	0.170	0.302	0.490	0.024	0.045	0.073				
		(LL)	0.178	0.349	0.554	0.016	0.026	0.044				
	Set up time	D	0.496		0.650							
	Hold time	D	0.331		0.339							
	Release time	RB	1.147		1.303							
	Removal time	RB	0.514		0.523							
	Min Pulse	GB	1.000		2.103							
	Min Pulse	RB	0.933		2.055							
F605NQ	D → Q	(HH)	0.396	0.652	1.037	0.013	0.025	0.039	D	1.0	Q	22
		(LL)	0.297	0.571	1.065	0.010	0.016	0.026	GB	1.0		
	GB → Q	(LH)	0.402	0.700	1.138	0.014	0.025	0.039	RB	1.0		
		(LL)	0.334	0.653	1.236	0.010	0.016	0.026				
	RB → Q	(HH)	0.370	0.651	1.072	0.013	0.025	0.039				
		(LL)	0.265	0.561	0.943	0.009	0.015	0.025				
	Set up time	D	0.590		1.070							
	Hold time	D	0.000		0.000							

FUNCTION BLOCK

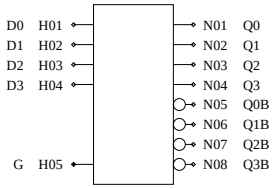
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	RB	0.310		0.860							
	Removal time	RB	0.000		0.000							
	Min Pulse	GB	0.813		1.534							
	Min Pulse	RB	0.797		1.373							
F605NQP	D → Q	(HH)	0.477	0.790	1.269	0.007	0.013	0.020	D	1.0	Q	43
		(LL)	0.351	0.685	1.303	0.005	0.008	0.014	GB	1.0		
	GB → Q	(LH)	0.485	0.841	1.374	0.007	0.013	0.020	RB	1.0		
		(LL)	0.381	0.755	1.463	0.005	0.008	0.014				
	RB → Q	(HH)	0.450	0.790	1.306	0.007	0.013	0.020				
		(LL)	0.313	0.662	1.130	0.005	0.008	0.013				
	Set up time	D	0.680		1.320							
	Hold time	D	0.000		0.000							
	Release time	RB	0.390		1.110							
	Removal time	RB	0.000		0.000							
	Min Pulse	GB	0.893		1.730							
	Min Pulse	RB	0.875		1.582							
F605NB	D → QB	(HL)	0.406	0.781	1.350	0.009	0.015	0.025	D	1.0	QB	23
		(LH)	0.317	0.579	1.013	0.012	0.023	0.037	GB	1.0		
	GB → QB	(LH)	0.370	0.689	1.214	0.012	0.023	0.037	RB	1.0		
		(LL)	0.463	0.892	1.550	0.009	0.015	0.025				
	RB → QB	(HL)	0.333	0.678	1.194	0.009	0.015	0.025				
		(LH)	0.230	0.392	0.635	0.012	0.023	0.037				
	Set up time	D	0.500		0.870							
	Hold time	D	0.040		0.000							
	Release time	RB	0.100		0.470							
	Removal time	RB	0.000		0.000							
	Min Pulse	GB	0.878		1.870							
	Min Pulse	RB	0.755		1.457							
F605NBP	D → QB	(HL)	0.491	0.963	1.695	0.005	0.008	0.014	D	1.0	QB	45
		(LH)	0.361	0.654	1.139	0.006	0.011	0.018	GB	1.0		
	GB → QB	(LH)	0.413	0.762	1.338	0.006	0.011	0.018	RB	1.0		
		(LL)	0.548	1.075	1.895	0.005	0.008	0.014				
	RB → QB	(HL)	0.418	0.860	1.537	0.005	0.008	0.014				
		(LH)	0.268	0.454	0.739	0.006	0.012	0.018				
	Set up time	D	0.530		1.140							
	Hold time	D	0.000		0.000							
	Release time	RB	0.180		0.740							
	Removal time	RB	0.000		0.000							
	Min Pulse	GB	0.955		2.181							
	Min Pulse	RB	0.832		1.767							

[MEMO]

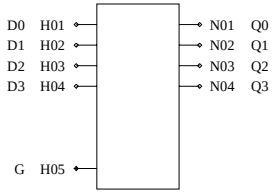
FUNCTION BLOCK

Function	4-BIT D-LATCH										SSI Family	
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L901	10		
x1	F901	20										
x2												
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

Dn	G	Qn	QnB
0	1	0	1
1	1	1	0
X	0	Latch	

n= 0 to 3

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F901	D0 → Q0	(HH)	0.424	0.761	1.276	0.012	0.022	0.036	D0	1.0	Q0	23
		(LL)	0.442	0.832	1.476	0.009	0.015	0.024	D1	1.0	Q1	23
	D0 → Q0B	(HL)	0.331	0.587	0.979	0.009	0.015	0.024	D2	1.0	Q2	23
		(LH)	0.328	0.598	1.049	0.012	0.023	0.036	D3	1.0	Q3	23
	D1 → Q1	(HH)	0.425	0.761	1.275	0.012	0.022	0.036	G	2.0	Q0B	22
		(LL)	0.442	0.832	1.477	0.009	0.015	0.024			Q1B	23
	D1 → Q1B	(HL)	0.331	0.587	0.979	0.009	0.015	0.024			Q2B	22
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036			Q3B	23
	D2 → Q2	(HH)	0.424	0.761	1.276	0.012	0.022	0.036				
		(LL)	0.442	0.832	1.476	0.009	0.015	0.024				
	D2 → Q2B	(HL)	0.331	0.587	0.979	0.009	0.015	0.024				
		(LH)	0.328	0.598	1.049	0.012	0.023	0.036				
	D3 → Q3	(HH)	0.425	0.761	1.275	0.012	0.022	0.036				
		(LL)	0.442	0.832	1.477	0.009	0.015	0.024				
	D3 → Q3B	(HL)	0.331	0.587	0.979	0.009	0.015	0.024				
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036				
	G → Q0	(HH)	0.559	1.020	1.710	0.012	0.022	0.036				
		(HL)	0.510	0.934	1.590	0.009	0.015	0.024				
	G → Q1	(HH)	0.559	1.020	1.710	0.012	0.022	0.036				
		(HL)	0.510	0.934	1.590	0.009	0.015	0.024				
	G → Q2	(HH)	0.559	1.020	1.710	0.012	0.022	0.036				
		(HL)	0.510	0.934	1.590	0.009	0.015	0.024				
	G → Q3	(HH)	0.559	1.020	1.710	0.012	0.022	0.036				
		(HL)	0.510	0.934	1.590	0.009	0.015	0.024				
	G → Q0B	(HH)	0.397	0.701	1.165	0.012	0.023	0.036				
		(HL)	0.465	0.846	1.414	0.009	0.015	0.024				
	G → Q1B	(HH)	0.397	0.701	1.165	0.012	0.023	0.036				
		(HL)	0.465	0.846	1.414	0.009	0.015	0.024				
	G → Q2B	(HH)	0.397	0.701	1.165	0.012	0.023	0.036				
		(HL)	0.465	0.846	1.414	0.009	0.015	0.024				
	G → Q3B	(HH)	0.397	0.701	1.165	0.012	0.023	0.036				
		(HL)	0.465	0.846	1.414	0.009	0.015	0.024				
	Set up time	D0	0.435		0.812							
	Set up time	D1	0.435		0.812							
	Set up time	D2	0.435		0.812							
	Set up time	D3	0.435		0.812							
	Hold time	D0	0.207		0.112							
	Hold time	D1	0.208		0.112							
	Hold time	D2	0.207		0.112							
	Hold time	D3	0.208		0.112							
	Min Pulse	G	1.201		2.485							
L901	D0 → Q0	(HH)	0.166	0.323	0.539	0.025	0.045	0.072	D0	3.0	Q0	10
		(LL)	0.186	0.319	0.531	0.017	0.028	0.045	D1	3.0	Q1	10
	D1 → Q1	(HH)	0.166	0.323	0.539	0.025	0.045	0.072	D2	3.0	Q2	10
		(LL)	0.186	0.319	0.531	0.017	0.028	0.045	D3	3.0	Q3	10
	D2 → Q2	(HH)	0.166	0.323	0.539	0.025	0.045	0.072	G	2.0		
		(LL)	0.186	0.319	0.531	0.017	0.028	0.045				
	D3 → Q3	(HH)	0.166	0.323	0.539	0.025	0.045	0.072				
		(LL)	0.186	0.319	0.531	0.017	0.028	0.045				
	G → Q0	(HH)	0.321	0.556	0.891	0.024	0.045	0.073				
		(HL)	0.371	0.668	1.120	0.017	0.027	0.045				
	G → Q1	(HH)	0.321	0.556	0.891	0.024	0.045	0.073				
		(HL)	0.371	0.668	1.120	0.017	0.027	0.045				
	G → Q2	(HH)	0.321	0.556	0.891	0.024	0.045	0.073				
		(HL)	0.371	0.668	1.120	0.017	0.027	0.045				
	G → Q3	(HH)	0.321	0.556	0.891	0.024	0.045	0.073				

FUNCTION BLOCK

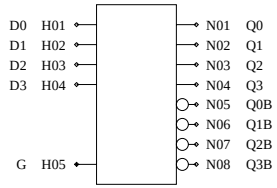
Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
		(HL)	0.371	0.668	1.120	0.017	0.027	0.045				
	Set up time	D0	0.484		0.857							
	Set up time	D1	0.484		0.857							
	Set up time	D2	0.484		0.857							
	Set up time	D3	0.484		0.857							
	Hold time	D0	0.450		0.541							
	Hold time	D1	0.450		0.541							
	Hold time	D2	0.450		0.541							
	Hold time	D3	0.450		0.541							
	Min Pulse	G	1.164		2.319							

[MEMO]

FUNCTION BLOCK

Function	4-BIT D-LATCH HIGH SPEED							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F971	20											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

Dn	G	Qn	QnB
0	1	0	1
1	1	1	0
X	0	Latch	

n= 0 to 3

X:Irrelevant

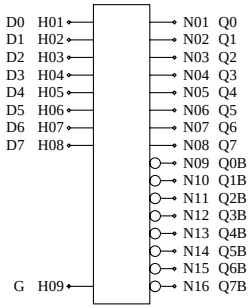
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F971	D0 → Q0	(HH)	0.264	0.442	0.699	0.013	0.023	0.037	D0	1.0	Q0	22
		(LL)	0.294	0.554	1.022	0.010	0.016	0.027	D1	1.0	Q1	22
	D0 → Q0B	(HL)	0.399	0.710	1.177	0.009	0.015	0.024	D2	1.0	Q2	22
		(LH)	0.395	0.749	1.365	0.012	0.022	0.036	D3	1.0	Q3	22
	D1 → Q1	(HH)	0.263	0.441	0.697	0.013	0.023	0.037	G	2.0	Q0B	22
		(LL)	0.294	0.552	1.019	0.010	0.016	0.027			Q1B	22
	D1 → Q1B	(HL)	0.398	0.709	1.177	0.009	0.015	0.024			Q2B	22
		(LH)	0.395	0.747	1.362	0.012	0.022	0.036			Q3B	22
	D2 → Q2	(HH)	0.263	0.441	0.699	0.013	0.023	0.037				
		(LL)	0.294	0.553	1.019	0.010	0.016	0.027				
	D2 → Q2B	(HL)	0.399	0.709	1.178	0.009	0.015	0.024				
		(LH)	0.394	0.748	1.362	0.012	0.022	0.036				
	D3 → Q3	(HH)	0.264	0.442	0.698	0.013	0.023	0.037				
		(LL)	0.295	0.553	1.023	0.010	0.016	0.027				
	D3 → Q3B	(HL)	0.400	0.710	1.180	0.009	0.015	0.024				
		(LH)	0.395	0.749	1.366	0.012	0.022	0.036				
	G → Q0	(HH)	0.394	0.693	1.117	0.013	0.023	0.037				
		(HL)	0.370	0.698	1.219	0.010	0.016	0.027				
	G → Q1	(HH)	0.394	0.693	1.118	0.013	0.023	0.037				
		(HL)	0.371	0.699	1.219	0.010	0.016	0.027				
	G → Q2	(HH)	0.394	0.693	1.118	0.013	0.023	0.037				
		(HL)	0.371	0.699	1.219	0.010	0.016	0.027				
	G → Q3	(HH)	0.394	0.693	1.117	0.013	0.023	0.037				
		(HL)	0.370	0.698	1.219	0.010	0.016	0.027				
	G → Q0B	(HH)	0.471	0.892	1.561	0.012	0.022	0.036				
		(HL)	0.530	0.963	1.601	0.009	0.015	0.024				
	G → Q1B	(HH)	0.471	0.892	1.561	0.012	0.022	0.036				
		(HL)	0.530	0.963	1.601	0.009	0.015	0.024				
	G → Q2B	(HH)	0.471	0.892	1.561	0.012	0.022	0.036				
		(HL)	0.530	0.963	1.601	0.009	0.015	0.024				
	G → Q3B	(HH)	0.471	0.892	1.561	0.012	0.022	0.036				
		(HL)	0.530	0.963	1.601	0.009	0.015	0.024				
	Set up time	D0	1.551		2.032							
	Set up time	D1	1.551		2.037							
	Set up time	D2	1.551		2.037							
	Set up time	D3	1.551		2.032							
	Hold time	D0	0.145		0.073							
	Hold time	D1	0.156		0.079							
	Hold time	D2	0.144		0.059							
	Hold time	D3	0.158		0.072							
	Min Pulse	G	1.143		2.349							

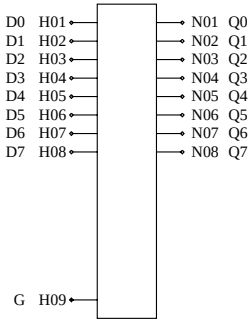
FUNCTION BLOCK

Function	8-BIT D-LATCH											SSI Family	
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power									L902	18			
x1	F902	38											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

Dn	G	Qn	QnB
0	1	0	1
1	1	1	0
X	0	Latch	

n= 0 to 7

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F902	D0 → Q0	(HH)	0.427	0.764	1.280	0.012	0.023	0.036	D0	1.0	Q0	23
		(LL)	0.444	0.839	1.484	0.009	0.015	0.024	D1	1.0	Q1	22
	D0 → Q0B	(HL)	0.330	0.586	0.978	0.009	0.015	0.024	D2	1.0	Q2	23
		(LH)	0.328	0.598	1.048	0.012	0.023	0.036	D3	1.0	Q3	22
	D1 → Q1	(HH)	0.426	0.763	1.280	0.012	0.023	0.036	D4	1.0	Q4	23
		(LL)	0.445	0.838	1.488	0.009	0.015	0.024	D5	1.0	Q5	22
	D1 → Q1B	(HL)	0.331	0.587	0.977	0.009	0.015	0.024	D6	1.0	Q6	23
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036	D7	1.0	Q7	22
	D2 → Q2	(HH)	0.427	0.764	1.280	0.012	0.023	0.036	G	2.0	Q0B	22
		(LL)	0.444	0.839	1.484	0.009	0.015	0.024			Q1B	22
	D2 → Q2B	(HL)	0.330	0.586	0.978	0.009	0.015	0.024			Q2B	22
		(LH)	0.328	0.598	1.048	0.012	0.023	0.036			Q3B	22
	D3 → Q3	(HH)	0.426	0.763	1.280	0.012	0.023	0.036			Q4B	22
		(LL)	0.445	0.838	1.488	0.009	0.015	0.024			Q5B	22
	D3 → Q3B	(HL)	0.331	0.587	0.977	0.009	0.015	0.024			Q6B	22
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036			Q7B	22
	D4 → Q4	(HH)	0.427	0.764	1.280	0.012	0.023	0.036				
		(LL)	0.444	0.839	1.484	0.009	0.015	0.024				
	D4 → Q4B	(HL)	0.330	0.586	0.978	0.009	0.015	0.024				
		(LH)	0.328	0.598	1.048	0.012	0.023	0.036				
	D5 → Q5	(HH)	0.426	0.763	1.280	0.012	0.023	0.036				
		(LL)	0.445	0.838	1.488	0.009	0.015	0.024				
	D5 → Q5B	(HL)	0.331	0.587	0.977	0.009	0.015	0.024				
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036				
	D6 → Q6	(HH)	0.427	0.764	1.280	0.012	0.023	0.036				
		(LL)	0.444	0.839	1.484	0.009	0.015	0.024				
	D6 → Q6B	(HL)	0.330	0.586	0.978	0.009	0.015	0.024				
		(LH)	0.328	0.598	1.048	0.012	0.023	0.036				
	D7 → Q7	(HH)	0.426	0.763	1.280	0.012	0.023	0.036				
		(LL)	0.445	0.838	1.488	0.009	0.015	0.024				
	D7 → Q7B	(HL)	0.331	0.587	0.977	0.009	0.015	0.024				
		(LH)	0.328	0.597	1.050	0.012	0.023	0.036				
	G → Q0	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q1	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q2	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q3	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q4	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q5	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q6	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q7	(HH)	0.667	1.214	2.056	0.012	0.022	0.036				
		(HL)	0.577	1.032	1.747	0.009	0.015	0.024				
	G → Q0B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q1B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q2B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q3B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	G → Q4B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q5B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q6B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	G → Q7B	(HH)	0.461	0.794	1.313	0.012	0.023	0.036				
		(HL)	0.571	1.036	1.751	0.009	0.015	0.025				
	Set up time	D0	0.429		0.736							
	Set up time	D1	0.429		0.736							
	Set up time	D2	0.429		0.736							
	Set up time	D3	0.429		0.736							
	Set up time	D4	0.429		0.736							
	Set up time	D5	0.429		0.736							
	Set up time	D6	0.429		0.736							
	Set up time	D7	0.429		0.736							
	Hold time	D0	0.402		0.454							
	Hold time	D1	0.403		0.454							
	Hold time	D2	0.402		0.454							
	Hold time	D3	0.403		0.454							
	Hold time	D4	0.402		0.454							
	Hold time	D5	0.403		0.454							
	Hold time	D6	0.402		0.454							
	Hold time	D7	0.403		0.454							
	Min Pulse	G	1.569		3.143							
L902	D0 → Q0	(HH)	0.165	0.322	0.549	0.024	0.045	0.072	D0	3.0	Q0	10
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045	D1	3.0	Q1	10
	D1 → Q1	(HH)	0.165	0.322	0.549	0.024	0.045	0.072	D2	3.0	Q2	10
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045	D3	3.0	Q3	10
	D2 → Q2	(HH)	0.165	0.322	0.549	0.024	0.045	0.072	D4	3.0	Q4	10
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045	D5	3.0	Q5	10
	D3 → Q3	(HH)	0.165	0.322	0.549	0.024	0.045	0.072	D6	3.0	Q6	10
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045	D7	3.0	Q7	10
	D4 → Q4	(HH)	0.165	0.322	0.549	0.024	0.045	0.072	G	2.0		
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045				
	D5 → Q5	(HH)	0.165	0.322	0.549	0.024	0.045	0.072				
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045				
	D6 → Q6	(HH)	0.165	0.322	0.549	0.024	0.045	0.072				
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045				
	D7 → Q7	(HH)	0.165	0.322	0.549	0.024	0.045	0.072				
		(LL)	0.185	0.319	0.532	0.017	0.028	0.045				
	G → Q0	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q1	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q2	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q3	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q4	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q5	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q6	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	G → Q7	(HH)	0.369	0.626	1.017	0.025	0.045	0.073				

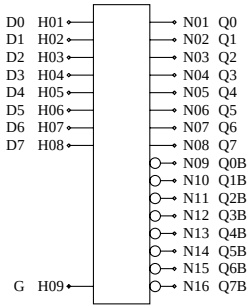
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
		(HL)	0.455	0.829	1.404	0.017	0.027	0.045				
	Set up time	D0	0.490		0.699							
	Set up time	D1	0.490		0.699							
	Set up time	D2	0.490		0.699							
	Set up time	D3	0.490		0.699							
	Set up time	D4	0.490		0.699							
	Set up time	D5	0.490		0.699							
	Set up time	D6	0.490		0.699							
	Set up time	D7	0.490		0.699							
	Hold time	D0	0.589		0.799							
	Hold time	D1	0.589		0.799							
	Hold time	D2	0.589		0.799							
	Hold time	D3	0.589		0.799							
	Hold time	D4	0.589		0.799							
	Hold time	D5	0.589		0.799							
	Hold time	D6	0.589		0.799							
	Hold time	D7	0.589		0.799							
	Min Pulse	G	1.467		2.849							

FUNCTION BLOCK

Function	8-BIT D-LATCH HIGH SPEED							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F972	38											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

Dn	G	Qn	QnB
0	1	0	1
1	1	1	0
X	0	Latch	

n= 0 to 7

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F972	D0 → Q0	(HH)	0.264	0.441	0.699	0.013	0.023	0.037	D0	1.0	Q0	22
		(LL)	0.295	0.554	1.023	0.010	0.016	0.027	D1	1.0	Q1	22
	D0 → Q0B	(HL)	0.399	0.709	1.178	0.009	0.015	0.024	D2	1.0	Q2	22
		(LH)	0.395	0.749	1.365	0.012	0.022	0.036	D3	1.0	Q3	22
	D1 → Q1	(HH)	0.263	0.440	0.696	0.013	0.023	0.037	D4	1.0	Q4	22
		(LL)	0.294	0.553	1.021	0.010	0.016	0.027	D5	1.0	Q5	22
	D1 → Q1B	(HL)	0.398	0.708	1.177	0.009	0.015	0.024	D6	1.0	Q6	22
		(LH)	0.394	0.748	1.364	0.012	0.022	0.036	D7	1.0	Q7	22
	D2 → Q2	(HH)	0.263	0.440	0.698	0.013	0.023	0.037	G	2.0	Q0B	22
		(LL)	0.294	0.552	1.020	0.010	0.016	0.027			Q1B	22
	D2 → Q2B	(HL)	0.398	0.708	1.177	0.009	0.015	0.024			Q2B	22
		(LH)	0.394	0.747	1.362	0.012	0.022	0.036			Q3B	22
	D3 → Q3	(HH)	0.264	0.441	0.697	0.013	0.023	0.037			Q4B	22
		(LL)	0.294	0.553	1.024	0.010	0.016	0.027			Q5B	22
	D3 → Q3B	(HL)	0.399	0.709	1.178	0.009	0.015	0.024			Q6B	22
		(LH)	0.395	0.749	1.367	0.012	0.022	0.036			Q7B	22
	D4 → Q4	(HH)	0.264	0.441	0.699	0.013	0.023	0.037				
		(LL)	0.295	0.554	1.023	0.010	0.016	0.027				
	D4 → Q4B	(HL)	0.399	0.709	1.178	0.009	0.015	0.024				
		(LH)	0.395	0.749	1.365	0.012	0.022	0.036				
	D5 → Q5	(HH)	0.263	0.440	0.696	0.013	0.023	0.037				
		(LL)	0.294	0.553	1.021	0.010	0.016	0.027				
	D5 → Q5B	(HL)	0.398	0.708	1.177	0.009	0.015	0.024				
		(LH)	0.394	0.748	1.364	0.012	0.022	0.036				
	D6 → Q6	(HH)	0.263	0.440	0.698	0.013	0.023	0.037				
		(LL)	0.294	0.552	1.020	0.010	0.016	0.027				
	D6 → Q6B	(HL)	0.398	0.708	1.177	0.009	0.015	0.024				
		(LH)	0.394	0.747	1.362	0.012	0.022	0.036				
	D7 → Q7	(HH)	0.264	0.441	0.697	0.013	0.023	0.037				
		(LL)	0.294	0.553	1.024	0.010	0.016	0.027				
	D7 → Q7B	(HL)	0.399	0.709	1.178	0.009	0.015	0.024				
		(LH)	0.395	0.749	1.367	0.012	0.022	0.036				
	G → Q0	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.367	0.010	0.016	0.027				
	G → Q1	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.368	0.010	0.016	0.027				
	G → Q2	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.368	0.010	0.016	0.027				
	G → Q3	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.367	0.010	0.016	0.027				
	G → Q4	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.367	0.010	0.016	0.027				
	G → Q5	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.368	0.010	0.016	0.027				
	G → Q6	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.368	0.010	0.016	0.027				
	G → Q7	(HH)	0.494	0.877	1.451	0.013	0.023	0.037				
		(HL)	0.453	0.813	1.367	0.010	0.016	0.027				
	G → Q0B	(HH)	0.554	1.006	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q1B	(HH)	0.555	1.007	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q2B	(HH)	0.555	1.007	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q3B	(HH)	0.554	1.006	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				

FUNCTION BLOCK

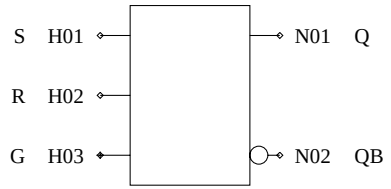
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	G → Q4B	(HH)	0.554	1.006	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q5B	(HH)	0.555	1.007	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q6B	(HH)	0.555	1.007	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	G → Q7B	(HH)	0.554	1.006	1.708	0.012	0.022	0.036				
		(HL)	0.631	1.147	1.937	0.009	0.015	0.024				
	Set up time	D0	1.497		1.962							
	Set up time	D1	1.496		1.961							
	Set up time	D2	1.496		1.961							
	Set up time	D3	1.497		1.961							
	Set up time	D4	1.497		1.962							
	Set up time	D5	1.496		1.961							
	Set up time	D6	1.496		1.961							
	Set up time	D7	1.497		1.961							
	Hold time	D0	0.325		0.391							
	Hold time	D1	0.334		0.403							
	Hold time	D2	0.324		0.385							
	Hold time	D3	0.334		0.398							
	Hold time	D4	0.325		0.391							
	Hold time	D5	0.334		0.403							
	Hold time	D6	0.324		0.385							
	Hold time	D7	0.334		0.398							
	Min Pulse	G	1.455		2.971							

[MEMO]

FUNCTION BLOCK

Function	RS-LATCH					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F595	5					
x2							
x4							

Logic Diagram



Truth Table

S	R	G	Q	QB
0	0	1	Latch	
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
1	1	1->0	Undefined	
X	X	0	Latch	

X:Irrelevant

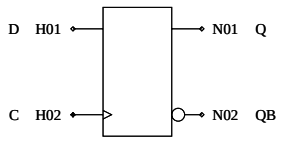
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F595	S → Q	(HH)	0.254	0.434	0.717	0.013	0.023	0.037	S	1.0	Q	22
		(LL)	0.345	0.714	1.265	0.010	0.016	0.026	R	1.0	QB	22
	S → QB	(HL)	0.553	1.053	1.825	0.010	0.016	0.026	G	2.1		
	R → Q	(HL)	0.553	1.053	1.826	0.010	0.016	0.026				
	R → QB	(HH)	0.254	0.435	0.718	0.013	0.023	0.037				
		(LL)	0.347	0.717	1.269	0.010	0.016	0.026				
	G → Q	(HH)	0.276	0.438	0.683	0.013	0.023	0.037				
		(HL)	0.570	1.053	1.788	0.010	0.016	0.026				
	G → QB	(HH)	0.276	0.439	0.684	0.013	0.023	0.037				
		(HL)	0.570	1.052	1.786	0.010	0.016	0.026				
	Min Pulse	G	1.042		2.887							

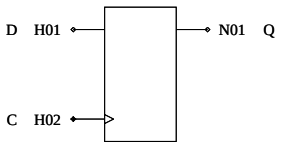
FUNCTION BLOCK

Function	D-F/F								SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L611	5		
x1	F641	8	F641NQ	7	F641NB	7	F611	8				
x2	F641NP	10	F641NQP	8	F641NBP	8						
x4												

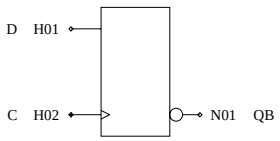
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	Q	QB
0	↗	0	1
1	↗	1	0
X	↘	Hold	

X:Irrelevant

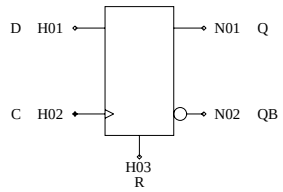
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L611	C → Q	(HH)	0.341	0.613	0.999	0.025	0.045	0.072		D	3.1	Q	10
		(HL)	0.303	0.542	0.905	0.017	0.027	0.044		C	1.0		
	Set up time	D	0.383		0.774								
	Hold time	D	0.415		0.387								
	Min Pulse	C	1.090		2.050								
F641	C → Q	(HH)	0.373	0.666	1.113	0.012	0.023	0.036		D	1.0	Q	22
		(HL)	0.439	0.812	1.367	0.009	0.015	0.025		C	1.0	QB	23
	C → QB	(HH)	0.537	0.992	1.676	0.012	0.023	0.036					
		(HL)	0.491	0.908	1.555	0.009	0.015	0.024					
	Set up time	D	0.432		0.937								
	Hold time	D	0.286		0.148								
	Min Pulse	C	1.238		2.483								
F611	C → Q	(HH)	0.373	0.666	1.113	0.012	0.023	0.036		D	1.0	Q	22
		(HL)	0.439	0.812	1.367	0.009	0.015	0.025		C	1.0	QB	23
	C → QB	(HH)	0.537	0.992	1.676	0.012	0.023	0.036					
		(HL)	0.491	0.908	1.555	0.009	0.015	0.024					
	Set up time	D	0.432		0.937								
	Hold time	D	0.286		0.148								
	Min Pulse	C	1.238		2.483								
F641NP	C → Q	(HH)	0.399	0.712	1.187	0.006	0.011	0.018		D	1.0	Q	46
		(HL)	0.473	0.889	1.509	0.005	0.008	0.012		C	1.0	QB	46
	C → QB	(HH)	0.626	1.164	1.978	0.006	0.011	0.018					
		(HL)	0.565	1.055	1.812	0.004	0.007	0.012					
	Set up time	D	0.480		0.750								
	Hold time	D	0.130		0.030								
	Min Pulse	C	1.061		2.365								
F641NQ	C → Q	(HH)	0.359	0.642	1.070	0.012	0.023	0.037		D	1.0	Q	23
		(HL)	0.422	0.790	1.332	0.009	0.014	0.023		C	1.0		
	Set up time	D	0.480		0.750								
	Hold time	D	0.130		0.030								
	Min Pulse	C	0.838		1.653								
F641NQP	C → Q	(HH)	0.400	0.713	1.190	0.006	0.011	0.018		D	1.0	Q	44
		(HL)	0.474	0.891	1.512	0.005	0.008	0.012		C	1.0		
	Set up time	D	0.480		0.750								
	Hold time	D	0.130		0.030								
	Min Pulse	C	0.884		1.808								
F641NB	C → QB	(HH)	0.358	0.644	1.050	0.013	0.023	0.037		D	1.0	QB	22
		(HL)	0.342	0.662	1.154	0.010	0.016	0.026		C	1.0		
	Set up time	D	0.480		0.750								
	Hold time	D	0.130		0.040								
	Min Pulse	C	0.776		1.407								
F641NBP	C → QB	(HH)	0.414	0.740	1.207	0.006	0.012	0.019		D	1.0	QB	43
		(HL)	0.390	0.779	1.446	0.005	0.008	0.014		C	1.0		
	Set up time	D	0.490		0.760								
	Hold time	D	0.130		0.030								
	Min Pulse	C	0.827		1.662								

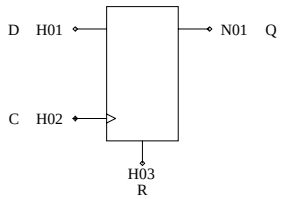
FUNCTION BLOCK

Function	D-F/F WITH R						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F642	9	F642NQ	8	F642NB	8						
x2	F642NP	11	F642NQP	9	F642NBP	9						
x4												

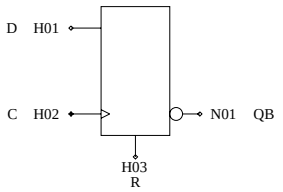
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	R	Q	QB
0	↗	0	0	1
1	↗	0	1	0
X	↘	0	Hold	
X	X	1	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t_{LD0} (ns)			t_1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F642	C → Q	(HH)	0.392	0.700	1.182	0.013	0.023	0.037	D	1.0	Q	23
		(HL)	0.446	0.822	1.377	0.009	0.015	0.024	C	1.0	QB	23
	C → QB	(HH)	0.544	0.998	1.677	0.012	0.023	0.036	R	2.2		
		(HL)	0.597	1.137	1.987	0.009	0.015	0.025				
	R → Q	(HL)	0.372	0.668	1.100	0.009	0.014	0.024				
	R → QB	(HH)	0.172	0.334	0.493	0.013	0.023	0.037				
	Set up time	D	0.460		1.330							
	Hold time	D	0.130		0.050							
	Release time	R	0.150		0.810							
	Removal time	R	0.000		0.000							
	Min Pulse	C	1.002		2.274							
	Min Pulse	R	0.790		1.431							
F642NP	C → Q	(HH)	0.440	0.783	1.324	0.006	0.011	0.018	D	1.0	Q	46
		(HL)	0.501	0.927	1.565	0.005	0.007	0.012	C	1.0	QB	46
	C → QB	(HH)	0.656	1.210	2.050	0.006	0.011	0.018	R	2.2		
		(HL)	0.746	1.429	2.517	0.005	0.008	0.013				
	R → Q	(HL)	0.430	0.850	1.423	0.005	0.007	0.012				
	R → QB	(HH)	0.219	0.398	0.600	0.006	0.012	0.019				
	Set up time	D	0.460		1.330							
	Hold time	D	0.130		0.060							
	Release time	R	0.150		0.810							
	Removal time	R	0.000		0.000							
	Min Pulse	C	1.143		2.768							
	Min Pulse	R	0.841		1.724							
F642NQ	C → Q	(HH)	0.391	0.701	1.181	0.012	0.023	0.037	D	1.0	Q	22
		(HL)	0.445	0.822	1.373	0.009	0.014	0.023	C	1.0		
	R → Q	(HL)	0.332	0.644	1.052	0.009	0.014	0.023	R	2.2		
	Set up time	D	0.460		1.330							
	Hold time	D	0.130		0.050							
	Release time	R	0.150		0.810							
	Removal time	R	0.000		0.000							
	Min Pulse	C	0.858		1.693							
	Min Pulse	R	0.753		1.380							
F642NQP	C → Q	(HH)	0.441	0.786	1.329	0.006	0.011	0.018	D	1.0	Q	45
		(HL)	0.501	0.930	1.566	0.005	0.007	0.012	C	1.0		
	R → Q	(HL)	0.388	0.757	1.250	0.005	0.007	0.012	R	2.2		
	Set up time	D	0.460		1.330							
	Hold time	D	0.130		0.060							
	Release time	R	0.150		0.810							
	Removal time	R	0.000		0.000							
	Min Pulse	C	0.905		1.856							
	Min Pulse	R	0.801		1.550							
F642NB	C → QB	(HH)	0.387	0.682	1.100	0.013	0.023	0.037	D	1.0	QB	22
		(HL)	0.373	0.742	1.365	0.010	0.017	0.029	C	1.0		
	R → QB	(HH)	0.265	0.500	0.781	0.013	0.023	0.037	R	2.2		
	Set up time	D	0.470		1.280							
	Hold time	D	0.140		0.070							
	Release time	R	0.150		0.750							
	Removal time	R	0.000		0.000							
	Min Pulse	C	0.799		1.564							
	Min Pulse	R	0.683		1.121							
F642NBP	C → QB	(HH)	0.453	0.789	1.271	0.006	0.012	0.019	D	1.0	QB	43
		(HL)	0.439	0.893	1.759	0.005	0.009	0.016	C	1.0		
	R → QB	(HH)	0.324	0.606	0.955	0.006	0.012	0.019	R	2.2		
	Set up time	D	0.470		1.220							
	Hold time	D	0.140		0.070							

FUNCTION BLOCK

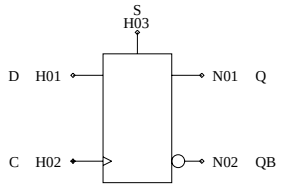
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	R	0.170		0.710							
	Removal time	R	0.000		0.000							
	Min Pulse	C	0.859		1.917							
	Min Pulse	R	0.736		1.275							

[MEMO]

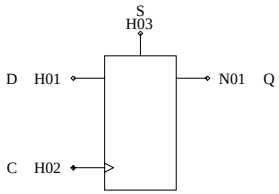
FUNCTION BLOCK

Function	D-F/F WITH S							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F643	9	F643NQ	8	F643NB	8							
x2	F643NP	11	F643NQP	9	F643NBP	9							
x4													

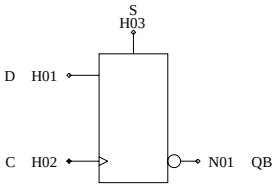
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	S	Q	QB
0	↗	0	0	1
1	↗	0	1	0
X	↘	0	Hold	
X	X	1	1	0

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F643	C → Q	(HH)	0.380	0.671	1.108	0.013	0.023	0.037	D	1.0	Q	23
		(HL)	0.530	1.021	1.762	0.010	0.016	0.026	C	1.0	QB	23
	C → QB	(HH)	0.640	1.220	2.103	0.012	0.022	0.036	S	2.2		
		(HL)	0.504	0.916	1.547	0.009	0.014	0.023				
	S → Q	(HH)	0.183	0.291	0.429	0.013	0.023	0.037				
	S → QB	(HL)	0.315	0.661	1.077	0.009	0.015	0.024				
	Set up time	D	0.470		0.740							
	Hold time	D	0.140		0.050							
	Release time	S	0.000		0.000							
	Removal time	S	0.210		0.830							
	Min Pulse	C	1.075		2.504							
	Min Pulse	S	0.735		1.382							
F643NP	C → Q	(HH)	0.424	0.746	1.231	0.006	0.011	0.018	D	1.0	Q	46
		(HL)	0.616	1.206	2.104	0.005	0.008	0.014	C	1.0	QB	45
	C → QB	(HH)	0.802	1.549	2.700	0.006	0.011	0.018	S	2.2		
		(HL)	0.610	1.113	1.887	0.005	0.007	0.012				
	S → Q	(HH)	0.228	0.355	0.533	0.006	0.011	0.018				
	S → QB	(HL)	0.424	0.842	1.387	0.005	0.008	0.013				
	Set up time	D	0.470		0.740							
	Hold time	D	0.140		0.050							
	Release time	S	0.000		0.000							
	Removal time	S	0.210		0.830							
	Min Pulse	C	1.240		3.110							
	Min Pulse	S	0.833		1.675							
F643NQ	C → Q	(HH)	0.379	0.668	1.104	0.012	0.023	0.037	D	1.0	Q	22
		(HL)	0.530	1.022	1.758	0.010	0.016	0.026	C	1.0		
	S → Q	(HH)	0.181	0.289	0.426	0.012	0.023	0.037	S	2.2		
	Set up time	D	0.470		0.740							
	Hold time	D	0.140		0.050							
	Release time	S	0.000		0.000							
	Removal time	S	0.210		0.830							
	Min Pulse	C	0.927		2.016							
	Min Pulse	S	0.607		0.798							
F643NQP	C → Q	(HH)	0.414	0.734	1.219	0.006	0.011	0.018	D	1.0	Q	45
		(HL)	0.614	1.202	2.098	0.005	0.008	0.014	C	1.0		
	S → Q	(HH)	0.219	0.343	0.518	0.006	0.011	0.018	S	2.2		
	Set up time	D	0.470		0.740							
	Hold time	D	0.140		0.050							
	Release time	S	0.000		0.000							
	Removal time	S	0.210		0.830							
	Min Pulse	C	1.003		2.321							
	Min Pulse	S	0.633		0.881							
F643NB	C → QB	(HH)	0.383	0.677	1.094	0.013	0.023	0.037	D	1.0	QB	22
		(HL)	0.356	0.681	1.180	0.010	0.016	0.026	C	1.0		
	S → QB	(HL)	0.347	0.863	1.537	0.009	0.016	0.025	S	2.2		
	Set up time	D	0.480		0.760							
	Hold time	D	0.140		0.060							
	Release time	S	0.000		0.000							
	Removal time	S	0.170		0.780							
	Min Pulse	C	0.794		1.431							
	Min Pulse	S	0.762		1.795							
F643NBP	C → QB	(HH)	0.445	0.780	1.261	0.007	0.012	0.019	D	1.0	QB	44
		(HL)	0.406	0.803	1.483	0.005	0.008	0.014	C	1.0		
	S → QB	(HL)	0.404	0.987	1.791	0.005	0.008	0.014	S	2.2		
	Set up time	D	0.480		0.780							
	Hold time	D	0.140		0.060							

FUNCTION BLOCK

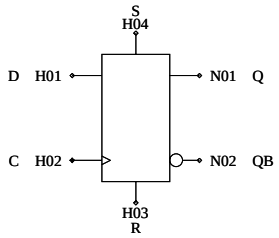
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	S	0.000		0.000							
	Removal time	S	0.150		0.760							
	Min Pulse	C	0.851		1.697							
	Min Pulse	S	0.815		2.021							

[MEMO]

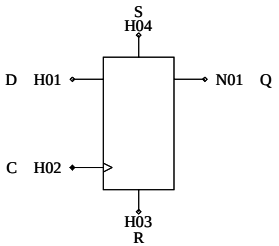
FUNCTION BLOCK

Function	D-F/F WITH R,S								SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L614	7		
x1	F644	10	F644NQ	9	F644NB	9	F614	10				
x2	F644NP	12	F644NQP	10	F644NBP	10						
x4												

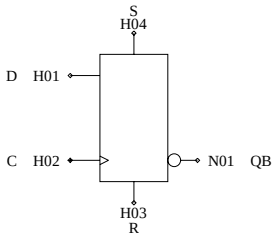
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	R	S	Q	QB	
0	↗	0	0	0	1	
1	↗	0	0	1	0	
X	↘	0	0	Hold		
X	X	0	1	1	0	
X	X	1	0	0	1	
X	X	1	1	1	1	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L614	C → Q	(HH)	0.392	0.723	1.197	0.043	0.088	0.147	D	3.1	Q	4
		(HL)	0.341	0.614	1.045	0.017	0.027	0.046	C	1.0		
	R → Q	(HL)	0.161	0.164	0.231	0.012	0.026	0.043	R	2.3		
	S → Q	(HH)	0.323	0.564	0.911	0.044	0.088	0.148	S	2.1		
	Set up time	D	0.680		1.580							
	Hold time	D	0.334		0.241							
	Release time	R	1.060		1.182							
	Release time	S	1.250		1.693							
	Removal time	R	0.641		0.703							
	Removal time	S	0.483		0.294							
	Min Pulse	C	1.074		2.065							
	Min Pulse	R	0.866		1.692							
	Min Pulse	S	1.128		2.300							
F644	C → Q	(HH)	0.413	0.743	1.265	0.012	0.023	0.036	D	1.0	Q	23
		(HL)	0.564	1.082	1.870	0.010	0.016	0.027	C	1.0	QB	22
	C → QB	(HH)	0.664	1.276	2.214	0.012	0.022	0.036	R	2.2		
		(HL)	0.629	1.201	2.108	0.010	0.016	0.026	S	2.3		
	R → Q	(HL)	0.475	0.932	1.599	0.010	0.016	0.026				
	R → QB	(HH)	0.184	0.352	0.529	0.012	0.023	0.037				
	S → Q	(HH)	0.191	0.301	0.457	0.012	0.023	0.036				
	S → QB	(HL)	0.404	1.005	1.734	0.010	0.017	0.028				
	Set up time	D	0.733		1.615							
	Hold time	D	0.193		0.010							
	Release time	R	1.241		1.653							
	Release time	S	1.079		1.188							
	Removal time	R	0.529		0.358							
	Removal time	S	0.663		0.730							
	Min Pulse	C	1.325		2.690							
	Min Pulse	R	1.242		2.646							
	Min Pulse	S	1.133		2.745							
F614	C → Q	(HH)	0.413	0.743	1.265	0.012	0.023	0.036	D	1.0	Q	23
		(HL)	0.564	1.082	1.870	0.010	0.016	0.027	C	1.0	QB	22
	C → QB	(HH)	0.664	1.276	2.214	0.012	0.022	0.036	R	2.2		
		(HL)	0.629	1.201	2.108	0.010	0.016	0.026	S	2.3		
	R → Q	(HL)	0.475	0.932	1.599	0.010	0.016	0.026				
	R → QB	(HH)	0.184	0.352	0.529	0.012	0.023	0.037				
	S → Q	(HH)	0.191	0.301	0.457	0.012	0.023	0.036				
	S → QB	(HL)	0.404	1.005	1.734	0.010	0.017	0.028				
	Set up time	D	0.733		1.615							
	Hold time	D	0.193		0.010							
	Release time	R	1.241		1.653							
	Release time	S	1.079		1.188							
	Removal time	R	0.529		0.358							
	Removal time	S	0.663		0.730							
	Min Pulse	C	1.325		2.690							
	Min Pulse	R	1.242		2.646							
	Min Pulse	S	1.133		2.745							
F644NP	C → Q	(HH)	0.425	0.770	1.312	0.006	0.011	0.018	D	1.0	Q	46
		(HL)	0.589	1.159	2.036	0.005	0.008	0.014	C	1.0	QB	46
	C → QB	(HH)	0.758	1.485	2.612	0.006	0.011	0.018	R	2.1		
		(HL)	0.725	1.411	2.501	0.005	0.008	0.013	S	2.2		
	R → Q	(HL)	0.515	1.108	1.917	0.005	0.008	0.013				
	R → QB	(HH)	0.219	0.398	0.602	0.006	0.012	0.019				
	S → Q	(HH)	0.214	0.337	0.509	0.006	0.011	0.018				
	S → QB	(HL)	0.513	1.197	2.098	0.005	0.009	0.014				
	Set up time	D	0.480		1.360							

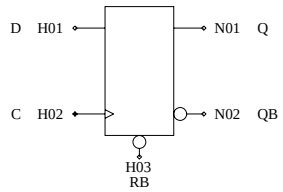
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Hold time	D	0.120		0.030							
	Release time	R	0.150		0.820							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.210		0.850							
	Min Pulse	C	1.199		3.020							
	Min Pulse	R	0.910		2.168							
	Min Pulse	S	0.903		2.314							
F644NQ	C → Q	(HH)	0.381	0.693	1.178	0.012	0.023	0.036	D	1.0	Q	23
		(HL)	0.508	0.988	1.712	0.009	0.015	0.025	C	1.0		
	R → Q	(HL)	0.411	0.798	1.370	0.009	0.015	0.025	R	2.1		
	S → Q	(HH)	0.173	0.278	0.413	0.012	0.023	0.036	S	2.2		
	Set up time	D	0.480		1.350							
	Hold time	D	0.120		0.030							
	Release time	R	0.150		0.820							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.210		0.850							
	Min Pulse	C	0.908		1.973							
	Min Pulse	R	0.819		1.646							
	Min Pulse	S	0.598		0.785							
F644NQP	C → Q	(HH)	0.425	0.772	1.317	0.006	0.011	0.018	D	1.0	Q	45
		(HL)	0.590	1.163	2.043	0.005	0.008	0.014	C	1.0		
	R → Q	(HL)	0.495	0.975	1.710	0.005	0.008	0.013	R	2.1		
	S → Q	(HH)	0.215	0.337	0.511	0.006	0.011	0.018	S	2.2		
	Set up time	D	0.480		1.360							
	Hold time	D	0.120		0.030							
	Release time	R	0.150		0.820							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.210		0.850							
	Min Pulse	C	0.984		2.272							
	Min Pulse	R	0.896		1.953							
	Min Pulse	S	0.630		0.873							
F644NB	C → QB	(HH)	0.361	0.649	1.059	0.013	0.023	0.037	D	1.0	QB	22
		(HL)	0.371	0.742	1.373	0.010	0.017	0.029	C	1.0		
	R → QB	(HH)	0.274	0.474	0.752	0.013	0.023	0.037	R	2.1		
	S → QB	(HL)	0.461	1.159	2.149	0.010	0.017	0.028	S	2.2		
	Set up time	D	0.490		1.280							
	Hold time	D	0.120		0.040							
	Release time	R	0.150		0.760							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.170		0.780							
	Min Pulse	C	0.777		1.574							
	Min Pulse	R	0.691		1.095							
	Min Pulse	S	0.871		2.357							
F644NBP	C → QB	(HH)	0.416	0.745	1.216	0.006	0.012	0.019	D	1.0	QB	44
		(HL)	0.435	0.890	1.759	0.005	0.009	0.016	C	1.0		
	R → QB	(HH)	0.336	0.571	0.915	0.006	0.012	0.019	R	2.1		
	S → QB	(HL)	0.546	1.350	2.554	0.005	0.009	0.015	S	2.2		
	Set up time	D	0.490		1.240							
	Hold time	D	0.120		0.040							
	Release time	R	0.180		0.710							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Removal time	S	0.140		0.750							
	Min Pulse	C	0.829		1.915							
	Min Pulse	R	0.747		1.238							
	Min Pulse	S	0.950		2.725							

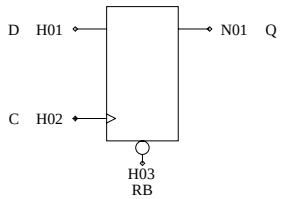
FUNCTION BLOCK

Function	D-F/F WITH RB							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F615	9	F615NQ	8	F615NB	8							
x2	F615NP	11	F615NQP	9	F615NBP	9							
x4													

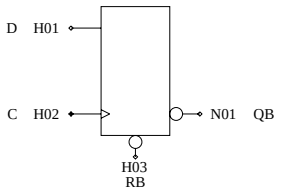
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	RB	Q	QB
0	↗	1	0	1
1	↗	1	1	0
X	↘	1	Hold	
X	X	0	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F615	C → Q	(HH)	0.424	0.768	1.289	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.459	0.844	1.418	0.009	0.015	0.025	C	1.0	QB	22
	C → QB	(HH)	0.557	1.022	1.718	0.012	0.023	0.036	RB	2.1		
		(HL)	0.552	1.023	1.743	0.010	0.016	0.026				
	RB → Q	(LL)	0.217	0.384	0.644	0.009	0.015	0.025				
	RB → QB	(LH)	0.326	0.645	1.070	0.012	0.023	0.036				
	Set up time	D	0.541		1.046							
	Hold time	D	0.257		0.064							
	Release time	RB	1.001		1.043							
	Removal time	RB	0.712		0.834							
	Min Pulse	C	1.248		2.488							
	Min Pulse	RB	1.082		2.292							
F615NP	C → Q	(HH)	0.480	0.869	1.453	0.006	0.012	0.019	D	1.0	Q	45
		(HL)	0.506	0.939	1.582	0.005	0.007	0.012	C	1.0	QB	45
	C → QB	(HH)	0.669	1.231	2.076	0.006	0.011	0.018	RB	2.2		
		(HL)	0.676	1.259	2.150	0.005	0.007	0.012				
	RB → Q	(LL)	0.258	0.475	0.808	0.005	0.007	0.012				
	RB → QB	(LH)	0.444	0.849	1.425	0.006	0.011	0.018				
	Set up time	D	0.470		0.740							
	Hold time	D	0.130		0.050							
	Release time	RB	0.000		0.000							
	Removal time	RB	0.310		0.750							
	Min Pulse	C	1.102		2.479							
	Min Pulse	RB	0.896		1.848							
F615NQ	C → Q	(HH)	0.418	0.756	1.260	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.448	0.830	1.388	0.009	0.015	0.024	C	1.0		
	RB → Q	(LL)	0.206	0.373	0.621	0.009	0.014	0.024	RB	2.2		
	Set up time	D	0.470		0.750							
	Hold time	D	0.130		0.050							
	Release time	RB	0.000		0.000							
	Removal time	RB	0.310		0.750							
	Min Pulse	C	0.861		1.707							
	Min Pulse	RB	0.638		0.999							
F615NQP	C → Q	(HH)	0.469	0.857	1.439	0.006	0.012	0.019	D	1.0	Q	43
		(HL)	0.501	0.931	1.570	0.005	0.007	0.012	C	1.0		
	RB → Q	(LL)	0.256	0.471	0.802	0.005	0.007	0.012	RB	2.2		
	Set up time	D	0.470		0.740							
	Hold time	D	0.130		0.050							
	Release time	RB	0.000		0.000							
	Removal time	RB	0.310		0.750							
	Min Pulse	C	0.905		1.861							
	Min Pulse	RB	0.681		1.153							
F615NB	C → QB	(HH)	0.384	0.677	1.094	0.013	0.023	0.037	D	1.0	QB	22
		(HL)	0.353	0.673	1.167	0.010	0.016	0.026	C	1.0		
	RB → QB	(LH)	0.353	0.843	1.448	0.013	0.023	0.037	RB	2.2		
	Set up time	D	0.470		0.740							
	Hold time	D	0.140		0.060							
	Release time	RB	0.000		0.000							
	Removal time	RB	0.300		0.720							
	Min Pulse	C	0.795		1.431							
	Min Pulse	RB	0.790		1.852							
F615NBP	C → QB	(HH)	0.446	0.780	1.261	0.006	0.012	0.019	D	1.0	QB	43
		(HL)	0.404	0.796	1.469	0.005	0.009	0.014	C	1.0		
	RB → QB	(LH)	0.417	0.955	1.634	0.006	0.012	0.019	RB	2.2		
	Set up time	D	0.480		0.760							
	Hold time	D	0.140		0.060							

FUNCTION BLOCK

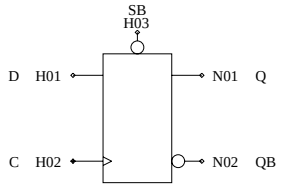
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	RB	0.000		0.000							
	Removal time	RB	0.270		0.680							
	Min Pulse	C	0.851		1.686							
	Min Pulse	RB	0.849		2.013							

[MEMO]

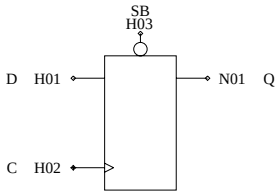
FUNCTION BLOCK

Function	D-F/F WITH SB							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F616	9	F616NQ	8	F616NB	8							
x2	F616NP	11	F616NQP	9	F616NBP	9							
x4													

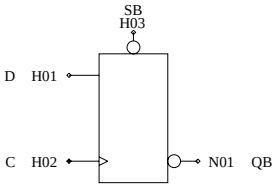
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	SB	Q	QB
0	↗	1	0	1
1	↗	1	1	0
X	↘	1	Hold	
X	X	0	1	0

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F616	C → Q	(HH)	0.384	0.678	1.131	0.012	0.023	0.037	D	1.0	Q	22
		(HL)	0.472	0.876	1.475	0.009	0.015	0.025	C	1.0	QB	22
	C → QB	(HH)	0.610	1.145	1.937	0.012	0.023	0.036	SB	2.1		
		(HL)	0.508	0.924	1.572	0.010	0.016	0.026				
	SB → Q	(LH)	0.397	0.772	1.374	0.012	0.023	0.036				
	SB → QB	(LL)	0.213	0.486	0.809	0.010	0.017	0.027				
	Set up time	D	0.524		1.017							
	Hold time	D	0.264		0.130							
	Release time	SB	1.168		1.392							
	Removal time	SB	0.572		0.554							
	Min Pulse	C	1.333		2.755							
	Min Pulse	SB	1.179		2.600							
F616NP	C → Q	(HH)	0.423	0.740	1.223	0.006	0.011	0.018	D	1.0	Q	46
		(HL)	0.512	0.961	1.621	0.005	0.007	0.012	C	1.0	QB	45
	C → QB	(HH)	0.730	1.380	2.337	0.006	0.011	0.018	SB	2.2		
		(HL)	0.611	1.115	1.892	0.004	0.007	0.012				
	SB → Q	(LH)	0.434	0.992	1.742	0.006	0.011	0.018				
	SB → QB	(LL)	0.257	0.570	0.970	0.005	0.008	0.012				
	Set up time	D	0.490		0.850							
	Hold time	D	0.150		0.060							
	Release time	SB	0.000		0.000							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	1.157		2.695							
	Min Pulse	SB	0.884		2.158							
F616NQ	C → Q	(HH)	0.377	0.665	1.100	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.456	0.851	1.430	0.009	0.014	0.023	C	1.0		
	SB → Q	(LH)	0.352	0.704	1.217	0.013	0.023	0.037	SB	2.2		
	Set up time	D	0.490		0.840							
	Hold time	D	0.150		0.060							
	Release time	SB	0.000		0.000							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.867		1.749							
	Min Pulse	SB	0.796		1.647							
F616NQP	C → Q	(HH)	0.424	0.742	1.228	0.006	0.012	0.018	D	1.0	Q	44
		(HL)	0.513	0.962	1.626	0.005	0.007	0.012	C	1.0		
	SB → Q	(LH)	0.402	0.789	1.353	0.006	0.012	0.018	SB	2.2		
	Set up time	D	0.490		0.840							
	Hold time	D	0.150		0.060							
	Release time	SB	0.000		0.000							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.917		1.916							
	Min Pulse	SB	0.842		1.769							
F616NB	C → QB	(HH)	0.405	0.729	1.186	0.013	0.024	0.038	D	1.0	QB	22
		(HL)	0.350	0.674	1.174	0.010	0.016	0.026	C	1.0		
	SB → QB	(LL)	0.298	0.627	1.163	0.009	0.015	0.025	SB	2.2		
	Set up time	D	0.500		0.860							
	Hold time	D	0.150		0.070							
	Release time	SB	0.000		0.000							
	Removal time	SB	0.040		0.160							
	Min Pulse	C	0.813		1.496							
	Min Pulse	SB	0.712		1.475							
F616NBP	C → QB	(HH)	0.479	0.857	1.397	0.007	0.012	0.019	D	1.0	QB	43
		(HL)	0.400	0.794	1.473	0.005	0.008	0.014	C	1.0		
	SB → QB	(LL)	0.354	0.749	1.415	0.005	0.008	0.013	SB	2.2		
	Set up time	D	0.510		0.880							
	Hold time	D	0.150		0.060							

FUNCTION BLOCK

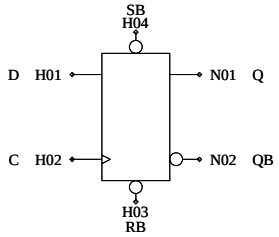
Block type	Switching speed											
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	SB	0.000		0.000							
	Removal time	SB	0.030		0.140							
	Min Pulse	C	0.881		1.689							
	Min Pulse	SB	0.764		1.696							

[MEMO]

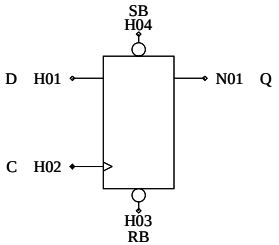
FUNCTION BLOCK

Function	D-F/F WITH RB,SB								SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L617	7		
x1	F647	10	F647NQ	9	F647NB	9	F617	10				
x2	F647NP	12	F647NQP	10	F647NBP	10						
x4												

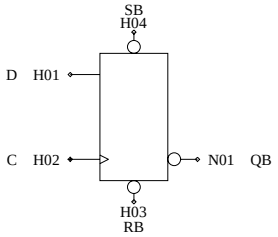
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	RB	SB	Q	QB	
0	↗	1	1	0	1	
1	↗	1	1	1	0	
X	↘	1	1	Hold		
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L617	C → Q	(HH)	0.373	0.674	1.097	0.025	0.045	0.073	D	3.1	Q	12
		(HL)	0.336	0.597	0.991	0.025	0.045	0.078	C	1.0		
	RB → Q	(LL)	0.301	0.616	1.090	0.026	0.046	0.079	RB	2.2		
	SB → Q	(LH)	0.171	0.176	0.264	0.014	0.045	0.072	SB	2.3		
	Set up time	D	0.382		0.873							
	Hold time	D	0.374		0.314							
	Release time	RB	1.154		1.358							
	Release time	SB	0.984		1.039							
	Removal time	RB	0.561		0.560							
	Removal time	SB	0.703		0.815							
	Min Pulse	C	1.098		2.092							
	Min Pulse	RB	1.155		2.551							
	Min Pulse	SB	0.895		1.953							
F647	C → Q	(HH)	0.428	0.781	1.307	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.477	0.885	1.480	0.009	0.015	0.025	C	1.0	QB	22
	C → QB	(HH)	0.620	1.165	1.960	0.012	0.023	0.036	RB	2.3		
		(HL)	0.560	1.048	1.784	0.009	0.015	0.024	SB	2.3		
	RB → Q	(LL)	0.212	0.379	0.627	0.009	0.015	0.024				
	RB → QB	(LH)	0.356	0.783	1.302	0.012	0.023	0.037				
	SB → Q	(LH)	0.413	0.883	1.557	0.012	0.023	0.037				
	SB → QB	(LL)	0.218	0.498	0.833	0.009	0.016	0.026				
	Set up time	D	0.447		1.019							
	Hold time	D	0.278		0.100							
	Release time	RB	1.004		1.046							
	Release time	SB	1.162		1.344							
	Removal time	RB	0.725		0.842							
	Removal time	SB	0.593		0.603							
	Min Pulse	C	1.351		2.748							
	Min Pulse	RB	1.120		2.570							
	Min Pulse	SB	1.216		2.768							
F617	C → Q	(HH)	0.428	0.781	1.307	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.477	0.885	1.480	0.009	0.015	0.025	C	1.0	QB	22
	C → QB	(HH)	0.620	1.165	1.960	0.012	0.023	0.036	RB	2.3		
		(HL)	0.560	1.048	1.784	0.009	0.015	0.024	SB	2.3		
	RB → Q	(LL)	0.212	0.379	0.627	0.009	0.015	0.024				
	RB → QB	(LH)	0.356	0.783	1.302	0.012	0.023	0.037				
	SB → Q	(LH)	0.413	0.883	1.557	0.012	0.023	0.037				
	SB → QB	(LL)	0.218	0.498	0.833	0.009	0.016	0.026				
	Set up time	D	0.447		1.019							
	Hold time	D	0.278		0.100							
	Release time	RB	1.004		1.046							
	Release time	SB	1.162		1.344							
	Removal time	RB	0.725		0.842							
	Removal time	SB	0.593		0.603							
	Min Pulse	C	1.351		2.748							
	Min Pulse	RB	1.120		2.570							
	Min Pulse	SB	1.216		2.768							
F647NP	C → Q	(HH)	0.459	0.843	1.419	0.006	0.012	0.019	D	1.0	Q	45
		(HL)	0.499	0.946	1.602	0.005	0.008	0.012	C	1.0	QB	45
	C → QB	(HH)	0.715	1.361	2.316	0.006	0.011	0.018	RB	2.2		
		(HL)	0.652	1.234	2.124	0.004	0.007	0.012	SB	2.2		
	RB → Q	(LL)	0.253	0.460	0.783	0.005	0.007	0.012				
	RB → QB	(LH)	0.469	0.997	1.684	0.006	0.012	0.019				
	SB → Q	(LH)	0.455	1.113	1.960	0.006	0.012	0.018				
	SB → QB	(LL)	0.260	0.576	0.984	0.004	0.008	0.013				
	Set up time	D	0.510		0.880							

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Hold time	D	0.130		0.030							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	1.145		2.673							
	Min Pulse	RB	0.915		2.060							
	Min Pulse	SB	0.902		2.355							
F647NQ	C → Q	(HH)	0.405	0.744	1.247	0.013	0.023	0.037	D	1.0	Q	22
		(HL)	0.448	0.843	1.418	0.009	0.014	0.023	C	1.0		
	RB → Q	(LL)	0.205	0.368	0.612	0.009	0.014	0.023	RB	2.2		
	SB → Q	(LH)	0.381	0.758	1.331	0.013	0.023	0.037	SB	2.2		
	Set up time	D	0.510		0.880							
	Hold time	D	0.130		0.030							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.862		1.742							
	Min Pulse	RB	0.635		0.990							
	Min Pulse	SB	0.823		1.744							
F647NQP	C → Q	(HH)	0.460	0.846	1.425	0.006	0.012	0.019	D	1.0	Q	44
		(HL)	0.499	0.948	1.606	0.005	0.008	0.012	C	1.0		
	RB → Q	(LL)	0.253	0.463	0.788	0.005	0.007	0.012	RB	2.2		
	SB → Q	(LH)	0.438	0.867	1.516	0.006	0.012	0.019	SB	2.2		
	Set up time	D	0.510		0.880							
	Hold time	D	0.130		0.030							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.909		1.901							
	Min Pulse	RB	0.678		1.140							
	Min Pulse	SB	0.877		1.915							
F647NB	C → QB	(HH)	0.393	0.714	1.167	0.013	0.024	0.038	D	1.0	QB	22
		(HL)	0.344	0.667	1.165	0.010	0.016	0.026	C	1.0		
	RB → QB	(LH)	0.400	0.965	1.680	0.013	0.024	0.038	RB	2.2		
	SB → QB	(LL)	0.305	0.624	1.164	0.009	0.015	0.025	SB	2.2		
	Set up time	D	0.520		0.900							
	Hold time	D	0.130		0.050							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.290		0.720							
	Removal time	SB	0.040		0.160							
	Min Pulse	C	0.804		1.480							
	Min Pulse	RB	0.832		2.056							
	Min Pulse	SB	0.719		1.469							
F647NBP	C → QB	(HH)	0.462	0.836	1.370	0.006	0.012	0.019	D	1.0	QB	43
		(HL)	0.393	0.784	1.456	0.005	0.008	0.014	C	1.0		
	RB → QB	(LH)	0.473	1.100	1.913	0.006	0.012	0.019	RB	2.2		
	SB → QB	(LL)	0.360	0.743	1.409	0.005	0.008	0.013	SB	2.2		
	Set up time	D	0.520		0.920							
	Hold time	D	0.130		0.040							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.260		0.670							

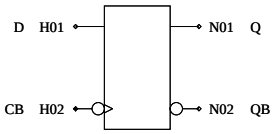
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Removal time	SB	0.030		0.140							
	Min Pulse	C	0.868		1.671							
	Min Pulse	RB	0.901		2.262							
	Min Pulse	SB	0.769		1.686							

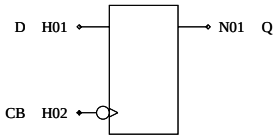
FUNCTION BLOCK

Function	D-F/F (CB)								SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L631	5		
x1	F661	8	F661NQ	7	F661NB	7	F631	8				
x2	F661NP	10	F661NQP	8	F661NBP	8						
x4												

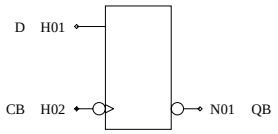
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	C	Q	QB
0	↘	0	1
1	↘	1	0
X	↗	Hold	

X:Irrelevant

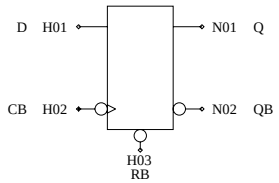
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L631	CB → Q	(LH)	0.318	0.557	0.915	0.025	0.045	0.072	D	3.1	Q	10
		(LL)	0.352	0.665	1.186	0.017	0.027	0.045	CB	1.0		
	Set up time	D	0.364		0.473							
	Hold time	D	0.421		0.533							
	Min Pulse	CB	1.118		2.435							
F661	CB → Q	(LH)	0.420	0.788	1.394	0.012	0.023	0.036	D	1.0	Q	22
		(LL)	0.411	0.751	1.269	0.009	0.015	0.025	CB	1.0	QB	23
	CB → QB	(LH)	0.509	0.931	1.578	0.012	0.023	0.036				
		(LL)	0.538	1.031	1.838	0.009	0.015	0.024				
	Set up time	D	0.408		0.827							
	Hold time	D	0.274		0.248							
	Min Pulse	CB	1.219		2.821							
F631	CB → Q	(LH)	0.420	0.788	1.394	0.012	0.023	0.036	D	1.0	Q	22
		(LL)	0.411	0.751	1.269	0.009	0.015	0.025	CB	1.0	QB	23
	CB → QB	(LH)	0.509	0.931	1.578	0.012	0.023	0.036				
		(LL)	0.538	1.031	1.838	0.009	0.015	0.024				
	Set up time	D	0.408		0.827							
	Hold time	D	0.274		0.248							
	Min Pulse	CB	1.219		2.821							
F661NP	CB → Q	(LH)	0.450	0.835	1.474	0.006	0.011	0.018	D	1.0	Q	46
		(LL)	0.446	0.824	1.411	0.005	0.008	0.012	CB	1.0	QB	46
	CB → QB	(LH)	0.600	1.100	1.882	0.006	0.011	0.018				
		(LL)	0.614	1.177	2.101	0.004	0.007	0.012				
	Set up time	D	0.340		0.740							
	Hold time	D	0.420		0.480							
	Min Pulse	CB	1.048		2.475							
F661NQ	CB → Q	(LH)	0.406	0.759	1.353	0.012	0.023	0.037	D	1.0	Q	22
		(LL)	0.394	0.727	1.235	0.009	0.014	0.023	CB	1.0		
	Set up time	D	0.340		0.740							
	Hold time	D	0.420		0.480							
	Min Pulse	CB	0.850		1.782							
F661NQP	CB → Q	(LH)	0.448	0.833	1.472	0.006	0.011	0.018	D	1.0	Q	44
		(LL)	0.448	0.829	1.419	0.005	0.008	0.012	CB	1.0		
	Set up time	D	0.340		0.740							
	Hold time	D	0.420		0.480							
	Min Pulse	CB	0.889		1.893							
F661NB	CB → QB	(LH)	0.346	0.611	1.009	0.013	0.023	0.037	D	1.0	QB	22
		(LL)	0.363	0.709	1.326	0.010	0.016	0.026	CB	1.0		
	Set up time	D	0.340		0.740							
	Hold time	D	0.430		0.490							
	Min Pulse	CB	0.778		1.634							
F661NBP	CB → QB	(LH)	0.408	0.722	1.199	0.006	0.012	0.019	D	1.0	QB	43
		(LL)	0.408	0.808	1.557	0.005	0.008	0.014	CB	1.0		
	Set up time	D	0.340		0.740							
	Hold time	D	0.430		0.500							
	Min Pulse	CB	0.836		1.830							

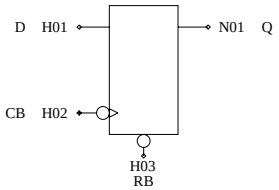
FUNCTION BLOCK

Function	D-F/F (CB) WITH RB						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F665	9	F665NQ	8	F665NB	8						
x2	F665NP	11	F665NQP	9	F665NBP	9						
x4												

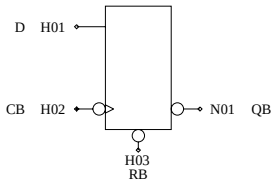
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	CB	RB	Q	QB
0	↘	1	0	1
1	↘	1	1	0
X	↗	1	Hold	
X	X	0	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F665	CB → Q		(LH)	0.469	0.885	1.558	0.013	0.023	0.037	D	1.0	Q	22
			(LL)	0.421	0.767	1.294	0.009	0.015	0.024	CB	1.0	QB	23
	CB → QB		(LH)	0.526	0.951	1.599	0.012	0.023	0.036	RB	2.2		
			(LL)	0.597	1.140	2.016	0.009	0.014	0.023				
	RB → Q		(LL)	0.207	0.374	0.623	0.009	0.015	0.024				
	RB → QB		(LH)	0.328	0.638	1.051	0.013	0.023	0.037				
	Set up time	D		0.340		0.740							
	Hold time	D		0.430		0.500							
	Release time	RB		0.000		0.000							
	Removal time	RB		0.500		1.090							
	Min Pulse	CB		1.034		2.420							
	Min Pulse	RB		0.775		1.472							
F665NP	CB → Q		(LH)	0.525	0.993	1.746	0.006	0.012	0.019	D	1.0	Q	45
			(LL)	0.475	0.872	1.483	0.005	0.007	0.012	CB	1.0	QB	45
	CB → QB		(LH)	0.638	1.163	1.974	0.006	0.011	0.018	RB	2.2		
			(LL)	0.718	1.377	2.434	0.005	0.007	0.012				
	RB → Q		(LL)	0.258	0.475	0.808	0.005	0.007	0.012				
	RB → QB		(LH)	0.444	0.849	1.423	0.006	0.011	0.018				
	Set up time	D		0.340		0.740							
	Hold time	D		0.430		0.500							
	Release time	RB		0.000		0.000							
	Removal time	RB		0.500		1.100							
	Min Pulse	CB		1.151		2.824							
	Min Pulse	RB		0.895		1.844							
F665NQ	CB → Q		(LH)	0.467	0.881	1.552	0.013	0.023	0.037	D	1.0	Q	22
			(LL)	0.421	0.767	1.293	0.009	0.015	0.024	CB	1.0		
	RB → Q		(LL)	0.206	0.373	0.620	0.009	0.015	0.024	RB	2.2		
	Set up time	D		0.340		0.740							
	Hold time	D		0.430		0.500							
	Release time	RB		0.000		0.000							
	Removal time	RB		0.500		1.090							
	Min Pulse	CB		0.904		1.962							
	Min Pulse	RB		0.638		0.999							
F665NQP	CB → Q		(LH)	0.521	0.985	1.737	0.006	0.012	0.019	D	1.0	Q	43
			(LL)	0.475	0.871	1.480	0.005	0.007	0.012	CB	1.0		
	RB → Q		(LL)	0.256	0.471	0.803	0.005	0.007	0.012	RB	2.2		
	Set up time	D		0.340		0.740							
	Hold time	D		0.430		0.500							
	Release time	RB		0.000		0.000							
	Removal time	RB		0.500		1.100							
	Min Pulse	CB		0.956		2.129							
	Min Pulse	RB		0.681		1.153							
F665NB	CB → QB		(LH)	0.373	0.646	1.057	0.013	0.023	0.037	D	1.0	QB	22
			(LL)	0.375	0.727	1.352	0.010	0.016	0.026	CB	1.0		
	RB → QB		(LH)	0.353	0.842	1.447	0.013	0.023	0.037	RB	2.2		
	Set up time	D		0.340		0.740							
	Hold time	D		0.430		0.520							
	Release time	RB		0.000		0.000							
	Removal time	RB		0.480		1.030							
	Min Pulse	CB		0.801		1.665							
	Min Pulse	RB		0.789		1.853							
F665NBP	CB → QB		(LH)	0.441	0.767	1.258	0.006	0.012	0.019	D	1.0	QB	43
			(LL)	0.421	0.829	1.585	0.005	0.009	0.014	CB	1.0		
	RB → QB		(LH)	0.417	0.954	1.633	0.006	0.012	0.019	RB	2.2		
	Set up time	D		0.340		0.740							
	Hold time	D		0.440		0.520							

FUNCTION BLOCK

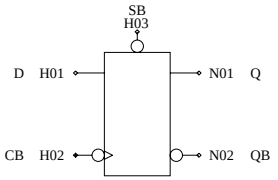
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	RB	0.000		0.000							
	Removal time	RB	0.460		0.940							
	Min Pulse	CB	0.864		1.864							
	Min Pulse	RB	0.849		2.012							

[MEMO]

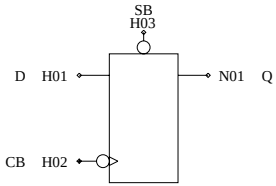
FUNCTION BLOCK

Function	D-F/F (CB) WITH SB						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F666	9	F666NQ	8	F666NB	8						
x2	F666NP	11	F666NQP	9	F666NBP	9						
x4												

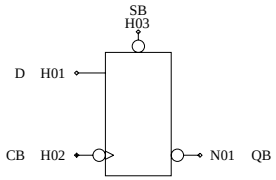
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	CB	SB	Q	QB
0	↘	1	0	1
1	↘	1	1	0
X	↗	1	Hold	
X	X	0	1	0

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F666	CB → Q		(LH)	0.425	0.785	1.384	0.013	0.023	0.037	D	1.0	Q	23
			(LL)	0.422	0.776	1.318	0.009	0.015	0.024	CB	1.0	QB	22
	CB → QB		(LH)	0.563	1.048	1.777	0.012	0.023	0.036	SB	2.2		
			(LL)	0.551	1.037	1.835	0.009	0.014	0.023				
	SB → Q		(LH)	0.387	0.767	1.348	0.012	0.023	0.037				
	SB → QB		(LL)	0.204	0.465	0.781	0.009	0.015	0.024				
	Set up time	D		0.360		0.830							
	Hold time	D		0.440		0.510							
	Release time	SB		0.000		0.000							
	Removal time	SB		0.240		0.330							
	Min Pulse	CB		1.008		2.237							
	Min Pulse	SB		0.836		1.775							
F666NP	CB → Q		(LH)	0.473	0.864	1.517	0.006	0.011	0.018	D	1.0	Q	46
			(LL)	0.478	0.886	1.509	0.005	0.007	0.012	CB	1.0	QB	45
	CB → QB		(LH)	0.697	1.305	2.227	0.006	0.011	0.018	SB	2.2		
			(LL)	0.660	1.238	2.185	0.004	0.007	0.012				
	SB → Q		(LH)	0.434	0.992	1.743	0.006	0.011	0.018				
	SB → QB		(LL)	0.257	0.570	0.971	0.004	0.008	0.012				
	Set up time	D		0.360		0.830							
	Hold time	D		0.440		0.510							
	Release time	SB		0.000		0.000							
	Removal time	SB		0.240		0.330							
	Min Pulse	CB		1.141		2.646							
	Min Pulse	SB		0.883		2.158							
F666NQ	CB → Q		(LH)	0.423	0.781	1.382	0.013	0.023	0.037	D	1.0	Q	22
			(LL)	0.423	0.778	1.318	0.009	0.014	0.023	CB	1.0		
	SB → Q		(LH)	0.353	0.703	1.216	0.012	0.023	0.037	SB	2.2		
	Set up time	D		0.360		0.830							
	Hold time	D		0.440		0.510							
	Release time	SB		0.000		0.000							
	Removal time	SB		0.240		0.330							
	Min Pulse	CB		0.863		1.808							
	Min Pulse	SB		0.796		1.645							
F666NQP	CB → Q		(LH)	0.471	0.861	1.512	0.006	0.012	0.018	D	1.0	Q	44
			(LL)	0.480	0.890	1.517	0.005	0.007	0.012	CB	1.0		
	SB → Q		(LH)	0.401	0.789	1.351	0.006	0.012	0.019	SB	2.2		
	Set up time	D		0.360		0.830							
	Hold time	D		0.440		0.510							
	Release time	SB		0.000		0.000							
	Removal time	SB		0.240		0.330							
	Min Pulse	CB		0.908		1.924							
	Min Pulse	SB		0.842		1.768							
F666NB	CB → QB		(LH)	0.390	0.693	1.143	0.013	0.024	0.038	D	1.0	QB	22
			(LL)	0.370	0.718	1.341	0.010	0.016	0.026	CB	1.0		
	SB → QB		(LL)	0.298	0.627	1.162	0.009	0.015	0.025	SB	2.2		
	Set up time	D		0.360		0.820							
	Hold time	D		0.440		0.520							
	Release time	SB		0.000		0.000							
	Removal time	SB		0.230		0.320							
	Min Pulse	CB		0.815		1.651							
	Min Pulse	SB		0.712		1.473							
F666NBP	CB → QB		(LH)	0.471	0.838	1.392	0.007	0.012	0.019	D	1.0	QB	43
			(LL)	0.416	0.820	1.578	0.005	0.008	0.014	CB	1.0		
	SB → QB		(LL)	0.354	0.748	1.414	0.005	0.008	0.013	SB	2.2		
	Set up time	D		0.370		0.820							
	Hold time	D		0.450		0.530							

FUNCTION BLOCK

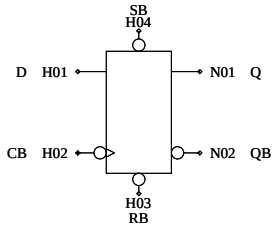
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	SB	0.000		0.000							
	Removal time	SB	0.230		0.310							
	Min Pulse	CB	0.890		1.852							
	Min Pulse	SB	0.764		1.694							

[MEMO]

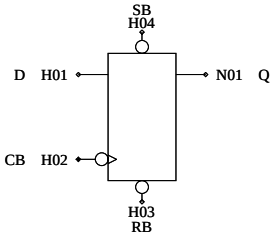
FUNCTION BLOCK

Function	D-F/F (CB) WITH RB,SB										SSI Family	
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L637	7		
x1	F667	10	F667NQ	9	F667NB	9	F637	10				
x2	F667NP	12	F667NQP	10	F667NBP	10						
x4												

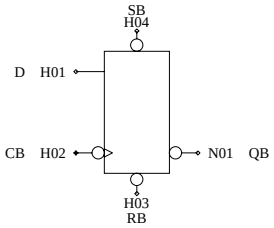
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

D	CB	RB	SB	Q	QB	
0	↘	1	1	0	1	
1	↘	1	1	1	0	
X	↗	1	1	Hold		
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L637	CB → Q	(LH)	0.344	0.612	1.006	0.025	0.045	0.073	D	3.1	Q	12
		(LL)	0.377	0.713	1.263	0.025	0.045	0.078	CB	1.0		
	RB → Q	(LL)	0.301	0.617	1.089	0.026	0.045	0.079	RB	2.1		
	SB → Q	(LH)	0.171	0.176	0.264	0.014	0.045	0.072	SB	2.3		
	Set up time	D	0.360		0.671							
	Hold time	D	0.379		0.442							
	Release time	RB	1.146		1.357							
	Release time	SB	0.976		1.039							
	Removal time	RB	0.566		0.687							
	Removal time	SB	0.708		0.942							
	Min Pulse	CB	1.105		2.377							
	Min Pulse	RB	1.160		2.678							
	Min Pulse	SB	0.900		2.081							
F667	CB → Q	(LH)	0.473	0.898	1.584	0.012	0.023	0.037	D	1.0	Q	22
		(LL)	0.436	0.806	1.367	0.009	0.015	0.025	CB	1.0	QB	22
	CB → QB	(LH)	0.580	1.087	1.849	0.012	0.023	0.036	RB	2.3		
		(LL)	0.605	1.163	2.060	0.009	0.015	0.024	SB	2.3		
	RB → Q	(LL)	0.212	0.375	0.626	0.009	0.015	0.024				
	RB → QB	(LH)	0.356	0.781	1.302	0.012	0.023	0.037				
	SB → Q	(LH)	0.412	0.882	1.558	0.012	0.023	0.037				
	SB → QB	(LL)	0.218	0.497	0.833	0.009	0.015	0.026				
	Set up time	D	0.545		1.040							
	Hold time	D	0.256		0.196							
	Release time	RB	0.960		1.018							
	Release time	SB	1.118		1.316							
	Removal time	RB	0.703		0.936							
	Removal time	SB	0.572		0.698							
	Min Pulse	CB	1.305		2.946							
	Min Pulse	RB	1.098		2.665							
	Min Pulse	SB	1.194		2.864							
F637	CB → Q	(LH)	0.473	0.898	1.584	0.012	0.023	0.037	D	1.0	Q	22
		(LL)	0.436	0.806	1.367	0.009	0.015	0.025	CB	1.0	QB	22
	CB → QB	(LH)	0.580	1.087	1.849	0.012	0.023	0.036	RB	2.3		
		(LL)	0.605	1.163	2.060	0.009	0.015	0.024	SB	2.3		
	RB → Q	(LL)	0.212	0.375	0.626	0.009	0.015	0.024				
	RB → QB	(LH)	0.356	0.781	1.302	0.012	0.023	0.037				
	SB → Q	(LH)	0.412	0.882	1.558	0.012	0.023	0.037				
	SB → QB	(LL)	0.218	0.497	0.833	0.009	0.015	0.026				
	Set up time	D	0.545		1.040							
	Hold time	D	0.256		0.196							
	Release time	RB	0.960		1.018							
	Release time	SB	1.118		1.316							
	Removal time	RB	0.703		0.936							
	Removal time	SB	0.572		0.698							
	Min Pulse	CB	1.305		2.946							
	Min Pulse	RB	1.098		2.665							
	Min Pulse	SB	1.194		2.864							
F667NP	CB → Q	(LH)	0.510	0.966	1.705	0.006	0.012	0.019	D	1.0	Q	45
		(LL)	0.470	0.878	1.499	0.005	0.007	0.012	CB	1.0	QB	45
	CB → QB	(LH)	0.686	1.294	2.214	0.006	0.011	0.018	RB	2.2		
		(LL)	0.701	1.356	2.409	0.004	0.007	0.012	SB	2.2		
	RB → Q	(LL)	0.252	0.460	0.783	0.005	0.007	0.012				
	RB → QB	(LH)	0.469	0.997	1.683	0.006	0.012	0.019				
	SB → Q	(LH)	0.454	1.113	1.960	0.006	0.012	0.018				
	SB → QB	(LL)	0.260	0.576	0.984	0.004	0.008	0.013				
	Set up time	D	0.370		0.840							

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Hold time	D	0.430		0.490							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.510		1.100							
	Removal time	SB	0.250		0.340							
	Min Pulse	CB	1.132		2.787							
	Min Pulse	RB	0.915		2.060							
	Min Pulse	SB	0.902		2.356							
F667NQ	CB → Q	(LH)	0.453	0.861	1.523	0.013	0.023	0.037	D	1.0	Q	22
		(LL)	0.419	0.776	1.318	0.009	0.014	0.023	CB	1.0		
	RB → Q	(LL)	0.205	0.368	0.612	0.009	0.014	0.023	RB	2.2		
	SB → Q	(LH)	0.382	0.758	1.329	0.012	0.023	0.037	SB	2.2		
	Set up time	D	0.370		0.850							
	Hold time	D	0.430		0.490							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.510		1.100							
	Removal time	SB	0.250		0.340							
	Min Pulse	CB	0.891		1.936							
	Min Pulse	RB	0.635		0.990							
	Min Pulse	SB	0.823		1.744							
F667NQP	CB → Q	(LH)	0.508	0.962	1.700	0.006	0.012	0.019	D	1.0	Q	44
		(LL)	0.472	0.883	1.507	0.005	0.008	0.012	CB	1.0		
	RB → Q	(LL)	0.253	0.463	0.788	0.005	0.007	0.012	RB	2.2		
	SB → Q	(LH)	0.438	0.866	1.516	0.006	0.012	0.019	SB	2.2		
	Set up time	D	0.370		0.850							
	Hold time	D	0.430		0.490							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.510		1.100							
	Removal time	SB	0.250		0.340							
	Min Pulse	CB	0.943		2.095							
	Min Pulse	RB	0.678		1.140							
	Min Pulse	SB	0.877		1.914							
F667NB	CB → QB	(LH)	0.380	0.681	1.130	0.013	0.024	0.038	D	1.0	QB	22
		(LL)	0.365	0.711	1.332	0.010	0.016	0.026	CB	1.0		
	RB → QB	(LH)	0.400	0.965	1.680	0.013	0.024	0.038	RB	2.2		
	SB → QB	(LL)	0.305	0.624	1.163	0.009	0.015	0.025	SB	2.2		
	Set up time	D	0.370		0.830							
	Hold time	D	0.430		0.500							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.480		1.030							
	Removal time	SB	0.240		0.320							
	Min Pulse	CB	0.805		1.641							
	Min Pulse	RB	0.832		2.056							
	Min Pulse	SB	0.719		1.468							
F667NBP	CB → QB	(LH)	0.455	0.820	1.368	0.007	0.012	0.019	D	1.0	QB	43
		(LL)	0.410	0.812	1.563	0.005	0.008	0.014	CB	1.0		
	RB → QB	(LH)	0.473	1.099	1.911	0.006	0.012	0.019	RB	2.2		
	SB → QB	(LL)	0.360	0.741	1.407	0.005	0.008	0.013	SB	2.2		
	Set up time	D	0.370		0.840							
	Hold time	D	0.440		0.510							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.450		0.940							

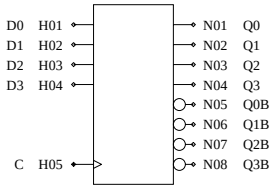
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Removal time	SB	0.230		0.310							
	Min Pulse	CB	0.876		1.838							
	Min Pulse	RB	0.901		2.263							
	Min Pulse	SB	0.769		1.684							

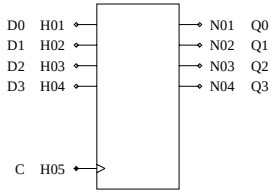
FUNCTION BLOCK

Function	4-BIT D-F/F							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L924	18		
x1	F924	28										
x2												
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

D0	D1	D2	D3	C	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
D0	D1	D2	D3	↗	D0	D1	D2	D3	D0B	D1B	D2B	D3B
X	X	X	X	↘	HOLD				HOLD			

X:Irrelevant

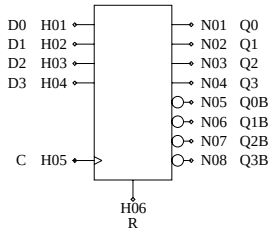
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F924	C → Q0	(HH)	0.456	0.777	1.281	0.012	0.023	0.036		D0	1.0	Q0	22
		(HL)	0.560	1.007	1.696	0.009	0.015	0.025		D1	1.0	Q1	22
	C → Q1	(HH)	0.454	0.774	1.277	0.012	0.023	0.036		D2	1.0	Q2	22
		(HL)	0.555	0.998	1.681	0.010	0.016	0.026		D3	1.0	Q3	22
	C → Q2	(HH)	0.454	0.774	1.277	0.013	0.023	0.037		C	2.0	Q0B	23
		(HL)	0.553	0.995	1.678	0.009	0.015	0.024				Q1B	23
	C → Q3	(HH)	0.456	0.777	1.281	0.012	0.023	0.036				Q2B	23
		(HL)	0.560	1.007	1.696	0.009	0.015	0.025				Q3B	23
	C → Q0B	(HH)	0.657	1.187	2.005	0.012	0.022	0.036					
		(HL)	0.573	1.017	1.718	0.009	0.015	0.024					
	C → Q1B	(HH)	0.647	1.171	1.979	0.012	0.022	0.036					
		(HL)	0.570	1.011	1.708	0.009	0.015	0.024					
	C → Q2B	(HH)	0.648	1.172	1.981	0.012	0.022	0.036					
		(HL)	0.570	1.011	1.708	0.009	0.015	0.024					
	C → Q3B	(HH)	0.657	1.187	2.005	0.012	0.022	0.036					
		(HL)	0.573	1.017	1.718	0.009	0.015	0.024					
	Set up time	D0	0.444		0.724								
	Set up time	D1	0.444		0.724								
	Set up time	D2	0.444		0.724								
	Set up time	D3	0.444		0.724								
	Hold time	D0	0.435		0.434								
	Hold time	D1	0.438		0.443								
	Hold time	D2	0.422		0.436								
	Hold time	D3	0.406		0.436								
	Min Pulse	C	1.563		3.080								
L924	C → Q0	(HH)	0.459	0.802	1.318	0.025	0.045	0.073		D0	3.0	Q0	10
		(HL)	0.385	0.652	1.072	0.018	0.028	0.046		D1	3.0	Q1	10
	C → Q1	(HH)	0.459	0.802	1.318	0.025	0.045	0.073		D2	3.0	Q2	10
		(HL)	0.385	0.652	1.072	0.018	0.028	0.046		D3	3.0	Q3	10
	C → Q2	(HH)	0.459	0.802	1.318	0.025	0.045	0.073		C	2.1		
		(HL)	0.385	0.652	1.072	0.018	0.028	0.046					
	C → Q3	(HH)	0.458	0.800	1.316	0.025	0.045	0.073					
		(HL)	0.384	0.648	1.066	0.018	0.028	0.046					
	Set up time	D0	0.385		0.566								
	Set up time	D1	0.385		0.566								
	Set up time	D2	0.385		0.566								
	Set up time	D3	0.385		0.566								
	Hold time	D0	0.575		0.629								
	Hold time	D1	0.575		0.629								
	Hold time	D2	0.575		0.629								
	Hold time	D3	0.575		0.629								
	Min Pulse	C	1.406		2.564								

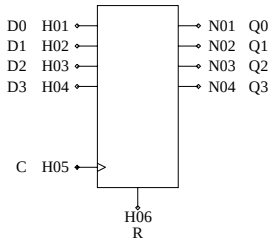
FUNCTION BLOCK

Function	4-BIT D-F/F WITH R							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power			L922	23									
x1	F922	33											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

D0	D1	D2	D3	C	R	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
D0	D1	D2	D3	↗	0	D0	D1	D2	D3	D0B	D1B	D2B	D3B
X	X	X	X	↘	0	HOLD				HOLD			
X	X	X	X	X	1	0	0	0	0	1	1	1	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F922	C → Q0	(HH)	0.488	0.860	1.434	0.013	0.023	0.037		D0	1.0	Q0	22
		(HL)	0.559	1.017	1.720	0.009	0.015	0.025		D1	1.0	Q1	22
	C → Q1	(HH)	0.495	0.876	1.460	0.013	0.023	0.037		D2	1.0	Q2	22
		(HL)	0.571	1.037	1.750	0.009	0.015	0.025		D3	1.0	Q3	22
	C → Q2	(HH)	0.491	0.866	1.443	0.013	0.023	0.037		C	2.0	Q0B	22
		(HL)	0.560	1.020	1.724	0.009	0.015	0.025		R	2.0	Q1B	22
	C → Q3	(HH)	0.489	0.863	1.439	0.013	0.023	0.037				Q2B	22
		(HL)	0.567	1.028	1.734	0.009	0.015	0.025				Q3B	22
	C → Q0B	(HH)	0.660	1.201	2.034	0.012	0.023	0.036					
		(HL)	0.619	1.122	1.905	0.009	0.015	0.024					
	C → Q1B	(HH)	0.668	1.213	2.048	0.012	0.023	0.036					
		(HL)	0.621	1.126	1.909	0.010	0.016	0.026					
	C → Q2B	(HH)	0.668	1.213	2.050	0.012	0.023	0.036					
		(HL)	0.623	1.131	1.919	0.009	0.015	0.024					
	C → Q3B	(HH)	0.667	1.211	2.045	0.012	0.023	0.036					
		(HL)	0.619	1.123	1.906	0.009	0.015	0.024					
	R → Q0	(HL)	0.389	0.670	1.093	0.009	0.015	0.025					
	R → Q1	(HL)	0.391	0.674	1.100	0.009	0.015	0.025					
	R → Q2	(HL)	0.390	0.670	1.094	0.009	0.015	0.025					
	R → Q3	(HL)	0.389	0.669	1.092	0.009	0.015	0.025					
	R → Q0B	(HH)	0.491	0.933	1.528	0.012	0.023	0.036					
	R → Q1B	(HH)	0.499	0.933	1.526	0.012	0.023	0.036					
	R → Q2B	(HH)	0.499	0.947	1.546	0.012	0.023	0.037					
	R → Q3B	(HH)	0.501	0.933	1.526	0.012	0.023	0.036					
	Set up time	D0	0.422		0.802								
	Set up time	D1	0.422		0.802								
	Set up time	D2	0.422		0.802								
	Set up time	D3	0.422		0.802								
	Hold time	D0	0.394		0.361								
	Hold time	D1	0.388		0.371								
	Hold time	D2	0.397		0.372								
	Hold time	D3	0.386		0.363								
	Release time	R	1.209		1.595								
	Removal time	R	0.606		0.619								
	Min Pulse	C	1.528		3.047								
	Min Pulse	R	1.433		3.064								
L922	C → Q0	(HH)	0.490	0.869	1.423	0.025	0.045	0.072		D0	3.0	Q0	10
		(HL)	0.389	0.659	1.080	0.016	0.027	0.044		D1	3.0	Q1	9
	C → Q1	(HH)	0.493	0.874	1.432	0.025	0.045	0.072		D2	3.0	Q2	10
		(HL)	0.394	0.669	1.096	0.017	0.028	0.046		D3	3.0	Q3	9
	C → Q2	(HH)	0.490	0.869	1.423	0.025	0.045	0.072		C	2.1		
		(HL)	0.389	0.659	1.080	0.016	0.027	0.044		R	2.1		
	C → Q3	(HH)	0.493	0.876	1.434	0.025	0.045	0.072					
		(HL)	0.395	0.670	1.098	0.017	0.028	0.046					
	R → Q0	(HL)	0.444	0.864	1.469	0.017	0.027	0.045					
	R → Q1	(HL)	0.452	0.880	1.490	0.018	0.028	0.046					
	R → Q2	(HL)	0.444	0.864	1.469	0.017	0.027	0.045					
	R → Q3	(HL)	0.451	0.881	1.491	0.018	0.028	0.046					
	Set up time	D0	0.361		0.556								
	Set up time	D1	0.361		0.556								
	Set up time	D2	0.361		0.556								
	Set up time	D3	0.361		0.556								
	Hold time	D0	0.587		0.623								
	Hold time	D1	0.583		0.620								
	Hold time	D2	0.587		0.623								
	Hold time	D3	0.583		0.620								

FUNCTION BLOCK

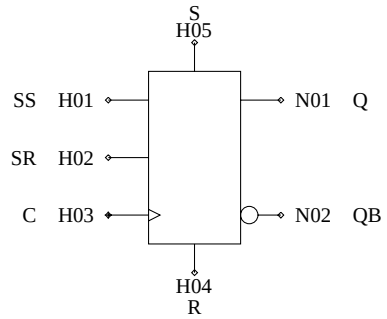
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Release time	R	1.389		1.810							
	Removal time	R	0.456		0.401							
	Min Pulse	C	1.469		2.702							
	Min Pulse	R	1.563		3.276							

[MEMO]

FUNCTION BLOCK

Function	RS-F/F WITH R,S					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F596	11					
x2							
x4							

Logic Diagram



Truth Table

SS	SR	C	R	S	Q	QB	
0	0	↗	0	0	Hold		
1	0	↗	0	0	1	0	
X	1	↗	0	0	0	1	
X	X	↘	0	0	Hold		
X	X	X	0	1	1	0	
X	X	X	1	0	0	1	
X	X	X	1	1	1	1	← Prohibition

X:Irrelevant

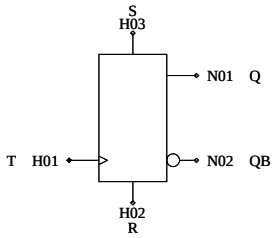
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F596	C → Q	(HH)	0.412	0.749	1.273	0.013	0.023	0.037	S	1.0	Q	22
		(HL)	0.553	1.071	1.848	0.010	0.016	0.027	R	1.0	QB	22
	C → QB	(HH)	0.698	1.347	2.332	0.012	0.022	0.036	C	1.0		
		(HL)	0.709	1.381	2.440	0.010	0.017	0.028	Rset	2.1		
	Rset → Q	(HL)	0.469	0.986	1.687	0.010	0.016	0.026	Set	2.3		
	Rset → QB	(HH)	0.224	0.413	0.625	0.012	0.023	0.037				
	Set → Q	(HH)	0.189	0.304	0.455	0.013	0.023	0.037				
	Set → QB	(HL)	0.489	1.191	2.075	0.010	0.018	0.030				
	Set up time	S	1.712		2.543							
	Set up time	R	1.655		2.305							
	Hold time	S	0.163		0.010							
	Hold time	R	0.159		0.010							
	Release time	Rset	1.205		1.620							
	Release time	Set	1.055		1.132							
	Removal time	Rset	0.549		0.380							
	Removal time	Set	0.674		0.771							
	Min Pulse	C	1.369		2.921							
	Min Pulse	Rset	1.170		2.677							
	Min Pulse	Set	1.208		3.020							

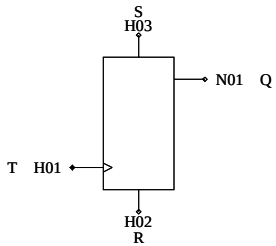
FUNCTION BLOCK

Function	T-F/F WITH R,S							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L714	7		
x1	F744	9	F744NQ	8			F714	9				
x2	F744NP	11	F744NQP	9								
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

T	R	S	Q	QB	
↗	0	0	Invert		
↘	0	0	Hold		
X	1	0	0	1	
X	0	1	1	0	
X	1	1	1	1	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L714	T → Q	(HH)	0.391	0.723	1.197	0.043	0.088	0.147	T	1.0	Q	4
		(HL)	0.346	0.632	1.082	0.017	0.027	0.046	R	2.3		
	R → Q	(HL)	0.160	0.163	0.231	0.011	0.026	0.043	S	2.2		
	S → Q	(HH)	0.316	0.653	1.052	0.044	0.088	0.148				
	Release time	R	1.056		1.128							
	Release time	S	1.198		1.599							
	Removal time	R	0.665		0.757							
	Removal time	S	0.546		0.380							
	Min Pulse	T	0.587		1.679							
	Min Pulse	R	0.381		1.311							
	Min Pulse	S	0.640		2.044							
F744	T → Q	(HH)	0.408	0.743	1.271	0.013	0.023	0.037	T	1.0	Q	22
		(HL)	0.544	1.052	1.823	0.010	0.016	0.027	R	2.2	QB	22
	T → QB	(HH)	0.684	1.317	2.289	0.012	0.022	0.036	S	2.3		
		(HL)	0.695	1.353	2.392	0.010	0.016	0.027				
	R → Q	(HL)	0.465	1.043	1.790	0.010	0.016	0.026				
	R → QB	(HH)	0.218	0.462	0.701	0.012	0.023	0.037				
	S → Q	(HH)	0.188	0.301	0.456	0.013	0.023	0.037				
	S → QB	(HL)	0.474	1.381	2.420	0.010	0.019	0.033				
	Release time	R	1.179		1.586							
	Release time	S	1.039		1.117							
	Removal time	R	0.548		0.370							
	Removal time	S	0.666		0.745							
	Min Pulse	T	1.240		3.470							
	Min Pulse	R	1.064		3.375							
	Min Pulse	S	1.093		3.944							
F714	T → Q	(HH)	0.408	0.743	1.271	0.013	0.023	0.037	T	1.0	Q	22
		(HL)	0.544	1.052	1.823	0.010	0.016	0.027	R	2.2	QB	22
	T → QB	(HH)	0.684	1.317	2.289	0.012	0.022	0.036	S	2.3		
		(HL)	0.695	1.353	2.392	0.010	0.016	0.027				
	R → Q	(HL)	0.465	1.043	1.790	0.010	0.016	0.026				
	R → QB	(HH)	0.218	0.462	0.701	0.012	0.023	0.037				
	S → Q	(HH)	0.188	0.301	0.456	0.013	0.023	0.037				
	S → QB	(HL)	0.474	1.381	2.420	0.010	0.019	0.033				
	Release time	R	1.179		1.586							
	Release time	S	1.039		1.117							
	Removal time	R	0.548		0.370							
	Removal time	S	0.666		0.745							
	Min Pulse	T	1.240		3.470							
	Min Pulse	R	1.064		3.375							
	Min Pulse	S	1.093		3.944							
F744NP	T → Q	(HH)	0.427	0.776	1.322	0.006	0.011	0.018	T	1.0	Q	46
		(HL)	0.589	1.162	2.036	0.005	0.008	0.014	R	2.1	QB	45
	T → QB	(HH)	0.786	1.537	2.695	0.006	0.011	0.018	S	2.2		
		(HL)	0.771	1.512	2.681	0.005	0.008	0.014				
	R → Q	(HL)	0.517	1.210	2.097	0.005	0.008	0.014				
	R → QB	(HH)	0.240	0.487	0.740	0.006	0.012	0.019				
	S → Q	(HH)	0.215	0.338	0.511	0.006	0.011	0.018				
	S → QB	(HL)	0.556	1.504	2.656	0.005	0.010	0.016				
	Release time	R	0.150		0.810							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.210		0.830							
	Min Pulse	T	1.225		3.094							
	Min Pulse	R	0.913		2.348							
	Min Pulse	S	0.943		2.823							

FUNCTION BLOCK

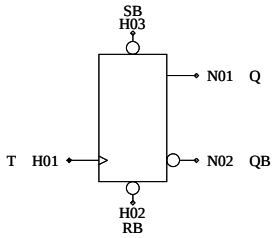
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F744NQ	T → Q	(HH)	0.381	0.694	1.182	0.012	0.023	0.036	T	1.0	Q	23
		(HL)	0.503	0.978	1.696	0.010	0.015	0.025	R	2.1		
	R → Q	(HL)	0.421	0.875	1.493	0.009	0.015	0.025	S	2.2		
	S → Q	(HH)	0.171	0.276	0.409	0.012	0.023	0.036				
	Release time	R	0.140		0.790							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.200		0.820							
	Min Pulse	T	0.907		1.961							
	Min Pulse	R	0.826		1.772							
	Min Pulse	S	0.598		0.783							
F744NQP	T → Q	(HH)	0.428	0.776	1.325	0.006	0.011	0.018	T	1.0	Q	45
		(HL)	0.589	1.163	2.039	0.005	0.008	0.014	R	2.1		
	R → Q	(HL)	0.508	1.065	1.839	0.005	0.008	0.013	S	2.2		
	S → Q	(HH)	0.214	0.337	0.510	0.006	0.011	0.018				
	Release time	R	0.150		0.800							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.200		0.820							
	Min Pulse	T	0.983		2.270							
	Min Pulse	R	0.905		2.088							
	Min Pulse	S	0.630		0.873							

[MEMO]

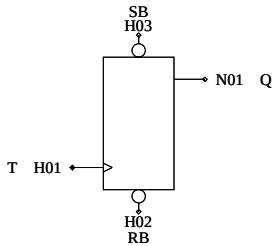
FUNCTION BLOCK

Function	T-F/F WITH RB,SB							SSI Family			
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L717	7		
x1	F747	9	F747NQ	8			F717	9				
x2	F747NP	11	F747NQP	9								
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

T	RB	SB	Q	QB	
↗	1	1	Invert		
↘	1	1	Hold		
X	0	1	0	1	
X	1	0	1	0	
X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L717	T → Q	(HH)	0.369	0.673	1.102	0.025	0.045	0.072	T	1.0	Q	12
		(HL)	0.332	0.599	1.002	0.024	0.044	0.076	RB	2.2		
	RB → Q	(LL)	0.322	0.755	1.333	0.025	0.045	0.078	SB	2.3		
	SB → Q	(LH)	0.171	0.180	0.272	0.014	0.045	0.072				
	Release time	RB	1.167		1.342							
	Release time	SB	1.010		1.051							
	Removal time	RB	0.571		0.584							
	Removal time	SB	0.701		0.817							
	Min Pulse	T	0.568		1.632							
	Min Pulse	RB	0.673		2.321							
	Min Pulse	SB	0.373		1.492							
F747	T → Q	(HH)	0.421	0.773	1.301	0.012	0.023	0.037	T	1.0	Q	22
		(HL)	0.462	0.863	1.453	0.010	0.016	0.026	RB	2.3	QB	22
	T → QB	(HH)	0.635	1.199	2.032	0.012	0.023	0.037	SB	2.2		
		(HL)	0.587	1.102	1.889	0.009	0.015	0.025				
	RB → Q	(LL)	0.212	0.376	0.625	0.010	0.016	0.026				
	RB → QB	(LH)	0.386	0.949	1.574	0.012	0.024	0.038				
	SB → Q	(LH)	0.411	1.063	1.892	0.012	0.023	0.037				
	SB → QB	(LL)	0.248	0.669	1.138	0.009	0.016	0.027				
	Release time	RB	0.994		1.040							
	Release time	SB	1.150		1.331							
	Removal time	RB	0.703		0.805							
	Removal time	SB	0.572		0.572							
	Min Pulse	T	1.159		3.172							
	Min Pulse	RB	0.930		3.209							
	Min Pulse	SB	1.003		3.383							
F717	T → Q	(HH)	0.421	0.773	1.301	0.012	0.023	0.037	T	1.0	Q	22
		(HL)	0.462	0.863	1.453	0.010	0.016	0.026	RB	2.3	QB	22
	T → QB	(HH)	0.635	1.199	2.032	0.012	0.023	0.037	SB	2.2		
		(HL)	0.587	1.102	1.889	0.009	0.015	0.025				
	RB → Q	(LL)	0.212	0.376	0.625	0.010	0.016	0.026				
	RB → QB	(LH)	0.386	0.949	1.574	0.012	0.024	0.038				
	SB → Q	(LH)	0.411	1.063	1.892	0.012	0.023	0.037				
	SB → QB	(LL)	0.248	0.669	1.138	0.009	0.016	0.027				
	Release time	RB	0.994		1.040							
	Release time	SB	1.150		1.331							
	Removal time	RB	0.703		0.805							
	Removal time	SB	0.572		0.572							
	Min Pulse	T	1.159		3.172							
	Min Pulse	RB	0.930		3.209							
	Min Pulse	SB	1.003		3.383							
F747NP	T → Q	(HH)	0.460	0.847	1.426	0.006	0.012	0.019	T	1.0	Q	45
		(HL)	0.499	0.945	1.598	0.005	0.007	0.012	RB	2.2	QB	44
	T → QB	(HH)	0.744	1.415	2.405	0.006	0.011	0.018	SB	2.1		
		(HL)	0.681	1.295	2.227	0.005	0.007	0.012				
	RB → Q	(LL)	0.252	0.459	0.783	0.005	0.007	0.012				
	RB → QB	(LH)	0.497	1.156	1.944	0.006	0.012	0.019				
	SB → Q	(LH)	0.455	1.291	2.284	0.006	0.012	0.018				
	SB → QB	(LL)	0.285	0.729	1.251	0.005	0.008	0.013				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.770							
	Removal time	SB	0.060		0.210							
	Min Pulse	T	1.171		2.752							
	Min Pulse	RB	0.941		2.272							
	Min Pulse	SB	0.903		2.682							

FUNCTION BLOCK

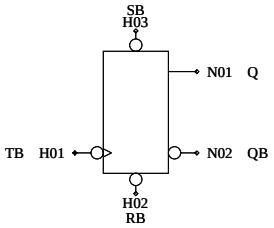
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F747NQ	T → Q	(HH)	0.402	0.741	1.239	0.013	0.023	0.037	T	1.0	Q	22
		(HL)	0.442	0.833	1.402	0.009	0.014	0.024	RB	2.2		
	RB → Q	(LL)	0.201	0.359	0.598	0.009	0.014	0.023	SB	2.1		
	SB → Q	(LH)	0.397	0.885	1.556	0.013	0.023	0.037				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.770							
	Removal time	SB	0.060		0.210							
	Min Pulse	T	0.859		1.730							
	Min Pulse	RB	0.634		0.982							
	Min Pulse	SB	0.841		1.973							
F747NQP	T → Q	(HH)	0.461	0.848	1.429	0.006	0.012	0.019	T	1.0	Q	44
		(HL)	0.498	0.943	1.599	0.005	0.007	0.012	RB	2.2		
	RB → Q	(LL)	0.250	0.458	0.783	0.005	0.007	0.012	SB	2.1		
	SB → Q	(LH)	0.459	1.008	1.763	0.006	0.012	0.019				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.770							
	Removal time	SB	0.060		0.210							
	Min Pulse	T	0.907		1.896							
	Min Pulse	RB	0.677		1.138							
	Min Pulse	SB	0.899		2.161							

[MEMO]

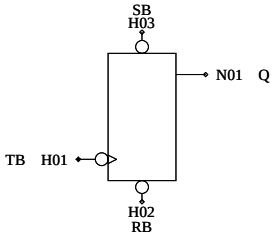
FUNCTION BLOCK

Function	T-F/F (TB) WITH RB,SB							SSI Family				
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L737	7		
x1	F767	9	F767NQ	8			F737	9				
x2	F767NP	11	F767NQP	9								
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

TB	RB	SB	Q	QB	
↘	1	1	Invert		
↗	1	1	Hold		
X	0	1	0	1	
X	1	0	1	0	
X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L737	TB → Q	(LH)	0.342	0.614	1.012	0.025	0.045	0.072	TB	1.0	Q	12
		(LL)	0.376	0.716	1.269	0.024	0.044	0.076	RB	2.2		
	RB → Q	(LL)	0.323	0.755	1.333	0.025	0.045	0.078	SB	2.3		
	SB → Q	(LH)	0.171	0.180	0.272	0.014	0.045	0.072				
	Release time	RB	1.121		1.315							
	Release time	SB	0.965		1.024							
	Removal time	RB	0.559		0.683							
	Removal time	SB	0.690		0.916							
	Min Pulse	TB	0.771		2.401							
	Min Pulse	RB	0.872		2.921							
	Min Pulse	SB	0.573		2.092							
F767	TB → Q	(LH)	0.467	0.891	1.574	0.013	0.023	0.037	TB	1.0	Q	22
		(LL)	0.433	0.801	1.358	0.009	0.015	0.024	RB	2.3	QB	22
	TB → QB	(LH)	0.607	1.138	1.936	0.012	0.023	0.036	SB	2.2		
		(LL)	0.631	1.220	2.157	0.009	0.015	0.025				
	RB → Q	(LL)	0.211	0.373	0.622	0.009	0.015	0.024				
	RB → QB	(LH)	0.385	0.947	1.570	0.012	0.024	0.038				
	SB → Q	(LH)	0.410	1.062	1.888	0.012	0.023	0.037				
	SB → QB	(LL)	0.247	0.666	1.133	0.009	0.016	0.027				
	Release time	RB	0.974		1.033							
	Release time	SB	1.130		1.324							
	Removal time	RB	0.703		0.942							
	Removal time	SB	0.572		0.709							
	Min Pulse	TB	1.126		3.307							
	Min Pulse	RB	0.926		3.205							
	Min Pulse	SB	1.004		3.380							
F737	TB → Q	(LH)	0.467	0.891	1.574	0.013	0.023	0.037	TB	1.0	Q	22
		(LL)	0.433	0.801	1.358	0.009	0.015	0.024	RB	2.3	QB	22
	TB → QB	(LH)	0.607	1.138	1.936	0.012	0.023	0.036	SB	2.2		
		(LL)	0.631	1.220	2.157	0.009	0.015	0.025				
	RB → Q	(LL)	0.211	0.373	0.622	0.009	0.015	0.024				
	RB → QB	(LH)	0.385	0.947	1.570	0.012	0.024	0.038				
	SB → Q	(LH)	0.410	1.062	1.888	0.012	0.023	0.037				
	SB → QB	(LL)	0.247	0.666	1.133	0.009	0.016	0.027				
	Release time	RB	0.974		1.033							
	Release time	SB	1.130		1.324							
	Removal time	RB	0.703		0.942							
	Removal time	SB	0.572		0.709							
	Min Pulse	TB	1.126		3.307							
	Min Pulse	RB	0.926		3.205							
	Min Pulse	SB	1.004		3.380							
F767NP	TB → Q	(LH)	0.509	0.966	1.704	0.006	0.012	0.019	TB	1.0	Q	45
		(LL)	0.471	0.877	1.499	0.005	0.007	0.012	RB	2.2	QB	44
	TB → QB	(LH)	0.716	1.349	2.307	0.006	0.011	0.018	SB	2.1		
		(LL)	0.730	1.413	2.503	0.005	0.007	0.012				
	RB → Q	(LL)	0.252	0.459	0.783	0.005	0.007	0.012				
	RB → QB	(LH)	0.497	1.157	1.944	0.006	0.012	0.019				
	SB → Q	(LH)	0.453	1.290	2.282	0.006	0.012	0.018				
	SB → QB	(LL)	0.285	0.726	1.254	0.005	0.008	0.013				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.500		1.070							
	Removal time	SB	0.250		0.340							
	Min Pulse	TB	1.158		2.871							
	Min Pulse	RB	0.941		2.272							
	Min Pulse	SB	0.903		2.680							

FUNCTION BLOCK

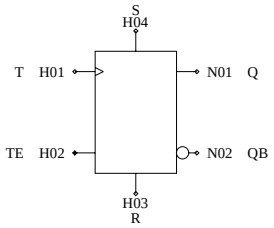
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F767NQ	TB → Q	(LH)	0.449	0.854	1.511	0.013	0.023	0.037	TB	1.0	Q	22
		(LL)	0.414	0.768	1.306	0.009	0.014	0.024	RB	2.2		
	RB → Q	(LL)	0.202	0.358	0.599	0.009	0.014	0.023	SB	2.1		
	SB → Q	(LH)	0.397	0.885	1.557	0.013	0.023	0.037				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.490		1.060							
	Removal time	SB	0.250		0.340							
	Min Pulse	TB	0.888		1.926							
	Min Pulse	RB	0.634		0.982							
	Min Pulse	SB	0.841		1.974							
F767NQP	TB → Q	(LH)	0.508	0.963	1.699	0.006	0.012	0.019	TB	1.0	Q	44
		(LL)	0.471	0.878	1.501	0.005	0.007	0.012	RB	2.2		
	RB → Q	(LL)	0.250	0.458	0.783	0.005	0.007	0.012	SB	2.1		
	SB → Q	(LH)	0.459	1.008	1.764	0.006	0.012	0.019				
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.490		1.070							
	Removal time	SB	0.250		0.340							
	Min Pulse	TB	0.943		2.094							
	Min Pulse	RB	0.677		1.137							
	Min Pulse	SB	0.899		2.162							

[MEMO]

FUNCTION BLOCK

Function	T-F/F WITH DATA-HOLD R,S						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F791	12										
x2												
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

T	TE	R	S	Q	QB	
↗	1	0	0	Invert		
↘	1	0	0	Hold		
X	0	0	0	Hold		
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	← Prohibition

X:Irrelevant

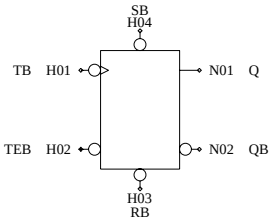
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F791	T → Q	(HH)	0.459	0.839	1.431	0.013	0.023	0.037	T	1.0	Q	22
		(HL)	0.647	1.277	2.236	0.011	0.017	0.029	TE	2.1	QB	22
	T → QB	(HH)	0.759	1.499	2.637	0.012	0.022	0.036	R	2.1		
		(HL)	0.702	1.350	2.371	0.010	0.016	0.026	S	2.4		
	R → Q	(HL)	0.571	1.169	2.034	0.010	0.017	0.028				
	R → QB	(HH)	0.194	0.370	0.554	0.012	0.023	0.037				
	S → Q	(HH)	0.239	0.377	0.577	0.013	0.023	0.037				
	S → QB	(HL)	0.478	1.130	1.944	0.010	0.017	0.029				
	Set up time	TE	1.798		2.852							
	Hold time	TE	0.023		0.010							
	Release time	R	1.213		1.638							
	Release time	S	1.069		1.181							
	Removal time	R	0.520		0.327							
	Removal time	S	0.641		0.693							
	Min Pulse	T	1.266		3.024							
	Min Pulse	R	1.192		2.990							
	Min Pulse	S	1.036		2.917							

FUNCTION BLOCK

Function	T-F/F (TB) WITH DATA-HOLD RB,SB							SSI Family						
Block type	Standard type						Low Gate type							
	Normal		Q output		QB output		Normal		Q output		QB output			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power														
x1	F792	12												
x2														
x4														

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

TB	TEB	RB	SB	Q	QB	
↘	0	1	1	Invert		
↗	0	1	1	Hold		
X	1	1	1	Hold		
X	X	0	1	0	1	
X	X	1	0	1	0	
X	X	0	0	0	0	← Prohibition

X:Irrelevant

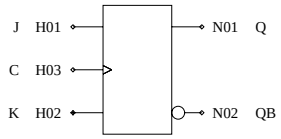
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F792	TB → Q		(LH)	0.538	1.024	1.807	0.013	0.023	0.037	TB	1.0	Q	22
			(LL)	0.504	0.940	1.605	0.010	0.016	0.026	TEB	2.2	QB	22
	TB → QB		(LH)	0.651	1.230	2.102	0.012	0.023	0.036	RB	2.4		
			(LL)	0.671	1.293	2.293	0.009	0.015	0.024	SB	2.1		
	RB → Q		(LL)	0.274	0.500	0.851	0.010	0.015	0.025				
	RB → QB		(LH)	0.423	0.925	1.558	0.012	0.023	0.037				
	SB → Q		(LH)	0.488	1.031	1.808	0.013	0.023	0.037				
	SB → QB		(LL)	0.218	0.500	0.839	0.009	0.016	0.026				
	Set up time	TEB		1.717		2.665							
	Hold time	TEB		0.079		0.010							
	Release time	RB		0.967		1.026							
	Release time	SB		1.121		1.316							
	Removal time	RB		0.688		0.913							
	Removal time	SB		0.559		0.681							
	Min Pulse	TB		1.233		2.934							
	Min Pulse	RB		1.043		2.634							
	Min Pulse	SB		1.112		2.850							

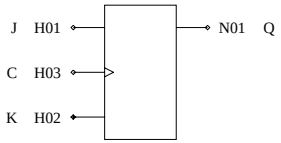
FUNCTION BLOCK

Function	JK-F/F						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F771	10	F771NQ	9	F771NB	9						
x2	F771NP	12	F771NQP	10	F771NBP	10						
x4												

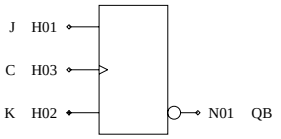
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

J	K	C	Q	QB
0	0	↗	Hold	
0	1	↗	0	1
1	0	↗	1	0
1	1	↗	Invert	
X	X	↘	Hold	

X:Irrelevant

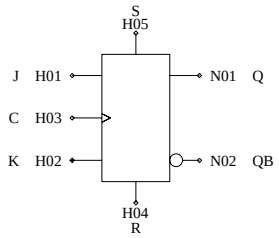
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F771	C → Q	(HH)	0.375	0.668	1.117	0.013	0.023	0.037	J	1.0	Q	22
		(HL)	0.449	0.826	1.387	0.009	0.015	0.024	K	1.0	QB	22
	C → QB	(HH)	0.593	1.088	1.833	0.012	0.023	0.036	C	1.0		
		(HL)	0.552	1.028	1.772	0.010	0.015	0.025				
	Set up time	J	1.594		2.340							
	Set up time	K	1.495		2.128							
	Hold time	J	0.204		0.010							
	Hold time	K	0.169		0.010							
	Min Pulse	C	1.244		2.483							
F771NP	C → Q	(HH)	0.419	0.748	1.221	0.006	0.012	0.019	J	1.0	Q	45
		(HL)	0.392	0.784	1.464	0.005	0.008	0.014	K	1.0	QB	45
	C → QB	(HH)	0.565	1.119	2.061	0.006	0.011	0.018	C	1.0		
		(HL)	0.618	1.145	1.932	0.005	0.007	0.012				
	Set up time	J	0.450		1.080							
	Set up time	K	0.410		0.910							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	C	1.038		2.470							
F771NQ	C → Q	(HH)	0.356	0.640	1.044	0.013	0.023	0.037	J	1.0	Q	22
		(HL)	0.339	0.655	1.145	0.010	0.016	0.026	K	1.0		
	Set up time	J	0.430		1.050				C	1.0		
	Set up time	K	0.410		0.980							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	C	0.774		1.399							
F771NQP	C → Q	(HH)	0.412	0.737	1.204	0.006	0.012	0.019	J	1.0	Q	44
		(HL)	0.388	0.775	1.439	0.005	0.008	0.014	K	1.0		
	Set up time	J	0.440		1.070				C	1.0		
	Set up time	K	0.410		0.910							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	C	0.826		1.655							
F771NB	C → QB	(HH)	0.356	0.640	1.044	0.013	0.023	0.037	J	1.0	QB	22
		(HL)	0.339	0.655	1.145	0.010	0.016	0.026	K	1.0		
	Set up time	J	0.410		0.970				C	1.0		
	Set up time	K	0.410		0.970							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	C	0.774		1.399							
F771NBP	C → QB	(HH)	0.412	0.737	1.204	0.006	0.012	0.019	J	1.0	QB	44
		(HL)	0.388	0.775	1.439	0.005	0.008	0.014	K	1.0		
	Set up time	J	0.410		0.900				C	1.0		
	Set up time	K	0.420		1.000							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	C	0.826		1.655							

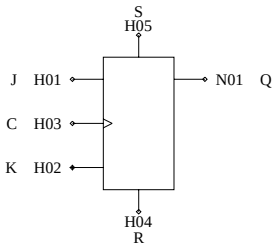
FUNCTION BLOCK

Function	JK-F/F WITH R,S							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F774	12	F774NQ	11	F774NB	11							
x2	F774NP	14	F774NQP	12	F774NBP	12							
x4													

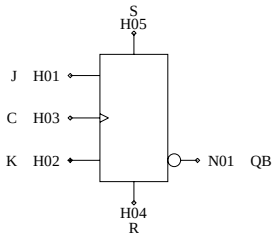
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

J	K	C	R	S	Q	QB	
0	0	↗	0	0	Hold		
0	1	↗	0	0	0	1	
1	0	↗	0	0	1	0	
1	1	↗	0	0	Invert		
X	X	↘	0	0	Hold		
X	X	X	1	0	0	1	
X	X	X	0	1	1	0	
X	X	X	1	1	1	1	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F774	C → Q	(HH)	0.404	0.735	1.257	0.013	0.023	0.037	J	1.0	Q	22
		(HL)	0.542	1.051	1.822	0.010	0.016	0.027	K	1.0	QB	22
	C → QB	(HH)	0.705	1.359	2.362	0.012	0.023	0.036	C	1.0		
		(HL)	0.731	1.434	2.557	0.010	0.017	0.028	R	2.1		
	R → Q	(HL)	0.467	1.006	1.729	0.010	0.016	0.026	S	2.4		
	R → QB	(HH)	0.239	0.431	0.663	0.012	0.023	0.037				
	S → Q	(HH)	0.189	0.300	0.454	0.013	0.023	0.037				
	S → QB	(HL)	0.631	1.249	2.200	0.011	0.019	0.031				
	Set up time	J	1.786		2.682							
	Set up time	K	1.649		2.373							
	Hold time	J	0.063		0.010							
	Hold time	K	0.043		0.010							
	Release time	R	1.213		1.637							
	Release time	S	1.069		1.181							
	Removal time	R	0.521		0.328							
	Removal time	S	0.641		0.693							
	Min Pulse	C	1.308		3.002							
	Min Pulse	R	1.073		2.712							
	Min Pulse	S	1.157		3.117							
F774NP	C → Q	(HH)	0.423	0.767	1.310	0.006	0.011	0.018	J	1.0	Q	46
		(HL)	0.589	1.161	2.035	0.005	0.008	0.014	K	1.0	QB	46
	C → QB	(HH)	0.807	1.577	2.767	0.006	0.011	0.018	C	1.0		
		(HL)	0.800	1.579	2.828	0.005	0.009	0.014	R	2.1		
	R → Q	(HL)	0.518	1.176	2.039	0.005	0.008	0.013	S	2.3		
	R → QB	(HH)	0.258	0.459	0.705	0.006	0.012	0.019				
	S → Q	(HH)	0.215	0.338	0.511	0.006	0.011	0.018				
	S → QB	(HL)	0.591	1.383	2.444	0.005	0.009	0.015				
	Set up time	J	0.450		1.610							
	Set up time	K	0.420		1.000							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	R	0.150		0.820							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.220		0.840							
	Min Pulse	C	1.245		3.155							
	Min Pulse	R	0.913		2.285							
	Min Pulse	S	0.972		2.617							
F774NQ	C → Q	(HH)	0.376	0.686	1.166	0.012	0.023	0.036	J	1.0	Q	23
		(HL)	0.501	0.976	1.689	0.010	0.015	0.025	K	1.0		
	R → Q	(HL)	0.424	0.846	1.441	0.009	0.015	0.025	C	1.0		
	S → Q	(HH)	0.171	0.276	0.409	0.012	0.023	0.036	R	2.1		
	Set up time	J	0.450		1.610				S	2.3		
	Set up time	K	0.410		0.990							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	R	0.150		0.810							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.220		0.840							
	Min Pulse	C	0.905		1.957							
	Min Pulse	R	0.827		1.722							
	Min Pulse	S	0.598		0.784							
F774NQP	C → Q	(HH)	0.424	0.770	1.314	0.006	0.011	0.018	J	1.0	Q	46
		(HL)	0.589	1.162	2.037	0.005	0.008	0.014	K	1.0		
	R → Q	(HL)	0.511	1.036	1.801	0.005	0.008	0.013	C	1.0		

FUNCTION BLOCK

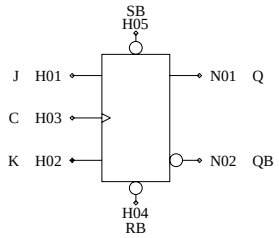
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	S → Q	(HH)	0.215	0.339	0.512	0.006	0.011	0.018	R	2.1		
	Set up time	J	0.450		1.610				S	2.3		
	Set up time	K	0.420		1.000							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	R	0.150		0.830							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.220		0.840							
	Min Pulse	C	0.984		2.270							
	Min Pulse	R	0.908		2.045							
	Min Pulse	S	0.631		0.876							
F774NB	C → QB	(HH)	0.359	0.646	1.056	0.013	0.023	0.037	J	1.0	QB	22
		(HL)	0.368	0.736	1.357	0.010	0.017	0.029	K	1.0		
	R → QB	(HH)	0.286	0.525	0.835	0.013	0.023	0.037	C	1.0		
	S → QB	(HL)	0.563	1.177	2.236	0.011	0.018	0.029	R	2.1		
	Set up time	J	0.450		1.550				S	2.4		
	Set up time	K	0.420		1.010							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	R	0.150		0.750							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.180		0.770							
	Min Pulse	C	0.775		1.562							
	Min Pulse	R	0.697		1.173							
	Min Pulse	S	0.962		2.428							
F774NBP	C → QB	(HH)	0.414	0.741	1.211	0.006	0.012	0.019	J	1.0	QB	44
		(HL)	0.433	0.886	1.748	0.006	0.010	0.016	K	1.0		
	R → QB	(HH)	0.342	0.628	1.004	0.006	0.012	0.019	C	1.0		
	S → QB	(HL)	0.654	1.375	2.646	0.006	0.010	0.016	R	2.1		
	Set up time	J	0.460		1.500				S	2.4		
	Set up time	K	0.430		1.050							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	R	0.180		0.700							
	Release time	S	0.000		0.000							
	Removal time	R	0.000		0.000							
	Removal time	S	0.150		0.750							
	Min Pulse	C	0.827		1.907							
	Min Pulse	R	0.749		1.321							
	Min Pulse	S	1.048		2.814							

[MEMO]

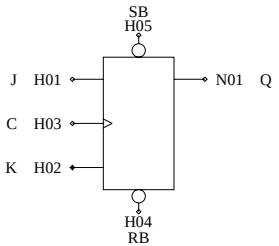
FUNCTION BLOCK

Function	JK-F/F WITH RB,SB						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F777	12	F777NQ	11	F777NB	11						
x2	F777NP	14	F777NQP	12	F777NBP	12						
x4												

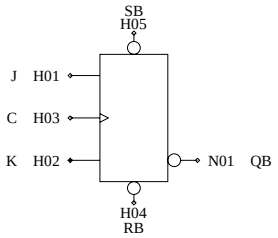
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

J	K	C	RB	SB	Q	QB	
0	0	↗	1	1	Hold		
0	1	↗	1	1	0	1	
1	0	↗	1	1	1	0	
1	1	↗	1	1	Invert		
X	X	↘	1	1	Hold		
X	X	X	0	1	0	1	
X	X	X	1	0	1	0	
X	X	X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F777	C → Q	(HH)	0.420	0.773	1.304	0.013	0.023	0.037	J	1.0	Q	22
		(HL)	0.462	0.861	1.454	0.009	0.015	0.024	K	1.0	QB	22
	C → QB	(HH)	0.664	1.253	2.128	0.013	0.023	0.037	C	1.0		
		(HL)	0.611	1.156	1.986	0.010	0.015	0.025	RB	2.4		
	RB → Q	(LL)	0.211	0.372	0.621	0.009	0.015	0.024	SB	2.1		
	RB → QB	(LH)	0.415	0.891	1.496	0.012	0.023	0.037				
	SB → Q	(LH)	0.520	1.008	1.794	0.012	0.023	0.037				
	SB → QB	(LL)	0.333	0.611	1.039	0.010	0.016	0.026				
	Set up time	J	1.751		2.697							
	Set up time	K	1.574		2.245							
	Hold time	J	0.093		0.010							
	Hold time	K	0.087		0.010							
	Release time	RB	0.997		1.044							
	Release time	SB	1.151		1.333							
	Removal time	RB	0.700		0.802							
	Removal time	SB	0.572		0.570							
	Min Pulse	C	1.249		2.657							
	Min Pulse	RB	1.018		2.517							
	Min Pulse	SB	1.051		2.728							
F777NP	C → Q	(HH)	0.456	0.839	1.416	0.006	0.012	0.019	J	1.0	Q	45
		(HL)	0.499	0.944	1.598	0.005	0.007	0.012	K	1.0	QB	44
	C → QB	(HH)	0.770	1.465	2.496	0.006	0.011	0.018	C	1.0		
		(HL)	0.699	1.334	2.303	0.005	0.007	0.012	RB	2.3		
	RB → Q	(LL)	0.252	0.460	0.783	0.005	0.007	0.012	SB	2.1		
	RB → QB	(LH)	0.525	1.101	1.865	0.006	0.012	0.019				
	SB → Q	(LH)	0.455	1.234	2.178	0.006	0.012	0.018				
	SB → QB	(LL)	0.306	0.672	1.163	0.005	0.008	0.013				
	Set up time	J	0.420		1.040							
	Set up time	K	0.450		1.130							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.190							
	Min Pulse	C	1.194		2.825							
	Min Pulse	RB	0.965		2.221							
	Min Pulse	SB	0.902		2.573							
F777NQ	C → Q	(HH)	0.399	0.731	1.226	0.013	0.023	0.037	J	1.0	Q	22
		(HL)	0.442	0.831	1.401	0.009	0.014	0.023	K	1.0		
	RB → Q	(LL)	0.202	0.358	0.597	0.009	0.014	0.023	C	1.0		
	SB → Q	(LH)	0.400	0.839	1.472	0.012	0.023	0.037	RB	2.3		
	Set up time	J	0.420		1.040				SB	2.1		
	Set up time	K	0.440		1.110							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.858		1.727							
	Min Pulse	RB	0.634		0.982							
	Min Pulse	SB	0.842		1.892							
F777NQP	C → Q	(HH)	0.457	0.841	1.417	0.006	0.012	0.019	J	1.0	Q	44
		(HL)	0.498	0.944	1.599	0.005	0.007	0.012	K	1.0		
	RB → Q	(LL)	0.253	0.461	0.785	0.005	0.007	0.012	C	1.0		

FUNCTION BLOCK

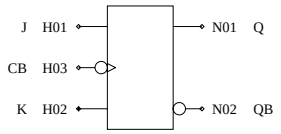
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	SB → Q	(LH)	0.463	0.962	1.683	0.006	0.012	0.019	RB	2.3		
	Set up time	J	0.420		1.040				SB	2.1		
	Set up time	K	0.450		1.130							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.310		0.760							
	Removal time	SB	0.060		0.200							
	Min Pulse	C	0.908		1.898							
	Min Pulse	RB	0.678		1.142							
	Min Pulse	SB	0.901		2.082							
F777NB	C → QB	(HH)	0.390	0.710	1.161	0.013	0.024	0.038	J	1.0	QB	22
		(HL)	0.343	0.660	1.150	0.010	0.016	0.026	K	1.0		
	RB → QB	(LH)	0.455	0.968	1.684	0.013	0.024	0.038	C	1.0		
	SB → QB	(LL)	0.325	0.697	1.306	0.010	0.016	0.026	RB	2.4		
	Set up time	J	0.420		1.020				SB	2.1		
	Set up time	K	0.450		1.130							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.290		0.710							
	Removal time	SB	0.040		0.160							
	Min Pulse	C	0.801		1.475							
	Min Pulse	RB	0.888		2.057							
	Min Pulse	SB	0.736		1.602							
F777NBP	C → QB	(HH)	0.459	0.832	1.363	0.007	0.012	0.019	J	1.0	QB	43
		(HL)	0.391	0.780	1.447	0.005	0.008	0.014	K	1.0		
	RB → QB	(LH)	0.534	1.104	1.916	0.006	0.012	0.019	C	1.0		
	SB → QB	(LL)	0.381	0.823	1.557	0.005	0.008	0.014	RB	2.4		
	Set up time	J	0.420		0.960				SB	2.1		
	Set up time	K	0.460		1.160							
	Hold time	J	0.000		0.000							
	Hold time	K	0.000		0.000							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.260		0.670							
	Removal time	SB	0.030		0.130							
	Min Pulse	C	0.866		1.663							
	Min Pulse	RB	0.961		2.262							
	Min Pulse	SB	0.788		1.826							

[MEMO]

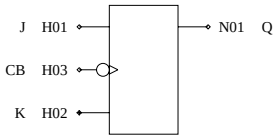
FUNCTION BLOCK

Function	JK-F/F (CB)						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F781	10	F781NQ	9	F781NB	9						
x2	F781NP	12	F781NQP	10	F781NBP	10						
x4												

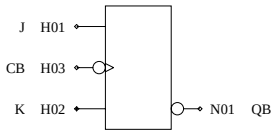
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

J	K	CB	Q	QB
0	0	↘	Hold	
0	1	↘	0	1
1	0	↘	1	0
1	1	↘	Invert	
X	X	↗	Hold	

X:Irrelevant

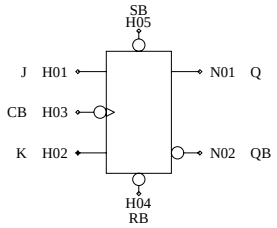
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t_{LD0} (ns)			t_1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F781	CB → Q	(LH)	0.429	0.802	1.419	0.013	0.023	0.037	J	1.0	Q	22
		(LL)	0.422	0.765	1.292	0.009	0.015	0.024	K	1.0	QB	22
	CB → QB	(LH)	0.567	1.028	1.739	0.012	0.023	0.036	CB	1.0		
		(LL)	0.607	1.164	2.076	0.010	0.015	0.025				
	Set up time	J	1.575		2.332							
	Set up time	K	1.476		2.119							
	Hold time	J	0.205		0.103							
	Hold time	K	0.170		0.104							
	Min Pulse	CB	1.247		2.843							
F781NP	CB → Q	(LH)	0.414	0.731	1.215	0.006	0.012	0.019	J	1.0	Q	45
		(LL)	0.411	0.816	1.569	0.005	0.008	0.014	K	1.0	QB	45
	CB → QB	(LH)	0.585	1.152	2.168	0.006	0.011	0.018	CB	1.0		
		(LL)	0.612	1.128	1.926	0.005	0.007	0.012				
	Set up time	J	0.300		1.060							
	Set up time	K	0.240		0.730							
	Hold time	J	0.140		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	CB	1.045		2.639							
F781NQ	CB → Q	(LH)	0.344	0.607	1.004	0.013	0.023	0.037	J	1.0	Q	22
		(LL)	0.361	0.705	1.313	0.010	0.016	0.026	K	1.0		
	Set up time	J	0.290		1.040				CB	1.0		
	Set up time	K	0.230		0.720							
	Hold time	J	0.140		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	CB	0.776		1.624							
F781NQP	CB → Q	(LH)	0.407	0.719	1.195	0.006	0.012	0.019	J	1.0	Q	44
		(LL)	0.407	0.807	1.550	0.005	0.008	0.014	K	1.0		
	Set up time	J	0.300		1.050				CB	1.0		
	Set up time	K	0.240		0.730							
	Hold time	J	0.140		0.000							
	Hold time	K	0.000		0.000							
	Min Pulse	CB	0.834		1.828							
F781NB	CB → QB	(LH)	0.344	0.607	1.004	0.013	0.023	0.037	J	1.0	QB	22
		(LL)	0.361	0.705	1.313	0.010	0.016	0.026	K	1.0		
	Set up time	J	0.230		0.720				CB	1.0		
	Set up time	K	0.280		0.970							
	Hold time	J	0.000		0.000							
	Hold time	K	0.210		0.090							
	Min Pulse	CB	0.776		1.624							
F781NBP	CB → QB	(LH)	0.407	0.719	1.195	0.006	0.012	0.019	J	1.0	QB	44
		(LL)	0.407	0.807	1.550	0.005	0.008	0.014	K	1.0		
	Set up time	J	0.240		0.720				CB	1.0		
	Set up time	K	0.280		0.980							
	Hold time	J	0.000		0.000							
	Hold time	K	0.210		0.080							
	Min Pulse	CB	0.834		1.828							

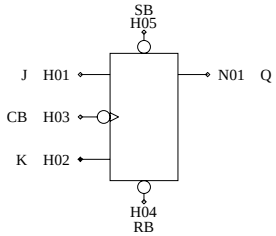
FUNCTION BLOCK

Function	JK-F/F (CB) WITH RB,SB						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F787	12	F787NQ	11	F787NB	11						
x2	F787NP	14	F787NQP	12	F787NBP	12						
x4												

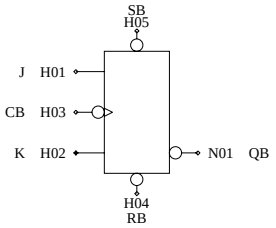
Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"



Truth Table

J	K	CB	RB	SB	Q	QB	
0	0	↘	1	1	Hold		
0	1	↘	1	1	0	1	
1	0	↘	1	1	1	0	
1	1	↘	1	1	Invert		
X	X	↗	1	1	Hold		
X	X	X	0	1	0	1	
X	X	X	1	0	1	0	
X	X	X	0	0	0	0	← Prohibition

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path			t_{LD0} (ns)			t_1					
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F787	CB → Q		(LH)	0.467	0.892	1.575	0.013	0.023	0.037	J	1.0	Q	22
			(LL)	0.435	0.802	1.363	0.009	0.015	0.024	K	1.0	QB	22
	CB → QB		(LH)	0.638	1.195	2.039	0.012	0.023	0.037	CB	1.0		
			(LL)	0.656	1.274	2.256	0.010	0.015	0.025	RB	2.4		
	RB → Q		(LL)	0.211	0.371	0.621	0.009	0.015	0.024	SB	2.1		
	RB → QB		(LH)	0.415	0.891	1.496	0.012	0.023	0.037				
	SB → Q		(LH)	0.415	1.009	1.794	0.012	0.023	0.037				
	SB → QB		(LL)	0.273	0.610	1.039	0.010	0.016	0.026				
	Set up time	J		1.730		2.689							
	Set up time	K		1.553		2.236							
	Hold time	J		0.093		0.010							
	Hold time	K		0.086		0.010							
	Release time	RB		0.975		1.036							
	Release time	SB		1.129		1.325							
	Removal time	RB		0.701		0.940							
	Removal time	SB		0.572		0.708							
	Min Pulse	CB		1.196		2.929							
	Min Pulse	RB		1.018		2.647							
	Min Pulse	SB		1.051		2.859							
F787NP	CB → Q		(LH)	0.509	0.964	1.701	0.006	0.012	0.019	J	1.0	Q	45
			(LL)	0.470	0.875	1.496	0.005	0.007	0.012	K	1.0	QB	44
	CB → QB		(LH)	0.743	1.399	2.397	0.006	0.011	0.018	CB	1.0		
			(LL)	0.749	1.454	2.589	0.005	0.007	0.012	RB	2.3		
	RB → Q		(LL)	0.252	0.459	0.783	0.005	0.007	0.012	SB	2.1		
	RB → QB		(LH)	0.525	1.099	1.863	0.006	0.012	0.019				
	SB → Q		(LH)	0.455	1.233	2.180	0.006	0.012	0.018				
	SB → QB		(LL)	0.306	0.673	1.163	0.005	0.008	0.013				
	Set up time	J		0.230		0.750							
	Set up time	K		0.320		1.090							
	Hold time	J		0.000		0.000							
	Hold time	K		0.210		0.080							
	Release time	RB		0.000		0.000							
	Release time	SB		0.000		0.000							
	Removal time	RB		0.490		1.080							
	Removal time	SB		0.250		0.330							
	Min Pulse	CB		1.181		2.936							
	Min Pulse	RB		0.966		2.220							
	Min Pulse	SB		0.902		2.575							
F787NQ	CB → Q		(LH)	0.447	0.851	1.505	0.013	0.023	0.037	J	1.0	Q	22
			(LL)	0.414	0.766	1.303	0.009	0.014	0.023	K	1.0		
	RB → Q		(LL)	0.202	0.358	0.597	0.009	0.014	0.023	CB	1.0		
	SB → Q		(LH)	0.400	0.839	1.472	0.012	0.023	0.037	RB	2.3		
	Set up time	J		0.230		0.740				SB	2.1		
	Set up time	K		0.310		1.080							
	Hold time	J		0.000		0.000							
	Hold time	K		0.210		0.080							
	Release time	RB		0.000		0.000							
	Release time	SB		0.000		0.000							
	Removal time	RB		0.490		1.080							
	Removal time	SB		0.250		0.330							
	Min Pulse	CB		0.886		1.922							
	Min Pulse	RB		0.634		0.982							
	Min Pulse	SB		0.842		1.892							
F787NQP	CB → Q		(LH)	0.507	0.960	1.696	0.006	0.012	0.019	J	1.0	Q	44
			(LL)	0.470	0.878	1.502	0.005	0.007	0.012	K	1.0		
	RB → Q		(LL)	0.253	0.460	0.785	0.005	0.007	0.012	CB	1.0		

FUNCTION BLOCK

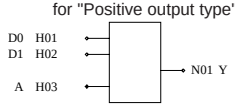
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	SB → Q	(LH)	0.462	0.962	1.684	0.006	0.012	0.019	RB	2.3		
	Set up time	J	0.230		0.750				SB	2.1		
	Set up time	K	0.320		1.090							
	Hold time	J	0.000		0.000							
	Hold time	K	0.210		0.070							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.490		1.080							
	Removal time	SB	0.250		0.330							
	Min Pulse	CB	0.942		2.094							
	Min Pulse	RB	0.678		1.142							
	Min Pulse	SB	0.901		2.083							
F787NB	CB → QB	(LH)	0.376	0.675	1.122	0.013	0.024	0.038	J	1.0	QB	22
		(LL)	0.364	0.709	1.324	0.010	0.016	0.026	K	1.0		
	RB → QB	(LH)	0.454	0.967	1.682	0.013	0.024	0.038	CB	1.0		
	SB → QB	(LL)	0.325	0.698	1.307	0.010	0.016	0.026	RB	2.4		
	Set up time	J	0.240		0.760				SB	2.1		
	Set up time	K	0.310		1.070							
	Hold time	J	0.000		0.000							
	Hold time	K	0.210		0.100							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.470		1.000							
	Removal time	SB	0.240		0.320							
	Min Pulse	CB	0.802		1.638							
	Min Pulse	RB	0.887		2.056							
	Min Pulse	SB	0.736		1.606							
F787NBP	CB → QB	(LH)	0.452	0.814	1.361	0.007	0.012	0.019	J	1.0	QB	43
		(LL)	0.410	0.810	1.557	0.005	0.008	0.014	K	1.0		
	RB → QB	(LH)	0.533	1.102	1.913	0.006	0.012	0.019	CB	1.0		
	SB → QB	(LL)	0.381	0.822	1.559	0.005	0.008	0.014	RB	2.4		
	Set up time	J	0.250		0.770				SB	2.1		
	Set up time	K	0.310		1.090							
	Hold time	J	0.000		0.000							
	Hold time	K	0.210		0.090							
	Release time	RB	0.000		0.000							
	Release time	SB	0.000		0.000							
	Removal time	RB	0.440		0.920							
	Removal time	SB	0.230		0.310							
	Min Pulse	CB	0.873		1.833							
	Min Pulse	RB	0.960		2.262							
	Min Pulse	SB	0.788		1.828							

[MEMO]

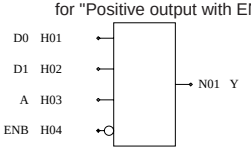
FUNCTION BLOCK

Function	2 TO 1 MULTIPLEXER						SSI Family					
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power			L571	4								
x1	F565	4	F571	6			F57B	5				
x2												
x4												

Logic Diagram for "Positive output type"

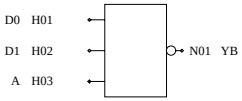


Logic Diagram for "Positive output with ENB"



Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"

Logic Diagram for "Negative output with EN"

Truth Table

D0	D1	A	ENB	Y	YB
X	X	X	1	0	1
A	X	0	0	A	AB
X	B	1	0	B	BB

X:Irrelevant

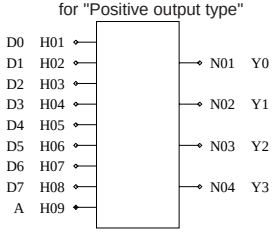
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F565	D0 → Y	(HH)	0.244	0.400	0.634	0.013	0.023	0.037	D0	1.0	Y	22
		(LL)	0.268	0.496	0.898	0.010	0.016	0.025	D1	1.0		
	D1 → Y	(HH)	0.232	0.386	0.613	0.013	0.023	0.037	A	1.0		
		(LL)	0.259	0.480	0.876	0.010	0.016	0.025				
	A → Y	(HH)	0.300	0.536	0.872	0.013	0.023	0.037				
		(HL)	0.285	0.545	0.955	0.010	0.016	0.025				
		(LH)	0.303	0.524	0.854	0.013	0.023	0.037				
		(LL)	0.310	0.588	1.080	0.010	0.016	0.025				
L571	D0 → Y	(HH)	0.254	0.437	0.700	0.044	0.088	0.147	D0	1.0	Y	5
		(LL)	0.251	0.456	0.808	0.017	0.027	0.045	D1	1.0		
	D1 → Y	(HH)	0.243	0.422	0.680	0.044	0.088	0.147	A	1.0		
		(LL)	0.242	0.441	0.787	0.017	0.027	0.045	ENB	1.0		
	A → Y	(HH)	0.320	0.585	0.957	0.044	0.088	0.147				
		(HL)	0.273	0.503	0.839	0.017	0.027	0.045				
		(LH)	0.316	0.562	0.921	0.044	0.088	0.147				
		(LL)	0.306	0.572	1.022	0.017	0.027	0.045				
	ENB → Y	(HL)	0.094	0.132	0.189	0.016	0.026	0.043				
		(LH)	0.102	0.196	0.327	0.044	0.088	0.147				
F571	D0 → Y	(HH)	0.391	0.701	1.158	0.013	0.023	0.037	D0	1.0	Y	22
		(LL)	0.391	0.727	1.287	0.009	0.015	0.024	D1	1.0		
	D1 → Y	(HH)	0.381	0.689	1.137	0.013	0.023	0.037	A	1.0		
		(LL)	0.383	0.711	1.264	0.009	0.015	0.024	ENB	1.0		
	A → Y	(HH)	0.458	0.850	1.418	0.013	0.023	0.037				
		(HL)	0.416	0.778	1.319	0.009	0.015	0.024				
		(LH)	0.454	0.822	1.379	0.013	0.023	0.037				
		(LL)	0.444	0.842	1.497	0.009	0.015	0.024				
	ENB → Y	(HL)	0.240	0.438	0.722	0.009	0.015	0.024				
		(LH)	0.245	0.441	0.729	0.013	0.023	0.037				
F57B	D1 → Y	(HL)	0.240	0.442	0.757	0.010	0.016	0.026	D1	1.0	Y	22
		(LH)	0.264	0.471	0.776	0.013	0.023	0.037	D2	1.0		
	D2 → Y	(HL)	0.253	0.465	0.798	0.010	0.016	0.026	A	1.0		
		(LH)	0.255	0.458	0.761	0.013	0.023	0.037				
	A → Y	(HH)	0.321	0.577	0.955	0.013	0.023	0.037				
		(HL)	0.389	0.725	1.226	0.010	0.016	0.026				
		(LH)	0.386	0.704	1.196	0.013	0.023	0.037				
		(LL)	0.345	0.636	1.073	0.010	0.016	0.026				

FUNCTION BLOCK

Function	QUAD 2 TO 1 MULTIPLEXER							SSI Family				
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L572	10		
x1	F552	13					F555	9	F572	14		
x2												
x4												

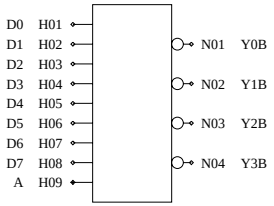
Logic Diagram for "Positive output type"



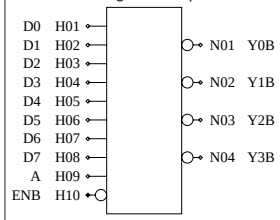
Logic Diagram for "Positive output with ENB"

Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"



Logic Diagram for "Negative output with EN"

Truth Table

Da	Da+1	A	ENB	Yn	YnB
A	X	0	0	A	AB
X	B	1	0	B	BB
X	X	X	1	0	1

X:Irrelevant

a=2*n(n=0 to 3)

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F552	D1 → Y1	(HH)	0.233	0.383	0.609	0.013	0.023	0.037	D1	1.0	Y1	21
		(LL)	0.259	0.483	0.877	0.010	0.016	0.025	D2	1.0	Y2	21
	D2 → Y1	(HH)	0.243	0.401	0.631	0.013	0.023	0.037	D3	1.0	Y3	21
		(LL)	0.268	0.496	0.893	0.010	0.016	0.026	D4	1.0	Y4	21
	D3 → Y2	(HH)	0.233	0.383	0.609	0.013	0.023	0.037	D5	1.0		
		(LL)	0.261	0.483	0.873	0.010	0.016	0.025	D6	1.0		
	D4 → Y2	(HH)	0.243	0.399	0.632	0.013	0.023	0.037	D7	1.0		
		(LL)	0.268	0.495	0.897	0.010	0.016	0.026	D8	1.0		
	D5 → Y3	(HH)	0.233	0.383	0.609	0.013	0.023	0.037	A	1.0		
		(LL)	0.259	0.483	0.877	0.010	0.016	0.025				
	D6 → Y3	(HH)	0.243	0.401	0.631	0.013	0.023	0.037				
		(LL)	0.268	0.496	0.893	0.010	0.016	0.026				
	D7 → Y4	(HH)	0.233	0.383	0.609	0.013	0.023	0.037				
		(LL)	0.261	0.482	0.873	0.010	0.016	0.025				
	D8 → Y4	(HH)	0.243	0.399	0.632	0.013	0.023	0.037				
		(LL)	0.268	0.495	0.897	0.010	0.016	0.026				
	A → Y1	(HH)	0.440	0.797	1.335	0.013	0.023	0.037				
		(HL)	0.384	0.681	1.148	0.010	0.015	0.025				
		(LH)	0.390	0.708	1.194	0.013	0.023	0.037				
		(LL)	0.434	0.840	1.542	0.010	0.016	0.025				
	A → Y2	(HH)	0.440	0.797	1.335	0.013	0.023	0.037				
		(HL)	0.384	0.681	1.148	0.010	0.015	0.025				
		(LH)	0.390	0.708	1.194	0.013	0.023	0.037				
		(LL)	0.434	0.840	1.542	0.010	0.016	0.025				
	A → Y3	(HH)	0.440	0.797	1.335	0.013	0.023	0.037				
		(HL)	0.384	0.681	1.148	0.010	0.015	0.025				
		(LH)	0.390	0.708	1.194	0.013	0.023	0.037				
		(LL)	0.434	0.840	1.542	0.010	0.016	0.025				
	A → Y4	(HH)	0.440	0.797	1.335	0.013	0.023	0.037				
		(HL)	0.384	0.681	1.148	0.010	0.015	0.025				
		(LH)	0.390	0.708	1.194	0.013	0.023	0.037				
		(LL)	0.434	0.840	1.542	0.010	0.016	0.025				
F555	D1 → Y1	(HL)	0.119	0.208	0.367	0.010	0.015	0.024	D1	1.6	Y1	22
		(LH)	0.120	0.195	0.304	0.012	0.023	0.037	D2	1.6	Y2	22
	D2 → Y1	(HL)	0.115	0.209	0.366	0.010	0.015	0.024	D3	1.6	Y3	22
		(LH)	0.112	0.187	0.294	0.012	0.023	0.037	D4	1.6	Y4	22
	D3 → Y2	(HL)	0.115	0.209	0.365	0.010	0.015	0.024	D5	1.6		
		(LH)	0.112	0.187	0.292	0.012	0.023	0.037	D6	1.6		
	D4 → Y2	(HL)	0.119	0.208	0.365	0.010	0.015	0.024	D7	1.6		
		(LH)	0.120	0.195	0.306	0.012	0.023	0.037	D8	1.6		
	D5 → Y3	(HL)	0.114	0.207	0.365	0.010	0.015	0.024	A	1.0		
		(LH)	0.113	0.187	0.294	0.012	0.023	0.037				
	D6 → Y3	(HL)	0.120	0.210	0.368	0.010	0.015	0.024				
		(LH)	0.120	0.196	0.304	0.012	0.023	0.037				
	D7 → Y4	(HL)	0.120	0.211	0.367	0.010	0.015	0.024				
		(LH)	0.120	0.196	0.303	0.012	0.023	0.037				
	D8 → Y4	(HL)	0.115	0.207	0.364	0.010	0.015	0.024				
		(LH)	0.113	0.187	0.294	0.012	0.023	0.037				
	A → Y1	(HH)	0.378	0.687	1.158	0.012	0.023	0.037				
		(HL)	0.311	0.524	0.856	0.009	0.015	0.024				
		(LH)	0.346	0.612	1.030	0.012	0.023	0.037				
		(LL)	0.379	0.704	1.267	0.009	0.015	0.024				
	A → Y2	(HH)	0.387	0.700	1.174	0.012	0.023	0.037				
		(HL)	0.311	0.523	0.855	0.009	0.015	0.024				
		(LH)	0.331	0.592	1.005	0.012	0.023	0.037				
		(LL)	0.378	0.703	1.266	0.009	0.015	0.024				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A → Y3	(HH)	0.388	0.701	1.176	0.012	0.023	0.037				
		(HL)	0.312	0.525	0.858	0.009	0.015	0.024				
		(LH)	0.332	0.594	1.008	0.012	0.023	0.037				
		(LL)	0.378	0.704	1.268	0.009	0.015	0.024				
	A → Y4	(HH)	0.379	0.688	1.160	0.012	0.023	0.037				
		(HL)	0.312	0.526	0.859	0.009	0.015	0.024				
		(LH)	0.347	0.614	1.033	0.012	0.023	0.037				
		(LL)	0.380	0.705	1.269	0.009	0.015	0.024				
L572	D0 → Y0B	(HL)	0.123	0.210	0.345	0.025	0.044	0.077	D0	2.9	Y0B	11
		(LH)	0.103	0.172	0.270	0.025	0.045	0.073	D1	3.0	Y1B	11
	D1 → Y0B	(HL)	0.124	0.210	0.345	0.025	0.044	0.077	D2	2.9	Y2B	11
		(LH)	0.109	0.180	0.280	0.025	0.045	0.073	D3	3.0	Y3B	11
	D2 → Y1B	(HL)	0.123	0.210	0.345	0.025	0.044	0.077	D4	2.9		
		(LH)	0.103	0.172	0.270	0.025	0.045	0.073	D5	3.0		
	D3 → Y1B	(HL)	0.124	0.210	0.345	0.025	0.044	0.077	D6	2.9		
		(LH)	0.109	0.180	0.280	0.025	0.045	0.073	D7	3.0		
	D4 → Y2B	(HL)	0.123	0.210	0.345	0.025	0.044	0.077	A	1.0		
		(LH)	0.103	0.172	0.270	0.025	0.045	0.073	ENB	1.0		
	D5 → Y2B	(HL)	0.124	0.210	0.345	0.025	0.044	0.077				
		(LH)	0.109	0.180	0.280	0.025	0.045	0.073				
	D6 → Y3B	(HL)	0.123	0.210	0.345	0.025	0.044	0.077				
		(LH)	0.103	0.172	0.270	0.025	0.045	0.073				
	D7 → Y3B	(HL)	0.124	0.210	0.345	0.025	0.044	0.077				
		(LH)	0.109	0.180	0.280	0.025	0.045	0.073				
	A → Y0B	(HH)	0.397	0.716	1.202	0.025	0.045	0.073				
		(HL)	0.305	0.508	0.823	0.024	0.044	0.077				
		(LH)	0.329	0.591	1.001	0.025	0.045	0.073				
		(LL)	0.399	0.746	1.325	0.024	0.044	0.077				
	A → Y1B	(HH)	0.397	0.716	1.202	0.025	0.045	0.073				
		(HL)	0.305	0.508	0.823	0.024	0.044	0.077				
		(LH)	0.329	0.591	1.001	0.025	0.045	0.073				
		(LL)	0.399	0.746	1.325	0.024	0.044	0.077				
	A → Y2B	(HH)	0.397	0.716	1.202	0.025	0.045	0.073				
		(HL)	0.305	0.508	0.823	0.024	0.044	0.077				
		(LH)	0.329	0.591	1.001	0.025	0.045	0.073				
		(LL)	0.399	0.746	1.325	0.024	0.044	0.077				
	A → Y3B	(HH)	0.397	0.716	1.202	0.025	0.045	0.073				
		(HL)	0.305	0.508	0.823	0.024	0.044	0.077				
		(LH)	0.329	0.591	1.001	0.025	0.045	0.073				
		(LL)	0.399	0.746	1.325	0.024	0.044	0.077				
	ENB → Y0B	(HH)	0.244	0.385	0.596	0.025	0.045	0.072				
		(LL)	0.255	0.452	0.767	0.024	0.044	0.077				
	ENB → Y1B	(HH)	0.244	0.385	0.596	0.025	0.045	0.072				
		(LL)	0.255	0.452	0.767	0.024	0.044	0.077				
	ENB → Y2B	(HH)	0.244	0.385	0.596	0.025	0.045	0.072				
		(LL)	0.255	0.452	0.767	0.024	0.044	0.077				
	ENB → Y3B	(HH)	0.244	0.385	0.596	0.025	0.045	0.072				
		(LL)	0.255	0.452	0.767	0.024	0.044	0.077				
F572	D0 → Y0B	(HL)	0.126	0.231	0.414	0.012	0.022	0.039	D0	3.9	Y0B	21
		(LH)	0.129	0.219	0.349	0.012	0.023	0.036	D1	4.0	Y1B	21
	D1 → Y0B	(HL)	0.131	0.233	0.416	0.012	0.022	0.039	D2	3.9	Y2B	21
		(LH)	0.137	0.229	0.364	0.012	0.023	0.036	D3	4.0	Y3B	21
	D2 → Y1B	(HL)	0.126	0.231	0.416	0.012	0.022	0.039	D4	3.9		
		(LH)	0.129	0.220	0.347	0.012	0.023	0.036	D5	4.0		
	D3 → Y1B	(HL)	0.131	0.237	0.416	0.012	0.022	0.039	D6	3.9		
		(LH)	0.137	0.229	0.363	0.012	0.023	0.036	D7	4.0		

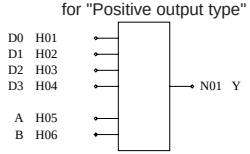
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D4 → Y2B	(HL)	0.126	0.231	0.414	0.012	0.022	0.039	A	1.0		
		(LH)	0.129	0.219	0.349	0.012	0.023	0.036	ENB	2.0		
	D5 → Y2B	(HL)	0.131	0.233	0.416	0.012	0.022	0.039				
		(LH)	0.137	0.229	0.364	0.012	0.023	0.036				
	D6 → Y3B	(HL)	0.126	0.231	0.416	0.012	0.022	0.039				
		(LH)	0.129	0.220	0.347	0.012	0.023	0.036				
	D7 → Y3B	(HL)	0.131	0.237	0.416	0.012	0.022	0.039				
		(LH)	0.137	0.229	0.363	0.012	0.023	0.036				
	A → Y0B	(HH)	0.445	0.805	1.358	0.012	0.023	0.036				
		(HL)	0.348	0.587	0.966	0.012	0.022	0.039				
		(LH)	0.375	0.678	1.158	0.012	0.023	0.036				
		(LL)	0.434	0.813	1.466	0.012	0.022	0.039				
	A → Y1B	(HH)	0.445	0.805	1.358	0.012	0.023	0.036				
		(HL)	0.348	0.587	0.966	0.012	0.022	0.039				
		(LH)	0.375	0.678	1.158	0.012	0.023	0.036				
		(LL)	0.434	0.813	1.466	0.012	0.022	0.039				
	A → Y2B	(HH)	0.445	0.805	1.358	0.012	0.023	0.036				
		(HL)	0.348	0.587	0.966	0.012	0.022	0.039				
		(LH)	0.375	0.678	1.158	0.012	0.023	0.036				
		(LL)	0.434	0.813	1.466	0.012	0.022	0.039				
	A → Y3B	(HH)	0.445	0.805	1.358	0.012	0.023	0.036				
		(HL)	0.348	0.587	0.966	0.012	0.022	0.039				
		(LH)	0.375	0.678	1.158	0.012	0.023	0.036				
		(LL)	0.434	0.813	1.466	0.012	0.022	0.039				
	ENB → Y0B	(HH)	0.247	0.379	0.576	0.012	0.023	0.037				
		(LL)	0.247	0.438	0.737	0.012	0.022	0.039				
	ENB → Y1B	(HH)	0.247	0.379	0.576	0.012	0.023	0.037				
		(LL)	0.247	0.438	0.737	0.012	0.022	0.039				
	ENB → Y2B	(HH)	0.247	0.379	0.576	0.012	0.023	0.037				
		(LL)	0.247	0.438	0.737	0.012	0.022	0.039				
	ENB → Y3B	(HH)	0.247	0.379	0.576	0.012	0.023	0.037				
		(LL)	0.247	0.438	0.737	0.012	0.022	0.039				

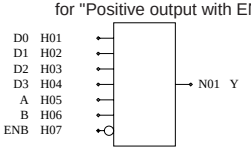
FUNCTION BLOCK

Function	4 TO 1 MULTIPLEXER						SSI Family					
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F564	8	F570	10			F57A	10				
x2												
x4												

Logic Diagram for "Positive output type"

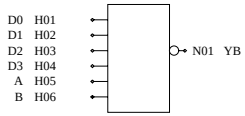


Logic Diagram for "Positive output with ENB"



Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"

Logic Diagram for "Negative output with EN"

Truth Table

D0	D1	D2	D3	A	B	ENB	Y	YB
X	X	X	X	X	X	1	0	1
A	X	X	X	0	0	0	A	AB
X	B	X	X	1	0	0	B	BB
X	X	C	X	0	1	0	C	CB
X	X	X	D	1	1	0	D	DB

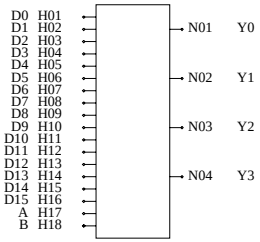
X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F564	D0 → Y		(HH)	0.396	0.659	1.063	0.013	0.024	0.038	D0	1.0	Y	21
			(LL)	0.395	0.767	1.497	0.011	0.018	0.028	D1	1.0		
	D1 → Y		(HH)	0.379	0.635	1.033	0.013	0.024	0.038	D2	1.0		
			(LL)	0.386	0.753	1.474	0.011	0.017	0.028	D3	1.0		
	D2 → Y		(HH)	0.377	0.630	1.020	0.013	0.024	0.038	A	1.0		
			(LL)	0.378	0.739	1.444	0.011	0.017	0.028	B	1.0		
	D3 → Y		(HH)	0.364	0.611	0.996	0.013	0.024	0.037				
			(LL)	0.372	0.732	1.434	0.011	0.017	0.028				
	A → Y		(HH)	0.465	0.856	1.407	0.013	0.024	0.038				
			(HL)	0.432	0.892	1.701	0.011	0.017	0.028				
			(LH)	0.469	0.849	1.398	0.013	0.024	0.038				
			(LL)	0.455	0.929	1.817	0.011	0.017	0.028				
	B → Y		(HH)	0.355	0.631	1.010	0.013	0.024	0.038				
			(HL)	0.309	0.615	1.146	0.010	0.017	0.028				
			(LH)	0.357	0.621	1.000	0.013	0.024	0.038				
			(LL)	0.334	0.662	1.281	0.011	0.017	0.028				
F570	D0 → Y		(HH)	0.526	0.925	1.540	0.013	0.023	0.037	D0	1.0	Y	22
			(LL)	0.499	0.963	1.819	0.009	0.015	0.024	D1	1.0		
	D1 → Y		(HH)	0.513	0.907	1.514	0.013	0.023	0.037	D2	1.0		
			(LL)	0.490	0.948	1.799	0.009	0.015	0.024	D3	1.0		
	D2 → Y		(HH)	0.507	0.898	1.492	0.013	0.023	0.037	A	1.0		
			(LL)	0.481	0.931	1.756	0.009	0.015	0.024	B	1.0		
	D3 → Y		(HH)	0.496	0.883	1.474	0.013	0.023	0.037	ENB	1.0		
			(LL)	0.476	0.922	1.751	0.009	0.015	0.024				
	A → Y		(HH)	0.610	1.145	1.920	0.013	0.023	0.037				
			(HL)	0.550	1.103	2.018	0.009	0.015	0.024				
			(LH)	0.609	1.127	1.899	0.013	0.023	0.037				
			(LL)	0.573	1.148	2.176	0.009	0.015	0.024				
	B → Y		(HH)	0.501	0.916	1.516	0.013	0.023	0.037				
			(HL)	0.428	0.823	1.441	0.009	0.015	0.024				
			(LH)	0.494	0.888	1.484	0.013	0.023	0.037				
			(LL)	0.453	0.880	1.616	0.009	0.015	0.024				
	ENB → Y		(HL)	0.234	0.433	0.717	0.009	0.015	0.024				
			(LH)	0.246	0.439	0.728	0.013	0.023	0.037				
F57A	D1 → Y		(HL)	0.331	0.587	0.972	0.012	0.022	0.039	D1	1.0	Y	21
			(LH)	0.370	0.695	1.215	0.012	0.023	0.036	D2	1.0		
	D2 → Y		(HL)	0.322	0.571	0.952	0.012	0.022	0.039	D3	1.0		
			(LH)	0.361	0.679	1.192	0.012	0.023	0.036	D4	1.0		
	D3 → Y		(HL)	0.322	0.565	0.941	0.012	0.022	0.038	A	1.0		
			(LH)	0.359	0.672	1.175	0.012	0.023	0.036	B	1.0		
	D4 → Y		(HL)	0.310	0.552	0.922	0.012	0.022	0.039				
			(LH)	0.350	0.657	1.153	0.012	0.023	0.036				
	A → Y		(HH)	0.399	0.766	1.293	0.012	0.023	0.036				
			(HL)	0.421	0.797	1.348	0.012	0.022	0.039				
			(LH)	0.444	0.872	1.546	0.012	0.023	0.037				
			(LL)	0.404	0.755	1.277	0.012	0.022	0.039				
	B → Y		(HH)	0.330	0.600	1.004	0.012	0.023	0.036				
			(HL)	0.276	0.493	0.817	0.012	0.022	0.039				
			(LH)	0.287	0.517	0.869	0.012	0.023	0.037				
			(LL)	0.341	0.624	1.058	0.012	0.022	0.039				

Function	QUAD 4 TO 1 MULTIPLEXER						SSI Family					
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F551	27					F554	31				
x2												
x4												

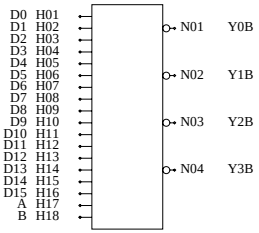
Logic Diagram for "Positive output type"



Logic Diagram for "Positive output with ENB"

Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"

Logic Diagram for "Negative output with EN"

Truth Table

Da	Da+1	Da+2	Da+3	A	B	Yn	YnB
A	X	X	X	0	0	A	AB
X	B	X	X	1	0	B	BB
X	X	C	X	0	1	C	CB
X	X	X	D	1	1	D	DB

X:Irrelevant

a=4*n(n=0 to 3)

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F551	D1 → Y1	(HH)	0.378	0.634	1.025	0.013	0.024	0.038	D1	1.0	Y1	21
		(LL)	0.389	0.756	1.475	0.011	0.017	0.028	D2	1.0	Y2	21
	D2 → Y1	(HH)	0.363	0.611	0.992	0.013	0.024	0.038	D3	1.0	Y3	21
		(LL)	0.379	0.742	1.451	0.011	0.017	0.028	D4	1.0	Y4	21
	D3 → Y1	(HH)	0.375	0.625	1.009	0.013	0.024	0.038	D5	1.0		
		(LL)	0.378	0.740	1.441	0.011	0.017	0.028	D6	1.0		
	D4 → Y1	(HH)	0.361	0.607	0.986	0.013	0.024	0.037	D7	1.0		
		(LL)	0.372	0.731	1.432	0.011	0.017	0.028	D8	1.0		
	D5 → Y2	(HH)	0.378	0.634	1.025	0.013	0.024	0.038	D9	1.0		
		(LL)	0.389	0.758	1.475	0.011	0.017	0.028	D10	1.0		
	D6 → Y2	(HH)	0.363	0.611	0.992	0.013	0.024	0.038	D11	1.0		
		(LL)	0.379	0.742	1.451	0.011	0.017	0.028	D12	1.0		
	D7 → Y2	(HH)	0.375	0.625	1.009	0.013	0.024	0.038	D13	1.0		
		(LL)	0.378	0.740	1.441	0.011	0.017	0.028	D14	1.0		
	D8 → Y2	(HH)	0.361	0.607	0.986	0.013	0.024	0.037	D15	1.0		
		(LL)	0.372	0.731	1.432	0.011	0.017	0.028	D16	1.0		
	D9 → Y3	(HH)	0.386	0.648	1.049	0.013	0.024	0.038	A	2.0		
		(LL)	0.398	0.772	1.505	0.011	0.018	0.028	B	1.0		
	D10 → Y3	(HH)	0.371	0.624	1.016	0.013	0.024	0.038				
		(LL)	0.387	0.757	1.483	0.011	0.018	0.028				
	D11 → Y3	(HH)	0.379	0.632	1.019	0.013	0.024	0.038				
		(LL)	0.381	0.745	1.454	0.011	0.017	0.028				
	D12 → Y3	(HH)	0.365	0.613	0.997	0.013	0.024	0.037				
		(LL)	0.375	0.738	1.445	0.011	0.017	0.028				
	D13 → Y4	(HH)	0.378	0.634	1.025	0.013	0.024	0.038				
		(LL)	0.389	0.758	1.475	0.011	0.017	0.028				
	D14 → Y4	(HH)	0.363	0.611	0.992	0.013	0.024	0.038				
		(LL)	0.380	0.742	1.451	0.011	0.017	0.028				
	D15 → Y4	(HH)	0.375	0.626	1.010	0.013	0.024	0.038				
		(LL)	0.378	0.738	1.441	0.011	0.017	0.028				
	D16 → Y4	(HH)	0.361	0.607	0.987	0.013	0.024	0.037				
		(LL)	0.372	0.732	1.432	0.011	0.017	0.028				
	A → Y1	(HH)	0.567	1.018	1.695	0.013	0.024	0.038				
		(HL)	0.520	0.996	1.799	0.011	0.017	0.028				
		(LH)	0.530	0.952	1.597	0.013	0.024	0.038				
		(LL)	0.535	1.073	2.064	0.011	0.017	0.028				
	A → Y2	(HH)	0.567	1.018	1.695	0.013	0.024	0.038				
		(HL)	0.520	0.996	1.799	0.011	0.017	0.028				
		(LH)	0.530	0.952	1.597	0.013	0.024	0.038				
		(LL)	0.535	1.073	2.064	0.011	0.017	0.028				
	A → Y3	(HH)	0.571	1.032	1.718	0.013	0.024	0.038				
		(HL)	0.523	1.017	1.842	0.011	0.017	0.028				
		(LH)	0.535	0.970	1.625	0.013	0.024	0.038				
		(LL)	0.538	1.086	2.093	0.011	0.018	0.028				
	A → Y4	(HH)	0.567	1.018	1.696	0.013	0.024	0.038				
		(HL)	0.520	0.996	1.799	0.011	0.017	0.028				
		(LH)	0.530	0.952	1.597	0.013	0.024	0.038				
		(LL)	0.535	1.073	2.064	0.011	0.017	0.028				
	B → Y1	(HH)	0.522	0.948	1.568	0.013	0.024	0.038				
		(HL)	0.454	0.825	1.418	0.010	0.017	0.028				
		(LH)	0.482	0.868	1.448	0.013	0.024	0.038				
		(LL)	0.494	0.994	1.883	0.010	0.017	0.028				
	B → Y2	(HH)	0.522	0.948	1.568	0.013	0.024	0.038				
		(HL)	0.454	0.825	1.418	0.010	0.017	0.028				
		(LH)	0.482	0.868	1.448	0.013	0.024	0.038				
		(LL)	0.494	0.994	1.883	0.010	0.017	0.028				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B → Y3	(HH)	0.525	0.955	1.577	0.013	0.024	0.038				
		(HL)	0.459	0.836	1.439	0.010	0.017	0.028				
		(LH)	0.486	0.875	1.459	0.013	0.024	0.038				
		(LL)	0.496	0.998	1.894	0.011	0.017	0.028				
	B → Y4	(HH)	0.522	0.948	1.568	0.013	0.024	0.038				
		(HL)	0.454	0.825	1.419	0.010	0.017	0.028				
		(LH)	0.482	0.868	1.448	0.013	0.024	0.038				
		(LL)	0.494	0.994	1.883	0.010	0.017	0.028				
F554	D1 → Y1	(HL)	0.432	0.753	1.255	0.009	0.015	0.024	D1	1.0	Y1	22
		(LH)	0.422	0.811	1.530	0.012	0.023	0.036	D2	1.0	Y2	22
	D2 → Y1	(HL)	0.417	0.730	1.225	0.009	0.015	0.024	D3	1.0	Y3	22
		(LH)	0.413	0.794	1.506	0.012	0.023	0.036	D4	1.0	Y4	22
	D3 → Y1	(HL)	0.429	0.743	1.236	0.009	0.015	0.024	D5	1.0		
		(LH)	0.411	0.791	1.497	0.012	0.023	0.036	D6	1.0		
	D4 → Y1	(HL)	0.417	0.727	1.218	0.009	0.015	0.024	D7	1.0		
		(LH)	0.405	0.782	1.484	0.012	0.023	0.036	D8	1.0		
	D5 → Y2	(HL)	0.436	0.759	1.265	0.009	0.015	0.024	D9	1.0		
		(LH)	0.425	0.818	1.547	0.012	0.023	0.036	D10	1.0		
	D6 → Y2	(HL)	0.421	0.735	1.237	0.009	0.015	0.024	D11	1.0		
		(LH)	0.416	0.800	1.523	0.012	0.023	0.036	D12	1.0		
	D7 → Y2	(HL)	0.429	0.744	1.235	0.009	0.015	0.024	D13	1.0		
		(LH)	0.411	0.791	1.498	0.012	0.023	0.036	D14	1.0		
	D8 → Y2	(HL)	0.417	0.726	1.218	0.009	0.015	0.024	D15	1.0		
		(LH)	0.405	0.782	1.485	0.012	0.023	0.036	D16	1.0		
	D9 → Y3	(HL)	0.436	0.759	1.265	0.009	0.015	0.024	A	2.0		
		(LH)	0.425	0.818	1.547	0.012	0.023	0.036	B	1.0		
	D10 → Y3	(HL)	0.421	0.735	1.237	0.009	0.015	0.024				
		(LH)	0.416	0.800	1.523	0.012	0.023	0.036				
	D11 → Y3	(HL)	0.429	0.744	1.235	0.009	0.015	0.024				
		(LH)	0.411	0.791	1.498	0.012	0.023	0.036				
	D12 → Y3	(HL)	0.417	0.726	1.218	0.009	0.015	0.024				
		(LH)	0.405	0.782	1.485	0.012	0.023	0.036				
	D13 → Y4	(HL)	0.432	0.753	1.255	0.009	0.015	0.024				
		(LH)	0.422	0.811	1.530	0.012	0.023	0.036				
	D14 → Y4	(HL)	0.417	0.730	1.225	0.009	0.015	0.024				
		(LH)	0.413	0.794	1.506	0.012	0.023	0.036				
	D15 → Y4	(HL)	0.429	0.743	1.236	0.009	0.015	0.024				
		(LH)	0.411	0.791	1.497	0.012	0.023	0.036				
	D16 → Y4	(HL)	0.417	0.727	1.218	0.009	0.015	0.024				
		(LH)	0.405	0.782	1.484	0.012	0.023	0.036				
	A → Y1	(HH)	0.551	1.030	1.829	0.012	0.023	0.036				
		(HL)	0.628	1.148	1.945	0.009	0.015	0.024				
		(LH)	0.577	1.139	2.146	0.012	0.023	0.036				
		(LL)	0.581	1.070	1.825	0.009	0.015	0.024				
	A → Y2	(HH)	0.551	1.041	1.853	0.012	0.023	0.036				
		(HL)	0.628	1.153	1.954	0.009	0.015	0.024				
		(LH)	0.576	1.144	2.160	0.012	0.023	0.036				
		(LL)	0.581	1.078	1.838	0.009	0.015	0.024				
	A → Y3	(HH)	0.551	1.041	1.853	0.012	0.023	0.036				
		(HL)	0.628	1.153	1.954	0.009	0.015	0.024				
		(LH)	0.576	1.144	2.160	0.012	0.023	0.036				
		(LL)	0.581	1.078	1.838	0.009	0.015	0.024				
	A → Y4	(HH)	0.551	1.030	1.829	0.012	0.023	0.036				
		(HL)	0.628	1.148	1.945	0.009	0.015	0.024				
		(LH)	0.577	1.139	2.146	0.012	0.023	0.036				
		(LL)	0.581	1.070	1.825	0.009	0.015	0.024				

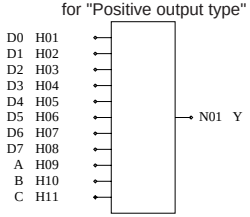
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B → Y1	(HH)	0.468	0.830	1.405	0.012	0.023	0.036				
		(HL)	0.586	1.082	1.828	0.009	0.015	0.024				
		(LH)	0.544	1.074	1.978	0.012	0.023	0.036				
		(LL)	0.528	0.972	1.655	0.009	0.015	0.024				
	B → Y2	(HH)	0.469	0.831	1.408	0.012	0.023	0.036				
		(HL)	0.586	1.081	1.826	0.009	0.015	0.024				
		(LH)	0.544	1.073	1.977	0.012	0.023	0.036				
		(LL)	0.527	0.971	1.653	0.009	0.015	0.024				
	B → Y3	(HH)	0.469	0.831	1.408	0.012	0.023	0.036				
		(HL)	0.586	1.081	1.826	0.009	0.015	0.024				
		(LH)	0.544	1.073	1.977	0.012	0.023	0.036				
		(LL)	0.527	0.971	1.653	0.009	0.015	0.024				
	B → Y4	(HH)	0.468	0.830	1.405	0.012	0.023	0.036				
		(HL)	0.586	1.082	1.828	0.009	0.015	0.024				
		(LH)	0.544	1.074	1.978	0.012	0.023	0.036				
		(LL)	0.528	0.972	1.655	0.009	0.015	0.024				

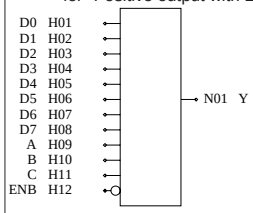
FUNCTION BLOCK

Function	8 TO 1 MULTIPLEXER						SSI Family					
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F563	17	F569	18			F579	17				
x2												
x4												

Logic Diagram for "Positive output type"

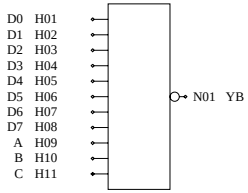


Logic Diagram for "Positive output with ENB"



Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"

Logic Diagram for "Negative output with EN"

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	A	B	C	ENB	Y	YB
X	X	X	X	X	X	X	X	X	X	X	1	0	1
A	X	X	X	X	X	X	X	0	0	0	0	A	AB
X	B	X	X	X	X	X	X	1	0	0	0	B	BB
X	X	C	X	X	X	X	X	0	1	0	0	C	CB
X	X	X	D	X	X	X	X	1	1	0	0	D	DB
X	X	X	X	E	X	X	X	0	0	1	0	E	EB
X	X	X	X	X	F	X	X	1	0	1	0	F	FB
X	X	X	X	X	X	G	X	0	1	1	0	G	GB
X	X	X	X	X	X	X	H	1	1	1	0	H	HB

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F563	D0 → Y		(HH)	0.510	0.900	1.518	0.012	0.023	0.037	D0	1.0	Y	22
			(LL)	0.544	1.067	1.986	0.009	0.015	0.024	D1	1.0		
	D1 → Y		(HH)	0.496	0.881	1.489	0.012	0.023	0.037	D2	1.0		
			(LL)	0.535	1.050	1.956	0.009	0.015	0.024	D3	1.0		
	D2 → Y		(HH)	0.506	0.894	1.503	0.012	0.023	0.037	D4	1.0		
			(LL)	0.532	1.047	1.949	0.009	0.015	0.024	D5	1.0		
	D3 → Y		(HH)	0.495	0.878	1.482	0.012	0.023	0.037	D6	1.0		
			(LL)	0.527	1.037	1.942	0.009	0.015	0.024	D7	1.0		
	D4 → Y		(HH)	0.515	0.913	1.530	0.012	0.023	0.037	A	1.0		
			(LL)	0.533	1.045	1.944	0.009	0.015	0.024	B	1.0		
	D5 → Y		(HH)	0.501	0.893	1.502	0.012	0.023	0.037	C	1.0		
			(LL)	0.524	1.031	1.917	0.009	0.015	0.024				
	D6 → Y		(HH)	0.511	0.904	1.512	0.012	0.023	0.037				
			(LL)	0.521	1.024	1.905	0.009	0.015	0.024				
	D7 → Y		(HH)	0.499	0.888	1.491	0.012	0.023	0.037				
			(LL)	0.515	1.016	1.890	0.009	0.015	0.024				
	A → Y		(HH)	0.693	1.296	2.202	0.012	0.023	0.037				
			(HL)	0.653	1.293	2.302	0.009	0.015	0.024				
			(LH)	0.665	1.236	2.109	0.012	0.023	0.037				
			(LL)	0.694	1.423	2.651	0.009	0.015	0.024				
	B → Y		(HH)	0.562	1.050	1.749	0.012	0.023	0.037				
			(HL)	0.514	0.999	1.723	0.009	0.015	0.024				
			(LH)	0.533	0.983	1.651	0.012	0.023	0.037				
			(LL)	0.555	1.123	2.042	0.009	0.015	0.024				
	C → Y		(HH)	0.337	0.607	1.011	0.012	0.023	0.037				
			(HL)	0.392	0.721	1.220	0.009	0.015	0.024				
			(LH)	0.417	0.764	1.289	0.012	0.023	0.037				
			(LL)	0.359	0.659	1.123	0.009	0.015	0.024				
F569	D0 → Y		(HH)	0.634	1.167	2.000	0.013	0.023	0.037	D0	1.0	Y	22
			(LL)	0.601	1.167	2.172	0.009	0.015	0.024	D1	1.0		
	D1 → Y		(HH)	0.647	1.186	2.026	0.013	0.023	0.037	D2	1.0		
			(LL)	0.608	1.175	2.188	0.009	0.015	0.024	D3	1.0		
	D2 → Y		(HH)	0.648	1.186	2.029	0.013	0.023	0.037	D4	1.0		
			(LL)	0.613	1.187	2.213	0.009	0.015	0.024	D5	1.0		
	D3 → Y		(HH)	0.664	1.207	2.060	0.013	0.023	0.037	D6	1.0		
			(LL)	0.621	1.202	2.232	0.009	0.015	0.024	D7	1.0		
	D4 → Y		(HH)	0.609	1.123	1.920	0.013	0.023	0.037	A	1.0		
			(LL)	0.582	1.125	2.087	0.009	0.015	0.024	B	1.0		
	D5 → Y		(HH)	0.625	1.141	1.953	0.013	0.023	0.037	C	1.0		
			(LL)	0.591	1.137	2.104	0.009	0.015	0.024	ENB	1.0		
	D6 → Y		(HH)	0.598	1.104	1.898	0.013	0.023	0.037				
			(LL)	0.567	1.098	2.042	0.009	0.015	0.024				
	D7 → Y		(HH)	0.610	1.120	1.921	0.013	0.023	0.037				
			(LL)	0.573	1.108	2.057	0.009	0.015	0.024				
	A → Y		(HH)	0.851	1.592	2.736	0.013	0.023	0.037				
			(HL)	0.747	1.419	2.524	0.009	0.015	0.024				
			(LH)	0.793	1.489	2.588	0.013	0.023	0.037				
			(LL)	0.782	1.542	2.877	0.009	0.015	0.024				
	B → Y		(HH)	0.701	1.313	2.236	0.013	0.023	0.037				
			(HL)	0.606	1.145	1.985	0.009	0.015	0.024				
			(LH)	0.670	1.248	2.150	0.013	0.023	0.037				
			(LL)	0.634	1.242	2.276	0.009	0.015	0.024				
	C → Y		(HH)	0.373	0.707	1.190	0.013	0.023	0.037				
			(HL)	0.381	0.705	1.169	0.009	0.015	0.024				
			(LH)	0.402	0.765	1.355	0.013	0.023	0.037				
			(LL)	0.380	0.684	1.143	0.009	0.015	0.024				

FUNCTION BLOCK

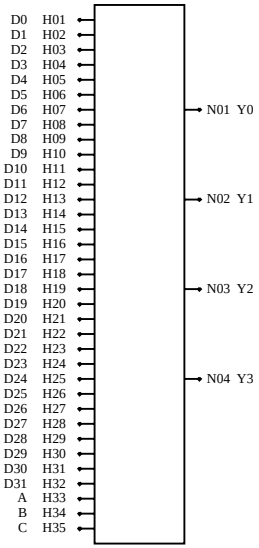
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	ENB → Y	(HL)	0.241	0.440	0.726	0.009	0.015	0.024				
		(LH)	0.249	0.445	0.738	0.013	0.023	0.037				
F579	D1 → Y	(HL)	0.452	0.794	1.331	0.012	0.022	0.039	D1	1.0	Y	21
		(LH)	0.485	0.951	1.768	0.012	0.023	0.036	D2	1.0		
	D2 → Y	(HL)	0.438	0.774	1.301	0.012	0.022	0.039	D3	1.0		
		(LH)	0.475	0.936	1.739	0.012	0.023	0.036	D4	1.0		
	D3 → Y	(HL)	0.448	0.785	1.315	0.012	0.022	0.039	D5	1.0		
		(LH)	0.472	0.929	1.730	0.012	0.023	0.036	D6	1.0		
	D4 → Y	(HL)	0.437	0.769	1.290	0.012	0.022	0.039	D7	1.0		
		(LH)	0.466	0.919	1.712	0.012	0.023	0.036	D8	1.0		
	D5 → Y	(HL)	0.455	0.803	1.344	0.012	0.022	0.039	A	1.0		
		(LH)	0.490	0.962	1.780	0.012	0.023	0.036	B	1.0		
	D6 → Y	(HL)	0.442	0.782	1.314	0.012	0.022	0.039	C	1.0		
		(LH)	0.481	0.945	1.753	0.012	0.023	0.036				
	D7 → Y	(HL)	0.452	0.794	1.330	0.012	0.022	0.039				
		(LH)	0.478	0.940	1.741	0.012	0.023	0.036				
	D8 → Y	(HL)	0.440	0.777	1.306	0.012	0.022	0.039				
		(LH)	0.471	0.932	1.727	0.012	0.023	0.036				
	A → Y	(HH)	0.605	1.184	2.095	0.012	0.023	0.036				
		(HL)	0.634	1.185	2.015	0.012	0.022	0.039				
		(LH)	0.645	1.318	2.447	0.012	0.023	0.036				
		(LL)	0.606	1.126	1.924	0.012	0.022	0.039				
	B → Y	(HH)	0.467	0.880	1.509	0.012	0.023	0.036				
		(HL)	0.504	0.938	1.563	0.012	0.022	0.039				
		(LH)	0.505	1.014	1.841	0.012	0.023	0.036				
		(LL)	0.475	0.875	1.467	0.012	0.022	0.039				
	C → Y	(HH)	0.337	0.611	1.021	0.012	0.023	0.036				
		(HL)	0.272	0.487	0.807	0.012	0.022	0.039				
		(LH)	0.289	0.519	0.871	0.012	0.023	0.036				
		(LL)	0.350	0.640	1.085	0.012	0.022	0.039				

[MEMO]

FUNCTION BLOCK

Function	QUAD 8 TO 1 MULTIPLEXER							SSI Family	
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power												
x1	F550	64										
x2												
x4												

Logic Diagram for "Normal type"



Logic Diagram for "with ENB"

Logic Diagram for "with EN"

Truth Table

Da	Da+1	Da+2	Da+3	Da+4	Da+5	Da+6	Da+7	A	B	C	Yn	YnB
A	X	X	X	X	X	X	X	0	0	0	A	AB
X	B	X	X	X	X	X	X	1	0	0	B	BB
X	X	C	X	X	X	X	X	0	1	0	C	CB
X	X	X	D	X	X	X	X	1	1	0	D	DB
X	X	X	X	E	X	X	X	0	0	1	E	EB
X	X	X	X	X	F	X	X	1	0	1	F	FB
X	X	X	X	X	X	G	X	0	1	1	G	GB
X	X	X	X	X	X	X	H	1	1	1	H	HB

X:Irrelevant

a=8*n(n=0 to 3)

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F550	D1 → Y1	(HH)	0.495	0.875	1.472	0.012	0.023	0.037	D1	1.0	Y1	22
		(LL)	0.534	1.045	1.936	0.009	0.015	0.024	D2	1.0	Y2	22
	D2 → Y1	(HH)	0.482	0.857	1.443	0.012	0.023	0.037	D3	1.0	Y3	22
		(LL)	0.525	1.029	1.914	0.009	0.015	0.024	D4	1.0	Y4	22
	D3 → Y1	(HH)	0.491	0.866	1.455	0.012	0.023	0.037	D5	1.0		
		(LL)	0.522	1.025	1.897	0.009	0.015	0.024	D6	1.0		
	D4 → Y1	(HH)	0.481	0.852	1.434	0.012	0.023	0.037	D7	1.0		
		(LL)	0.517	1.018	1.883	0.009	0.015	0.024	D8	1.0		
	D5 → Y1	(HH)	0.502	0.891	1.486	0.012	0.023	0.037	D9	1.0		
		(LL)	0.523	1.025	1.901	0.009	0.015	0.024	D10	1.0		
	D6 → Y1	(HH)	0.489	0.871	1.459	0.012	0.023	0.037	D11	1.1		
		(LL)	0.514	1.009	1.878	0.009	0.015	0.024	D12	1.0		
	D7 → Y1	(HH)	0.498	0.881	1.470	0.012	0.023	0.037	D13	1.0		
		(LL)	0.511	1.004	1.861	0.009	0.015	0.024	D14	1.0		
	D8 → Y1	(HH)	0.487	0.867	1.449	0.012	0.023	0.037	D15	1.0		
		(LL)	0.506	0.997	1.847	0.009	0.015	0.024	D16	1.0		
	D9 → Y2	(HH)	0.495	0.875	1.472	0.012	0.023	0.037	D17	1.1		
		(LL)	0.534	1.046	1.936	0.009	0.015	0.024	D18	1.0		
	D10 → Y2	(HH)	0.482	0.857	1.443	0.012	0.023	0.037	D19	1.0		
		(LL)	0.524	1.029	1.913	0.009	0.015	0.024	D20	1.0		
	D11 → Y2	(HH)	0.491	0.866	1.455	0.012	0.023	0.037	D21	1.1		
		(LL)	0.522	1.025	1.900	0.009	0.015	0.024	D22	1.0		
	D12 → Y2	(HH)	0.481	0.852	1.434	0.012	0.023	0.037	D23	1.0		
		(LL)	0.517	1.018	1.883	0.009	0.015	0.024	D24	1.1		
	D13 → Y2	(HH)	0.502	0.890	1.486	0.012	0.023	0.037	D25	1.1		
		(LL)	0.523	1.025	1.901	0.009	0.015	0.024	D26	1.0		
	D14 → Y2	(HH)	0.489	0.871	1.459	0.012	0.023	0.037	D27	1.0		
		(LL)	0.514	1.009	1.878	0.009	0.015	0.024	D28	1.0		
	D15 → Y2	(HH)	0.498	0.881	1.470	0.012	0.023	0.037	D29	1.1		
		(LL)	0.511	1.004	1.862	0.009	0.015	0.024	D30	1.0		
	D16 → Y2	(HH)	0.487	0.867	1.449	0.012	0.023	0.037	D31	1.0		
		(LL)	0.506	0.997	1.847	0.009	0.015	0.024	D32	1.0		
	D17 → Y3	(HH)	0.513	0.902	1.503	0.012	0.023	0.037	A	4.1		
		(LL)	0.523	1.029	1.907	0.009	0.015	0.024	B	2.0		
	D18 → Y3	(HH)	0.501	0.886	1.481	0.012	0.023	0.037	C	2.0		
		(LL)	0.518	1.018	1.894	0.009	0.015	0.024				
	D19 → Y3	(HH)	0.502	0.894	1.494	0.012	0.023	0.037				
		(LL)	0.525	1.030	1.924	0.009	0.015	0.024				
	D20 → Y3	(HH)	0.488	0.872	1.466	0.012	0.023	0.037				
		(LL)	0.516	1.019	1.895	0.009	0.015	0.024				
	D21 → Y3	(HH)	0.510	0.893	1.499	0.012	0.023	0.037				
		(LL)	0.537	1.056	1.963	0.009	0.015	0.024				
	D22 → Y3	(HH)	0.499	0.879	1.478	0.012	0.023	0.037				
		(LL)	0.532	1.046	1.949	0.009	0.015	0.024				
	D23 → Y3	(HH)	0.495	0.876	1.476	0.012	0.023	0.037				
		(LL)	0.534	1.048	1.956	0.009	0.015	0.024				
	D24 → Y3	(HH)	0.481	0.856	1.448	0.012	0.023	0.037				
		(LL)	0.526	1.036	1.927	0.009	0.015	0.024				
	D25 → Y4	(HH)	0.513	0.902	1.503	0.012	0.023	0.037				
		(LL)	0.523	1.029	1.907	0.009	0.015	0.024				
	D26 → Y4	(HH)	0.501	0.886	1.481	0.012	0.023	0.037				
		(LL)	0.518	1.018	1.894	0.009	0.015	0.024				
	D27 → Y4	(HH)	0.502	0.894	1.494	0.012	0.023	0.037				
		(LL)	0.524	1.030	1.925	0.009	0.015	0.024				
	D28 → Y4	(HH)	0.488	0.872	1.466	0.012	0.023	0.037				
		(LL)	0.516	1.019	1.895	0.009	0.015	0.024				

FUNCTION BLOCK

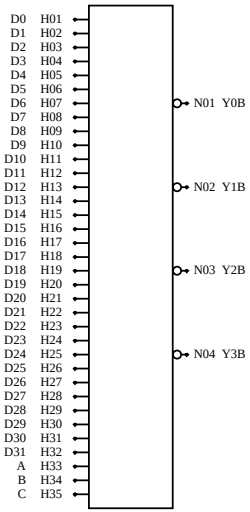
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D29 → Y4	(HH)	0.509	0.892	1.498	0.012	0.023	0.037				
		(LL)	0.537	1.053	1.959	0.009	0.015	0.024				
	D30 → Y4	(HH)	0.498	0.876	1.476	0.012	0.023	0.037				
		(LL)	0.531	1.047	1.942	0.009	0.015	0.024				
	D31 → Y4	(HH)	0.494	0.876	1.474	0.012	0.023	0.037				
		(LL)	0.534	1.046	1.955	0.009	0.015	0.024				
	D32 → Y4	(HH)	0.480	0.856	1.447	0.012	0.023	0.037				
		(LL)	0.525	1.036	1.924	0.009	0.015	0.024				
	A → Y1	(HH)	0.683	1.271	2.148	0.012	0.023	0.037				
		(HL)	0.640	1.257	2.228	0.009	0.015	0.024				
		(LH)	0.638	1.192	2.036	0.012	0.023	0.037				
		(LL)	0.674	1.369	2.549	0.009	0.015	0.024				
	A → Y2	(HH)	0.683	1.271	2.148	0.012	0.023	0.037				
		(HL)	0.640	1.257	2.228	0.009	0.015	0.024				
		(LH)	0.638	1.192	2.036	0.012	0.023	0.037				
		(LL)	0.674	1.369	2.549	0.009	0.015	0.024				
	A → Y3	(HH)	0.688	1.281	2.164	0.012	0.023	0.037				
		(HL)	0.657	1.280	2.274	0.009	0.015	0.024				
		(LH)	0.647	1.206	2.060	0.012	0.023	0.037				
		(LL)	0.683	1.382	2.577	0.009	0.015	0.024				
	A → Y4	(HH)	0.688	1.281	2.164	0.012	0.023	0.037				
		(HL)	0.657	1.277	2.268	0.009	0.015	0.024				
		(LH)	0.646	1.206	2.059	0.012	0.023	0.037				
		(LL)	0.683	1.381	2.573	0.009	0.015	0.024				
	B → Y1	(HH)	0.649	1.195	2.003	0.012	0.023	0.037				
		(HL)	0.564	1.050	1.788	0.009	0.015	0.024				
		(LH)	0.572	1.073	1.823	0.012	0.023	0.037				
		(LL)	0.632	1.275	2.309	0.009	0.015	0.024				
	B → Y2	(HH)	0.649	1.195	2.003	0.012	0.023	0.037				
		(HL)	0.564	1.050	1.788	0.009	0.015	0.024				
		(LH)	0.572	1.073	1.823	0.012	0.023	0.037				
		(LL)	0.632	1.275	2.309	0.009	0.015	0.024				
	B → Y3	(HH)	0.647	1.192	1.997	0.012	0.023	0.037				
		(HL)	0.560	1.039	1.774	0.009	0.015	0.024				
		(LH)	0.572	1.073	1.823	0.012	0.023	0.037				
		(LL)	0.633	1.274	2.308	0.009	0.015	0.024				
	B → Y4	(HH)	0.647	1.192	1.997	0.012	0.023	0.037				
		(HL)	0.560	1.040	1.774	0.009	0.015	0.024				
		(LH)	0.572	1.073	1.823	0.012	0.023	0.037				
		(LL)	0.633	1.274	2.308	0.009	0.015	0.024				
	C → Y1	(HH)	0.387	0.674	1.107	0.012	0.023	0.037				
		(HL)	0.490	0.875	1.472	0.009	0.015	0.024				
		(LH)	0.506	0.927	1.566	0.012	0.023	0.037				
		(LL)	0.400	0.738	1.261	0.009	0.015	0.024				
	C → Y2	(HH)	0.387	0.674	1.107	0.012	0.023	0.037				
		(HL)	0.490	0.875	1.472	0.009	0.015	0.024				
		(LH)	0.506	0.927	1.566	0.012	0.023	0.037				
		(LL)	0.400	0.738	1.261	0.009	0.015	0.024				
	C → Y3	(HH)	0.394	0.689	1.121	0.012	0.023	0.037				
		(HL)	0.501	0.899	1.512	0.009	0.015	0.024				
		(LH)	0.500	0.914	1.556	0.012	0.023	0.037				
		(LL)	0.389	0.714	1.222	0.009	0.015	0.024				
	C → Y4	(HH)	0.394	0.689	1.121	0.012	0.023	0.037				
		(HL)	0.501	0.899	1.512	0.009	0.015	0.024				
		(LH)	0.500	0.914	1.556	0.012	0.023	0.037				
		(LL)	0.389	0.714	1.222	0.009	0.015	0.024				

[MEMO]

FUNCTION BLOCK

Function	QUAD 8 TO 1 MULTIPLEXER							SSI Family						
Block type	Positive output type						Negative output type							
	Normal		with ENB		with EN		Normal		with ENB		with EN			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power														
x1							F553	64						
x2														
x4														

Logic Diagram for "Normal type"



Logic Diagram for "with ENB"

Logic Diagram for "with EN"

Truth Table

Da	Da+1	Da+2	Da+3	Da+4	Da+5	Da+6	Da+7	A	B	C	Yn	YnB
A	X	X	X	X	X	X	X	0	0	0	A	AB
X	B	X	X	X	X	X	X	1	0	0	B	BB
X	X	C	X	X	X	X	X	0	1	0	C	CB
X	X	X	D	X	X	X	X	1	1	0	D	DB
X	X	X	X	E	X	X	X	0	0	1	E	EB
X	X	X	X	X	F	X	X	1	0	1	F	FB
X	X	X	X	X	X	G	X	0	1	1	G	GB
X	X	X	X	X	X	X	H	1	1	1	H	HB

X:Irrelevant

a=8*n(n=0 to 3)

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F553	D1 → Y1	(HL)	0.440	0.773	1.293	0.012	0.022	0.039	D1	1.0	Y1	21
		(LH)	0.477	0.937	1.727	0.012	0.023	0.036	D2	1.0	Y2	21
	D2 → Y1	(HL)	0.426	0.753	1.264	0.012	0.022	0.039	D3	1.1	Y3	21
		(LH)	0.468	0.920	1.704	0.012	0.023	0.036	D4	1.0	Y4	21
	D3 → Y1	(HL)	0.436	0.764	1.277	0.012	0.022	0.039	D5	1.0		
		(LH)	0.465	0.914	1.690	0.012	0.023	0.036	D6	1.0		
	D4 → Y1	(HL)	0.424	0.749	1.258	0.012	0.022	0.039	D7	1.0		
		(LH)	0.459	0.908	1.676	0.012	0.023	0.036	D8	1.0		
	D5 → Y1	(HL)	0.437	0.767	1.282	0.012	0.022	0.039	D9	1.0		
		(LH)	0.473	0.928	1.715	0.012	0.023	0.036	D10	1.0		
	D6 → Y1	(HL)	0.422	0.746	1.254	0.012	0.022	0.039	D11	1.1		
		(LH)	0.464	0.911	1.691	0.012	0.023	0.036	D12	1.0		
	D7 → Y1	(HL)	0.434	0.756	1.264	0.012	0.022	0.039	D13	1.0		
		(LH)	0.461	0.906	1.675	0.012	0.023	0.036	D14	1.0		
	D8 → Y1	(HL)	0.422	0.741	1.243	0.012	0.022	0.039	D15	1.0		
		(LH)	0.455	0.897	1.662	0.012	0.023	0.036	D16	1.0		
	D9 → Y2	(HL)	0.436	0.766	1.281	0.012	0.022	0.039	D17	1.1		
		(LH)	0.473	0.929	1.714	0.012	0.023	0.036	D18	1.0		
	D10 → Y2	(HL)	0.422	0.747	1.251	0.012	0.022	0.039	D19	1.0		
		(LH)	0.464	0.912	1.691	0.012	0.023	0.036	D20	1.0		
	D11 → Y2	(HL)	0.433	0.756	1.263	0.012	0.022	0.039	D21	1.1		
		(LH)	0.461	0.907	1.678	0.012	0.023	0.036	D22	1.0		
	D12 → Y2	(HL)	0.421	0.742	1.242	0.012	0.022	0.039	D23	1.0		
		(LH)	0.455	0.900	1.662	0.012	0.023	0.036	D24	1.0		
	D13 → Y2	(HL)	0.441	0.774	1.296	0.012	0.022	0.039	D25	1.1		
		(LH)	0.477	0.937	1.729	0.012	0.023	0.036	D26	1.0		
	D14 → Y2	(HL)	0.427	0.755	1.266	0.012	0.022	0.039	D27	1.0		
		(LH)	0.468	0.920	1.706	0.012	0.023	0.036	D28	1.0		
	D15 → Y2	(HL)	0.438	0.765	1.278	0.012	0.022	0.039	D29	1.0		
		(LH)	0.466	0.915	1.689	0.012	0.023	0.036	D30	1.0		
	D16 → Y2	(HL)	0.426	0.750	1.257	0.012	0.022	0.039	D31	1.0		
		(LH)	0.460	0.909	1.677	0.012	0.023	0.036	D32	1.1		
	D17 → Y3	(HL)	0.451	0.785	1.312	0.012	0.022	0.039	A	4.1		
		(LH)	0.477	0.938	1.735	0.012	0.023	0.036	B	2.0		
	D18 → Y3	(HL)	0.439	0.769	1.287	0.012	0.022	0.039	C	2.0		
		(LH)	0.472	0.929	1.719	0.012	0.023	0.036				
	D19 → Y3	(HL)	0.440	0.776	1.299	0.012	0.022	0.039				
		(LH)	0.479	0.942	1.752	0.012	0.023	0.036				
	D20 → Y3	(HL)	0.426	0.755	1.272	0.012	0.022	0.039				
		(LH)	0.471	0.929	1.722	0.012	0.023	0.036				
	D21 → Y3	(HL)	0.452	0.785	1.309	0.012	0.022	0.039				
		(LH)	0.478	0.940	1.742	0.012	0.023	0.036				
	D22 → Y3	(HL)	0.441	0.768	1.287	0.012	0.022	0.039				
		(LH)	0.472	0.931	1.728	0.012	0.023	0.036				
	D23 → Y3	(HL)	0.438	0.769	1.290	0.012	0.022	0.039				
		(LH)	0.475	0.937	1.742	0.012	0.023	0.036				
	D24 → Y3	(HL)	0.423	0.748	1.264	0.012	0.022	0.039				
		(LH)	0.467	0.923	1.713	0.012	0.023	0.036				
	D25 → Y4	(HL)	0.452	0.786	1.313	0.012	0.022	0.039				
		(LH)	0.478	0.939	1.737	0.012	0.023	0.036				
	D26 → Y4	(HL)	0.440	0.770	1.290	0.012	0.022	0.039				
		(LH)	0.472	0.930	1.721	0.012	0.023	0.036				
	D27 → Y4	(HL)	0.441	0.776	1.301	0.012	0.022	0.039				
		(LH)	0.480	0.943	1.754	0.012	0.023	0.036				
	D28 → Y4	(HL)	0.427	0.756	1.276	0.012	0.022	0.039				
		(LH)	0.471	0.930	1.724	0.012	0.023	0.036				

FUNCTION BLOCK

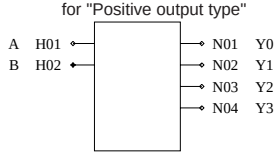
Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	D29 → Y4	(HL)	0.451	0.784	1.308	0.012	0.022	0.039				
		(LH)	0.477	0.938	1.738	0.012	0.023	0.036				
	D30 → Y4	(HL)	0.438	0.768	1.286	0.012	0.022	0.039				
		(LH)	0.471	0.930	1.723	0.012	0.023	0.036				
	D31 → Y4	(HL)	0.435	0.765	1.283	0.012	0.022	0.039				
		(LH)	0.473	0.932	1.732	0.012	0.023	0.036				
	D32 → Y4	(HL)	0.420	0.745	1.257	0.012	0.022	0.039				
		(LH)	0.465	0.919	1.704	0.012	0.023	0.036				
	A → Y1	(HH)	0.590	1.148	2.018	0.012	0.023	0.036				
		(HL)	0.625	1.154	1.955	0.012	0.022	0.039				
		(LH)	0.624	1.261	2.343	0.012	0.023	0.036				
		(LL)	0.581	1.077	1.846	0.012	0.022	0.039				
	A → Y2	(HH)	0.590	1.149	2.019	0.012	0.023	0.036				
		(HL)	0.624	1.155	1.956	0.012	0.022	0.039				
		(LH)	0.624	1.262	2.343	0.012	0.023	0.036				
		(LL)	0.580	1.078	1.847	0.012	0.022	0.039				
	A → Y3	(HH)	0.609	1.166	2.055	0.012	0.023	0.036				
		(HL)	0.631	1.165	1.974	0.012	0.022	0.039				
		(LH)	0.634	1.267	2.361	0.012	0.023	0.036				
		(LL)	0.592	1.095	1.874	0.012	0.022	0.039				
	A → Y4	(HH)	0.606	1.164	2.052	0.012	0.023	0.036				
		(HL)	0.629	1.165	1.973	0.012	0.022	0.039				
		(LH)	0.633	1.267	2.362	0.012	0.023	0.036				
		(LL)	0.589	1.093	1.871	0.012	0.022	0.039				
	B → Y1	(HH)	0.511	0.929	1.571	0.012	0.023	0.036				
		(HL)	0.590	1.078	1.810	0.012	0.022	0.039				
		(LH)	0.582	1.159	2.096	0.012	0.023	0.036				
		(LL)	0.513	0.957	1.627	0.012	0.022	0.039				
	B → Y2	(HH)	0.511	0.929	1.573	0.012	0.023	0.036				
		(HL)	0.590	1.079	1.810	0.012	0.022	0.039				
		(LH)	0.582	1.160	2.098	0.012	0.023	0.036				
		(LL)	0.512	0.958	1.629	0.012	0.022	0.039				
	B → Y3	(HH)	0.506	0.919	1.556	0.012	0.023	0.036				
		(HL)	0.587	1.074	1.805	0.012	0.022	0.039				
		(LH)	0.582	1.160	2.096	0.012	0.023	0.036				
		(LL)	0.513	0.958	1.629	0.012	0.022	0.039				
	B → Y4	(HH)	0.506	0.920	1.558	0.012	0.023	0.036				
		(HL)	0.587	1.075	1.807	0.012	0.022	0.039				
		(LH)	0.582	1.161	2.098	0.012	0.023	0.036				
		(LL)	0.513	0.959	1.630	0.012	0.022	0.039				
	C → Y1	(HH)	0.430	0.759	1.259	0.012	0.023	0.036				
		(HL)	0.326	0.561	0.916	0.012	0.022	0.039				
		(LH)	0.332	0.603	1.022	0.012	0.023	0.036				
		(LL)	0.435	0.793	1.350	0.012	0.022	0.039				
	C → Y2	(HH)	0.434	0.765	1.270	0.012	0.023	0.036				
		(HL)	0.323	0.555	0.906	0.012	0.022	0.039				
		(LH)	0.329	0.597	1.011	0.012	0.023	0.036				
		(LL)	0.439	0.800	1.361	0.012	0.022	0.039				
	C → Y3	(HH)	0.430	0.759	1.258	0.012	0.023	0.036				
		(HL)	0.326	0.561	0.916	0.012	0.022	0.039				
		(LH)	0.332	0.603	1.022	0.012	0.023	0.036				
		(LL)	0.435	0.793	1.350	0.012	0.022	0.039				
	C → Y4	(HH)	0.430	0.759	1.258	0.012	0.023	0.036				
		(HL)	0.326	0.562	0.918	0.012	0.022	0.039				
		(LH)	0.332	0.604	1.023	0.012	0.023	0.036				
		(LL)	0.435	0.793	1.350	0.012	0.022	0.039				

[MEMO]

FUNCTION BLOCK

Function	2 TO 4 DECODER						SSI Family					
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power	L560	6					L561	6	L981	8		
x1	F560	10					F561	10	F981	13		
x2												
x4												

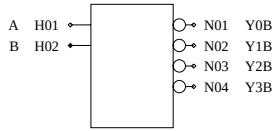
Logic Diagram for "Positive output type"



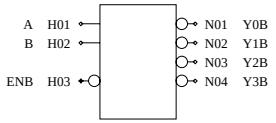
Logic Diagram for "Positive output with ENB"

Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"



Logic Diagram for "Negative output with ENB"



Logic Diagram for "Negative output with EN"

Truth Table

A	B	ENB	Y0	Y1	Y2	Y3	Y0B	Y1B	Y2B	Y3B
0	0	0	1	0	0	0	0	1	1	1
1	0	0	0	1	0	0	1	0	1	1
0	1	0	0	0	1	0	1	1	0	1
1	1	0	0	0	0	1	1	1	1	0
X	X	1	0	0	0	0	1	1	1	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
L560	A → Y0	(HL)	0.265	0.470	0.767	0.016	0.026	0.044		A	1.0	Y0	5
		(LH)	0.290	0.521	0.870	0.043	0.088	0.147		B	1.0	Y1	5
	A → Y1	(HH)	0.191	0.324	0.496	0.043	0.088	0.147				Y2	5
		(LL)	0.201	0.349	0.578	0.017	0.027	0.044				Y3	5
	A → Y2	(HL)	0.265	0.470	0.768	0.016	0.026	0.044					
		(LH)	0.290	0.521	0.870	0.043	0.088	0.147					
	A → Y3	(HH)	0.191	0.324	0.496	0.043	0.088	0.147					
		(LL)	0.201	0.349	0.578	0.017	0.027	0.044					
	B → Y0	(HL)	0.279	0.492	0.802	0.016	0.026	0.044					
		(LH)	0.301	0.551	0.928	0.043	0.087	0.146					
	B → Y1	(HL)	0.279	0.492	0.802	0.016	0.026	0.044					
		(LH)	0.301	0.551	0.929	0.043	0.087	0.146					
	B → Y2	(HH)	0.197	0.346	0.537	0.043	0.088	0.146					
		(LL)	0.216	0.377	0.627	0.017	0.027	0.044					
	B → Y3	(HH)	0.197	0.346	0.537	0.043	0.088	0.146					
		(LL)	0.217	0.377	0.627	0.017	0.027	0.044					
F560	A → Y0	(HL)	0.268	0.466	0.750	0.009	0.014	0.023		A	1.0	Y0	23
		(LH)	0.304	0.551	0.926	0.012	0.023	0.037		B	1.0	Y1	23
	A → Y1	(HH)	0.360	0.649	1.071	0.012	0.023	0.037				Y2	23
		(LL)	0.362	0.660	1.135	0.009	0.014	0.023				Y3	23
	A → Y2	(HL)	0.269	0.467	0.750	0.009	0.014	0.023					
		(LH)	0.304	0.550	0.925	0.012	0.023	0.036					
	A → Y3	(HH)	0.360	0.649	1.072	0.012	0.023	0.037					
		(LL)	0.363	0.661	1.134	0.009	0.014	0.023					
	B → Y0	(HL)	0.285	0.498	0.801	0.009	0.014	0.023					
		(LH)	0.294	0.524	0.885	0.012	0.023	0.037					
	B → Y1	(HL)	0.284	0.498	0.803	0.009	0.014	0.023					
		(LH)	0.294	0.526	0.889	0.012	0.023	0.036					
	B → Y2	(HH)	0.362	0.647	1.074	0.012	0.023	0.037					
		(LL)	0.385	0.699	1.193	0.009	0.014	0.023					
	B → Y3	(HH)	0.361	0.647	1.075	0.012	0.023	0.037					
		(LL)	0.384	0.702	1.197	0.009	0.014	0.023					
L561	A → Y0B	(HH)	0.180	0.296	0.442	0.025	0.045	0.073		A	1.0	Y0B	11
		(LL)	0.220	0.387	0.638	0.025	0.044	0.077		B	1.0	Y1B	11
	A → Y1B	(HL)	0.276	0.493	0.799	0.024	0.044	0.077				Y2B	11
		(LH)	0.280	0.498	0.832	0.025	0.045	0.073				Y3B	11
	A → Y2B	(HH)	0.180	0.295	0.443	0.025	0.045	0.073					
		(LL)	0.220	0.387	0.637	0.025	0.044	0.077					
	A → Y3B	(HL)	0.276	0.492	0.803	0.024	0.044	0.077					
		(LH)	0.281	0.498	0.834	0.025	0.045	0.073					
	B → Y0B	(HH)	0.207	0.335	0.510	0.025	0.045	0.073					
		(LL)	0.209	0.372	0.628	0.025	0.044	0.077					
	B → Y1B	(HH)	0.206	0.335	0.508	0.025	0.045	0.073					
		(LL)	0.209	0.372	0.625	0.025	0.044	0.077					
	B → Y2B	(HL)	0.293	0.510	0.841	0.024	0.044	0.076					
		(LH)	0.314	0.561	0.940	0.025	0.045	0.072					
	B → Y3B	(HL)	0.292	0.509	0.842	0.024	0.044	0.076					
		(LH)	0.314	0.560	0.937	0.025	0.045	0.072					
F561	A → Y0B	(HH)	0.365	0.646	1.069	0.013	0.023	0.037		A	1.0	Y0B	22
		(LL)	0.476	0.912	1.588	0.010	0.016	0.026		B	1.0	Y1B	22
	A → Y1B	(HL)	0.368	0.690	1.181	0.010	0.016	0.026				Y2B	22
		(LH)	0.291	0.513	0.858	0.012	0.023	0.037				Y3B	22
	A → Y2B	(HH)	0.365	0.646	1.068	0.012	0.023	0.037					
		(LL)	0.475	0.911	1.590	0.010	0.016	0.026					
	A → Y3B	(HL)	0.368	0.690	1.181	0.010	0.016	0.026					
		(LH)	0.291	0.513	0.857	0.012	0.023	0.037					

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B → Y0B	(HH)	0.377	0.663	1.095	0.012	0.023	0.037				
		(LL)	0.485	0.937	1.631	0.010	0.016	0.026				
	B → Y1B	(HH)	0.376	0.663	1.095	0.012	0.023	0.037				
		(LL)	0.484	0.937	1.631	0.010	0.016	0.026				
	B → Y2B	(HL)	0.373	0.710	1.219	0.010	0.016	0.026				
		(LH)	0.305	0.538	0.896	0.012	0.023	0.037				
	B → Y3B	(HL)	0.372	0.710	1.220	0.010	0.016	0.026				
		(LH)	0.305	0.538	0.896	0.012	0.023	0.037				
L981	A → Y0B	(HH)	0.193	0.315	0.468	0.025	0.045	0.073	A	1.0	Y0B	11
		(LL)	0.224	0.402	0.668	0.025	0.044	0.077	B	1.0	Y1B	11
	A → Y1B	(HL)	0.293	0.530	0.854	0.025	0.044	0.077	ENB	2.0	Y2B	11
		(LH)	0.298	0.531	0.889	0.025	0.045	0.072			Y3B	11
	A → Y2B	(HH)	0.193	0.315	0.468	0.025	0.045	0.073				
		(LL)	0.224	0.402	0.668	0.025	0.044	0.077				
	A → Y3B	(HL)	0.292	0.529	0.853	0.025	0.044	0.077				
		(LH)	0.298	0.530	0.889	0.025	0.045	0.072				
	B → Y0B	(HH)	0.331	0.588	0.959	0.024	0.045	0.072				
		(LL)	0.433	0.833	1.473	0.024	0.044	0.077				
	B → Y1B	(HH)	0.331	0.589	0.959	0.024	0.045	0.072				
		(LL)	0.433	0.834	1.475	0.025	0.044	0.077				
	B → Y2B	(HL)	0.360	0.691	1.200	0.024	0.044	0.077				
		(LH)	0.292	0.511	0.846	0.025	0.045	0.072				
	B → Y3B	(HL)	0.360	0.691	1.199	0.024	0.044	0.077				
		(LH)	0.292	0.511	0.845	0.025	0.045	0.072				
	ENB → Y0B	(HH)	0.205	0.335	0.510	0.024	0.045	0.072				
		(LL)	0.270	0.546	0.994	0.024	0.044	0.077				
	ENB → Y1B	(HH)	0.204	0.336	0.511	0.025	0.045	0.072				
		(LL)	0.272	0.548	0.999	0.024	0.044	0.077				
	ENB → Y2B	(HH)	0.204	0.335	0.508	0.025	0.045	0.072				
		(LL)	0.269	0.543	0.991	0.024	0.044	0.077				
	ENB → Y3B	(HH)	0.204	0.335	0.509	0.025	0.045	0.072				
		(LL)	0.269	0.545	0.995	0.024	0.044	0.077				
F981	A → Y0B	(HH)	0.382	0.672	1.106	0.012	0.023	0.036	A	1.0	Y0B	22
		(LL)	0.499	0.950	1.653	0.011	0.017	0.027	B	1.1	Y1B	22
	A → Y1B	(HL)	0.390	0.718	1.216	0.011	0.017	0.027	ENB	1.0	Y2B	22
		(LH)	0.304	0.540	0.904	0.012	0.023	0.036			Y3B	22
	A → Y2B	(HH)	0.382	0.672	1.106	0.012	0.023	0.036				
		(LL)	0.499	0.950	1.653	0.011	0.017	0.027				
	A → Y3B	(HL)	0.390	0.718	1.216	0.011	0.017	0.027				
		(LH)	0.304	0.540	0.904	0.012	0.023	0.036				
	B → Y0B	(HH)	0.360	0.641	1.049	0.012	0.023	0.036				
		(LL)	0.484	0.940	1.644	0.011	0.017	0.027				
	B → Y1B	(HH)	0.360	0.641	1.049	0.012	0.023	0.036				
		(LL)	0.484	0.940	1.643	0.011	0.017	0.027				
	B → Y2B	(HL)	0.517	1.005	1.741	0.011	0.017	0.027				
		(LH)	0.427	0.772	1.303	0.012	0.023	0.036				
	B → Y3B	(HL)	0.517	1.005	1.741	0.011	0.017	0.027				
		(LH)	0.427	0.772	1.304	0.012	0.023	0.036				
	ENB → Y0B	(HH)	0.390	0.693	1.133	0.012	0.023	0.037				
		(LL)	0.497	0.961	1.687	0.011	0.017	0.027				
	ENB → Y1B	(HH)	0.391	0.693	1.133	0.012	0.023	0.037				
		(LL)	0.497	0.963	1.687	0.011	0.017	0.027				
	ENB → Y2B	(HH)	0.388	0.689	1.125	0.012	0.023	0.037				
		(LL)	0.496	0.958	1.679	0.011	0.017	0.027				
	ENB → Y3B	(HH)	0.388	0.689	1.125	0.012	0.023	0.037				
		(LL)	0.496	0.958	1.679	0.011	0.017	0.027				

[MEMO]

FUNCTION BLOCK

Function	3 TO 8 DECODER										SSI Family	
Block type	Positive output type						Negative output type					
	Normal		with ENB		with EN		Normal		with ENB		with EN	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power									L982	21		
x1									F982	26		
x2												
x4												

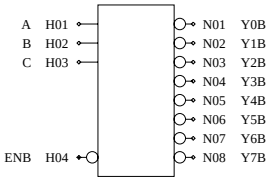
Logic Diagram for "Positive output type"

Logic Diagram for "Positive output with ENB"

Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"

Logic Diagram for "Negative output with ENB"



Logic Diagram for "Negative output with EN"

Truth Table

A	B	C	ENB	Y0B	Y1B	Y2B	Y3B	Y4B	Y5B	Y6B	Y7B
0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1
0	1	0	0	1	1	0	1	1	1	1	1
1	1	0	0	1	1	1	0	1	1	1	1
0	0	1	0	1	1	1	1	0	1	1	1
1	0	1	0	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
1	1	1	0	1	1	1	1	1	1	1	0
X	X	X	1	1	1	1	1	1	1	1	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t_{LD0} (ns)			t_1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
L982	A → Y0B	(HH)	0.254	0.409	0.627	0.025	0.045	0.073	A	1.0	Y0B	8
		(LL)	0.323	0.599	1.010	0.038	0.068	0.117	B	1.1	Y1B	8
	A → Y1B	(HL)	0.439	0.790	1.317	0.038	0.068	0.117	C	1.0	Y2B	8
		(LH)	0.426	0.782	1.336	0.025	0.045	0.073	ENB	2.0	Y3B	8
	A → Y2B	(HH)	0.253	0.408	0.627	0.025	0.045	0.073			Y4B	8
		(LL)	0.324	0.599	1.005	0.038	0.068	0.117			Y5B	8
	A → Y3B	(HL)	0.439	0.791	1.319	0.038	0.068	0.117			Y6B	8
		(LH)	0.427	0.784	1.337	0.025	0.045	0.073			Y7B	8
	A → Y4B	(HH)	0.254	0.408	0.627	0.025	0.045	0.073				
		(LL)	0.323	0.599	1.007	0.038	0.068	0.117				
	A → Y5B	(HL)	0.439	0.791	1.319	0.038	0.068	0.117				
		(LH)	0.426	0.783	1.338	0.025	0.045	0.073				
	A → Y6B	(HH)	0.254	0.409	0.627	0.025	0.045	0.073				
		(LL)	0.324	0.599	1.010	0.038	0.068	0.117				
	A → Y7B	(HL)	0.438	0.791	1.317	0.038	0.068	0.117				
		(LH)	0.426	0.783	1.338	0.025	0.045	0.073				
	B → Y0B	(HH)	0.277	0.450	0.699	0.025	0.045	0.072				
		(LL)	0.330	0.597	1.010	0.038	0.068	0.117				
	B → Y1B	(HH)	0.277	0.449	0.697	0.025	0.045	0.072				
		(LL)	0.329	0.596	1.008	0.038	0.068	0.117				
	B → Y2B	(HL)	0.453	0.808	1.353	0.038	0.068	0.116				
		(LH)	0.464	0.843	1.437	0.025	0.045	0.072				
	B → Y3B	(HL)	0.454	0.808	1.354	0.038	0.068	0.116				
		(LH)	0.464	0.844	1.438	0.025	0.045	0.072				
	B → Y4B	(HH)	0.278	0.449	0.698	0.025	0.045	0.072				
		(LL)	0.329	0.596	1.008	0.038	0.068	0.117				
	B → Y5B	(HH)	0.277	0.450	0.700	0.025	0.045	0.072				
		(LL)	0.328	0.597	1.010	0.038	0.068	0.117				
	B → Y6B	(HL)	0.454	0.808	1.353	0.038	0.068	0.116				
		(LH)	0.464	0.844	1.438	0.025	0.045	0.072				
	B → Y7B	(HL)	0.453	0.807	1.352	0.038	0.068	0.116				
		(LH)	0.462	0.844	1.436	0.025	0.045	0.072				
	C → Y0B	(HH)	0.411	0.734	1.200	0.024	0.045	0.072				
		(LL)	0.565	1.118	1.994	0.038	0.068	0.117				
	C → Y1B	(HH)	0.410	0.730	1.195	0.024	0.045	0.072				
		(LL)	0.562	1.112	1.984	0.038	0.068	0.117				
	C → Y2B	(HH)	0.410	0.731	1.195	0.024	0.045	0.072				
		(LL)	0.563	1.114	1.985	0.038	0.068	0.117				
	C → Y3B	(HH)	0.411	0.734	1.200	0.024	0.045	0.072				
		(LL)	0.564	1.118	1.992	0.038	0.068	0.117				
	C → Y4B	(HL)	0.493	0.976	1.729	0.038	0.068	0.117				
		(LH)	0.376	0.663	1.093	0.024	0.045	0.072				
	C → Y5B	(HL)	0.495	0.982	1.738	0.038	0.068	0.117				
		(LH)	0.378	0.667	1.100	0.024	0.045	0.072				
	C → Y6B	(HL)	0.495	0.982	1.739	0.038	0.068	0.117				
		(LH)	0.378	0.667	1.099	0.024	0.045	0.072				
	C → Y7B	(HL)	0.493	0.975	1.727	0.038	0.068	0.117				
		(LH)	0.376	0.663	1.096	0.024	0.045	0.072				
	ENB → Y0B	(HH)	0.291	0.477	0.742	0.025	0.045	0.073				
		(LL)	0.398	0.831	1.527	0.038	0.068	0.118				
	ENB → Y1B	(HH)	0.289	0.474	0.737	0.025	0.045	0.073				
		(LL)	0.395	0.827	1.513	0.038	0.068	0.118				
	ENB → Y2B	(HH)	0.289	0.474	0.737	0.025	0.045	0.073				
		(LL)	0.395	0.826	1.517	0.038	0.068	0.117				
	ENB → Y3B	(HH)	0.291	0.477	0.742	0.025	0.045	0.073				
		(LL)	0.397	0.831	1.525	0.038	0.068	0.118				

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	ENB → Y4B	(HH)	0.290	0.476	0.742	0.025	0.045	0.073				
		(LL)	0.398	0.831	1.527	0.038	0.068	0.117				
	ENB → Y5B	(HH)	0.292	0.480	0.747	0.025	0.045	0.073				
		(LL)	0.400	0.837	1.536	0.038	0.068	0.118				
	ENB → Y6B	(HH)	0.292	0.480	0.747	0.025	0.045	0.073				
		(LL)	0.401	0.837	1.538	0.038	0.068	0.118				
	ENB → Y7B	(HH)	0.290	0.476	0.742	0.025	0.045	0.073				
		(LL)	0.397	0.831	1.525	0.038	0.068	0.118				
F982	A → Y0B	(HH)	0.519	0.925	1.557	0.012	0.023	0.036	A	1.0	Y0B	22
		(LL)	0.753	1.460	2.585	0.011	0.018	0.030	B	1.0	Y1B	22
	A → Y1B	(HL)	0.566	1.054	1.819	0.011	0.018	0.030	C	1.0	Y2B	22
		(LH)	0.382	0.699	1.201	0.012	0.023	0.036	ENB	1.1	Y3B	22
	A → Y2B	(HH)	0.518	0.924	1.555	0.012	0.023	0.036			Y4B	22
		(LL)	0.751	1.459	2.579	0.011	0.018	0.030			Y5B	22
	A → Y3B	(HL)	0.567	1.057	1.821	0.011	0.018	0.029			Y6B	22
		(LH)	0.383	0.701	1.203	0.012	0.023	0.036			Y7B	22
	A → Y4B	(HH)	0.519	0.925	1.557	0.012	0.023	0.036				
		(LL)	0.753	1.460	2.585	0.011	0.018	0.030				
	A → Y5B	(HL)	0.566	1.054	1.819	0.011	0.018	0.030				
		(LH)	0.382	0.699	1.201	0.012	0.023	0.036				
	A → Y6B	(HH)	0.518	0.924	1.555	0.012	0.023	0.036				
		(LL)	0.751	1.459	2.579	0.011	0.018	0.030				
	A → Y7B	(HL)	0.567	1.057	1.821	0.011	0.018	0.029				
		(LH)	0.383	0.701	1.203	0.012	0.023	0.036				
	B → Y0B	(HH)	0.533	0.950	1.596	0.012	0.023	0.036				
		(LL)	0.762	1.498	2.653	0.011	0.018	0.030				
	B → Y1B	(HH)	0.532	0.949	1.595	0.012	0.023	0.036				
		(LL)	0.760	1.497	2.651	0.011	0.018	0.030				
	B → Y2B	(HL)	0.566	1.086	1.883	0.011	0.018	0.030				
		(LH)	0.395	0.719	1.232	0.012	0.023	0.036				
	B → Y3B	(HL)	0.567	1.089	1.888	0.011	0.018	0.029				
		(LH)	0.396	0.721	1.234	0.012	0.023	0.036				
	B → Y4B	(HH)	0.533	0.950	1.596	0.012	0.023	0.036				
		(LL)	0.762	1.498	2.653	0.011	0.018	0.030				
	B → Y5B	(HH)	0.532	0.949	1.595	0.012	0.023	0.036				
		(LL)	0.760	1.497	2.651	0.011	0.018	0.030				
	B → Y6B	(HL)	0.566	1.086	1.883	0.011	0.018	0.030				
		(LH)	0.395	0.719	1.232	0.012	0.023	0.036				
	B → Y7B	(HL)	0.567	1.088	1.888	0.011	0.018	0.029				
		(LH)	0.396	0.721	1.234	0.012	0.023	0.036				
	C → Y0B	(HH)	0.450	0.819	1.370	0.012	0.023	0.036				
		(LL)	0.703	1.403	2.479	0.011	0.018	0.029				
	C → Y1B	(HH)	0.449	0.818	1.369	0.012	0.023	0.036				
		(LL)	0.702	1.401	2.476	0.011	0.018	0.030				
	C → Y2B	(HH)	0.449	0.818	1.369	0.012	0.023	0.036				
		(LL)	0.702	1.405	2.477	0.011	0.018	0.030				
	C → Y3B	(HH)	0.450	0.819	1.371	0.012	0.023	0.036				
		(LL)	0.702	1.404	2.478	0.011	0.018	0.029				
	C → Y4B	(HL)	0.738	1.472	2.575	0.011	0.018	0.030				
		(LH)	0.520	0.954	1.636	0.012	0.023	0.036				
	C → Y5B	(HL)	0.737	1.469	2.572	0.011	0.018	0.030				
		(LH)	0.520	0.952	1.633	0.012	0.023	0.036				
	C → Y6B	(HL)	0.737	1.469	2.572	0.011	0.018	0.030				
		(LH)	0.519	0.953	1.633	0.012	0.023	0.036				
	C → Y7B	(HL)	0.738	1.472	2.576	0.011	0.018	0.030				
		(LH)	0.521	0.954	1.634	0.012	0.023	0.036				

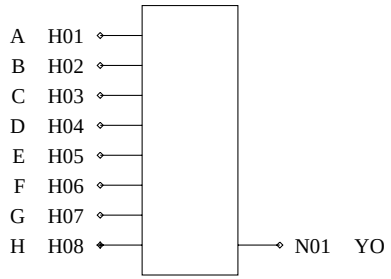
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	ENB → Y0B	(HH)	0.471	0.858	1.437	0.013	0.023	0.037				
		(LL)	0.707	1.408	2.490	0.011	0.018	0.030				
	ENB → Y1B	(HH)	0.470	0.856	1.434	0.013	0.023	0.037				
		(LL)	0.707	1.407	2.487	0.011	0.018	0.030				
	ENB → Y2B	(HH)	0.470	0.856	1.435	0.012	0.023	0.037				
		(LL)	0.706	1.406	2.488	0.011	0.018	0.030				
	ENB → Y3B	(HH)	0.471	0.858	1.436	0.013	0.023	0.037				
		(LL)	0.708	1.408	2.489	0.011	0.018	0.030				
	ENB → Y4B	(HH)	0.473	0.861	1.442	0.013	0.023	0.037				
		(LL)	0.709	1.413	2.494	0.011	0.018	0.030				
	ENB → Y5B	(HH)	0.472	0.860	1.441	0.013	0.023	0.037				
		(LL)	0.708	1.410	2.490	0.011	0.018	0.030				
	ENB → Y6B	(HH)	0.472	0.860	1.441	0.013	0.023	0.037				
		(LL)	0.708	1.411	2.492	0.011	0.018	0.030				
	ENB → Y7B	(HH)	0.473	0.861	1.443	0.013	0.023	0.037				
		(LL)	0.709	1.411	2.493	0.011	0.018	0.030				

FUNCTION BLOCK

Function	8-BIT ODD PARITY GENERATOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F581	19					
x2							
x4							

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YO
&2 of 1's at A through H is Odd								1
&2 of 1's at A through H is Even								0

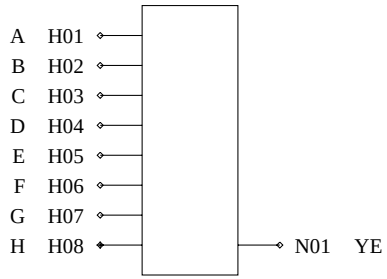
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F581	A → YO	(HH)	0.599	1.121	1.905	0.013	0.023	0.037	A	2.1	YO	22
		(HL)	0.622	1.193	2.036	0.009	0.015	0.024	B	2.1		
		(LH)	0.620	1.168	1.992	0.013	0.023	0.037	C	2.1		
		(LL)	0.682	1.382	2.424	0.009	0.015	0.024	D	2.1		
	B → YO	(HH)	0.568	1.065	1.817	0.013	0.023	0.037	E	2.1		
		(HL)	0.611	1.179	2.043	0.009	0.015	0.024	F	2.1		
		(LH)	0.683	1.259	2.130	0.013	0.023	0.037	G	2.1		
		(LL)	0.682	1.332	2.329	0.009	0.015	0.024	H	2.1		
	C → YO	(HH)	0.654	1.207	2.034	0.013	0.023	0.037				
		(HL)	0.610	1.167	2.001	0.009	0.015	0.024				
		(LH)	0.676	1.254	2.118	0.013	0.023	0.037				
		(LL)	0.658	1.328	2.338	0.009	0.015	0.024				
	D → YO	(HH)	0.623	1.149	1.944	0.013	0.023	0.037				
		(HL)	0.599	1.154	2.007	0.009	0.015	0.024				
		(LH)	0.739	1.346	2.261	0.013	0.023	0.037				
		(LL)	0.658	1.278	2.242	0.009	0.015	0.024				
	E → YO	(HH)	0.654	1.207	2.035	0.013	0.023	0.037				
		(HL)	0.612	1.167	2.004	0.009	0.015	0.024				
		(LH)	0.677	1.258	2.122	0.013	0.023	0.037				
		(LL)	0.670	1.349	2.377	0.009	0.015	0.024				
	F → YO	(HH)	0.625	1.152	1.946	0.013	0.023	0.037				
		(HL)	0.601	1.156	2.009	0.009	0.015	0.024				
		(LH)	0.741	1.348	2.263	0.013	0.023	0.037				
		(LL)	0.669	1.303	2.281	0.009	0.015	0.024				
	G → YO	(HH)	0.725	1.316	2.195	0.013	0.023	0.037				
		(HL)	0.610	1.162	1.999	0.009	0.015	0.024				
		(LH)	0.745	1.361	2.283	0.013	0.023	0.037				
		(LL)	0.659	1.329	2.346	0.009	0.015	0.024				
	H → YO	(HH)	0.692	1.259	2.108	0.013	0.023	0.037				
		(HL)	0.599	1.148	2.001	0.009	0.015	0.024				
		(LH)	0.807	1.456	2.426	0.013	0.023	0.037				
		(LL)	0.659	1.278	2.252	0.009	0.015	0.024				

FUNCTION BLOCK

Function	8-BIT EVEN PARITY GENERATOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F582	19					
x2							
x4							

Logic Diagram



Truth Table

A	B	C	D	E	F	G	H	YE
&2 of 1's at A through H is Odd								0
&2 of 1's at A through H is Even								1

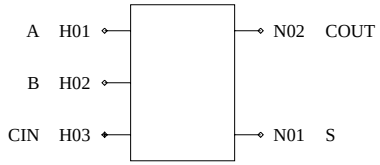
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F582	A → YE	(HH)	0.600	1.119	1.891	0.013	0.023	0.037	A	2.1	YE	21
		(HL)	0.677	1.319	2.276	0.010	0.016	0.026	B	2.1		
		(LH)	0.661	1.310	2.280	0.013	0.023	0.037	C	2.1		
		(LL)	0.698	1.366	2.366	0.010	0.016	0.026	D	2.1		
	B → YE	(HH)	0.590	1.106	1.896	0.013	0.023	0.037	E	2.1		
		(HL)	0.645	1.263	2.191	0.010	0.016	0.026	F	2.1		
		(LH)	0.661	1.259	2.186	0.013	0.023	0.037	G	2.1		
		(LL)	0.760	1.457	2.503	0.010	0.016	0.026	H	2.1		
	C → YE	(HH)	0.587	1.093	1.853	0.013	0.023	0.037				
		(HL)	0.715	1.386	2.380	0.010	0.016	0.026				
		(LH)	0.635	1.249	2.184	0.013	0.023	0.037				
		(LL)	0.737	1.432	2.466	0.010	0.016	0.026				
	D → YE	(HH)	0.577	1.077	1.856	0.013	0.023	0.037				
		(HL)	0.682	1.324	2.289	0.010	0.016	0.026				
		(LH)	0.635	1.198	2.090	0.013	0.023	0.037				
		(LL)	0.800	1.523	2.605	0.010	0.016	0.026				
	E → YE	(HH)	0.603	1.121	1.880	0.013	0.023	0.037				
		(HL)	0.613	1.190	2.060	0.010	0.016	0.025				
		(LH)	0.660	1.304	2.253	0.013	0.023	0.037				
		(LL)	0.636	1.241	2.145	0.010	0.016	0.025				
	F → YE	(HH)	0.592	1.110	1.887	0.013	0.023	0.037				
		(HL)	0.584	1.135	1.971	0.010	0.016	0.025				
		(LH)	0.661	1.255	2.160	0.013	0.023	0.037				
		(LL)	0.699	1.329	2.286	0.010	0.016	0.025				
	G → YE	(HH)	0.601	1.116	1.878	0.013	0.023	0.037				
		(HL)	0.675	1.291	2.215	0.010	0.016	0.025				
		(LH)	0.652	1.283	2.226	0.013	0.023	0.037				
		(LL)	0.696	1.337	2.300	0.010	0.016	0.026				
	H → YE	(HH)	0.590	1.103	1.884	0.013	0.023	0.037				
		(HL)	0.644	1.234	2.122	0.010	0.016	0.025				
		(LH)	0.652	1.233	2.130	0.013	0.023	0.037				
		(LL)	0.759	1.433	2.440	0.010	0.016	0.026				

FUNCTION BLOCK

Function	1-BIT FULL ADDER					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F521	9					
x2							
x4							

Logic Diagram



Truth Table

A	B	CIN	S	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

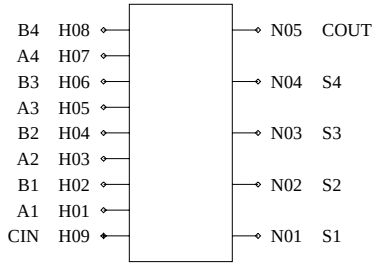
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F521	A → S	(HH)	0.476	0.910	1.552	0.012	0.023	0.037	A	2.1	S	22
		(HL)	0.493	1.045	1.804	0.009	0.016	0.026	B	2.1	COUT	22
		(LH)	0.530	1.439	2.407	0.012	0.023	0.037	CIN	1.0		
		(LL)	0.570	1.529	2.604	0.009	0.016	0.026				
	A → COUT	(HH)	0.425	0.992	1.679	0.013	0.023	0.037				
		(LL)	0.318	1.165	2.061	0.010	0.015	0.025				
	B → S	(HH)	0.465	1.001	1.640	0.013	0.023	0.037				
		(HL)	0.527	1.083	1.841	0.009	0.016	0.026				
		(LH)	0.533	1.309	2.220	0.012	0.023	0.037				
		(LL)	0.573	1.395	2.408	0.009	0.016	0.026				
	B → COUT	(HH)	0.460	1.004	1.670	0.013	0.023	0.037				
		(LL)	0.282	1.215	2.140	0.010	0.015	0.025				
	CIN → S	(HH)	0.368	0.650	1.056	0.013	0.023	0.037				
		(HL)	0.478	0.907	1.528	0.010	0.016	0.026				
		(LH)	0.450	0.811	1.349	0.013	0.023	0.037				
		(LL)	0.391	0.724	1.228	0.009	0.015	0.024				
	CIN → COUT	(HH)	0.304	0.497	0.788	0.013	0.023	0.037				
		(LL)	0.342	0.647	1.196	0.010	0.016	0.026				

FUNCTION BLOCK

Function	4-BIT BINARY FULL ADDER				SSI Family	
Block type	Standard type					
	Normal		High speed			
Drivability	Name	cells	Name	cells		
Low Power						
x1	F523	34				
x2						
x4						

Logic Diagram



Truth Table

An	Bn	CIN	Sn	COUT
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

(Condition of one stage, n=1,2,3 4)

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F523	A1 → S1		(HH)	0.438	0.807	1.375	0.012	0.023	0.037	A1	2.1	S1	22
			(HL)	0.539	1.030	1.777	0.010	0.016	0.025	B1	2.1	S2	22
			(LH)	0.836	1.565	2.657	0.012	0.023	0.036	A2	2.0	S3	22
			(LL)	0.601	1.193	2.107	0.010	0.016	0.026	B2	2.1	S4	22
	A1 → S2		(HH)	0.773	1.471	2.517	0.013	0.023	0.037	A3	2.1	COUT	20
			(HL)	1.267	2.198	3.534	0.011	0.017	0.028	B3	2.1		
			(LH)	0.838	1.696	2.911	0.013	0.023	0.037	A4	2.1		
			(LL)	0.589	1.147	2.025	0.010	0.016	0.026	B4	2.1		
	A1 → S3		(HH)	1.048	1.967	3.384	0.012	0.023	0.036	CIN	2.0		
			(HL)	1.548	2.821	4.616	0.010	0.016	0.026				
			(LH)	1.074	2.148	3.916	0.013	0.023	0.037				
			(LL)	0.818	1.626	3.006	0.009	0.015	0.024				
	A1 → S4		(HH)	1.343	2.507	4.339	0.012	0.023	0.036				
			(HL)	1.691	3.085	5.271	0.011	0.017	0.027				
			(LH)	1.157	2.376	4.657	0.013	0.023	0.037				
			(LL)	1.057	2.143	4.188	0.010	0.016	0.026				
	A1 → COUT		(HH)	1.479	2.693	4.631	0.016	0.029	0.045				
			(LL)	1.068	2.211	4.575	0.014	0.025	0.039				
	B1 → S1		(HH)	0.479	0.872	1.474	0.012	0.023	0.037				
			(HL)	0.556	1.046	1.775	0.010	0.016	0.025				
			(LH)	0.733	1.411	2.428	0.012	0.023	0.037				
			(LL)	0.604	1.244	2.200	0.010	0.016	0.026				
	B1 → S2		(HH)	0.790	1.487	2.516	0.013	0.023	0.037				
			(HL)	1.286	2.215	3.532	0.011	0.017	0.028				
			(LH)	0.797	1.631	2.814	0.013	0.023	0.037				
			(LL)	0.572	1.105	1.952	0.010	0.016	0.026				
	B1 → S3		(HH)	1.065	1.984	3.381	0.012	0.023	0.036				
			(HL)	1.565	2.839	4.613	0.010	0.016	0.026				
			(LH)	1.032	2.088	3.827	0.013	0.023	0.037				
			(LL)	0.790	1.576	2.927	0.009	0.015	0.024				
	B1 → S4		(HH)	1.361	2.523	4.336	0.012	0.023	0.036				
			(HL)	1.707	3.103	5.269	0.011	0.017	0.027				
			(LH)	1.117	2.319	4.572	0.013	0.023	0.037				
			(LL)	1.023	2.092	4.107	0.010	0.016	0.026				
	B1 → COUT		(HH)	1.496	2.709	4.629	0.016	0.029	0.045				
			(LL)	1.027	2.153	4.490	0.014	0.025	0.039				
	A2 → S2		(HH)	0.505	0.910	1.530	0.013	0.023	0.037				
			(HL)	0.527	1.000	1.730	0.010	0.016	0.025				
			(LH)	0.923	1.681	2.804	0.013	0.023	0.037				
			(LL)	0.574	1.135	2.018	0.010	0.016	0.025				
	A2 → S3		(HH)	0.765	1.456	2.491	0.012	0.023	0.037				
			(HL)	1.102	2.071	3.440	0.010	0.016	0.026				
			(LH)	0.786	1.521	2.621	0.013	0.023	0.037				
			(LL)	0.575	1.127	2.010	0.009	0.015	0.024				
	A2 → S4		(HH)	0.998	1.889	3.265	0.012	0.023	0.036				
			(HL)	1.241	2.352	4.040	0.011	0.017	0.027				
			(LH)	0.870	1.757	3.334	0.013	0.023	0.037				
			(LL)	0.785	1.567	2.928	0.010	0.016	0.026				
	A2 → COUT		(HH)	1.063	1.975	3.405	0.014	0.027	0.042				
			(LL)	0.781	1.599	3.294	0.013	0.024	0.038				
	B2 → S2		(HH)	0.564	1.003	1.662	0.013	0.023	0.037				
			(HL)	0.544	1.015	1.730	0.010	0.016	0.025				
			(LH)	0.799	1.500	2.542	0.013	0.023	0.037				
			(LL)	0.594	1.219	2.161	0.010	0.016	0.026				
	B2 → S3		(HH)	0.782	1.472	2.489	0.012	0.023	0.037				
			(HL)	1.120	2.083	3.434	0.010	0.016	0.026				

FUNCTION BLOCK

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
		(LH)	0.771	1.496	2.564	0.013	0.023	0.037				
		(LL)	0.562	1.097	1.940	0.009	0.015	0.024				
	B2 → S4	(HH)	1.014	1.905	3.265	0.012	0.023	0.036				
		(HL)	1.259	2.368	4.036	0.011	0.017	0.027				
		(LH)	0.858	1.741	3.326	0.013	0.023	0.037				
		(LL)	0.763	1.528	2.876	0.010	0.016	0.026				
	B2 → COUT	(HH)	1.080	1.990	3.402	0.014	0.027	0.042				
		(LL)	0.768	1.580	3.280	0.014	0.024	0.038				
	A3 → S3	(HH)	0.545	0.954	1.587	0.013	0.023	0.037				
		(HL)	0.527	1.002	1.739	0.009	0.015	0.024				
		(LH)	0.904	1.623	2.694	0.013	0.023	0.037				
		(LL)	0.574	1.132	2.012	0.009	0.015	0.024				
	A3 → S4	(HH)	0.757	1.436	2.455	0.012	0.023	0.037				
		(HL)	0.951	1.830	3.126	0.011	0.017	0.027				
		(LH)	0.652	1.259	2.194	0.012	0.023	0.037				
		(LL)	0.577	1.124	1.993	0.010	0.016	0.026				
	A3 → COUT	(HH)	0.784	1.455	2.481	0.014	0.025	0.039				
		(LL)	0.562	1.115	2.106	0.011	0.019	0.031				
	B3 → S3	(HH)	0.584	1.022	1.689	0.013	0.023	0.037				
		(HL)	0.545	1.018	1.737	0.009	0.015	0.024				
		(LH)	0.810	1.483	2.490	0.013	0.023	0.037				
		(LL)	0.576	1.184	2.109	0.009	0.015	0.024				
	B3 → S4	(HH)	0.774	1.452	2.452	0.012	0.023	0.037				
		(HL)	0.969	1.846	3.123	0.011	0.017	0.027				
		(LH)	0.629	1.214	2.118	0.012	0.023	0.037				
		(LL)	0.561	1.085	1.921	0.010	0.016	0.026				
	B3 → COUT	(HH)	0.801	1.470	2.479	0.014	0.025	0.039				
		(LL)	0.542	1.074	2.038	0.011	0.019	0.031				
	A4 → S4	(HH)	0.496	0.898	1.510	0.013	0.023	0.037				
		(HL)	0.511	0.970	1.683	0.010	0.016	0.026				
		(LH)	0.778	1.407	2.357	0.012	0.023	0.037				
		(LL)	0.566	1.120	1.990	0.010	0.016	0.026				
	A4 → COUT	(HH)	0.511	0.967	1.641	0.013	0.023	0.037				
		(LL)	0.332	0.634	1.139	0.010	0.015	0.025				
	B4 → S4	(HH)	0.538	0.964	1.617	0.013	0.023	0.037				
		(HL)	0.526	0.984	1.678	0.010	0.016	0.026				
		(LH)	0.695	1.283	2.167	0.013	0.023	0.037				
		(LL)	0.568	1.172	2.089	0.010	0.016	0.026				
	B4 → COUT	(HH)	0.527	0.981	1.635	0.013	0.023	0.037				
		(LL)	0.315	0.599	1.074	0.010	0.015	0.025				
	CIN → S1	(HH)	0.387	0.677	1.090	0.013	0.023	0.037				
		(HL)	0.478	0.863	1.421	0.011	0.017	0.027				
		(LH)	0.346	0.622	1.038	0.012	0.023	0.037				
		(LL)	0.324	0.599	1.012	0.010	0.016	0.026				
	CIN → S2	(HH)	0.465	0.821	1.351	0.013	0.023	0.037				
		(HL)	0.737	1.236	2.004	0.011	0.017	0.027				
		(LH)	0.579	1.186	2.206	0.013	0.023	0.037				
		(LL)	0.464	0.895	1.615	0.010	0.016	0.026				
	CIN → S3	(HH)	0.668	1.181	1.972	0.012	0.023	0.036				
		(HL)	1.045	1.809	2.897	0.010	0.016	0.026				
		(LH)	0.842	1.715	3.288	0.013	0.023	0.037				
		(LL)	0.636	1.282	2.490	0.009	0.015	0.024				
	CIN → S4	(HH)	0.911	1.610	2.720	0.012	0.023	0.036				
		(HL)	1.185	2.088	3.495	0.011	0.017	0.027				
		(LH)	0.935	1.957	4.045	0.013	0.023	0.037				
		(LL)	0.839	1.741	3.593	0.010	0.016	0.026				

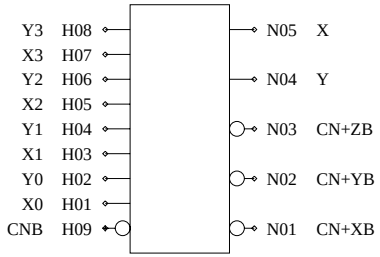
FUNCTION BLOCK

Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	CIN → COUT	(HH)	0.997	1.708	2.861	0.015	0.027	0.042				
		(LL)	0.842	1.788	3.955	0.014	0.025	0.039				

FUNCTION BLOCK

Function	4-BIT LOOK AHEAD CARRY GENERATOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F526	34					
x2							
x4							

Logic Diagram



Truth Table

Y3	Y2	Y1	Y0	X3	X2	X1	Y
0	X	X	X	X	X	X	1
X	0	X	X	0	X	X	1
X	X	0	X	0	0	X	1
X	X	X	0	0	0	0	1
All other combinations							0

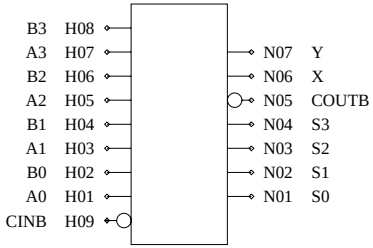
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F526	X0 → CN+XB	(HL)	0.149	0.204	0.263	0.018	0.028	0.046	X0	7.4	CN+XB	10
		(LH)	0.153	0.268	0.434	0.024	0.046	0.076	Y0	12.2	CN+YB	5
	X0 → CN+YB	(HL)	0.174	0.240	0.304	0.019	0.034	0.058	X1	6.2	CN+ZB	22
		(LH)	0.222	0.434	0.755	0.034	0.069	0.114	Y1	12.2	X	19
	X0 → CN+ZB	(HL)	0.502	0.859	1.349	0.010	0.016	0.026	X2	4.1	Y	22
		(LH)	0.451	0.886	1.543	0.012	0.023	0.037	Y2	8.3		
	X0 → Y	(HH)	0.168	0.277	0.413	0.012	0.023	0.036	X3	2.5		
		(LL)	0.429	0.861	1.573	0.012	0.019	0.031	Y3	4.4		
	Y0 → CN+XB	(HL)	0.093	0.259	0.254	0.018	0.029	0.046	CNB	2.0		
		(LH)	0.147	0.268	0.395	0.018	0.036	0.056				
	Y0 → CN+YB	(HL)	0.115	0.332	0.277	0.019	0.034	0.057				
		(LH)	0.203	0.485	0.624	0.029	0.059	0.096				
	Y0 → CN+ZB	(HL)	0.387	0.923	1.150	0.010	0.016	0.025				
		(LH)	0.357	0.752	1.130	0.012	0.023	0.037				
	Y0 → X	(HH)	0.333	0.579	0.935	0.013	0.024	0.038				
		(LL)	0.323	0.613	1.059	0.019	0.030	0.048				
	X1 → CN+YB	(HL)	0.187	0.290	0.386	0.012	0.022	0.040				
		(LH)	0.347	0.502	1.176	0.029	0.047	0.095				
	X1 → CN+ZB	(HL)	0.357	0.635	1.042	0.010	0.016	0.025				
		(LH)	0.367	0.702	1.216	0.012	0.023	0.037				
	X1 → X	(HH)	0.429	0.748	1.224	0.013	0.024	0.038				
		(LL)	0.408	0.815	1.378	0.019	0.030	0.048				
	X1 → Y	(HH)	0.178	0.290	0.431	0.012	0.023	0.036				
		(LL)	0.450	0.953	1.747	0.012	0.019	0.031				
	Y1 → CN+YB	(HL)	0.179	0.367	0.454	0.013	0.034	0.040				
		(LH)	0.329	0.534	1.109	0.021	0.047	0.071				
	Y1 → CN+ZB	(HL)	0.355	0.961	1.086	0.010	0.016	0.025				
		(LH)	0.400	0.805	1.344	0.012	0.023	0.037				
	Y1 → X	(HH)	0.448	0.815	1.355	0.013	0.024	0.038				
		(LL)	0.391	0.763	1.286	0.018	0.030	0.048				
	X2 → CN+ZB	(HL)	0.345	0.601	0.994	0.010	0.016	0.026				
		(LH)	0.436	0.718	1.533	0.012	0.023	0.037				
	X2 → X	(HH)	0.317	0.550	0.886	0.013	0.023	0.037				
		(LL)	0.299	0.581	1.033	0.018	0.029	0.047				
	X2 → Y	(HH)	0.189	0.302	0.447	0.012	0.023	0.037				
		(LL)	0.497	1.084	1.965	0.012	0.019	0.031				
	Y2 → CN+ZB	(HL)	0.334	1.003	1.037	0.010	0.016	0.026				
		(LH)	0.424	0.939	1.448	0.012	0.023	0.037				
	Y2 → X	(HH)	0.455	0.867	1.453	0.013	0.024	0.038				
		(LL)	0.433	0.850	1.427	0.019	0.030	0.048				
	X3 → X	(HH)	0.296	0.498	0.809	0.013	0.023	0.037				
		(LL)	0.366	0.585	1.343	0.018	0.029	0.047				
	X3 → Y	(HH)	0.190	0.304	0.451	0.012	0.023	0.037				
		(LL)	0.497	1.095	1.996	0.012	0.019	0.031				
	Y3 → X	(HH)	0.183	0.869	0.582	0.007	0.024	0.019				
		(LL)	0.622	0.889	2.046	0.019	0.030	0.049				
	CNB → CN+XB	(HH)	0.301	0.541	0.862	0.024	0.046	0.076				
		(LL)	0.260	0.449	0.729	0.018	0.029	0.046				
	CNB → CN+YB	(HH)	0.491	0.949	1.569	0.034	0.068	0.114				
		(LL)	0.329	0.574	0.964	0.019	0.034	0.058				
	CNB → CN+ZB	(HH)	0.656	1.260	2.126	0.012	0.023	0.037				
		(LL)	0.650	1.199	2.045	0.010	0.016	0.026				

FUNCTION BLOCK

Function	4-BIT FULL ADDER					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	F527	68					
x2							
x4							

Logic Diagram



Truth Table

A0	B0	A1	B1	A2	B2	A3	B3	*1	S0	S1	S2	S3	*2	X	Y
0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	1
1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	1
1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1
0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
0	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1
1	0	1	0	1	0	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1

(n=0,1,2,3) , *1:CinB , *2:CoutB

Sn=(An+Bn+CinB)

X=(A0¥B0)+(A1¥B1)+(A2¥B2)+(A3¥B3)

Y=1:(An+Bn)>=1111

Y=0:(An+Bn)<1111

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path			t_{LD0} (ns)			t_1					
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F527	A0 → S0		(HH)	0.510	1.059	1.568	0.013	0.023	0.037	A0	3.1	S0	22
			(HL)	0.564	1.089	1.883	0.011	0.017	0.027	B0	3.1	S1	22
			(LH)	0.612	1.179	1.970	0.012	0.023	0.037	A1	3.1	S2	22
			(LL)	0.591	1.144	2.055	0.011	0.017	0.027	B1	3.1	S3	22
	A0 → S1		(HH)	0.518	1.146	1.611	0.012	0.023	0.037	A2	3.1	COUTB	20
			(HL)	0.509	0.979	1.700	0.011	0.017	0.027	B2	3.0	X	12
			(LH)	0.621	1.163	1.995	0.013	0.023	0.037	A3	3.1	Y	19
			(LL)	0.612	1.212	2.146	0.011	0.017	0.027	B3	3.0		
	A0 → S2		(HH)	0.761	1.418	2.382	0.013	0.023	0.037	CINB	2.0		
			(HL)	0.760	1.449	2.521	0.010	0.016	0.025				
			(LH)	0.805	1.524	2.634	0.013	0.023	0.037				
			(LL)	0.794	1.546	2.773	0.010	0.016	0.026				
	A0 → S3		(HH)	0.787	1.468	2.477	0.012	0.023	0.037				
			(HL)	0.787	1.510	2.629	0.010	0.016	0.025				
			(LH)	0.861	1.626	2.795	0.013	0.023	0.037				
			(LL)	0.849	1.647	2.938	0.010	0.016	0.026				
	A0 → COUTB		(HL)	0.771	1.428	2.390	0.038	0.069	0.113				
			(LH)	0.824	1.568	2.718	0.027	0.046	0.073				
	A0 → X		(HH)	0.367	0.579	0.890	0.013	0.023	0.037				
			(LL)	0.298	0.539	0.901	0.023	0.043	0.074				
	A0 → Y		(HH)	0.706	1.314	2.179	0.013	0.023	0.037				
			(LL)	0.771	1.481	2.560	0.010	0.016	0.025				
	B0 → S0		(HH)	0.520	1.086	1.588	0.013	0.023	0.037				
			(HL)	0.574	1.096	1.901	0.011	0.017	0.027				
			(LH)	0.599	1.198	2.010	0.012	0.023	0.037				
			(LL)	0.578	1.160	2.094	0.011	0.017	0.027				
	B0 → S1		(HH)	0.528	1.173	1.629	0.013	0.023	0.037				
			(HL)	0.519	0.992	1.719	0.011	0.017	0.027				
			(LH)	0.609	1.171	2.036	0.013	0.023	0.037				
			(LL)	0.599	1.230	2.186	0.011	0.017	0.027				
	B0 → S2		(HH)	0.771	1.431	2.401	0.013	0.023	0.037				
			(HL)	0.770	1.463	2.541	0.010	0.016	0.025				
			(LH)	0.792	1.531	2.674	0.013	0.023	0.037				
			(LL)	0.782	1.554	2.816	0.010	0.016	0.026				
	B0 → S3		(HH)	0.797	1.481	2.494	0.012	0.023	0.037				
			(HL)	0.796	1.524	2.646	0.010	0.016	0.025				
			(LH)	0.848	1.634	2.835	0.013	0.023	0.037				
			(LL)	0.836	1.655	2.975	0.010	0.016	0.026				
	B0 → COUTB		(HL)	0.780	1.446	2.408	0.038	0.068	0.113				
			(LH)	0.812	1.576	2.758	0.027	0.046	0.073				
	B0 → X		(HH)	0.341	0.578	0.922	0.013	0.023	0.037				
			(LL)	0.325	0.589	0.976	0.023	0.043	0.074				
	B0 → Y		(HH)	0.716	1.326	2.201	0.013	0.023	0.037				
			(LL)	0.758	1.488	2.602	0.010	0.016	0.025				
	A1 → S1		(HH)	0.516	1.115	1.587	0.013	0.023	0.037				
			(HL)	0.569	1.138	1.901	0.011	0.017	0.027				
			(LH)	0.615	1.188	1.982	0.012	0.023	0.037				
			(LL)	0.594	1.154	2.063	0.011	0.017	0.027				
	A1 → S2		(HH)	0.622	1.154	1.945	0.013	0.023	0.037				
			(HL)	0.617	1.187	2.069	0.010	0.016	0.025				
			(LH)	0.681	1.282	2.192	0.013	0.023	0.037				
			(LL)	0.673	1.306	2.332	0.010	0.016	0.026				
	A1 → S3		(HH)	0.812	1.528	2.588	0.013	0.023	0.037				
			(HL)	0.812	1.570	2.740	0.010	0.016	0.025				
			(LH)	0.821	1.555	2.678	0.013	0.023	0.037				
			(LL)	0.813	1.578	2.820	0.010	0.016	0.026				

FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t LD0 (ns)			t 1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A1 → COUTB	(HL)	0.782	1.473	2.481	0.038	0.068	0.113				
		(LH)	0.826	1.556	2.676	0.027	0.046	0.073				
	A1 → X	(HH)	0.429	0.669	1.076	0.013	0.023	0.037				
		(LL)	0.334	0.598	1.025	0.023	0.042	0.074				
	A1 → Y	(HH)	0.719	1.354	2.269	0.013	0.023	0.037				
		(LL)	0.772	1.473	2.522	0.010	0.016	0.026				
	B1 → S1	(HH)	0.525	1.141	1.606	0.013	0.023	0.037				
		(HL)	0.579	1.151	1.918	0.011	0.017	0.027				
		(LH)	0.602	1.206	2.023	0.012	0.023	0.037				
		(LL)	0.580	1.170	2.103	0.011	0.017	0.027				
	B1 → S2	(HH)	0.632	1.166	1.963	0.013	0.023	0.037				
		(HL)	0.628	1.199	2.090	0.010	0.016	0.025				
		(LH)	0.668	1.290	2.234	0.013	0.023	0.037				
		(LL)	0.659	1.314	2.376	0.010	0.016	0.026				
	B1 → S3	(HH)	0.823	1.540	2.607	0.012	0.023	0.037				
		(HL)	0.823	1.582	2.759	0.010	0.016	0.025				
		(LH)	0.807	1.562	2.718	0.013	0.023	0.037				
		(LL)	0.799	1.586	2.859	0.010	0.016	0.026				
	B1 → COUTB	(HL)	0.795	1.483	2.497	0.038	0.069	0.113				
		(LH)	0.812	1.563	2.717	0.027	0.046	0.073				
	B1 → X	(HH)	0.401	0.666	1.107	0.013	0.023	0.037				
		(LL)	0.357	0.646	1.097	0.023	0.042	0.074				
	B1 → Y	(HH)	0.729	1.366	2.287	0.013	0.023	0.037				
		(LL)	0.759	1.482	2.562	0.010	0.016	0.026				
	A2 → S2	(HH)	0.491	1.108	1.494	0.013	0.023	0.037				
		(HL)	0.543	1.130	1.812	0.010	0.016	0.025				
		(LH)	0.592	1.144	1.914	0.012	0.023	0.037				
		(LL)	0.568	1.108	1.991	0.010	0.016	0.026				
	A2 → S3	(HH)	0.656	1.226	2.067	0.012	0.023	0.037				
		(HL)	0.655	1.268	2.219	0.010	0.016	0.025				
		(LH)	0.670	1.266	2.168	0.013	0.023	0.037				
		(LL)	0.663	1.291	2.309	0.010	0.016	0.026				
	A2 → COUTB	(HL)	0.695	1.291	2.172	0.038	0.068	0.113				
		(LH)	0.687	1.295	2.247	0.027	0.046	0.073				
	A2 → X	(HH)	0.450	0.708	1.144	0.013	0.023	0.037				
		(LL)	0.336	0.628	1.087	0.023	0.042	0.074				
	A2 → Y	(HH)	0.629	1.172	1.961	0.013	0.023	0.037				
		(LL)	0.634	1.210	2.094	0.010	0.016	0.025				
	B2 → S2	(HH)	0.500	1.124	1.511	0.013	0.023	0.037				
		(HL)	0.553	1.131	1.830	0.010	0.016	0.025				
		(LH)	0.580	1.165	1.952	0.012	0.023	0.037				
		(LL)	0.555	1.127	2.032	0.010	0.016	0.026				
	B2 → S3	(HH)	0.666	1.237	2.087	0.012	0.023	0.037				
		(HL)	0.666	1.279	2.237	0.010	0.016	0.025				
		(LH)	0.657	1.274	2.207	0.013	0.023	0.037				
		(LL)	0.650	1.300	2.350	0.010	0.016	0.026				
	B2 → COUTB	(HL)	0.705	1.302	2.190	0.038	0.068	0.113				
		(LH)	0.674	1.303	2.288	0.027	0.046	0.073				
	B2 → X	(HH)	0.407	0.689	1.152	0.013	0.023	0.037				
		(LL)	0.355	0.662	1.143	0.023	0.042	0.074				
	B2 → Y	(HH)	0.639	1.184	1.980	0.013	0.023	0.037				
		(LL)	0.622	1.218	2.132	0.010	0.016	0.025				
	A3 → S3	(HH)	0.477	1.042	1.442	0.013	0.023	0.037				
		(HL)	0.529	1.061	1.764	0.010	0.016	0.025				
		(LH)	0.581	1.122	1.874	0.012	0.023	0.037				
		(LL)	0.555	1.084	1.951	0.010	0.016	0.026				

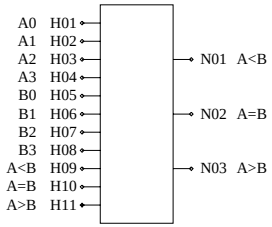
FUNCTION BLOCK

Block type	Switching speed							Input		Output	
	Path		t LD0 (ns)			t 1					
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	A3 → COUTB	(HL)	0.577	1.065	1.785	0.038	0.069	0.113				
		(LH)	0.565	1.061	1.825	0.027	0.046	0.074				
	A3 → X	(HH)	0.414	0.664	1.048	0.013	0.023	0.037				
		(LL)	0.313	0.575	0.993	0.023	0.042	0.074				
	A3 → Y	(HH)	0.512	0.948	1.572	0.013	0.023	0.037				
		(LL)	0.512	0.977	1.668	0.010	0.016	0.026				
	B3 → S3	(HH)	0.486	1.058	1.461	0.013	0.023	0.037				
		(HL)	0.540	1.061	1.785	0.010	0.016	0.025				
		(LH)	0.567	1.143	1.913	0.012	0.023	0.037				
		(LL)	0.541	1.103	1.994	0.010	0.016	0.026				
	B3 → COUTB	(HL)	0.588	1.077	1.804	0.038	0.069	0.113				
		(LH)	0.552	1.069	1.865	0.027	0.046	0.074				
	B3 → X	(HH)	0.370	0.641	1.055	0.013	0.023	0.037				
		(LL)	0.328	0.609	1.048	0.023	0.042	0.074				
	B3 → Y	(HH)	0.522	0.961	1.590	0.013	0.023	0.037				
		(LL)	0.498	0.985	1.708	0.010	0.016	0.026				
	CINB → S0	(HH)	0.398	0.738	1.220	0.013	0.023	0.037				
		(HL)	0.397	0.784	1.383	0.011	0.017	0.027				
		(LH)	0.399	0.718	1.165	0.013	0.023	0.037				
		(LL)	0.385	0.724	1.239	0.011	0.017	0.027				
	CINB → S1	(HH)	0.565	1.061	1.800	0.013	0.023	0.037				
		(HL)	0.554	1.083	1.948	0.011	0.017	0.027				
		(LH)	0.588	1.078	1.805	0.013	0.023	0.037				
		(LL)	0.578	1.096	1.894	0.011	0.017	0.027				
	CINB → S2	(HH)	0.666	1.260	2.125	0.013	0.023	0.037				
		(HL)	0.654	1.283	2.264	0.010	0.016	0.026				
		(LH)	0.666	1.217	2.046	0.013	0.023	0.037				
		(LL)	0.661	1.250	2.175	0.010	0.016	0.025				
	CINB → S3	(HH)	0.768	1.468	2.496	0.013	0.023	0.037				
		(HL)	0.759	1.490	2.639	0.010	0.016	0.026				
		(LH)	0.788	1.457	2.447	0.012	0.023	0.037				
		(LL)	0.787	1.500	2.596	0.010	0.016	0.025				
	CINB → COUTB	(HH)	0.658	1.247	2.114	0.013	0.024	0.038				
		(LL)	0.463	0.843	1.410	0.017	0.028	0.046				

FUNCTION BLOCK

Function	4-BIT MAGNITUDE COMPARATOR							SSI Family					
Block type	Positive output type						Negative output type						
	Normal		with ENB		with EN		Normal		with ENB		with EN		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power													
x1	F985	32											
x2													
x4													

Logic Diagram for "Positive output type"



Logic Diagram for "Positive output with ENB"

Logic Diagram for "Positive output with EN"

Logic Diagram for "Negative output type"

Logic Diagram for "Negative output with ENB"

Logic Diagram for "Negative output with EN"

Truth Table

A3,B3	A2,B2	A1,B1	A0,B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	X	0	0	1
A3<B3	X	X	X	X	X	X	1	0	0
A3=B3	A2>B2	X	X	X	X	X	0	0	1
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3=B3	A2=B2	A1>B1	X	X	X	X	0	0	1
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	0	0	1
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	X	1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	0	1	0	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	0	0	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	0	1	0	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F985	A0 → A<B	(HL)	0.861	1.674	2.888	0.010	0.016	0.026	A0	1.0	A<B	22
		(LH)	0.805	1.521	2.590	0.012	0.023	0.036	A1	1.0	A=B	22
	A0 → A=B	(HH)	0.765	1.498	2.560	0.012	0.023	0.037	A2	1.0	A>B	21
		(HL)	0.721	1.395	2.435	0.009	0.015	0.024	A3	1.0		
		(LH)	0.933	1.784	3.059	0.012	0.023	0.036	B0	2.1		
		(LL)	0.626	1.144	1.932	0.009	0.015	0.024	B1	2.1		
	A0 → A>B	(HH)	0.739	1.440	2.482	0.012	0.023	0.036	B2	2.1		
		(LL)	0.604	1.119	1.917	0.012	0.022	0.038	B3	2.1		
	A1 → A<B	(HL)	0.927	1.850	3.201	0.010	0.016	0.026	A<B	1.0		
		(LH)	0.873	2.270	3.950	0.012	0.023	0.036	A=B	3.1		
	A1 → A=B	(HH)	0.850	1.671	2.873	0.012	0.023	0.037	A>B	1.0		
		(HL)	0.800	1.548	2.692	0.009	0.015	0.024				
		(LH)	1.026	1.968	3.397	0.012	0.023	0.037				
		(LL)	0.697	1.274	2.151	0.009	0.015	0.024				
	A1 → A>B	(HH)	0.839	1.618	2.801	0.012	0.023	0.036				
		(LL)	0.994	1.963	3.431	0.012	0.022	0.038				
	A2 → A<B	(HL)	0.880	2.011	3.514	0.010	0.016	0.026				
		(LH)	0.947	2.374	4.107	0.012	0.023	0.036				
	A2 → A=B	(HH)	0.917	1.829	3.180	0.012	0.023	0.037				
		(HL)	0.847	1.638	2.838	0.009	0.015	0.024				
		(LH)	1.082	2.110	3.676	0.012	0.023	0.037				
		(LL)	0.770	1.414	2.387	0.009	0.015	0.024				
	A2 → A>B	(HH)	0.792	1.788	3.094	0.012	0.023	0.036				
		(LL)	0.851	2.068	3.588	0.012	0.022	0.038				
	A3 → A<B	(HL)	0.760	2.146	3.720	0.010	0.016	0.026				
		(LH)	0.819	2.178	3.761	0.012	0.023	0.037				
	A3 → A=B	(HH)	0.962	1.927	3.370	0.012	0.023	0.037				
		(HL)	0.906	1.754	3.032	0.009	0.015	0.024				
		(LH)	1.127	2.204	3.879	0.012	0.023	0.036				
		(LL)	0.825	1.513	2.559	0.009	0.015	0.024				
	A3 → A>B	(HH)	0.670	1.965	3.389	0.012	0.023	0.036				
		(LL)	0.670	1.873	3.240	0.012	0.022	0.039				
	B0 → A<B	(HH)	0.700	1.344	2.298	0.012	0.023	0.036				
		(LL)	0.840	1.662	2.873	0.010	0.016	0.026				
	B0 → A=B	(HH)	0.762	1.464	2.493	0.012	0.023	0.036				
		(HL)	0.521	0.967	1.641	0.009	0.015	0.024				
		(LH)	0.744	1.484	2.546	0.012	0.023	0.037				
		(LL)	0.650	1.232	2.159	0.009	0.015	0.024				
	B0 → A>B	(HL)	0.501	0.926	1.557	0.012	0.022	0.038				
		(LH)	0.668	1.277	2.204	0.012	0.023	0.036				
	B1 → A<B	(HH)	0.767	2.073	3.586	0.012	0.023	0.036				
		(LL)	0.822	1.834	3.187	0.010	0.016	0.026				
	B1 → A=B	(HH)	0.853	1.645	2.818	0.012	0.023	0.037				
		(HL)	0.588	1.091	1.853	0.009	0.015	0.024				
		(LH)	0.825	1.653	2.860	0.012	0.023	0.037				
		(LL)	0.727	1.382	2.420	0.009	0.015	0.024				
	B1 → A>B	(HL)	0.889	1.768	3.066	0.012	0.022	0.038				
		(LH)	0.767	1.451	2.525	0.012	0.022	0.036				
	B2 → A<B	(HH)	0.839	2.219	3.831	0.012	0.023	0.036				
		(LL)	0.778	1.989	3.502	0.010	0.016	0.026				
	B2 → A=B	(HH)	0.916	1.800	3.114	0.012	0.023	0.037				
		(HL)	0.663	1.232	2.087	0.009	0.015	0.024				
		(LH)	0.890	1.810	3.174	0.012	0.023	0.037				
		(LL)	0.776	1.472	2.561	0.009	0.015	0.024				
	B2 → A>B	(HL)	0.726	1.914	3.306	0.012	0.022	0.038				
		(LH)	0.689	1.775	3.086	0.012	0.023	0.036				

FUNCTION BLOCK

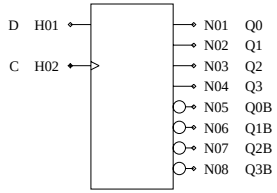
Block type	Switching speed										
	Path		t_{LD0} (ns)			t_1			Input		Output	
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	B3 → A<B	(HH)	0.686	2.028	3.478	0.012	0.023	0.036				
		(LL)	0.659	2.145	3.732	0.010	0.016	0.026				
	B3 → A=B	(HH)	0.963	1.897	3.313	0.012	0.023	0.036				
		(HL)	0.717	1.325	2.252	0.009	0.015	0.024				
		(LH)	0.935	1.904	3.359	0.012	0.023	0.037				
		(LL)	0.834	1.586	2.759	0.009	0.015	0.024				
	B3 → A>B	(HL)	0.536	1.723	2.959	0.012	0.022	0.038				
		(LH)	0.569	1.963	3.401	0.012	0.023	0.036				
	A<B → A>B	(HL)	0.277	0.501	0.819	0.012	0.022	0.039				
		(LH)	0.331	0.650	1.156	0.012	0.023	0.036				
	A=B → A<B	(HL)	0.450	0.832	1.383	0.010	0.016	0.026				
		(LH)	0.461	0.851	1.475	0.012	0.023	0.036				
	A=B → A=B	(HH)	0.179	0.314	0.511	0.012	0.023	0.037				
		(LL)	0.194	0.333	0.547	0.009	0.015	0.024				
	A=B → A>B	(HL)	0.266	0.488	0.804	0.012	0.022	0.038				
		(LH)	0.346	0.644	1.120	0.012	0.023	0.036				
	A>B → A<B	(HL)	0.460	0.846	1.402	0.010	0.016	0.026				
		(LH)	0.447	0.858	1.512	0.012	0.023	0.037				

[MEMO]

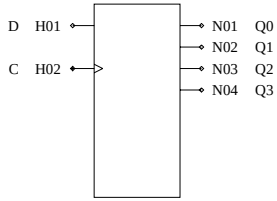
FUNCTION BLOCK

Function	4-BIT SERIAL/PARALLEL SHIFT REGISTER						SSI Family					
Block type	Standard type						Low Gate type					
	Normal		Q output		QB output		Normal		Q output		QB output	
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells
Low Power			L914	18								
x1	F914	28										
x2												
x4												

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

D	C	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
0	↗	0		SHIFT		1		SHIFT	
1	↗	1		SHIFT		0		SHIFT	
X	↘	HOLD							

X:Irrelevant

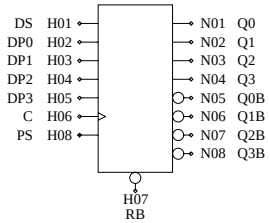
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F914	C → Q0		(HH)	0.435	0.753	1.251	0.012	0.023	0.037	D	1.0	Q0	22
			(HL)	0.561	1.006	1.688	0.009	0.015	0.025	C	2.0	Q1	22
	C → Q1		(HH)	0.434	0.750	1.246	0.012	0.023	0.036			Q2	23
			(HL)	0.558	0.999	1.675	0.009	0.015	0.025			Q3	22
	C → Q2		(HH)	0.434	0.750	1.246	0.012	0.023	0.037			Q0B	22
			(HL)	0.557	1.001	1.680	0.009	0.015	0.025			Q1B	22
	C → Q3		(HH)	0.438	0.756	1.255	0.012	0.023	0.036			Q2B	22
			(HL)	0.556	0.998	1.674	0.009	0.015	0.025			Q3B	22
	C → Q0B		(HH)	0.690	1.237	2.077	0.012	0.023	0.036				
			(HL)	0.591	1.061	1.804	0.010	0.015	0.025				
	C → Q1B		(HH)	0.685	1.231	2.068	0.012	0.023	0.036				
			(HL)	0.583	1.055	1.800	0.010	0.015	0.025				
	C → Q2B		(HH)	0.679	1.222	2.058	0.012	0.023	0.036				
			(HL)	0.590	1.058	1.798	0.010	0.015	0.025				
	C → Q3B		(HH)	0.656	1.182	1.987	0.012	0.023	0.036				
			(HL)	0.553	0.994	1.688	0.009	0.015	0.024				
	Set up time	D		0.410		0.917							
	Hold time	D		0.404		0.389							
	Min Pulse	C		1.565		3.123							
L914	C → Q0		(HH)	0.463	0.811	1.328	0.025	0.045	0.072	D	3.1	Q0	9
			(HL)	0.377	0.647	1.076	0.016	0.026	0.044	C	2.0	Q1	9
	C → Q1		(HH)	0.469	0.822	1.345	0.025	0.045	0.072			Q2	9
			(HL)	0.380	0.653	1.086	0.016	0.026	0.044			Q3	10
	C → Q2		(HH)	0.463	0.811	1.328	0.025	0.045	0.072				
			(HL)	0.376	0.647	1.075	0.016	0.026	0.044				
	C → Q3		(HH)	0.444	0.776	1.272	0.025	0.045	0.072				
			(HL)	0.358	0.616	1.022	0.017	0.028	0.046				
	Set up time	D		0.357		0.683							
	Hold time	D		0.540		0.620							
	Min Pulse	C		1.377		2.584							

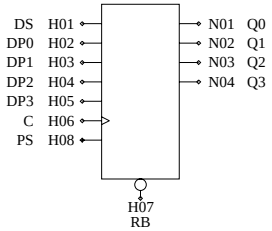
FUNCTION BLOCK

Function	4-BIT SERIAL/PARALLEL SHIFT REGISTER WITH RB						SSI Family						
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power			L913	27									
x1	F913	39											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

DS	DP0	DP1	DP2	DP3	C	RB	PS	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
0	X	X	X	X	↗	1	0	0		SHIFT		1		SHIFT	
1	X	X	X	X	↗	1	0	1		SHIFT		0		SHIFT	
X	DO	D1	D2	D3	↗	1	1	D0	D1	D2	D3	D0B	D1B	D2B	D3B
X	X	X	X	X	↘	1	X	HOLD							
X	X	X	X	X	X	0	X	0	0	0	0	1	1	1	1

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
F913	C → Q0	(HH)	0.486	0.878	1.461	0.012	0.023	0.037		DS	1.0	Q0	22
		(HL)	0.583	1.062	1.785	0.009	0.015	0.025		DP0	1.0	Q1	22
	C → Q1	(HH)	0.485	0.875	1.457	0.012	0.023	0.037		DP1	1.0	Q2	22
		(HL)	0.582	1.061	1.782	0.009	0.015	0.025		DP2	1.0	Q3	22
	C → Q2	(HH)	0.485	0.875	1.456	0.012	0.023	0.037		DP3	1.0	Q0B	22
		(HL)	0.582	1.060	1.782	0.009	0.015	0.025		C	2.0	Q1B	22
	C → Q3	(HH)	0.487	0.878	1.463	0.012	0.023	0.037		RB	10.7	Q2B	22
		(HL)	0.583	1.063	1.786	0.009	0.015	0.025		PS	1.0	Q3B	22
	C → Q0B	(HH)	0.707	1.287	2.169	0.012	0.023	0.036					
		(HL)	0.650	1.205	2.044	0.009	0.015	0.025					
	C → Q1B	(HH)	0.710	1.294	2.179	0.012	0.023	0.036					
		(HL)	0.656	1.215	2.063	0.009	0.015	0.025					
	C → Q2B	(HH)	0.706	1.285	2.166	0.012	0.023	0.036					
		(HL)	0.649	1.202	2.039	0.009	0.015	0.025					
	C → Q3B	(HH)	0.685	1.250	2.103	0.012	0.023	0.036					
		(HL)	0.621	1.145	1.942	0.009	0.015	0.024					
	RB → Q0	(LL)	0.218	0.386	0.641	0.009	0.015	0.025					
	RB → Q1	(LL)	0.218	0.385	0.641	0.009	0.015	0.025					
	RB → Q2	(LL)	0.218	0.385	0.641	0.009	0.015	0.025					
	RB → Q3	(LL)	0.218	0.386	0.642	0.009	0.015	0.025					
	RB → Q0B	(LH)	0.355	0.691	1.144	0.012	0.023	0.037					
	RB → Q1B	(LH)	0.360	0.699	1.158	0.012	0.023	0.037					
	RB → Q2B	(LH)	0.355	0.691	1.144	0.012	0.023	0.037					
	RB → Q3B	(LH)	0.332	0.655	1.083	0.012	0.023	0.037					
	Set up time	DS	1.515		2.218								
	Set up time	DP0	1.506		2.140								
	Set up time	DP1	1.506		2.141								
	Set up time	DP2	1.506		2.141								
	Set up time	DP3	1.506		2.140								
	Set up time	PS	1.984		3.059								
	Hold time	DS	0.286		0.121								
	Hold time	DP0	0.285		0.100								
	Hold time	DP1	0.285		0.102								
	Hold time	DP2	0.285		0.102								
	Hold time	DP3	0.285		0.100								
	Hold time	PS	0.019		0.010								
	Release time	RB	0.893		0.983								
	Removal time	RB	0.898		1.113								
	Min Pulse	C	1.475		2.953								
	Min Pulse	RB	1.146		2.435								
L913	C → Q0	(HH)	0.507	0.994	1.622	0.024	0.045	0.073		DS	5.1	Q0	8
		(HL)	0.396	0.720	1.180	0.017	0.028	0.046		DP0	5.2	Q1	8
	C → Q1	(HH)	0.512	0.997	1.626	0.024	0.045	0.073		DP1	5.1	Q2	8
		(HL)	0.398	0.723	1.186	0.017	0.028	0.045		DP2	4.8	Q3	10
	C → Q2	(HH)	0.505	0.982	1.604	0.024	0.045	0.073		DP3	4.8		
		(HL)	0.391	0.707	1.160	0.016	0.026	0.044		C	2.0		
	C → Q3	(HH)	0.481	0.866	1.422	0.025	0.045	0.072		RB	10.0		
		(HL)	0.365	0.648	1.065	0.016	0.026	0.044		PS	1.0		
	RB → Q0	(LL)	0.310	0.710	1.210	0.017	0.028	0.046					
	RB → Q1	(LL)	0.314	0.712	1.215	0.017	0.028	0.046					
	RB → Q2	(LL)	0.303	0.691	1.185	0.016	0.027	0.045					
	RB → Q3	(LL)	0.288	0.599	1.052	0.017	0.027	0.044					
	Set up time	DS	1.260		1.806								
	Set up time	DP0	1.266		1.801								
	Set up time	DP1	1.260		1.796								
	Set up time	DP2	1.252		1.788								

FUNCTION BLOCK

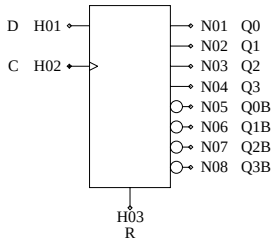
Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
	Set up time	DP3	1.252		1.788							
	Set up time	PS	1.961		3.134							
	Hold time	DS	0.455		0.440							
	Hold time	DP0	0.437		0.475							
	Hold time	DP1	0.445		0.443							
	Hold time	DP2	0.449		0.442							
	Hold time	DP3	0.449		0.442							
	Hold time	PS	0.113		0.010							
	Release time	RB	1.097		1.348							
	Removal time	RB	0.708		0.791							
	Min Pulse	C	1.365		2.717							
	Min Pulse	RB	1.241		2.814							

[MEMO]

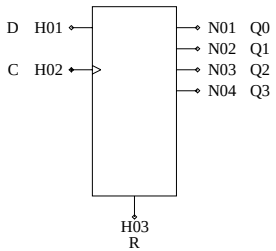
FUNCTION BLOCK

Function	4-BIT SHIFT REGISTER WITH R							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power			L911	23									
x1	F911	33											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

D	G	R	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
0	↗	0	0		SHIFT		1		SHIFT	
1	↗	0	1		SHIFT		0		SHIFT	
X	↘	0				Hold				
X	X	1	0	0	0	0	1	1	1	1

X:Irrelevant

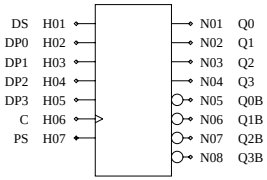
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F911	C → Q0	(HH)	0.472	0.837	1.401	0.012	0.023	0.037	D	1.0	Q0	22
		(HL)	0.562	1.012	1.699	0.009	0.015	0.024	C	2.0	Q1	22
	C → Q1	(HH)	0.475	0.843	1.409	0.013	0.023	0.037	R	2.0	Q2	22
		(HL)	0.561	1.010	1.696	0.009	0.015	0.024			Q3	22
	C → Q2	(HH)	0.472	0.837	1.401	0.012	0.023	0.037			Q0B	22
		(HL)	0.562	1.012	1.699	0.009	0.015	0.024			Q1B	22
	C → Q3	(HH)	0.475	0.844	1.410	0.013	0.023	0.037			Q2B	22
		(HL)	0.560	1.010	1.697	0.009	0.015	0.024			Q3B	22
	C → Q0B	(HH)	0.685	1.235	2.079	0.012	0.023	0.036				
		(HL)	0.635	1.163	1.982	0.009	0.015	0.025				
	C → Q1B	(HH)	0.696	1.250	2.100	0.012	0.023	0.036				
		(HL)	0.644	1.178	2.009	0.010	0.015	0.025				
	C → Q2B	(HH)	0.685	1.235	2.079	0.012	0.023	0.036				
		(HL)	0.635	1.163	1.982	0.009	0.015	0.025				
	C → Q3B	(HH)	0.667	1.201	2.017	0.012	0.023	0.036				
		(HL)	0.606	1.105	1.880	0.009	0.015	0.024				
	R → Q0	(HL)	0.387	0.665	1.085	0.009	0.015	0.025				
	R → Q1	(HL)	0.387	0.666	1.087	0.009	0.015	0.025				
	R → Q2	(HL)	0.387	0.665	1.085	0.009	0.015	0.025				
	R → Q3	(HL)	0.387	0.666	1.088	0.009	0.015	0.025				
	R → Q0B	(HH)	0.512	0.966	1.584	0.012	0.023	0.036				
	R → Q1B	(HH)	0.542	0.988	1.614	0.012	0.023	0.037				
	R → Q2B	(HH)	0.512	0.966	1.584	0.012	0.023	0.036				
	R → Q3B	(HH)	0.510	0.941	1.536	0.012	0.023	0.037				
	Set up time	D	0.430		0.907							
	Hold time	D	0.410		0.335							
	Release time	R	1.201		1.544							
	Removal time	R	0.623		0.637							
	Min Pulse	C	1.566		3.094							
	Min Pulse	R	1.497		3.086							
L911	C → Q0	(HH)	0.520	0.912	1.486	0.025	0.045	0.072	D	3.0	Q0	9
		(HL)	0.401	0.680	1.124	0.016	0.026	0.044	C	2.0	Q1	8
	C → Q1	(HH)	0.528	0.927	1.509	0.025	0.045	0.072	R	2.0	Q2	9
		(HL)	0.410	0.694	1.146	0.017	0.027	0.045			Q3	10
	C → Q2	(HH)	0.523	0.917	1.494	0.025	0.045	0.072				
		(HL)	0.406	0.688	1.136	0.017	0.028	0.045				
	C → Q3	(HH)	0.498	0.871	1.421	0.024	0.045	0.072				
		(HL)	0.378	0.644	1.064	0.016	0.027	0.044				
	R → Q0	(HL)	0.503	0.898	1.526	0.017	0.027	0.044				
	R → Q1	(HL)	0.516	0.921	1.558	0.017	0.028	0.046				
	R → Q2	(HL)	0.512	0.914	1.546	0.017	0.028	0.046				
	R → Q3	(HL)	0.448	0.864	1.470	0.017	0.027	0.044				
	Set up time	D	0.353		0.654							
	Hold time	D	0.556		0.636							
	Release time	R	1.378		1.803							
	Removal time	R	0.483		0.429							
	Min Pulse	C	1.476		2.774							
	Min Pulse	R	1.591		3.339							

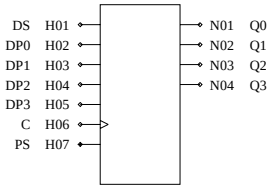
FUNCTION BLOCK

Function	4-BIT SHIFT REGISTER WITH LOAD							SSI Family					
Block type	Standard type						Low Gate type						
	Normal		Q output		QB output		Normal		Q output		QB output		
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	
Low Power			L912	23									
x1	F912	35											
x2													
x4													

Logic Diagram for "Normal"



Logic Diagram for "Q output"



Logic Diagram for "QB output"

Truth Table

DS	DP0	DP1	DP2	DP3	C	PS	Q0	Q1	Q2	Q3	Q0B	Q1B	Q2B	Q3B
0	X	X	X	X	↗	0	0		SHIFT		1		SHIFT	
1	X	X	X	X	↗	0	1		SHIFT		0		SHIFT	
X	DO	D1	D2	D3	↗	1	D0	D1	D2	D3	D0B	D1B	D2B	D3B
X	X	X	X	X	↘	X	HOLD							

X:Irrelevant

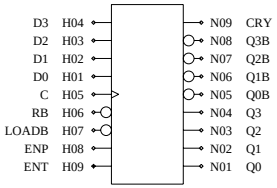
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F912	C → Q0	(HH)	0.438	0.770	1.273	0.012	0.023	0.036	DS	1.0	Q0	22
		(HL)	0.567	1.027	1.730	0.009	0.015	0.025	DP0	1.0	Q1	23
	C → Q1	(HH)	0.439	0.770	1.276	0.012	0.023	0.036	DP1	1.0	Q2	23
		(HL)	0.568	1.028	1.728	0.009	0.015	0.025	DP2	1.0	Q3	23
	C → Q2	(HH)	0.436	0.770	1.274	0.012	0.023	0.036	DP3	1.0	Q0B	22
		(HL)	0.557	1.014	1.714	0.009	0.015	0.024	C	2.0	Q1B	22
	C → Q3	(HH)	0.437	0.770	1.277	0.012	0.023	0.036	PS	1.0	Q2B	22
		(HL)	0.557	1.014	1.711	0.009	0.015	0.024			Q3B	22
	C → Q0B	(HH)	0.689	1.251	2.109	0.012	0.023	0.036				
		(HL)	0.581	1.065	1.809	0.009	0.015	0.025				
	C → Q1B	(HH)	0.695	1.260	2.122	0.012	0.023	0.036				
		(HL)	0.588	1.077	1.833	0.009	0.015	0.025				
	C → Q2B	(HH)	0.675	1.232	2.088	0.012	0.023	0.036				
		(HL)	0.582	1.069	1.818	0.009	0.015	0.025				
	C → Q3B	(HH)	0.651	1.191	2.016	0.012	0.023	0.036				
		(HL)	0.553	1.009	1.712	0.009	0.015	0.024				
	Set up time	DS	1.489		2.211							
	Set up time	DP0	1.518		2.114							
	Set up time	DP1	1.517		2.114							
	Set up time	DP2	1.513		2.106							
	Set up time	DP3	1.513		2.106							
	Set up time	PS	1.944		2.983							
	Hold time	DS	0.281		0.136							
	Hold time	DP0	0.234		0.207							
	Hold time	DP1	0.234		0.208							
	Hold time	DP2	0.240		0.242							
	Hold time	DP3	0.240		0.242							
	Hold time	PS	0.031		0.010							
	Min Pulse	C	1.441		2.992							
L912	C → Q0	(HH)	0.469	0.914	1.492	0.025	0.045	0.073	DS	5.1	Q0	8
		(HL)	0.384	0.698	1.146	0.016	0.027	0.044	DP0	5.2	Q1	8
	C → Q1	(HH)	0.481	0.936	1.523	0.025	0.045	0.073	DP1	5.1	Q2	8
		(HL)	0.392	0.712	1.165	0.017	0.028	0.046	DP2	5.1	Q3	10
	C → Q2	(HH)	0.474	0.922	1.503	0.025	0.045	0.073	DP3	5.1		
		(HL)	0.387	0.703	1.151	0.017	0.028	0.046	C	2.0		
	C → Q3	(HH)	0.446	0.795	1.307	0.025	0.045	0.072	PS	1.0		
		(HL)	0.359	0.636	1.046	0.017	0.027	0.044				
	Set up time	DS	1.212		1.644							
	Set up time	DP0	1.230		1.615							
	Set up time	DP1	1.238		1.662							
	Set up time	DP2	1.238		1.662							
	Set up time	DP3	1.228		1.600							
	Set up time	PS	1.833		2.910							
	Hold time	DS	0.498		0.489							
	Hold time	DP0	0.493		0.409							
	Hold time	DP1	0.490		0.399							
	Hold time	DP2	0.490		0.399							
	Hold time	DP3	0.499		0.420							
	Hold time	PS	0.144		0.010							
	Min Pulse	C	1.354		2.616							

FUNCTION BLOCK

Function	4-BIT SYNCHRONOUS BINARY COUNTER WITH RB							SSI Family						
Block type	Standard type						Low Gate type							
	Normal		Q output		QB output		Normal		Q output		QB output			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power														
x1	F961	54												
x2														
x4														

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

Dn	C	RB	LOADB	ENP	ENT	Qn	QnB
X	↗	1	1	1	1	INCREMENT COUNT	
X	↘	1	1	1	1	HOLD	
X	X	1	1	0	X	HOLD	
X	X	1	1	X	0	HOLD	
Dn	↗	1	0	X	X	Dn	DnB
X	↘	1	0	X	X	HOLD	
X	X	0	X	X	X	0	1

N09 is '1' only at H09=Qn=1

X:Irrelevant

n = 0,1,2,3

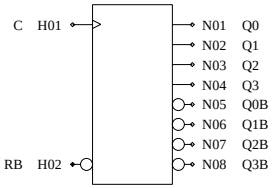
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F961	C → Q0	(HH)	1.013	1.919	3.271	0.012	0.023	0.037	D0	5.2	Q0	22
		(HL)	0.781	1.393	2.357	0.010	0.016	0.026	D1	5.2	Q1	22
	C → Q1	(HH)	0.989	1.868	3.177	0.012	0.023	0.037	D2	5.2	Q2	22
		(HL)	0.765	1.363	2.304	0.010	0.016	0.026	D3	5.2	Q3	22
	C → Q2	(HH)	0.961	1.811	3.074	0.012	0.023	0.037	C	2.1	Q0B	22
		(HL)	0.747	1.332	2.248	0.010	0.016	0.026	RB	10.9	Q1B	22
	C → Q3	(HH)	0.933	1.752	2.966	0.012	0.023	0.037	LOADB	1.0	Q2B	22
		(HL)	0.730	1.300	2.191	0.010	0.016	0.026	ENP	1.0	Q3B	22
	C → Q0B	(HH)	0.598	1.026	1.698	0.013	0.023	0.037	ENT	2.3	CRY	10
		(HL)	0.803	1.504	2.556	0.010	0.017	0.028				
	C → Q1B	(HH)	0.582	0.999	1.650	0.013	0.023	0.037				
		(HL)	0.781	1.458	2.472	0.010	0.017	0.028				
	C → Q2B	(HH)	0.566	0.971	1.600	0.013	0.023	0.037				
		(HL)	0.756	1.407	2.380	0.010	0.017	0.027				
	C → Q3B	(HH)	0.549	0.941	1.548	0.013	0.023	0.037				
		(HL)	0.730	1.355	2.283	0.010	0.016	0.027				
	C → CRY	(HH)	1.073	2.005	3.382	0.025	0.046	0.073				
		(HL)	0.545	0.961	1.610	0.017	0.027	0.043				
	RB → Q0	(LL)	0.261	0.467	0.784	0.010	0.016	0.026				
	RB → Q1	(LL)	0.261	0.467	0.784	0.010	0.016	0.026				
	RB → Q2	(LL)	0.261	0.466	0.782	0.010	0.016	0.026				
	RB → Q3	(LL)	0.261	0.466	0.782	0.010	0.016	0.026				
	RB → Q0B	(LH)	0.558	1.002	1.718	0.013	0.023	0.037				
	RB → Q1B	(LH)	0.542	0.975	1.670	0.013	0.023	0.037				
	RB → Q2B	(LH)	0.526	0.947	1.621	0.013	0.023	0.037				
	RB → Q3B	(LH)	0.509	0.917	1.570	0.013	0.023	0.037				
	RB → CRY	(LL)	0.507	0.938	1.632	0.017	0.027	0.043				
	ENT → CRY	(HH)	0.381	0.736	1.223	0.025	0.046	0.073				
		(LL)	0.248	0.450	0.739	0.017	0.027	0.045				
	Set up time	D0	1.253		1.802							
	Set up time	D1	1.253		1.801							
	Set up time	D2	1.253		1.802							
	Set up time	D3	1.253		1.801							
	Set up time	LOADB	1.981		3.065							
	Set up time	ENP	2.570		4.721							
	Set up time	ENT	2.447		4.716							
	Hold time	D0	0.465		0.425							
	Hold time	D1	0.464		0.426							
	Hold time	D2	0.465		0.412							
	Hold time	D3	0.465		0.425							
	Hold time	LOADB	0.065		0.010							
	Hold time	ENP	0.293		1.075							
	Hold time	ENT	0.010		0.010							
	Release time	RB	1.071		1.326							
	Removal time	RB	0.726		0.802							
	Min Pulse	C	2.120		5.093							
	Min Pulse	RB	1.582		3.908							

FUNCTION BLOCK

Function	4-BIT SYNCHRONOUS BINARY UP COUNTER WITH RB							SSI Family						
Block type	Standard type						Low Gate type							
	Normal		Q output		QB output		Normal		Q output		QB output			
Drivability	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells	Name	cells		
Low Power														
x1	F962	39												
x2														
x4														

Logic Diagram for "Normal"



Logic Diagram for "Q output"

Logic Diagram for "QB output"

Truth Table

C	RB	Qn	QnB
↗	1	INCREMENT COUNT	
↘	1	HOLD	
X	0	0	1

X:Irrelevant

(n=0,1,2,3)

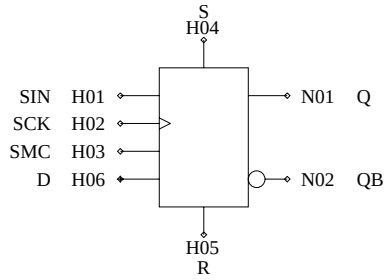
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
F962	C → Q0	(HH)	0.933	1.732	2.935	0.013	0.023	0.037	C	2.1	Q0	22
		(HL)	0.732	1.292	2.174	0.009	0.015	0.024	RB	10.3	Q1	22
	C → Q1	(HH)	0.897	1.653	2.807	0.012	0.023	0.037			Q2	22
		(HL)	0.773	1.370	2.304	0.009	0.015	0.025			Q3	22
	C → Q2	(HH)	0.853	1.566	2.655	0.012	0.023	0.037			Q0B	22
		(HL)	0.730	1.294	2.182	0.009	0.015	0.025			Q1B	22
	C → Q3	(HH)	0.804	1.470	2.487	0.012	0.023	0.036			Q2B	22
		(HL)	0.706	1.250	2.105	0.009	0.015	0.025			Q3B	23
	C → Q0B	(HH)	0.572	0.972	1.605	0.013	0.023	0.037				
		(HL)	0.749	1.367	2.309	0.010	0.016	0.027				
	C → Q1B	(HH)	0.556	0.945	1.565	0.013	0.023	0.037				
		(HL)	0.714	1.296	2.189	0.010	0.016	0.026				
	C → Q2B	(HH)	0.525	0.890	1.470	0.013	0.023	0.037				
		(HL)	0.673	1.210	2.041	0.010	0.016	0.026				
	C → Q3B	(HH)	0.505	0.851	1.401	0.013	0.023	0.037				
		(HL)	0.630	1.126	1.892	0.010	0.015	0.025				
	RB → Q0	(LL)	0.242	0.649	1.109	0.009	0.016	0.027				
	RB → Q1	(LL)	0.306	0.751	1.270	0.010	0.016	0.027				
	RB → Q2	(LL)	0.307	0.753	1.274	0.010	0.016	0.027				
	RB → Q3	(LL)	0.303	0.744	1.264	0.010	0.016	0.027				
	RB → Q0B	(LH)	0.517	1.161	2.038	0.012	0.023	0.037				
	RB → Q1B	(LH)	0.497	1.258	2.206	0.013	0.024	0.038				
	RB → Q2B	(LH)	0.474	1.186	2.092	0.013	0.024	0.038				
	RB → Q3B	(LH)	0.430	1.110	1.968	0.013	0.024	0.038				
	Release time	RB	1.078		1.318							
	Removal time	RB	0.759		0.858							
	Min Pulse	C	1.330		3.376							
	Min Pulse	RB	0.926		3.029							

FUNCTION BLOCK

Function	D-F/F WITH R,S,2 TO 1 SELECTOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S000	12					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	S	R	D	Q	QB	
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
A	↗	0	0	0	X	A	AB	
X	↗	1	0	0	B	B	BB	
X	↘	X	0	0	X	HOLD		
X	X	X	1	1	X	1	1	← Prohibition

X:Irrelevant

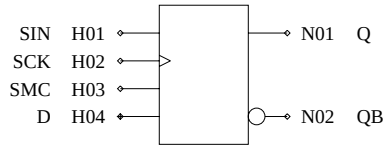
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S000	SCK → Q	(HH)	0.407	0.737	1.250	0.012	0.023	0.036	SIN	1.0	Q	23
		(HL)	0.559	1.075	1.851	0.011	0.017	0.028	SCK	1.0	QB	22
	SCK → QB	(HH)	0.655	1.263	2.188	0.012	0.022	0.036	SMC	1.0		
		(HL)	0.625	1.198	2.096	0.010	0.016	0.026	S	2.3		
	S → Q	(HH)	0.188	0.303	0.453	0.012	0.023	0.036	R	2.1		
	S → QB	(HL)	0.404	1.012	1.738	0.010	0.017	0.029	D	1.0		
	R → Q	(HL)	0.486	0.928	1.590	0.011	0.017	0.028				
	R → QB	(HH)	0.185	0.359	0.535	0.012	0.023	0.037				
	Set up time	SIN	0.849		2.118							
	Set up time	SMC	0.805		2.201							
	Set up time	D	0.805		2.201							
	Hold time	SIN	0.010		0.010							
	Hold time	SMC	0.010		0.010							
	Hold time	D	0.010		0.010							
	Release time	S	1.112		1.195							
	Release time	R	1.282		1.700							
	Removal time	S	0.617		0.704							
	Removal time	R	0.475		0.300							
	Min Pulse	SCK	1.115		2.618							
	Min Pulse	S	0.924		2.714							
	Min Pulse	R	1.045		2.590							

FUNCTION BLOCK

Function	D-F/F WITH 2 TO 1 SELECTOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S002	10					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	D	Q	QB
X	↗	1	B	B	BB
A	↗	0	X	A	AB
X	↘	X	X	HOLD	

X:Irrelevant

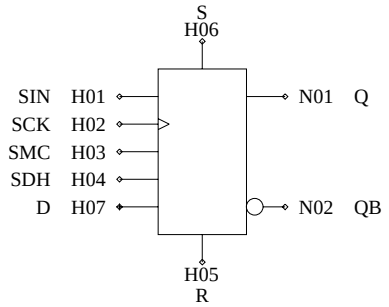
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S002	SCK → Q	(HH)	0.380	0.675	1.118	0.012	0.023	0.037	SIN	1.0	Q	22
		(HL)	0.428	0.802	1.354	0.009	0.015	0.025	SCK	1.0	QB	23
	SCK → QB	(HH)	0.520	0.974	1.648	0.012	0.022	0.036	SMC	1.0		
		(HL)	0.494	0.909	1.544	0.011	0.016	0.026	D	1.0		
	Set up time	SIN	0.607		1.328							
	Set up time	SMC	0.611		1.426							
	Set up time	D	0.611		1.426							
	Hold time	SIN	0.096		0.010							
	Hold time	SMC	0.061		0.010							
	Hold time	D	0.122		0.010							
	Min Pulse	SCK	1.055		2.211							

FUNCTION BLOCK

Function	D-F/F WITH R,S,HOLD,2 TO 1 SELECTOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S050	14					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	SDH	S	R	D	Q	QB	
X	↗	X	1	0	0	X	HOLD		
A	↗	0	0	0	0	X	A	AB	
X	↗	1	0	0	0	B	B	BB	
X	↘	X	X	0	0	X	HOLD		
X	X	X	X	0	1	X	0	1	
X	X	X	X	1	0	X	1	0	
X	X	X	X	1	1	X	1	1	← Prohibition

X:Irrelevant

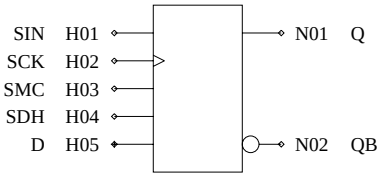
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t LD0 (ns)			t 1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
S050	SCK → Q	(HH)	0.414	0.751	1.277	0.012	0.023	0.036		SIN	3.1	Q	23
		(HL)	0.553	1.067	1.837	0.011	0.017	0.028		SCK	1.0	QB	22
	SCK → QB	(HH)	0.700	1.348	2.334	0.012	0.022	0.036		SMC	1.1		
		(HL)	0.727	1.416	2.500	0.010	0.017	0.028		SDH	1.0		
	R → Q	(HL)	0.472	0.999	1.709	0.011	0.017	0.028		R	2.1		
	R → QB	(HH)	0.229	0.421	0.642	0.012	0.023	0.037		S	2.2		
	S → Q	(HH)	0.187	0.301	0.452	0.012	0.023	0.036		D	3.1		
	S → QB	(HL)	0.498	1.215	2.118	0.010	0.018	0.031					
	Set up time	SIN	0.802		2.145								
	Set up time	SMC	0.818		2.126								
	Set up time	SDH	0.818		2.126								
	Set up time	D	0.818		2.126								
	Hold time	SIN	0.010		0.010								
	Hold time	SMC	0.010		0.010								
	Hold time	SDH	0.010		0.010								
	Hold time	D	0.010		0.010								
	Release time	R	1.232		1.659								
	Release time	S	1.084		1.198								
	Removal time	R	0.517		0.333								
	Removal time	S	0.640		0.702								
	Min Pulse	SCK	1.183		2.952								
	Min Pulse	R	0.991		2.710								
	Min Pulse	S	1.035		3.063								

FUNCTION BLOCK

Function	D-F/F WITH HOLD,2 TO 1 SELECTOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S052	13					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	SDH	D	Q	QB
X	↗	X	1	X	HOLD	
A	↗	0	0	X	A	AB
X	↗	1	0	B	B	BB
X	↘	X	X	X	HOLD	

X:Irrelevant

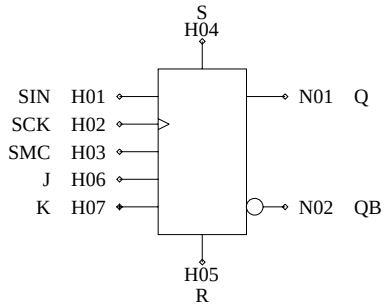
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path		t_{LD0} (ns)			t_1							
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		Symbol	Fanin	Symbol	Fanout
S052	SCK → Q	(HH)	0.385	0.680	1.125	0.012	0.023	0.037		SIN	3.1	Q	22
		(HL)	0.457	0.839	1.398	0.009	0.015	0.024		SCK	1.0	QB	22
	SCK → QB	(HH)	0.585	1.074	1.798	0.012	0.023	0.036		SMC	1.1		
		(HL)	0.547	1.008	1.715	0.011	0.017	0.027		SDH	1.0		
	Set up time	SIN	0.713		1.629					D	3.1		
	Set up time	SMC	0.713		1.629								
	Set up time	SDH	0.713		1.629								
	Set up time	D	0.713		1.629								
	Hold time	SIN	0.066		0.010								
	Hold time	SMC	0.010		0.010								
	Hold time	SDH	0.048		0.010								
	Hold time	D	0.068		0.010								
	Min Pulse	SCK	1.086		2.322								

FUNCTION BLOCK

Function	JK-F/F WITH R,S,D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S100	14					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	S	R	J	K	Qn	QBn	Qn+1	QBn+1	
X	X	X	1	0	X	X	X	X	1	0	
X	X	X	0	1	X	X	X	X	0	1	
A	↗	0	0	0	X	X	X	X	A	AB	
X	↗	1	0	0	B	X	0	1	B	BB	
X	↗	1	0	0	X	C	1	0	CB	C	
X	↘	X	0	0	X	X	X	X	HOLD		
X	X	X	1	1	X	X	X	X	1	1	← Prohibition

X:Irrelevant

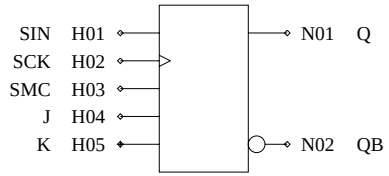
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S100	SCK → Q	(HH)	0.401	0.729	1.240	0.013	0.023	0.037	SIN	1.0	Q	22
		(HL)	0.552	1.068	1.842	0.010	0.016	0.026	SCK	1.0	QB	22
	SCK → QB	(HH)	0.716	1.376	2.381	0.012	0.023	0.036	SMC	1.0		
		(HL)	0.739	1.445	2.558	0.011	0.018	0.030	S	2.3		
	S → Q	(HH)	0.190	0.306	0.457	0.012	0.023	0.037	R	2.1		
	S → QB	(HL)	0.527	1.268	2.214	0.011	0.020	0.032	J	1.0		
	R → Q	(HL)	0.487	1.008	1.734	0.010	0.016	0.026	K	1.0		
	R → QB	(HH)	0.241	0.439	0.670	0.013	0.023	0.037				
	Set up time	SIN	1.680		2.520							
	Set up time	SMC	1.867		2.838							
	Set up time	J	2.002		3.375							
	Set up time	K	1.985		3.046							
	Hold time	SIN	0.010		0.010							
	Hold time	SMC	0.010		0.010							
	Hold time	J	0.010		0.010							
	Hold time	K	0.010		0.010							
	Release time	S	1.085		1.194							
	Release time	R	1.277		1.711							
	Removal time	S	0.640		0.704							
	Removal time	R	0.480		0.291							
	Min Pulse	SCK	1.245		2.997							
	Min Pulse	S	1.107		3.133							
	Min Pulse	R	1.044		2.730							

FUNCTION BLOCK

Function	JK-F/F WITH D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S102	12					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	J	K	Qn	QBn	Qn+1	QBn+1
A	↗	0	X	X	X	X	A	AB
X	↗	1	B	X	0	1	B	BB
X	↗	1	X	C	1	0	CB	C
X	↘	X	X	X	X	X	HOLD	

X:Irrelevant

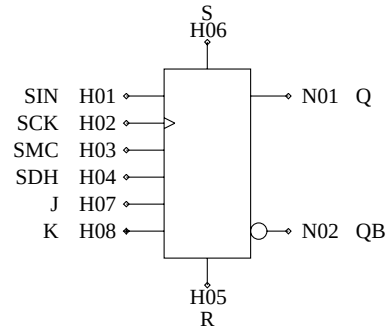
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S102	SCK → Q	(HH)	0.383	0.685	1.137	0.012	0.023	0.036	SIN	1.0	Q	23
		(HL)	0.456	0.842	1.409	0.009	0.015	0.024	SCK	1.0	QB	22
	SCK → QB	(HH)	0.613	1.124	1.887	0.012	0.022	0.036	SMC	1.0		
		(HL)	0.565	1.058	1.815	0.010	0.015	0.025	J	1.0		
	Set up time	SIN	1.583		2.286				K	1.0		
	Set up time	SMC	1.743		2.435							
	Set up time	J	1.821		3.117							
	Set up time	K	1.789		2.655							
	Hold time	SIN	0.124		0.010							
	Hold time	SMC	0.069		0.010							
	Hold time	J	0.047		0.010							
	Hold time	K	0.010		0.010							
	Min Pulse	SCK	1.190		2.465							

FUNCTION BLOCK

Function	JK-F/F WITH R,S,HOLD,D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S150	17					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	SDH	S	R	J	K	Qn	QBn	Qn+1	QBn+1	
X	↗	X	1	0	0	X	X	X	X	HOLD		
A	↗	0	0	0	0	X	X	X	X	A	AB	
X	↗	1	0	0	0	B	X	0	1	B	BB	
X	↗	1	0	0	0	X	C	1	0	CB	C	
X	↘	X	X	0	0	X	X	X	X	HOLD		
X	X	X	X	0	1	X	X	X	X	0	1	
X	X	X	X	1	0	X	X	X	X	1	0	
X	X	X	X	1	1	X	X	X	X	1	1	← Prohibition

X:Irrelevant

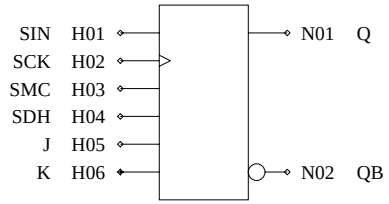
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S150	SCK → Q	(HH)	0.404	0.739	1.260	0.013	0.023	0.037	SIN	3.0	Q	22
		(HL)	0.551	1.065	1.838	0.010	0.016	0.027	SCK	1.0	QB	22
	SCK → QB	(HH)	0.754	1.444	2.496	0.012	0.023	0.036	SMC	1.0		
		(HL)	0.814	1.612	2.871	0.011	0.018	0.030	SDH	1.0		
	R → Q	(HL)	0.478	1.064	1.829	0.010	0.016	0.026	R	2.1		
	R → QB	(HH)	0.272	0.490	0.756	0.012	0.023	0.037	S	2.3		
	S → Q	(HH)	0.189	0.304	0.454	0.012	0.023	0.037	J	1.0		
	S → QB	(HL)	0.598	1.423	2.507	0.011	0.020	0.033	K	1.0		
	Set up time	SIN	1.740		2.568							
	Set up time	SMC	2.045		3.296							
	Set up time	SDH	1.793		2.681							
	Set up time	J	2.126		3.454							
	Set up time	K	2.199		3.517							
	Hold time	SIN	0.010		0.010							
	Hold time	SMC	0.010		0.010							
	Hold time	SDH	0.010		0.010							
	Hold time	J	0.010		0.010							
	Hold time	K	0.010		0.010							
	Release time	R	1.233		1.657							
	Release time	S	1.085		1.194							
	Removal time	R	0.517		0.332							
	Removal time	S	0.640		0.703							
	Min Pulse	SCK	1.312		3.297							
	Min Pulse	R	0.997		2.825							
	Min Pulse	S	1.173		3.416							

FUNCTION BLOCK

Function	JK-F/F WITH HOLD,D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S152	15					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	SDH	J	K	Qn	QBn	Qn+1	QBn+1
X	↗	X	1	X	X	X	X	HOLD	
A	↗	0	0	X	X	X	X	A	AB
X	↗	1	0	B	X	0	1	B	BB
X	↗	1	0	X	C	1	0	CB	C
X	↘	X	X	X	X	X	X	HOLD	

X:Irrelevant

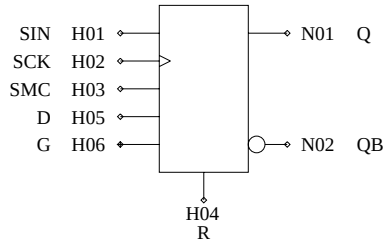
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S152	SCK → Q	(HH)	0.370	0.664	1.106	0.012	0.023	0.037	SIN	3.0	Q	22
		(HL)	0.433	0.803	1.348	0.009	0.015	0.024	SCK	1.0	QB	22
	SCK → QB	(HH)	0.603	1.112	1.872	0.012	0.023	0.036	SMC	1.0		
		(HL)	0.586	1.103	1.900	0.010	0.016	0.026	SDH	1.0		
	Set up time	SIN	1.633		2.320				J	1.0		
	Set up time	SMC	1.872		3.047				K	1.0		
	Set up time	SDH	1.666		2.449							
	Set up time	J	2.029		3.176							
	Set up time	K	1.972		3.136							
	Hold time	SIN	0.075		0.010							
	Hold time	SMC	0.010		0.010							
	Hold time	SDH	0.059		0.010							
	Hold time	J	0.010		0.010							
	Hold time	K	0.010		0.010							
	Min Pulse	SCK	1.125		2.399							

FUNCTION BLOCK

Function	D-LATCH WITH R,D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S201	12					
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	R	D	G	Q	QB	
X	X	X	1	X	X	0	1	
A	↗	0	0	X	X	A	AB	
X	↘	0	0	X	X	HOLD		
X	X	1	0	B	1	B	BB	
X	X	1	0	X	0	LATCH		
X	1	Down	0	1	1	X	X	← Prohibition

X:Irrelevant

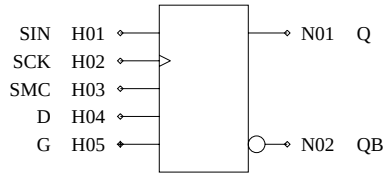
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path			t_{LD0} (ns)			t_1					
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S201	SCK → Q		(HH)	0.833	1.559	2.674	0.012	0.022	0.036	SIN	3.1	Q	22
			(HL)	0.660	1.212	2.083	0.009	0.015	0.024	SCK	1.0	QB	22
	SCK → QB		(HH)	0.529	0.954	1.623	0.012	0.023	0.037	SMC	1.0		
			(HL)	0.723	1.355	2.320	0.010	0.016	0.027	R	2.5		
	R → Q		(HL)	0.394	0.700	1.146	0.010	0.016	0.025	D	1.0		
	R → QB		(HH)	0.194	0.310	0.465	0.012	0.023	0.036	G	1.0		
	D → Q		(HH)	0.700	1.294	2.215	0.012	0.022	0.036				
			(LL)	0.589	1.138	2.099	0.009	0.015	0.024				
	D → QB		(HL)	0.589	1.091	1.862	0.010	0.016	0.027				
			(LH)	0.457	0.881	1.638	0.012	0.023	0.037				
	G → Q		(HH)	0.858	1.594	2.716	0.012	0.022	0.036				
			(HL)	0.674	1.233	2.114	0.009	0.015	0.024				
	G → QB		(HH)	0.543	0.976	1.656	0.012	0.023	0.037				
			(HL)	0.748	1.391	2.362	0.010	0.016	0.027				
	Set up time	SIN		1.194		1.480							
	Set up time	SMC		1.963		2.950							
	Set up time	D		1.736		2.532							
	Hold time	SIN		0.484		0.579							
	Hold time	SMC		0.030		0.010							
	Hold time	D		0.146		0.010							
	Release time	R		1.314		1.756							
	Removal time	R		0.801		1.043							
	Min Pulse	SCK		1.833		3.841							
	Min Pulse	R		1.400		2.892							
	Min Pulse	G		1.833		3.841							

FUNCTION BLOCK

Function	D-LATCH WITH D-F/F FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S202	11	S204	11			
x2							
x4							

Logic Diagram



Truth Table

SIN	SCK	SMC	D	G	Q	QB	
A	↗	0	X	X	A	AB	
X	↘	0	X	X	HOLD		
X	X	1	B	1	B	BB	
X	X	1	X	0	LATCH		
X	1	Down	1	1	X	X	← Prohibition

X:Irrelevant

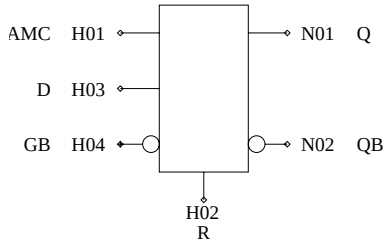
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S202	SCK → Q	(HH)	0.700	1.267	2.123	0.012	0.022	0.036	SIN	3.1	Q	22
		(HL)	0.626	1.153	1.992	0.009	0.015	0.024	SCK	1.0	QB	22
	SCK → QB	(HH)	0.509	0.914	1.556	0.012	0.023	0.036	SMC	1.0		
		(HL)	0.604	1.090	1.820	0.009	0.015	0.025	D	1.0		
	D → Q	(HH)	0.545	0.978	1.643	0.012	0.023	0.036	G	1.0		
		(LL)	0.556	1.088	2.028	0.009	0.015	0.024				
	D → QB	(HL)	0.450	0.801	1.340	0.009	0.015	0.025				
		(LH)	0.438	0.846	1.588	0.012	0.023	0.036				
	G → Q	(HH)	0.710	1.284	2.143	0.012	0.022	0.036				
		(HL)	0.643	1.182	2.034	0.009	0.015	0.024				
	G → QB	(HH)	0.527	0.943	1.597	0.012	0.023	0.036				
		(HL)	0.614	1.106	1.841	0.009	0.015	0.024				
	Set up time	SIN	1.166		1.335							
	Set up time	SMC	1.713		2.524							
	Set up time	D	1.531		2.248							
	Hold time	SIN	0.538		0.658							
	Hold time	SMC	0.051		0.010							
	Hold time	D	0.203		0.179							
	Min Pulse	SCK	1.731		3.447							
	Min Pulse	G	1.731		3.447							
S204	SCK → Q	(HH)	0.560	0.971	1.576	0.013	0.024	0.038	SIN	3.0	Q	21
		(HL)	0.497	0.955	1.719	0.011	0.018	0.030	SCK	1.0	QB	22
	SCK → QB	(HH)	0.599	1.160	2.092	0.012	0.022	0.036	SMC	1.0		
		(HL)	0.706	1.256	2.090	0.009	0.015	0.024	D	1.0		
	D → Q	(HH)	0.404	0.691	1.123	0.013	0.024	0.038	G	1.0		
		(LL)	0.416	0.823	1.628	0.011	0.018	0.030				
	D → QB	(HL)	0.549	0.975	1.633	0.009	0.015	0.024				
		(LH)	0.521	1.037	2.010	0.012	0.022	0.036				
	G → Q	(HH)	0.568	0.986	1.597	0.013	0.024	0.038				
		(HL)	0.515	0.983	1.766	0.011	0.018	0.030				
	G → QB	(HH)	0.618	1.189	2.138	0.012	0.022	0.036				
		(HL)	0.713	1.270	2.106	0.009	0.015	0.024				
	Set up time	SIN	1.167		1.341							
	Set up time	SMC	1.739		2.689							
	Set up time	D	1.636		2.439							
	Hold time	SIN	0.536		0.655							
	Hold time	SMC	0.019		0.010							
	Hold time	D	0.125		0.056							
	Min Pulse	SCK	1.756		3.431							
	Min Pulse	G	1.756		3.431							

FUNCTION BLOCK

Function	D-LATCH WITH R,SPECIAL FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S301	8					
x2							
x4							

Logic Diagram



Truth Table

AMC	R	D	GB	Q	QB
1	0	0	0	0	1
1	0	1	0	1	0
1	0	X	1	LATCH	
X	1	X	X	0	1
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	0

X:Irrelevant

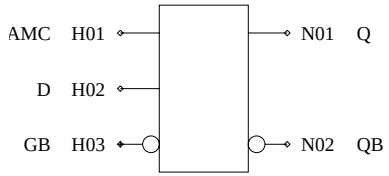
FUNCTION BLOCK

Block type	Switching speed									Input		Output	
	Path			t_{LD0} (ns)			t_1						
	IN → OUT			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S301	AMC → Q		(HH)	0.603	1.167	2.047	0.012	0.022	0.036	AMC	2.1	Q	22
			(LH)	0.678	1.287	2.217	0.012	0.022	0.036	R	1.0	QB	22
			(LL)	0.635	1.248	2.253	0.009	0.015	0.024	D	1.0		
	AMC → QB		(HL)	0.499	0.971	1.702	0.010	0.016	0.027	GB	2.1		
			(LH)	0.505	0.993	1.794	0.012	0.023	0.036				
			(LL)	0.574	1.091	1.872	0.010	0.016	0.027				
	R → Q		(HL)	0.322	0.562	0.913	0.009	0.015	0.024				
			(LH)	0.403	0.811	1.458	0.012	0.022	0.036				
	R → QB		(HH)	0.193	0.309	0.462	0.012	0.023	0.037				
			(LL)	0.299	0.615	1.113	0.010	0.016	0.027				
	D → Q		(HH)	0.607	1.154	2.001	0.012	0.022	0.036				
			(LL)	0.474	0.888	1.564	0.009	0.015	0.024				
	D → QB		(HL)	0.503	0.959	1.656	0.010	0.016	0.027				
			(LH)	0.345	0.634	1.109	0.012	0.023	0.037				
	GB → Q		(HH)	0.643	1.229	2.143	0.012	0.022	0.036				
			(LH)	0.630	1.213	2.119	0.012	0.022	0.036				
			(LL)	0.495	1.325	2.375	0.009	0.015	0.024				
	GB → QB		(HL)	0.539	1.033	1.798	0.010	0.016	0.027				
			(LH)	0.366	1.067	1.912	0.012	0.023	0.036				
			(LL)	0.526	1.018	1.775	0.010	0.016	0.027				
	Set up time	D		1.757		2.530							
	Hold time	D		0.119		0.010							
	Release time	R		1.432		1.924							
	Removal time	R		0.332		0.119							
	Min Pulse	R		1.071		2.456							
	Min Pulse	GB		1.216		2.821							

FUNCTION BLOCK

Function	D-LATCH WITH SPECIAL FUNCTION					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S302	7	S303	7			
x2							
x4							

Logic Diagram



Truth Table

AMC	D	GB	Q	QB
1	0	0	0	1
1	1	0	1	0
1	X	1	LATCH	
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0

X:Irrelevant

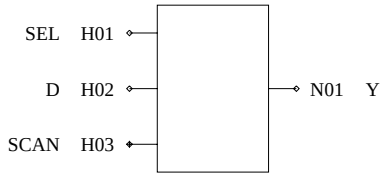
FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t LD0 (ns)			t 1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S302	AMC → Q	(HH)	0.475	0.879	1.500	0.012	0.022	0.036	AMC	2.1	Q	22
		(LH)	0.548	0.995	1.667	0.012	0.022	0.036	D	1.0	QB	22
		(LL)	0.606	1.198	2.172	0.009	0.015	0.024	GB	2.1		
	AMC → QB	(HL)	0.380	0.702	1.197	0.009	0.015	0.024				
		(LH)	0.487	0.956	1.732	0.013	0.023	0.037				
		(LL)	0.452	0.818	1.363	0.009	0.015	0.024				
	D → Q	(HH)	0.479	0.867	1.454	0.012	0.023	0.036				
		(LL)	0.442	0.841	1.489	0.009	0.015	0.024				
	D → QB	(HL)	0.384	0.690	1.150	0.009	0.015	0.025				
		(LH)	0.327	0.602	1.054	0.013	0.023	0.037				
	GB → Q	(HH)	0.515	0.940	1.596	0.012	0.022	0.036				
		(LH)	0.502	0.924	1.568	0.012	0.023	0.036				
		(LL)	0.465	1.276	2.295	0.009	0.015	0.024				
	GB → QB	(HL)	0.419	0.763	1.293	0.009	0.015	0.024				
		(LH)	0.349	1.032	1.851	0.013	0.023	0.037				
		(LL)	0.406	0.747	1.267	0.009	0.015	0.024				
	Set up time	D	1.502		2.068							
	Hold time	D	0.148		0.010							
	Min Pulse	GB	1.070		2.816							
S303	AMC → Q	(HH)	0.331	0.590	0.987	0.013	0.024	0.038	AMC	2.1	Q	21
		(LH)	0.417	0.730	1.184	0.013	0.024	0.038	D	1.0	QB	22
		(LL)	0.491	0.985	1.852	0.011	0.018	0.030	GB	2.0		
	AMC → QB	(HL)	0.465	0.857	1.469	0.009	0.015	0.024				
		(LH)	0.593	1.188	2.217	0.012	0.022	0.036				
		(LL)	0.553	0.999	1.671	0.009	0.015	0.024				
	D → Q	(HH)	0.336	0.577	0.936	0.013	0.023	0.038				
		(LL)	0.298	0.563	1.038	0.010	0.016	0.027				
	D → QB	(HL)	0.470	0.844	1.419	0.009	0.015	0.024				
		(LH)	0.394	0.750	1.369	0.012	0.023	0.036				
	GB → Q	(HH)	0.378	0.662	1.094	0.013	0.024	0.038				
		(LH)	0.363	0.654	1.079	0.013	0.024	0.038				
		(LL)	0.326	1.049	1.960	0.010	0.018	0.030				
	GB → QB	(HL)	0.514	0.932	1.581	0.009	0.015	0.024				
		(LH)	0.401	1.272	2.353	0.012	0.023	0.036				
		(LL)	0.497	0.920	1.562	0.009	0.015	0.024				
	Set up time	D	1.617		2.186							
	Hold time	D	0.140		0.010							
	Min Pulse	GB	1.084		2.722							

FUNCTION BLOCK

Function	2 TO 1 DATA SELECTOR					SSI Family	
Block type	Standard type						
	Normal		High speed				
Drivability	Name	cells	Name	cells			
Low Power							
x1	S999	4					
x2							
x4							

Logic Diagram



Truth Table

SEL	D	SCAN	Y
1	A	X	A
0	X	B	B

X:Irrelevant

FUNCTION BLOCK

Block type	Switching speed								Input		Output	
	Path		t_{LD0} (ns)			t_1						
	IN → OUT		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	Symbol	Fanin	Symbol	Fanout
S999	SEL → Y	(HH)	0.313	0.558	0.902	0.013	0.023	0.037	SEL	1.0	Y	21
		(HL)	0.295	0.568	0.996	0.010	0.016	0.026	D	1.0		
		(LH)	0.318	0.552	0.899	0.013	0.023	0.037	SCAN	1.0		
		(LL)	0.321	0.612	1.123	0.010	0.016	0.026				
	D → Y	(HH)	0.247	0.409	0.642	0.013	0.023	0.037				
		(LL)	0.268	0.497	0.901	0.010	0.016	0.026				
	SCAN → Y	(HH)	0.256	0.422	0.659	0.013	0.023	0.037				
		(LL)	0.273	0.506	0.917	0.010	0.016	0.026				

INDEX

Name	Function	I/O cells	int. cells	Page
B058	HIGH SPEED 3-STATE OUTPUT BUFFER 9mA 5kΩ PULL-UP	1	12	1-18
B059	HIGH SPEED 3-STATE OUTPUT BUFFER 18mA 5kΩ PULL-UP	1	16	1-18
B05C	HIGH SPEED I/O BUFFER 6mA 5kΩ PULL-UP	1	16	1-28
B05E	HIGH SPEED 3-STATE OUTPUT BUFFER 6mA 5kΩ PULL-UP	1	12	1-18
B05F	HIGH SPEED I/O BUFFER 24mA 5kΩ PULL-UP	1	20	1-28
B05H	HIGH SPEED 3-STATE OUTPUT BUFFER 24mA 5kΩ PULL-UP	1	16	1-18
B05T	HIGH SPEED 3-STATE OUTPUT BUFFER 3mA 5kΩ PULL-UP	1	12	1-18
B05U	HIGH SPEED I/O BUFFER 3mA 5kΩ PULL-UP	1	16	1-28
B0D1	I/O BUFFER 12mA 50kΩ PULL-DOWN	1	10	1-24
B0D3	I/O BUFFER 9mA 50kΩ PULL-DOWN	1	10	1-24
B0D5	I/O BUFFER 18mA 50kΩ PULL-DOWN	1	14	1-24
B0D7	3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-DOWN	1	6	1-14
B0D8	3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-DOWN	1	6	1-14
B0D9	3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-DOWN	1	10	1-14
B0DC	I/O BUFFER 6mA 50kΩ PULL-DOWN	1	10	1-24
B0DE	3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-DOWN	1	6	1-14
B0DF	I/O BUFFER 24mA 50kΩ PULL-DOWN	1	14	1-24
B0DH	3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-DOWN	1	10	1-14
B0DT	3-STATE OUTPUT BUFFER 3mA 50kΩ PULL-DOWN	1	6	1-14
B0DU	I/O BUFFER 3mA 50kΩ PULL-DOWN	1	10	1-24
B0U1	I/O BUFFER 12mA 50kΩ PULL-UP	1	10	1-24
B0U3	I/O BUFFER 9mA 50kΩ PULL-UP	1	10	1-24
B0U5	I/O BUFFER 18mA 50kΩ PULL-UP	1	14	1-24
B0U7	3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-UP	1	6	1-14
B0U8	3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-UP	1	6	1-14
B0U9	3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-UP	1	10	1-14
B0UC	I/O BUFFER 6mA 50kΩ PULL-UP	1	10	1-24
B0UE	3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-UP	1	6	1-14
B0UF	I/O BUFFER 24mA 50kΩ PULL-UP	1	14	1-24
B0UH	3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-UP	1	10	1-14
B0UT	3-STATE OUTPUT BUFFER 3mA 50kΩ PULL-UP	1	6	1-14
B0UU	I/O BUFFER 3mA 50kΩ PULL-UP	1	10	1-24
B0W1	I/O BUFFER 12mA 5kΩ PULL-UP	1	10	1-24
B0W3	I/O BUFFER 9mA 5kΩ PULL-UP	1	10	1-24
B0W5	I/O BUFFER 18mA 5kΩ PULL-UP	1	14	1-24
B0W7	3-STATE OUTPUT BUFFER 12mA 5kΩ PULL-UP	1	6	1-14
B0W8	3-STATE OUTPUT BUFFER 9mA 5kΩ PULL-UP	1	6	1-14
B0W9	3-STATE OUTPUT BUFFER 18mA 5kΩ PULL-UP	1	10	1-14
B0WC	I/O BUFFER 6mA 5kΩ PULL-UP	1	10	1-24
B0WE	3-STATE OUTPUT BUFFER 6mA 5kΩ PULL-UP	1	6	1-14
B0WF	I/O BUFFER 24mA 5kΩ PULL-UP	1	14	1-24
B0WH	3-STATE OUTPUT BUFFER 24mA 5kΩ PULL-UP	1	10	1-14
B0WT	3-STATE OUTPUT BUFFER 3mA 5kΩ PULL-UP	1	6	1-14
B0WU	I/O BUFFER 3mA 5kΩ PULL-UP	1	10	1-24
BD07	CMOS 3-STATE OUTPUT BUFFER 12mA	1	42	2-16
BD08	CMOS 3-STATE OUTPUT BUFFER 9mA	1	42	2-16
BD09	CMOS 3-STATE OUTPUT BUFFER 18mA	2	42	2-16
BD0E	CMOS 3-STATE OUTPUT BUFFER 6mA	1	32	2-16
BD0H	CMOS 3-STATE OUTPUT BUFFER 24mA	2	42	2-16
BD0T	CMOS 3-STATE OUTPUT BUFFER 3mA	1	32	2-16
BD17	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 12mA	1	42	2-24
BD18	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 9mA	1	42	2-24
BD19	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 18mA	2	42	2-24

Name	Function	I/O cells	int. cells	Page
BD1E	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 6mA	1	32	2-24
BD1H	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 24mA	2	42	2-24
BD1T	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 3mA	1	32	2-24
BD27	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-DOWN	1	42	2-24
BD28	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-DOWN	1	42	2-24
BD29	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-DOWN	2	42	2-24
BD2E	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-DOWN	1	32	2-24
BD2H	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-DOWN	2	42	2-24
BD2T	TTL HIGH SPEED 3-STATE OUTPUT BUFFER 3mA 50kΩ PULL-DOWN	1	32	2-24
BE01	LOW-NOISE I/O BUFFER 12mA	1	10	1-26
BE03	LOW-NOISE I/O BUFFER 9mA	1	10	1-26
BE05	LOW-NOISE I/O BUFFER 18mA	1	10	1-26
BE07	LOW-NOISE 3-STATE OUTPUT BUFFER 12mA	1	6	1-16
BE08	LOW-NOISE 3-STATE OUTPUT BUFFER 9mA	1	6	1-16
BE09	LOW-NOISE 3-STATE OUTPUT BUFFER 18mA	1	6	1-16
BE0C	LOW-NOISE I/O BUFFER 6mA	1	10	1-26
BE0E	LOW-NOISE 3-STATE OUTPUT BUFFER 6mA	1	6	1-16
BE0F	LOW-NOISE I/O BUFFER 24mA	1	10	1-26
BE0H	LOW-NOISE 3-STATE OUTPUT BUFFER 24mA	1	6	1-16
BED1	LOW-NOISE I/O BUFFER 12mA 50kΩ PULL-DOWN	1	10	1-26
BED3	LOW-NOISE I/O BUFFER 9mA 50kΩ PULL-DOWN	1	10	1-26
BED5	LOW-NOISE I/O BUFFER 18mA 50kΩ PULL-DOWN	1	10	1-26
BED7	LOW-NOISE 3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-DOWN	1	6	1-16
BED8	LOW-NOISE 3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-DOWN	1	6	1-16
BED9	LOW-NOISE 3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-DOWN	1	6	1-16
BEDC	LOW-NOISE I/O BUFFER 6mA 50kΩ PULL-DOWN	1	10	1-26
BEDE	LOW-NOISE 3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-DOWN	1	6	1-16
BEDF	LOW-NOISE I/O BUFFER 24mA 50kΩ PULL-DOWN	1	10	1-26
BEDH	LOW-NOISE 3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-DOWN	1	6	1-16
BEU1	LOW-NOISE I/O BUFFER 12mA 50kΩ PULL-UP	1	10	1-26
BEU3	LOW-NOISE I/O BUFFER 9mA 50kΩ PULL-UP	1	10	1-26
BEU5	LOW-NOISE I/O BUFFER 18mA 50kΩ PULL-UP	1	10	1-26
BEU7	LOW-NOISE 3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-UP	1	6	1-16
BEU8	LOW-NOISE 3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-UP	1	6	1-16
BEU9	LOW-NOISE 3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-UP	1	6	1-16
BEUC	LOW-NOISE I/O BUFFER 6mA 50kΩ PULL-UP	1	10	1-26
BEUE	LOW-NOISE 3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-UP	1	6	1-16
BEUF	LOW-NOISE I/O BUFFER 24mA 50kΩ PULL-UP	1	10	1-26
BEUH	LOW-NOISE 3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-UP	1	6	1-16
BEW1	LOW-NOISE I/O BUFFER 12mA 5kΩ PULL-UP	1	10	1-26
BEW3	LOW-NOISE I/O BUFFER 9mA 5kΩ PULL-UP	1	10	1-26
BEW5	LOW-NOISE I/O BUFFER 18mA 5kΩ PULL-UP	1	10	1-26
BEW7	LOW-NOISE 3-STATE OUTPUT BUFFER 12mA 5kΩ PULL-UP	1	6	1-16
BEW8	LOW-NOISE 3-STATE OUTPUT BUFFER 9mA 5kΩ PULL-UP	1	6	1-16
BEW9	LOW-NOISE 3-STATE OUTPUT BUFFER 18mA 5kΩ PULL-UP	1	6	1-16
BEWC	LOW-NOISE I/O BUFFER 6mA 5kΩ PULL-UP	1	10	1-26
BEWE	LOW-NOISE 3-STATE OUTPUT BUFFER 6mA 5kΩ PULL-UP	1	6	1-16
BEWF	LOW-NOISE I/O BUFFER 24mA 5kΩ PULL-UP	1	10	1-26
BEWH	LOW-NOISE 3-STATE OUTPUT BUFFER 24mA 5kΩ PULL-UP	1	6	1-16
BFD1	LOW-NOISE SCHMITT I/O BUFFER 12mA 50kΩ PULL-DOWN	1	14	1-32
BFD3	LOW-NOISE SCHMITT I/O BUFFER 9mA 50kΩ PULL-DOWN	1	14	1-32
BFD5	LOW-NOISE SCHMITT I/O BUFFER 18mA 50kΩ PULL-DOWN	1	14	1-32
BFDC	LOW-NOISE SCHMITT I/O BUFFER 6mA 50kΩ PULL-DOWN	1	14	1-32

Name	Function	I/O cells	int. cells	Page
BFDF	LOW-NOISE SCHMITT I/O BUFFER 24mA 50kΩ PULL-DOWN	1	14	1-32
BFI1	LOW-NOISE SCHMITT I/O BUFFER 12mA	1	14	1-32
BFI3	LOW-NOISE SCHMITT I/O BUFFER 9mA	1	14	1-32
BFI5	LOW-NOISE SCHMITT I/O BUFFER 18mA	1	14	1-32
BFIC	LOW-NOISE SCHMITT I/O BUFFER 6mA	1	14	1-32
BFIF	LOW-NOISE SCHMITT I/O BUFFER 24mA	1	14	1-32
BFU1	LOW-NOISE SCHMITT I/O BUFFER 12mA 50kΩ PULL-UP	1	14	1-32
BFU3	LOW-NOISE SCHMITT I/O BUFFER 9mA 50kΩ PULL-UP	1	14	1-32
BFU5	LOW-NOISE SCHMITT I/O BUFFER 18mA 50kΩ PULL-UP	1	14	1-32
BFUC	LOW-NOISE SCHMITT I/O BUFFER 6mA 50kΩ PULL-UP	1	14	1-32
BFUF	LOW-NOISE SCHMITT I/O BUFFER 24mA 50kΩ PULL-UP	1	14	1-32
BFW1	LOW-NOISE SCHMITT I/O BUFFER 12mA 5kΩ PULL-UP	1	14	1-32
BFW3	LOW-NOISE SCHMITT I/O BUFFER 9mA 5kΩ PULL-UP	1	14	1-32
BFW5	LOW-NOISE SCHMITT I/O BUFFER 18mA 5kΩ PULL-UP	1	14	1-32
BFWC	LOW-NOISE SCHMITT I/O BUFFER 6mA 5kΩ PULL-UP	1	14	1-32
BFWF	LOW-NOISE SCHMITT I/O BUFFER 24mA 5kΩ PULL-UP	1	14	1-32
BG0W	GTL I/O BUFFER	2	26	4-12
BJ07	CMOS LOW-NOISE 3-STATE OUTPUT BUFFER 12mA	1	20	2-18
BJ09	CMOS LOW-NOISE 3-STATE OUTPUT BUFFER 18mA	2	20	2-18
BJ0H	CMOS LOW-NOISE 3-STATE OUTPUT BUFFER 24mA	2	20	2-18
BKD3	TTL SCHMITT I/O BUFFER 9mA 50kΩ PULL-DOWN	1	28	2-44
BKDC	TTL SCHMITT I/O BUFFER 6mA 50kΩ PULL-DOWN	1	24	2-44
BKDK	TTL SCHMITT I/O BUFFER 2mA 50kΩ PULL-DOWN	1	24	2-44
BKDU	TTL SCHMITT I/O BUFFER 3mA 50kΩ PULL-DOWN	1	24	2-44
BKDX	TTL SCHMITT I/O BUFFER 1mA 50kΩ PULL-DOWN	1	24	2-44
BKI3	TTL SCHMITT I/O BUFFER 9mA	1	28	2-44
BKIC	TTL SCHMITT I/O BUFFER 6mA	1	24	2-44
BKIK	TTL SCHMITT I/O BUFFER 2mA	1	24	2-44
BKIU	TTL SCHMITT I/O BUFFER 3mA	1	24	2-44
BKIX	TTL SCHMITT I/O BUFFER 1mA	1	24	2-44
BM01	CMOS I/O BUFFER 12mA	1	46	2-30
BM03	CMOS I/O BUFFER 9mA	1	46	2-30
BM05	CMOS I/O BUFFER 18mA	2	46	2-30
BM0C	CMOS I/O BUFFER 6mA	1	36	2-30
BM0F	CMOS I/O BUFFER 24mA	2	46	2-30
BM0U	CMOS I/O BUFFER 3mA	1	36	2-30
BM11	TTL HIGH SPEED I/O BUFFER 12mA	1	46	2-42
BM13	TTL HIGH SPEED I/O BUFFER	1	46	2-42
BM15	TTL HIGH SPEED I/O BUFFER 18mA	2	46	2-42
BM1C	TTL HIGH SPEED I/O BUFFER 6mA	1	36	2-42
BM1F	TTL HIGH SPEED I/O BUFFER 24mA	2	46	2-42
BM1U	TTL HIGH SPEED I/O BUFFER 3mA	1	36	2-42
BM21	TTL HIGH SPEED I/O BUFFER 12mA 50kΩ PULL-DOWN	1	46	2-42
BM23	TTL HIGH SPEED I/O BUFFER 9mA 50kΩ PULL-DOWN	1	46	2-42
BM25	TTL HIGH SPEED I/O BUFFER 18mA 50kΩ PULL-DOWN	2	46	2-42
BM2C	TTL HIGH SPEED I/O BUFFER 6mA 50kΩ PULL-DOWN	1	36	2-42
BM2F	TTL HIGH SPEED I/O BUFFER 24mA 50kΩ PULL-DOWN	2	46	2-42
BM2U	TTL HIGH SPEED I/O BUFFER 3mA 50kΩ PULL-DOWN	1	36	2-42
BN3133	I/O BUFFER WITH EN(OR) 12mA	1	16	1-34
BN3135	CMOS I/O BUFFER WITH EN(OR) 12mA	1	32	2-48
BN3333	I/O BUFFER WITH EN(OR) 9mA	1	16	1-34
BN3335	CMOS I/O BUFFER WITH EN(OR) 9mA	1	32	2-48

Name	Function	I/O cells	int. cells	Page
BN3533	I/O BUFFER WITH EN(OR) 18mA	1	20	1-34
BN3535	CMOS I/O BUFFER WITH EN(OR) 18mA	2	36	2-48
BN3C33	I/O BUFFER WITH EN(OR) 6mA	1	16	1-34
BN3C35	CMOS I/O BUFFER WITH EN(OR) 6mA	1	32	2-48
BN3F33	I/O BUFFER WITH EN(OR) 24mA	1	20	1-34
BN3F35	CMOS I/O BUFFER WITH EN(OR) 24mA	2	36	2-48
BN3U33	I/O BUFFER WITH EN(OR) 3mA	1	16	1-34
BN3U35	CMOS I/O BUFFER WITH EN(OR) 3mA	1	32	2-48
BN5133	I/O BUFFER WITH EN(OR) 12mA 50kΩ PULL-DOWN	1	16	1-34
BN5333	I/O BUFFER WITH EN(OR) 9mA 50kΩ PULL-DOWN	1	16	1-34
BN5533	I/O BUFFER WITH EN(OR) 18mA 50kΩ PULL-DOWN	1	20	1-34
BN5C33	I/O BUFFER WITH EN(OR) 6mA 50kΩ PULL-DOWN	1	16	1-34
BN5F33	I/O BUFFER WITH EN(OR) 24mA 50kΩ PULL-DOWN	1	20	1-34
BN5U33	I/O BUFFER WITH EN(OR) 3mA 50kΩ PULL-DOWN	1	16	1-34
BN6135	TTL I/O BUFFER WITH EN(OR) 12mA	1	46	2-54
BN6335	TTL I/O BUFFER WITH EN(OR) 9mA	1	46	2-54
BN6535	TTL I/O BUFFER WITH EN(OR) 18mA	2	46	2-54
BN6C35	TTL I/O BUFFER WITH EN(OR) 6mA	1	36	2-54
BN6F35	TTL I/O BUFFER WITH EN(OR) 24mA	2	46	2-54
BN6U35	TTL I/O BUFFER WITH EN(OR) 3mA	1	36	2-54
BN7133	LOW NOISE I/O BUFFER WITH EN(OR) 12mA	1	10	1-38
BN7135	CMOS LOW NOISE I/O BUFFER WITH EN(OR) 12mA	1	24	2-52
BN7333	LOW NOISE I/O BUFFER WITH EN(OR) 9mA	1	10	1-38
BN7533	LOW NOISE I/O BUFFER WITH EN(OR) 18mA	1	10	1-38
BN7535	CMOS LOW NOISE I/O BUFFER WITH EN(OR) 18mA	2	24	2-52
BN7C33	LOW NOISE I/O BUFFER WITH EN(OR) 6mA	1	10	1-38
BN7F33	LOW NOISE I/O BUFFER WITH EN(OR) 24mA	1	10	1-38
BN7F35	CMOS LOW NOISE I/O BUFFER WITH EN(OR) 24mA	2	24	2-52
BN9135	TTL I/O BUFFER WITH EN(OR) 12mA 50kΩ PULL-DOWN	1	46	2-54
BN9335	TTL I/O BUFFER WITH EN(OR) 9mA 50kΩ PULL-DOWN	1	46	2-54
BN9535	TTL I/O BUFFER WITH EN(OR) 18mA 50kΩ PULL-DOWN	2	46	2-54
BN9C35	TTL I/O BUFFER WITH EN(OR) 6mA 50kΩ PULL-DOWN	1	36	2-54
BN9F35	TTL I/O BUFFER WITH EN(OR) 24mA 50kΩ PULL-DOWN	2	46	2-54
BN9U35	TTL I/O BUFFER WITH EN(OR) 3mA 50kΩ PULL-DOWN	1	36	2-54
BNA135	LOW NOISE I/O BUFFER WITH EN(OR) 12mA	1	20	2-58
BNA535	LOW NOISE I/O BUFFER WITH EN(OR) 18mA	2	20	2-58
BNAF35	LOW NOISE I/O BUFFER WITH EN(OR) 24mA	2	20	2-58
BNB133	LOW NOISE I/O BUFFER WITH EN(OR) 12mA 50kΩ PULL-DOWN	1	10	1-38
BNB333	LOW NOISE I/O BUFFER WITH EN(OR) 9mA 50kΩ PULL-DOWN	1	10	1-38
BNB533	LOW NOISE I/O BUFFER WITH EN(OR) 18mA 50kΩ PULL-DOWN	1	10	1-38
BNBC33	LOW NOISE I/O BUFFER WITH EN(OR) 6mA 50kΩ PULL-DOWN	1	10	1-38
BNBF33	LOW NOISE I/O BUFFER WITH EN(OR) 24mA 50kΩ PULL-DOWN	1	10	1-38
BND135	LOW NOISE I/O BUFFER WITH EN(OR) 12mA 50kΩ PULL-DOWN	1	20	2-58
BND535	LOW NOISE I/O BUFFER WITH EN(OR) 18mA 50kΩ PULL-DOWN	2	20	2-58
BNDF35	LOW NOISE I/O BUFFER WITH EN(OR) 24mA 50kΩ PULL-DOWN	2	20	2-58
BP01	CMOS LOW-NOISE I/O BUFFER 12mA	1	24	2-32
BP05	CMOS LOW-NOISE I/O BUFFER 18mA	2	24	2-32
BP0F	CMOS LOW-NOISE I/O BUFFER 24mA	2	24	2-32
BQI1	CMOS SCHMITT I/O BUFFER 12mA	1	50	2-34
BQI3	CMOS SCHMITT I/O BUFFER 9mA	1	50	2-34
BQI5	CMOS SCHMITT I/O BUFFER 18mA	2	50	2-34
BQIC	CMOS SCHMITT I/O BUFFER 6mA	1	40	2-34
BQIF	CMOS SCHMITT I/O BUFFER 24mA	2	50	2-34

Name	Function	I/O cells	int. cells	Page
BQIU	CMOS SCHMITT I/O BUFFER 3mA	1	40	2-34
BSD1	SCHMITT I/O BUFFER 12mA 50kΩ PULL-DOWN	1	14	1-30
BSD3	SCHMITT I/O BUFFER 9mA 50kΩ PULL-DOWN	1	14	1-30
BSD5	SCHMITT I/O BUFFER 18mA 50kΩ PULL-DOWN	1	18	1-30
BSDC	SCHMITT I/O BUFFER 6mA 50kΩ PULL-DOWN	1	14	1-30
BSDF	SCHMITT I/O BUFFER 24mA 50kΩ PULL-DOWN	1	18	1-30
BSDU	SCHMITT I/O BUFFER 3mA 50kΩ PULL-DOWN	1	14	1-30
BSI1	SCHMITT I/O BUFFER 12mA	1	14	1-30
BSI3	SCHMITT I/O BUFFER 9mA	1	14	1-30
BSI5	SCHMITT I/O BUFFER 18mA	1	18	1-30
BSIC	SCHMITT I/O BUFFER 6mA	1	14	1-30
BSIF	SCHMITT I/O BUFFER 24mA	1	18	1-30
BSIU	SCHMITT I/O BUFFER 3mA	1	14	1-30
BSU1	SCHMITT I/O BUFFER 12mA 50kΩ PULL-UP	1	14	1-30
BSU3	SCHMITT I/O BUFFER 9mA 50kΩ PULL-UP	1	14	1-30
BSU5	SCHMITT I/O BUFFER 18mA 50kΩ PULL-UP	1	18	1-30
BSUC	SCHMITT I/O BUFFER 6mA 50kΩ PULL-UP	1	14	1-30
BSUF	SCHMITT I/O BUFFER 24mA 50kΩ PULL-UP	1	18	1-30
BSUU	SCHMITT I/O BUFFER 3mA 50kΩ PULL-UP	1	14	1-30
BSW1	SCHMITT I/O BUFFER 12mA 5kΩ PULL-UP	1	14	1-30
BSW3	SCHMITT I/O BUFFER 9mA 5kΩ PULL-UP	1	14	1-30
BSW5	SCHMITT I/O BUFFER 18mA 5kΩ PULL-UP	1	18	1-30
BSWC	SCHMITT I/O BUFFER 6mA 5kΩ PULL-UP	1	14	1-30
BSWF	SCHMITT I/O BUFFER 24mA 5kΩ PULL-UP	1	18	1-30
BSWU	SCHMITT I/O BUFFER 3mA 5kΩ PULL-UP	1	14	1-30
BUI1	CMOS LOW-NOISE SCHMITT I/O BUFFER 12mA	1	28	2-36
BUI5	CMOS LOW-NOISE SCHMITT I/O BUFFER 18mA	2	28	2-36
BUIF	CMOS LOW-NOISE SCHMITT I/O BUFFER 24mA	2	28	2-36
BV08	TTL 3-STATE OUTPUT BUFFER 9mA	1	20	2-20
BV0E	TTL 3-STATE OUTPUT BUFFER 6mA	1	16	2-20
BV0M	TTL 3-STATE OUTPUT BUFFER 2mA	1	16	2-20
BV0Q	TTL 3-STATE OUTPUT BUFFER 1mA	1	16	2-20
BV0T	TTL 3-STATE OUTPUT BUFFER 3mA	1	16	2-20
BVD8	TTL 3-STATE OUTPUT BUFFER 9mA 50kΩ PULL-DOWN	1	20	2-20
BVDE	TTL 3-STATE OUTPUT BUFFER 6mA 50kΩ PULL-DOWN	1	16	2-20
BVDM	TTL 3-STATE OUTPUT BUFFER 2mA 50kΩ PULL-DOWN	1	16	2-20
BVDQ	TTL 3-STATE OUTPUT BUFFER 1mA 50kΩ PULL-DOWN	1	16	2-20
BVDT	TTL 3-STATE OUTPUT BUFFER 3mA 50kΩ PULL-DOWN	1	16	2-20
BW03	TTL I/O BUFFER 9mA	1	24	2-38
BW0C	TTL I/O BUFFER 6mA	1	20	2-38
BW0K	TTL I/O BUFFER 2mA	1	20	2-38
BW0U	TTL I/O BUFFER 3mA	1	20	2-38
BW0X	TTL I/O BUFFER 1mA	1	20	2-38
BWD3	TTL I/O BUFFER 9mA 50kΩ PULL-DOWN	1	24	2-38
BWDC	TTL I/O BUFFER 6mA 50kΩ PULL-DOWN	1	20	2-38
BWDK	TTL I/O BUFFER 2mA 50kΩ PULL-DOWN	1	20	2-38
BWDU	TTL I/O BUFFER 3mA 50kΩ PULL-DOWN	1	20	2-38
BWDX	TTL I/O BUFFER 1mA 50kΩ PULL-DOWN	1	20	2-38
BX01	TTL LOW-NOISE I/O BUFFER 12mA	1	20	2-40
BX05	TTL LOW-NOISE I/O BUFFER 18mA	2	20	2-40
BX0F	TTL LOW-NOISE I/O BUFFER 24mA	2	20	2-40
BXD1	TTL LOW-NOISE I/O BUFFER 12mA 50kΩ PULL-DOWN	1	20	2-40
BXD5	TTL LOW-NOISE I/O BUFFER 18mA 50kΩ PULL-DOWN	2	20	2-40

Name	Function	I/O cells	int. cells	Page
BXDF	TTL LOW-NOISE I/O BUFFER 24mA 50kΩ PULL-DOWN	2	20	2-40
BY07	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 12mA	1	16	2-22
BY09	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 18mA	2	16	2-22
BY0H	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 24mA	2	16	2-22
BYD7	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 12mA 50kΩ PULL-DOWN	1	16	2-22
BYD9	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 18mA 50kΩ PULL-DOWN	2	16	2-22
BYDH	TTL LOW-NOISE 3-STATE OUTPUT BUFFER 24mA 50kΩ PULL-DOWN	2	16	2-22
BZD1	TTL LOW-NOISE SCHMITT I/O BUFFER 12mA 50kΩ PULL-DOWN	1	24	2-46
BZD5	TTL LOW-NOISE SCHMITT I/O BUFFER 18mA 50kΩ PULL-DOWN	2	24	2-46
BZDF	TTL LOW-NOISE SCHMITT I/O BUFFER 24mA 50kΩ PULL-DOWN	2	24	2-46
BZI1	TTL LOW-NOISE SCHMITT I/O BUFFER 12mA	1	24	2-46
BZI5	TTL LOW-NOISE SCHMITT I/O BUFFER 18mA	2	24	2-46
BZIF	TTL LOW-NOISE SCHMITT I/O BUFFER 24mA	2	24	2-46
EET1	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 9mA	1	2	1-22
EET3	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 9mA 50kΩ PULL-UP	1	2	1-22
EET5	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 18mA	1	2	1-22
EET7	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 18mA 50kΩ PULL-UP	1	2	1-22
EET9	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 12mA	1	2	1-22
EETB	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 12mA 50kΩ PULL-UP	1	2	1-22
EETD	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 24mA	1	2	1-22
EETF	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 24mA 50kΩ PULL-UP	1	2	1-22
EETJ	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 6mA	1	2	1-22
EEUJ	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 6mA 50kΩ PULL-UP	1	2	1-22
EEW3	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 9mA 5kΩ PULL--UP	1	2	1-22
EEW7	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 18mA 5kΩ PULL-UP	1	2	1-22
EEWB	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 12mA 5kΩ PULL-UP	1	2	1-22
EEWF	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 24mA 5kΩ PULL-UP	1	2	1-22
EEWJ	LOW-NOISE N-CH OPEN DRAIN OUTPUT BUFFER 6mA 5kΩ PULL-UP	1	2	1-22
EGTL	GTL OUTPUT BUFFER WITH ENB	2	18	4-10
EVT5	TTL N-CH OPEN DRAIN OUTPUT BUFFER 18mA	2	8	2-26
EVT9	TTL N-CH OPEN DRAIN OUTPUT BUFFER 12mA	1	8	2-26
EVTD	TTL N-CH OPEN DRAIN OUTPUT BUFFER 24mA	2	8	2-26
EVTH	TTL N-CH OPEN DRAIN OUTPUT BUFFER 3mA	1	4	2-26
EVTJ	TTL N-CH OPEN DRAIN OUTPUT BUFFER 6mA	1	4	2-26
EXT1	N-CH OPEN DRAIN OUTPUT BUFFER 9mA	1	4	1-20
EXT3	N-CH OPEN DRAIN OUTPUT BUFFER 9mA 50kΩ PULL-UP	1	4	1-20
EXT5	N-CH OPEN DRAIN OUTPUT BUFFER 18mA	1	8	1-20
EXT7	N-CH OPEN DRAIN OUTPUT BUFFER 18mA 50kΩ PULL-UP	1	8	1-20
EXT9	N-CH OPEN DRAIN OUTPUT BUFFER 12mA	1	4	1-20
EXTB	N-CH OPEN DRAIN OUTPUT BUFFER 12mA 50kΩ PULL-UP	1	4	1-20
EXTD	N-CH OPEN DRAIN OUTPUT BUFFER 24mA	1	8	1-20
EXTF	N-CH OPEN DRAIN OUTPUT BUFFER 24mA 50kΩ PULL-UP	1	8	1-20
EXTH	N-CH OPEN DRAIN OUTPUT BUFFER 3mA	1	4	1-20
EXTJ	N-CH OPEN DRAIN OUTPUT BUFFER 6mA	1	4	1-20
EXUH	N-CH OPEN DRAIN OUTPUT BUFFER 3mA 50kΩ PULL-UP	1	4	1-20
EXUJ	N-CH OPEN DRAIN OUTPUT BUFFER 6mA 50kΩ PULL-UP	1	4	1-20
EXW3	N-CH OPEN DRAIN OUTPUT BUFFER 9mA 5kΩ PULL-UP	1	4	1-20
EXW7	N-CH OPEN DRAIN OUTPUT BUFFER 18mA 5kΩ PULL-UP	1	8	1-20
EXWB	N-CH OPEN DRAIN OUTPUT BUFFER 12mA 5kΩ PULL-UP	1	4	1-20
EXWF	N-CH OPEN DRAIN OUTPUT BUFFER 24mA 5kΩ PULL-UP	1	8	1-20
EXWH	N-CH OPEN DRAIN OUTPUT BUFFER 3mA 5kΩ PULL-UP	1	4	1-20
EXWJ	N-CH OPEN DRAIN OUTPUT BUFFER 6mA 5kΩ PULL-UP	1	4	1-20

Name	Function	I/O cells	int. cells	Page
F433NB	1-3-INPUT OR-AND-INVERTER	-	5	6-150
F433NBP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-150
F433NC	1-3-INPUT OR-AND-INVERTER	-	6	6-150
F433NCP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	7	6-150
F433ND	1-3-INPUT OR-AND-INVERTER	-	6	6-150
F433NDP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	7	6-150
F433NE	1-3-INPUT OR-AND-INVERTER	-	5	6-150
F433NEP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-150
F433NF	1-3-INPUT OR-AND-INVERTER	-	5	6-150
F433NFP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-150
F433NG	1-3-INPUT OR-AND-INVERTER	-	6	6-150
F433NGP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	7	6-150
F433NP	1-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	5	6-150
F434	2-2-INPUT OR-AND-INVERTER	-	4	6-156
F434NA	2-2-INPUT OR-AND-INVERTER	-	5	6-156
F434NAP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-156
F434NB	2-2-INPUT OR-AND-INVERTER	-	5	6-156
F434NBP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-156
F434NC	2-2-INPUT OR-AND-INVERTER	-	6	6-156
F434NCP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	7	6-156
F434ND	2-2-INPUT OR-AND-INVERTER	-	5	6-156
F434NDP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-156
F434NE	2-2-INPUT OR-AND-INVERTER	-	6	6-156
F434NEP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	7	6-156
F434NP	2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	5	6-156
F435	2-3-INPUT OR-AND-INVERTER	-	5	6-160
F435NP	2-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-160
F436	3-3-INPUT OR-AND-INVERTER	-	6	6-162
F436NP	3-3-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-162
F437	1-2-2-INPUT OR-AND-INVERTER	-	5	6-164
F437NP	1-2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-164
F438	2-2-2-INPUT OR-AND-INVERTER	-	6	6-166
F438NP	2-2-2-INPUT OR-AND-INVERTER (X2 DRIVE)	-	6	6-166
F442	4-4-INPUT AND-OR-INVERTER	-	8	6-136
F454	2-2-2-2-INPUT OR-AND-INVERTER	-	8	6-168
F462	1-2-3-INPUT AND-OR-INVERTER	-	6	6-138
F511	2-INPUT EXCLUSIVE OR	-	4	6-98
F512	2-INPUT EXCLUSIVE NOR	-	4	6-102
F516	3-INPUT EXCLUSIVE OR	-	8	6-100
F517	3-INPUT EXCLUSIVE NOR	-	8	6-104
F521	1-BIT FULL ADDER	-	9	6-332
F523	4-BIT FULL ADDER	-	34	6-334
F526	4-BIT LOOK AHEAD CARRY GENERATOR	-	34	6-338
F527	1-BIT CARRY LOOK AHEAD ADDER	-	68	6-340
F531	3-STATE BUFFER WITH EN	-	5	6-16
F532	3-STATE BUFFER WITH ENB	-	5	6-16
F550	QUAD 8 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	64	6-312
F551	QUAD 4 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	27	6-304
F552	QUAD 2 TO 1 MULTIPLEXER POSITIVE OUTPUT	-	13	6-298
F553	QUAD 8 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	64	6-316
F554	QUAD 4 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	31	6-304
F555	QUAD 2 TO 1 MULTIPLEXER NEGATIVE OUTPUT	-	9	6-298
F560	2 TO 4 DECODER POSITIVE OUTPUT	-	10	6-320

Name	Function	I/O cells	int. cells	Page
F666NBP	D-F/F (CB) WITH SB QB OUT ONLY (X2 DRIVE)	-	9	6-248
F666NP	D-F/F (CB) WITH SB (X2 DRIVE)	-	11	6-248
F666NQ	D-F/F (CB) WITH SB Q OUT ONLY	-	8	6-248
F666NQP	D-F/F (CB) WITH SB Q OUT ONLY (X2 DRIVE)	-	9	6-248
F667	D-F/F (CB) WITH RB,SB	-	10	6-252
F667NB	D-F/F (CB) WITH RB,SB QB OUT ONLY	-	9	6-252
F667NBP	D-F/F (CB) WITH RB,SB QB OUT ONLY (X2 DRIVE)	-	10	6-252
F667NP	D-F/F (CB) WITH RB,SB (X2 DRIVE)	-	12	6-252
F667NQ	D-F/F (CB) WITH RB,SB Q OUT ONLY	-	9	6-252
F667NQP	D-F/F (CB) WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	10	6-252
F6R1	D-LATCH HIGH SPEED	-	6	6-174
F6R2	D-LATCH WITH R HIGH SPEED	-	7	6-180
F6R5	D-LATCH WITH RB HIGH SPEED	-	6	6-186
F6R8	D-LATCH (GB) HIGH SPEED	-	6	6-194
F714	T-F/F WITH R,S	-	9	6-264
F717	T-F/F WITH RB,SB	-	9	6-268
F737	T-F/F (TB) WITH RB,SB	-	9	6-272
F744	T-F/F WITH R,S	-	9	6-264
F744NP	T-F/F WITH R,S (X2 DRIVE)	-	11	6-264
F744NQ	T-F/F WITH R,S Q OUT ONLY	-	8	6-264
F744NQP	T-F/F WITH R,S Q OUT ONLY (X2 DRIVE)	-	9	6-264
F747	T-F/F WITH RB,SB	-	9	6-268
F747NP	T-F/F WITH RB,SB (X2 DRIVE)	-	11	6-268
F747NQ	T-F/F WITH RB,SB Q OUT ONLY	-	8	6-268
F747NQP	T-F/F WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	9	6-268
F767	T-F/F (TB) WITH RB,SB	-	9	6-272
F767NP	T-F/F (TB) WITH RB,SB (X2 DRIVE)	-	11	6-272
F767NQ	T-F/F (TB) WITH RB,SB Q OUT ONLY	-	8	6-272
F767NQP	T-F/F (TB) WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	9	6-272
F771	JK-F/F	-	10	6-280
F771NB	JK-F/F QB OUT ONLY	-	9	6-280
F771NBP	JK-F/F QB OUT ONLY (X2 DRIVE)	-	10	6-280
F771NP	JK-F/F (X2 DRIVE)	-	12	6-280
F771NQ	JK-F/F Q OUT ONLY	-	9	6-280
F771NQP	JK-F/F Q OUT ONLY (X2 DRIVE)	-	10	6-280
F774	JK-F/F WITH R,S	-	12	6-282
F774NB	JK-F/F WITH R,S QB OUT ONLY	-	11	6-282
F774NBP	JK-F/F WITH R,S QB OUT ONLY (X2 DRIVE)	-	12	6-282
F774NP	JK-F/F WITH R,S (X2 DRIVE)	-	14	6-282
F774NQ	JK-F/F WITH R,S Q OUT ONLY	-	11	6-282
F774NQP	JK-F/F WITH R,S Q OUT ONLY (X2 DRIVE)	-	12	6-282
F777	JK-F/F WITH RB,SB	-	12	6-286
F777NB	JK-F/F WITH RB,SB QB OUT ONLY	-	11	6-286
F777NBP	JK-F/F WITH RB,SB QB OUT ONLY (X2 DRIVE)	-	12	6-286
F777NP	JK-F/F WITH RB,SB (X2 DRIVE)	-	14	6-286
F777NQ	JK-F/F WITH RB,SB Q OUT ONLY	-	11	6-286
F777NQP	JK-F/F WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	12	6-286
F781	JK-F/F (CB)	-	10	6-290
F781NB	JK-F/F (CB) QB OUT ONLY	-	9	6-290
F781NBP	JK-F/F (CB) QB OUT ONLY (X2 DRIVE)	-	10	6-290
F781NP	JK-F/F (CB) (X2 DRIVE)	-	12	6-290
F781NQ	JK-F/F (CB) Q OUT ONLY	-	9	6-290
F781NQP	JK-F/F (CB) Q OUT ONLY(X2 DRIVE)	-	10	6-290

Name	Function	I/O cells	int. cells	Page
F787	JK-F/F (CB) WITH RB,SB	-	12	6-292
F787NB	JK-F/F (CB) WITH RB,SB QB OUT ONLY	-	11	6-292
F787NBP	JK-F/F (CB) WITH RB,SB QB OUT ONLY (X2 DRIVE)	-	12	6-292
F787NP	JK-F/F (CB) WITH RB,SB (X2 DRIVE)	-	14	6-292
F787NQ	JK-F/F (CB) WITH RB,SB Q OUT ONLY	-	11	6-292
F787NQP	JK-F/F (CB) WITH RB,SB Q OUT ONLY (X2 DRIVE)	-	12	6-292
F791	T-F/F WITH DATA-HOLD R,S	-	12	6-276
F792	T-F/F (TB) WITH DATA-HOLD RB,SB	-	12	6-278
F901	4-BIT D-LATCH	-	20	6-200
F902	8-BIT D-LATCH	-	38	6-206
F911	4-BIT SHIFT REGISTER WITH R	-	33	6-354
F912	4-BIT SHIFT REGISTER WITH LOAD	-	35	6-356
F913	4-BIT SERIAL/PARALLEL SHIFT REGISTER WITH RB	-	39	6-350
F914	4-BIT SERIAL/PARALLEL SHIFT REGISTER	-	28	6-348
F922	4-BIT D-F/F WITH R	-	33	6-258
F924	4-BIT D-F/F	-	28	6-256
F961	4-BIT SYNCHRONOUS BINARY COUNTER WITH RB	-	54	6-358
F962	4-BIT SYNCHRONOUS BINARY UP COUNTER WITH RB	-	39	6-360
F971	4-BIT D-LATCH HIGH SPEED	-	20	6-204
F972	8-BIT D-LATCH HIGH SPEED	-	38	6-210
F981	2 TO 4 DECODER NEGATIVE OUTPUT WITH ENB	-	13	6-320
F982	3 TO 8 DECODER NEGATIVE OUTPUT WITH ENB	-	26	6-324
F985	4-BIT MAGNITUDE COMPARATOR	-	32	6-344
F9E6	DIGITAL PLL(25MHZ TO 50MHZ)	-	1900	5-6
F9E8	DIGITAL PLL(50MHZ TO 75MHZ)	-	1596	5-8
FC42	CLOCK TREE SYNTHESIS DRIVER	-	132	6-14
FC44	CLOCK TREE SYNTHESIS DRIVER	-	340	6-14
FC82	CLOCK TREE SYNTHESIS DRIVER	-	396	6-14
FC84	CLOCK TREE SYNTHESIS DRIVER	-	1020	6-14
FCK1	CLOCK DRIVER (LOW DRIVE)	-	40	6-10
FCK2	CLOCK DRIVER (LOW MIDDLE DRIVE)	-	80	6-10
FCK3	CLOCK DRIVER (MIDDLE DRIVE)	-	120	6-10
FCK4	CLOCK DRIVER (UPPER MIDDLE DRIVE)	-	160	6-10
FCK5	CLOCK DRIVER (HIGH DRIVE)	-	200	6-10
FCKA	CLOCK DRIVER SINGLE OUT (LOW DRIVE)	-	40	6-12
FCKB	CLOCK DRIVER SINGLE OUT (LOWEW MIDDLE DRIVE)	-	80	6-12
FCKC	CLOCK DRIVER SINGLE OUT (MIDDLE DRIVE)	-	120	6-12
FCKD	CLOCK DRIVER SINGLE OUT (UPPER MIDDLE DRIVE)	-	160	6-12
FCKE	CLOCK DRIVER SINGLE OUT (HIGH DRIVE)	-	200	6-12
FDA1	INPUT BUFFER WITH FAILSAFE 50kΩ PULL-DOWN	1	4	1-4
FDB1	INPUT BUFFER CLOCK DRIVER 50kΩ PULL-DOWN	1	24	1-2
FDE1	INPUT BUFFER WITH FAILSAFE SCHMITT 50kΩ PULL-DOWN	1	8	1-4
FDF1	INPUT BUFFER SCHMITT 50kΩ PULL-DOWN	1	8	2-2
FDG1	INPUT BUFFER CLOCK DRIVER 50kΩ PULL-DOWN	1	24	2-2
FDH1	INPUT BUFFER WITH FAILSAFE CLOCK DRIVER 50kΩ PULL-DOWN	1	24	1-4
FDS1	INPUT BUFFER SCHMITT 50kΩ PULL-DOWN	1	8	1-2
FDV1	INPUT BUFFER 50kΩ PULL-DOWN	1	4	2-2
FE01	LOW-NOISE OUTPUT BUFFER 9mA	1	4	1-10
FE02	LOW-NOISE OUTPUT BUFFER 12mA	1	4	1-10
FE03	LOW-NOISE OUTPUT BUFFER 18mA	1	4	1-10
FE04	LOW-NOISE OUTPUT BUFFER 6mA	1	4	1-10
FE06	LOW-NOISE OUTPUT BUFFER 24mA	1	4	1-10
FI01	INPUT BUFFER	1	4	1-2

Name	Function	I/O cells	int. cells	Page
FI0P	3V INPUT BUFFER REFERENCE CLOCK	1	3	5-2
FI0Q	5V INPUT BUFFER REFERENCE CLOCK	1	3	5-4
FIA1	INPUT BUFFER WITH FAILSAFE	1	4	1-4
FIB1	INPUT BUFFER CLOCK DRIVER	1	24	1-2
FID1	INPUT BUFFER 50kΩ PULL-DOWN	1	4	1-2
FIE1	INPUT BUFFER WITH FAILSAFE SCHMITT	1	8	1-4
FIF1	INPUT BUFFER SCHMITT	1	8	2-2
FIG1	INPUT BUFFER CLOCK DRIVER	1	24	2-2
FIH1	INPUT BUFFER WITH FAILSAFE CLOCK DRIVER	1	24	1-4
FIP1	GTL INPUT BUFFER FOR REFERENCE VOLTAGE	1	-	4-8
FIP3	P-ECL INPUT BUFFER FOR REFERENCE VOLTAGE	1	0	4-16
FIP4	P-ECL INPUT BUFFER FOR REFERENCE VOLTAGE	1	0	4-16
FIR1	GTL INPUT BUFFER WITH EN	1	8	4-6
FIS1	INPUT BUFFER SCHMITT	1	8	1-2
FIU1	INPUT BUFFER 50kΩ PULL-UP	1	4	1-2
FIV1	INPUT BUFFER	1	4	2-2
FIW1	INPUT BUFFER 5kΩ PULL-UP	1	4	1-2
FIX1	P-ECL INPUT BUFFER WITH EN	1	26	4-14
FIX2	P-ECL INPUT BUFFER WITH EN	1	26	4-14
FIXA	3V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL	1	24	4-2
FIZA	5V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL	1	24	4-4
FN13	INPUT BUFFER WITH EN(OR)	1	4	1-6
FN1335	INPUT BUFFER WITH EN(OR)	1	4	2-4
FN23	INPUT BUFFER WITH EN(OR) 50kΩ PULL-DOWN	1	4	1-6
FN2335	INPUT BUFFER WITH EN(OR) 50kΩ PULL-DOWN	1	4	2-4
FO01	OUTPUT BUFFER 9mA	1	4	1-8
FO02	OUTPUT BUFFER 12mA	1	4	1-8
FO03	OUTPUT BUFFER 18mA	1	8	1-8
FO04	OUTPUT BUFFER 6mA	1	4	1-8
FO06	OUTPUT BUFFER 24mA	1	8	1-8
FO09	OUTPUT BUFFER 3mA	1	4	1-8
FO0G	P-ECL OUTPUT BUFFER	1	4	4-18
FO21	HIGH SPEED OUTPUT BUFFER 9mA	1	4	1-12
FO22	HIGH SPEED OUTPUT BUFFER 12mA	1	4	1-12
FO23	HIGH SPEED OUTPUT BUFFER 18mA	1	8	1-12
FO24	HIGH SPEED OUTPUT BUFFER 6mA	1	4	1-12
FO26	HIGH SPEED OUTPUT BUFFER 24mA	1	8	1-12
FO29	HIGH SPEED OUTPUT BUFFER 3mA	1	4	1-12
FUB1	INPUT BUFFER CLOCK DRIVER 50kΩ PULL-UP	1	24	1-2
FUS1	INPUT BUFFER SCHMITT 50kΩ PULL-UP	1	8	1-2
FUXA	3V GTL/P-ECL INPUT BUFFER FOR ENABLE TERMINAL 50kΩ PULL-UP	1	24	4-2
FV01	TTL OUTPUT BUFFER 9mA	1	8	2-10
FV04	TTL OUTPUT BUFFER 6mA	1	4	2-10
FV09	TTL OUTPUT BUFFER 3mA	1	4	2-10
FV0A	TTL OUTPUT BUFFER 1mA	1	4	2-10
FV0B	TTL OUTPUT BUFFER 2mA	1	4	2-10
FW02	TTL LOW-NOISE OUTPUT BUFFER 12mA	1	4	2-12
FW03	TTL LOW-NOISE OUTPUT BUFFER 18mA	2	4	2-12
FW06	TTL LOW-NOISE OUTPUT BUFFER 24mA	2	4	2-12
FWB1	INPUT BUFFER CLOCK DRIVER 5kΩ PULL-UP	1	24	1-2
FWS1	INPUT BUFFER SCHMITT 5kΩ PULL-UP	1	8	1-2

Name	Function	I/O cells	int. cells	Page
FY01	CMOS OUTPUT BUFFER 9mA	1	24	2-6
FY02	CMOS OUTPUT BUFFER 12mA	1	24	2-6
FY03	CMOS OUTPUT BUFFER 18mA	2	24	2-6
FY04	CMOS OUTPUT BUFFER 6mA	1	20	2-6
FY06	CMOS OUTPUT BUFFER 24mA	2	24	2-6
FY09	CMOS OUTPUT BUFFER 3mA	1	20	2-6
FY11	TTL HIGH SPEED OUTPUT BUFFER 9mA	1	8	2-14
FY12	TTL HIGH SPEED OUTPUT BUFFER 12mA	1	8	2-14
FY13	TTL HIGH SPEED OUTPUT BUFFER 18mA	2	8	2-14
FY14	TTL HIGH SPEED OUTPUT BUFFER 6mA	1	4	2-14
FY16	TTL HIGH SPEED OUTPUT BUFFER 24mA	2	8	2-14
FY19	TTL HIGH SPEED OUTPUT BUFFER 3mA	1	4	2-14
FZ02	CMOS LOW-NOISE OUTPUT BUFFER 12mA	1	8	2-8
FZ03	CMOS LOW-NOISE OUTPUT BUFFER 18mA	2	8	2-8
FZ06	CMOS LOW-NOISE OUTPUT BUFFER 24mA	2	8	2-8
L101	INVERTER SINGLE OUT(LOW POWER)	-	1	6-6
L111	BUFFER SINGLE OUT(LOW POWER)	-	1	6-8
L202	2-INPUT NOR (LOW POWER)	-	1	6-20
L202N1	2-INPUT NOR 1-INPUT INVERTER (LOW POWER)	-	2	6-20
L203	3-INPUT NOR (LOW POWER)	-	2	6-22
L203N1	3-INPUT NOR 1-INPUT INVERTER (LOW POWER)	-	2	6-22
L203N2	3-INPUT NOR 2-INPUT INVERTER (LOW POWER)	-	3	6-22
L204	4-INPUT NOR (LOW POWER)	-	2	6-24
L204N1	4-INPUT NOR 1-INPUT INVERTER (LOW POWER)	-	3	6-24
L204N2	4-INPUT NOR 2-INPUT INVERTER (LOW POWER)	-	3	6-24
L205	5-INPUT NOR (LOW POWER)	-	4	6-28
L205N1	5-INPUT NOR 1-INPUT INVERTER (LOW POWER)	-	5	6-28
L205N2	5-INPUT NOR 2-INPUT INVERTER (LOW POWER)	-	5	6-28
L205N3	5-INPUT NOR 3-INPUT INVERTER (LOW POWER)	-	6	6-28
L212	2-INPUT OR (LOW POWER)	-	2	6-40
L213	3-INPUT OR (LOW POWER)	-	2	6-42
L214	4-INPUT OR (LOW POWER)	-	3	6-44
L214N1	4-INPUT OR 1-INPUT INVERTER (LOW POWER)	-	3	6-44
L215	5-INPUT OR (LOW POWER)	-	4	6-46
L215N1	5-INPUT OR 1-INPUT INVERTER (LOW POWER)	-	4	6-46
L302	2-INPUT NAND (LOW POWER)	-	1	6-58
L302N1	2-INPUT NAND 1-INPUT INVERTER (LOW POWER)	-	2	6-58
L303	3-INPUT NAND (LOW POWER)	-	2	6-60
L303N1	3-INPUT NAND 1-INPUT INVERTER (LOW POWER)	-	2	6-60
L303N2	3-INPUT NAND 2-INPUT INVERTER (LOW POWER)	-	3	6-60
L304	4-INPUT NAND (LOW POWER)	-	2	6-62
L304N1	4-INPUT NAND 1-INPUT INVERTER (LOW POWER)	-	3	6-62
L304N2	4-INPUT NAND 2-INPUT INVERTER (LOW POWER)	-	3	6-62
L305	5-INPUT NAND (LOW POWER)	-	3	6-66
L305N1	5-INPUT NAND 1-INPUT INVERTER (LOW POWER)	-	3	6-66
L305N2	5-INPUT NAND 2-INPUT INVERTER (LOW POWER)	-	4	6-66
L305N3	5-INPUT NAND 3-INPUT INVERTER (LOW POWER)	-	4	6-66
L306	6-INPUT NAND (LOW POWER)	-	3	6-70
L306N1	6-INPUT NAND 1-INPUT INVERTER (LOW POWER)	-	4	6-70
L306N2	6-INPUT NAND 2-INPUT INVERTER (LOW POWER)	-	4	6-70
L306N3	6-INPUT NAND 3-INPUT INVERTER (LOW POWER)	-	5	6-70
L312	2-INPUT AND (LOW POWER)	-	2	6-78
L313	3-INPUT AND (LOW POWER)	-	2	6-80

Name	Function	I/O cells	int. cells	Page
L432NB	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-144
L432NC	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-144
L432ND	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-144
L432NE	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-144
L432NF	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-144
L432NG	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-144
L432NH	1-1-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-144
L433	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	2	6-150
L433NA	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-150
L433NB	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-150
L433NC	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-150
L433ND	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-150
L433NE	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-150
L433NF	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-150
L433NG	1-3-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-150
L434	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	2	6-156
L434NA	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-156
L434NB	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-156
L434NC	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-156
L434ND	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-156
L434NE	2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	4	6-156
L435	2-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-160
L436	3-3-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-162
L437	1-2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-164
L438	2-2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	3	6-166
L442	4-4-INPUT AND-OR-INVERTER (LOW POWER)	-	4	6-136
L454	2-2-2-2-INPUT OR-AND-INVERTER (LOW POWER)	-	5	6-168
L462	1-2-3-INPUT AND-OR-INVERTER (LOW POWER)	-	3	6-138
L511	2-INPUT EXCLUSIVE OR (LOW POWER)	-	3	6-98
L512	2-INPUT EXCLUSIVE NOR (LOW POWER)	-	3	6-102
L516	3-INPUT EXCLUSIVE OR (LOW POWER)	-	6	6-100
L517	3-INPUT EXCLUSIVE NOR (LOW POWER)	-	6	6-104
L560	2 TO 4 DECODER POSITIVE OUTPUT (LOW POWER)	-	6	6-320
L561	2 TO 4 DECODER NEGATIVE OUTPUT (LOW POWER)	-	6	6-320
L571	2 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB (LOW POWER)	-	4	6-296
L572	QUAD 2 TO 1 MULTIPLEXER POSITIVE OUTPUT WITH ENB (LOW POWER)	-	10	6-298
L601	D-LATCH Q OUT ONLY (LOW POWER)	-	3	6-170
L602	D-LATCH WITH R Q OUT ONLY (LOW POWER)	-	4	6-176
L603	D-LATCH WITH RB Q OUT ONLY (LOW POWER)	-	4	6-182
L604	D-LATCH (GB) Q OUT ONLY (LOW POWER)	-	3	6-190
L605	D-LATCH (GB) WITH RB Q OUT ONLY (LOW POWER)	-	4	6-196
L606	D-LATCH WITH SB (LOW POWER)	-	4	6-188
L611	D-F/F Q OUT ONLY (LOW POWER)	-	5	6-216
L614	D-F/F WITH R,S Q OUT ONLY (LOW POWER)	-	7	6-226
L617	D-F/F WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-238
L631	D-F/F (CB) Q OUT ONLY (LOW POWER)	-	5	6-242
L637	D-F/F (CB) WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-252
L714	T-F/F WITH R,S Q OUT ONLY (LOW POWER)	-	7	6-264
L717	T-F/F WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-268
L737	T-F/F (TB) WITH RB,SB Q OUT ONLY (LOW POWER)	-	7	6-272
L901	4-BIT D-LATCH Q OUT ONLY (LOW POWER)	-	10	6-200
L902	8-BIT D-LATCH Q OUT ONLY (LOW POWER)	-	18	6-206
L911	4-BIT SHIFT REGISTER WITH R Q OUT ONLY (LOW POWER)	-	23	6-354

Name	Function	I/O cells	int. cells	Page
L912	4-BIT SHIFT REGISTER WITH LOAD Q OUT ONLY (LOW POWER)	-	23	6-356
L913	4-BIT SERIAL/PARALLEL SHIFT REGISTER WITH RB Q OUT ONLY (LOW POWE	-	27	6-350
L914	4-BIT SERIAL/PARALLEL SHIFT REGISTER (LOW POWER)	-	18	6-348
L922	4-BIT D-F/F WITH R Q OUT ONLY (LOW POWER)	-	23	6-258
L924	4-BIT D-F/F Q OUT ONLY (LOW POWER)	-	18	6-256
L981	2 TO 4 DECODER NEGATIVE OUTPUT WITH ENB (LOW POWER)	-	8	6-320
L982	3 TO 8 DECODER NEGATIVE OUTPUT WITH ENB (LOW POWER)	-	21	6-324
OSF1	FEEDBACK RESISTOR FOR OSCILLATOR	1	0	3-14
OSF3	FEEDBACK RESISTOR FOR OSCILLATOR FOR ENABLE	1	2	3-16
OSI1	OSCILLATOR INPUT BUFFER	1	0	3-2
OSI2	OSCILLATOR INPUT BUFFER FOR ENABLE	1	0	3-4
OSO1	OSCILLATOR OUTPUT BUFFER INTERNAL FEEDBACK RESISTOR	1	4	3-6
OSO3	OSCILLATOR OUTPUT BUFFER FOR OSF TYPE	1	4	3-8
OSO7	OSCILLATOR OUTPUT BUFFER FOR ENABLE TYPE	1	6	3-10
OSO9	OSCILLATOR OUTPUT BUFFER EXTERNAL FEEDBACK RESISTOR	1	4	3-12
S000	D-F/F WITH R,S,2 TO 1 SELECTOR	-	12	6-362
S002	D-F/F WITH 2 TO 1 SELECTOR	-	10	6-364
S050	D-F/F WITH R,S,HOLD,2 TO 1 SELECTOR	-	14	6-366
S052	D-F/F WITH HOLD,2 TO 1 SELECTOR	-	13	6-368
S100	JK-F/F WITH R,S,D-F/F FUNCTION	-	14	6-370
S102	JK-F/F WITH D-F/F FUNCTION	-	12	6-372
S150	JK-F/F WITH R,S,HOLD,D-F/F FUNCTION	-	17	6-374
S152	JK-F/F WITH HOLD,D-F/F FUNCTION	-	15	6-376
S201	D-LATCH WITH R,D-F/F FUNCTION	-	12	6-378
S202	D-LATCH WITH D-F/F FUNCTION	-	11	6-380
S204	D-LATCH WITH D-F/F FUNCTION HIGH SPEED	-	11	6-380
S301	D-LATCH WITH R,SPECIAL FUNCTION	-	8	6-382
S302	D-LATCH WITH SPECIAL FUNCTION	-	7	6-384
S303	D-LATCH WITH SPECIAL FUNCTION HIGH SPEED	-	7	6-384
S999	2 TO 1 DATA SELECTOR	-	4	6-386

[MEMO]

お問い合わせ先

【技術的なお問い合わせ先】

ＮＥＣ半導体テクニカルホットライン（インフォメーションセンター）
（電話：午前 9:00～12:00，午後 1:00～5:00）

電　話　：044-548-8899
FAX　：044-548-7900
E-mail　：s-info@saed.tmg.nec.co.jp

【営業関係お問い合わせ先】

半導体第一販売事業部 半導体第二販売事業部 半導体第三販売事業部	〒108-8001	東京都港区芝５－７－１　（日本電気本社ビル）	(03)3454-1111
中部支社	半導体第一販売部 半導体第二販売部	〒460-8525	愛知県名古屋市中区錦１－17－１　（日本電気中部ビル）	(052)222-2170 (052)222-2190
関西支社	半導体第一販売部 半導体第二販売部 半導体第三販売部	〒540-8551	大阪府大阪市中央区城見１－４－24　（日本電気関西ビル）	(06) 945-3178 (06) 945-3200 (06) 945-3208

北海道支社	札　幌	(011)251-5599	宇都宮支店	宇都宮	(028)621-2281	北陸支社	金　沢	(076)232-7303
東北支社	仙　台	(022)267-8740	小山支店	小　山	(0285)24-5011	京都支社	京　都	(075)344-7824
岩手支店	盛　岡	(019)651-4344	甲府支店	甲　府	(0552)24-4141	神戸支社	神　戸	(078)333-3854
郡山支店	郡　山	(0249)23-5511	長野支社	松　本	(0263)35-1662	中国支社	広　島	(082)242-5504
いわき支店	いわき	(0246)21-5511	静岡支社	静　岡	(054)254-4794	鳥取支店	鳥　取	(0857)27-5311
長岡支店	長　岡	(0258)36-2155	立川支社	立　川	(042)526-5981,6167	岡山支店	岡　山	(086)225-4455
水戸支店	水　戸	(029)226-1717	埼玉支社	大　宮	(048)649-1415	松山支店	松　山	(089)945-4149
土浦支店	土　浦	(0298)23-6161	千葉支社	千　葉	(043)238-8116	九州支社	福　岡	(092)261-2806
群馬支店	高　崎	(027)326-1255	神奈川支社	横　浜	(045)682-4524			
太田支店	太　田	(0276)46-4011	三重支店	津	(059)225-7341			

アンケート記入のお願い

お手数ですが，このドキュメントに対するご意見をお寄せください。今後のドキュメント作成の参考にさせていただきます。

［ドキュメント名］CMOS-8L Family Block Library Ver.5.0 User's Manual

（A12213XJ5V0UM00（5th edition））

［お名前など］（さしつかえのない範囲で）

御社名（学校名，その他）（　　）
ご住所（　　）
お電話番号（　　）
お仕事の内容（　　）
お名前（　　）

1. ご評価（各欄に○をご記入ください）

項　　目	大変良い	良　い	普　通	悪　い	大変悪い
全体の構成					
説明内容					
用語解説					
調べやすさ					
デザイン，字の大きさなど					
その他（　　）					
（　　）					

2. わかりやすい所（第　章，第　章，第　章，第　章，その他　　）

理由［　　］

3. わかりにくい所（第　章，第　章，第　章，第　章，その他　　）

理由［　　］

4. ご意見，ご要望

5. このドキュメントをお届けしたのは

NEC 販売員，特約店販売員，NEC 半導体ソリューション技術本部員，
その他（　　）

ご協力ありがとうございました。
下記あてに FAX で送信いただくか，最寄りの販売員にコピーをお渡しください。

NEC 半導体テクニカルホットライン
FAX：（044）548-7900

キリトリ

NEC

Facsimile Message

From:

Name

Company

Tel. FAX

Address

Although NEC has taken all possible steps to ensure that the documentation supplied to our customers is complete, bug free and up-to-date, we readily accept that errors may occur. Despite all the care and precautions we've taken, you may encounter problems in the documentation. Please complete this form whenever you'd like to report errors or suggest improvements to us.

Thank you for your kind support.

North America
NEC Electronics Inc.
Corporate Communications Dept.
Fax: 1-800-729-9288
1-408-588-6130

Europe
NEC Electronics (Europe) GmbH
Technical Documentation Dept.
Fax: +49-211-6503-274

South America
NEC do Brasil S.A.
Fax: +55-11-6465-6829

Hong Kong, Philippines, Oceania
NEC Electronics Hong Kong Ltd.
Fax: +852-2886-9022/9044

Korea
NEC Electronics Hong Kong Ltd.
Seoul Branch
Fax: 02-528-4411

Taiwan
NEC Electronics Taiwan Ltd.
Fax: 02-2719-5951

Asian Nations except Philippines
NEC Electronics Singapore Pte. Ltd.
Fax: +65-250-3583

Japan
NEC Semiconductor Technical Hotline
Fax: 044-548-7900

I would like to report the following error/make the following suggestion:

Document title: _____

Document number: _____ Page number: _____

If possible, please fax the referenced page or drawing.

Document Rating	Excellent	Good	Acceptable	Poor
Clarity	❑	❑	❑	❑
Technical Accuracy	❑	❑	❑	❑
Organization	❑	❑	❑	❑