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April 1st, 2010
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USER'S MANUAL

RENESAS

Phase-out/Discontinued

AS17006 DEVICE FILE

PC-9800 SERIES(MS-DOS™)BASED

IBM PC/AT™(PC DOS™)BASED

VERSION 1

Document No. EEU-1450
(O. D. No. EEU-831)
Date Published October 1993 P
Printed in Japan

USER'S MANUAL

NEC

AS17006 DEVICE FILE

PC-9800 SERIES(MS-DOS™)BASED

IBM PC/AT™(PC DOS™)BASED

VERSION 1

Phase-out/Discontinued

FOREWORD

The AS17006 is a Device File is used together with the AS17K assemble to enable uPD17006 programs to be assembled.

During assembly, the AS17006 provides uPD17006 program memory capacity, data memory capacity, usable instructions, and reserved symbols.

Please refer to the AS17K User's Manual (EEU-603) for the operation procedure for the AS17K assembler and the AS17006 Device File.

CONTENTS

CHAPTER 1. DEVICE INFORMATION

The AS17006 Device File provides the following uPD17006 related information during assembly:

(1) Program memory (ROM) capacity

- Segment 0: 8192 x 16 bits (0000H to 1FFFH)
- Segment 1: 3840 x 16 bits (0000H to 0EFFH)

Total	12032 x 16 bits

(2) Data memory (RAM) capacity

896 x 4 bits (BANK0 to BANK7)

(3) Usable instructions

See Chapter 2 "uPD17006 INSTRUCTION SET".

(4) Register files, port registers and peripheral register read/write information
See Chapter 3 "RESERVED SYMBOLS".

(5) Reserved symbols
See Chapter 3 "RESERVED SYMBOLS".

CHAPTER 2. uPD17006 INSTRUCTION SET

2.1 OUTLINE OF INSTRUCTION SET

b_{14} to b_{11} \ b_{15}		0	1
BIN	HEX		
0000	0	ADD r, m	ADD m, #i
0001	1	SUB r, m	SUB m, #i
0010	2	ADDC r, m	ADDC m, #i
0011	3	SUBC r, m	SUBC m, #i
0100	4	AND r, m	AND m, #i
0101	5	XOR r, m	XOR m, #i
0110	6	OR r, m	OR m, #i
0111	7	INC AR INC IX MOVT DBF, @AR BR @AR CALL @AR SYSCAL entry RET RETSK EI DI RETI PUSH AR POP AR GET DBF, p PUT p, DBF PEEK WR, rf POKE rf, WR RORC r STOP s HALT h NOP	
1000	8	LD r, m	ST m, r

(to be continued)

(cont'd)

b_{14} to b_{11} \ b_{15}		0	1
BIN	HEX		
1001	9	SKE m, #i	SKGE m, #i
1010	A	MOV @r,m	MOV m, @i
1011	B	SKNE m, #i	SKLT m, #i
1100	C	BR addr (page 0)	CALL addr (page 0)
1101	D	BR addr (page 1)	MOV m, #i
1110	E	BR addr (page 2)	SKT m, #n
1111	F	BR addr (page 3)	SKF m, #n

2.2 LEGEND

AR	:	Address register
ASR	:	Address stack register indicated by stack pointer
addr	:	Program memory address (low-order 11 bits)
BANK	:	Bank register
(BANK)	:	Bank register contents
b	:	Borrow
CY	:	Carry flag
c	:	Carry
DBF	:	Data buffer
entry	:	Program memory address (bits b_{10} to b_8, b_3 to b_0)
h	:	Halt release condition (h = 0 to 3, 8 to 0FH)
INTEF	:	Interrupt enable flag
INTSK	:	Interrupt stack register
IX	:	Index register
(IX)	:	Index register value
IXE	:	Index enable flag
i	:	Immediate data

M	:	Data memory address When IXE = 0, M = [(BANK), m_H, m_L] When IXE = 1, M = [(BANK), m_H, m_L] OR (IX)
m	:	Data memory address excluding bank indicated by [m_H, m_L]
m_H	:	Data memory row address (3 bits)
m_L	:	Data memory column address (4 bits)
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
n	:	Bit position (4 bits)
PC	:	Program counter
PE	:	Peripheral register
p	:	Peripheral register address
p_H	:	Peripheral register address (higher to order 3 bits)
p_L	:	Peripheral register address (low to order 4 bits)
R	:	General register address R = [(RP_H), (RP_L), r]
r	:	General register column address (4 bits)
RP	:	General register pointer

RF	:	Register file indicated by rf.
rf	:	Register file address indicated by [rf_H, rf_L]
rf_H	:	Register file address (higher to order 3 bits)
rf_L	:	Register file address (low to order 4 bits)
$(ROM)_{SGR,\ PC}$	:	Contents of ROM of address specified by SGR and PC.
SGR	:	Segment register
SP	:	Stack pointer
s	:	Stop release condition (s = 4)
WR	:	Window register
[ ]	:	Data memory or register address
( )	:	Data memory or register value

2.3 LIST OF INSTRUCTIONS

Instruction Grope	Mnemonic	Operands	Operation	Machine Code			
				Op Code	Operands		
Addition		r,m	(R)←(R)+(M)	00000	m_H	m_L	r
	ADD	m,#i	(M)←(M)+i	10000	m_H	m_L	i
	ADDC	r,m	(R)←(R)+(M)+(CY)	00010	m_H	m_L	r
		m,#i	(M)←(M)+i+(CY)	10010	m_H	m_L	i
	INC	AR	(AR)←(AR)+1	00111	000	1001	0000
		IX	(IX)←(IX)+1	00111	000	1000	0000
Subtraction	SUB	r,m	(R)←(R)-(M)	00001	m_H	m_L	r
		r,#i	(M)←(M)-i	10001	m_H	m_L	i
	SUBC	r,m	(R)←(R)-(M)-(CY)	00011	m_H	m_L	r
		m,#i	(M)←(M)-i-(CY)	10011	m_H	m_L	i
Comparison	SKE	m,#i	(M)-i,skip if zero	01001	m_H	m_L	i
	SKGE	m,#i	(M)-i,skip if not borrow	11001	m_H	m_L	i
	SKLT	m,#i	(M)-i,skip if borrow	11011	m_H	m_L	i
	SKNE	m,#i	(M)-i,skip if not zero	01011	m_H	m_L	i
Logical Operation	AND	m,#i	(M)←(M) AND i	10100	m_H	m_L	i
		r,m	(R)←(R) AND (M)	00100	m_H	m_L	r
	OR	m,#i	(M)←(M) OR i	10110	m_H	m_L	i
		r,m	(R)←(R) OR (M)	00110	m_H	m_L	r
	XOR	m,#i	(M)←(M) XOR i	10101	m_H	m_L	i
		r,m	(R)←(R) XOR (M)	00101	m_H	m_L	r

(to be continude)

(cont'd)

Instruction Grope	Mnemonic	Operands	Operation	Machine Code			
				Op Code	Operands		
Transfer	LD	r,m	(R)←(M)	01000	m_H	m_L	r
	ST	m,r	(M)←(R)	11000	m_H	m_L	r
	MOV	@r,m	if MPE=1:[(MP),(R)]←(M) if MPE=0:[(m_H,(R)] ←(M)	01010	m_H	m_L	r
		m,@r	if MPE=1: (M)←[(MP),(R)] if MPE=0: (M)←[(m_H),(R)]	11010	m_H	m_L	r
		m,#i	(M)←i	11101	m_H	m_L	i
	MOVI*	DBF,@AR	(ASR)←(SGR,PC), (SGR,PC)←(AR), (DBF)←$(ROM)_{SGR,PC}$, (SGR,PC)←(ASR)	00111	000	0001	0000
	PUSH	AR	(SP)←(SP)-1,(ASR)←(AR)	00111	000	1101	0000
	POP	AR	(AR)←(ASR),(SP)←(SP)+1	00111	000	1100	0000
	PEEK	WR,rf	(WR)←(RF)	00111	rf_H	0011	rf_L
	POKE	rf,WR	(RF)←(WR)	00111	rf_H	0010	rf_L
	GET	DBF,p	(DBF)←(PE)	00111	P_H	1011	P_L
	PUT	p,DBF	(PE)←(DBF)	00111	P_H	1010	P_L
Decision	SKT	m,#n	if $(M)_n$=all"1",then skip	11110	m_H	m_L	n
	SKF	m,#n	if $(M)_n$=all"0",then skip	11111	m_H	m_L	n
Branch	BR	addr	(PC)←addr & $(PC)_{b12}$, b11 ←00	01100	addr (lower-order 11 bits)		
			(PC)←addr & $(PC)_{b12}$, b11←01	01101			
			(PC)←addr & $(PC)_{b12}$, b11←10	01110			
			(PC)←addr & $(PC)_{b12}$, b11←11	00111			
		@AR	(SGR,PC)←(AR)	00111	000	0100	0000

(to be continude)

(cont'd)

Instruction Grope	Mnemonic	Operands	Operation	Machine Code			
				Op Code	Operands		
Sift	RORC	r	$\lfloor (CY) \rightarrow (R)_{b3} \rightarrow (R)_{b2} \rightarrow (R)_{b1} \rightarrow (R)_{b0} \rfloor$	00111	000	0111	r
Subroutine	CALL	addr	$\begin{matrix}(SP)\\(PC)\end{matrix} \leftarrow (SP)-1,\ (ASR) \leftarrow ((PC)+1),\ (PC)_{b11} \leftarrow 0,\ (PC)_{b10 \text{ to } b0} \leftarrow addr$	11100	addr (low-order 11 bits)		
		@AR	(SP)←(SP)-1, (ASR)←((PC)+1), (SGR,PC)←(AR)	00111	000	0101	0000
	SYSCAL	entry	(SP)←(SP)-1, (ASR)←((PC)+1), PB←0,PC(10-8)←B,PC(7-4)←0 PC(3-0)←E B=entry (6-4),E=entry (3-0)	00111	B	0000	E
	RET		(SGR,PC)←(ASR),(SP)←(SP)+1	00111	000	1110	0000
	RETSK		(SGR,PC)←(ASR),(SP)←(SP)+1 and skip	00111	001	1110	0000
	RET1		(SGR,PC)←(ASR),(BANK) (IXE)←(INTSK), (SP)←(SP)+1	00111	100	1110	0000
Interrupt	EI		INTEF←1	00111	000	1111	0000
	DI		INTEF←0	00111	001	1111	0000
Others	STOP	S	stop clock if CE=low	00111	010	1111	s
	HALT	h	halt	00111	011	1111	h
	NOP		Not operation	00111	100	1111	0000

* Two machine cycles (equivalent to 2 instructions) are needed to execute a MOVT instruction. When the instruction is executed, one stack level is used temprorarily.

2.4 ASSEMBLER (AS17K) INTRINSIC MACRO INSTRUCTIONS

Legend

flag : 1 of flag1 to flagn
flag1 to flagn: Reserved word or symbol-defined flag name
n : Number
< > : Omission possible

	Mnemonic	Operands	n	Operation
Built-in macro instruction	SKTn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag1) to (flagn) = all "1", then skip
	SKFn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag1) to (flagn) = all "0", then skip
	SETn	flag1, ... flagn	$1 \leqq n \leqq 4$	(flag1) to (flagn) ← 1
	CLRn	flag1, ... flagn	$1 \leqq n \leqq 4$	(flag1) to (flagn) ← 0
	NOTn	flag1, ... flagn	$1 \leqq n \leqq 4$	if (flag) = "0", then (flag) ← 1, if (flag) = "1", then (flag) ← 0
	INITFLG	<NOT> flag1, ... <NOT> flagn	n = 4	if description = NOT flag, (flag) ← 0 if description = flag, (flag) ← 1
	BANKn		$0 \leqq n \leqq 7$	(BANK) ← n

CHAPTER 3. RESERVED SYMBOLS

Symbols defined by the uPD17006 device file are shown on the following pages.

The defined symbols are as follows :

- System registers
- Data buffers
- Port registers
- Register files (control registers)
- Peripheral registers

3.1 SYSTEM REGISTERS

Symbol Name	Attribute	Value	R/W	Description
AR3	MEM	0.74H	R/W	Address register bits 15 to 12
AR2	MEM	0.75H	R/W	Address register bits 11 to 8
AR1	MEM	0.76H	R/W	Address register bits 7 to 4
ARO	MEM	0.77H	R/W	Address register bits 3 to 0
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register bits 11 to 8
MPH	MEM	0.7AH	R/W	Memory pointer bits 7 to 4
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register bits 7 to 4
MPL	MEM	0.7BH	R/W	Memory pointer bits 3 to 0
IXL	MEM	0.7CH	R/W	Index register bits 3 to 0
RPH	MEM	0.7DH	R/W	Register pointer bits 7 to 4
RPL	MEM	0.7EH	R/W	Register pointer bits 3 to 0
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD operation flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

3.2 DATA BUFFERS

Symbol Name	Attribute	Value	R/W	Description
DBF3	MEM	0.0CH	R/W	Data buffer bits bits 15 to 12
DBF2	MEM	0.0DH	R/W	Data buffer bits bits 11 to 8
DBF1	MEM	0.0EH	R/W	Data buffer bits bits 7 to 4
DBF0	MEM	0.0FH	R/W	Data buffer bits bits 3 to 0

3.3 PORT REGISTERS

Symbol Name	Attribute	Value	R/W	Description
POA3	FLG	0.70H.3	R/W	Port OA bit 3
POA2	FLG	0.70H.2	R/W	Port OA bit 2
POA1	FLG	0.70H.1	R/W	Port OA bit 1
POA0	FLG	0.70H.0	R/W	Port OA bit 0
POB3	FLG	0.71H.3	R/W	Port OB bit 3
POB2	FLG	0.71H.2	R/W	Port OB bit 2
POB1	FLG	0.71H.1	R/W	Port OB bit 1
POB0	FLG	0.71H.0	R/W	Port OB bit 0
POC3	FLG	0.72H.3	R/W	Port OC bit 3
POC2	FLG	0.72H.2	R/W	Port OC bit 2
POC1	FLG	0.72H.1	R/W	Port OC bit 1
POC0	FLG	0.72H.0	R/W	Port OC bit 0
POD3	FLG	0.73H.3	R/W	Port OD bit 3
POD2	FLG	0.73H.2	R/W	Port OD bit 2
POD1	FLG	0.73H.1	R/W	Port OD bit 1
POD0	FLG	0.73H.0	R/W	Port OD bit 0
P1A3	FLG	1.70H.3	R/W	Port 1A bit 3
P1A2	FLG	1.70H.2	R/W	Port 1A bit 2
P1A1	FLG	1.70H.1	R/W	Port 1A bit 1
P1A0	FLG	1.70H.0	R/W	Port 1A bit 0
P1B3	FLG	1.71H.3	R/W	Port 1B bit 3
P1B2	FLG	1.71H.2	R/W	Port 1B bit 2
P1B1	FLG	1.71H.1	R/W	Port 1B bit 1
P1B0	FLG	1.71H.0	R/W	Port 1B bit 0

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
P1C3	FLG	1.72H.3	R/W	Port 1C bit 3
P1C2	FLG	1.72H.2	R/W	Port 1C bit 2
P1D3	FLG	1.73H.3	R/W	Port 1D bit 3
P1D2	FLG	1.73H.2	R/W	Port 1D bit 2
P1D1	FLG	1.73H.1	R/W	Port 1D bit 1
P1D0	FLG	1.73H.0	R/W	Port 1D bit 0
P2A3	FLG	2.70H.3	R/W	Port 2A bit 3
P2A2	FLG	2.70H.2	R/W	Port 2A bit 2
P2A1	FLG	2.70H.1	R/W	Port 2A bit 1
P2A0	FLG	2.70H.0	R/W	Port 2A bit 0
P2B3	FLG	2.71H.3	R/W	Port 2B bit 3
P2B2	FLG	2.71H.2	R/W	Port 2B bit 2
P2B1	FLG	2.71H.1	R/W	Port 2B bit 1
P2B0	FLG	2.71H.0	R/W	Port 2B bit 0
P2C3	FLG	2.72H.3	R/W	Port 2C bit 3
P2C2	FLG	2.72H.2	R/W	Port 2C bit 2
P2C1	FLG	2.72H.1	R/W	Port 2C bit 1
P2C0	FLG	2.72H.0	R/W	Port 2C bit 0
P2D3	FLG	2.73H.3	R/W	Port 2D bit 3
P2D2	FLG	2.73H.2	R/W	Port 2D bit 2
P2D1	FLG	2.73H.1	R/W	Port 2D bit 1
P2D0	FLG	2.73H.0	R/W	Port 2D bit 0

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
P3A3	FLG	3.70H.3	R/W	Port 3A bit 3
P3A2	FLG	3.70H.2	R/W	Port 3A bit 2
P3A1	FLG	3.70H.1	R/W	Port 3A bit 1
P3A0	FLG	3.70H.0	R/W	Port 3A bit 0
P3B3	FLG	3.71H.3	R/W	Port 3B bit 3
P3B2	FLG	3.71H.2	R/W	Port 3B bit 2
P3B1	FLG	3.71H.1	R/W	Port 3B bit 1
P3B0	FLG	3.71H.0	R/W	Port 3B bit 0
P3C3	FLG	3.72H.3	R/W	Port 3C bit 3
P3C2	FLG	3.72H.2	R/W	Port 3C bit 2
P3C1	FLG	3.72H.1	R/W	Port 3C bit 1
P3C0	FLG	3.72H.0	R/W	Port 3C bit 0
P3D3	FLG	3.73H.3	R/W	Port 3D bit 3
P4A3	FLG	4.70H.3	R/W	Port 4A bit 3
P4A2	FLG	4.70H.2	R/W	Port 4A bit 2

3.4 REGISTER FILES (CONTROL REGISTERS)

Symbol Name	Attribute	Value	R/W	Description
SP	MEM	0.81H	R/W	Stack pointer
SIO1TS	FLG	0.82H.3	R/W	SIO1 start flag
SIO1HIZ	FLG	0.82H.2	R/W	SIO1/port 1 select flag
SIO1CK1	FLG	0.82H.1	R/W	SIO1 clock select flag
SIO1CK0	FLG	0.82H.0	R/W	SIO1 clock select flag
TM3EN	FLG	0.83H.3	R/W	Timer 3 enable flag
TM3RES	FLG	0.83H.2	R/W	Timer 3 reset flag
TM3RPT	FLG	0.83H.1	R/W	Timer 3 count mode select flag
TM3SEL	FLG	0.83H.0	R/W	Timer 3 select flag
IFCGOSTT	FLG	0.84H.0	R	IF counter gate status flag
PLLUL	FLG	0.85H.0	R	PLL unlock time select flag
CE	FLG	0.87H.0	R	CE pin status flag
SIO0CH	FLG	0.88H.3	R/W	SIO0 channel select flag
SB	FLG	0.88H.2	R/W	SIO0 mode select flag
SIO0MS	FLG	0.88H.1	R/W	SIO0 clock mode select flag
SIO0TX	FLG	0.88H.0	R/W	SIO0 TX/RX select flag
TM2EN	FLG	0.89H.3	R/W	Timer 2 enable flag
TM2RES	FLG	0.89H.2	R/W	Timer 2 reset flag
TM2CK1	FLG	0.89H.1	R/W	Timer 2 source clock selection flag
TM2CK0	FLG	0.89H.0	R/W	Timer 2 source clock selection flag
TM1GCMAN	FLG	0.8AH.3	R/W	Timer 1 gate manual close selection flag
TM1GOAUT	FLG	0.8AH.2	R/W	Timer 1 gate auto open selection flag

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
TM1EN	FLG	0.8AH.1	R/W	Timer 1 enable flag
TM1RES	FLG	0.8AH.0	R/W	Timer 1 reset flag
TMOEN	FLG	0.8BH.3	R/W	Timer 0 enable flag
TMOOVF	FLG	0.8BH.2	R/W	Timer 0 overflow detection flag
TMORES	FLG	0.8BH.1	R/W	Timer 0 reset flag
TMOCK	FLG	0.8BH.0	R/W	Timer 0 source clock selection flag
DBFSP	MEM	0.90H	R	DBF register stack pointer
SYSRSP	MEM	0.91H	R	System register stack pointer
IFCMD1	FLG	0.92H.3	R/W	IF counter mode select flag
IFCMDO	FLG	0.92H.2	R/W	IF counter mode select flag
IFCCK1	FLG	0.92H.1	R/W	IF counter clock select flag
IFCCKO	FLG	0.92H.0	R/W	IF counter clock select flag
PWM2SEL	FLG	0.93H.3	R/W	PWM2/P1B3 select flag
PWM1SEL	FLG	0.93H.2	R/W	PWM1/P1B2 select flag
PWMOSEL	FLG	0.93H.0	R/W	PWMO/P1B1 select flag
CGPSEL	FLG	0.93H.0	R/W	CGP/P1BO select flag
TM1CK3	FLG	0.94H.3	R/W	Timer 1 source clock selection flag (dummy)
TM1CK2	FLG	0.94H.2	R/W	Timer 1 source clock selection flag (dummy)
TM1CK1	FLG	0.94H.1	R/W	Timer 1 source clock selection flag
TM1CKO	FLG	0.94H.0	R/W	Timer 1 source clock selection flag
TM1OVF	FLG	0.95H.0	R	Timer 1 overflow detection flag

Remarks: Dummy is "0".

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
TM1INSEL	FLG	0.96H.3	R/W	Timer 1 event counter select flag
TM1GOSEL	FLG	0.96H.2	R/W	Timer 1 gate input terminal selection flag
TM1GCEG	FLG	0.96H.1	R/W	Timer 1 gate close edge selection flag
TM1GOEG	FLG	0.96H.0	R/W	Timer 1 gate open edge selection flag
BTMOCY	FLG	0.97H.0	R	Basic timer 0 carry flag
SBACK	FLG	0.98H.3	R/W	SIO acknowledge flag
SIOONWT	FLG	0.98H.2	R/W	SIO0 not wait flag
SIOOWRQ1	FLG	0.98H.1	R/W	SIO0 wait mode flag
SIOOWRQ0	FLG	0.98H.0	R/W	SIO0 wait mode flag
SIOOWSTT	FLG	0.99H.0	R	SIO0 wait status judge flag
ADCSTRT	FLG	0.9AH.0	W	A/D converter start flag
ADCSOFT	FLG	0.9BH.3	R/W	A/D converter compare control
ADCCMP	FLG	0.9BH.1	R/W	A/D converter compare output
ADCEND	FLG	0.9BH.0	R/W	A/D converter compare end flag
ADCCH3	FLG	0.9CH.3	R/W	A/D converter channel select flag (dummy)
ADCCH2	FLG	0.9CH.2	R/W	A/D converter channel select flag
ADCCH1	FLG	0.9CH.1	R/W	A/D converter channel select flag
ADCCH0	FLG	0.9CH.0	R/W	A/D converter channel select flag

Remarks: Dummy is "0".

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
IEGGRP1	FLG	0.9EH.3	R/W	Interrupt group 1 edge detection selection flag
SIOOTMG	FLG	0.9FH.1	R/W	SIOO interrupt timing selection flag
IEG1	FLG	0.9FH.2	R/W	INT1 pin edge detection selection flag
IEGTMO	FLG	0.9FH.1	R/W	Timer 0 edge detection selection flag
IEGO	FLG	0.9FH.0	R/W	INTO pin edge detection selection flag
PLLEOBST	FLG	0.0AOH.0	R/W	PLL error out booster selection flag
PLLMD3	FLG	0.0A1H.3	R/W	PLL band mode select flag (dummy)
PLLMD2	FLG	0.0A1H.2	R/W	PLL band mode select flag (dummy)
PLLMD1	FLG	0.0A1H.1	R/W	PLL band mode select flag
PLLMDO	FLG	0.0A1H.0	R/W	PLL band mode select flag
IFCSTRT	FLG	0.0A3H.1	R/W	IF counter start flag
IFCRES	FLG	0.0A3H.0	R/W	IF counter reset flag
TM1GOSTT	FLG	0.0A4H.0	R	Timer 1 gate status flag
TM1MSEL	FLG	0.0A5H.1	R/W	Timer 1 mode select flag
TM1RPT	FLG	0.0A5H.0	R/W	Timer 1 repeat mode select flag
P3BGIO	FLG	0.0A6H.1	R/W	Port 3B group I/O select flag
P3AGIO	FLG	0.0A6H.1	R/W	Port 3A group I/O select flag
P2DGIO	FLG	0.0A7H.3	R/W	Port 2D group I/O select flag
P2CGIO	FLG	0.0A7H.2	R/W	Port 2C group I/O select flag

Remarks: Dummy is "0".

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
P2BGIO	FLG	0.0A7H.1	R/W	Port 2B group I/O select flag
POCGIO	FLG	0.0A7H.0	R/W	Port 0C group I/O select flag
SIOOSF8	FLG	0.0A8H.3	R	SIO0 shift 8 clock register
SIOOSF9	FLG	0.0A8H.2	R	SIO0 shift 9 clock register
SBSTT	FLG	0.0A8H.1	R	SIO0 start condition detector flag
SBBSY	FLG	0.0A8H.0	R	SIO0 busy condition detector flag
INTGRP1	FLG	0.0AAH.3	R	Interrupt group 1 interrupt status flag
IRQGRP1	FLG	0.0AAH.0	R/W	Interrupt group 1 interrupt request flag
INTGRP0	FLG	0.0ABH.3	R	Interrupt group 0 interrupt status flag
IRQGRP0	FLG	0.0ABH.0	R/W	Interrupt group 0 interrupt request flag
IGRPLSL2	FLG	0.0ACH.2	R/W	Interrupt group 1 selection flag
IGRPLSL1	FLG	0.0ACH.1	R/W	Interrupt group 1 selection flag
IGRPLSL0	FLG	0.0ACH.0	R/W	Interrupt group 1 selection flag
IGRP0SL	FLG	0.0ADH.0	R/W	Interrupt group 0 selection flag
IPGRP1	FLG	0.0AEH.3	R/W	Interrupt group 1 interrupt enable flag
IPGRP0	FLG	0.0AEH.2	R/W	Interrupt group 0 interrupt enable flag
IPSIO0	FLG	0.0AEH.1	R/W	SIO0 interrupt enable flag
IPTM2	FLG	0.0AEH.0	R/W	Timer 2 interrupt enable flag

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
IPTM1	FLG	0.0AFH.3	R/W	Timer 1 interrupt enable flag
IP1	FLG	0.0AFH.2	R/W	INT1 pin interrupt enable flag
IPTM0	FLG	0.0AFH.1	R/W	Timer 0 interrupt enable flag
IP0	FLG	0.0AFH.0	R/W	INT0 pin interrupt enable flag
CKOEN	FLG	0.0B0H.0	R/W	Clock out enable flag
PLLRFCK3	FLG	0.0B1H.3	R/W	PLL reference clock select flag
PLLRFCK2	FLG	0.0B1H.2	R/W	PLL reference clock select flag
PLLRFCK1	FLG	0.0B1H.1	R/W	PLL reference clock select flag
PLLRFCK0	FLG	0.0B1H.0	R/W	PLL reference clock select flag
ERAMSEL	FLG	0.0B3H.1	R/W	Expansion RAM select flag
ERAMHSEL	FLG	0.0B3H.0	R/W	Expansion RAM high-order bit select flag
P2ABIO3	FLG	0.0B4H.3	R/W	P2A3 I/O select flag
P2ABIO2	FLG	0.0B4H.2	R/W	P2A2 I/O select flag
P2ABIO1	FLG	0.0B4H.1	R/W	P2A1 I/O select flag
P2ABIO0	FLG	0.0B4H.0	R/W	P2A0 I/O select flag
P1ABIO3	FLG	0.0B5H.3	R/W	P1A3 I/O select flag
P1ABIO2	FLG	0.0B5H.2	R/W	P1A2 I/O select flag
P1ABIO1	FLG	0.0B5H.0	R/W	P1A1 I/O select flag
P1ABIO0	FLG	0.0B5H.0	R/W	P1A0 I/O select flag
P0BBIO3	FLG	0.0B6H.3	R/W	P0B3 I/O select flag
P0BBIO2	FLG	0.0B6H.2	R/W	P0B2 I/O select flag
P0BBIO1	FLG	0.0B6H.1	R/W	P0B1 I/O select flag

(to be continude)

(cont'd)

Symbol Name	Attribute	Value	R/W	Description
POBBIO0	FLG	0.0B6H.0	R/W	POB0 I/O select flag
POABIO3	FLG	0.0B7H.3	R/W	POA3 I/O select flag
POABIO2	FLG	0.0B7H.2	R/W	POA2 I/O select flag
POABIO1	FLG	0.0B7H.1	R/W	POA1 I/O select flag
POABIO0	FLG	0.0B7H.0	R/W	POA0 I/O select flag
SIO0IMD3	FLG	0.0B8H.3	R/W	SIO0 interrupt source register (dummy)
SIO0IMD2	FLG	0.0B8H.2	R/W	SIO0 interrupt source register (dummy)
SIO0IMD1	FLG	0.0B8H.1	R/W	SIO0 interrupt source register
SIO0IMD0	FLG	0.0B8H.0	R/W	SIO0 interrupt source register
SIO0CK3	FLG	0.0B9H.3	R/W	SIO0 shift clock select flag (dummy)
SIO0CK2	FLG	0.0B9H.2	R/W	SIO0 shift clock select flag (dummy)
SIO0CK1	FLG	0.0B9H.1	R/W	SIO0 shift clock select flag
SIO0CK0	FLG	0.0B9H.0	R/W	SIO0 shift clock select flag
IRQSIO0	FLG	0.0BAH.0	R/W	SIO0 interrupt request flag
IRQTM2	FLG	0.0BBH.0	R/W	Timer 2 interrupt request flag
INTTM1	FLG	0.0BCH.3	R	Timer 1 interrupt status flag
IRQTM1	FLG	0.0BCH.0	R/W	Timer 1 interrupt request flag
INT1	FLG	0.0BDH.3	R	INT1 pin interrupt status flag
IRQ1	FLG	0.0BDH.0	R/W	INT1 pin interrupt request flag
INTTM0	FLG	0.0BEH.3	R	Timer 0 interrupt status flag
IRQTM0	FLG	0.0BEH.0	R/W	Timer 0 interrupt request flag
INT0	FLG	0.0BFH.3	R	INT0 pin interrupt status flag
IRQ0	FLG	0.0BFH.0	R/W	INT0 pin interrupt request flag

Remarks: Dummy is "0".

3.5 PERIPHERAL REGISTERS

Symbol	Attribute	Value	R/W	Description
SIO1SFR	DAT	03H	R/W	SIO1 shift register
SIO0SFR	DAT	04H	R/W	SIO0 shift register
TM2M	DAT	08H	W	Timer 2 modulo register
TM2C	DAT	09H	R	Timer 2 counter
TM1C	DAT	10H	W	Timer 1 counter
TM1M	DAT	11H	R/W	Timer 1 modulo register
ADCR	DAT	0AH	R/W	ADC reference voltage setting register
CGPR	DAT	20H	R/W	CGP data register
AR	DAT	40H	R/W	GET/PUT/PUSH/CALL/BR/ MOVT/MOVTH/MOVTL instruction address register
PLLR	DAT	41H	R/W	PLL data register
IFC	DAT	43H	R	IF counter data register
TM0M	DAT	46H	R/W	Timer 0 modulo register
TM0C	DAT	47H	R	Timer 0 counter
PWMR0	DAT	48H	R/W	PWM0 data register
PWMR1	DAT	49H	R/W	PWM1 data register
PWMR2	DAT	4AH	R/W	PWM2 data register
TM3M	DAT	4AH	R/W	Timer 3 modulo register
DBFSTK	DAT	4FH	R/W	DBF stack

3.6 LIST OF RESERVED WORDS (ALPHABETICAL ORDER)

3.6.1 INSTRUCTIONS/ PSEUDO-INSTRUCTIONS (1/2)

ADD	CLR1	ENDIFNC	INITFLG
ADDC	CLR2	ENDM	IRP
AND	CLR3	ENDP	LAB
BANK0	CLR4	ENDR	LBMAC
BANK1	CSEG	EOF	LD
BANK2	DAT	EXIT	LFCOND
BANK3	DB	EXITR	LIST
BANK4	DCP	EXTRN	LITERAL
BANK5	DI	FLG	LMAC
BANK6	DW	GET	MACRO
BANK7	EI	GLOBAL	MEM
BELLOW	EJECT	HALT	MOV
BR	ELSE	IF	MOVT
C14344	END	IFCHAR	NIBBLE
C4444	ENDCASE	IFNCHAR	NIBBLE1
CALL	ENDIF	INC	NIBBLE2
CASE	ENDIFC	INCLUDE	NIBBLE2V

INSTRUCTIONS/ PSEUDO-INSTRUCTIONS (2/2)

NIBBLE3	NOT3	RORC	SKT1
NIBBLE3V	NOT4	SBMAC	SKT2
NIBBLE4	OBMAC	SET	SKT3
NIBBLE4V	OMAC	SET1	SKT4
NIBBLE5	OR	SET2	SMAC
NIBBLE5V	ORG	SET3	ST
NIBBLE6	OTHER	SET4	STOP
NIBBLE6V	PEEK	SFCOND	SUB
NIBBLE7	POKE	SKE	SUBC
NIBBLE7V	POP	SKF	SUMMARY
NIBBLE8	PUBLIC	SKF1	SYSCAL
NIBBLE8V	PURGE	SKF2	TAG
NOBMAC	PUSH	SKF3	TITTLE
NOLIST	PUT	SKF4	XOR
NOMAC	REPT	SKGE	ZZZERROR
NOP	RET	SKLT	ZZZMCHK
NOT1	RETI	SKNE	ZZZMSG
NOT2	RETSK	SKT	

3.6.2 REGISTERS/FLAGS (1/4)

ADCCH0	BTM0CY	IEGGRP1	INTGRP1
ADCCH1	CE	IEGTM0	INTTM0
ADCCH2	CGPR	IFC	INTTM1
ADCCH3	CGPSEL	IFCCK0	IP0
ADCCMP	CKOEN	IFCCK1	IP1
ADCEND	CMP	IFCGOSTT	IPGRP0
ADCR	CY	IFCMD0	IPGRP1
ADCSOFT	DBF	IFCMD1	IPSIO0
ADCSTRT	DBF0	IFCRES	IPTM0
AR	DBF1	IFCSTRT	IPTM1
AR0	DBF2	IGRPOSL	IPTM2
AR1	DBF3	IGRP1SL0	IRQ0
AR2	DBFSP	IGRP1SL1	IRQ1
AR3	DBFSTK	IGRP1SL2	IRQGRP0
AR_EPA0	ERAMHSEL	INT0	IRQGRQ1
AR_EPA1	ERAMSEL	INT1	IRQSIO0
BANK	IEG0	IRQTM0	IRQTM1
BCD	IEG1	INTGRP0	IRQTM2

REGISTERS/FLAGS (2/4)

IX	P0B2	P1A3	P2A3
IXE	P0B3	P1ABI00	P2ABI00
IXH	P0BBI00	P1ABI01	P2ABI01
IXL	P0BBI01	PIABI02	P2ABI02
IXM	P0BBI02	PIABI03	P2ABI03
MPE	P0BBI03	P1B0	P2B0
MPH	P0C0	P1B1	P2B1
MPL	P0C1	P1B2	P2B2
P0A0	P0C2	P1B3	P2B3
P0A1	P0C3	P1C2	P2BGIO
P0A2	P0CGIO	P1C3	P2C0
P0A3	P0D0	P1D0	P2C1
P0ABI00	P0D1	P9D9	P2C2
P0ABI01	P0D2	P1D2	P2C3
P0ABI02	P0D3	P1D3	P2CGIO
P0ABI03	P1A0	P2A0	P2D0
P0B0	P1A1	P2A1	P2D1
P0B1	P1A2	P2A2	P2D2

REGISTERS/FLAGS (3/4)

P2D3	P4A3	PWMR2	SIO0MS
P2DGIO	PLLEOBST	RPH	SIO0NWT
P3A0	PLLMD0	RPL	SIO0SF8
P3A1	PLLMD1	SB	SIO0SF9
P3A2	PLLMD2	SBACK	SIO0SFR
P3A3	PLLMD3	SBBSY	SIO0TX
P3AGIO	PLLR	SBSTT	SIO0WRQ0
P3B0	PLLRFCK0	SIO0CH	SIO0WRQ1
P3B1	PLLRFCK1	SIO0CK0	SIO0WSTT
P3B2	PLLRFCK2	SIO0CK1	SIO1CK0
P3B3	PLLRFCK3	SIO0CK2	SIO1CK1
P3BGIO	PLLUL	SIO0CK3	SIO1SFR
P3C0	PSW	SIO1HIZ	SIO1TS
P3C1	PWM0SEL	SIO0IMD0	SP
P3C2	PWM1SEL	SIO0IMD1	SYSRSP
P3C3	PWM2SEL	SIO0IMD2	TM0C
P3D3	PWMR0	SIO0IMD3	TM0CK
P4A2	PWMR1	SIO0ITMG	TM0EN

REGISTERS/FLAGS (4/4)

TM0M	TM1OVF	ZZZ2
TM0OVF	TM1RES	ZZZ3
TM0RES	TM1RPT	ZZZ4
TM1C	TM2C	ZZZ5
TM1CK0	TM2CK0	ZZZ6
TM1CK1	TM2CK1	ZZZ7
TM1CK2	TM2EN	ZZZ8
TM1CK3	TM2M	ZZZ9
TM1EN	TM2RES	ZZZDEVID
TM1GCEG	TM3EN	ZZZEPA
TMIGCMAN	TM3M	ZZZLSARG
TMIGOAUT	TM3RES	ZZZPRINT
TMIGOEG	TM3RPT	ZZZSKIP
TMIGOSEL	TM3SEL	ZZZSYDOC
TMIGOSTT	WR	ZZZALBMAC
TM1INSEL	Z	ZZZALMAC
TM1M	ZZZ0	ZZZARGC
TM1MSEL	ZZZ1	ZZZLINE

Phase-out/Discontinued