ZL2005PEVK4

10A Evaluation Board

AN1464
Rev.1.2
May 7, 2009

ZL2005PEVK4 10A Evaluation Board

Description

The ZL2005P is an innovative mixed-signal power management and conversion IC that combines a compact, efficient, synchronous buck controller, adaptive drivers and key power and thermal management functions in a single package. The FG ZL2005PEVK4 platform allows evaluation of the features in the highly-configurable ZL2005P via the SMBus interface using PMBus™ commands. The PMBus command set is accessed by using Zilker Labs evaluation software from a PC running Microsoft Windows.

This evaluation board is meant to enable rapid evaluation of the functionality of the ZL2005P in a 10A configuration. It has been optimized for ease of evaluation across a wide range of input and output conditions. This FG ZL2005PEVK4 platform is provided as a reference design.

Features

- PMBus™ control via SMBus™
- Pin-strap selection for stand-alone operation
- V_{OUT} settable from +0.8V to +3.3V
- $^{r}DS(ON)$ sensing
- Convenient power connection
- Onboard enable switch
- Power-good indicator
- External temperature sensor

Target Specifications

This board has been designed for the following conditions:

- V_{IN} = 12V (Board range 4.5V to 13.2V)
- V_{OUT} = 1.2V (Board range is 0.8V to 3.3V)
- I_{OUT} = 0A to 10A
- F_{SW} = 600kHz
- Output ripple: <1%
- Dynamic response: 4% (7.5A to 10A step) @ 2.5V
- Temperature: +25°C

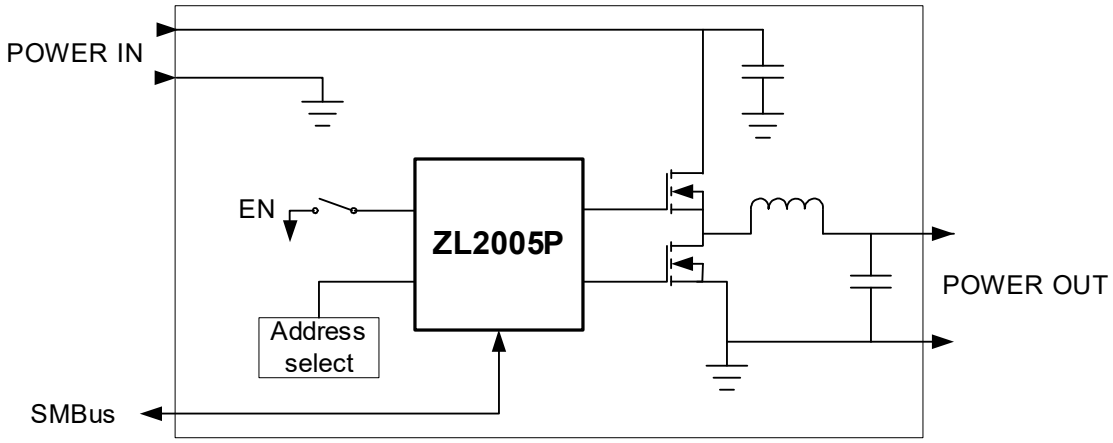

FIGURE 1. FG ZL2005PEVK4 BLOCK DIAGRAM

Functional Description

The FG ZL2005PEVK4 provides the circuit required to demonstrate the features of the ZL2005P in a 10A configuration. The FG ZL2005PEVK4 has a functionally-optimized layout that allows highly-efficient operation to its maximum output current (see Figure 2). The input power connection is provided through banana jack terminals. Stand-alone operation of the ZL2005P is achieved by factory installed pin-strap settings and pre-configuration via PMBus commands. PMBus protocol communication is performed via a SMBus interface using an external USB to SMBus adaptor. PMBus commands can be used to modify the settings of the evaluation platform.

Figure 3 shows the ZL2005P circuit schematic. The circuit consists of the ZL2005P power conversion and management IC with its minimal component count.

The input voltage connection is made at J1 which is labeled VIN±. J2 is the output connector for the output voltage, VOUT±. The VIN± and VOUT± connections are rated to 10A.

Figure 4 shows the FG ZL2005PEVK4 interface schematic. It contains various circuits that interface to the ZL2005P's circuit. The hardware enable function is controlled by a toggle switch (SW1) on the FG ZL2005PEVK4 board. External temperature is monitored from a 2N3904 transistor (Q3) connected to the XTEMP pin. This external temperature is read with the READ_TEMPERATURE_2 PMBus™ command. The power good status is indicated by the PG LED at D11. The PG LED indicates the correct state of the power good signal when power is applied to the FG ZL2005PEVK4 board. The right angle headers at opposite ends of the board (J10 and J11) are available to daisy chain multiple boards. The SMBus and Enable signals are passed between these connectors. All header pins and switch positions are labeled on the FG ZL2005PEVK4 board's silkscreen as shown in Figure 5.

The ZL2005P SMBus™ address is set by the jumper applied to J12. The SA1 pin is strapped by an 11kΩ resistor to ground. The J12 jumper applies a different resistor to the SA0 pin to achieve the indicated SMBus address settings. Note that power must be cycled to set a new address.

Refer to Figures 5 through 10 for component placement and board layout. The board layout has been optimized for two-sided component area and thermal performance. For ZL2005P circuit layout design considerations refer to Zilker Labs Application Note AN10 (Reference 1 on page 18).

Operation

Stand-Alone Operation

The FG ZL2005PEVK4 is easy to setup and operate. It is configured, out of the box, to provide 1.2V at 10A from a 12V source. All input and output connections should be made before turning the input supply on.

When the input power supply is turned on, and the enable switch is set to enable, the ZL2005P will output the configured voltage. A load can be applied to the output and the circuit can be tested.

PMBus Operation

The ZL2005P utilizes the PMBus protocol. The PMBus functionality can be accessed via USB from a PC running the Zilker Labs Evaluation software on a Windows XP or Windows 2000/NT operating system.

Install the Zilker Labs Evaluation software using the CD included in the FG ZL2005PEVK4 kit or download it from the web at www.zilkerlabs.com.

For PMBus operation, connect a USB to SMBus adaptor (J2) to the EVB (J10). Apply a USB cable between the USB to SMBus adaptor and the PC. Connect the output of the FG ZL2005PEVK4 to the desired load. Then connect an appropriate power supply to the input. Place the enable switch in "DISABLE" and turn on the power. Invoke the ZL2005P interface software.

The Zilker Labs Evaluation software allows modification of all ZL2005P PMBus parameters. Manually configure the ZL2005P with the interface software or load a predefined configuration from a configuration text file.

Use the mouse-over pop-ups for help with the Zilker Labs Evaluation software. Refer to the Zilker Labs Application Note AN13 (Reference 3 on page 18) for PMBus details.

The enable switch can then be moved to "ENABLE" and the ZL2005P can be tested. Alternatively, the PMBus commands ON_OFF_CONFIG and OPERATION may be used to manipulate the enable state.

Modifying the FG ZL2005PEVK4

In order to design and test an alternative power train circuit with the ZL2005P, choose a desired operating conditions and power train. Enter the selected power design parameters into Zilker Labs' PID calculation/simulation tool. The results from the simulation tool provide appropriate compensation values to configure the new ZL2005P circuit. Apply the new power train circuit to the evaluation board. Power the board and invoke the evaluation software. Then configure the new PID coefficients using the "PMBus: Basic" command page or loading a configuration text file with the new compensation coefficients in it.

Quick Start Guide

Stand-alone Operation

- Set enable switch (EN) to "DISABLE"
- Apply load to VOUT+/VOUT-
- Connect power supply to VIN+/VIN- (supply turned off)
- Turn power supply on
- Set enable switch (EN) to "ENABLE"
- Test ZL2005P operation

PMBus Operation

- Insert the Zilker Labs Eval Software CD.
- Install the Eval Software by running setup.exe from the PowerNavigator_installer folder on the CD.
- Connect a USB/SMBus™ adaptor (J2) to the EVB (J10)
- Select a SMBus address with the jumper on J12.
- Connect supplied USB cable from computer to EVB
- Upon first time connection, the Found New Hardware Wizard will appear. Select "No, Not this time" and click Next.
- Select "Install from a list or specific location (Advanced)" and click Next.
- Select "Search the best driver in these locations" and only select the "Search removable media" option, then click Next.
- If you encounter a popup warning during driver installation, click the "Continue Anyway" button
- Follow steps 1 - 4 under Stand-alone Operation
- Invoke "PowerNavigator" from the Start menu under Zilker Labs.
- Monitor and configure EVB using the informative pages in the evaluation software.
- Test the ZL2005P operation.

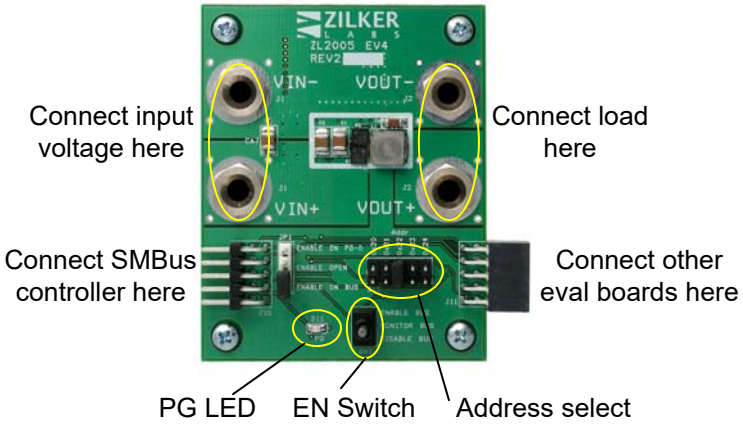

FIGURE 2. FG ZL2005PEVK4 EVALUATION BOARD

Schematics

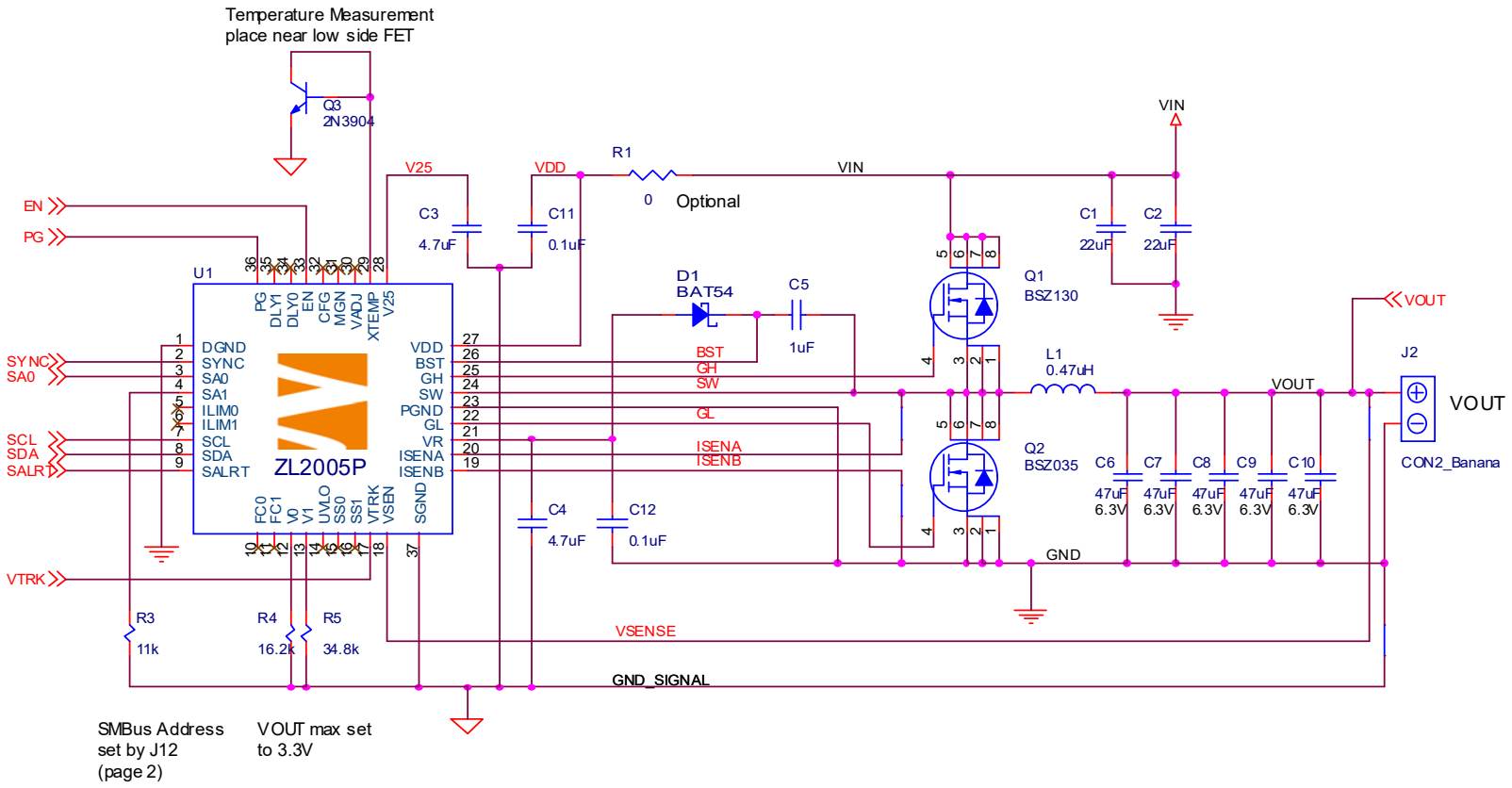

FIGURE 3. FG ZL2005PEVK4 CIRCUIT

Schematics (Continued)

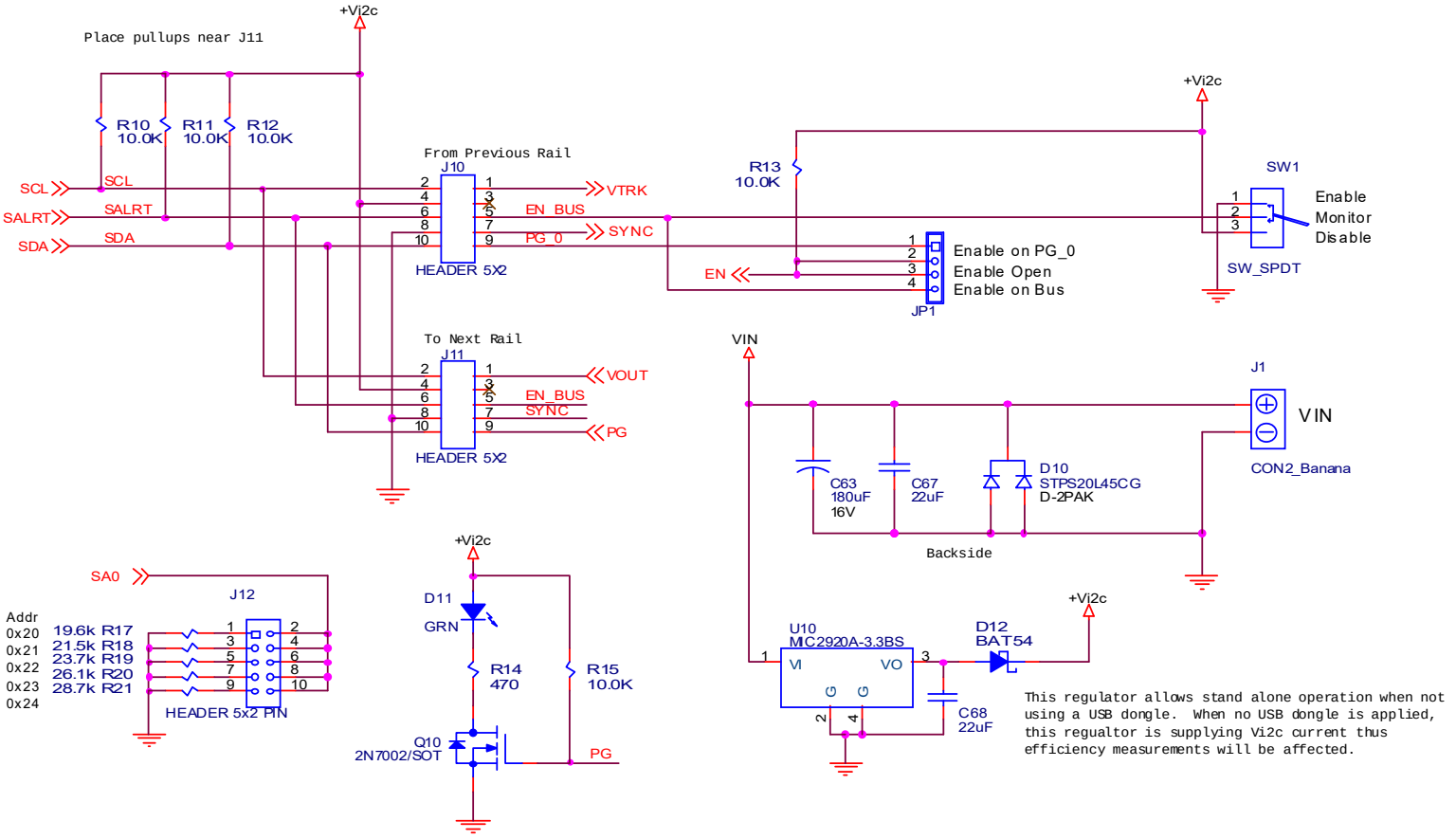

FIGURE 4. FG ZL2005PEVK4 INTERFACE

Board Layout

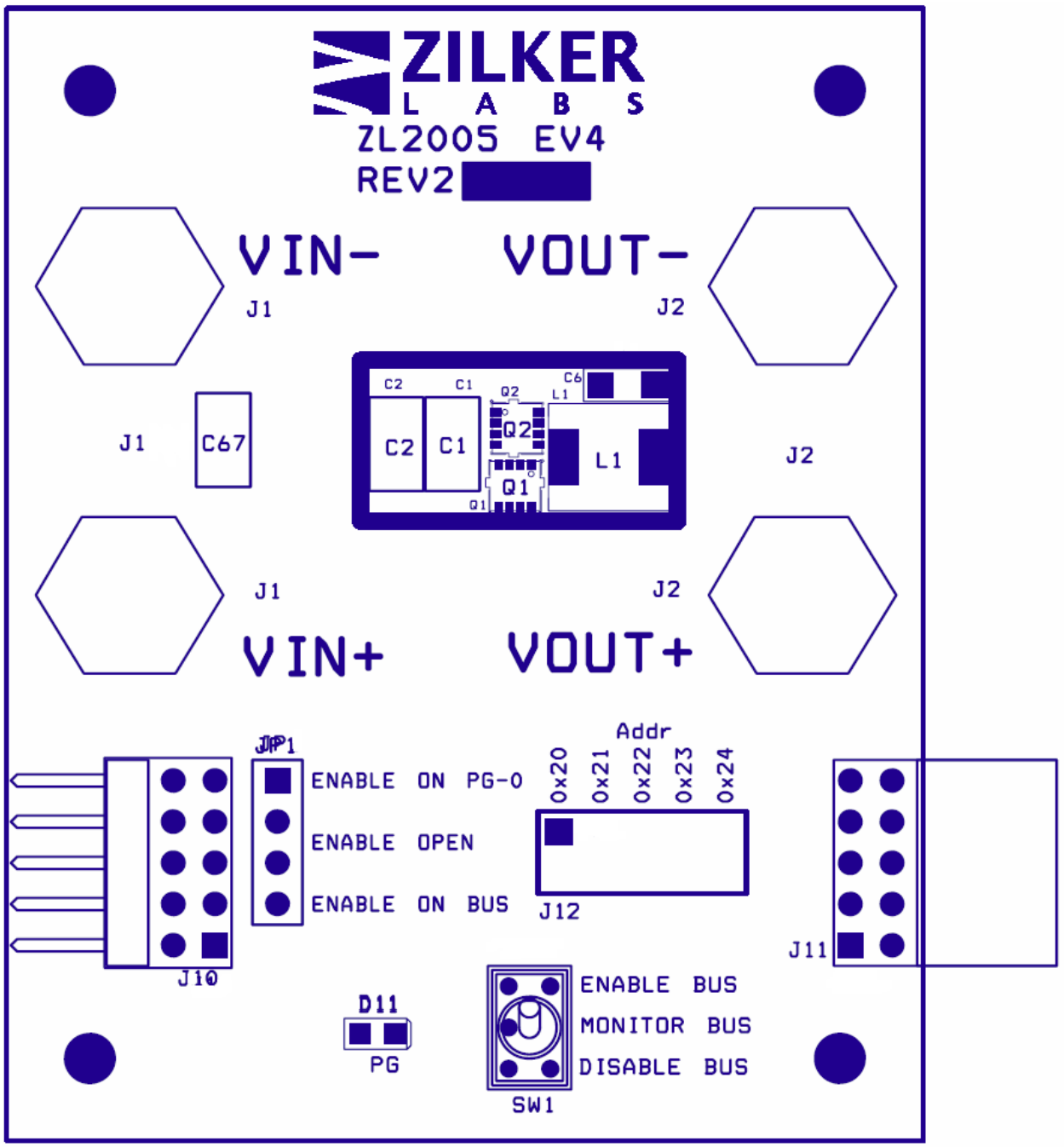

FIGURE 5. FG ZL2005PEVK4 SILK SCREEN TOP

Board Layout (Continued)

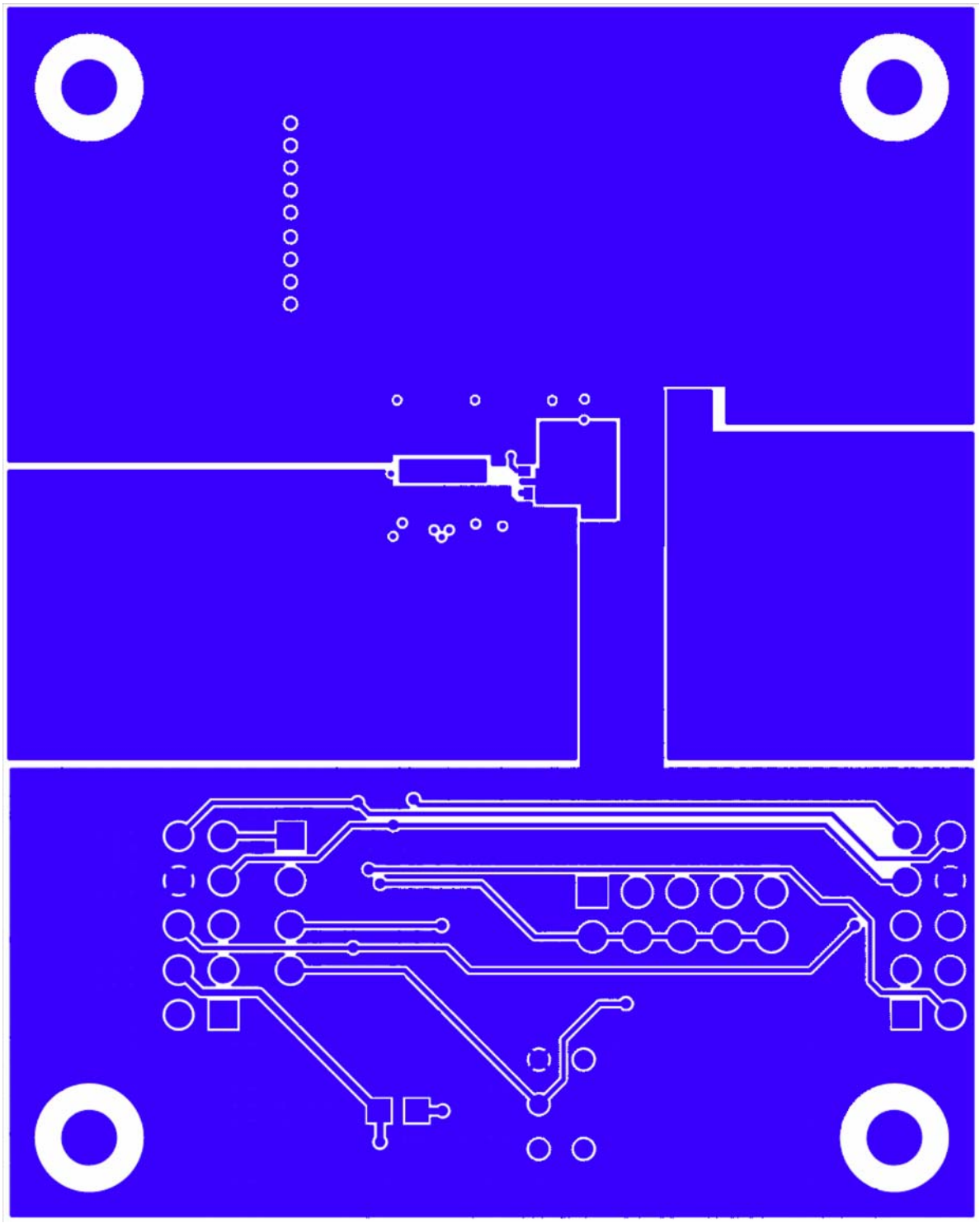

FIGURE 6. FG ZL2005PEVK4 PCB TOP LAYER

Board Layout (Continued)

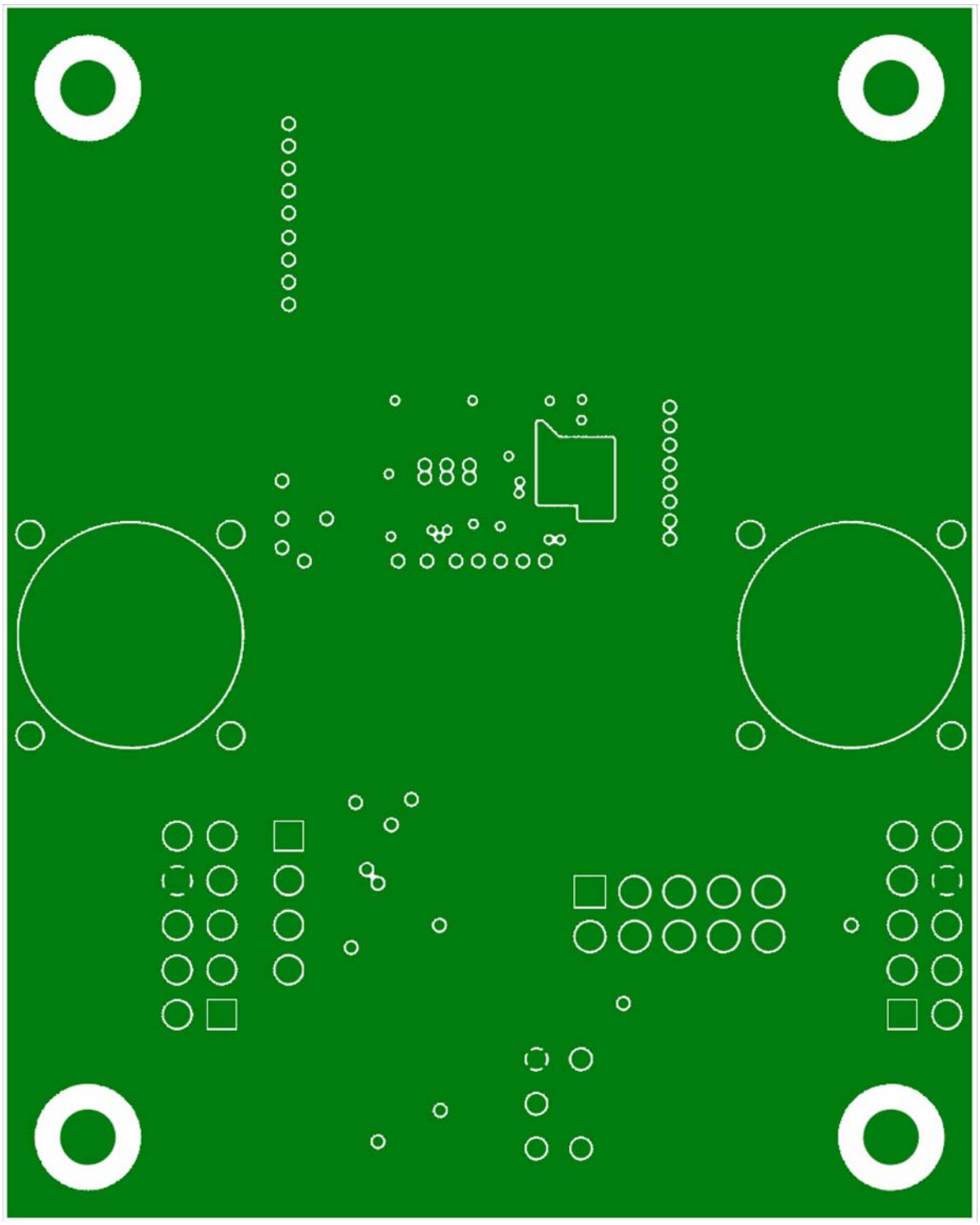

FIGURE 7. FG ZL2005PEVK4 PCB INNER LAYER 1

Board Layout (Continued)

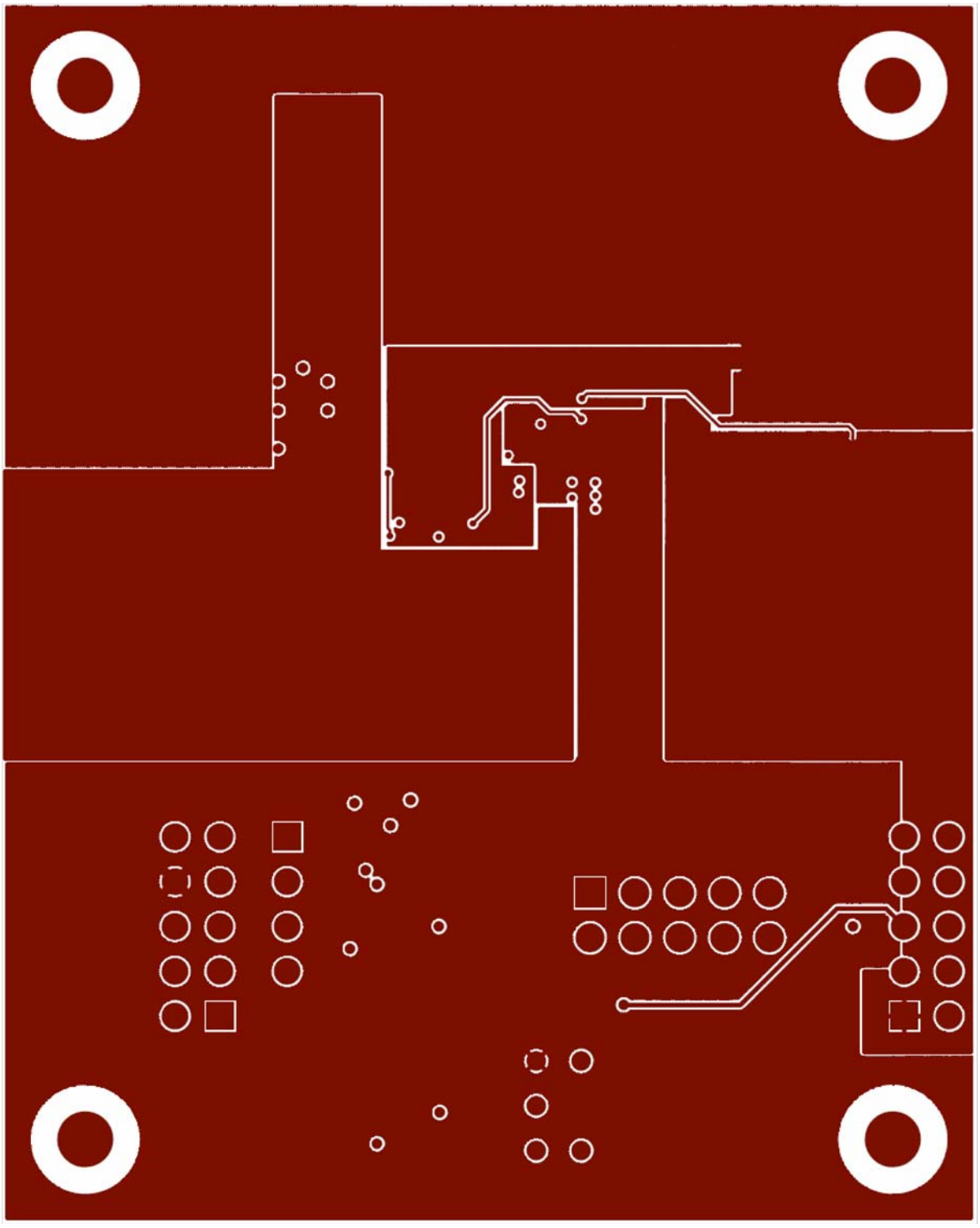

FIGURE 8. FG ZL2005PEVK4 PCB INNER LAYER 2

Board Layout (Continued)

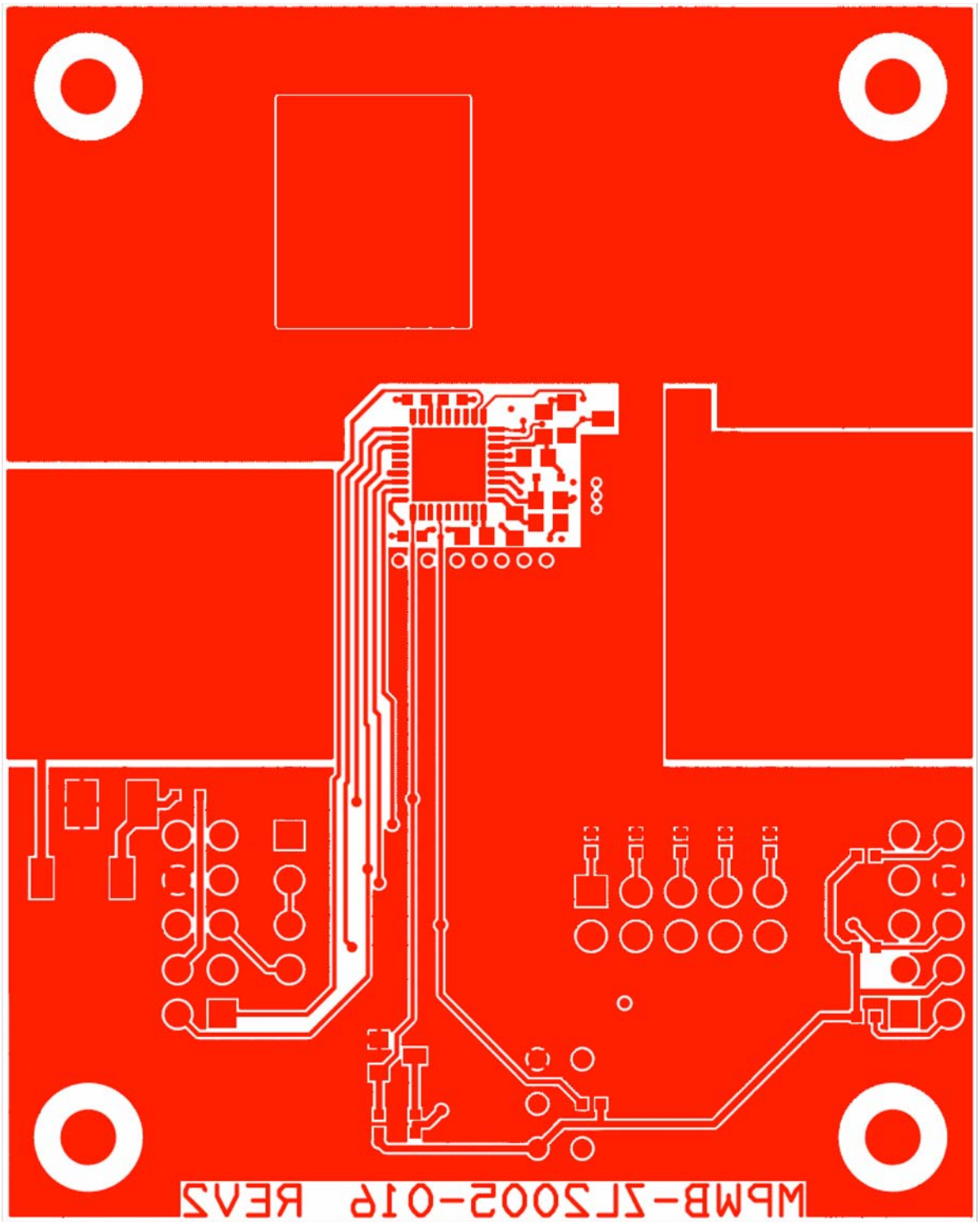

FIGURE 9. FG ZL2005PEVK4 BOTTOM LAYER (TOP VIEW)

Board Layout (Continued)

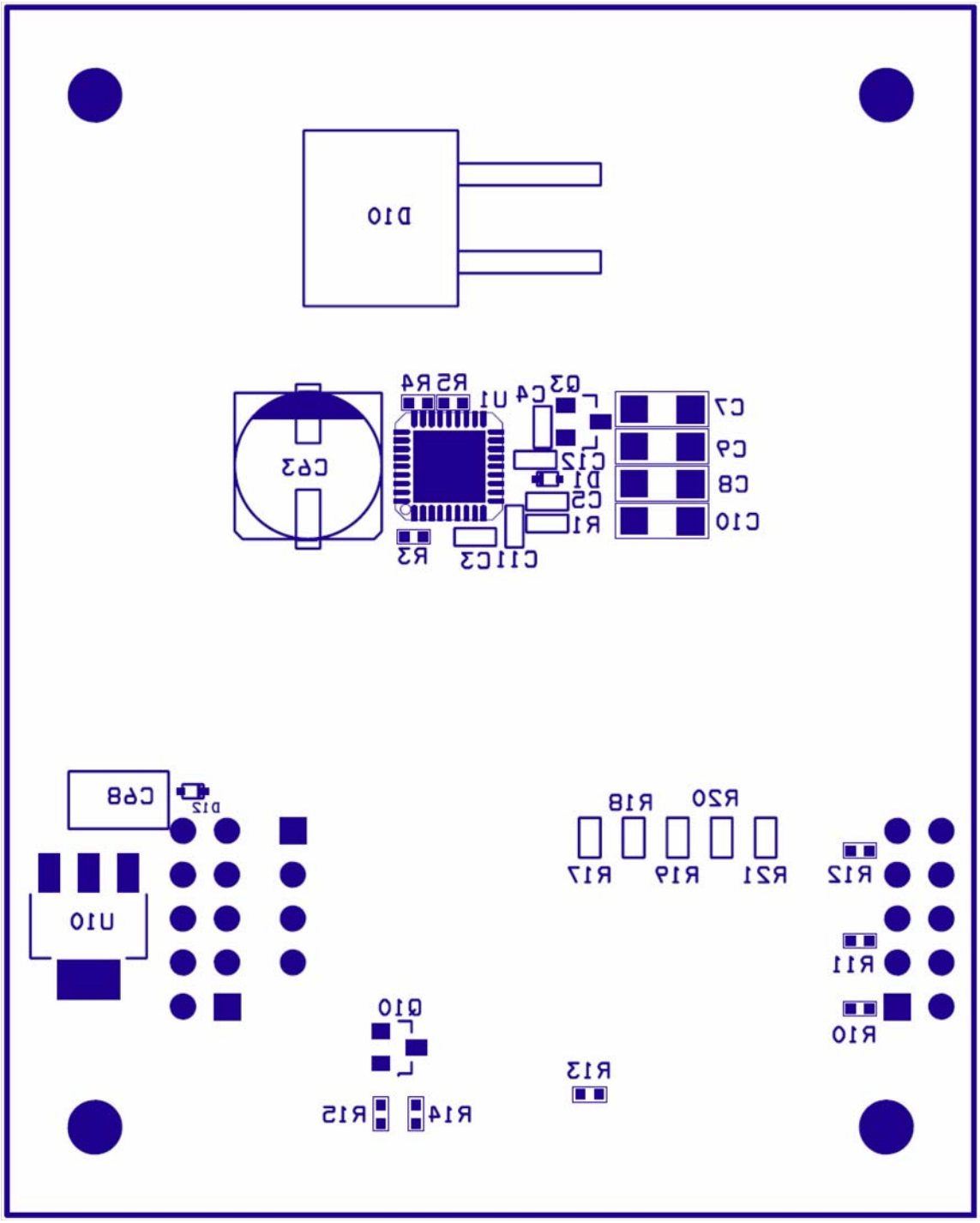

FIGURE 10. FG ZL2005PEVK4 SILK SCREEN BOTTOM (TOP VIEW - REVERSED)

Bill of Materials

TABLE 1. FG ZL2005PEVK4 REV. 2

ITEM	QTY	REFERENCE	VALUE	TOLERANCE	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
1	4	C1, C2, C67, C68	22µF		16V	X5R	SM1210	MURATA	GRM32ER61C226KE20L
2	2	C3,C4	4.7µF		6.3V	X5R	SM0603	Panasonic - ECG	ECJ-1VB0J475M
3	1	C5	1µF		25V	X5R	SM0603	TAIYO YUDEN	TMK107BJ105KA-T
4	5	C6, C7, C8, C9, C10	47µF	20%	6.3V	X5R	SM1206_A_REV1	TDK	C3216X5R0J476M
5	2	C11, C12	0.1µF	10%	50V	X7R	SM0603	MURATA	GRM39X7R104K050AD
6	1	C63	180µF		16V	ELECT POLY	SM_CAP_8.3X8.3_PXA	United Chemi-Con	APXA160ARA181MHC0G
7	2	D1, D12	BAT54		30V	Schottky	SOD523	ON Semiconductor	BAT54XV2T1OS
8	1	D10	STPS20L45CG				D-2PAK	STMicro	STPS20L45CG
9	1	D11	GRN		2V		led2-45x51	CHICAGO MINIATURE	CMD17-21VGC
10	1	JP1	4 PIN				SIP4/100	SAMTEC	TSW-104-07-T-S
11	2	J1,J2	CON2_Banana				JACK_F_NI_2P.750SP_ .175PLUG	Emerson	108-0740-001
12	1	J10	HEADER 5x2				HDR10DUAL100X100	SAMTEC	TSW-105-08-T-D-RA
13	1	J11	HEADER 5x2				HDR10DUAL100X100	SAMTEC	SSQ-105-02-T-D-RA
14	1	J12	HEADER 5x2 PIN				HDR10DUAL100X100	SAMTEC	TSW-105-07-T-D
15	1	L1	0.47µH		17.5A	Powder	IHLP_2525BD_REV1	Vishay	IHLP2525CZERR47M01
16	1	Q1	BSZ130				PP1212SP	INFINEON	BSZ130N03LS
17	1	Q2	BSZ035				PP1212SP	INFINEON	BSZ035N03LS
18	1	Q3	2N3904		40V	NPN	SOT-23	ON SEMI	MMBT3904LT3
19	1	Q10	2N7002/SOT		60V	N-CH	SOT-23	ON SEMI	2N7002LT1
20	1	R1	0				SM0603	PANASONIC-ECG	ERJ-3GEY0R00V
21	1	R3	11k	1%			SM0402	PANASONIC-ECG	ERJ-2RKF1102X
22	1	R4	16.2k	1%			SM0402	PANASONIC-ECG	ERJ-2RKF1622X
23	1	R5	34.8k	1%			SM0402	PANASONIC-ECG	ERJ-2RKF3482X
24	5	R10, R11, R12, R13, R15	10.0k	1%			SM0402	VENKEL	CR0402-16W-1002FT
25	1	R14	470	1%			SM0402	Rohm	MCR01MZPF4700
26	1	R17	19.6k	1%			SM0402	VISHAY	CRCW040219K6FKED

Bill of Materials (Continued)

TABLE 1. FG ZL2005PEVK4 REV. 2

ITEM	QTY	REFERENCE	VALUE	TOLERANCE	RATING	TYPE	PCB FOOTPRINT	MANUFACTURER	PART NUMBER
27	1	R18	21.5k	1%			SM0402	VISHAY	CRCW040221K5FKED
28	1	R19	23.7k	1%			SM0402	VISHAY	CRCW040223K7FKED
29	1	R20	26.1k	1%			SM0402	VENKEL	CR0402-16W-2612FT
30	1	R21	28.7k	1%			SM0402	VISHAY	CRCW040228K7FKED
31	1	SW1	SW_SPDT				SW_TOG_ULTRAMIN_SPDT	NKK	G-13AP-RO
32	1	U1	ZL2005P				MLF36	Zilker Labs	ZL2005P
33	1	U10	MIC2920A-3.3BS				SOT223_1234_FLD	Micrel	MIC2920A-3.3WS
34	1		PCB						MPWB-ZL2005-016
35	2	J12-Addr22, JP1ENbus	CONN JUMPER SHORTING GOLD					SULLINS	SSC02SYAN
36	4		SCREW MACHINE PHILLIPS 4-40X1/4					BUILDING FASTENERS	PMS 440 0025 PH
37	4		STANDOFF RD 4-40THR .750" ALUM					KEYSTONE ELECTRONICS	3481
38	4	J1_2ea,J2_2ea	CAP_MOLDED .25ID_BLK				CAP_MOLDED.25ID	CAPLUGS	VC-234-8

ZL2005P Characterization Data

The following data was acquired using a FG ZL2005PEVK4 Rev. 2 Evaluation Board.

Test 1: Efficiency

Efficiency data was collected for several output voltages for input voltages of 5V and 12V. Note that this data is for informational use only, as the board is optimized for 12V input and 1.2V output operation.

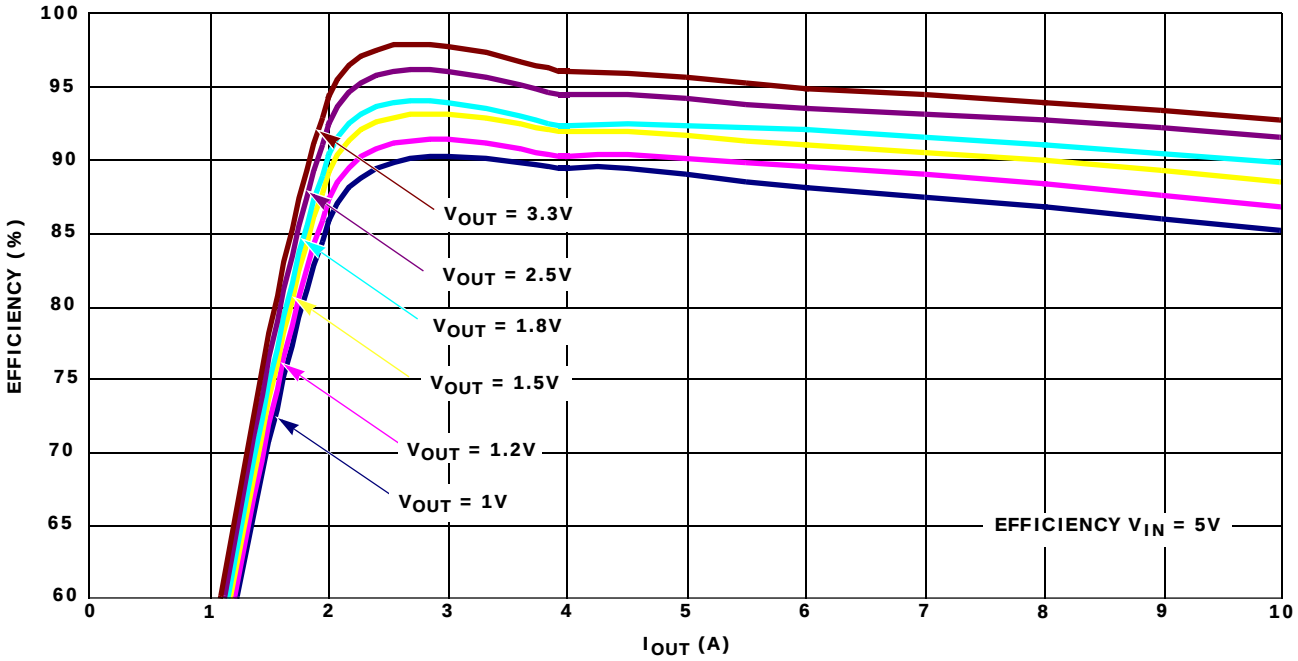

FIGURE 11. EFFICIENCY TEST, V_{IN} = 12V. f_{SW} = 600kHz

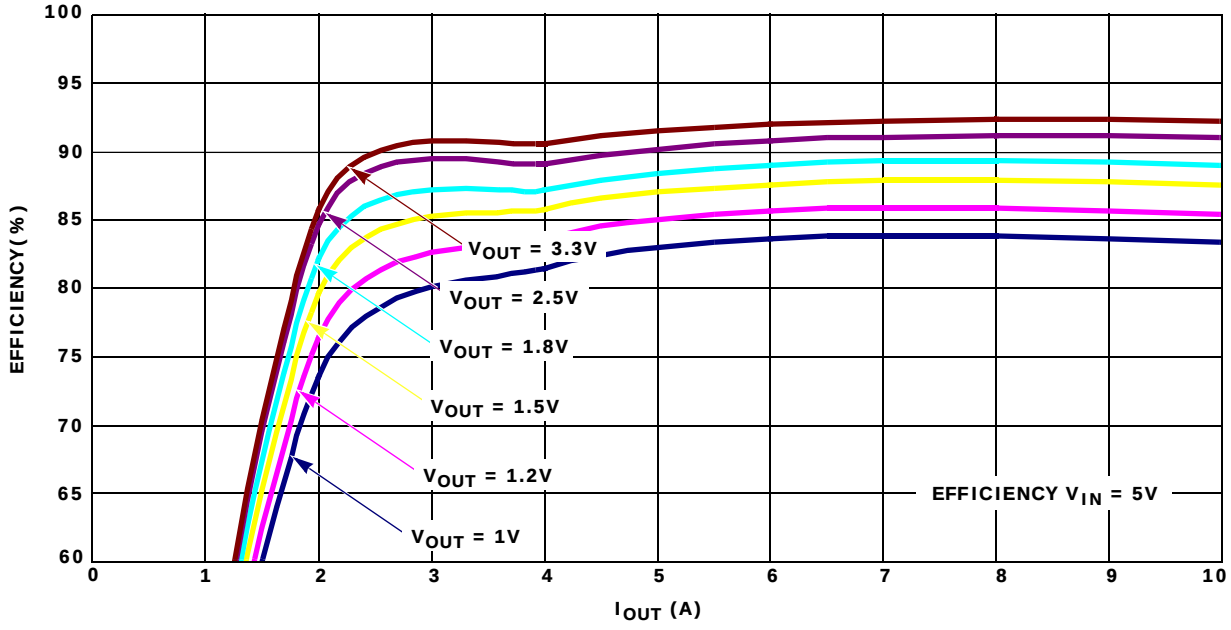

FIGURE 12. EFFICIENCY TEST, V_{IN} = 5V. f_{SW} = 600kHz

ZL2005P Characterization Data (Continued)

The following data was acquired using a FG ZL2005PEVK4 Rev. 2 Evaluation Board.

Test 2: Ramp-Up/Ramp-Down Characteristics

Ramp-up and ramp-down data was acquired based on a nominal output voltage of 1.5V and a preset ramp-up and ramp-down period of 10ms.

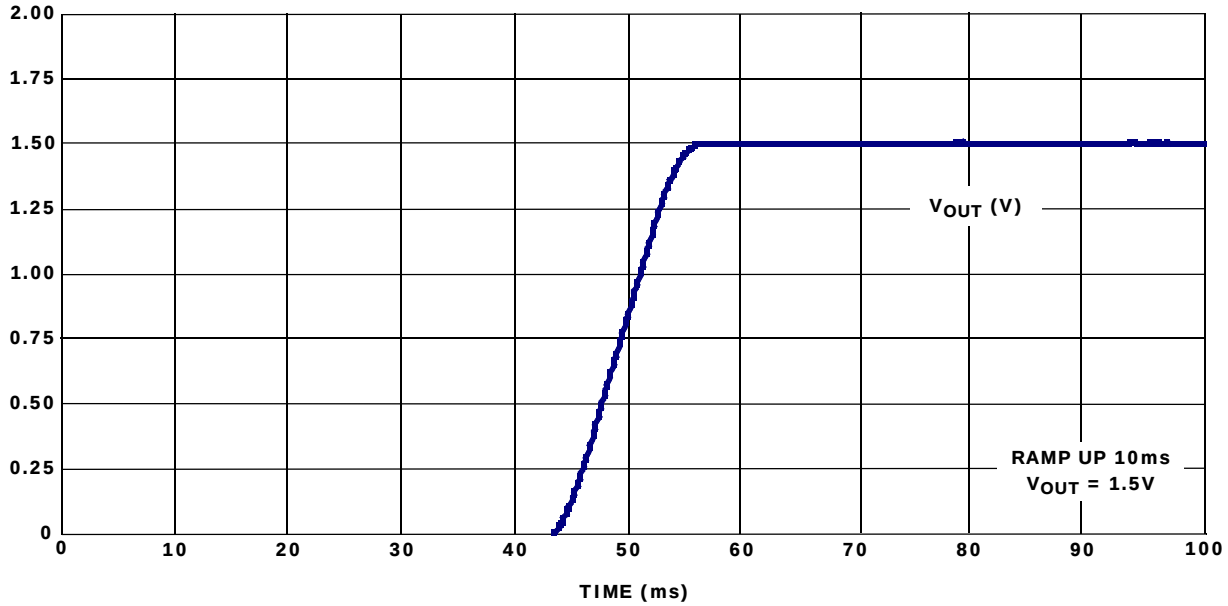

FIGURE 13. RAMP-UP CHARACTERISTIC TEST RESULTS, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 1A

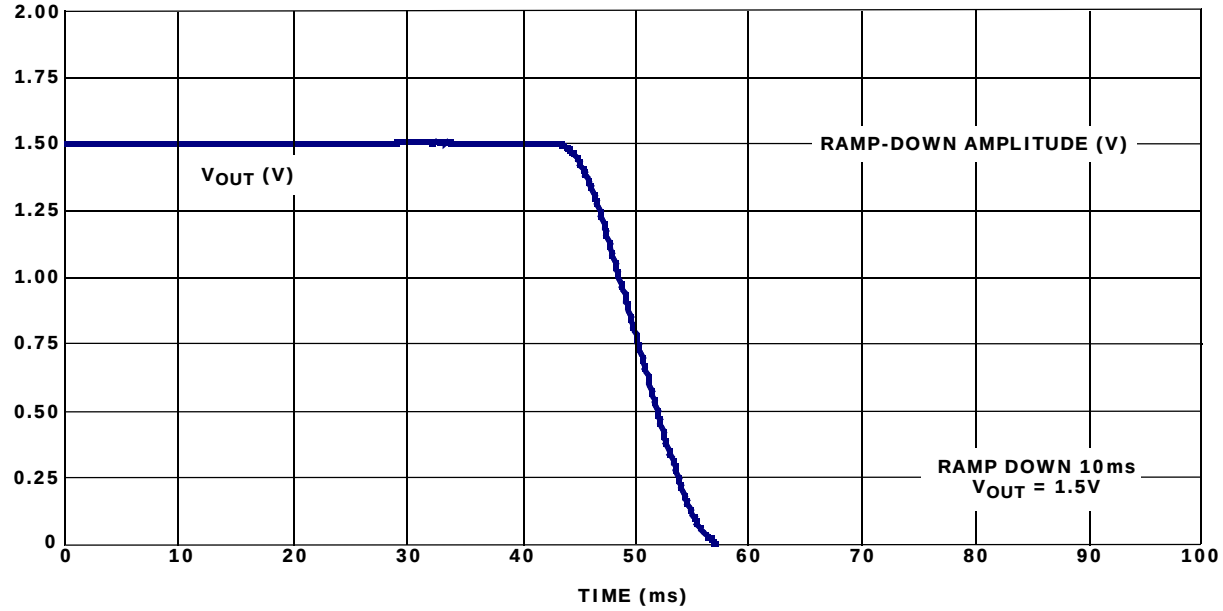

FIGURE 14. RAMP-DOWN CHARACTERISTIC TEST RESULTS, V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 1A

ZL2005P Characterization Data (Continued)

The following data was acquired using a FG ZL2005PEVK4 Rev. 2 Evaluation Board.

Test 3: Dynamic Load Response

For the dynamic load response test, the circuit was set to a nominal output voltage of 2.5V and an input voltage of 6V. A 7.5A to 10A load step (rate of 2.5A/µs) was applied and then released, and the deviation from nominal output was captured in the charts below.

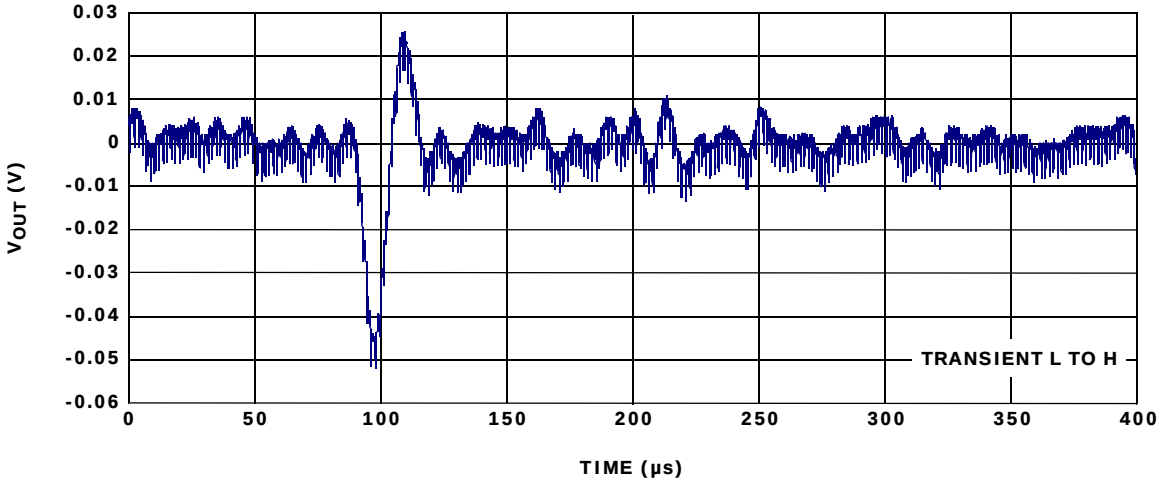

FIGURE 15. DYNAMIC LOAD TEST RESULTS (V)

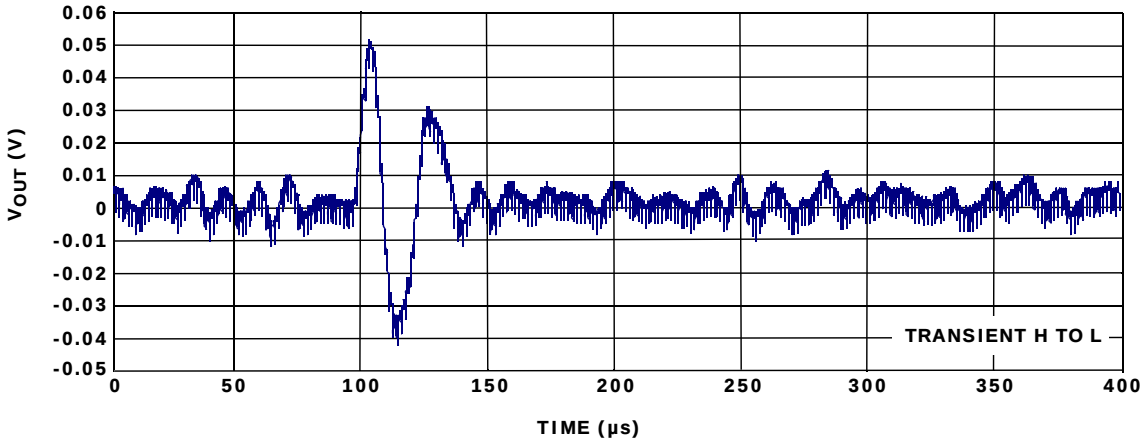

FIGURE 16. DYNAMIC UNLOAD TEST RESULTS (V)

Default Configuration Text

The following PMBus commands have been loaded and stored into the Default Store of the ZL2005P device. Each PMBus can be accessed with the Zilker Labs Evaluation software. The # symbol is used for a comment line.

```
# Configuration file for FG ZL2005PEVK4, Rev 2
#syntax:
#PMBus Command <tab> Value
#Erase default and user store
RESTORE_FACTORY
STORE_DEFAULT_ALL

MFR_ID                    ZilkerLabs
MFR_MODEL           FG ZL2005PEVK4
MFR_REVISION        Rev_1.6
MFR_LOCATION        Austin_TX

VIN_OV_FAULT_LIMIT13.5
VIN_OV_WARN_LIMIT13.2
VIN_UV_FAULT_LIMIT4.2
VIN_UV_WARN_LIMIT4.5

VOUT_COMMAND        1.2    #V
FREQUENCY_SWITCH600  #kHz
POWER_GOOD_DELAY1
TON_DELAY              15
TON_RISE                5
TOFF_DELAY              15
TOFF_FALL               5
SEQUENCE            0x0000

#Use Rdson current sense method with internal
temp sensor
MFR_CONFIG            0x7981
USER_CONFIG             0x0000

PID_TAPSA=1569.69, B=-2903.12, C=1412.91

IOUT_OC_FAULT_LIMIT         20.0
IOUT_AVG_OC_FAULT_LIMIT     15.0

IOUT_UC_FAULT_LIMIT         -10.0
IOUT_AVG_UC_FAULT_LIMIT     -8.0

#low FET not enabled for output OV, output OV
and UV count to 2
OVUV_CONFIG         0x01
IOUT_SCALE       3.65
IOUT_CAL_OFFSET 0

#Set temperature compensation at 4000ppm/ C
internal temp sensor
TEMPCO_CONFIG0x28
NLR_CONFIG0xB303
#VOUT_DROOP          2              #mV/A

STORE_DEFAULT_ALL
RESTORE_DEFAULT_ALL
```

References

[1] *AN10 – ZL2005 Thermal and Layout Guidlelines for the ZL2005,* Zilker Labs Inc., 2007.

[2] AN13 – *ZL2005 and PMBus™*, Zilker Labs, Inc., 2007.

[3] *ZL2005 Data Sheet*, Zilker Labs, Inc., 2007.

Revision History

DATE	REV. #	CHANGE
May 7, 2009	1.2	Converted to Intersil format and assigned file number AN1464. This is the first release with this file number.
Jul 14, 2008	1.1	Changed transient spec to 4%.
Jan 29, 2008	1.0	Initial Release.

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