User's Manual

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R0K0F4022C000BR

V850E2/ML4 CPU Board User's Manual

Renesas Microcomputer

V850E2/ML4 Microcontroller

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About This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this CPU board. A basic knowledge of electrical circuits, logical circuits, and microcomputers (MCUs) is necessary in order to use this manual.

This manual is composed of an overview of the CPU board; its functional and operating specifications.

Carefully read all notes described in the body of text in the manual.

The Revision History summarizes the modifications and additions to the previous versions. Refer to the text of the manual for details.

The following documents apply to the V850E2/ML4 CPU Board R0K0F4022C000BR.

Document Type	Description	Document Title	Document No.
User's Manual	Describes functions (devices, memory maps, electrical characteristics), and operating specifications (connectors, and switches)	V850E2/ML4 CPU Board R0K0F4022C000BR User's Manual	This publication
Installation Manual	Describes how to set up hardware and software	SH726B CPU Board R0K5726B0C000BR Installation Manual	R20UT0603JJ

The following documents apply to the V850E2/ML4 . Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics website.

Document Type	Description	Document Title	Document No.
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to application notes for details on using peripheral functions	V850E2/ML4 User's manual: Hardware	R01UH0262EJ
User's manual: Architecture	Description of CPU instruction set	V850E2M User's manual: Architecture	R01US0001EJ
Application note	Applications, sample programs	Available from the Renesas Electronics website.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Frequently Used Abbreviations and Acronyms

ACIA	Asynchronous Communication Interface Adapter
bps	Bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Registers
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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1. Overview

1.1 Overview

The V850E2/ML4 CPU Board R0K0F4022C000BR (hereinafter called the “R0K0F4022C000BR”) is the evaluation board designed to evaluate features and performance of the V850E2/ML4 of Renesas Electronics 32-bit single chip microcontroller and to conduct development and evaluation for its application software. The features of the R0K0F4022C000BR are described below.

1.1.1 Features of the R0K0F4022C000BR

- Usually includes a 16MB SDRAM (16-bit bus connect) and an 8KB EEPROM as external memories.
- Usually includes a serial port connector (RS-232C), a USB connector, an ETHERNET connector, and a CAN connector as peripheral interfaces of the V850E2/ML4.
- The USB connector normally equips a Series A-receptacle to evaluate the USB host controller, and a Series Mini-B receptacle to evaluate the USB function controller.
- The data bus, the address bus and the pins of peripheral functions of the V850E2/ML4 are connected to the expansion connector to enable timing evaluation with the peripheral devices using measurement hardware, and development of expansion boards for the development purpose.
- Enables to evaluate the debugging with Renesas Electronics On-chip Debugging Emulator E1 (14-pin connector).

1.2 System Configuration

Figure 1.1 shows the system configuration with the R0K0F4022C000BR.

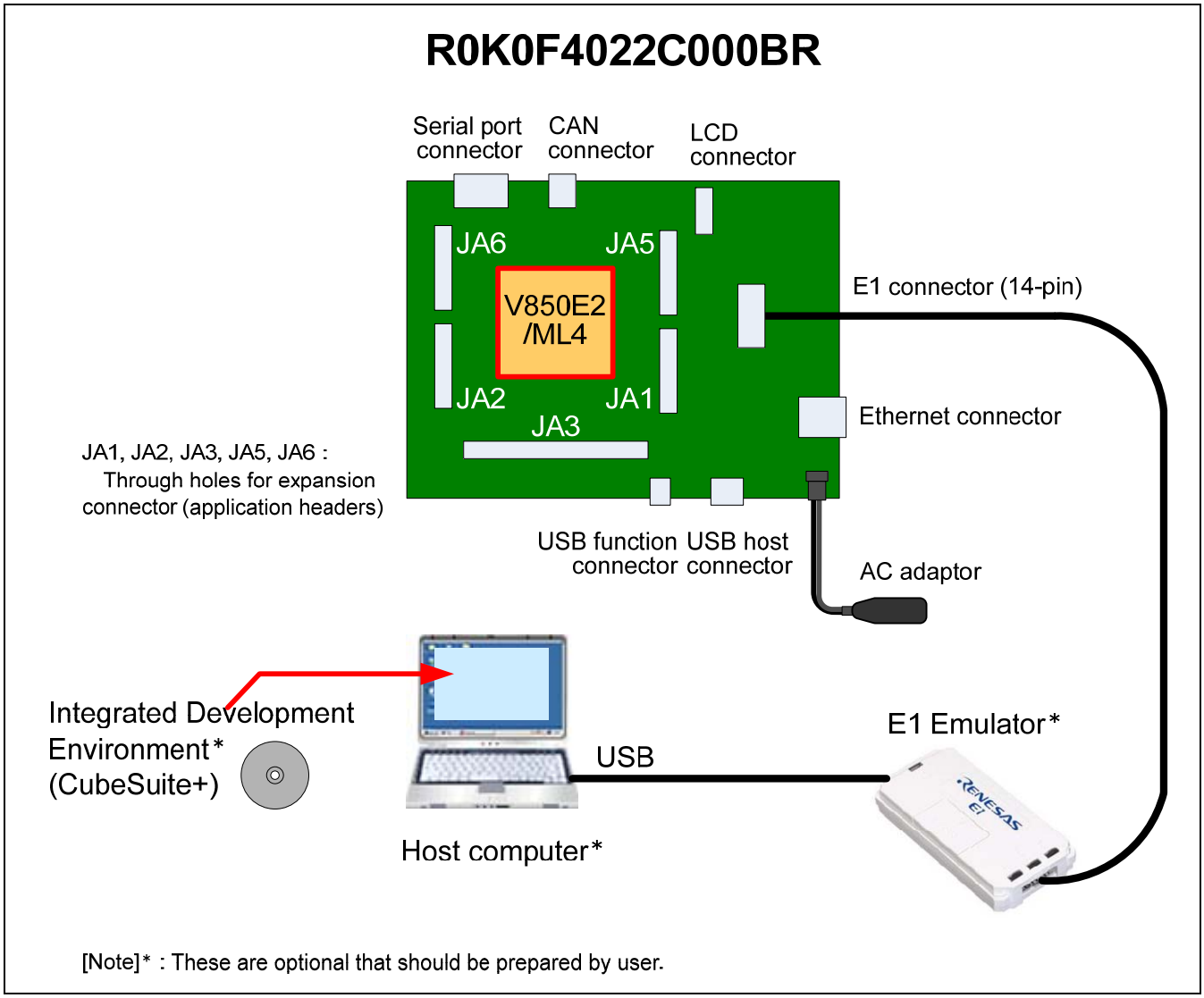

Figure 1.1 System Configuration

1.3 External Specifications

Table 1.1 lists the external specifications of the R0K0F4022C000BR.

Table 1.1 External Specifications

No.	Item	Description
1	CPU	● V850E2/ML4 • Input (XIN) clock: 10MHz • CPU clock: Up to 200MHz • Memory controller bus (E bus) clock: Up to 66.667MHz (SDRAM interface: Up to 50MHz) • Peripheral bus (P bus) clock: Up to 66.667MHz • On-chip memories -Flash memory: 1MB -On-chip RAM: 64KB -H bus shared memory: 64KB -Flash cache: 16KB • Source voltage: -Internal: 1.2V -I/O: 3.3V (5V external supply when using the AD converter with 5.0V) • Package: 216 pin QFP (0.4mm pitch)
2	External memories	● SDRAM: 16MB (CS4 space) ● EEPROM: 8KB (12C bus interface)
3	Connectors/ Through holes	● Serial port connector (D-sub 9-pin, RS232C) ● CAN connector (3-pin) ● LCD connector (14-pin) ● USB host connector (Series A receptacle) ● USB function connector (Series Mini-B receptacle) ● ETHERNET connector 100Base-T(8-pin, RJ-45) ● E1 connector (14-pin) ● Through holes for the expansion connector (Application header): JA1/JA2 (26 pins for each), JA3 (50 pins), JA5/JA6 (24pins for each)
4	Switches	● Reset switch: 1 ● External interrupt switches: 3 (NMI, INTP1, INTP2) ● Operation mode setting DIP switch: 1 (4/package) ● Users DIP switch: 1 (4/package) ● Ethernet PHY setting DIP switch: 1
5	LED, Potentiometer	● Power LED: 1 ● User LEDs: 4 (connected with the I/O port pins of the V850E2/ML4) ● Ethernet PHY LEDs: 3 ● 10kΩ Potentiometer:1
6	Clock	● Resonator for CPU: 10MHz ● Oscillator for USB: 48MHz ● Resonator for Ethernet PHY: 25MHz
7	Dimensions/ Lamination	● Dimensions: 125mm × 170 mm ● Mounting form: 4 layered double-sided, (thickness:1.6mm) ● Number of boards: 1

1.4 R0K0F4022C000BR Block Diagram

Figure 1.2 shows the R0K0F4022C000BRsystem block diagram.

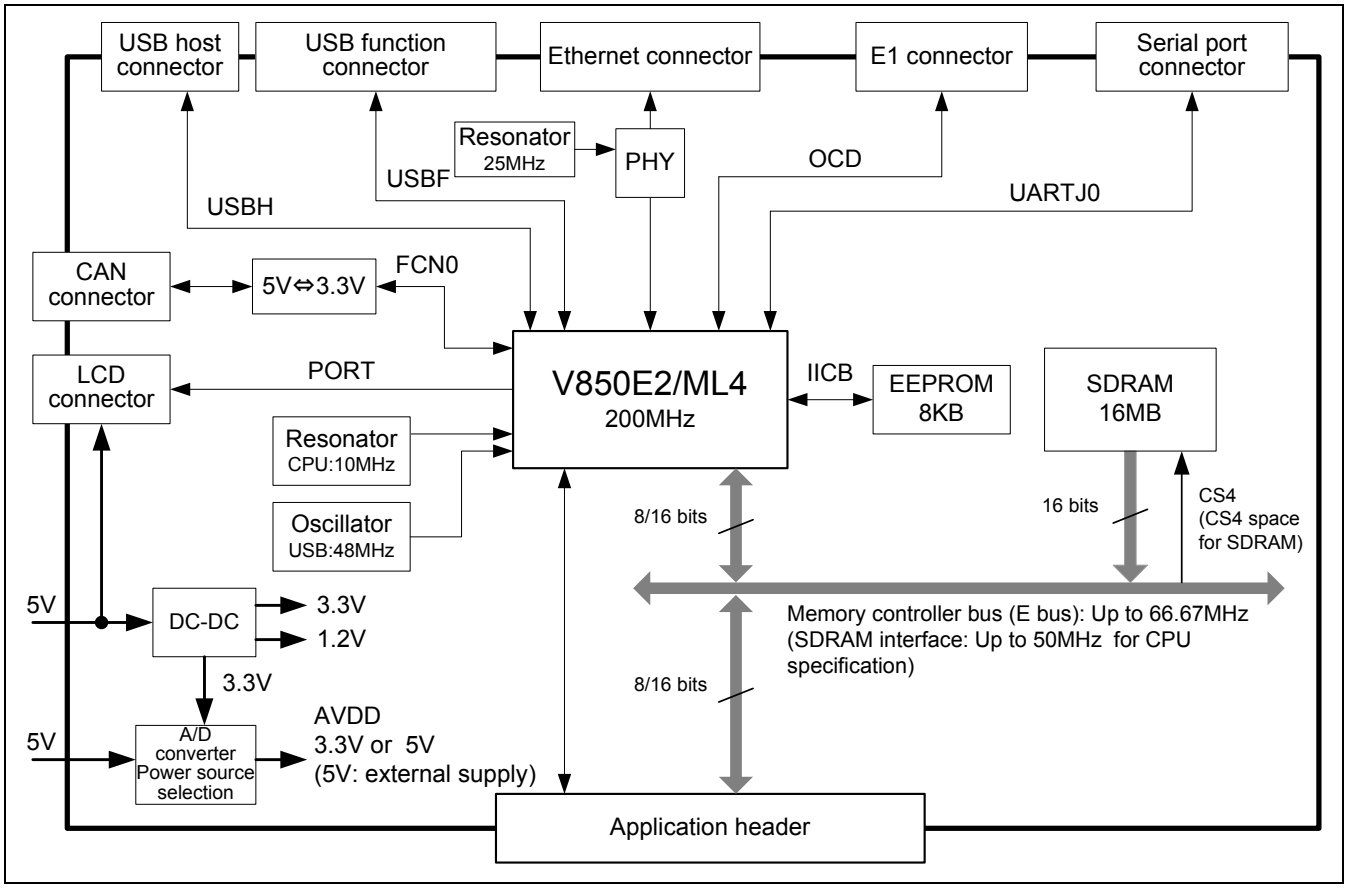

Figure 1.2 System Block Diagram

1.5 Memory Mapping

Figure 1.3 shows the memory mapping on the V850E2/ML4 and the R0K0F4022C000BR.

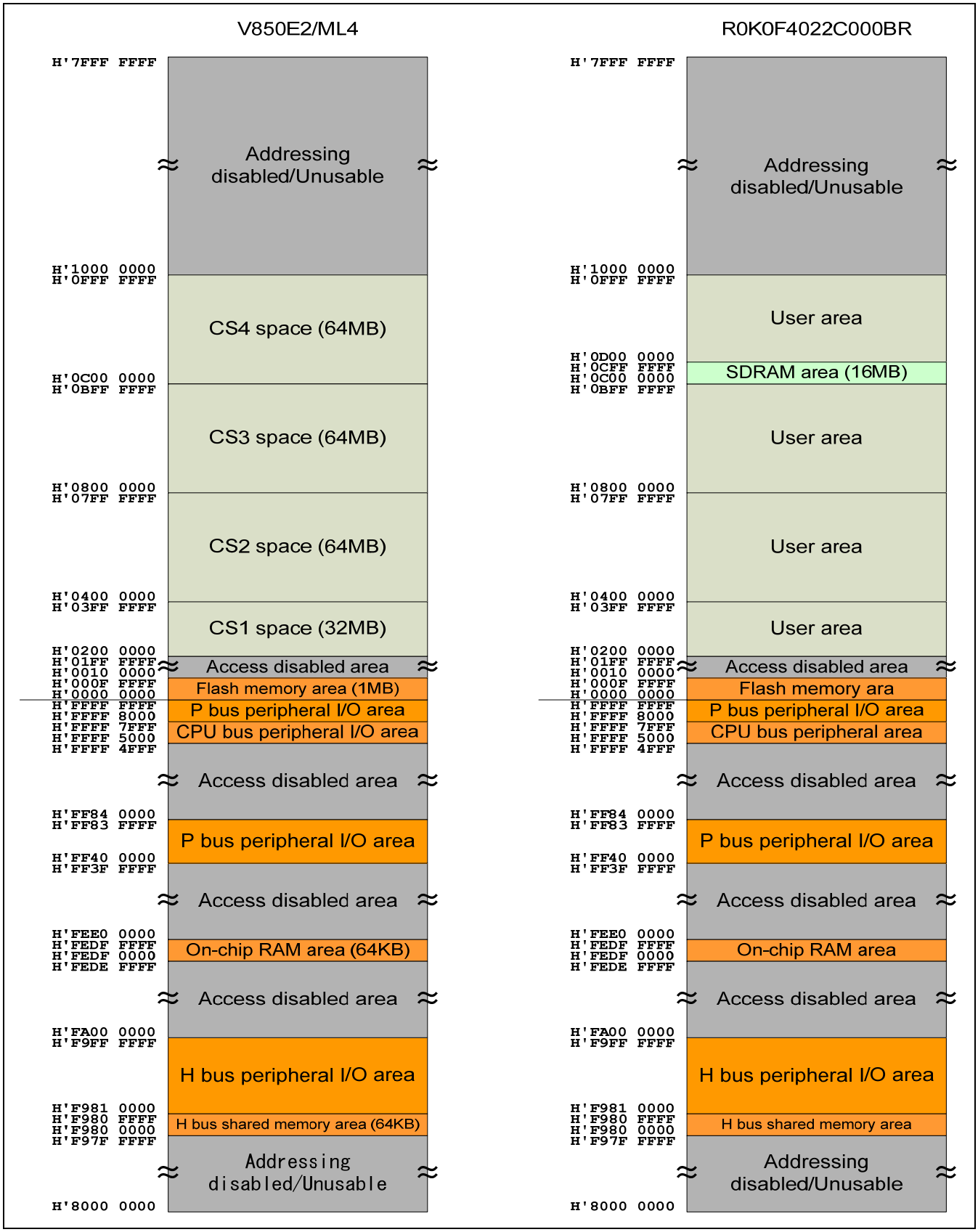

Figure 1.3 Memory Mapping

1.6 Absolute Maximum Rating

Table 1.2 shows the absolute maximum rating on the R0K0F4022C000BR.

Table 1.2 Absolute Maximum Rating

Symbol	Item	Value	Remarks
VCC	5V system power supply voltage	-0.5V to 6.0V	Reference voltage: VSS
3VCC	3.3V system power supply voltage	-0.5V to 4.1V	Reference voltage: VSS (only direct supply)
1.2VCC	1.25V system power supply voltage	-0.5V to 1.6V	Reference voltage: VSS (only direct supply)
T_{opr}	Operating ambient temperature	0C to 50C	Do not expose to condensation or corrosive gases
T_{stg}	Storage ambient temperature	-20C to 60C	Do not expose to condensation or corrosive gases

Note: The ambient temperature is the air temperature immediate to the board.

1.7 Operating Conditions

Table 1.3 lists the operating conditions on the R0K0F4022C000BR.

Table 1.3 Operating Conditions

Symbol	Item	Value	Remarks
VCC	5V system power supply voltage	4.75V to 5.25V	Reference voltage: VSS
-	Maximum consumption voltage on the board	Up to 1.5A	
T_{opr}	Operating ambient temperature	0C to 50C	Do not expose to condensation or corrosive gases

Note: The ambient temperature is the air temperature immediate to the board.

2. Function Specification

2.1 Functions Overview

Table 2.1 lists the R0K0F4022C000BR function modules.

Table 2.1 R0K0F4022C000BR Function modules

Section	Function	Description
2.2	CPU	V850E2/ML4 • Input (XIN) clock: 10MHz • CPU clock: Up to 200MHz • Memory contoroller bus (E bus) clock: Up to 66.667MHz (SDRAM Interface: Up to 50MHz) • Perepheral bus (P bus) clock: Up to 66.667MHz • Internal memory: - Flash memory: 1MB - Internal RAM: 64KB - H bus shared memory: 64KB - Flash cache: 16KB
2.3	External Memory	• SDRAM: 16MB (CS4 space) • EEPROM: 8KB (I2C bus interface)
2.4	I/O Ports	Connects the V850E2/ML4bus and I/O port to the application header
2.5	Serial Port Interface	Connects the V850E2/ML4 UARTJ0 signal to the serial port connector
2.6	CAN Interface	Connects the V850E2/ML4 CAN signal to the CAN connector via the CAN transceiver
2.7	LCD Interface	Character LCD interface
2.8	USB Interface	Connects the V850E2/ML4 USB signal to the USB connector
2.9	Ethernet Interface	Connects the V850E2/ML4 Ethernet MAC signal to the Ethernet connector via the PHY
2.10	Emulator Interface	Connects the V850E2/ML4 OCD signal to the E1 connector (14-pin) Enables debug evaluation with the E1 emulator
2.11	Switches	• User DIP swich: 1 (4/package) • Operation mode setting DIP switch: 1 (4/package) • External interrupt swiches: 3 (NMI, INTP1, and INTP2) • Reset swich: 1 • Ethernet PHY Setting DIP switch: 1 (8/package)
2.12	LEDs and Potentiometer	• User LEDs: 4 • USB host bus LED: 1 • Ethernet PHY LEDs: 3 • Power LED: 1 • 10kΩ Potentiometer: 1
2.13	Power Module	Controls the R0K0F4022C000BR system power supply
2.14	Clock Module	• Resonator for CPU: 10MHz • Oscillator for USB: 48MHz • Resonator for Ethernet PHY: 25MHz）
2.15	Reset Module	Executes reset control of the device which mounted in theR0K0F4022C000BR
—	Operating specifications	Refer to Chapter 3 for details on connectors, jumpers, switches, LEDs, and potentiometer.

2.2 CPU

The R0K0F4022C000BR includes the V850E2/ML4, the 32-bit RISK microcontroller, which operates with a maximum CPU clock of 200MHz and a maximum peripheral clock of 66.667MHz. The V850E2/ML4 is the microcontroller which has 1 MB of flash memory, 64 KB of RAM, and 64 KB of H bus shared memory to support various applications such as data processing and equipment control

Figure 2.1 shows the block diagram on the V850E2/ML4. The unused pins on the R0K0F4022C000BR are not listed.

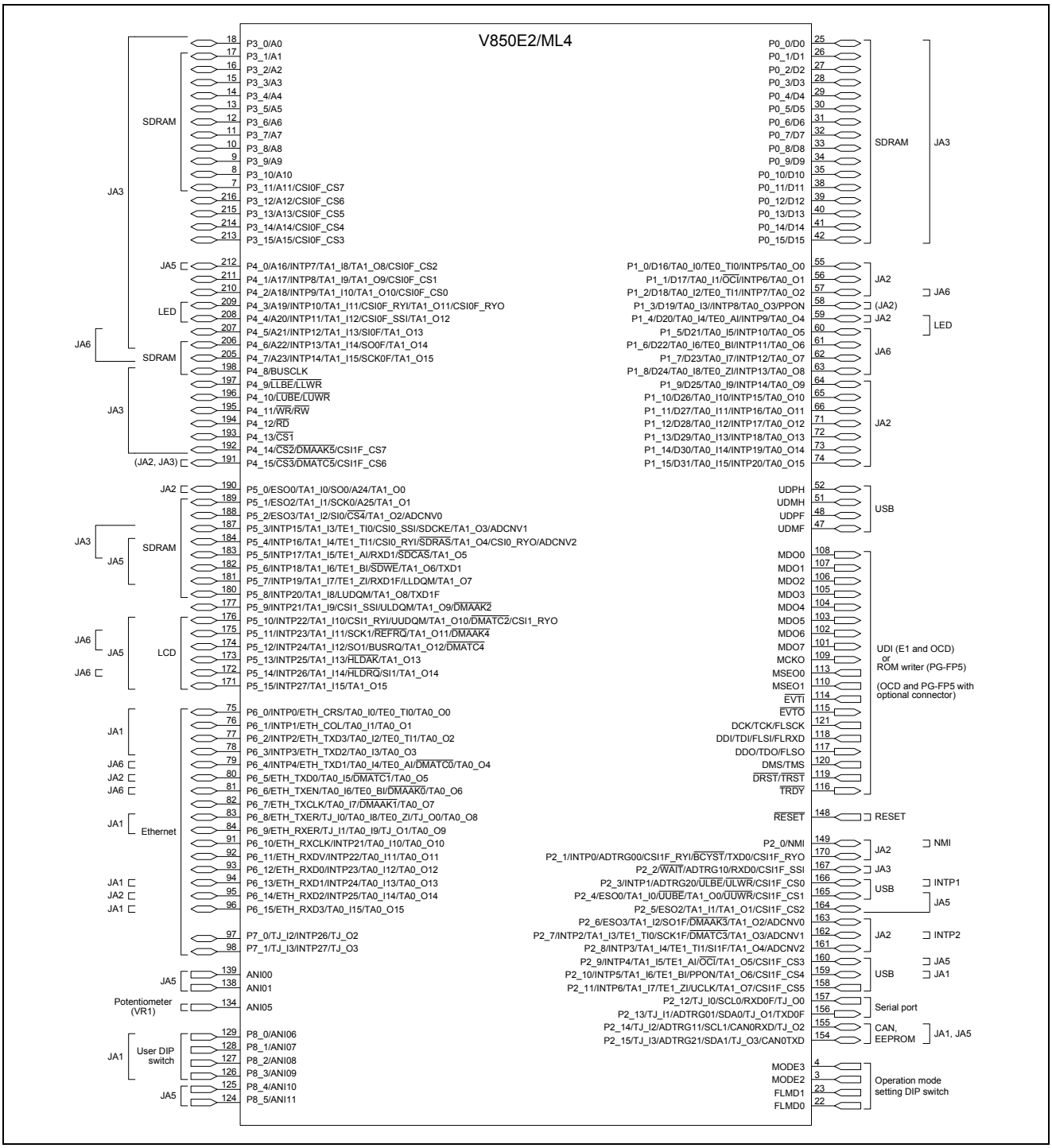

Figure 2.1 V850E2/ML4 Block Diagram

2.3 External Memory

2.3.1 SDRAM

The R0K0F4022C000BR includes 16-MB SDRAM (2-Mword x 16-bit x 4-bank), which is controlled by the V850E2/ML4 memory controller $\overline{CS4}$. The pins used for SDRAM control are also connected to the application headers (JA3, JA5 and JA6) as pins related to bus, pins related to the SCI and pins related to timer respectively. These pins cannot be used to avoid overlaps. Uninstall the $\overline{CS4}$ jumper (JP11) when using the application headers.
Figure 2.2 shows the circuit configuration for the connection between the V850E2/ML4 and the SDRAM.

Note: The items of rising and falling of the bus clock do not satisfy with the requirement specification for the SDRAM on the R0K0F4022C000BR. Only the R0K0F4022C000BR which have no operational problem are delivered. We do not guarantee operation of the R0K0F4022C000BR when users apply it to their system. Users should carefully execute evaluation on their system and determine its applicability.

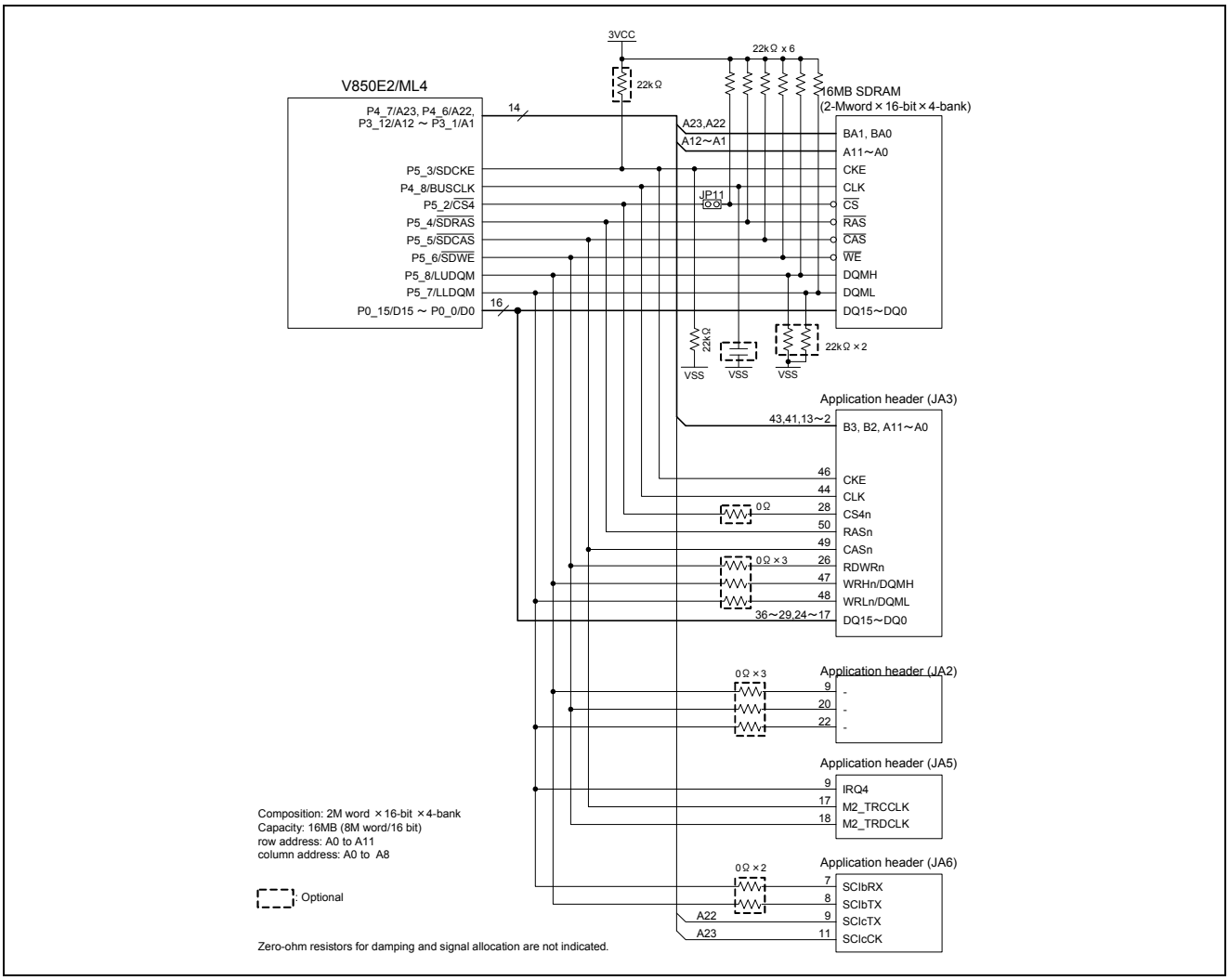

Figure 2.2 Circuit Configuration of SDRAM

2.3.2 EEPROM

The R0K0F4022C000BR includes the 8-KB EEPROM (8-Kword x 8-bit), which is controlled by the I2C bus (IICB) interface mounted in the V850E2/ML4. The IICB signal is multiplexed with the CAN signal, therefore the EEPROM is not available when the CAN connector is in use. Install the jumper (JP8 and JP10) in appropriate pin to use.
Figure 2.3 shows the circuit configuration of the V850E2/ML4 and the EEPROM.

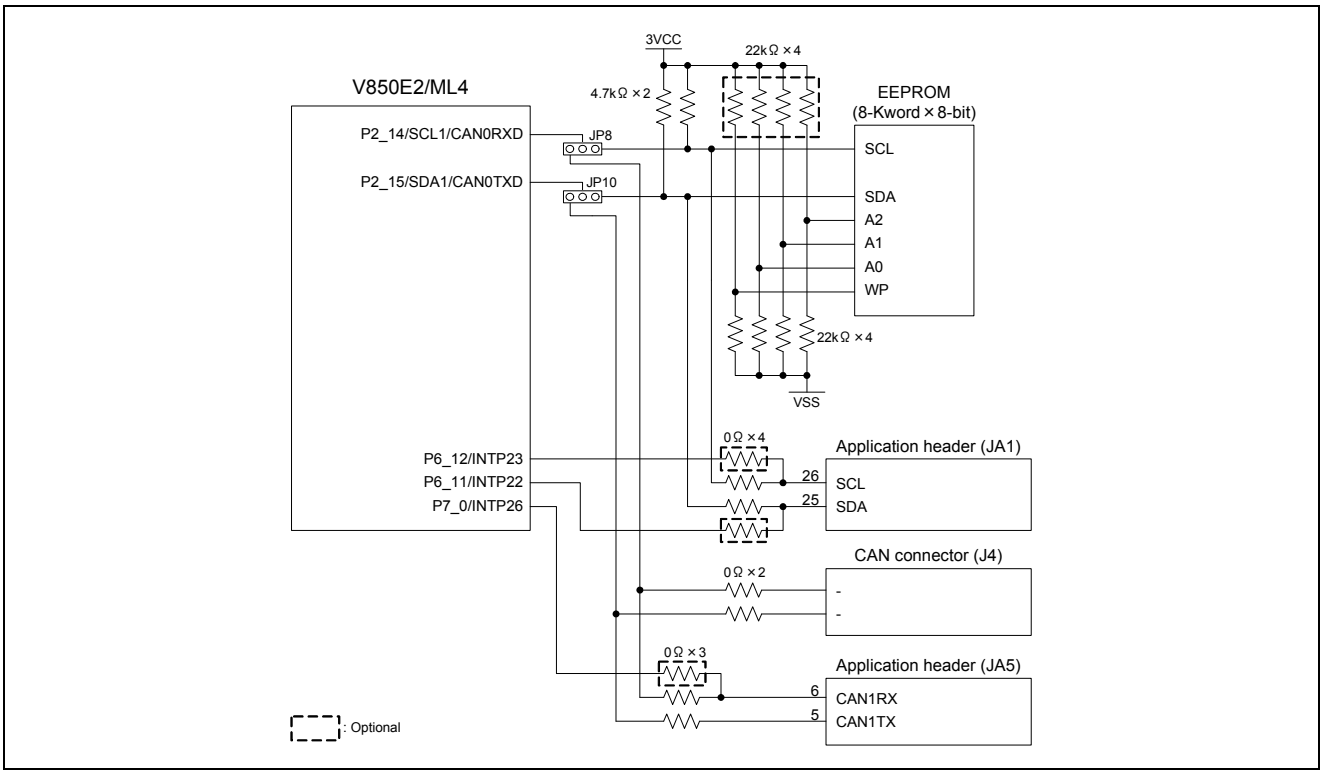

Figure 2.3 Circuit Configuration of EEPROM

2.4 I/O Ports

On the R0K0F4022C000BR, the V850E2/ML4 I/O ports are connected to the application headers. Table 2.1 to Table 2.6 list the I/O port functions. The unused pins on the R0K0F4022C000BR are not listed. Some of the I/O ports are connected to devices, I/O connectors, switches and LEDs on the board. Refer to Chapter 3 Operational Specification for details.

Table 2.2 I/O Port Functions (1/5)

V850E2/ML4		Application headers					On-board function					
Pin No.	Pin name	JA1	JA2	JA3	JA5	JA6	M	E	U	C_S	LC	S,L,V
3	MODE2											SW2
4	MODE3											SW2
7	P3_11/A11/CSI0F_CS7			12			SD					
8	P3_10/A10			11			SD					
9	P3_9/A9			10			SD					
10	P3_8/A8			9			SD					
11	P3_7/A7			8			SD					
12	P3_6/A6			7			SD					
13	P3_5/A5			6			SD					
14	P3_4/A4			5			SD					
15	P3_3/A3			4			SD					
16	P3_2/A2			3			SD					
17	P3_1/A1			2			SD					
18	P3_0/A0	(13)		1								
22	FLMD0											SW2
23	FLMD1											SW2
25	P0_0/D0			17			SD					
26	P0_1/D1			18			SD					
27	P0_2/D2			19			SD					
28	P0_3/D3			20			SD					
29	P0_4/D4			21			SD					
30	P0_5/D5			22			SD					
31	P0_6/D6			23			SD					
32	P0_7/D7			24			SD					
33	P0_8/D8			29			SD					
34	P0_9/D9			30			SD					
35	P0_10/D10			31			SD					
38	P0_11/D11			32			SD					
39	P0_12/D12			33			SD					
40	P0_13/D13			34			SD					
41	P0_14/D14			35			SD					
42	P0_15/D15			36			SD					

【Notes】 M: On-board memory (SD=SDRAM), E: Ethernet, U: USB, C_S: CAN_Serial, LC:LCD, S,L,V: Switches, LED, Potentiometer

( ): Not connected by default. Connectable at a zero-ohm resistor.

Table 2.3 I/O Port Functions (2/5)

V850E2/ML4		Application headers					Ob-board functions					
Pin No.	Pin name	JA1	JA2	JA3	JA5	JA6	M	E	U	C_S	LC	S,L,V
47	UDMF								F			
48	UDPF								F			
51	UDMH								H			
52	UDPH								H			
55	P1_0/D16/TA0_I0/TE0_TI0/INTP5/TA0_O0		21									
56	P1_1/D17/TA0_I1/$\overline{OCI}$/INTP6/TA0_O1		(15), 19									
57	P1_2/D18/TA0_I2/TE0_TI1/INTP7/TA0_O2		22			14						
58	P1_3/D19/TA0_I3/INTP8/TA0_O3/PPON		(9)									
59	P1_4/D20/TA0_I4/TE0_AI/INTP9/TA0_O4		25									LED0
60	P1_5/D21/TA0_I5/INTP10/TA0_O5					15						LED1
61	P1_6/D22/TA0_I6/TE0_BI/INTP11/TA0_O6		26			16						
62	P1_7/D23/TA0_I7/INTP12/TA0_O7					1						
63	P1_8/D24/TA0_I8/TE0_ZI/INTP13/TA0_O8		(23)			13						
64	P1_9/D25/TA0_I9/INTP14/TA0_O9		11									
65	P1_10/D26/TA0_I10/INTP15/TA0_O10		13									
66	P1_11/D27/TA0_I11/INTP16/TA0_O11		14		(12)							
71	P1_12/D28/TA0_I12/INTP17/TA0_O12		15, (17)									
72	P1_13/D29/TA0_I13/INTP18/TA0_O13		16		(14)							
73	P1_14/D30/TA0_I14/INTP19/TA0_O14	(8)	(15), 17									
74	P1_15/D31/TA0_I15/INTP20/TA0_O15		18		(11)							
75	P6_0/INTP0/ETH_CRS/TA0_I0/TE0_TI0/TA0_O0	15						E				SW7
76	P6_1/INTP1/ETH_COL/TA0_I1/TA0_O1	16						E				
77	P6_2/INTP2/ETH_TXD3/TA0_I2/TE0_TI1/TA0_O2	17						E				
78	P6_3/INTP3/ETH_TXD2/TA0_I3/TA0_O3	18						E				
79	P6_4/INTP4/ETH_TXD1/TA0_I4/TE0_AI/$\overline{DMATC0}$/TA0_O4					3		E				
80	P6_5/ETH_TXD0/TA0_I5/$\overline{DMATC1}$/TA0_O5		20					E				
81	P6_6/ETH_TXEN/TA0_I6/TE0_BI/$\overline{DMAAK0}$/TA0_O6					2		E				
82	P6_7/ETH_TXCLK/TA0_I7/$\overline{DMAAK1}$/TA0_O7							E				SW7
83	P6_8/ETH_TXER/TJ_I0/TA0_I8/TE0_ZI/TJ_O0/TA0_O8	19						E				
84	P6_9/ETH_RXER/TJ_I1/TA0_I9/TJ_O1/TA0_O9	20						E				SW7
91	P6_10/ETH_RXCLK/INTP21/TA0_I10/TA0_O10							E				SW7
92	P6_11/ETH_RXDV/INTP22/TA0_I11/TA0_O11	(25)						E				
93	P6_12/ETH_RXD0/INTP23/TA0_I12/TA0_O12	(26)						E				SW7

【Notes】 M: On-board memory (SD=SDRAM), E: Ethernet, U: USB, C_S: CAN_Serial, LC:LCD, S,L,V: Switches, LED, Potentiometer

( ): Not connected by default. Connectable at a zero-ohm resistor.

Table 2.4 I/O Port Functions (3/5)

V850E2/ML4		Application headers					On-board functions					
Pin No.	Pin name	JA1	JA2	JA3	JA5	JA6	M	E	U	C_S	LC	S,L,V
94	P6_13/ETH_RXD1/INTP24/TA0_I13/TA0_O13	21						E				
95	P6_14/ETH_RXD2/INTP25/TA0_I14/TA0_O14		7					E				SW7
96	P6_15/ETH_RXD3/TA0_I15/TA0_O15	22						E				SW7
97	P7_0/TJ_I2/INTP26/TJ_O2				(6)			E				
98	P7_1/TJ_I3/INTP27/TJ_O3							E				
124	P8_5/ANI11				2							
125	P8_4/ANI10				1							
126	P8_3/ANI09	12										SW1
127	P8_2/ANI08	11										SW1
128	P8_1/ANI07	10										SW1
129	P8_0/ANI06	9										SW1
134	ANI05											VR1
138	ANI01				4							
139	ANI00				3							
144	X1		(2)									
145	X2											
148	$\overline{\text{RESET}}$		1									
149	P2_0/NMI		3			(17)						SW3
154	P2_15/TJ_I3/ADTRG21/SDA1/TJ_O3/CAN0TXD	25			5		EE			CAN		
155	P2_14/TJ_I2/ADTRG11/SCL1/CAN0RXD/TJ_O2	26			6		EE			CAN		
156	P2_13/TJ_I1/ADTRG01/SDA0/TJ_O1/TXD0F		(6)							UR		
157	P2_12/TJ_I0/SCL0/RXD0F/TJ_O0		(8)							UR		
158	P2_11/INTP6/TA1_I7/TE1_ZI0/UCLK/TA1_O7/CSI1F_CS5								HF			
159	P2_10/INTP5/TA1_I6/TE1_BI/PPON/TA1_O6/CSI1F_CS4	23							H			
160	P2_9/INTP4/TA1_I5/TE1_AI/$\overline{\text{OCI}}$/TA1_O5/CSI1F_CS3		(16)		14				H			
161	P2_8/INTP3/TA1_I4/TE1_TI1/SI1F/TA1_O4		8									
162	P2_7/INTP2/TA1_I3/TE1_TI0/SCK1F/$\overline{\text{DMATC3}}$/TA1_O3		10, 23		13							SW5
163	P2_6/ESO3/TA1_I2/SO1F/$\overline{\text{DMAAK3}}$/TA1_O2		6									
164	P2_5/ESO2/TA1_I1/TA1_O1/CSI1F_CS2		(14)		12							
165	P2_4/ESO0/TA1_I0/$\overline{\text{UUBE}}$/TA1_O0/$\overline{\text{UUWR}}$/CSI1F_CS1		(18)		11				F			
166	P2_3/INTP1/ADTRG20/$\overline{\text{ULBE}}$/$\overline{\text{ULWR}}$/CSI1F_CS0	8	9						F			SW4
167	P2_2/$\overline{\text{WAIT}}$/ADTRG10/RXD0/CSI1F_SSI			45		(12)						

【Notes】 M: On-board memory (SD=SDRAM), E: Ethernet, U: USB, C_S: CAN_Serial, LC:LCD, S,L,V: Switches, LED, Potentiometer

( ): Not connected by default. Connectable at a zero-ohm resistor.

Table 2.5 I/O Port Functions (4/5)

V850E2/ML4		Application headers					On-board functions					
Pin No.	Pin name	JA1	JA2	JA3	JA5	JA6	M	E	U	C_S	LC	S,L,V
170	P2_1/INTP0/ADTRG00/CSI1F_RYI/$\overline{\text{BCYST}}$/TXD0/ CSI1F_RYO		12			(9), (13)						
171	P5_15/INTP27/TA1_I15/TA1_O15		(3)		24						LC	
172	P5_14/INTP26/TA1_I14/$\overline{\text{HLDRQ}}$/SI1/TA1_O14	(14)			23	7					LC	
173	P5_13/INTP25/TA1_I13/$\overline{\text{HLDAK}}$/TA1_O13			(39)	22						LC	
174	P5_12/INTP24/TA1_I12/SO1/CPUBUSRQ/TA1_O12/$\overline{\text{DMATC4}}$				21	8					LC	
175	P5_11/INTP23/TA1_I11/SCK1/$\overline{\text{REFRQ}}$/TA1_O11/$\overline{\text{DMAAK4}}$			(38)	20	10					LC	
176	P5_10/INTP22/TA1_I10/CSI1_RYI/UUDQM/TA1_O10/ $\overline{\text{DMATC2}}$/CSI1_RYO	(14)			19						LC	
177	P5_9/INTP21/TA1_I9/CSI1_SSI/ULDQM/TA1_O9/$\overline{\text{DMAAK2}}$	(13)										
180	P5_8/INTP20/TA1_I8/LUDQM/TA1_O8/TXD1F		(9)	(47)		(8)	SD					
181	P5_7/INTP19/TA1_I7/TE1_ZI/RXD1F/LLDQM/TA1_O7		(22)	(48)	9	(7)	SD					
182	P5_6/INTP18/TA1_I6/TE1_BI/$\overline{\text{SDWE}}$/TA1_O6/TXD1		(20)	(26)	18		SD					
183	P5_5/INTP17/TA1_I5/TE1_AI/RXD1/$\overline{\text{SDCAS}}$/TA1_O5			49	17		SD					
184	P5_4/INTP16/TA1_I4/TE1_TI1/CSI0_RYI/$\overline{\text{SDRAS}}$/ TA1_O4/CSI0_RYO			50	10		SD					
187	P5_3/INTP15/TA1_I3/TE1_TI0/CSI0_SSI/SDCKE/TA1_O3			46			SD					
188	P5_2/ESO3/TA1_I2/SI0/$\overline{\text{CS4}}$/TA1_O2			(28)			SD					
189	P5_1/ESO2/TA1_I1/SCK0/A25/TA1_O1			(43)								
190	P5_0/ESO0/TA1_I0/SO0/A24/TA1_O0		24	(42)								
191	P4_15/$\overline{\text{CS3}}$/$\overline{\text{DMATC5}}$/CSI1F_CS06		(10)	(27)								
192	P4_14/$\overline{\text{CS2}}$/$\overline{\text{DMAAK5}}$/CSI1F_CS7		(26)	28, (45)								
193	P4_13/$\overline{\text{CS1}}$			27								
194	P4_12/$\overline{\text{RD}}$			25								
195	P4_11/$\overline{\text{WR}}$/$\overline{\text{RW}}$			26								
196	P4_10/$\overline{\text{LUBE}}$/$\overline{\text{LUWR}}$			47								
197	P4_9/$\overline{\text{LLBE}}$/$\overline{\text{LLWR}}$			48								
198	P4_8/BUSCLK			44			SD					
205	P4_7/A23/INTP14/TA1_I15/SCK0F/TA1_O15		(13)	(41)		11	SD					
206	P4_6/A22/INTP13/TA1_I14/SO0F/TA1_O14		(11)	43		9	SD					
207	P4_5/A21/INTP12/TA1_I13/SI0F/TA1_O13			42		12						
208	P4_4/A20/INTP11/TA1_I12/CSI0F_SSI/TA1_O12			41								LED3
209	P4_3/A19/INTP10/TA1_I11/CSI0F_RYI/TA1_O11/CSI0F_RYO			40								LED2

【Notes】 M: On-board memory (SD=SDRAM), E: Ethernet, U: USB, C_S: CAN_Serial, LC:LCD, S,L,V: Switches, LED, Potentiometer

( ): Not connected by default. Connectable at a zero-ohm resistor.

Table 2.6 I/O Port Functions (5/5)

V850E2/ML4		Application headers					On-board functions					
Pin No.	Pin name	JA1	JA2	JA3	JA5	JA6	M	E	U	C_S	LC	S,L,V
210	P4_2/A18/INTP9/TA1_I10/TA1_O10/CSI0F_CS0			39								
211	P4_1/A17/INTP8/TA1_I9/TA1_O9/CSI0F_CS1			38								
212	P4_0/A16/INTP7/TA1_I8/TA1_O8/CSI0F_CS2			37	15							
213	P3_15/A15/CSI0F_CS3			16								
214	P3_14/A14/CSI0F_CS4			15								
215	P3_13/A13/CSI0F_CS5			14								
216	P3_12/A12/CSI0F_CS6			13			SD					

【Notes】 M: On-board memory (SD=SDRAM), E: Ethernet, U: USB, C_S: CAN_Serial, LC:LCD, S,L,V: Switches, LED, Potentiometer

2.5 Serial Port Interface

On the R0K0F4022C000BR, the V850E2/ML4 UARTJ0 is connected to the serial port connector (J5) via the RS-232C transceiver. Also, pins 5 and 6 of the application header (JA6) can be connected to the serial port connector (J5) via the RS-232C transceiver by installing JP2 and JP5 in appropriate pin. Short-circuit is used for pins 1and 2 of both JP2 and JP5 to connect to the serial port connector (J5). When using the V850E2/ML4 UARTJ0 as the serial port, it cannot be used as the application header.

Figure 2.4 shows the R0K0F4022C000BR serial port block diagram.

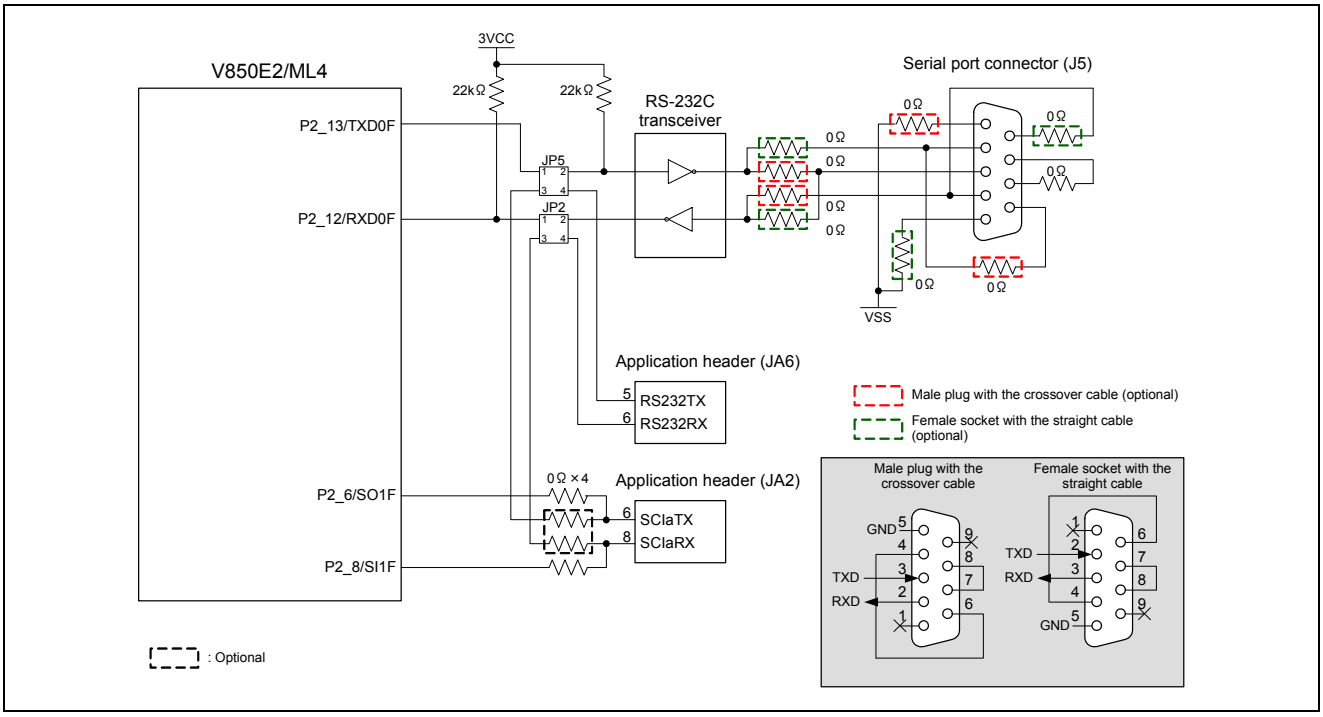

Figure 2.4 Serial Port Block Diagram

2.6 CAN Interface

The R0K0F4022C000BR includes a 3-pin CAN connector (J4). The V850E2/ML4 CAN0TXD is connected to J4 connector via the jumper, a zero-ohm resistor and the CAN transceiver, and the CAN0RXD is connected to J4 connector via the jumper, a zero-ohm resistor and the level shifter and the CAN transceiver. The CAN0TXD and the CAN0RXD are also connected to the application header (JA5). When using the application header (JA5), remove zero-ohm resistors on the CAN connector side. The CAN signals both at the CAN connector and the application header cannot be used.

The V850E2/ML4 SDA1/CAN0TXD and the SCL1/CAN0RXD pins are also connected to the EEPROM and the application header (JA1), and remove or install the jumper to specify the pin function. The CAN connector and the EEPROM cannot be used at the same time. (When storing the Ethernet MAC address to the EEPROM, both the CAN connector and the Ethernet MAC address cannot be accessed at the same time).

Figure 2.5 shows the CAN interface block diagram.

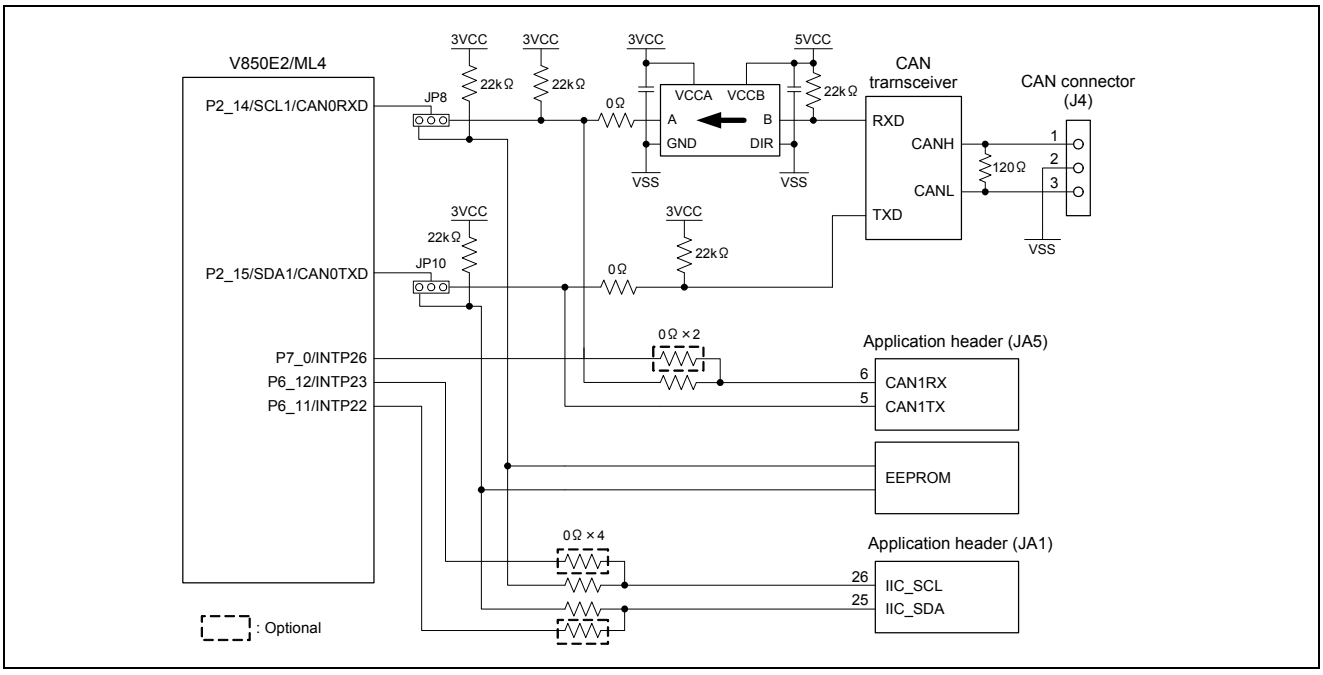

Figure 2.5 CAN Interface Block Diagram

2.7 LCD Interface

The R0K0F4022C000BR includes a 14-pin character LCD connector (J6). The V850E2/ML4 P5_10 to P5_15 control the character LCD. The signals are connected to the application headers (JA5 and JA6) as timer and SCI signals. The functions of these application headers are not available when using the LCD connector. Remove the LCD connector to use the application headers.

Figure 2.6 shows the character LCD interface block diagram.

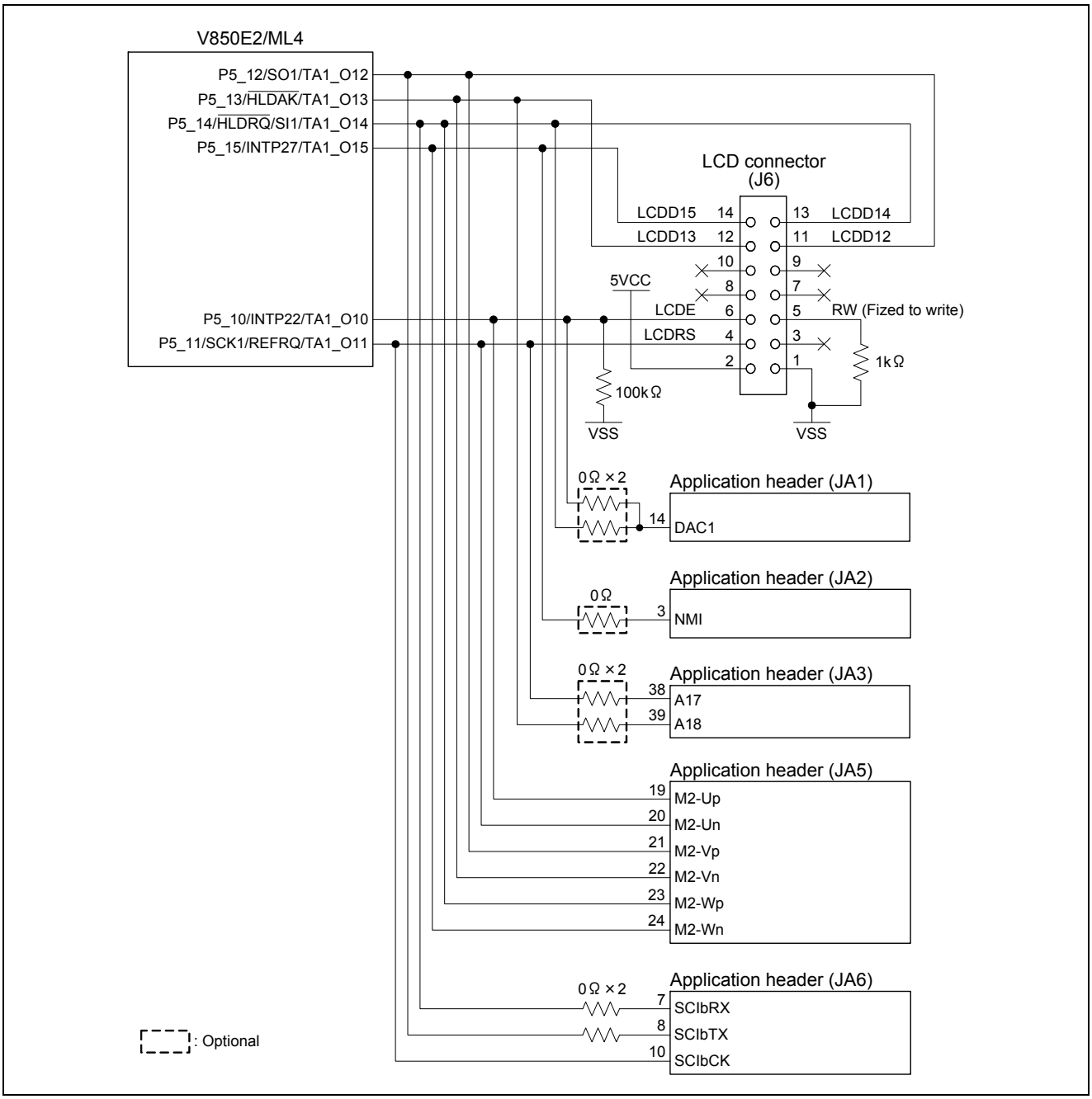

Figure 2.6 Character LCD Interface Block Diagram

2.8 USB Interface

The R0K0F4022C000BR includes the USB host connector (series A-receptacle, J1) and USB function connector (series Mini-B receptacle, J3). The V850E2/ML4 USB host bus is connected to the series A-receptacle, and the $\overline{OCI}$ and PPON are connected to the USB host bus switch. The $\overline{OCI}$ signal is connected to the application header (JA5) as port and timer signals, which can be selected instead of using the USB host bus switch. The PPON signal is connected to the application header (JA1) as IRQ signal, which can be selected instead of using the USB host bus switch. The V850E2/ML4 USB function bus is connected to the series Mini-B receptacle, and P2_4 and INTP1 are used to control the USB function. The P2_4 and the INTP1 are also connected to the application headers (JA1, JA2, and JA5), which can be selected instead of using the series Mini-B receptacle.
Figure 2.7 shows the USB interface block diagram.

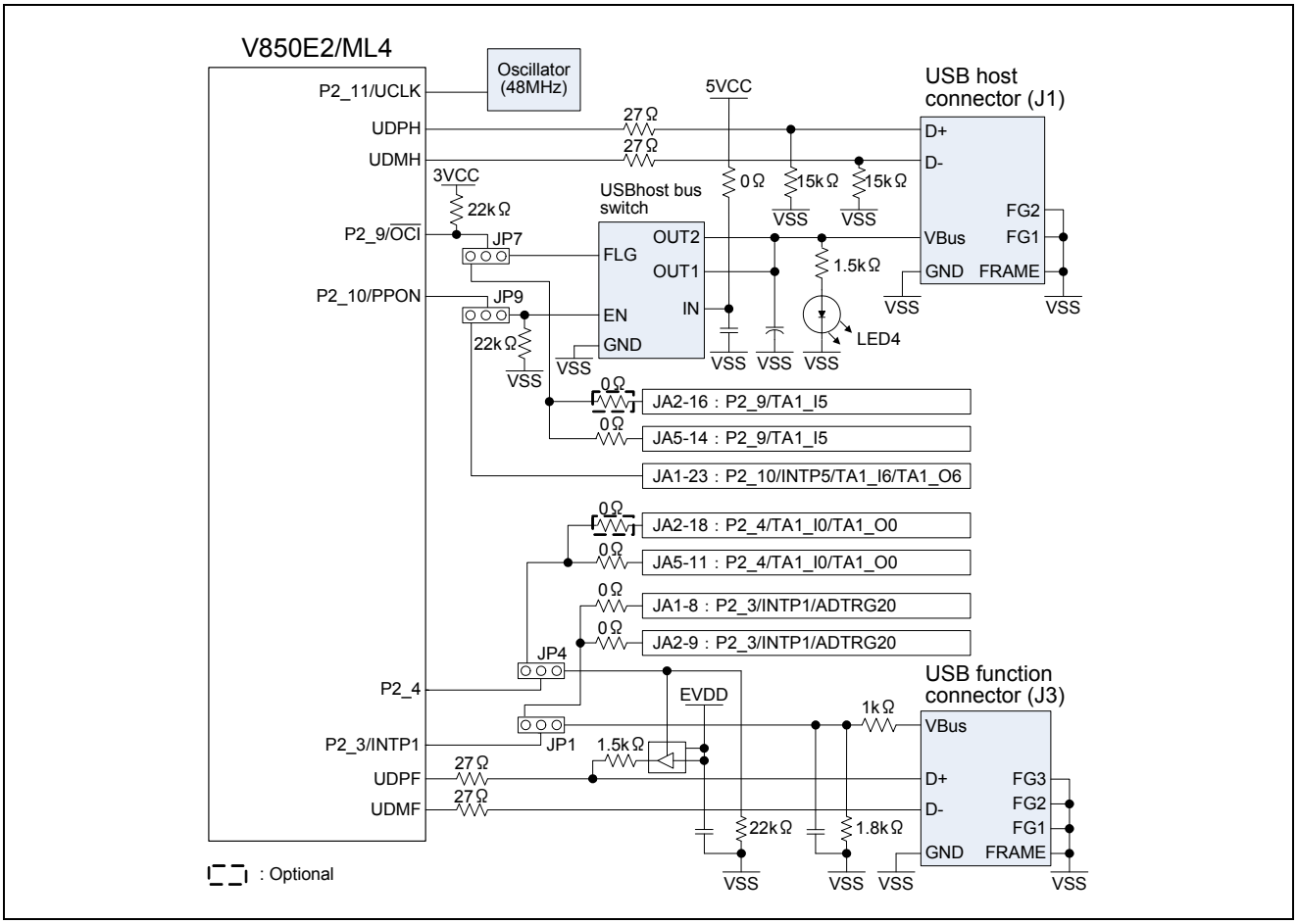

Figure 2.7 USB Interface Block Diagram

2.9 Ethernet Interface

The R0K0F4022C000BR includes the Ethernet connector (J2) via PHY. The V850E2/ML4 Ethernet-related signals are connected to the application headers (JA1, JA2 and JA6) as port signals. When using the Ethernet-related signals as port signal of JA1, remove the zero-ohm resistor (R261) and the 22-ohm resistors between JA1-15, 16, and 20 to 22 and the PHY (R61, R258, R259, R68 and R70 respectively), and install a 22-ohm resistor at R276. When pull-ups and pull-downs are required for the signals of JA1-17 to 19, use the resistor with up to 10k ohms.

The MAC address can be stored in the EEPROM of the R0K0F4022C000BR. When storing the MAC address in the EEPROM, the CAN cannot be use.

Figure 2.8 shows the Ethernet interface block diagram.

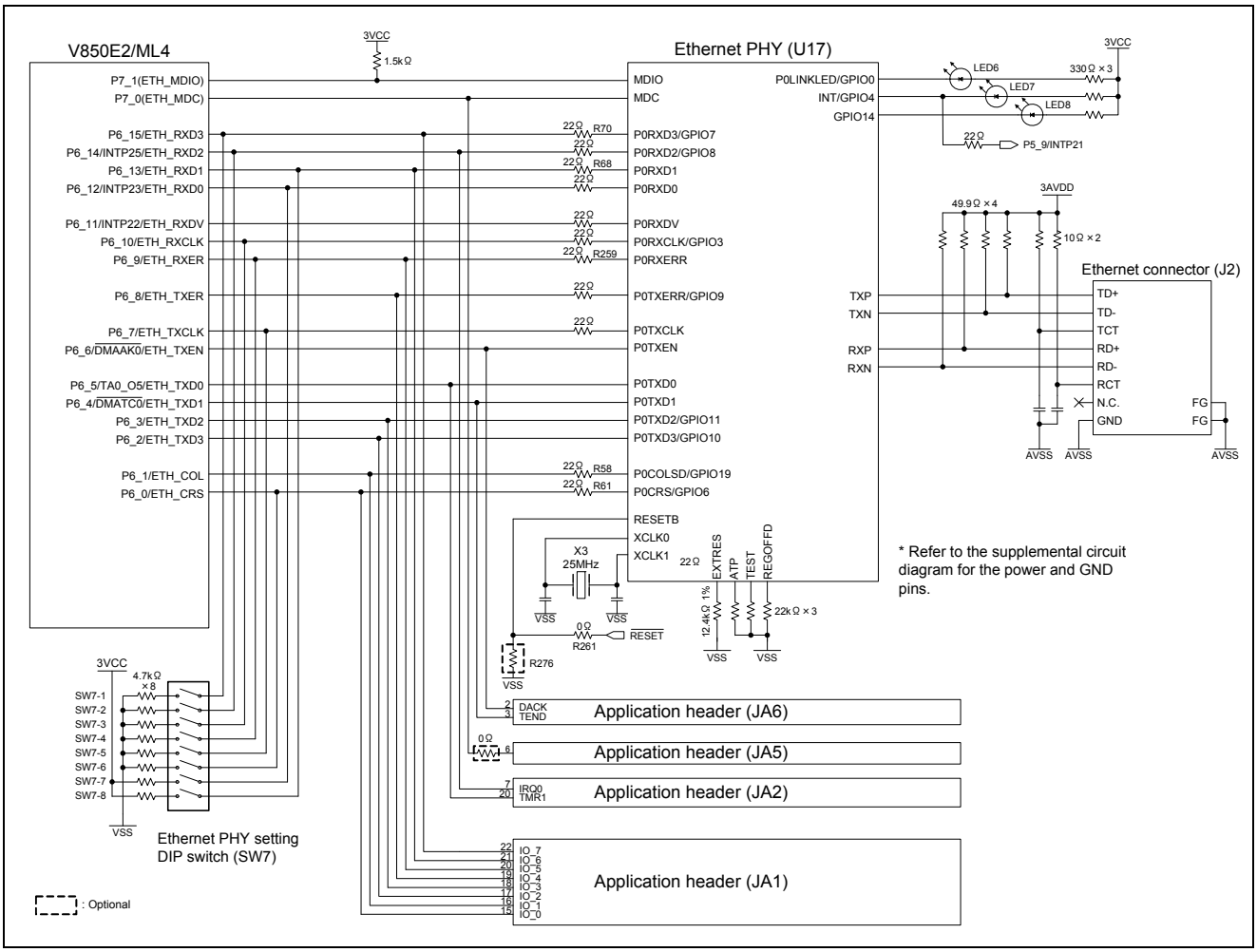

Figure 2.8 Ethernet Interface Block Diagram

2.10 Emulator Interface

The R0K0F4022C000BR includes 14-pin E1 connector (J10) to connect to the emulator, and enables to connect to the E1 emulator.

Figure 2.9 shows the E1 connector block diagram.

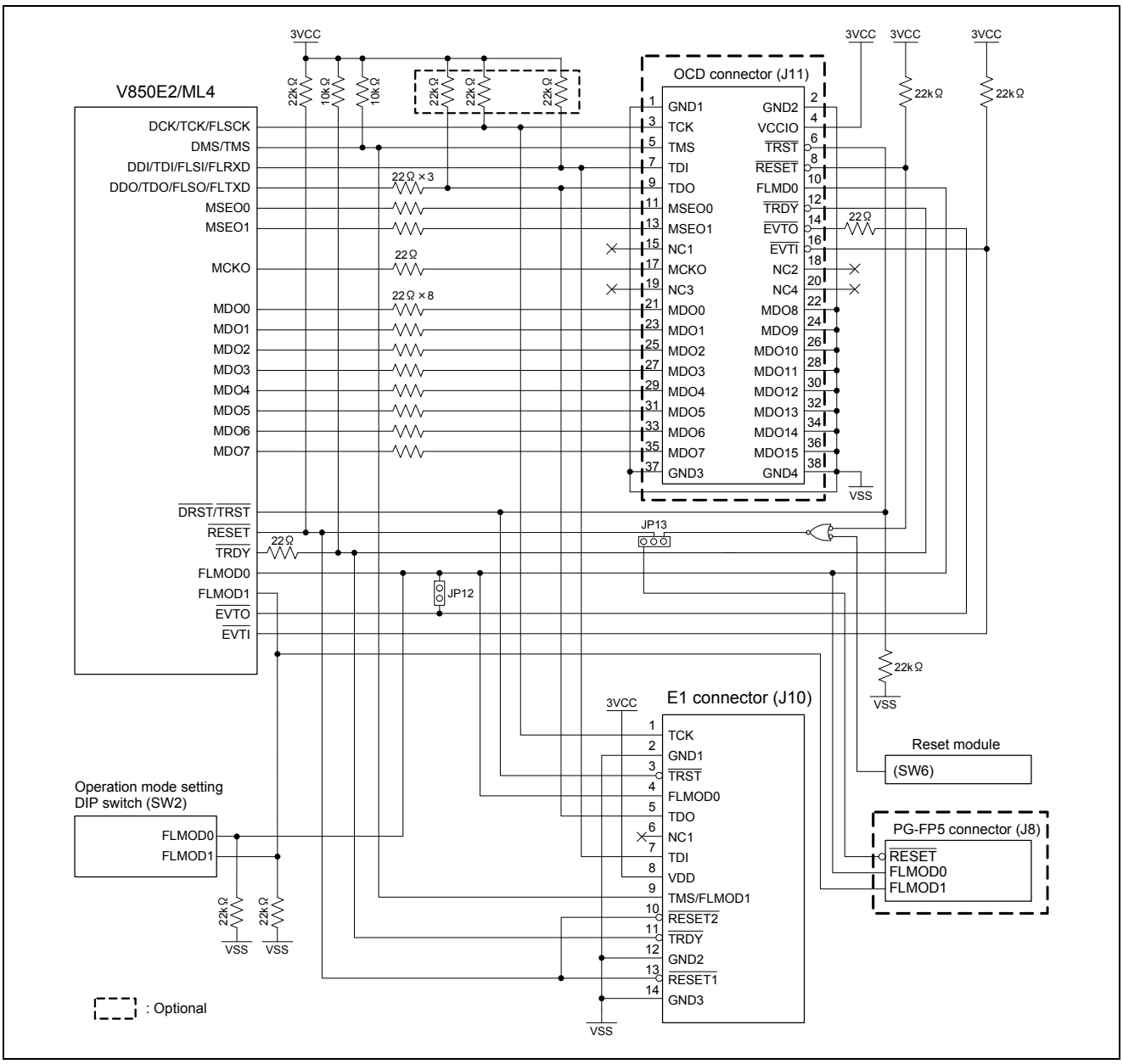

Figure 2.9 E1 Connector Block Diagram

2.11 Switches

The R0K0F4022C000BR includes push switches for reset, external interrupts (NMI, INTP1 and INTP2) and $\overline{\text{ADTRG}}$ input, and DIP switches for users, operation mode setting and Ethernet PHY. The user DIP switch is connected to P8_0 to P8_3. The operation mode setting DIP switch executes settings for the V850E2/ML4 FLMD0, FLMD1, MODE2 and MODE3 signals. Refer to Figure 2.11 for these DIP switches, and Figure 2.8 for the Ethernet PHY DIP switch.
Figure 2.10 shows the push switch block diagram related to the external interrupt input.

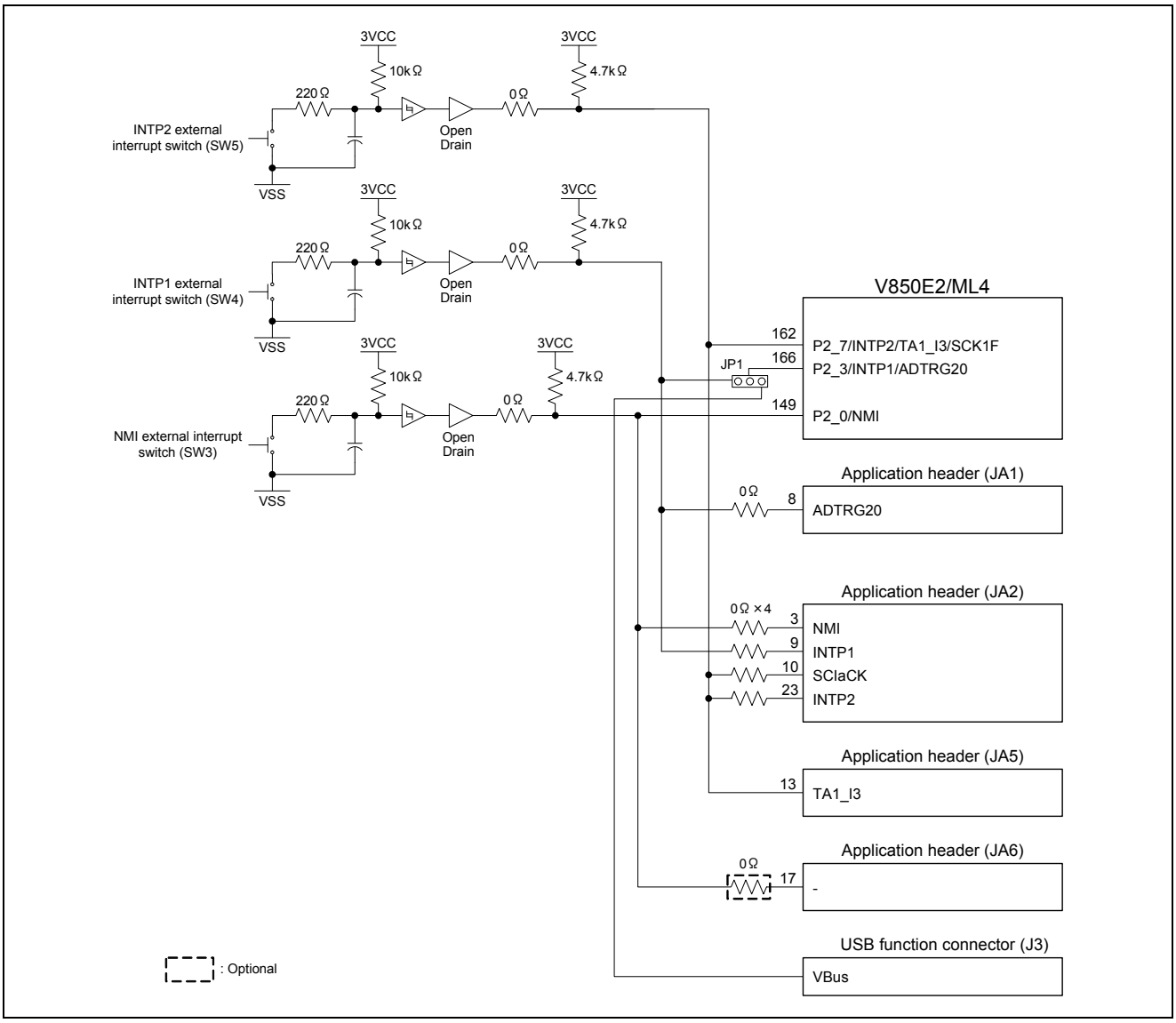

Figure 2.10 Push Switch Block Diagram

2.12 LEDs and Potentiometer

The R0K0F4022C000BR includes four user LEDs (LED0 to LED3), a USB host bus LED (LED4), three Ethernet PHY LEDs (LED6 to LED8), and a power LED (LED9). The user LEDs are controlled by the V850E2/ML4 P1_4, P1_5, P4_3 and P4_4. The R0K0F4022C000BR also includes a potentiometer, which is connected to the ANI05 of the A/D converter.
Figure 2.11 shows LED (user LED) and potentiometer block diagram.

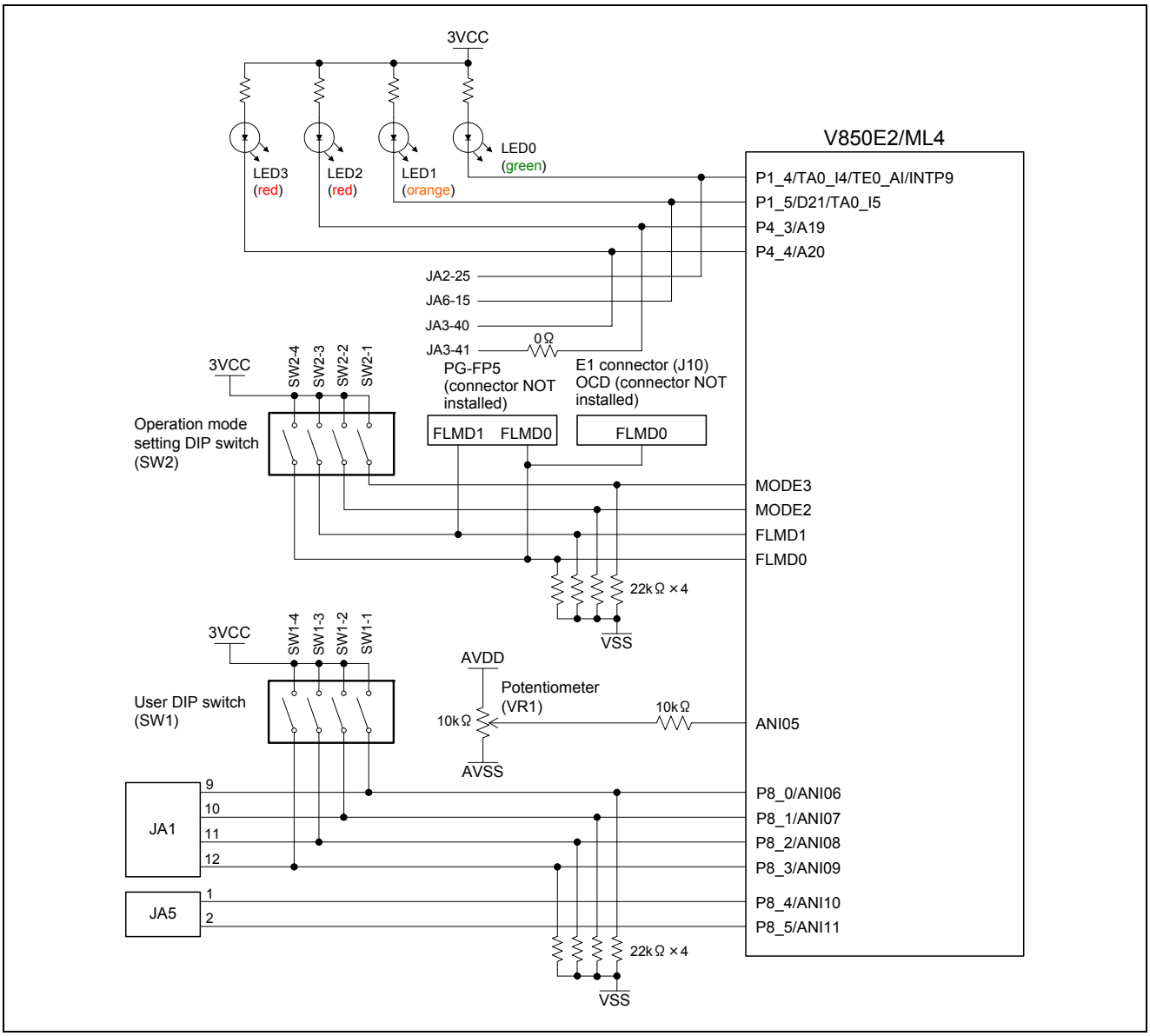

Figure 2.11 LED and Potentiometer Block Diagram

2.13 Power Module

On the R0K0F4022C000BR, a 5V power supply is input to the board to generate 3.3V and 1.2 V using the regulator.
A 3.3V is input to the AVDD, although a 5V can be provided from the external power supply by removing the zero-ohm resistor.
Figure 2.12 show the R0K0F4022C000BR power supply circuit block diagram.

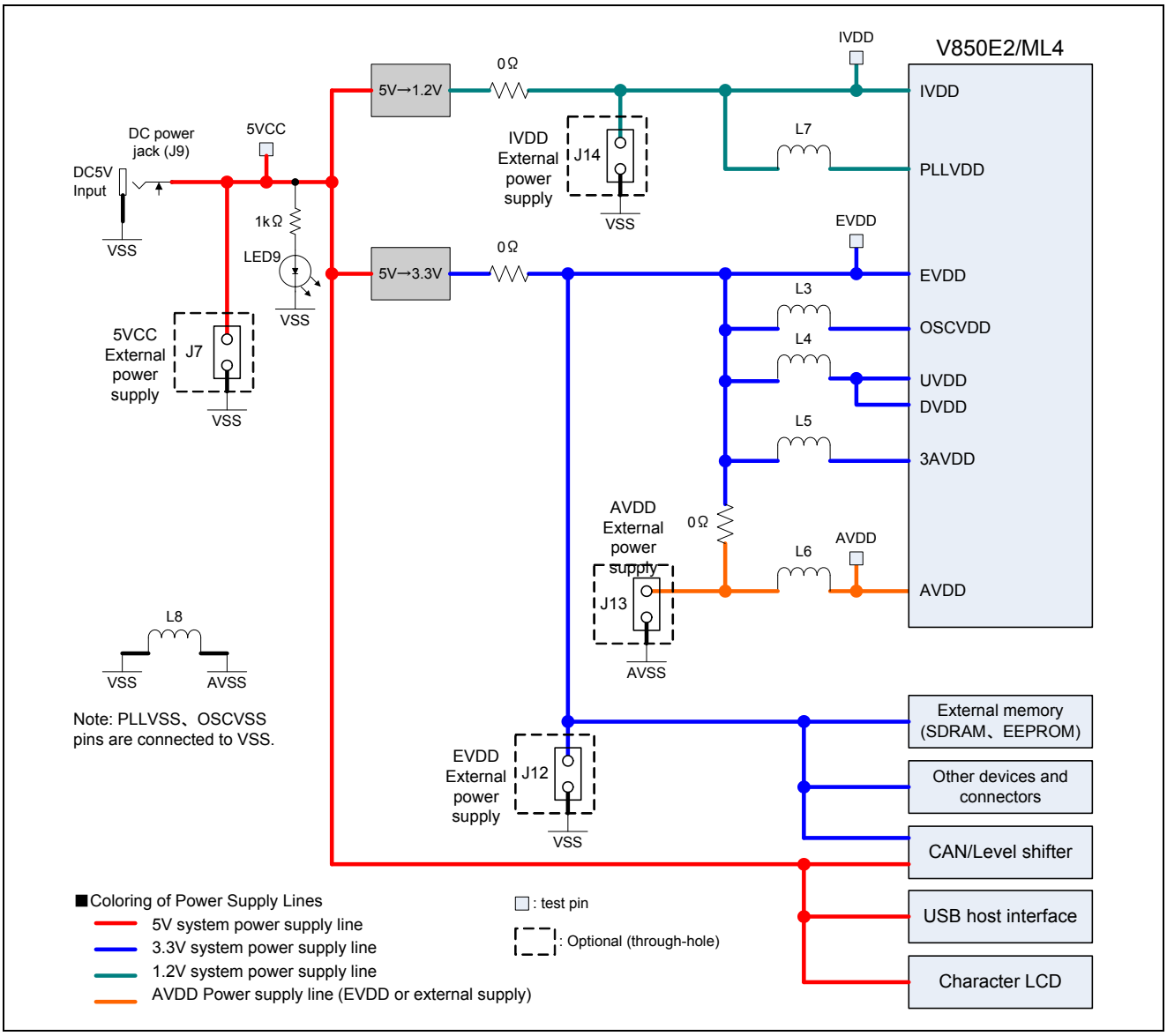

Figure 2.12 Power Supply Circuit Block Diagram

2.14 Clock Module

The R0K0F4022C000BR connects the 10MHz resonator to the V850E2/ML4 X1 and X2 pins, and the 48MHz oscillator to the UCLK pin.

A clock input can be provided to the EXTAL pin via the application header (JA2). In this case, remove the zero-ohm resistor of X1 (R35) and install a zero-ohm (R2, not installed by default). A pull-up resistor (R29) can be installed if needed.

Figure 2.13 shows the R0K0F4022C000BR clock module block diagram.

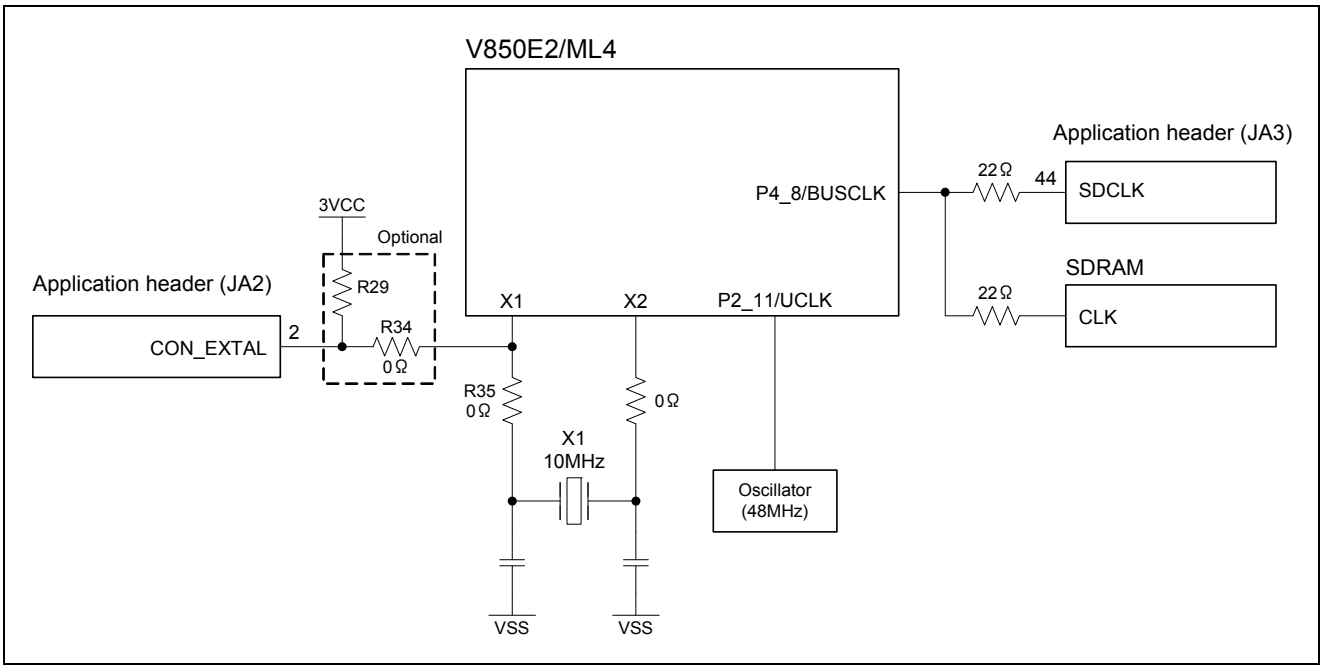

Figure 2.13 Clock Module Block Diagram

2.15 Reset Module

The R0K0F4022C000BR reset module generates $\overline{\text{RESET}}$ signal using the power-on reset and reset switch (SW).
Figure 2.14 shows the R0K0F4022C000BR reset module block diagram.

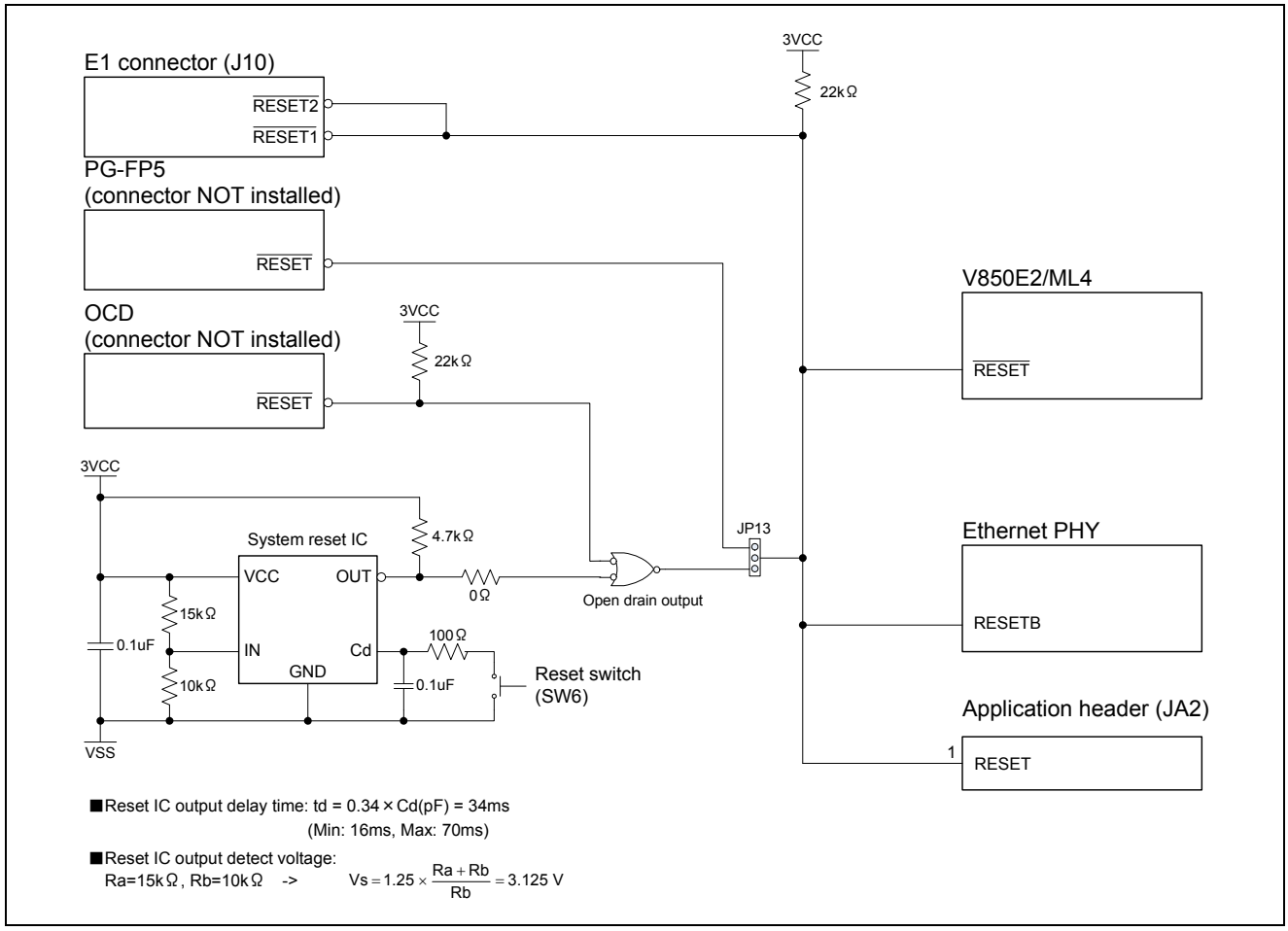

Figure 2.14 Reset Module Block Diagram

3. Operational Specification

3.1 Connector Overview

Figure 3.1 shows the connector assignments for the R0K0F4022C000BR.

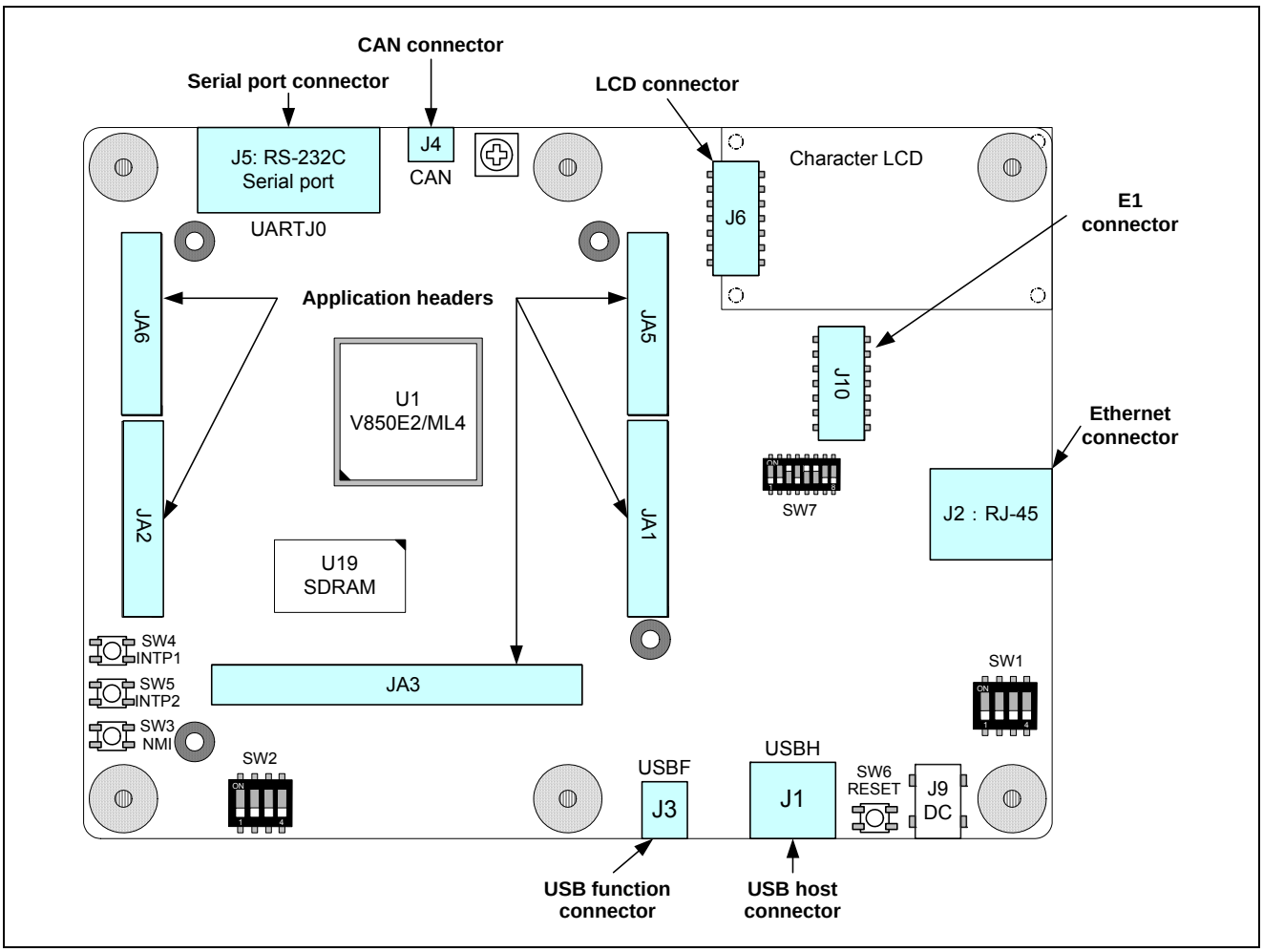

Figure 3.1 R0K0F4022C000BR Connector Assignments

3.1.1 Application Headers (JA1 to JA3, JA5 and JA6)

The R0K0F4022C000BR includes through-holes for mounting application headers (JA1 to JA3, JA5 and JA6) to which the V850E2/ML4 I/O pins are connected. The standard MIL connectors can be implemented to the through-holes to connect an expansion board.

Figure 3.2 shows the pin assignments, and Table 3.1 to Table 3.6 lists the pin descriptions for the application headers (JA1 to JA3, JA5 and JA6).

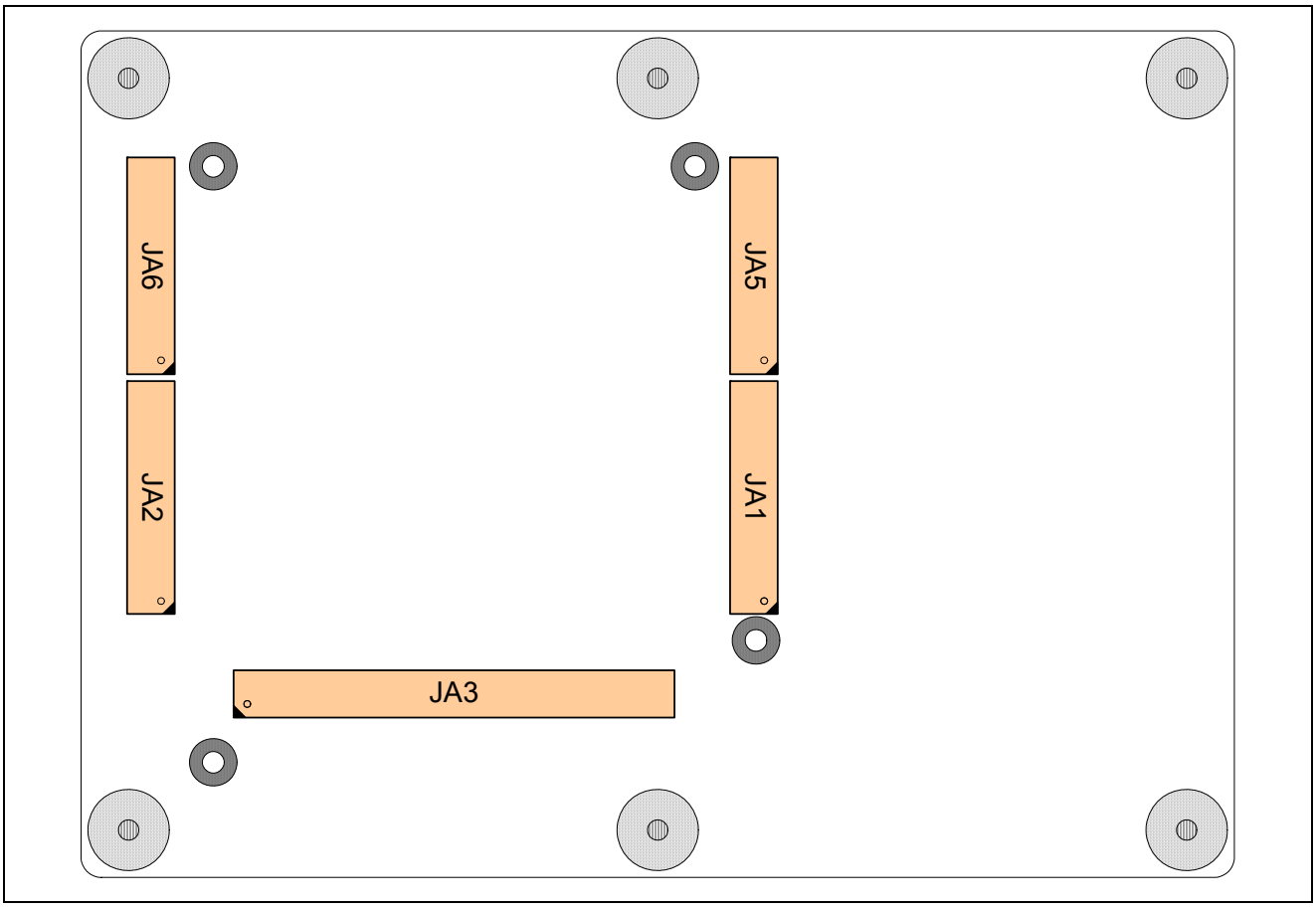

Figure 3.2 Application Header Pin Assignments (JA1 to JA3, JA5 and JA6)

Table 3.1 Application Header (JA1) Pin Descriptions

Pin No.	Signal Name	Signal connected to JA1 by default	Other connection
1	5VCC	5VCC	
2	GND	GND	
3	3VCC	3VCC	
4	GND	GND	
5	AVDD	AVDD	
6	AVSS	AVSS	
7	AVDD	AVDD	
8	P2_3/INTP1/ADTRG20*1, P1_14/TA0_O14*2	P2_3 (JP1-3)	SW4 (INTP1), JA2-9
9	P8_0/ANI06	P8_0	SW1-1
10	P8_1/ANI07	P8_1	SW1-2
11	P8_2/ANI08	P8_2	SW1-3
12	P8_3/ANI09	P8_3	SW1-4
13	P3_0/A0*2, P5_9/INTP21*2	NC	-
14	P5_14/$\overline{\text{HLDRQ}}$/SI1/TA1_O14*2, P5_10/INTP22/TA1_O10*2	NC	-
15	P6_0	P6_0	Ethernet PHY (P0CRS)
16	P6_1	P6_1	Ethernet PHY (P0COLSD)
17	P6_2	P6_2	Ethernet PHY (P0TXD3)
18	P6_3	P6_3	Ethernet PHY (P0TXD2)
19	P6_8	P6_8	Etherne tPHY (P0TXERR)
20	P6_9	P6_9	Ethernet PHY (P0RXERR)
21	P6_13	P6_13	Ethernet PHY (P0RXD1)
22	P6_15	P6_15	Ethernet PHY (P0RXD3)
23	P2_10/INTP5/TA1_I6/TA1_O6	P2_10	USBH
24	NC	NC	-
25	P2_15/SDA1/CAN0TXD*1, P6_11/INTP22*2	P2_15 (JP10-1)	EEPROM (SDA)
26	P2_14/SCL1/CAN0RXD*1, P6_12/INTP23*2	P2_14 (JP8-1)	EEPROM (SCL)

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default) and jumpers.

2.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.2 Application Header (JA2) Pin Descriptions

Pin No.	Signal Name	Signal connected to JA2 by default	Other connection
1	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	Ethernet PHY, E1
2	X1*3	NC	-
3	P2_0/NMI*1, P5_15/INTP27/TA 1 _O15*3	P2_0	SW3 (NMI)
4	GND	GND	-
5	NC	NC	-
6	P2_6/SO1F*1, P2_13/TXD0F*3	P2_6	-
7	P6_14/INTP25/TA0_I14/TA0_O14	P6_14	Ethernet PHY (P0RXD2)
8	P2_8/SI1F*1, P2_12/RXD0F*3	P2_8	-
9	P2_3/INTP1/ADTRG20*2, P1_3/INTP8/TA0_I3/TA0_O3*3, P5_8/LUDQM/TXD1F*3	P2_3 (JP1-3)	SW4 (INTP1), JA1-8
10	P2_7/INTP2/TA1_I3/SCK1F*1, P4_15/$\overline{\text{CS3}}$*3	P2_7	SW5 (INTP2), JA2-23, JA5-13
11	P1_9/TA0_I9/TA0_O9*1, P4_6/A22/SO0F*3	P1_9	-
12	P2_1/CSI1F_RYI/CSI1F_RYO/TXD0	P2_1	-
13	P1_10/TA0_O10*1, P4_7/A23/SCK0F*3	P1_10	-
14	P1_11/TA0_O11*1, P2_5/TA1_I1*3	P1_11	-
15	P1_12/TA0_O12*1, P1_14/TA0_O14*3, P1_1/INTP6/TA0_O1*3	P1_12	-
16	P1_13/TA0_O13*1 P2_9/TA1_I5*3	P1_13	-
17	P1_14/TA0_O14*1 P1_12/TA0_O12*3	P1_14	-
18	P1_15/TA0_O15*1, P2_4/TA1_I0/TA1_O0*3	P1_15	-
19	P1_1/INTP6/TA0_O1	P1_1	-
20	P6_5/TA0_O5*1, P5_6/$\overline{\text{SDWE}}$/TE1_BI*3	P6_5	EtherPHY(P0 TXD0)
21	P1_0/TE0_TI0/INTP5	P1_0	-
22	P1_2/TA0_I2/TE0_TI1*1, P5_7/INTP19/RXD1F/LLDQM*3	P1_2	JA6-14
23	P2_7/INTP2/TA1_I3/SCK1F*1, P1_8/TE0_ZI/INTP13/TA0_I8/TA0_ O8*3	P2_7	SW5(INTP2), JA2-10, JA5-13
24	P5_0/A24/ESO0	P5_0	-
25	P1_4/TA0_I4/TE0_AI/INTP9*1	P1_4	LED0
26	P1_6/D22/TA0_I6/TE0_BI/INTP11*1, P4_14/$\overline{\text{CS2}}$*3	P1_6	JA6-16

Notes: 1.These pins are connected to through-holes via zero-ohm resistors (installed by default).

2.These pins are connected to through-holes via zero-ohm resistors (installed by default) and jumpers.

3.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.3 Application Header (JA3) Pin Descriptions (1/2)

Pin No.	Signal Name	Signal connected to JA3 by default	Other connection
1	P3_0/A0	P3_0	-
2	P3_1/A1	P3_1	SDRAM (A0)
3	P3_2/A2	P3_2	SDRAM (A1)
4	P3_3/A3	P3_3	SDRAM (A2)
5	P3_4/A4	P3_4	SDRAM (A3)
6	P3_5/A5	P3_5	SDRAM (A4)
7	P3_6/A6	P3_6	SDRAM (A5)
8	P3_7/A7	P3_7	SDRAM (A6)
9	P3_8/A8	P3_8	SDRAM (A7)
10	P3_9/A9	P3_9	SDRAM (A8)
11	P3_10/A10	P3_10	SDRAM (A9)
12	P3_11/A11	P3_11	SDRAM (A10)
13	P3_12/A12	P3_12	SDRAM (A11)
14	P3_13/A13	P3_13	-
15	P3_14/A14	P3_14	-
16	P3_15/A15	P3_15	-
17	P0_0/D0	P0_0	SDRAM (DQ0)
18	P0_1/D1	P0_1	SDRAM (DQ1)
19	P0_2/D2	P0_2	SDRAM (DQ2)
20	P0_3/D3	P0_3	SDRAM (DQ3)
21	P0_4/D4	P0_4	SDRAM (DQ4)
22	P0_5/D5	P0_5	SDRAM (DQ5)
23	P0_6/D6	P0_6	SDRAM (DQ6)
24	P0_7/D7	P0_7	SDRAM (DQ7)
25	P4_12/$\overline{RD}$	P4_12	-
26	P4_11/$\overline{WR}$/$\overline{RW}$[*1], P5_6/$\overline{SDWE}$/TE1_BI[*2]	P4_11	-
27	P4_13/$\overline{CS1}$[*1], P4_15/$\overline{CS3}$[*2]	P4_13	-
28	P4_14/$\overline{CS2}$[*1], P5_2/$\overline{CS4}$[*2]	P4_14	-
29	P0_8/D8	P0_8	SDRAM (DQ8)
30	P0_9/D9	P0_9	SDRAM (DQ9)
31	P0_10/D10	P0_10	SDRAM (DQ10)
32	P0_11/D11	P0_11	SDRAM (DQ11)
33	P0_12/D12	P0_12	SDRAM (DQ12)
34	P0_13/D13	P0_13	SDRAM (DQ13)
35	P0_14/D14	P0_14	SDRAM (DQ14)
36	P0_15/D15	P0_15	SDRAM (DQ15)

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).

2.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.4 Application Header (JA3) Pin Descriptions (2/2)

Pin No.	Signal Name	Signal connected to JA3 by default	Other connection
37	P4_0/A16/TA1_O8	P4_0	-
38	P4_1/A17*1, P5_11/SCK1/$\overline{\text{REFRQ}}$/TA1_O11*2	P4_1	-
39	P4_2/A18*1, P5_13/$\overline{\text{HLDAK}}$/TA1_O13*2	P4_2	-
40	P4_3/A19	P4_3	LED2
41	P4_4/A20*1, P4_7/A23/SCK0F*2	P4_4	LED3
42	P4_5/A21/SI0F*1, P5_0/A24/ESO0*2	P4_5	JA6-12
43	P4_6/A22/SO0F*1, P5_1/A25/ESO2*2	P4_6	SDRAM (BA0), JA6-9
44	P4_8/BUSCLK	P4_8	SDRAM (CLK)
45	P2_2/$\overline{\text{WAIT}}$/RXD0*1, P4_14/$\overline{\text{CS2}}$*2	P2_2	-
46	P5_3/TA1_O3/SDCKE	P5_3	SDRAM (CKE)
47	P4_10/$\overline{\text{LUWR}}$*1, P5_8/LUDQM/TXD1F*2	P4_10	-
48	P4_9/$\overline{\text{LLWR}}$*1, P5_7 /RXD1F/LLDQM/TA1_I7/TA1_O7*2	P4_9	-
49	P5_5/TE1_AI/$\overline{\text{SDCAS}}$	P5_5	SDRAM (CAS), JA5-17
50	P5_4/INTP16/$\overline{\text{SDRAS}}$/TA1_I4	P5_4	SDRAM (RAS), JA5-10

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).

2.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.5 Application Header (JA5) Pin Descriptions

Pin No.	Signal Name	Signal connected to JA5 by default	Other connection
1	P8_4/ANI10	P8_4	-
2	P8_5/ANI11	P8_5	-
3	ANI00	ANI00	-
4	ANI01	ANI01	-
5	P2_15/SDA1/CAN0TXD*2	P2_15 (JP10-3)	U20 (TxD)
6	P2_14/SCL1/CAN0RXD*2, P7_0/INTP26*3	P2_14 (JP8-3)	U21 (A)
7	NC	NC	-
8	NC	NC	-
9	P5_7/INTP19 /RXD1F/LLDQM	P5_7	SDRAM ($\overline{\text{DQML}}$)
10	P5_4/INTP16/SDRAS/TA1_I4	P5_4	SDRAM ($\overline{\text{RAS}}$), JA3-50
11	P2_4/TA1_I0/TA1_O0*2, P1_15/TA0_O15*3	P2_4 (JP4-3)	-
12	P2_5/TA1_I1*1, P1_11/TA0_O11*3	P2_5	-
13	P2_7/TA1_I3/SCK1F	P2_7	JA2-10, JA2-23
14	P2_9/TA1_I5*2, P1_13/TA0_O13*3	P2_9 (JP7-3)	-
15	P4_0/A16/TA1_O8	P4_0	-
16	NC	NC	-
17	P5_5/TE1_AI/$\overline{\text{SDCAS}}$	P5_5	SDRAM ($\overline{\text{CAS}}$), JA3-49
18	P5_6/$\overline{\text{SDWE}}$/TE1_BI	P5_6	SDRAM ($\overline{\text{WE}}$)
19	P5_10/INTP22/TA1_O10	P5_10	LCD (J6-6)
20	P5_11/SCK1/$\overline{\text{REFRQ}}$/TA1_O11	P5_11	LCD (J6-4), JA6-10
21	P5_12/SO1/TA1_O12	P5_12	LCD (J6-11), JA6-8
22	P5_13/$\overline{\text{HLDAK}}$/TA1_O13	P5_13	LCD (J6-12)
23	P5_14/$\overline{\text{HLDRQ}}$/SI1/TA1_O14	P5_14	LCD (J6-13), JA6-7
24	P5_15/INTP27/TA1_O15	P5_15	LCD (J6-14)

Notes: 1.These pins are connected to through-holes via zero-ohm resistors (installed by default).

2.These pins are connected to through-holes via zero-ohm resistors (installed by default) and jumpers.

3.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

Table 3.6 Application Header (JA6) Pin Descriptions

Pin No.	Signal Name	Signal connected to JA6 by default	Other connection
1	P1_7/INTP12	P1_7	-
2	P6_6/$\overline{\text{DMAAK0}}$	P6_6	Ethernet PHY (P0TXEN)
3	P6_4/$\overline{\text{DMATC0}}$	P6_4	Ethernet PHY (P0TXD1)
4	NC	NC	-
5	RS232TX (JP5-4)	RS232TX (JP5-4)	-
6	RS232RX (JP2-4)	RS232RX (JP2-4)	-
7	P5_14/$\overline{\text{HLDRQ}}$/SI1/TA1_O14*1, P5_7/INTP19/RXD1F/LLDQM*2	P5_14	J6-13 (LCD), JA5-23
8	P5_12/SO1/TA1_O12*1, P5_8/LUDQM/TXD1F*2	P5_12	J6-11 (LCD), JA5-21
9	P4_6/A22/SO0F*1, P2_1/CSI1F_RYI/CSIF_RYO/$\overline{\text{BCYST}}$ /TXD0*2	P4_6	SDRAM (BA0), JA3-43
10	P5_11/SCK1/$\overline{\text{REFRQ}}$/TA1_O11	P5_11	J6-4 (LCD), JA5-20
11	P4_7/A23/SCK0F	P4_7	SDRAM (BA1)
12	P4_5/A21/SI0F*1, P2_2/$\overline{\text{WAIT}}$/RXD0*2	P4_5	JA3-42
13	P1_8/TE0_ZI/INTP13/TA0_I8/TA0_O8*1, P2_1/CSI1F_RYI/CSI_F_RYO/$\overline{\text{BCYST}}$ /TXD0*2	P1_8	-
14	P1_2/TA0_I2/TE0_TI1	P1_2	JA2-22
15	P1_5/D21/TA0_I5	P1_5	LED1
16	P1_6/D22/TA0_I6/TE0_BI/INTP11	P1_6	JA2-26
17	P2_0/NMI*2	NC	-
18	NC	NC	-
19	NC	NC	-
20	NC	NC	-
21	NC	NC	-
22	NC	NC	-
23	5VCC*2	NC	-
24	GND	GND	-

Notes: 1. These pins are connected to through-holes via zero-ohm resistors (installed by default).
2.These pins are connected to through-holes via zero-ohm resistors (NOT installed by default).

[Precautions on using application headers]

The signals connected to JA1-15 to JA1-22, JA2-20, JA6-1 and JA6-2 are also connected to the device U17 as the Ethernet PHY signals. These signals cannot be used as other pin functions. When using these signals as other pin functions, remove the zero-ohm resistor (R261) and the 22-ohm resistors between JA1-15, JA1-16, JA1-20 to JA1-22 (R61, R58, R259, R68, R70 respectively), and install a 22-ohm resistor to R276. When pull-ups and pull-downs are required for the signals of JA1-17 to JA1-19, JA2-7, JA2-20, JA6-1 and JA6-2, use the resistor with up to 10k ohms. The operational guarantee does not cover any remodeling including a remove/install of a zero-ohm resistor to change the application header signal connection.

3.1.2 USB Connectors (J1 and J3)

The R0K0F4022C000BR includes a series A-receptacle (J1) as USB host connector, and a series Mini-B receptacle (J3) as USB function connector.

Figure 3.3 shows USB Connector (J1 and J3) Pin Assignments. Table 3.7 and Table 3.8 list USB host connector (J1) pin names and USB function connector (J3) pin names respectively.

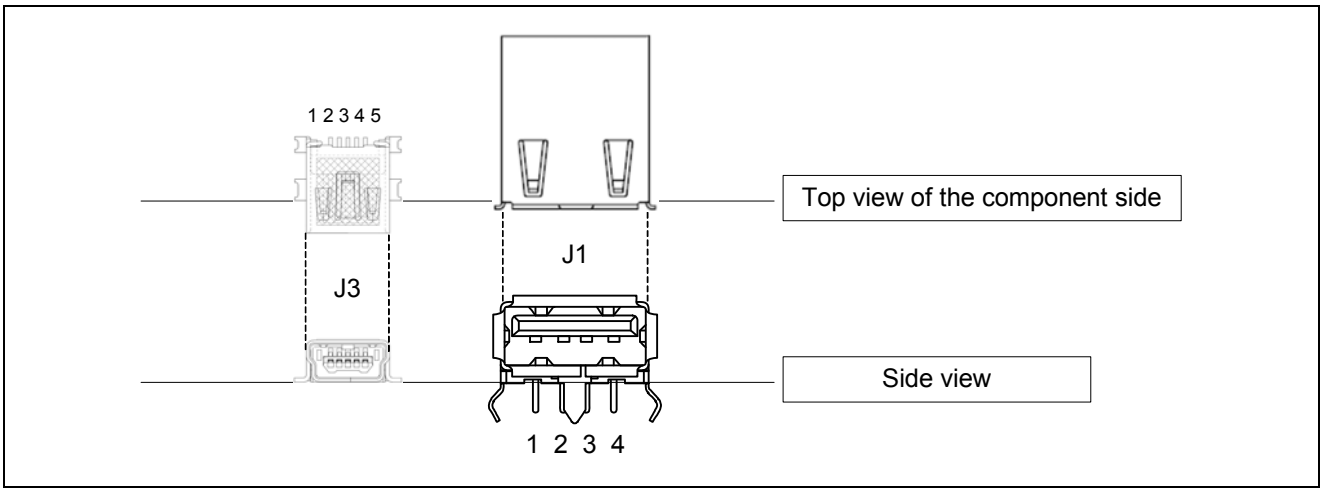

Figure 3.3 USB connector (J1 and J3) Pin Assignments

Table 3.7 USB Host Connector (J1) Pin Names

Pin No.	Signal Name
1	VBUS
2	DM
3	DP
4	GND

Table 3.8 USB Function Connector (J3) Pin Names

Pin No.	Signal Name
1	VBUS
2	DM
3	DP
4	ID (connected to test pin)
5	GND

3.1.3 Ethernet Connector (J2)

The R0K0F4022C000BR includes an Ethernet connector (J2).

Figure 3.4shows the Ethernet connector (J2) pin assignments. Table 3.9 lists the Ethernet connector (J2) pin names.

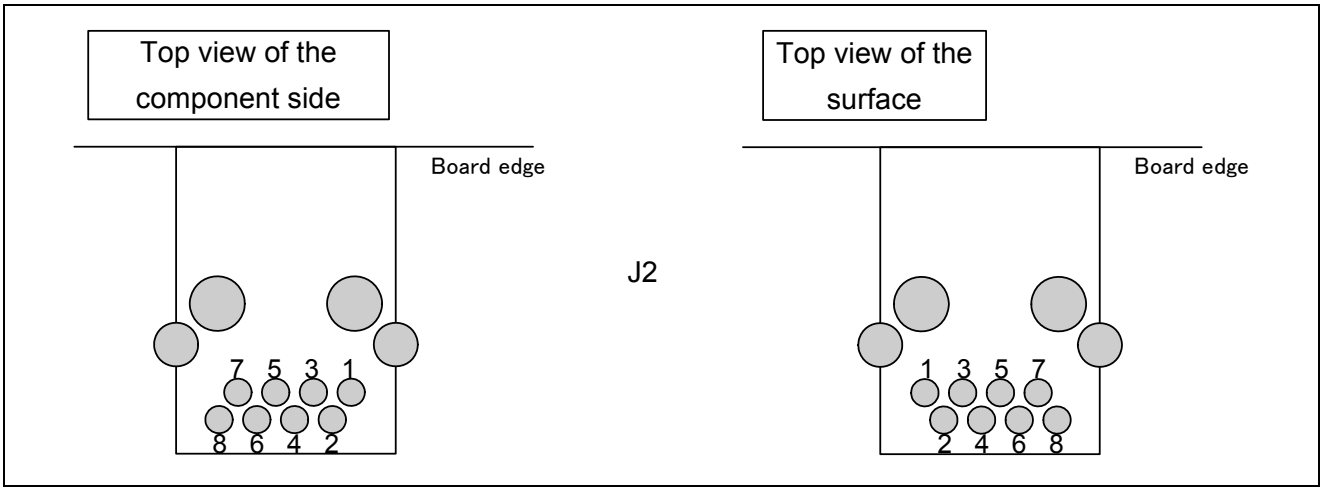

Figure 3.4 Ethernet Connector (J2) Pin Assignments

Table 3.9 Ethernet Connector (J2) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	TD+	2	TD−
3	TCT	4	RD+
5	RD−	6	RCT
7	N.C.	8	GND

3.1.4 CAN Connector (J4)

The R0K0F4022C000BR includes the CAN connector (J4) to execute CAN transmission and reception.
Figure 3.5 shows the CAN connector (J4) pin assignments. Table 3.10 lists the CAN connector (J4) pin names

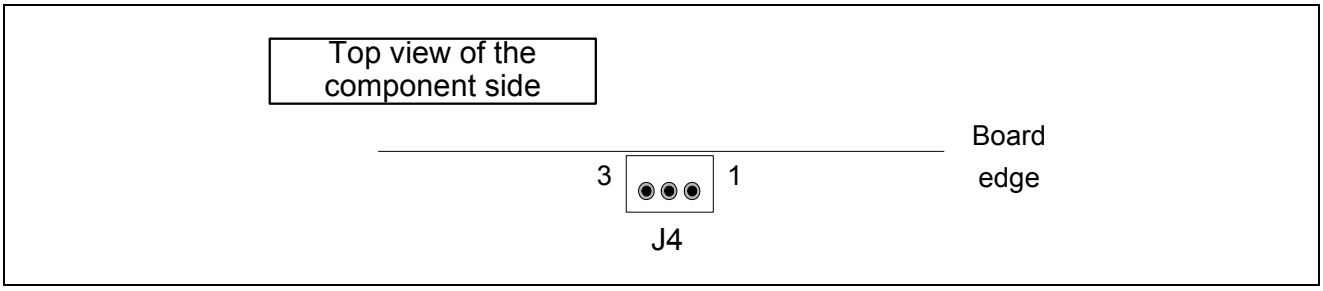

Figure 3.5 CAN Connector (J4) Pin Assignments

Table 3.10 CAN Connector (J4) Pin Names

Pin No.	Signal Name
1	CANH（U20）
2	GND
3	CANL（U20）

Note: P2_14/SCL1/CAN0RXD and P2_15/SDA1/CAN0TXD of the V850E2/ML4 are also connected to the EEPROM and SCL signal and SDA signal of the application header (JA1). When using these connections, switch the connection at JP8 and JP10. P2_14/SCL1/CAN0RXD and P2_15/SDA1/CAN0TXD of the V850E2/Ml4 are also connected to CAN signal of the application header (JA5), and can be used by installing the zero-ohm resistor. CAN connector (J4) cannot be used they are connected to the application header side.

3.1.5 Serial Port Connector (J5)

The R0K0F4022C000BR includes the serial port connector (J5). The serial port connector (J5) has two options for wiring on the R0K0F4022C000BR, using a male jack with the crossover cable, or a female socket with the straight cable by removing and installing zero-ohm resistors R109, R111, R112, R113, R115, R117, R118 and R119 as appropriate. The R0K0F4022C000BR installs resistors R111, R113, R115 and R119 to include a male jack with crossover cable by default.

Figure 3.6shows the serial port connector (J5) pin assignment on crossover cable by a male jack. Table 3.11 lists the serial port connector (J5) pin names on crossover cable by a make jack.

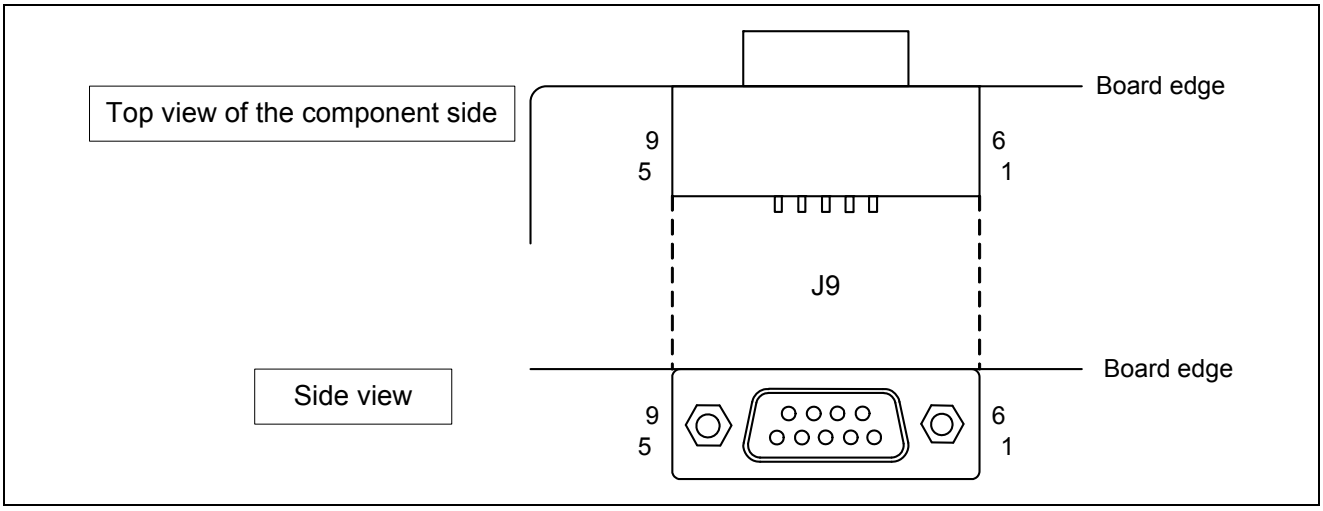

Figure 3.6 Serial Port Connector (J5) Pin Assignments (on crossover cable by a male jack)

Table 3.11 Serial Port Connector (J5) Pin Names (on crossover cable by a male jack)

Pin No.	Signal Name	Pin No.	Signal Name
1	NC	6	DSR
2	RXD	7	RTS
3	TXD	8	CTS
4	DTR	9	NC
5	GND		

Note: Pins 4 to 6, and Pins 7 to 8 are loop-back connected respectively.

3.1.6 LCD Connector (J6)

The R0K0F4022C000BR includes the LCD connector (J6).

Figure 3.7shows the LDC connector (J6) pin assignments, and Table 3.12 lists the LCD connector pin names.

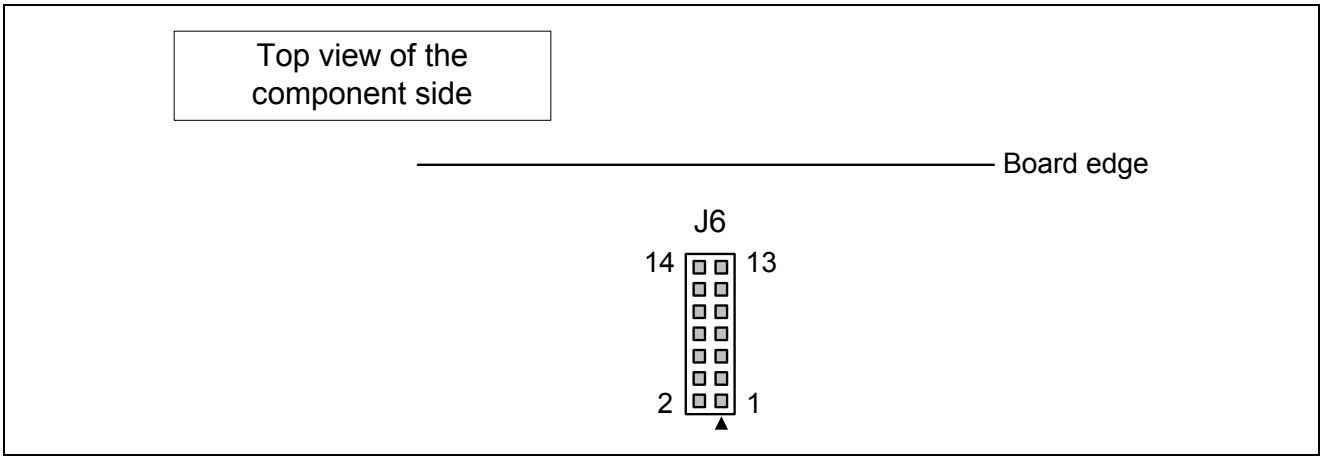

Figure 3.7 LCD Connector (J6) Pin Assignments

Table 3.12 LCD Connector (J6) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	5VCC
3	NC	4	LCDRS（P5_11）
5	R/W (Pulled down by a 1kΩ resistor)	6	LCDE（P5_10）
7	NC	8	NC
9	NC	10	NC
11	LCDD12（P5_12）	12	LCDD13（P5_13）
13	LCDD14（P5_14）	14	LCDD15（P5_15）

3.1.7 External Power Supply Connectors (J7 and J12 to J14)

The R0K0F4022C000BR includes four external power supply connectors (J7and J12 to J14) to apply 5V, 3.3V, 1.2V power, and the A/D converter power directly from external source, not via the DC power jack (J9). J7 and J12 to J14 connectors are not installed by default.

When operating the R0K0F4022C000BR by supplying 5V power from the external supply connector (J7), do not connect the AC adaptor to the DC power jack (J9). When supplying 3.3V power from the external supply connector (J12) to the board, remove the zero-ohm resistor, R155. Alternatively, remove the zero-ohm resistor, R156, to supply the A/D converter power from the external supply connector (J13), or remove the zero-ohm resistor, R162, to supply 1.2V power from the external supply connector (J14) to the board.

Figure 3.8 shows the external power supply connectors (J7 and J12 to J14) pin assignments,. Table 3.13 to Table 3.16 list the external power supply connectors (J7 and J12 to J14) pin names.

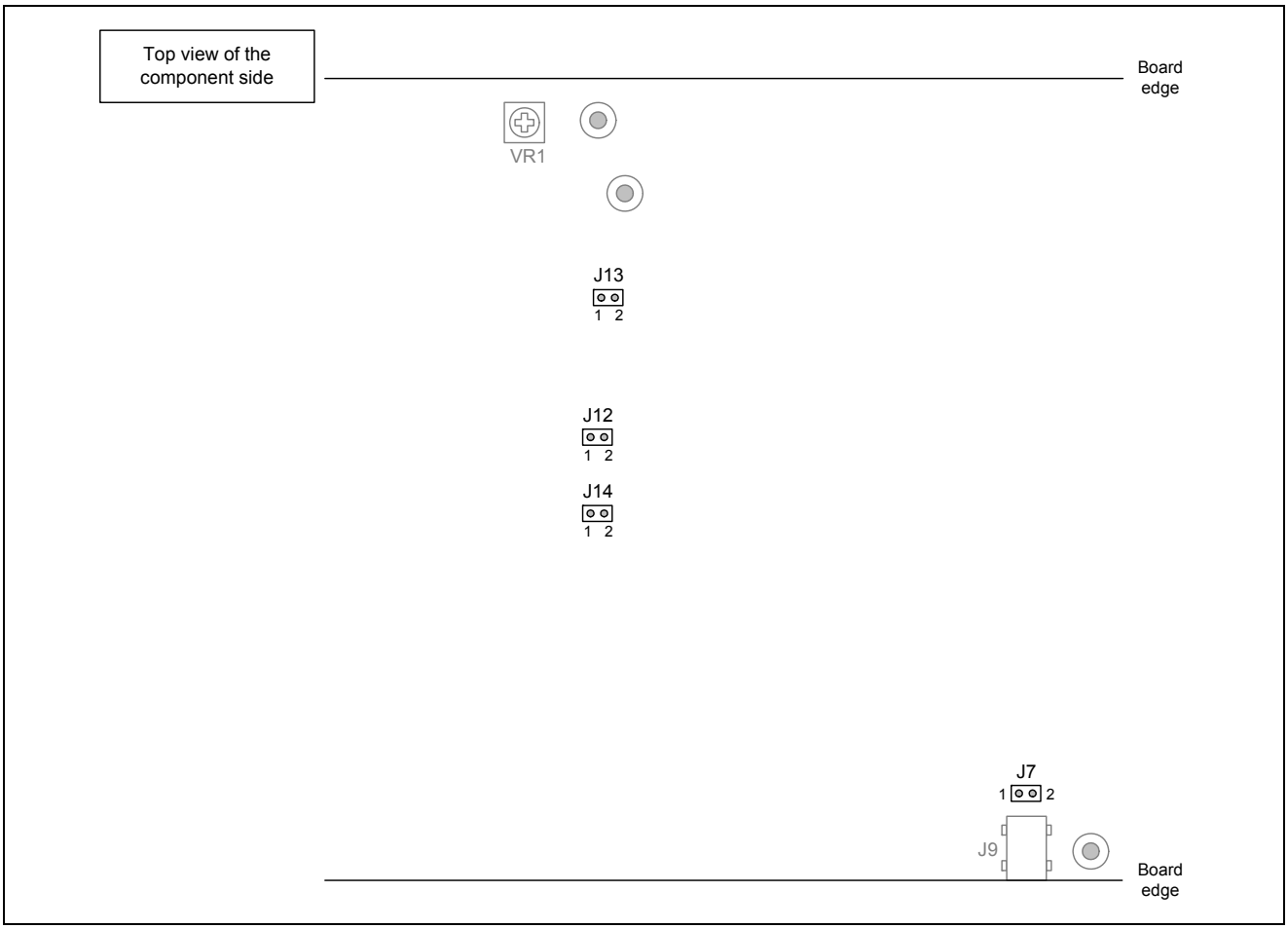

Figure 3.8 External Power Supply Connectors Pin Assignments

Table 3.13 External Power Supply Connector (J7) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	5VCC（5V power supply）	2	GND

Table 3.14 External Power Supply Connector (J12) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	EVDD（3.3V power supply）	2	GND

Table 3.15 External Power Supply Connector (J13) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	AVDD（5V power supply）	2	GND

Table 3.16 External Power Supply Connector (J14) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	IVDD（1.2V power supply）	2	GND

Note: When supplying 5V from the external power supply connector (J7), do not connect AC adapter to DC power jack (J9). The R0K0F4022C000BR and AC adapter may be destroyed when the power is supplied from the external power supply connector (J7) with the AC adapter connected.

When supplying 3.3V, 1.2V power and the A/D converter power from the external power supply connector (J12, J13 and J14), make sure to remove the zero-ohm resistors, R155, R156 and R162. The R0K0F4022C000BR may be destroyed when 3.3V, 1.2V and the A/D converter power is supplied from the external power supply connector (J12, J13 andJ14) with these resistors installed.

3.1.8 DC Power Jack (J9)

The R0K0F4022C000BR includes a DC power jack (J9).

Figure 3.9shows the DC power jack pin assignment. Table 3.17 lists the DC power jack pin names.

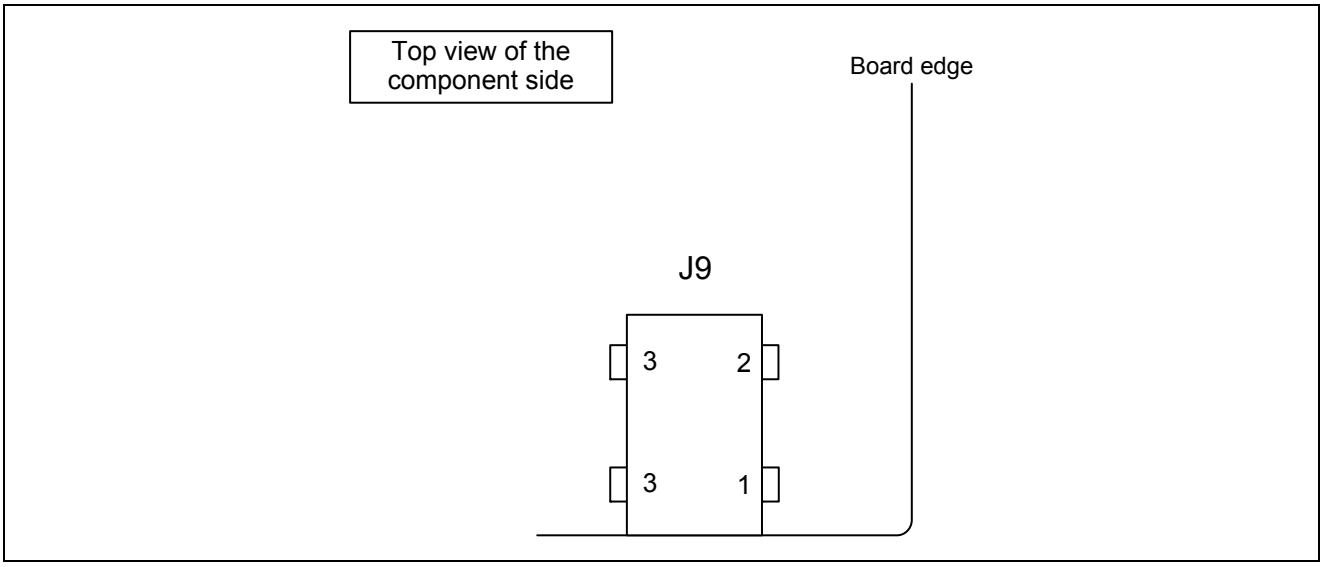

Figure 3.9 DC Power Jack (J9) Pin Assignments

Table 3.17 DC Power Jack (J9) Pin Names

Pin No.	Signal name
1	GND
2	GND
3	5VCC
3	5VCC

3.1.9 E1 Connector (J10)

The R0K0F4022C000BR includes a 14-pin E1 connector (J10) to connect the E1 emulator.
Figure 3.10 shows the E1 connector (J10) pin assignments. Table 3.18 lists the E1 connector (J10) pin names

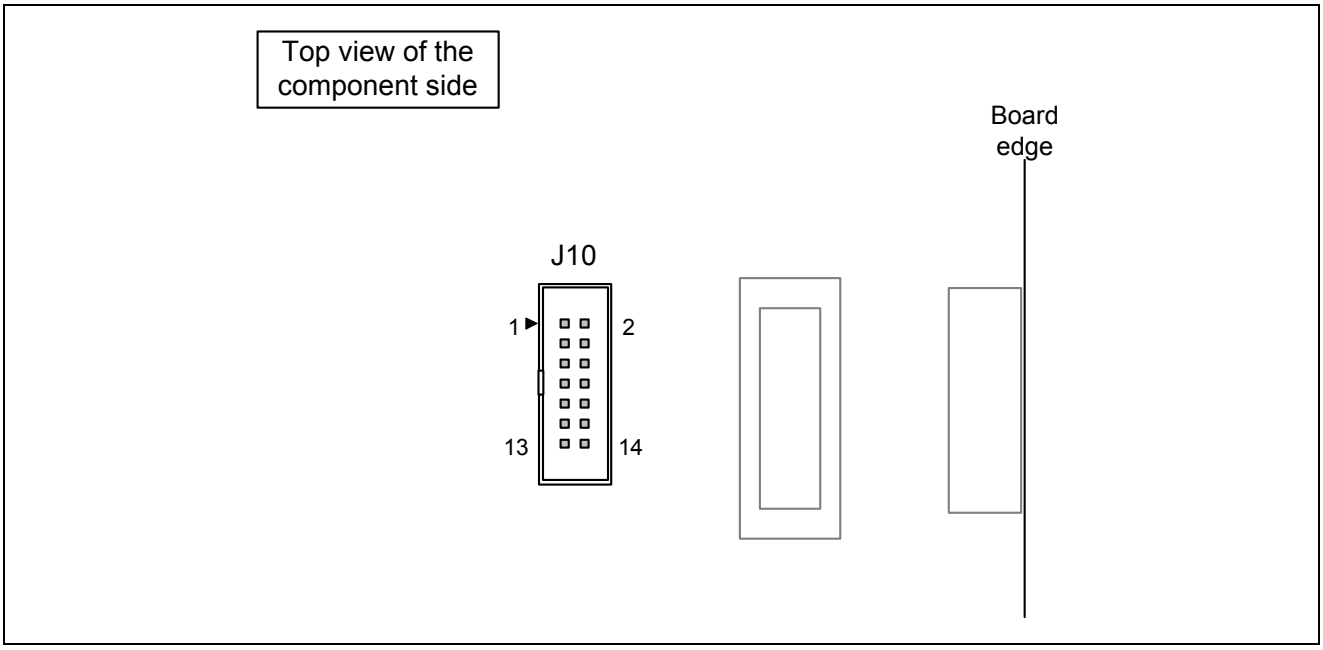

Figure 3.10 E1 Connector (J10) Pin Assignments

Table 3.18 E1 Connector (J1-) Pin Names

Pin No.	Signal Name	Pin No.	Signal Name
1	TCK	8	VDD
2	GND1	9	TMS/FLMD1
3	$\overline{\text{TRST}}$	10	$\overline{\text{RESET2}}$
4	FLMD0	11	$\overline{\text{TRDY}}$
5	TDO	12	GND2
6	NC1	13	$\overline{\text{RESET1}}$
7	TDI	14	GND3

3.1.10 GND Connector (J15)

The R0K0F4022C000BR includes a GND connector (J15).

Figure 3.11 shows the GND connector (J15) pin assignments. Table 3.19 lists the GND connector (J15) pin names.

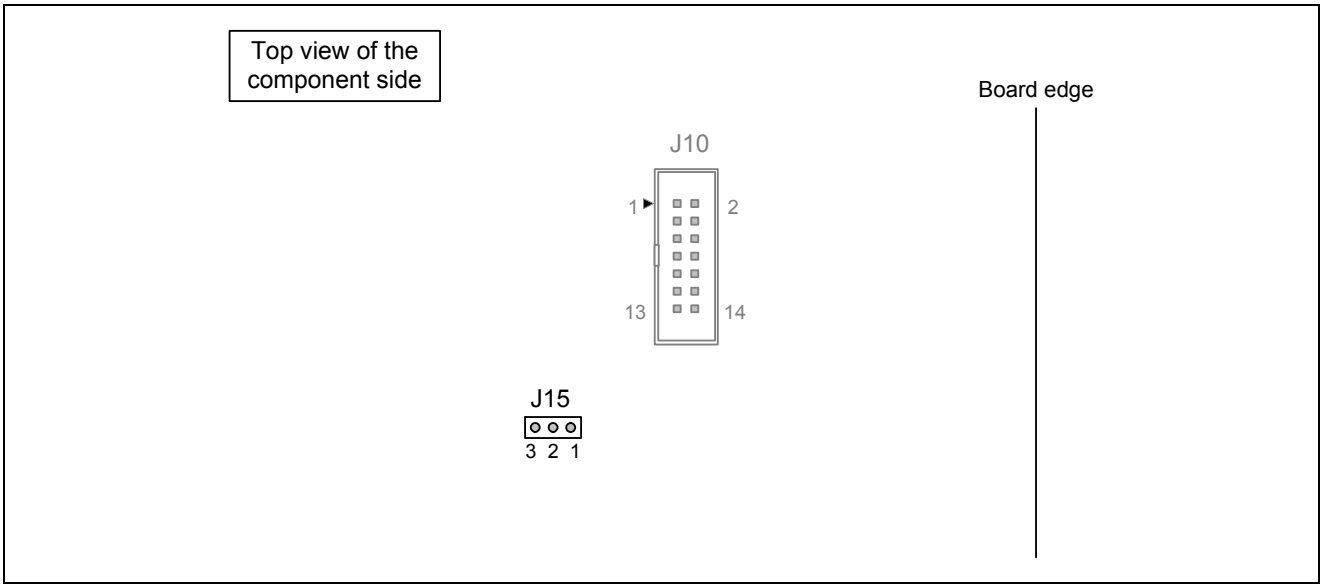

Figure 3.11 GND Connector (J15) Pin Assignments

Table 3.19 GND Connector (J15) Pin Names

Pin No.	Signal Name
1	GND
2	GND
3	GND

3.2 Operating Components

The R0K0F4022C000BR includes switches, jumpers, LEDs and a potentiometer as operating components.

3.2.1 Jumpers (JP1, JP2, JP4, JP5, JP7 to JP13)

The R0K0F4022C000BR provides eleven jumpers (JP1, JP2, JP4, JP5 and JP7 to JP13).

3.2.1.1 P2_3 Select Jumper (JP1)

JP1 is a jumper to specify whether to use the V850E2/ML4 P2_3 for USB function control or for INTP1 (SW4) and a 9-pin of the application header (JA2) on the board. Short-circuit pins 1 and 2 of JP1 to use the USB function connector (J3), and short-circuit pins 2 and 3 of JP1 to use the P2_3 as INTP1 (SW4) and a 9-pin of the application header (JA2).
Table 3.20 shows the P2_3 select jumper (JP1) settings.

Table 3.20 P2_3 Select Jumper (JP1) Settings

Number	Setting	Description
JP1	1–2	Uses the USB function connector (J3)
	2–3	Connects the V850E2/ML4 P2_3 to INTP1 (SW4) and a 9-pin of the application header (JA2)

【Note】 : set by default

3.2.1.2 Serial Port Received Signal Select Jumper (JP2)

JP2 is a jumper to switch signal wires the serial port received. Short-circuit pins 1 and 2 of JP2 when connecting the V850E2/ML4 P2_3 to the serial port connector (J5). Short-circuit pin 2 and 4 of JP2 to connect a 6-pin (RS232RX) of the application header (JA6) to the serial port connector (J5).
Table 3.21 shows the serial port received signal select jumper (JP2) settings.

Table 3.21 Serial Port Received Signal Select Jumper (JP2) Settings

Number	Setting	Description
JP2	1–2	Connects the V850E2/ML4 P2_12/RXD0F to the serial port connector (J5)
	2–4	Connects a 6-pin (RS232RX) of the application header (JA6) to the serial port connector (J5)

【Note】 : set by default

3.2.1.3 P2_4 Select Jumper (JP4)

JP4 is a jumper to specify whether to use the V850E2/ML4 P2_4 for the USB function control or for an 11-pin of the application header (JA5) on the board. Short-circuit pins 1 and 2 of JP4 to use the USB function connector (J3), and short-circuit pins 2 and 3 of JP4 to use P2_4 as an 11-pin of the application header (JA5).
Table 3.22 shows the P2_4 select jumper (JP4) settings.

Table 3.22 P2_4 Select Jumper (JP4) Settings

Number	Setting	Description
JP4	1–2	Uses the USB function connector (J3)
	2–3	Connects the V850E2/ML4 P2_4 to an 11-pin of the application header (JA5)

【Note】 : set by default

3.2.1.4 Serial Port Transmitted Signal Select Jumper (JP5)

JP5 is a jumper to switch signal wires the serial port transmitted. Short-circuit pins 1 and 2 of JP5 when connecting the V850E2/ML4 P2_13/TXD0F to the serial port connector (J5), and short-circuit pins 2 and 4 of JP5 to connect a 5-pin (RS232TX) of the application header (JA6) to the serial port connector (J5).
Table 3.23 shows the serial port transmitted signal select jumper (JP5) settings.

Table 3.23 Serial Port Transmitted Signal Select Jumper (JP5) settings

Number	Setting	Description
JP5	1–2	Connects the V850E2/ML4 P2_13/TXD0F to the serial port connector (J5)
	2–4	Connects a 5-pin (RS232TX) of the application header (JA6) to the serial port connector (J5)

【Note】 : set by default

3.2.1.5 P2_9 Select Jumper (JP7)

JP7 is a jumper to specify whether to use the V850E2/ML4 P2-9 for the USB host control or for a 14-pin of the application header (JA5) on the board. Short-circuit pins 1 and 2 of JP7 to use the USB host connector (J1), and short-circuit pins 2 and 3 of JP7 to use P2_9 as a 14-pin of the application header (JA5).
Table 3.24 shows the P2_9 select jumper (JP7) settings.

Table 3.24 P2_9 Select Jumper (JP7) Settings

Number	Setting	Description
JP7	1–2	Uses the USB host connector (J1)
	2–3	Connects the V850E2/ML4 P2_9 to a 14-pin of the application header (JA5)

【Note】 : set by default

3.2.1.6 P2_10 Select Jumper (JP9)

JP9 is a jumper to specify whether to use the V850E2/ML4 P2_10 of the USB host control or for a 23-pin of the application header (JA5) on the board. Short-circuit pins 1 and 2 of JP9 to use the USB host connector (J1), and short-circuit pins 2 and 3 of JP9 to use P2_10 as a 23-pin of the application header (JA5).
Table 3.25 shows P2_10 select jumper (JP9) settings.

Table 3.25 P2_-10 Select Jumper (JP9) Settings

Number	Setting	Description
JP9	1–2	Uses the USB host connector (J1)
	2–3	Connects the V850E2/ML4 P2_10 to a 23-pin of the application header (JA5)

【Note】 : set by default

3.2.1.7 CAN－EEPROM Select Jumper (JP8)

JP8 is a jumper to specify whether to connect the V850E2/ML4 P2_14/SCL1/CAN0RXD to the CAN connector (J4) and a 6-pin of the application header (JA5), or to the EEPROM and a 26-pin of the application header (JA1) on the board. Short-circuit pins 2 and 3 of JP8 when connecting the V850E2/ML4 P2_14/SCL1/CAN0RXD to the CAN connector (J4) and a 6-pin of the application, and short-circuit pins 1and 2 of JP8 to connect it to the EEPROM and a 26-pin of the application header (JA1).
Table 3.26 shows the CAN-EEPROM select jumper (JP8) settings.

Table 3.26 CAN-EEPROM Switch Jumper (JP8) Settings

Number	Setting	Description
JP8	1–2	Connects the V850E2/ML4 P2_14/SCL1/CAN0RXD to the EEPROM and a 26-pin of the application header (JA1)
	2–3	Connects the V850E2/ML4 P2_14/SCL1/CAN0RXD to the CAN connector (J4) and a 6-pinof the application header (JA5)

【Note】 : set by default

3.2.1.8 CAN－EEPROM Select Jumper (JP10)

JP10 is a jumper to specify whether to connect the V850E2/ML4 P2_15/SDA1/CAN0TXD to the CAN connector (J4) and a 5-pin of the application header (JA5), or to the EEPROM and a 25-pin of the application header (JA1) on the board. Short-circuit pins 2 and 3 of JP10 when connecting the V850E2/ML4 P2_15/SDA1/CAN0TXD to the CAN connector (J4) and a 5-pin of the application header (JA5), and short-circuit pin 1 and 2 of JP10 to connect it to the EEPROM and a 25-pin of the application header (JA1).
Table 3.27 shows the CAN-EEPROM select jumper (JP10) settings.

Table 3.27 CAN－EEPROM Select Jumper (J10) Settings

Number	Setting	Description
JP10	1–2	Connects the V850E2/ML4 P2_15/SDA1/CAN0TXD to the EEPROM and a 25-pin of the application header (JA5)
	2–3	Connects the V850E2/ML4 P2_15/SDA1/CAN0TXD to the CAN connector (J4) and a 5-pin of the application header (JA4)

【Note】 : set by default

3.2.1.9 SDRAM Jumper (JP11)

JP11 is a jumper to specify whether to use the SDRAM or the signal multiplexed with the SDRAM connection signal on the side of the application header. Short-circuit JP11 only when using the SDRAM. The signal multiplexed with the SDRAM connection signal on the side of the application cannot be used.
Table 3.28 shows the SDRAM jumper (JP11) settings.

Table 3.28 SDRAM Jumper (JP11) Settings

Number	Setting	Description
JP11	Short	Uses the SDRAM
	Open	Uses the multiplexed signal with the SDRAM connection signal on the side of the application header 用

【Note】 : set by default

3.2.1.10 OCD Jumper (JP12)

JP12 should be open to use.

3.2.1.11 PG-FP5 Connection Jumper (JP13)

JP13 is a jumper to specify the connection of the PG-FP5, the V850 internal flash writing tool. Short-circuit pins 2 and 3 when using the PG-FP5, and short-circuit pins 1 and 2 in any other case of the PG-FP5.
Table 3.29 shows the PG-FP5 connection jumper (J13) settings.

Table 3.29 PG-FP5 Connection Jumper (JP13) Settings

Number	Setting	Description
JP13	1–2	Uses other than PG-FP5
	2–3	Uses the PG-FP5

【Note】 : set by default

3.2.2 Switches

The R0K0F4022C000BR includes a user DIP switch (SW1), an operation mode setting DIP switch (SW2), four push switches (SW3 to SW6), and an Ethernet PHY DIP switch (SW7).
Table 3.30 lists switches on the R0K0F4022C000BR. Table 3.31 lists settings of the operation mode setting DIP switch (SW2).Table 3.32 lists settings of the V850E2/ML4 operation mode setting. Table 3.33 lists settings of the Ethernet PHY setting DIP switch (SW7).

Table 3.30 Switches on the R0K0F4022C000BR

Number	Function	Remarks
SW1	User DIP switch (4/package)	Refer to 2.12 for details
SW2	Operation mode setting DIP switch 4/package)	Refer to Table 3.32 for settings
SW3	External interrupt switch (NMI)	Refer to 2.11 for details
SW4	External interrupt switch (INTP1 input and $\overline{\text{ADTRG}}$ input)	Refer to 2.11 for details
SW5	External interrupt switch (INTP2)	Refer to 2.11 for details
SW6	Reset switch	Refer to 2.15 for details
SW7	Ethernet PHY setting DIP switch (8/package)	Refer to Table 3.33 for settings

Table 3.31 Operation Mode Setting DIP Switch (SW2) Settings

Number	Setting	Function
SW2-1	ON	Set theV850E2/ML4 MODE3 pin to high
	OFF	Set theV850E2/ML4 MODE3 pin to low
SW2-2	ON	Set theV850E2/ML4 MODE2 pin to high
	OFF	Set theV850E2/ML4 MODE2 pin to low
SW2-3	ON	Set theV850E2/ML4 FLMD1 pin to high
	OFF	Set theV850E2/ML4 FLMD1 pin to low
SW2-4	ON	Set theV850E2/ML4 FLMD0 pin to high
	OFF	Set theV850E2/ML4 FLMD0 pin to low

【Note】 : set by default

Table 3.32 Settings of the V850E2/ML4 Operation Mode Setting

SW2-1 (MODE3)	SW2-2 (MODE2)	SW2-3 (FLMD1)	SW2-4 (FLMD0)	V850E2/ML4 operation mode
OFF ("L")	OFF ("L")	OFF ("L")	OFF ("L")	Normal operation mode (Connectable with the E1 emulator)
OFF ("L")	OFF ("L")	OFF ("L")	ON ("H")	Flash memory programming mode
OFF ("L")	OFF ("L")	ON ("H")	ON ("H")	Boundary scan mode (Setting prohibited for the R0K0F4022C000BR)
Combinations other than listed above				Setting prohibited

【Note】 : set by default

Table 3.33 Ethernet PHY DIP Switch (SW7) Settings

Number	Setting	Function	Description
SW7-1	ON	Set P0RXD3 pin to low	Autoneg disabled, 100BaseT
	OFF	Set P0RXD3 pin to high	Autoneg enabled, 100BaseT
SW7-2	ON	Set P0RXD2 pin to low	If Autoneg disabled:Half Duplex If Autoneg enabled:Parallel detect ends in half duplex
	OFF	Set P0RXD2 pin to high	If Autoneg disabled: Full Duplex If Autoneg enabled: Forced Full Duplex in parallel detect
SW7-3	ON	Set P0RXCLK pin to low	Disable Quick Autonegotiation
	OFF	Set P0RXCLK pin to high	If Autoneg enabled: Quick Autonegotiation, shortest times If Autoneg disabled: Special Isolate. In this mode the Phys will not set up a link unless programmed and enabled through the SMI.
SW7-4	ON	Set P0RXERR pin to low	Configure RMII Interface
	OFF	Set P0RXERR pin to high	Configure MII Interface
SW7-5	ON	Set P0TXCLK pin to low	Standard Mode, “JK” required for Start of Frame detection
	OFF	Set P0TXCLK pin to high	Fast Mode, Only “J” required for Start of Frame detection
SW7-6	ON	Set P0CRS pin to low	AUTOMDI-X disabled
	OFF	Set P0CRS pin to high	AUTOMDI-X enabled
SW7-7	ON	Set P0RXD0 pin to high	Configures the upper two bits N and M of the Phy addresses: 00: device uses address 00xxx for SMI 01: device uses address 01xxx for SMI 10: device uses address 10xxx for SMI 11: device uses address 11xxx for SMI
	OFF	Set P0RXD0 pin to low	
SW7-8	ON	Set P0RXD1 pin to high	
	OFF	Set P0RXD1 pin to low	

【Note】 : set by default

3.2.3 Potentiometer

The R0K0F4022C000BR includes a potentiometer to evaluate AN105 input.
Table 3.34 lists the information of the potentiometer model installed on the R0K0F4022C000BR. For more details, refer to the datasheet provided from the manufacturer.

Table 3.34 Potentiometer

Number	Part Number	Manufacturer
VR1	CT-6ETV10KΩ	NIDEC Copal Electronics Corporation

3.2.4 LEDs

The R0K0F4022C000BR includes four user LEDs (LED0 to LED3), a USB host bus LED (LED4), three Ethernet PHY LEDs (LED6 to LED8), and a power LED (LED9).
Table 3.35 lists LEDs on the R0K0F4022C000BR.

Table 3.35 LEDs on the R0K0F4022C000BR

Number	Color	Description/Remarks
LED0	Green	User LED0 (illuminates when P1_4 outputs low level signal)
LED1	Orange	User LED1 (illuminates when P1_5 outputs low level signal)
LED2	Red	User LED2 (illuminates when P4_3 outputs low level signal)
LED3	Red	User LED3 (illuminates when P4_4 outputs low level signal)
LED4	Yellow	USB host bus LED (illuminates when the 5VCC is supplied)
LED6	Yellow	Ethernet PHY LED: LINK
LED7	Yellow	Ethernet PHY LED: ACT
LED8	Yellow	Ethernet PHY LED: DUPLEX
LED9	Blue	Power LED (illuminates when the 5VCC is supplied)

3.3 Dimensions

Figure 3.12 shows the R0K0F4022C000BR dimensions.

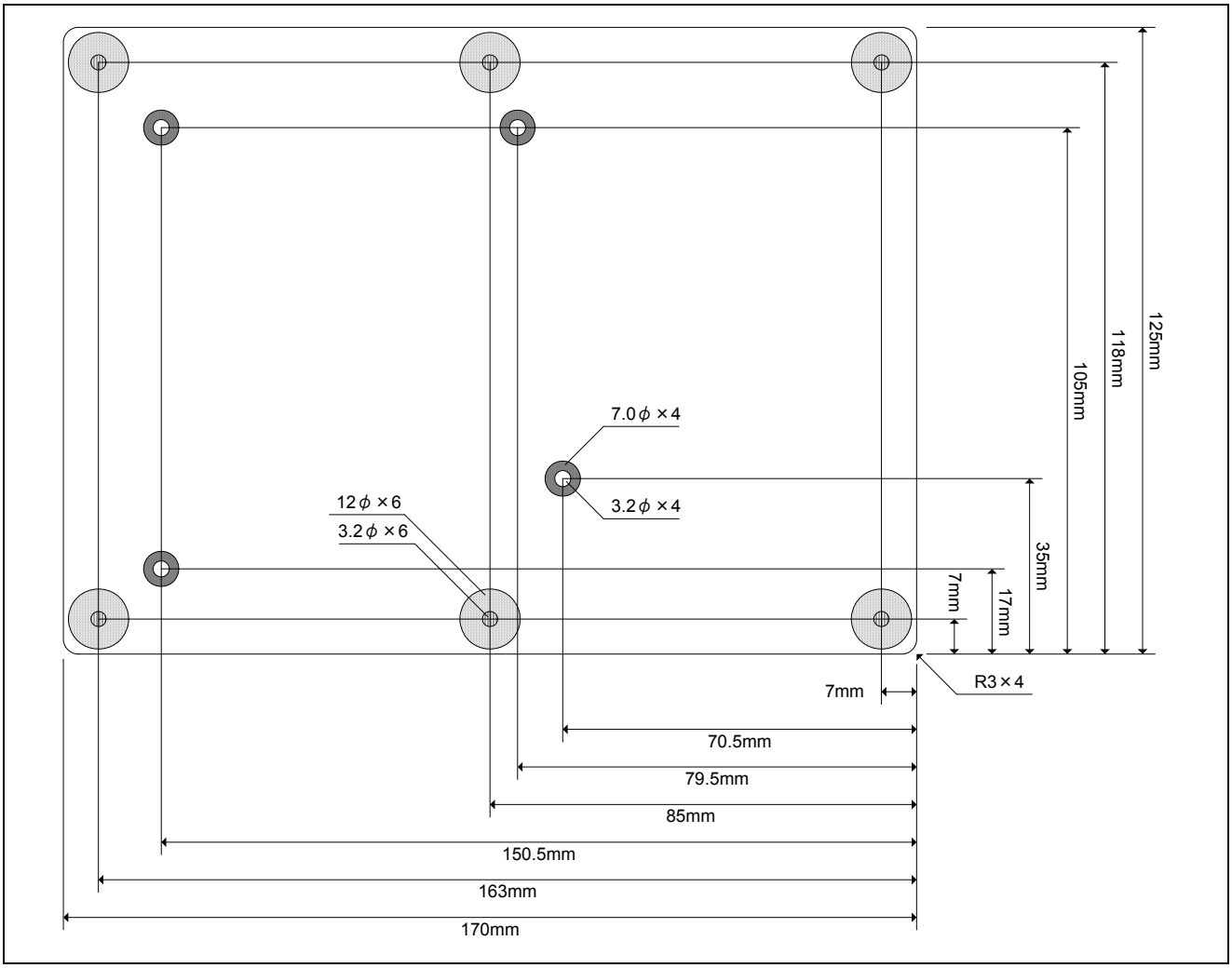

Figure 3.12 R0K0F4022C000BR Dimensions

Appendix R0K0F4022C000BR Schematics

V850E2/ML4 CPU board R0K0F4022C000BR SCHEMATICS

TITLE	PAGE
INDEX	1
CPU (V850E2/ML4), Clock, User-port	2
USB, LAN, SDRAM	3
CAN, Serial-port, EEPROM, LCD	4
UDI, Reset, Push-SW, Power	5
Application Header	6

Note:


Digital GND (GND)


Analog GND (AVss)


Not mounted

5VCC = Digital 5V
3VCC = Digital 3.3V
EVDD = 3.3V for CPU I/O
VDD = 3.3V for UVDD(USB) & DVDD(Debug)
OSCVDD = 3.3V for Oscillator
3AVDD = Analog 3.3V for uPD60610
1.2VCC = 1.2V
IVDD = 1.2V for CPU Core
PLLVDD = 1.2V for PLL
AVDD = Analog 3.3V or 5V for ADC

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps
L = Inductor

CHANGE			Renesas Solutions Corp.				R0K0F4022C000BR
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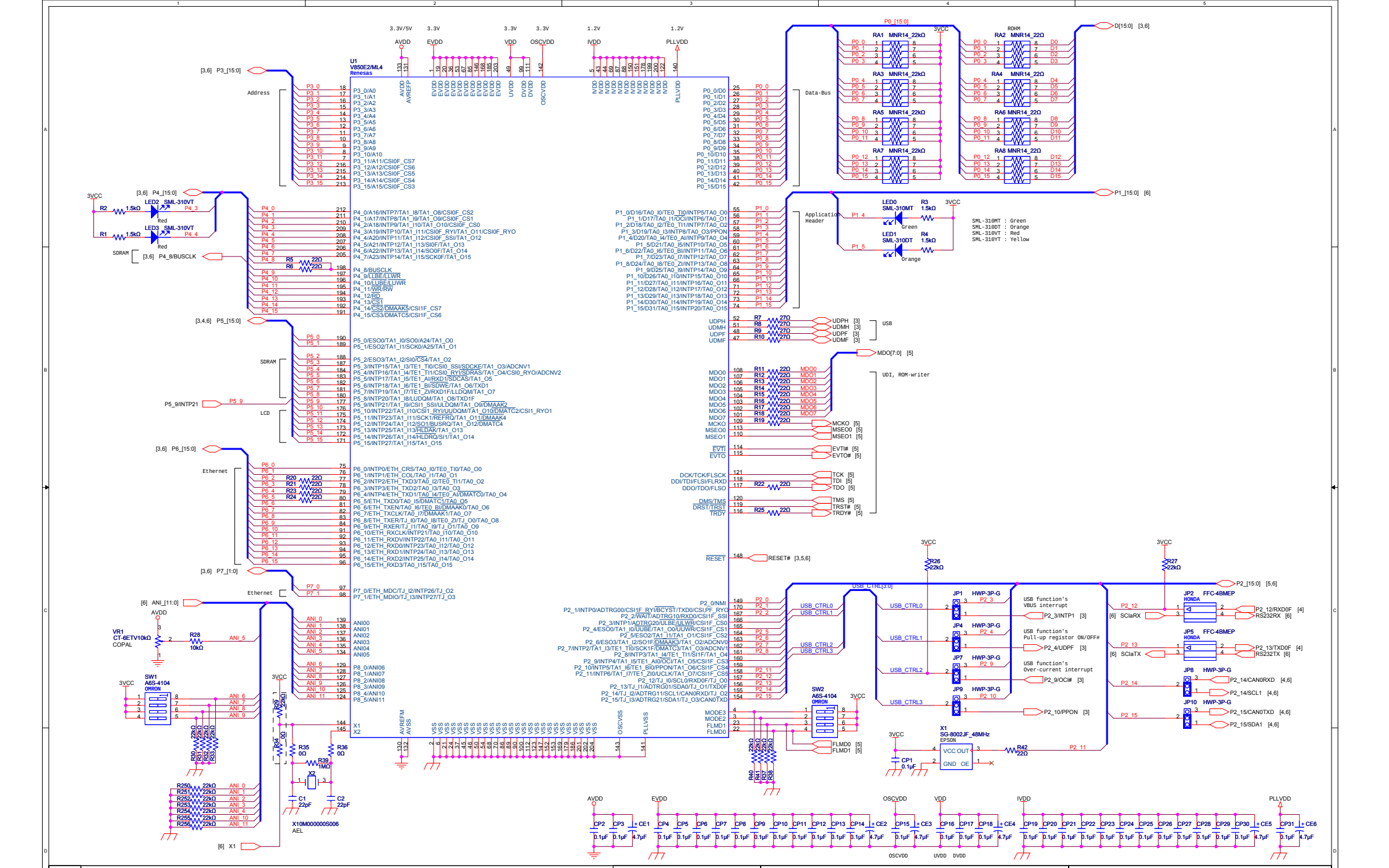
		DATE 12-05-15					D-R0K0F4022C000BR_C-B



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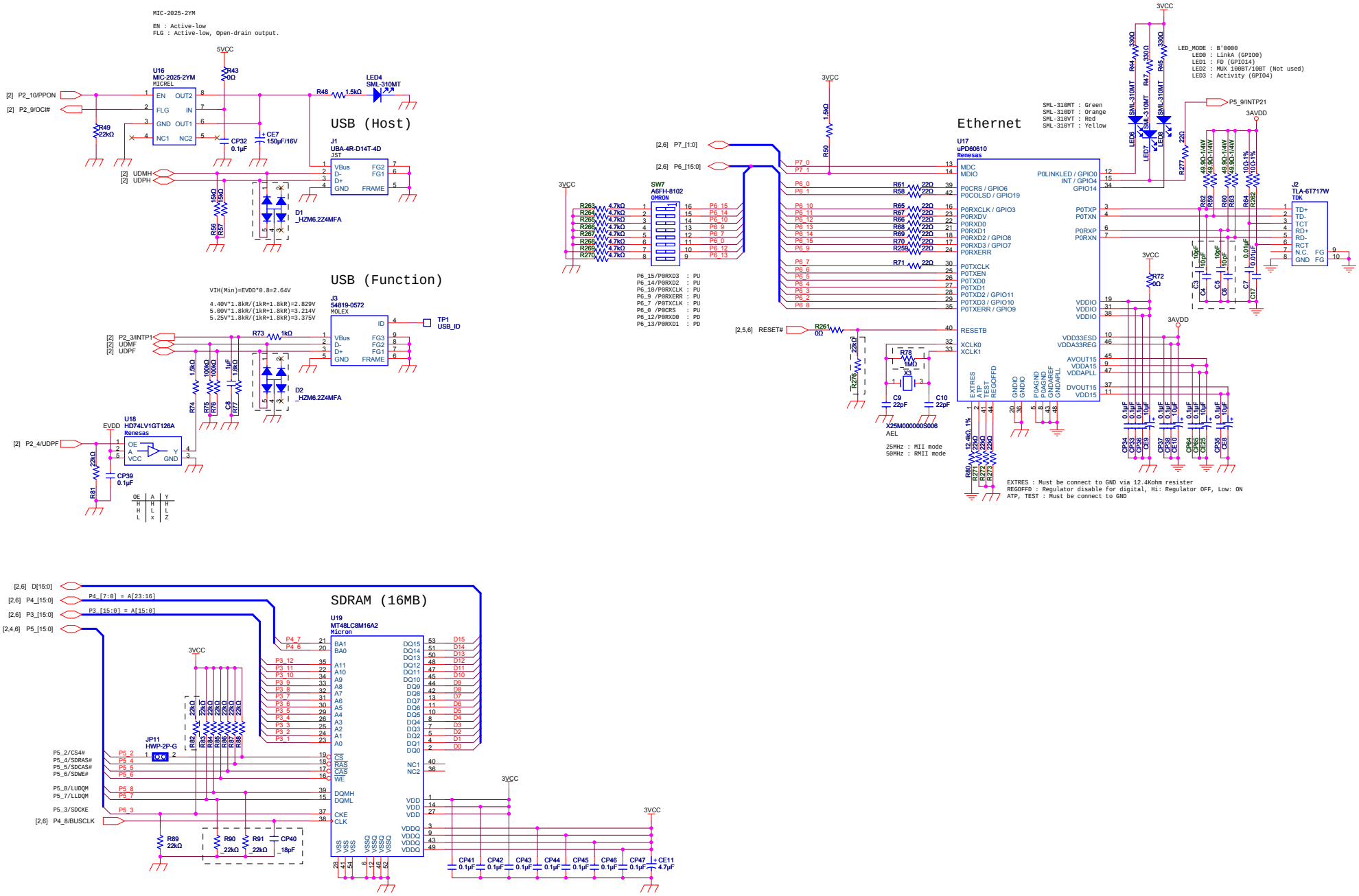

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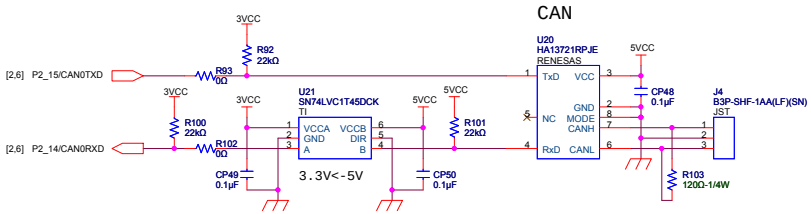

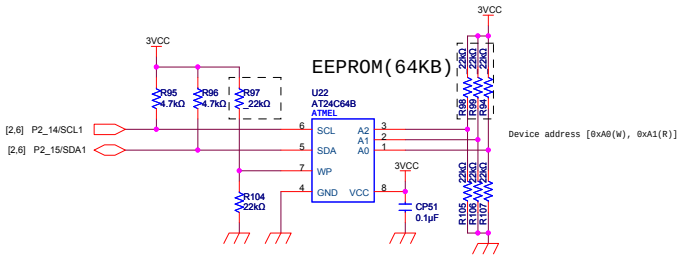

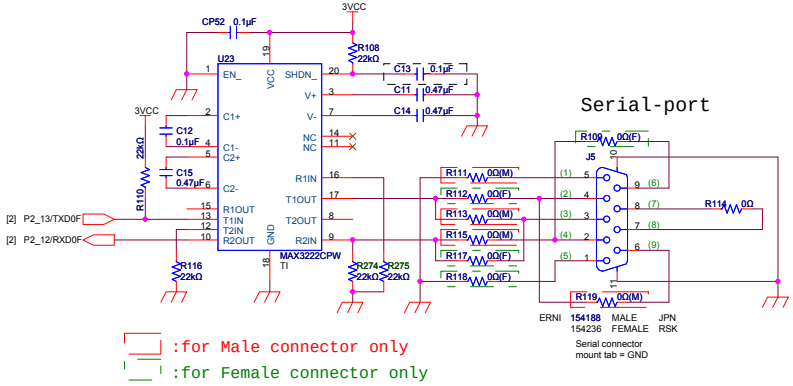

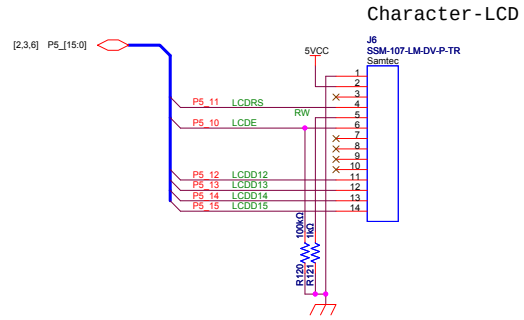

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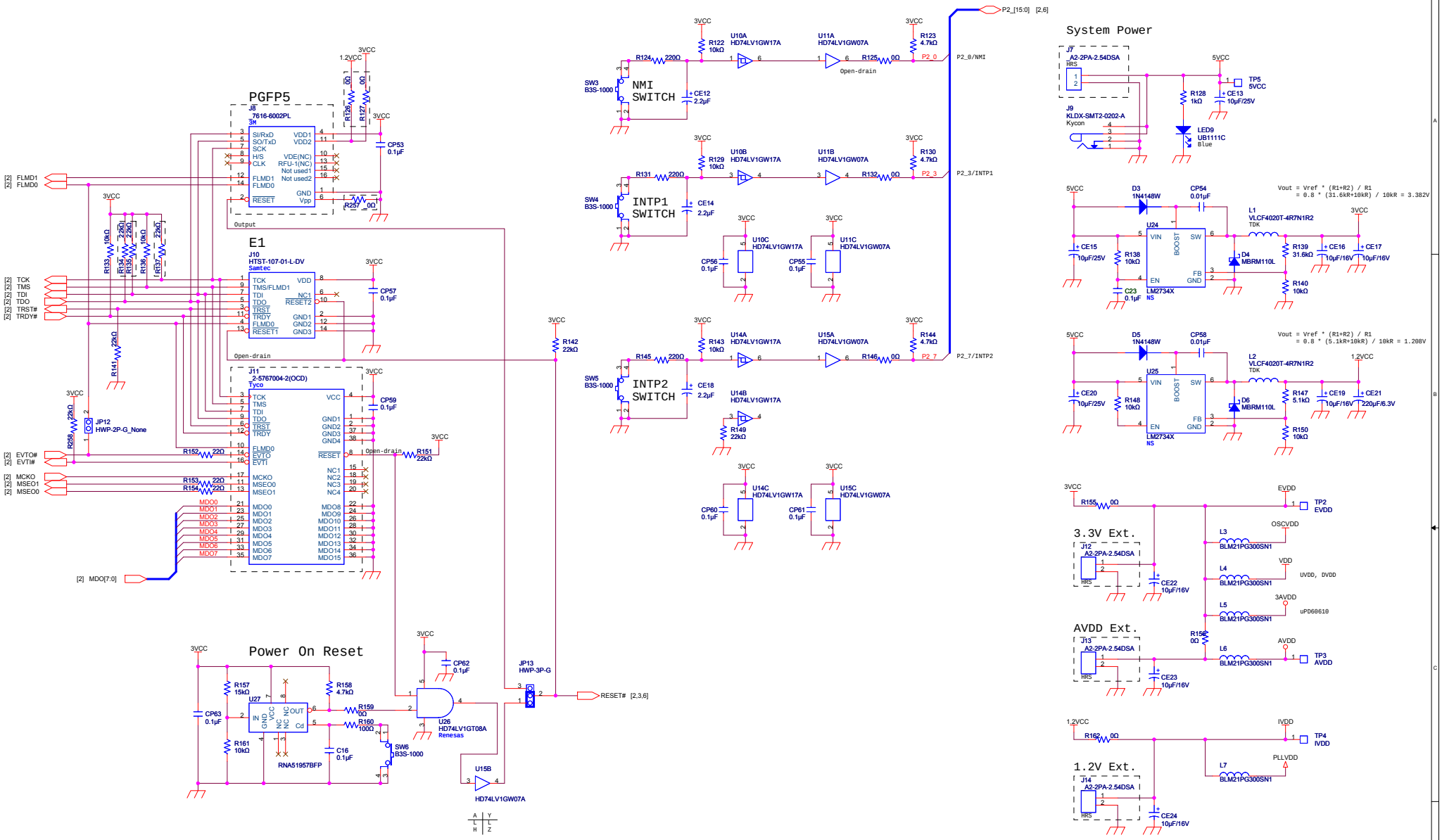

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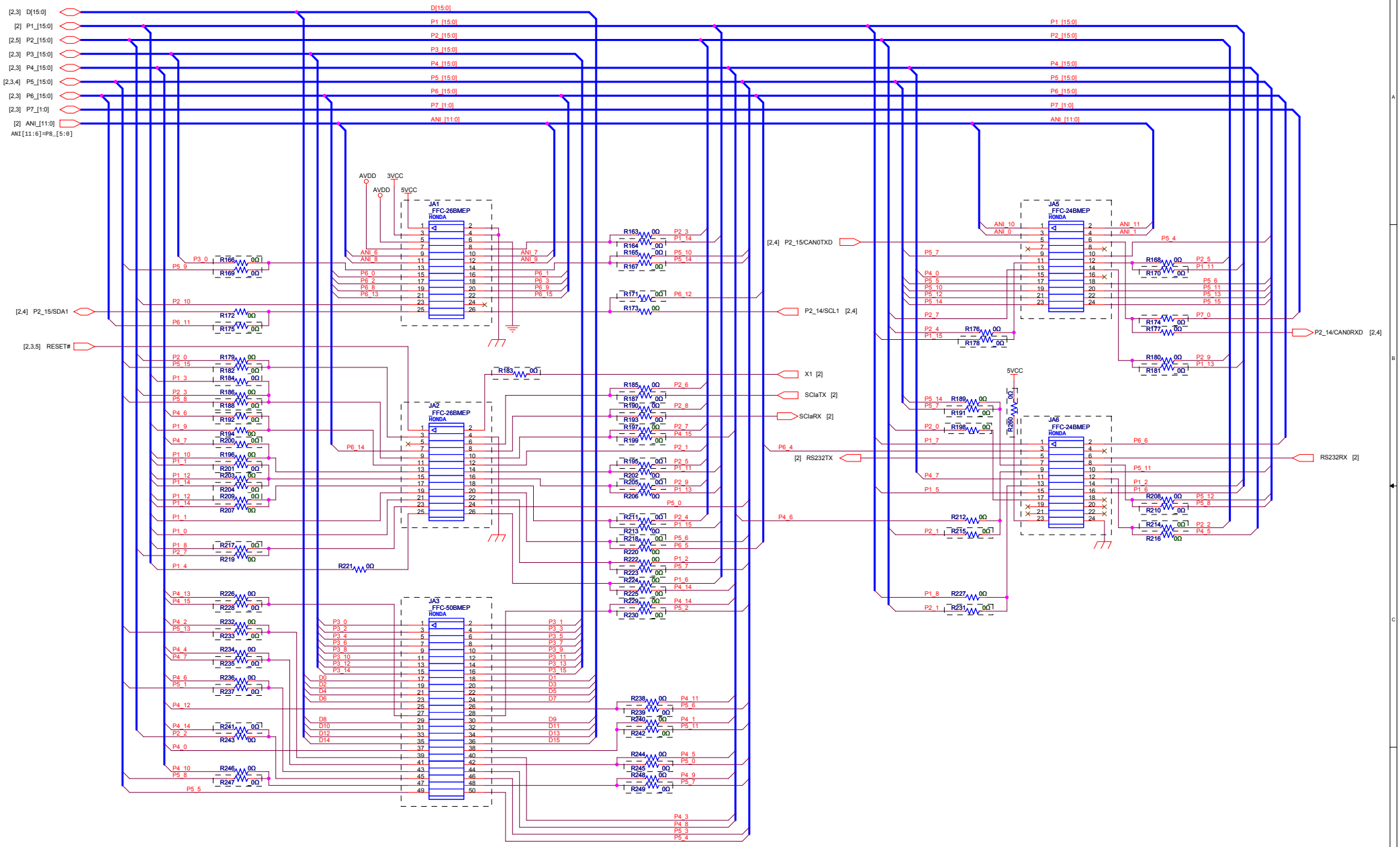

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		Page	Summary
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Colophon 1.2

V850E2/ML4 CPU Board
R0K0F4022C000BR

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