User’s Manual

QB-70F3534-PD
QB-70F3532-PD

IECUBE2-POD’s for V850E2/Dx4

Hardware

Target Devices

µPD70F3522
µPD70F3523
µPD70F3524
µPD70F3525
µPD70F3526
µPD70F3532
µPD70F3535
µPD70F3536
µPD70F3537

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To our customers,

Old Company Name in Catalogs and Other Documents

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- Availability of related technical literature
- Development environment specifications (for example, specifications forthird-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Warning & Caution

CE

This equipment complies with the EMC protection requirements

WARNING

This is a ‘Class A’ (EN 55022: 2006 + A1:2007) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

EEDT-ST-001-20

CAUTION

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tool including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The connectors and/or device pins should not be touched with bare hands.

EEDT-ST-004-10

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Notes for CMOS Devices

1. VOLTAGE APPLICATION WAVEFORM AT INPUT PIN
Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
2. HANDLING OF UNUSED INPUT PINS
Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
3. PRECAUTION AGAINST ESD
A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
4. STATUS BEFORE INITIALIZATION
Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
5. POWER ON/OFF SEQUENCE
In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
6. INPUT OF SIGNAL DURING POWER OFF STATE
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Introduction

Readers

This manual is intended for users who wish to perform debugging using the IECUBE2-POD's.The readers of this manual are assumed to be familiar with the device functions and usage, and to have knowledge of debuggers.

Purpose

This manual is intended to give users an understanding of the basic specifications and correct usage of the IECUBE2-POD's.

Organization

This manual is divided into the following sections.

- General
- Setup procedure
- Settings at product shipment
- Notes
- Optional functions

How to Read This Manual

It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.
This manual describes the basic setup procedures and how to set switches to understand the overall functions and usages of the IECUBE2-POD's.

→ Read this manual in the order of the **CONTENTS**.

To know the manipulations, command functions, and other software-related settings of the IECUBE2-POD's.

→ See the user's manual of the debugger (supplied with the IECUBE2-POD's) to be used.

Conventions

Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH

Prefix indicating power of 2 (address space, memory capacity):
K (kilo): $2_{10} = 1,024$
M (mega): $2_{20} = 1,024_2$

Terminology

The meanings of the terms used in this manual are described in the table below.

Term	Meaning
Target device	This is the device to be emulated.
Target system	This is the system to be debugged (system provided by the user). This includes the target program and the hardware provided by the user.
IECUBE2™	Generic name for Renesas Electronics high-performance, compact in-circuit emulator.
POD	This is IECUBE2 peripheral to interface with the target system.

Related Documents

Please use the following documents in combination with this manual.
The related documents listed below may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Development Tools (User's Manuals)

Document Name	Document Number
User's Manual IECUBE2-POD for V850E2/Dx4	This manual
User's Manual(Preliminary)IECUBE2 main (QB-V850E2) In-Circuit Emulator	ZUD-CD-10-0092 (actual)

Caution **The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing, etc.**

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1. Circumstances not covered by product guarantee

- If the product was disassembled, altered, or repaired by the customer.
- If it was dropped, broken, or given another strong shock.
- Use at overvoltage, use outside guaranteed temperature range, storing outside guaranteed temperature range.
- If power was turned on while the AC adapter, interface cable, or connection to the target system was in an unsatisfactory state.
- If the cable of the AC adapter, the interface cable, the target cable, or the like was bent or pulled excessively.
- If an AC adapter other than the supplied product was used.
- If the product got wet.
- If the product and target system were connected while a potential difference existed between the GND of the product and the GND of the target system.
- If a connector or cable was connected or disconnected while power was being supplied to the product.
- If an excessive load was applied to a connector or cable.
- If the product is used or stored in an environment where an electrostatic or electrical noise is likely to occur.

2. Safety precautions

- If used for a long time, the product may become hot (50 to 60°C). Be careful of high temperature burns and other dangers due to the product becoming hot.
- Be careful of electrical shock. There is a danger of electrical shock if the product is used as described above in 1.1 Circumstances not covered by product guarantee.
- The AC adapter supplied with the product is exclusively for this product, so do not use it with other products.

Table of Contents

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List of Tables

1. General

Each POD is part of an in-circuit emulator system for emulating the target devices shown below.
Hardware and software can be debugged efficiently in the development of systems in which the target device is used. This manual describes basic setup procedures, hardware specifications, system specifications, and how to set switches. For the whole system, both User's Manual's, this and the IECUBE2 User's manual are mandatory.

Table 1-1 Target devices subject of emulation

Device	Nick name	Package	Frequency	Internal flash memory	Internal RAM	vRAM	POD
			[MHz]	[kB]	[kB]	[kB]	
µPD70F3522	DJ4	QFP144	80	256	24	-	QB-70F3534-PD
µPD70F3523	DJ4	QFP144	80	512	48	-	QB-70F3534-PD
µPD70F3524	DJ4	QFP144	120	1024	96	-	QB-70F3534-PD
µPD70F3525	DJ4	QFP144	120	2048	192	-	QB-70F3534-PD
µPD70F3526	DJ4	QFP144	120	3072	256	-	QB-70F3534-PD
µPD70F3532	DN4-H	BGA352	160	3072	128	vRAM i/f	QB-70F3532-PD
µPD70F3535	DP4-H	BGA408	160	3072	256	3072	QB-70F3534-PD
µPD70F3536	DP4-H	BGA408	160	3072	256	5120	QB-70F3534-PD
µPD70F3537	DP4-H	BGA408	160	3072	256	8192	QB-70F3534-PD

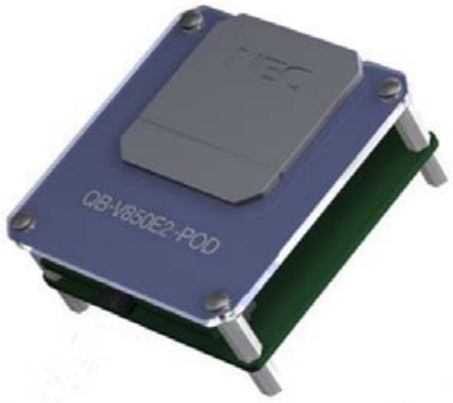
The QB-70F3532-PD emulates the µPD70F3532 device. For using profiling function on other devices, this POD could be used (refer to chapter 3 too).

1.1 Hardware Specifications

Table 1-2 Target specifications

Parameter		Specifications
Target system Interface Voltage	CVDD,MCVDD	1.1 to 1.3V
	ExVDD,AVDD,OSCVDD,SMVDD,REGxVDD	2.7 to 5.5V
	RVDD,BxVDD,FVDD,DVDD	3.0 or 3.6V
Maximum operating frequency		160 MHz
Capability of main clock oscillator		4 to 20MHz
2x Ring internal oscillator		8MHz & 240kHz (typ.)
Sub external oscillator		32kHz (typ.)
Main external oscillator		4MHz (typ.)
Operating temperature range		-0 to 40°C (No condensation)
Storage temperature range		-15 to 60°C (No condensation)
External dimensions		55 mm x 55 mm
Power Consumption	Supplied by IECUBE2	(part of the IECUBE2 power consumption)
	Supply from target system	(approx. device power consumption or less)
Weight		Approx. 40g
Host Interface		Control i/f to IECUBE2

Figure 1-1: Description of IECUBE2 POD



1.2 System Specification

This section shows the QB-70F3534-PD / QB-70F3532-PD system specifications. For the usage of the debugging function, refer to the documentation of the debugger.

Parameter		Specification
Emulation memory capacity	Internal FLASH	3 MB
	Internal RAM	256KB
	Internal Video RAM	8 MB / None *
	External memory	None / vRAM i/f *
Program execution functions	Real-time execution function	Available
	Non-real-time execution function	Available (Step execution in source level depends on debugger)
Event functions	Detection of execution	Pre-execution: 4 points (only for break function) Post-execution: 8 points
	Detection of access	6 points
	Pass counter	12 bits
	Sequential	4 steps
	Modification when running	Available
Break functions	Hardware break	4 Available
	Software break	96 Available
	Other	Trace full break, forced break, timer overflow break
Trace functions	Trace data types	Branch-source PC, branch-destination PC, access data, access address, R/W status, time stamp, DMA access data, DMA access address, DMA R/W status, DMA transfer count, DMA channel number
	Trace events	Delay trigger, section, qualify
	Memory capacity	512K frames
	Other	Trace full stop
Time measurement functions	Measurement clock	200 MHz
	Measurement objects	Beginning through end of program execution Start event through end event (6 sections)
	Maximum measurement time	Approximately 195 hours (When using measurement-dedicated clock divided by 32)
	Minimum resolution	5 ns
	Measurement results	Execution time (Start through end of execution) Maximum, minimum, average, pass count (between events)
	Other	Timer overflow break function (1 point)
Other functions		Open break function, peripheral break function, mask function(_RESET, internal reset)

Note: *(QB-70F3534-PD / QB-70F3532-PD)

1.3 Adapters, Connectors

The following adapters and connectors are necessary to connect the POD to the target system. These adapters and sockets are sold separately.

Type	QFP package	BGA package	BGA package
Exchange adapter	QB-144GJ-EA-60T	QB-408F1-EA-61T	QB-352F1-EA-60T
Emulator connector	QB-144GJ-YQ-01T	-	-
Target connector	QB-144GJ-NQ-01T	BSSOCKET408	QB-352F1-NQ-01T

Note: Products of Tokyo Eletech Corporation (http://www.tetc.co.jp)

Figure 1-2 Description of Target Connection Details

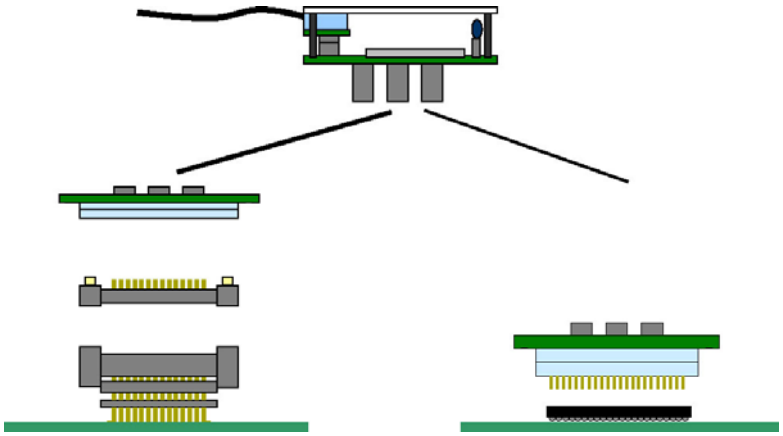
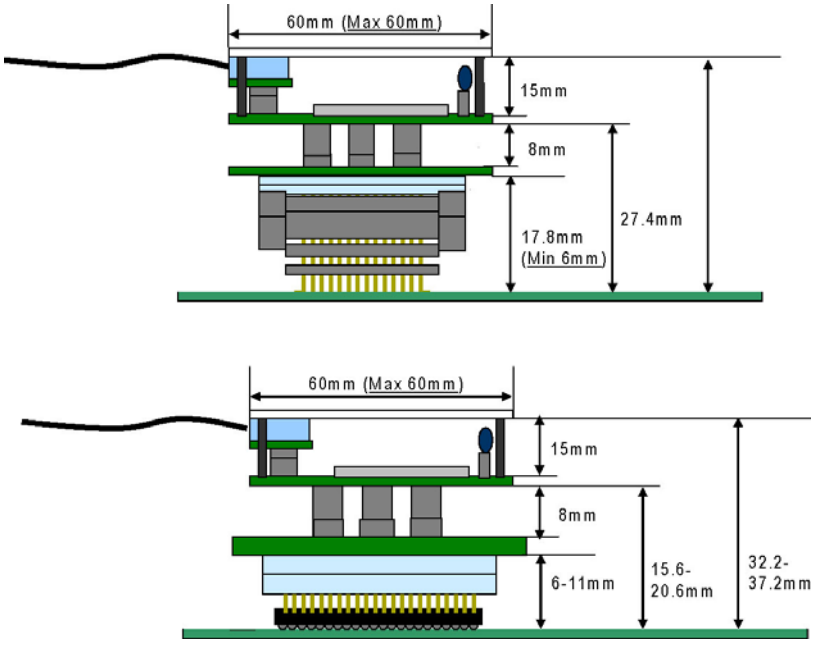


Figure 1-3 Target Connection Details (Height)



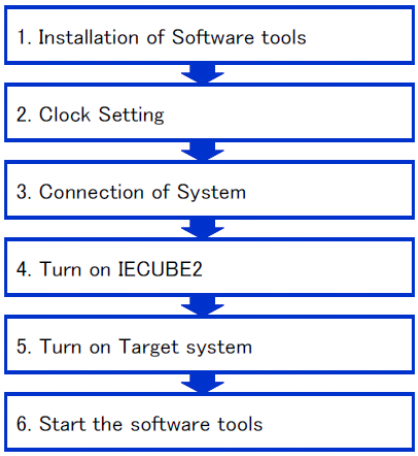
1.4 Package Contents

The packaged items might vary depending on the region in which the product is purchased. Therefore, confirm that the items in the attached packing list are included.

Refer to the actual Package Contents List (PCL) for the Products supplied with the IECUBE2 POD's.

2. Setup Procedure

This chapter explains the IECUBE2 setup procedure. Setup can be completed by performing installation/setup in the order in which it appears in this chapter.



Remark: Observe the power up sequence. Do not power on target, if POD is not powered.

2.1 Installation of Software tools

Before setting up hardware, install the necessary software tools. For details about how to do so, see the documents supplied with the software tools.

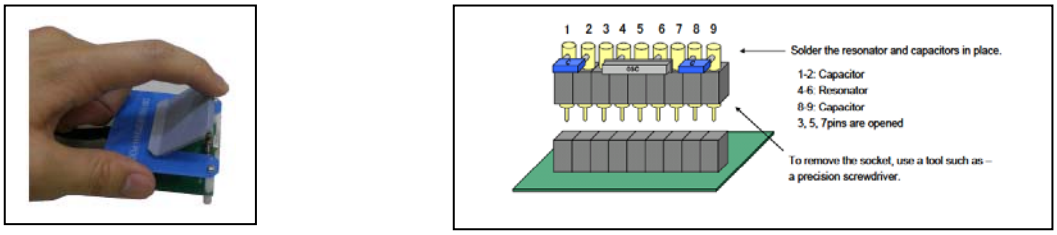
2.2 Clock Settings

The main clock is generated by the oscillator in the emulation POD. In case using the default frequency of the crystal, the setting is not required to be changed. In case of customer specific frequency modification is necessary, see following procedures.

Caution **This product does not support clock input from target. Sublock is fixed to 32.768kHz.**

(1) Open the emulation POD cover as shown below.

Figure 2-1 Clock setup



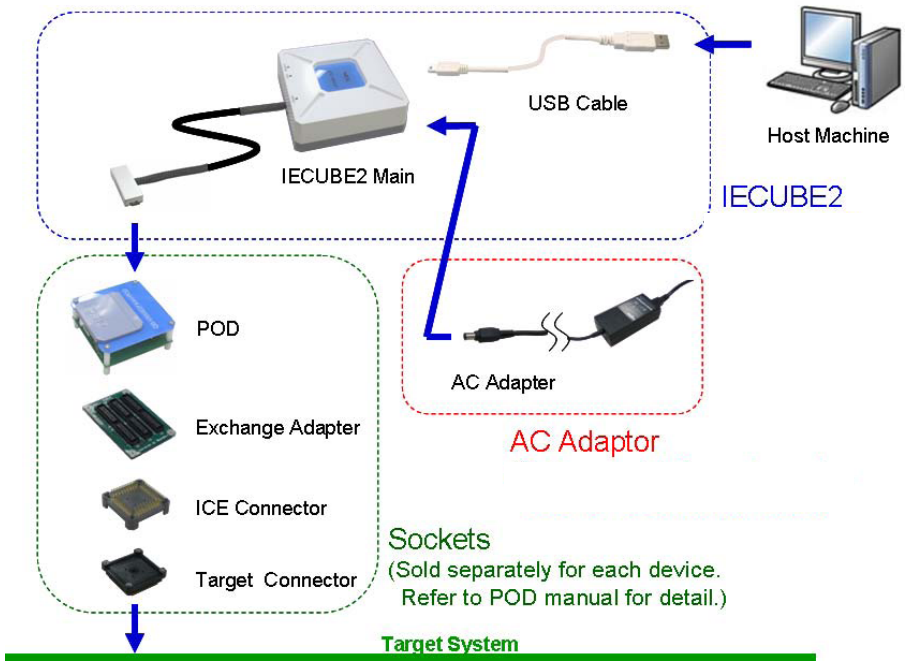
(2) Mount the resonator and capacitors onto the parts board in the emulation POD.
(3) Close the emulation POD cover.

Factory setting: 4MHz crystal is mounted upon shipment

2.3 Connection of System

This section describes how to mount and connect components including connectors. Mount the target connector onto the target board. For details about how to do so, see the document supplied with the connector. For details and setup about IECUBE2 refer to the IECUBE2 User's Manual.

Figure 2-2 System setup



0) Connecting POD and IECUBE2 main. Remove top cover of the POD using a screw driver for the four screws. Plug the cable connector onto the POD connector CN1. Observe the direction. Mount the top cover with the four screws.

1) Soldering Target Connector: Mount the target connector onto the target board. For details about how to do so, refer to the document supplied with the connector.

2) Connecting ICE Connector: Plug the ICE connector to the target connector. For details about how to do so, refer to the document supplied with the connector.

3) Connecting Exchange Adapter: Note the position of pin 1 (positioned at the cut corner) and connect the exchange adapter to the ICE connector (144QFP only) or to the target connector (408BGA or 352BGA only).

4) Connecting POD and target system: Plug the POD to the exchange adapter. Be careful not to excessively bend the cable.

> **Caution:** Do not put any pressure on the small devices on the POD (on PCB top and bottom side). They may be damaged in that case.

To remove the exchange adapter, use the stick included within the IECUBE2 package to gradually pull up the sides of the adapter (refer to IECUBE2 User's Manual).

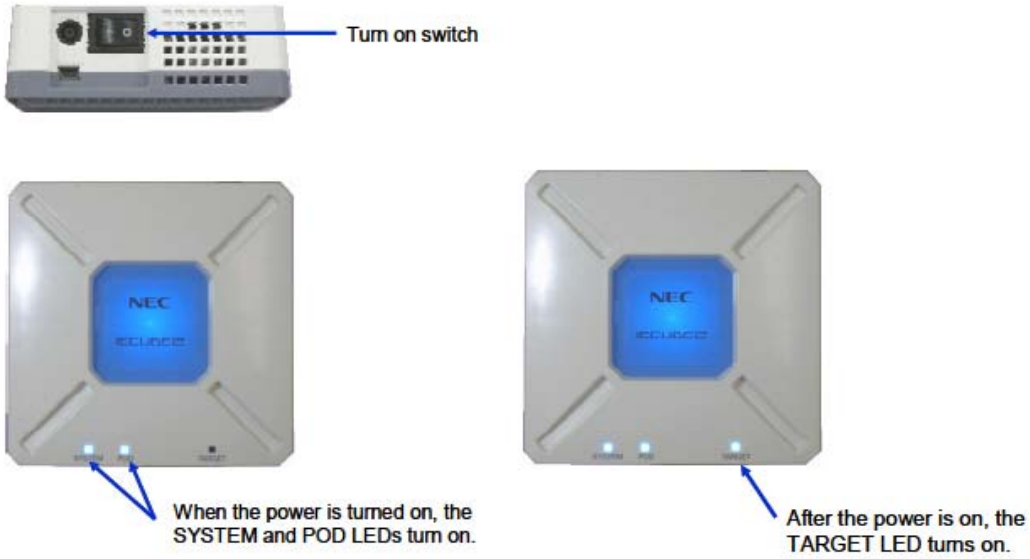
5) Connecting to the IECUBE2 the USB cable and AC adapter: Connect the USB cable and power supply adapter. At this time, make sure that IECUBE2 and the target system are not on.

6) Turn on IECUBE2: At this time, make sure that the target system is not on. When the power is turned on, the System and POD LED turn on. If these LEDs blink or remain off, IECUBE2 might be faulty.

Remark: When the power is turned on for the first time, Plug and Play starts and sets up the USB driver. Continue setup according to the wizard.

7) Turn on the target system: After the power is on, the TARGET LED turns on. If the LED remains off, connectors might be connected poorly, the emulation POD cable might be broken, or voltage might not be correctly applied to the power supply pins of the micro-controller (such as VDD).

Figure 2-3 Turn on system



2.4 Start the Software Tool

After the above procedure, the system starts up. For downloading and debugging a program by using the GHS MULTI generic debugger, please make sure that you have establish a USB connection between the host and the IECUBE2 emulation environment. For doing so, please specify the following command string within the first line of your debugger script file (*.rc file). Example:

Stand-alone mode (without connected target):

```
connect 850eserv2 -iecube -e2 -ip=C:\GHS\v850e -df=dfxxxx.800 -id ffffffffffffffffffffffff
```

Target mode (with connected target):

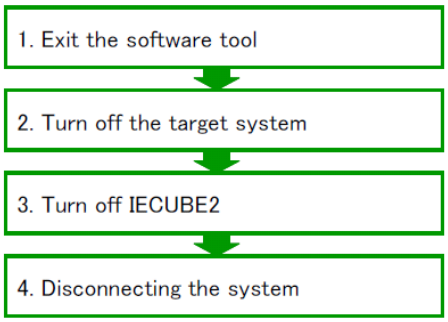
```
connect 850eserv2 -iecube -e2 -ip=C:\GHS\v850e -df=dfxxxx.800 -tc -id ffffffffffffffffffffffff
```

Please note, when -df, -ip and environment variable DEVICE_FILE, IEPATH are specified simultaneously, the device file and the directory specified by -df and -ip are given to priority.

For details about debugging procedures, see the document supplied with the software tool.

2.5 Shut down procedure

Shut down the system according to the procedure below. Note that shutting down the system incorrectly might damage IECUBE2.



Remark:
Observe the power down sequence.
Do not power down POD, if target is still powered.

3. Differences between Target Device and POD

This chapter explains the differences on using the POD to the V850E2/Dx4 devices.
There are other User's Manuals important, covering the specific description of the devices, the Core Architecture and the IECUBE2. Refer to these versions or check for current version:

Hardware	UM -V850E2/Dx4 U20018EE0V3UM00
Architecture	UM -V850E2/Dx4 U17135EJ1V1UM00
Customer Notification	CN -V850E2/Dx4

Customer Notification	EEDT-OP-0044 (for QB-70F3534-PD)
Customer Notification	EEDT-OP-0046 (for QB-70F3532-PD)

Note: Download the documents from the Renesas web site.
Renesas Electronics website: http://www.renesas.com

3.1 Electrical differences

The following listed electrical characteristics may differ from tool to the devices.

3.1.1 Electrical differences on power pins

The current load on all power pins may differ between tool and device. This is valid for all power pins due to the usage of target connectors, ea-adapter, additional PCB wiring and internal switches on the POD.
Power groups are handled different on POD side. For example power is supplied statically internal.

Internal static supply for Core, Flash, Oscillator and eDRAM power.
Internal supply for E0VDD and REGCVDD in case of target voltage is less 3.0V.
All other power pins will be supplied from target.

All VSS-pins are short circuited inside the tool to a common ground plane.
REG0VSS is used to detect the target-hardware and is not connected to ground, but to a weak pull-up resistor. Connect it to ground on the target hardware as usual.

Internal supply for E0VDD and REGCVDD is less than on target side.

Due to the usage of schottky diodes for these power on the POD, the supplied device part is approx. 0.2V less than on target side.

Ports - P0, JP0, Wake output levels are approx. 0.2V lower than on device
LVI - effective levels are approx. 0.2V higher than on device
POC - effective levels are approx. 0.2V higher than on device
VLVF - not supported

3.1.2 Target power on

REG0VDD is used for target power on detection. It is considered to be "on" when > 2.7V. The Target LED turns on when target power is over this threshold value.

3.1.3 Electrical differences on port pins

The electrical characteristics of the port pins may differ between tool and device. This is valid for all pins due to the usage of target connectors, ea-adapter and additional PCB wiring for each signal pin.

3.1.3.1 Electrical differences on ADC pins

As any of the analogue input signals and the reference voltage is connected via target connectors, ea-adapter, additional PCB wiring and internal switches on the POD for Vref, the converted values may differ between tool and device.

3.1.3.2 Electrical differences on RSDS pins

As these signals are not routed as different pairs on the POD-PCB, the signal may differ between tool and device.

3.1.3.3 Electrical differences on other pins

IC/FLMD0 has a 12k1 pull-down and may have different input characteristics.
P0.1/FLMD1 has a 100k pull-down (QB-70F3532 only) and may have different input characteristics.
RESETZ is emulated with similar circuit may have different input characteristics.
PWGD is emulated with similar circuit may have different input characteristics.
WAKE is emulated with similar circuit may have different input characteristics.
X1,X2 and XT1,XT2 are not connected to target.

3.2 Functions not emulated by real-chip on the POD

The emulation tool is based on real-chip base. All notifications of the real device applies for the POD too. For this information refer to the customer notification of the device.
For functions which are not emulated by the real-chip on the POD, discrete circuits are used to emulate these functions. For these functions the behavior may differ.

The following listed functions are emulated may differ from tool to the target devices.

3.2.1 RAM contents during deep-stop

When entering deep-stop, 1.2V are not removed. RAM content will remain unchanged.

3.2.2 RESET function

The Reset signal is emulated with an additional circuit. The input is sampled in every 200ns.
After that, true RUN will happen but IECUBE2 needs hundreds of ms delay than on target device.

3.2.3 POC function

POC function is emulated with an additional circuit. The period of POC (Power On Clear) is longer than on a target device, because the emulation chip is also reset. The emulator reconfigures the setting for debugging (e.g. breakpoint) after POC.
Parts of trace data before POC (Power On Clear) may be lost, because the emulation chip is also reset. The trace data FIFO in emulation chip is cleared in case of a POC.

3.2.4 WAKE, PWGD function

Wake and PWGD function is emulated with an additional circuit. The generation time may differ than on the target device.

3.2.4.1 Watchdog timer (WDTA)

During break mode the WDTA is always stopped, even if peripheral break is disabled.
The WDT macro clears WDTA-counter to 0x0000 when you write RUN (WDTE = 0xAC) during break.

3.2.4.2 Reset Controller (RESF)

The RESF SFR is cleared by software reset and on initial startup, as well as by a target reset.

3.2.4.3 Clock Monitor (CLMA)

The CLMA can be triggered in two different ways:
a) The CLMA can be triggered by removing the target clock X1. This can be done by removing the clock board under the plastic lid of the emulator. However it is strongly suggest not to remove the clock board for this feature. We recommend using solution b) instead.
b) The CLMA can be triggered by SFR write.
If the CLMA is triggered (i.e. the main clock fails) during break, the reset will be generated just after restarting from break.

The CLM will continue to operate in peripheral break mode.

3.2.4.4 Peripheral macros will operate during peripheral break when retry registers are accessed

The peripheral clock will run for a few cycles when peripheral break is enabled and an SFR requiring RETRY is accessed in break mode.
Because of this, all peripheral macros will operate for these few cycles.
An access to a SFR can occur by the SFR window, a watch window or the TCL console.

3.2.4.5 iRAM content

The content of the iRAM will be unchanged after a RESET/Target Power off/on.
This behavior may differ than on the target device. In the target device the contents of the iRAM may change to that contents before a RESET/Power off/on.

3.2.5 Target Memory emulation concept (QB-70F3532-PD only)

The emulation of the external memory interface (device uPD70F3532 only) is substituted on POD. This memory interface is not connected to the target application.
The memory interface to the target is clamped at an inactive level with a 10k pull down.
The software may differ for the setup of the memory controller.

Port	SDRAM signal	Termination
P21[6]	CK	33 Ohm series damping
P21[13]	CKE	10k pull-down
P21[8]	CSZ	10k pull-up
P21[14]	RASZ	10k pull-up
P21[15]	CASZ	10k pull-up
P22[0]	WEZ	10k pull-up
P22[6:3]	DQM[3:0]	10k pull-down
P22[2:1]	BA[1:0]	10k pull-down
P26[12:0]	A[12:0]	10k pull-down
P23[15:0]	DQ[31:16]	10k pull-down
P24[15:0]	DQ[15:0]	10k pull-down

Table 3-1 Memory interface pins (on POD)

3.2.5.1 Memory usage

The memory can be used either for application usage, or for profiling, depending on the device subject of emulation and the requirements. It can be used both for code and for data.
The profiling memory can be used by software profiling tools to store information collected during run-time. No hardware support for profiling is implemented in this tool.

Device(s)	Family	Package	(e)DRAM (substitute)	Max. available profiling memory (optional)
uPD70F3522/23	DJ4	LQFP/HQFP144	None	64MB/32MB
uPD70F3524/25/26	DJ4	LQFP/HQFP144	None	64MB/32MB
uPD70F3535	DP4-H	BGA408	3MB	61MB/23MB
uPD70F3536	DP4-H	BGA408	5MB	59MB/32MB
uPD70F3537	DP4-H	BGA408	8MB	56MB/32MB
uPD70F3532	DN4-H	BGA352	0..64MB	64MB reduced by the amount of target memory

3.2.5.2 Memory map

The profiling RAM will be located in an area that is usually used for HSFI1 interface (for devices supporting this feature). The HSFI1 interface usually is located in the area from 0xF400 0000-0xF77F FFFF (56MB).
To be able to access the profiling memory this area is reduced according to the following table.
DJ4 devices remain all their features; they just gain the profiling memory.

Mode	HSFI1 size	HSFI1 area	DRAM type	DRAM size	DRAM area	Profiling mem. size	Profiling mem. area
DP4-H	56MB	0xF400 0000-0xF77F FFFF	Internal eDRAM	8MB	0xF780 0000-0xF7FF FFFF	0MB	-
DN4-H	0MB	-	External SDRAM	0..64MB	0xF400 0000-0xF7FF FFFF	0..64MB	0xF400 0000-0xF7FF FFFF
DP4-H profiling	32MB	0xF400 0000-0xF5FF FFFF	Emulation only	8MB	0xF780 0000-0xF7FF FFFF	32MB	0xF600 0000-0xF7FF FFFF

3.2.5.3 Available memory

The amount of (external) available memory is 64MB.
It is implemented as SDR (single data rate) SDRAM (synchronous dynamic random access memory).
The selected RAM device has the following characteristics:

Feature	eDRAM (LEHUA)	Substitution RAM (IS42S32160A-75BL)
Interface	3.3V	Same
Size [bytes]	8M	64MB
JEDEC SDR SDRAM compliant	No	Yes
Bus width [bits]	32bit	Same
Bank address width [bits]	2 (=4 banks)	Same
Row address width [bits]	13	Same
Column address width [bits]	6	9 (A10 is auto-precharge)
Max. frequency (tck) [MHz]	126 (120 + 5% dithering)	Same (133MHz is supported, but not required)
Suitable for SSCG	Yes	Same
Auto refresh	Yes	Same
Auto refresh cycle timing (tREF)	4096/2ms	Same (8192/64ms), more often is no problem)
Refresh cycle timing (tREF)	2ms (4096 cycles)	Same (64ms, more often is no problem)
Self refresh	No	Same (supported, but not required)
Precharge all	No (at init only)	Same (supported, but not required)
Auto precharge	Yes (during read and write)	Same
Refresh command timing (tRC) [CLKs]	2	9 (70ns)
CAS latency (tRCD) [CLKs]	3	Same (and 2)
Activate timing (tRCD) [CLKs]	2(2/4)	3 (20ns)
Command period (tRP) [CLKs]	2	3 (20ns)
Burst (4) allowed	Yes (sequential address only)	Same (interleaved also supported, but not required)
Burst abort	No	Same (supported, but not required)
Mode setting pattern	(see SDM for pattern)	Same (more features supported, but not required)
Mode timing (tMRD)		2CLKs
DQM during read	Not supported	Same (supported, but not required)

For setup refer to Hardware UM -V850E2/Dx4 – (chapter 37)

3.3 Cautions

3.3.1 Data flash read access

The data flash read access is only 32 bit (GHS memview)

3.3.2 Data flash read access

The iRAM ECC error occurs, when accessing unused areas. This is same behavior as on device.
In case of power down iRAM content will not be deleted and ECC error will not occur; may be different from device.

3.3.3 Reset issued by the debugger

A reset issued by the debugger (e.g. "target rst") will behave the same way as power-cycling the device. I.e. the status SFRs RESF and SRESF will be cleared.

3.3.4 Reset during break mode

A reset applied to the target RESETZ pin will not be handled if the debugger is in break mode. The reset will be lost unless it is held active until the application starts to run again.

3.3.5 Flash

The flash lifetime for data and code flash on the POD, as it is real chip based, is the same as on device.

The User program is downloaded to the flash memory of the device mounted on POD. However, it is recommended to download the application program at the beginning of a debug session in order to guarantee proper operation.

In case of repair of a POD, the Flash contents will be cleared during repair.

3.3.6 FLMD0 during TRESETZ active

If target TFLMD0 is clamped to High level during TRESETZ, the POD will not be functionable.

3.3.7 AHB time out during memview

The AHB time out is set to unlimited (because of GFX issue, ETAWRL = 0x0000)

If you debug the below sequence and have a memory window (memview GHS) with eDRAM contents open, the debugger will loose connection as soon as you set the memory controller into idle state.

```
do
  {
   PROTCMD5  = 0x000000A5;          // write A5 fixed value to protection command register
   GSSDICTRL = 0x00000001;          // write desired value to destination
   GSSDICTRL = 0xFFFFFFFE;          // write bit-wise inversion to destination
   // make sure to close the debugger memory window here
   GSSDICTRL = 0x00000001;          // write desired value to destination
  }  while ( _PROTS5ERR == 1 );     // check error state
 while ( GSSDICTRL != 3 );          // wait for idle request acknowledge
```

3.3.8 Single stepping entry of standby modes

Summary:
Debugger might loose connection and in most cases it is able to resume operation after system wake up. Furthermore, by temporary (i.e. in a debugger data window) masking the (normally unmasked) debugger wake up flag it is possible to debug the deep stop sequence. Set the debugger connection timeout to be long enough for another wake up event to occur.

Additional Info:
The connection loss is not influenced by any data or memory window.

Disabling debugger wake up for ISO1only does not prevent the connection loss issue and still and does not solve the debugging of the deep stop sequence for ISO0. And additionally, after debugger wake up the system is not really operational, as the ISO1 is still disabled.

Details:
Case 1: WUFH0 bit cleared, WUFH1 bit set (wake up by debugger enabled only for ISO0)
a) Stepping through deep stop entry sequence:
- For ISO1: no problem
- For ISO0: - as expected immediate wake up after DS entry (in the debugger window you see the status: HARDWARE STOP, but in fact there is no DS entry, as the software just continues without "going through reset")
The debugger does not lose connection independent from any memory or data windows open

b) Stepping over deep stop entry sequence:
The DS mode is reached as expected. Wake up by debugger works for ISO0, ISO1 remains stopped.
The debugger does not looses connection independent from any memory or data windows open.

Case 2: WUFH0 bit cleared, WUFH1 bit cleared (wake up by debugger enabled for ISO0 and ISO1)
a) Stepping through deep stop entry sequence :
- For ISO1: as expected no standby, so the software remains in a while loop waiting for the ISO1 to report stand by mode.
- For ISO0: no DS entry attempt - the software waits for ISO1
The debugger does not crash or lose connection independent from any memory or data windows open

b) Stepping over deep stop entry sequence :
The DS mode is reached as expected.Target: CPU status (0x8): HARDWARE STOP. Wake up by debugger works for ISO0 and ISO1. The debugger does not crash or looses connection independent from any memory or data windows open.

Case 3: WUFH0 bit set, WUFH1 bit set (wake up by debugger disabled for ISO0 and ISO1)
a) Stepping through deep stop entry sequence :
- For ISO1: no problem
- For ISO0: after completing the last write command of the protected sequence that sets the ISO into deep stop the debugger can't set the breakpoint for the next instruction and might loose connection. It is not influenced by any open data or memory window. The debugger looses connection to the target and tries to reconnect. After a while (connection timeout period) it shows a dialogue box asking if you want to continue waiting or terminate the connection. If you choose to continue and generate a valid wake up event the debugger resumes operation at the expected entry point (reset

vector). This was a bit different for the umbrella device (as far as I remember ;) There a resume of operation did not work.

b) Stepping over deep stop entry sequence :
The DS mode is reached as expected. In the debugger command window it shows:
Target: CPU status (0x8): HARDWARE STOP. Wake up by debugger of course does not work for ISO0 and ISO1. An attempt to set a breakpoint or a click on the debugger stop button leads to connection loss as described above. If you generate a valid wake up event before the connection timeout occurs the debugger resumes operation at the expected entry point (reset vector). After the dialogue box occurrence (connection timeout) the debugger cannot resume after wake up. But it is still able to reset the target.

Case 4: WUFH0 bit set, WUFH1 bit cleared (wake up by debugger disabled for ISO0 and enabled for ISO1)
This case is not used.

3.3.9 Not supported functions

The following functions are not supported by the POD
OCD
Boundary Scan
FP5 programming