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RENESAS

User's Manual

μPD4992

8-bit Parallel I/O Calendar Clock

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[MEMO]

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CHAPTER 1 OUTLINE OF μPD4992

The μPD4992 is a CMOS IC that inputs or outputs 8-bit parallel real-time clock or calendar data from or to a microprocessor based system.

This IC has seven types of internal counters: year, month, day, date, hour, minute, and second. The hour counter can operate in 12-hour or 24-hour mode.

This IC can operate at a voltage of 2.4 to 5.5 V, and can use a battery backup. Because a constant-voltage circuit is provided as a reference oscillation source, the current consumption can be kept low and the accuracy can be kept high even if the supply voltage fluctuates.

This makes the μPD4992 ideal for electronic systems requiring a real-time clock function, such as personal computers, word processors, facsimiles, VCRs, and cameras.

1.1 Features

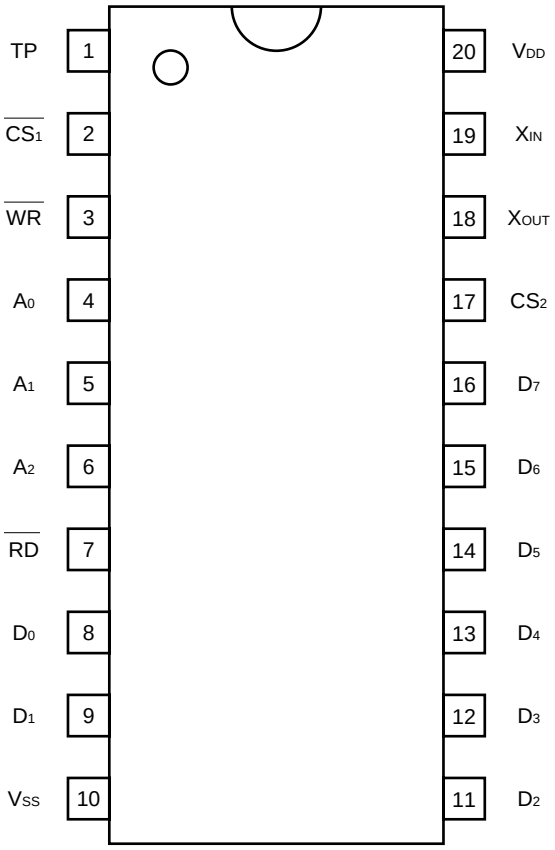
- Internal counters for real-time clock (RTC) (hour, minute, second) and calendar (leap year, year, month, day, date)
- Super low current consumption (I_{DD} = 2 μA MAX. @V_{DD} = 2.4 V)
- Automatic identification and manual setting of leap year
- 12-/24-hour mode selectable
- 3-bit parallel input address bus and 8-bit parallel I/O data bus
- 12 types of interval timer output (can be used as watchdog timer)
- Validity of time data can be checked during backup by internal oscillation stop detection circuit
- High accuracy

Basic specifications

- Reference frequency (crystal oscillation): 32.768 kHz
- Data format: BCD format
- Data function
  Year, month, day, date, hour, minute, and second counters
  The leap year is automatically identified until 2099 (a year whose low-order 2 digits are a multiple of 4 is identified as a leap year), and can be set manually by the user.
  A year can be set using the low-order 2 digits.
  Hours can be indicated in 12- or 24-hour mode.
- Data input/output (D_0 through D_7)
  8-bit parallel I/O mode
  Data writing is enabled by $\overline{WR}$ signal and reading is enabled by $\overline{RD}$ signal to input/output data.
- Timing pulse output (TP output)
  One pulse with a duty factor of 50% can be selected from 2048, 1048, 256, or 64 Hz.
  Or, one interval timer output can be selected from 1/2048, 1/1024, 1/256, 1/64, 1, 10, or 60 s.
- Chip select ($\overline{CS_1}$, CS_2)
  $\overline{CS_1}$ = “H” or CS_2 = “L”: Disables all inputs except X_{IN}.
  $\overline{CS_1}$ = “L” and CS_2 = “H”: Selects all inputs.

1.2 Pin Connections

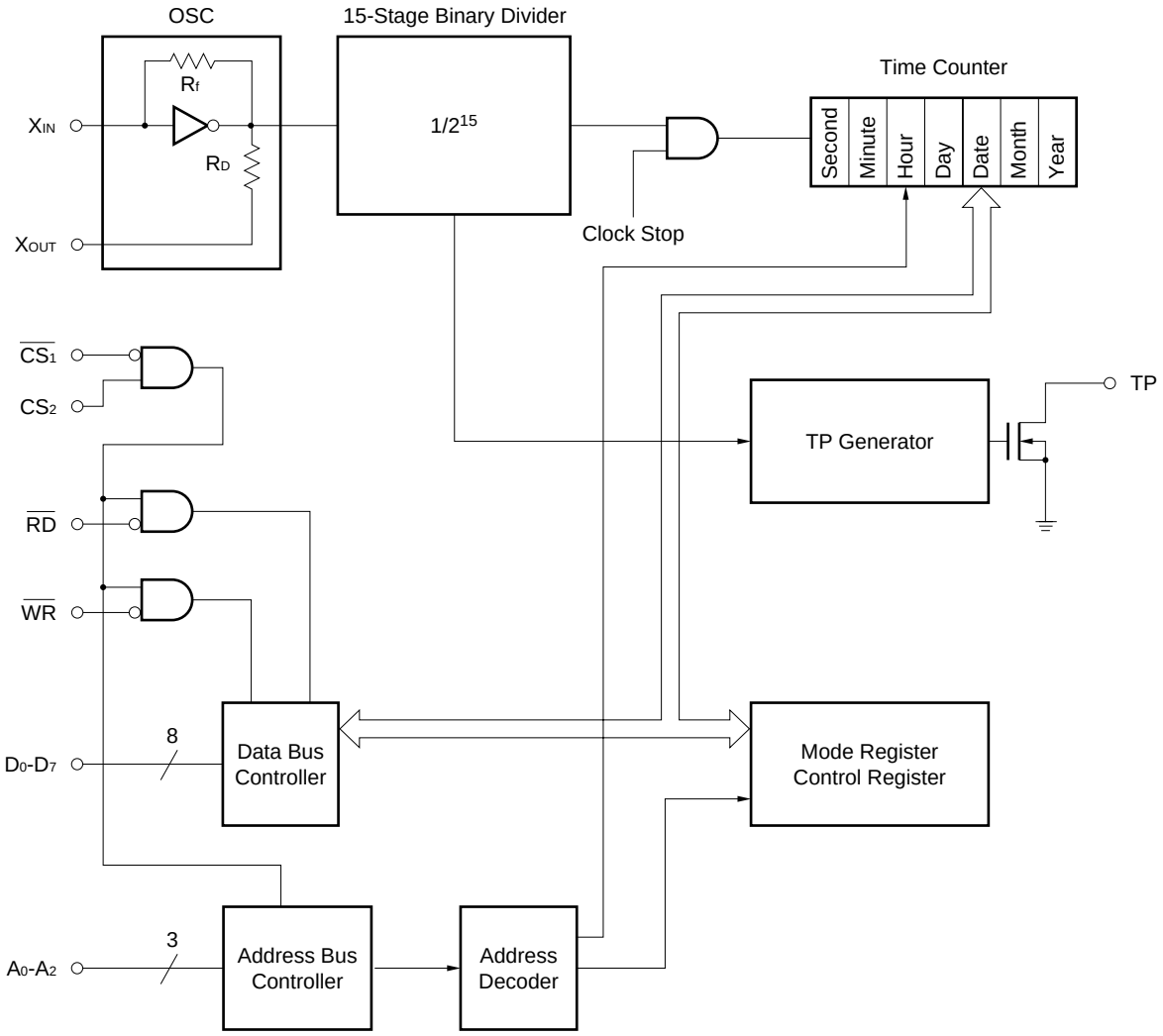
μPD4992CX/μPD4992GS



1.3 Pin Functions

Pin Symbol	Pin Name	Pin No.	Function
$\overline{CS_1}$	Chip select input	2	Access to the internal registers is enabled when $\overline{CS_1}$ = L, CS_2 = H.
CS_2	Chip select input	17	
$\overline{WR}$	Write signal input	3	The contents of the data bus are written to the register selected by inputting an address at the rising edge of this signal.
$\overline{RD}$	Read signal input	7	The contents of the register selected by inputting an address are output to the data bus at the falling edge of this signal.
D_0 to D_7	Data I/O	8, 9, 11 to 16	Data I/O bus.
A_0 to A_2	Address input	4 to 6	Input an address to select an internal register.
TP	Timing pulse output	1	Outputs an interval signal or timing pulse (N-ch open drain output).
X_{IN}	Crystal resonator connecting pin	19	Connect a crystal resonator and a capacitor.
X_{OUT}	Crystal resonator connecting pin	18	
V_{DD}	Power supply pin	20	2.4 V to 5.5 V
V_{SS}	Ground pin	10	Ground

1.4 Block Diagram



1.5 Oscillation Stage and 15-Stage Binary Divider

A reference frequency of 32.768 kHz is obtained by using a 32.768-kHz crystal resonator and a crystal oscillation circuit that uses a CMOS inverter. This reference frequency is divided by 15 to create 1 Hz (1 second) to be input to the time counter.

1.6 Register Configuration

Table 1-2 shows the register configuration.

Table 1-2. Register Configuration

Address				Register Contents							
HEX	A_2	A_1	A_0	b7	b6	b5	b4	b3	b2	b1	b0
0_H	0	0	0	10-second digit				1-second digit			
1_H	0	0	1	10-minute digit				1-minute digit			
2_H	0	1	0	12/$\overline{24}$H	$\overline{AM}$/PM	10-hour digit		1-hour digit			
3_H	0	1	1	Leap year control		Leap year counter		Date digit			
4_H	1	0	0	10-day digit				1-day digit			
5_H	1	0	1	10-month digit				1-month digit			
6_H	1	1	0	10-year digit				1-year digit			
7_H	1	1	1	Mode register				Control register			

1.7 Notes on Use

(1) Be sure to stop the clock (by means of CLK stop) before writing time data. For details, refer to **3.1 Time Setting**.

(2) To change the hour mode between 12-hour and 24-hour, be sure to rewrite AM/PM and the 10-hour digit, as well as the value of b7.

(3) Before changing the setting of the leap year counter, be sure to rewrite the year counter. For details, refer to **2.6 Leap Year Control Register and Leap Year Counter**.

(4) Adjust the oscillation frequency by using TP output. If X_{IN} and X_{OUT} are used to adjust the oscillation frequency, oscillation may be stopped.

(5) While the CPU is in back-up state, keep the CS_2 pin low. For details, refer to **4.5 Power-Fail Circuit**.

(6) Because only the low-order 2 digits of the year code are supported, set the low-order 2 digits of a year. Even when the year changes from 1999 to 2000 (year code: 99 → 00), the μPD4992 correctly counts time. Although leap years are automatically identified until 2099, adjustments such as re-setting the date are necessary in 2100. This is because this IC identifies 2100 as a leap year even though it is not. The other functions of the IC are not affected when the user makes such adjustments.

(7) The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.
The characteristic examples and the description of the application examples in this document are only for this IC alone, and it is still necessary to confirm that there are no problems when the IC is incorporated in your own system designs.

CHAPTER 2 OPERATIONS

2.1 Write Timing

Write data to the internal registers in the following procedure.

(1) Make CS_2 high.
(2) Specify an address value at address pins A_0 through A_2.
(3) Make $\overline{CS_1}$ low.
(4) Make $\overline{WR}$ low, and then high; the values of data pins D_0 through D_7 will be written to the internal registers at the rising edge of $\overline{WR}$.

Table 2-1 and Figures 2-1 and 2-2 indicate the definition of write timing.

Table 2-1. Switching Characteristics

Write cycle (CS_2 = H)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{WC}	150			ns
$\overline{CS_1}$-$\overline{WR}$ reset time	t_{CW}	120			
Address-$\overline{WR}$ reset time	t_{AW}	120			
Address-$\overline{WR}$ setup time	t_{AS}	0			
Write pulse width	t_{WP}	90			
Address hold time	t_{WR}	20			
Input data setup time	t_{DW}	50			
Input data hold time	t_{DH}	0			
$\overline{WR}$-output floating time	t_{WHZ}			50	

Figure 2-1. Write Cycle Timing 1

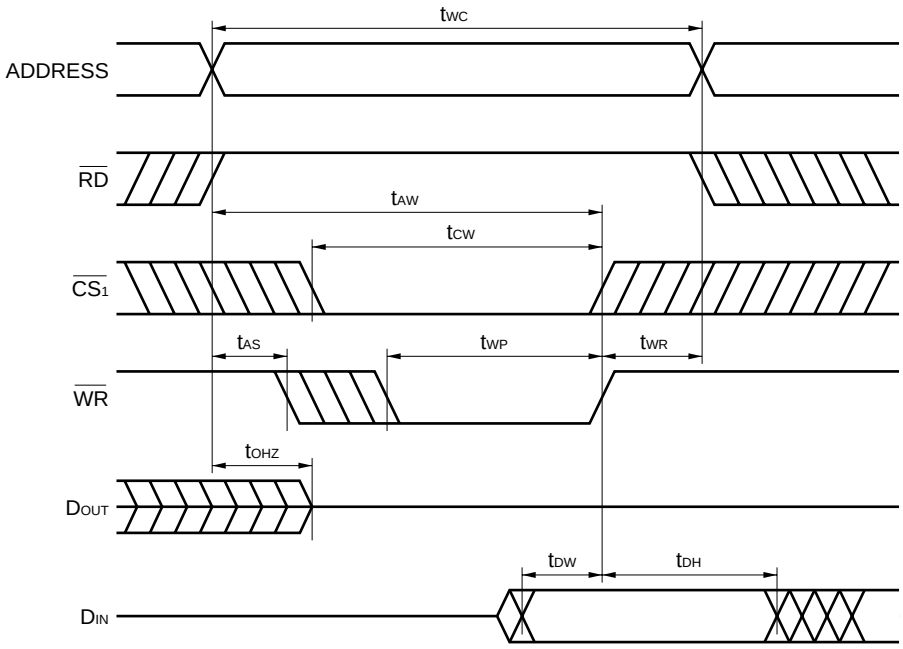
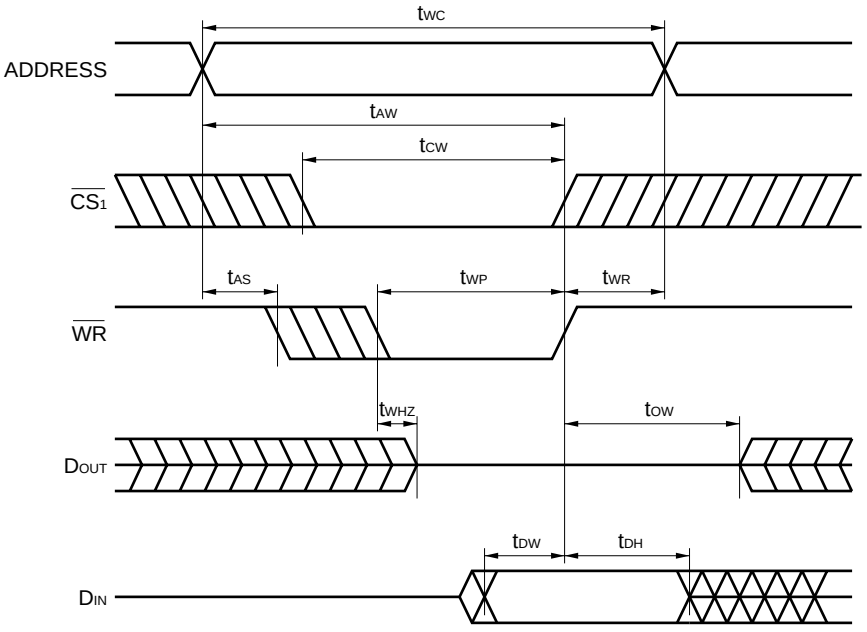


Figure 2-2. Write Cycle Timing 2 ($\overline{RD}$ = V_{IL})



2.2 Read Timing

Read data from the internal registers in the following procedure.

(1) Make CS_2 high.
(2) Specify an address value at address pins A_0 through A_2.
(3) Make $\overline{CS_1}$ low.
(4) Make $\overline{RD}$ low; the value of an internal register will be read to data pins D_0 through D_7 at the falling edge of $\overline{RD}$.

Table 2-2 and Figures 2-3 and 2-4 indicate the definition of read timing.

Table 2-2. Switching Characteristics

Read cycle (CS_2 = H)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Cycle time	t_{RC}	150			ns
Address access time	t_{AA}			150	
$\overline{CS_1}$-access time	t_{ACS}			150	
$\overline{RD}$-output delay time	t_{OE}			75	
	t_{OLZ}	5			
	t_{OHZ}			50	
Output hold time	t_{OH}	15			
$\overline{CS_1}$-output setup time	t_{CLZ}	10			
$\overline{CS_1}$-output floating time	t_{CHZ}	5			

Figure 2-3. Read Cycle Timing 1

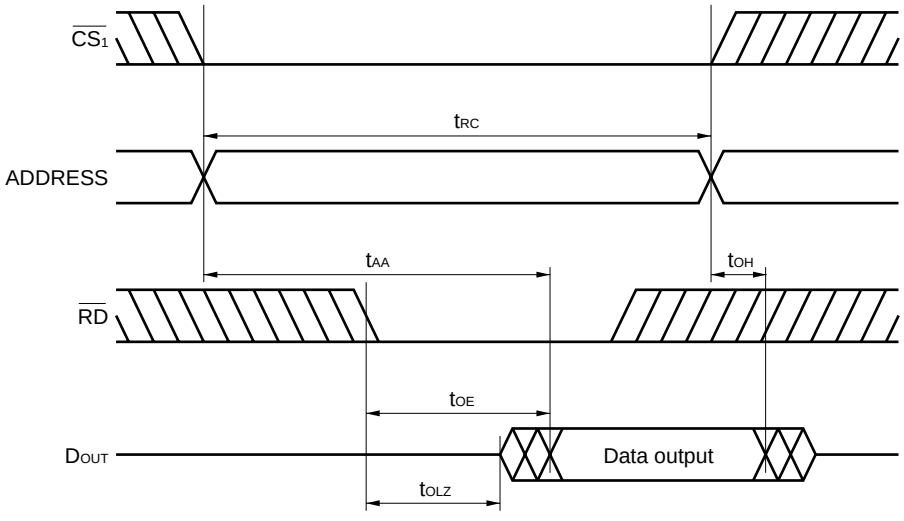
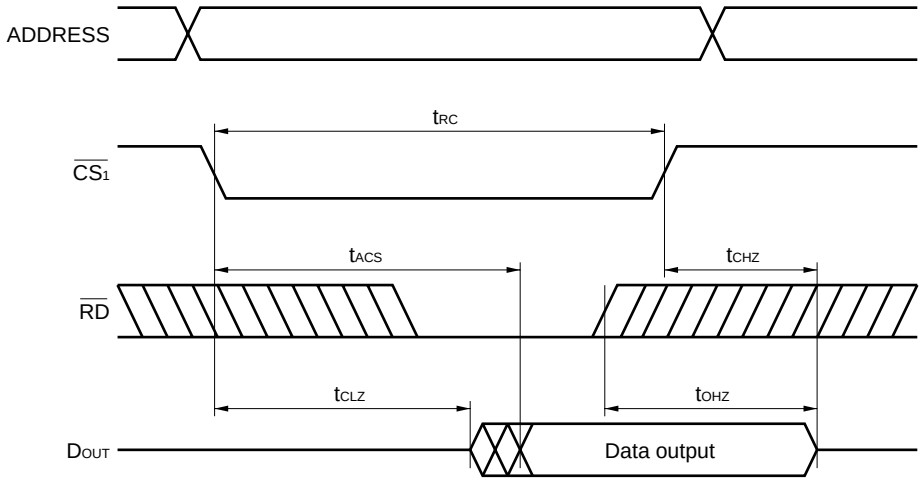


Figure 2-4. Read Cycle Timing 2



2.3 Outline of Registers

The registers of the μPD4992 are allocated as shown in Table 2-3. Addresses 0_H through 6_H are for time data, and address 7_H is a mode register and a control register.

Bits b7 and b6 of address 2_H are a 12/$\overline{24}$H and $\overline{AM}$/PM flags, and b7 through b4 of address 3_H are a leap year control register and a leap year counter.

Table 2-3. Correspondence between Registers and Addresses

Address				Register Contents							
HEX	A_2	A_1	A_0	b7	b6	b5	b4	b3	b2	b1	b0
0_H	0	0	0	10-second digit				1-second digit			
1_H	0	0	1	10-minute digit				1-minute digit			
2_H	0	1	0	12/$\overline{24}$H	$\overline{AM}$/PM	10-hour digit		1-hour digit			
3_H	0	1	1	Leap year control		Leap year counter		Date digit			
4_H	1	0	0	10-day digit				1-day digit			
5_H	1	0	1	10-month digit				1-month digit			
6_H	1	1	0	10-year digit				1-year digit			
7_H	1	1	1	Mode register				Control register			

2.4 RTC Counter (R/W)

Input or output clock data by writing or reading the RTC counter and calendar counter.

The data that can be written are as follows:

Register	Data That Can Be Written
1-second digit	0 through 9
10-second digit	0 through 5
1-minute digit	0 through 9
10-minute digit	0 through 5
1-hour digit	0 through 9
10-hour digit (including flag)	0 through 2 (24-hour mode)/8, 9, C, D (12-hour mode)
Date digit	0 through 6
1-day digit	0 through 9
10-day digit	0 through 3 (except February)/0 to 2 (February)
1-month digit	0 through 9
10-month digit	0 through 1
1-year digit	0 through 9
10-year digit	0 through 9

For the counter data of the 1-hour and 10-hour digits, refer to **Table 2-4**.

The date digit can take a value of 0_H to 6_H and counts up (+1) in synchronization with the 1-day digit. It goes back to 0_H after 6_H. The date of the week is arbitrarily assigned.

Each register is automatically incremented.

While it is possible to write data other than the above or a time that does not actually exist, the registers cannot be correctly incremented in that event. Write only time data that is actually feasible and that is correct.

Example 23 hours 45 minutes 01 second (in 24-hour mode) on Thursday, October 8, 1998

Register	Data (Hex)	b7	b6	b5	b4	b3	b2	b1	b0
Second counter	01	0	0	0	0	0	0	0	1
Minute counter	45	0	1	0	0	0	1	0	1
Hour counter	23	0	0	1	0	0	0	1	1
Leap year, date counter	24	0	0	1	0	0	1	0	0
Day counter	08	0	0	0	0	1	0	0	0
Month counter	10	0	0	0	1	0	0	0	0
Year counter	98	1	0	0	1	1	0	0	0

In this example, the date counter is set so that Sunday is “0”. For the leap year counter, refer to **Table 2-5**.

2.5 12/$\overline{24}$H and $\overline{AM}$/PM Flags (R/W)

The 12/$\overline{24}$H flag selects the 12- or 24-hour mode of the hour counter of the μPD4992.

- 12/$\overline{24}$H flag = 0: 24-hour mode
- 12/$\overline{24}$H flag = 1: 12-hour mode

The $\overline{AM}$/PM flag indicates either morning or afternoon in the 12-hour mode (when the 12/$\overline{24}$H flag = 1).

- $\overline{AM}$/PM flag = 0: Morning (AM 12 hours 00 minutes 00 seconds to AM11 hours 59 minutes 59 seconds)
- $\overline{AM}$/PM flag = 1: Afternoon (PM 12 hours 00 minutes 00 seconds to AM 11 hours 59 minutes 59 seconds)

In the 24-hour mode (12/$\overline{24}$H flag = 0), the $\overline{AM}$/PM flag is always “0”.
Table 2-4 shows the time counter data including the 12/$\overline{24}$H and $\overline{AM}$/PM flags.

Table 2-4. Time Counter Data

Time	24-Hour Mode	12-Hour Mode	Time	24-Hour Mode	12-Hour Mode
AM 1	01H	81H	PM 1	13H	C1H
AM 2	02H	82H	PM 2	14H	C2H
AM 3	03H	83H	PM 3	15H	C3H
AM 4	04H	84H	PM 4	16H	C4H
AM 5	05H	85H	PM 5	17H	C5H
AM 6	06H	86H	PM 6	18H	C6H
AM 7	07H	87H	PM 7	19H	C7H
AM 8	08H	88H	PM 8	20H	C8H
AM 9	09H	89H	PM 9	21H	C9H
AM 10	10H	90H	PM 10	22H	D0H
AM 11	11H	91H	PM 11	23H	D1H
PM 12	12H	D2H	AM 12	00H	92H

2.6 Leap Year Control Register and Leap Year Counter (R/W)

The leap year control register turns the identification of leap years on and off, and enables or disables writing to the leap year counter.

Table 2-5 shows the allocation of the leap year control register. Because the leap year counter does not have to be written again once it has been written, it is usually set to “x0” (disabling writing the leap year counter).

Table 2-5. Leap Year Control Register

b7	b6	Mode
0	0	Identifies leap year, writing leap year counter is disabled.
0	1	Identifies leap year, writing leap year counter is enabled.
1	0	Ignores leap year, writing leap year counter is disabled.
1	1	Ignores leap year, writing leap year counter is enabled.

The user does not have to set the leap year counter if the low-order 2 digits of the year have been written to the year counter. The user can write any data to the leap year counter.

A leap year is identified when the value of the leap year counter is “00”.

Be sure to write data to the leap year counter after setting the year counter. If the leap year counter is set after the year counter, the leap year counter is re-set regardless of the setting of the leap year control register.

Example The leap year counter is automatically set if the year counter is set.

Year	Year counter			Leap year counter	
1997	“10010111”	(97)	→	“01”	(1)
1998	“10011000”	(98)	→	“10”	(2)
1999	“10011001”	(99)	→	“11”	(3)
2000	“00000000”	(00)	→	“00”	(0)
•	•			•	
•	•			•	
•	•			•	
2015	“00010101”	(15)	→	“11”	(3)
2016	“00010110”	(16)	→	“00”	(0)

2.7 Mode Register (R/W)

The mode register to specify TP output and the test mode. Table 2-6 lists the functions of the mode register.

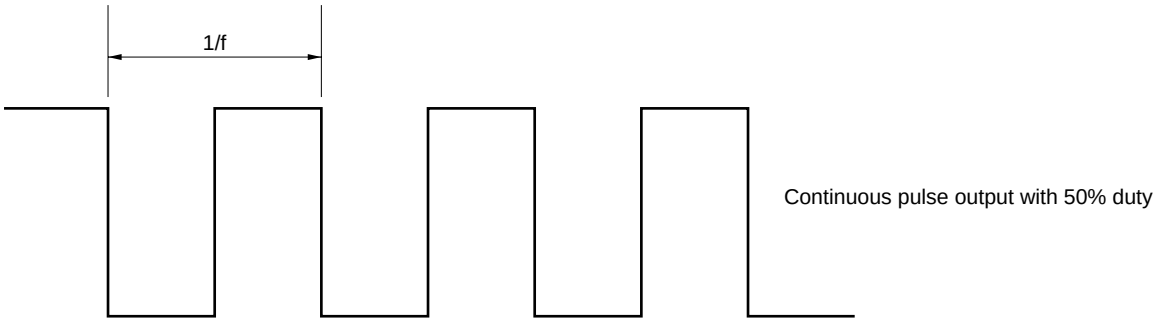
Table 2-6. Mode Register List

HEX	b7	b6	b5	b4	Mode
0_H	0	0	0	0	TP 2048 Hz output
1_H	0	0	0	1	TP 1024 Hz output
2_H	0	0	1	0	TP 256 Hz output
3_H	0	0	1	1	TP 64 Hz output
4_H	0	1	0	0	INT 1/2048 s output
5_H	0	1	0	1	INT 1/1024 s output
6_H	0	1	1	0	INT 1/256 s output
7_H	0	1	1	1	INT 1/64 s output
8_H	1	0	0	0	INT 1 s output
9_H	1	0	0	1	INT 10 s output
A_H	1	0	1	0	INT 60 s output
B_H	1	0	1	1	BUSY signal output
C_H	1	1	0	0	Test mode
D_H	1	1	0	1	
E_H	1	1	1	0	
F_H	1	1	1	1	

2.7.1 TP output (1) (continuous pulse output)

When a value between 0_H and 3_H is written to the mode register, pulses with a frequency of between 64 and 2048 Hz and a duty factor of 50% are continuously output from the TP pin (refer to **Figure 2-5**).

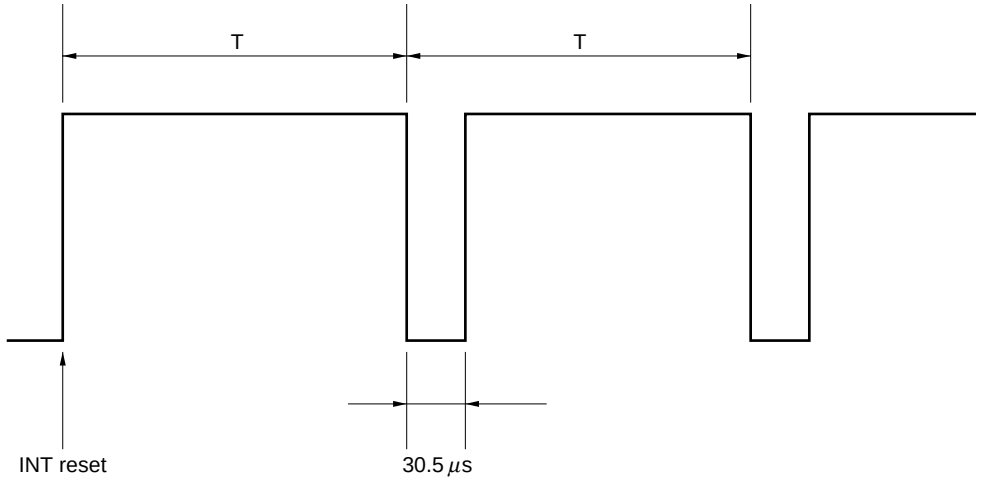
Figure 2-5. Continuous Pulse Output



2.7.2 TP output (2) (interval pulse output)

Pulses are output from the TP pin at intervals of between 1/2048 and 60 seconds when a value between 4_H and A_H is written to the mode register. The pulse width is 30.5 μs (refer to **Figure 2-6**).

Figure 2-6. Interval Pulse Output



2.7.3 TP output (3) (BUSY output)

The BUSY signal is output from the TP pin when B_H is written to the mode register. While this BUSY signal is low, reading the counters is disabled and the counters are internally incremented in this period. The BUSY signal is used to read time data at its rising or falling edge. For an example of using the BUSY signal, refer to **3.2.1**.

2.7.4 Test mode

The test mode is selected when C_H to F_H is written to the mode register. Do not use this mode for normal operation.

2.8 Control Register

The control register sets the clock (CLK) of the RTC counter and controls the TP pin when data is written to it. When it is read, the register is used to check the TP, OSC, and BUSY flags. Table 2-7 lists the functions of the control register.

Table 2-7. Control Register

Access Mode	b3	b2	b1	b0
Write	0	CLK adjust[Note 4]	CLK reset[Note 4]	CLK stop
		0: NOP	0: NOP	0: CLK start
		1: CLK adjust	1: Reset	1: CLK stop
	1	TP enable[Note 1]	INT reset[Note 4]	INT stop
		0: TP = ENABLE	0: NOP	0: INT start
		1: TP = DISABLE	1: Reset	1: INT stop
Read	*	TP flag	OSC flag[Note 2]	BUSY flag[Note 3]
	(Don't care)	0: TP = Z	0: Oscillation stop	0: OFF
		1: TP = L	1: Oscillation	1: ON

Notes 1. When the TP enable flag is set to "1" (TP = DISABLE), the TP pin forcibly goes into a high-impedance state (actually, goes high because a pull-up resistor is connected to the TP pin).

2. When oscillation is stopped and the OSC flag is reset to "0", the OSC flag remains "0" even if oscillation is later resumed. To set the OSC flag to "1", execute CLK reset.
If the OSC flag still remains "0" even after CLK reset has been executed, oscillation remains stopped. If the OSC flag is "0", TP output is disabled.
The OSC flag is reset to "0" on the first power application to the μPD4992.
Be sure to initialize the OSC flag before using it.

3. The BUSY flag is set to "1" while the time counter of the μPD4992 is operating (while reading the counter is disabled).

4. Be sure to return the CLK adjust, CLK reset, and INT reset flags to NOP ("0") after setting these flags to "1". Otherwise, adjust and reset remain valid, and unexpected operation may occur when data is subsequently written.

2.8.1 Write control register

Data writing to the control register is to select whether CLK or TP pin is to be controlled depending on the status of b3.

(1) When b3 = 0

The CLK stop and CLK reset flags are assigned to b0 and b1, respectively.

CLK stop : Stops the 1-second pulse signal to the second digits of the RTC counter to prevent the counter from being incremented.
CLK reset : Resets the 15-stage binary divider (32.768 kHz → 1 Hz).

For details of how to use these flags, refer to **CHAPTER 3**.
The CLK adjust flag is assigned to b2. When b2 = 1, an adjustment of ±30 seconds is made and the second counter is reset (to 00 second). The BUSY flag is 1 while the CLK adjust operation is performed.

- Every minute 00 second to 29 seconds —CLK adjust→ 00 second (digits other than second digits are not affected)
- Every minute 00 second to 59 seconds —CLK adjust→ 00 second + Digits higher than minute digits are incremented.

Incrementing affects all the digits.

Example 11 hours 59 minutes 45 seconds in the afternoon on December 31, 1995
↓ CLK adjust
0 hour 0 minute 0 second in the morning on January 1,1996

(2) When b3 = 1

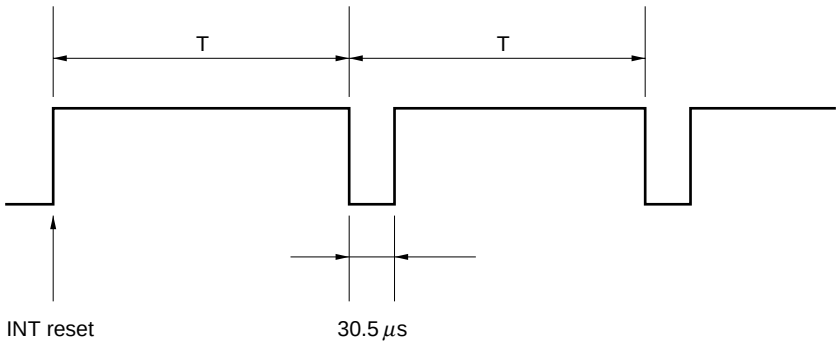
The INT stop, INT reset, and TP enable flags are assigned to b0, b1, and b2, respectively.

INT stop : Stops the internal clock for interval pulse output and retains the status in which the output goes into a high-impedance state. Allows continuous operation of output by releasing the stop mode.
INT reset : Allows the output to go into a high-impedance state regardless of the status of interval pulse output.
Also resets the internal clock for interval pulse. The interval pulse operation continues.
TP enable : Enables TP output. If this flag is disabled, output forcibly goes into a high-impedance state, regardless of the status of the interval pulse output. However, the TP and BUSY flags are not disabled even in this case.

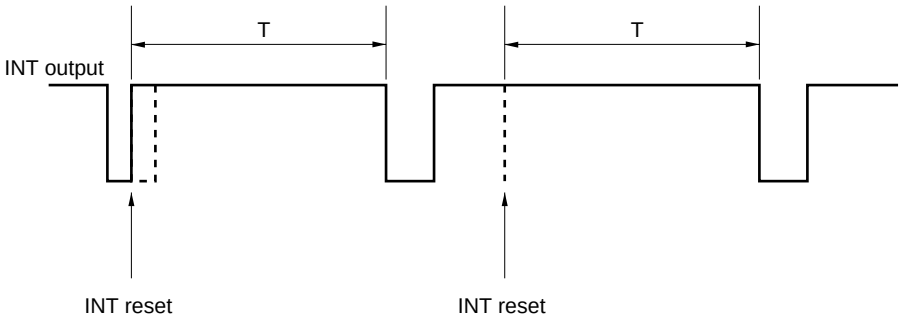
For how to use these flags, refer to **Figure 2-7**.

Figure 2-7. Example of Controlling TP Pin (in INT output mode)

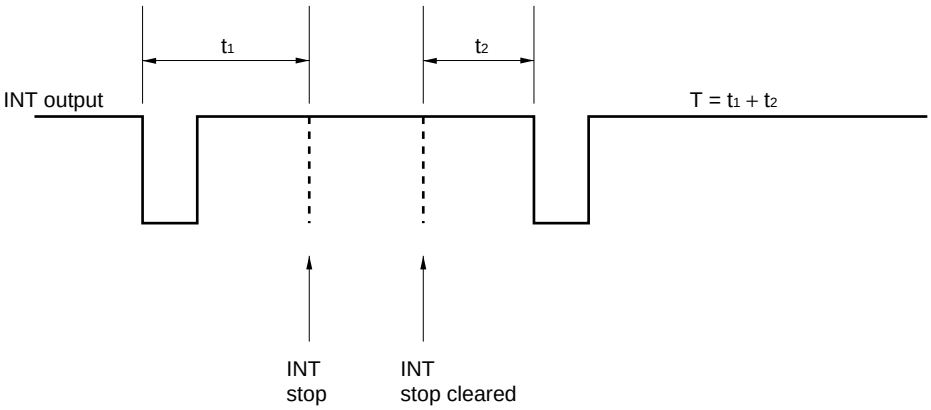
(1) Use of INT reset (1)



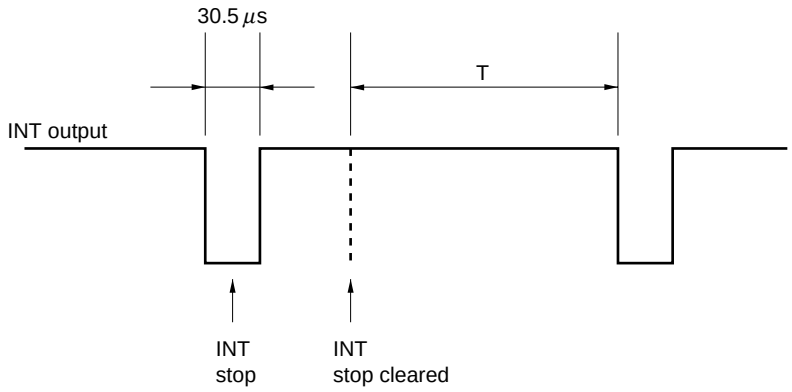
(2) Use of INT reset (2)



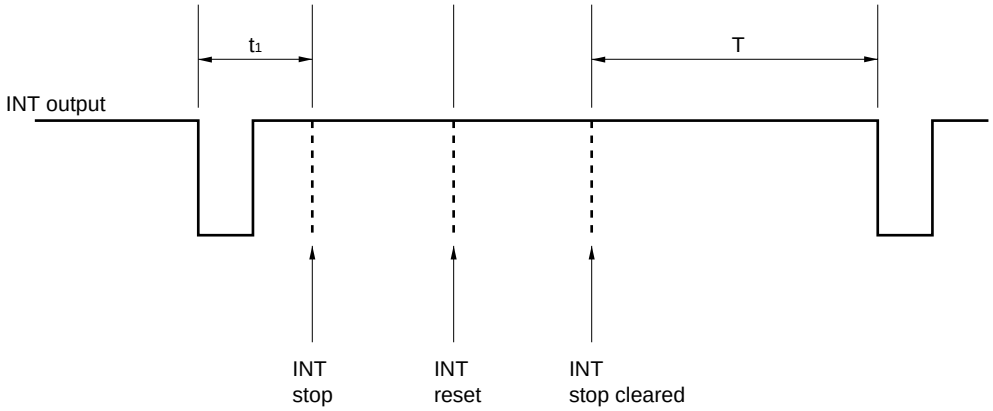
(3) Use of INT stop (1)



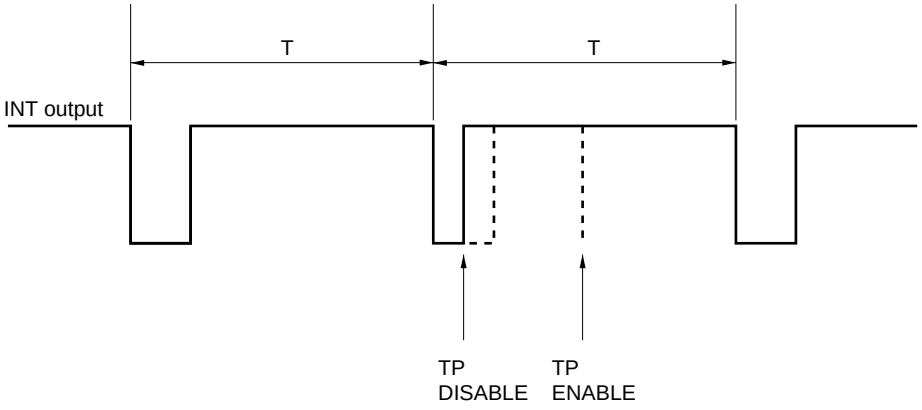
(4) Use of INT stop (2)



(5) Use of INT reset and stop



(6) Use of TP enable



2.8.2 Read control register

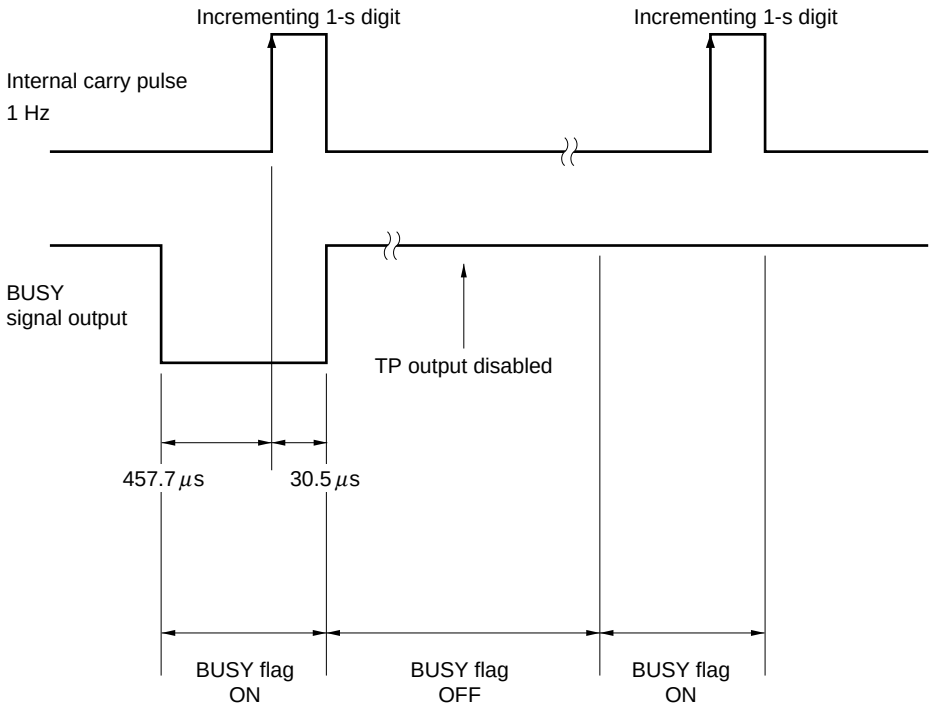
When the control register is read, the BUSY, OSC, and TP flags can be read. b3 is don't care.

(1) BUSY flag (b0)

The BUSY flag is set to ON (b0 = 1) while the internal counter operates (for the ON period, refer to **Figure 2-8**). By checking (polling) this flag before reading time, therefore, the correct time data can be read. For details, refer to **3.2.2**.

Even if data is read during the BUSY period, the internal counter is not affected.

Figure 2-8. Relation between Internal Counter, BUSY Signal Output, and BUSY Flag



(2) OSC flag (b1)

The OSC flag is reset to "0" when the 32.768-kHz reference crystal resonator stops oscillating. Once the OSC flag has been reset to "0", it remains "0" even if oscillation has been resumed. This means that, when the operation mode has returned from the backup mode to the operation mode, whether the μPD4992 has been correctly backed up can be checked by reading this flag. To set the OSC flag to "1", execute CLK reset.

When the OSC flag is reset to "0", TP output is disabled, regardless of the contents of the TP enable flag (in the control register). For details, refer to **3.4**.

The OSC flag is reset to "0" on the first power application to the μPD4992.

(3) TP flag (b2)

The TP flag is synchronized with the TP output. It is reset to "0" when TP output goes into a high-impedance state, and is set to "1" when TP output goes low. The TP flag is not forcibly reset to "0" even if the TP enable flag is set to "1" (TP = DISABLE).

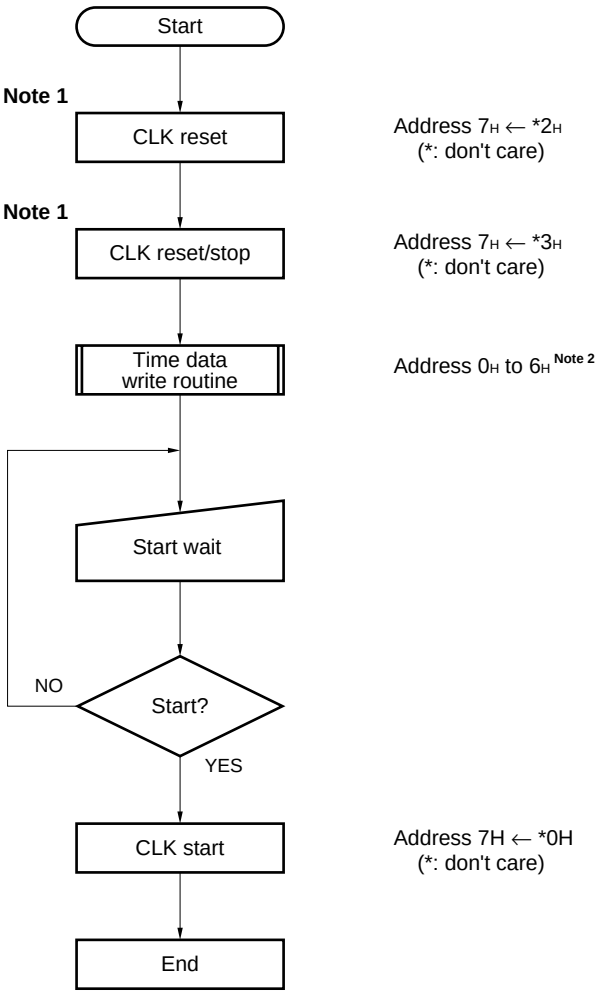
[MEMO]

CHAPTER 3 ACCESS PROCEDURE

3.1 Time Setting

Because the time counter is updated real-time, it may be set to the wrong value if it is incremented while data is being written to it because of the lapse of time. Therefore, the clock input to the time counter must be stopped before setting the time. Figure 3-1 shows a flowchart illustrating how to set the time.

Figure 3-1. Setting the Time



Notes 1. It is necessary to write the CLK reset/stop flag after writing the CLK reset flag.

2. It is not necessary to write data to the leap year counter if data is written to the low-order 2 digits of the year counter.

3. The usage shown above is on the assumption that it takes 1 second or more to set the time. Make sure that it takes 1 second or more to set the time (from CLK reset/stop to CLK start).

3.2 Reading the Time

Because the time counter is updated every second, the wrong time data may be read if the time counter is read while it is being incremented. Therefore, read the time by either of the following two methods.

<1> Use the BUSY signal as an interrupt. Or, poll the BUSY flag.
→ Read the time by outputting the BUSY signal to the TP pin or by reading the BUSY flag.
<2> Read the time twice and take the read value as valid when the two read values coincide.

3.2.1 Using BUSY signal to interrupt CPU (TP: BUSY signal output)

It is possible to read time data every second by outputting the BUSY signal to the TP pin (address $7_H \leftarrow B*_H$ where * is don't care) and by using the rising or falling edge of the BUSY signal to interrupt the CPU.

If it takes the CPU less than 457.7 μs to read the time data of the μPD4992 after the interrupt, use the falling edge of the BUSY signal. Use the rising edge of the BUSY signal if it takes 457.7 μs or more.

Figure 3-2 shows the waveform of the BUSY signal, and Figure 3-3 shows a flowchart illustrating how the BUSY signal is used to interrupt the CPU.

Figure 3-2. BUSY Signal Waveform

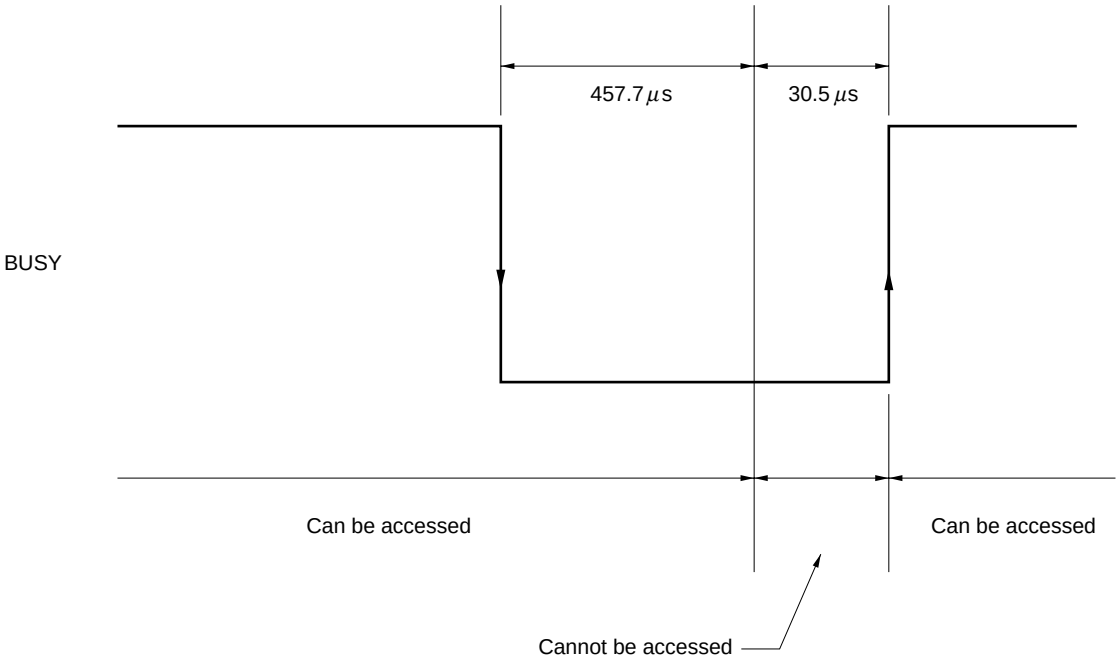
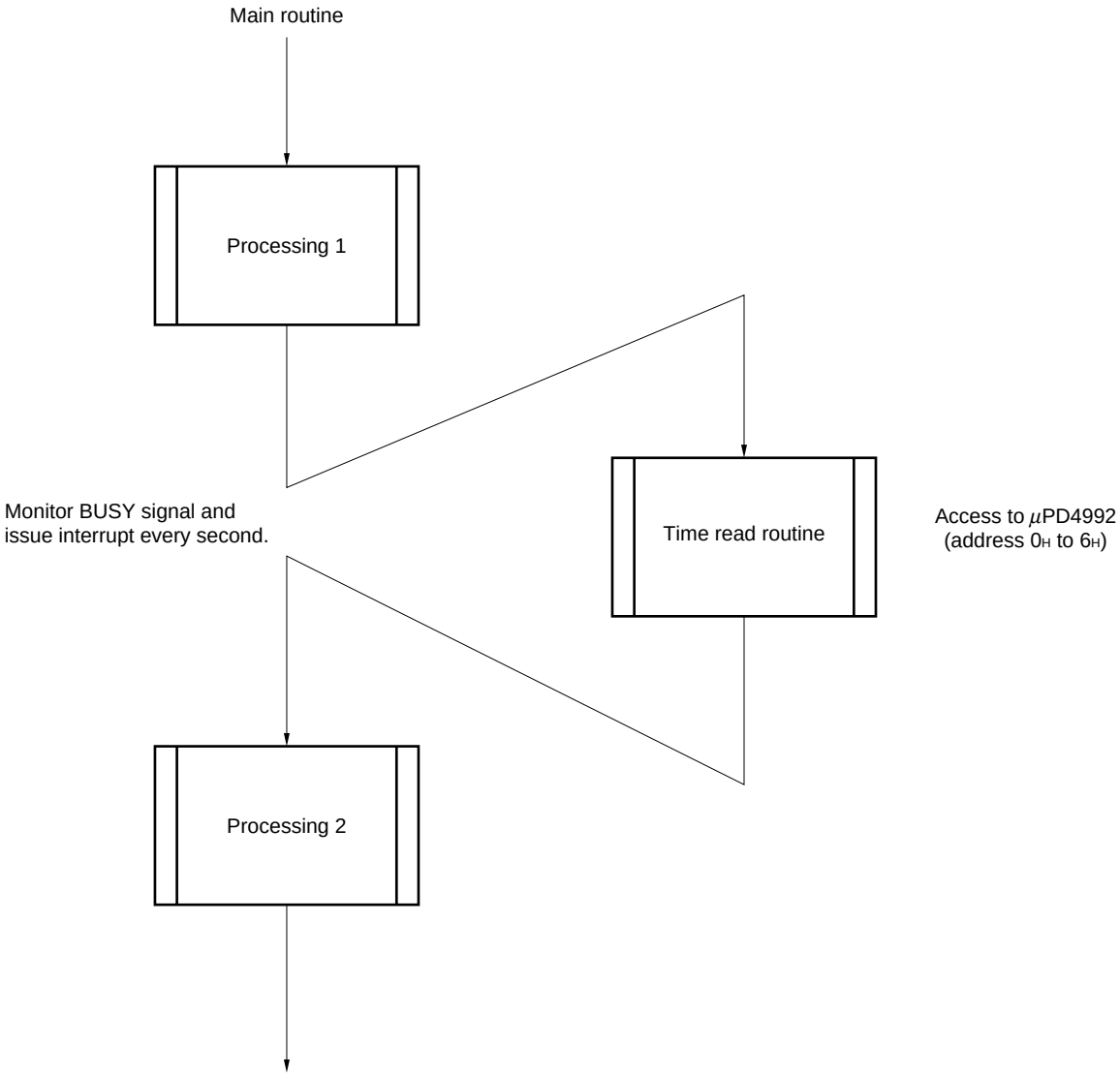


Figure 3-3. Using BUSY Signal to Interrupt CPU



3.2.2 Polling BUSY flag

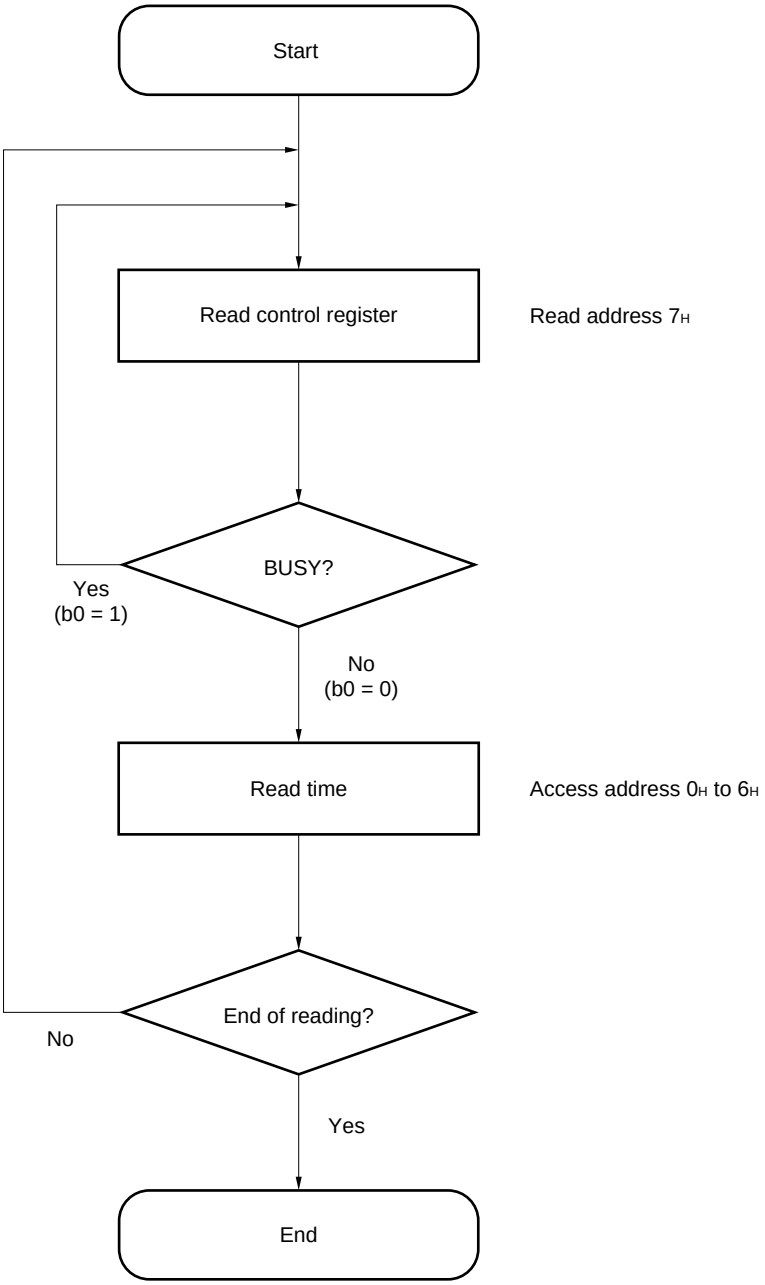
The BUSY signal can be also used by polling the BUSY flag. The BUSY flag is assigned to b0 of address 7_H (control register). Check (poll) the BUSY flag before reading the time, confirm that it is “0”, and read the time.

When the BUSY flag is “1”, the chances are that the time counter is being incremented. Wait until the BUSY flag is reset to “0”.

When polling the BUSY flag, make sure that it takes less than 457.7 μs to completely read the time from the start. If it takes 457.7 μs or longer, the time may be incremented while it is being read, and the wrong time data may be read.

Figure 3-4 shows how to poll the BUSY flag.

Figure 3-4. Polling BUSY Flag



3.2.3 Reading the time twice

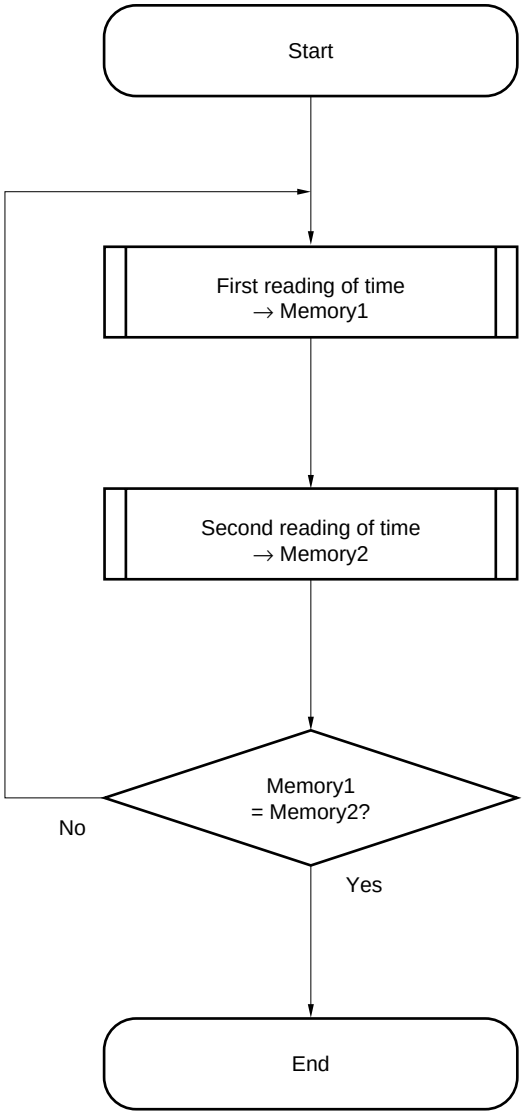
Read the time twice and compare the read values. When both the values coincide, it can be assumed that the time value is correct.

To ensure the correct operation, make sure that the rated values of the switching characteristics are satisfied when the time is read.

If the first time value is read and the second value is read more than 1 second later, the two values do not coincide and therefore, the correct time value can not be determined.

Figure 3-5 shows how to read the time value twice.

Figure 3-5. Reading Time Twice



3.2.4 Limitations on reading time

With the μPD4992, clock stop and clock start, which are two of the methods of reading the time with NEC's 4-bit parallel I/O calendar RTC μPD4991A, cannot be used (because the time may be delayed).

Therefore, use either of the following methods to read the time of the μPD4992.

<1> Use the BUSY signal for interrupt, or poll the BUSY flag.

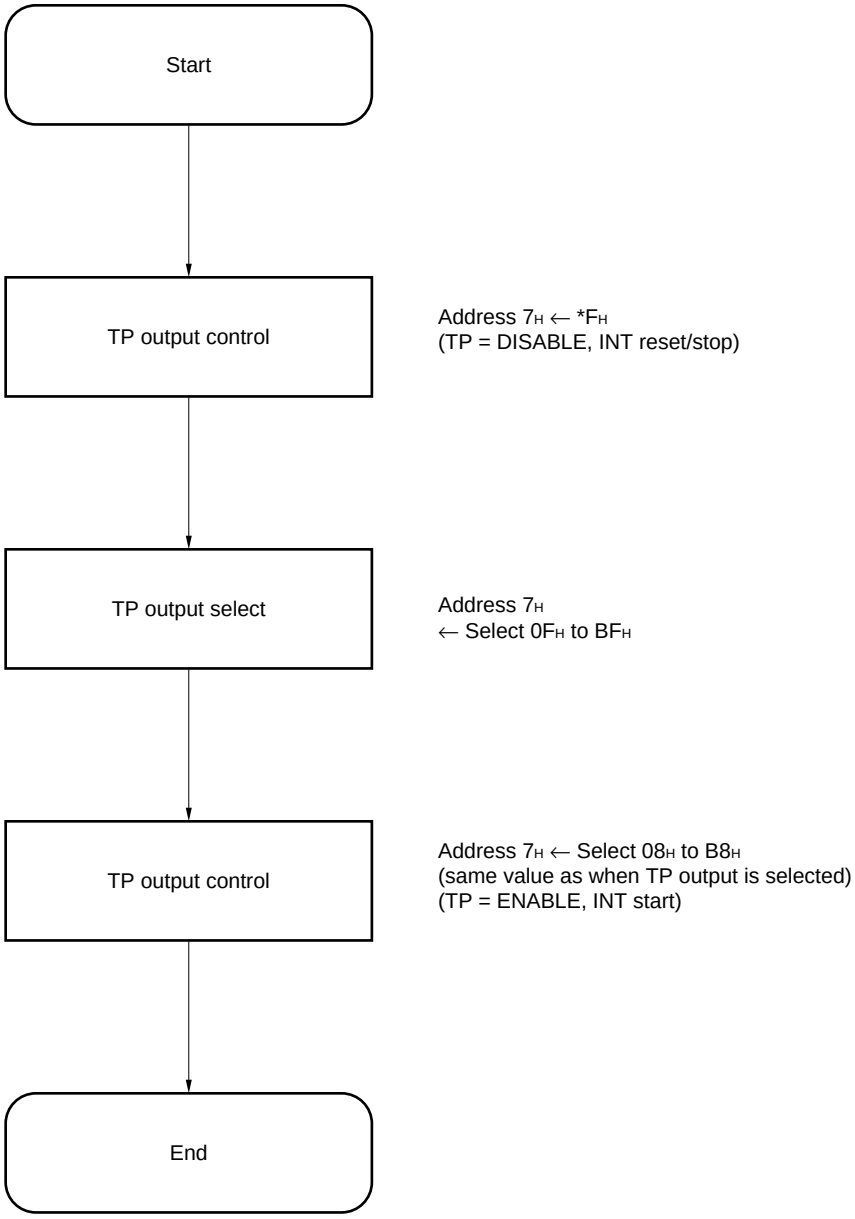
<2> Read time twice and assume that the read time value is true only if the two values coincide.

3.3 Setting TP Output

TP output is set by using the mode register (address 7_H). Because the interval timer is independent of the time counter, it can be independently stopped, resumed, or reset.

Figure 3-6 illustrates how to set TP output.

Figure 3-6. Setting TP Output



3.4 Setting When OSC Flag Is “0”

The OSC flag (b1 of address 7_H) is reset to “0” on power application or on stopping oscillation. In this case, the internal status is undefined, but TP output is disabled, regardless of the contents of the internal registers (refer to **Figure 3-7**).

To clear this disabled status, execute CLK reset and set TP output, as illustrated by the flowchart in Figure 3-8.

Figure 3-7. TP Pin Control Equivalent Circuit

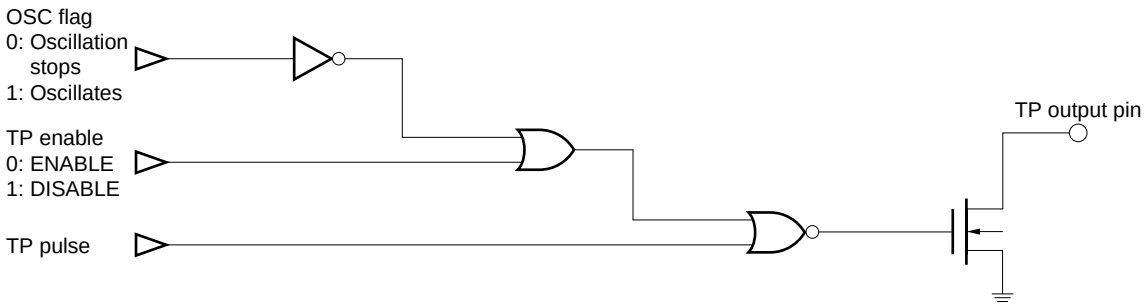
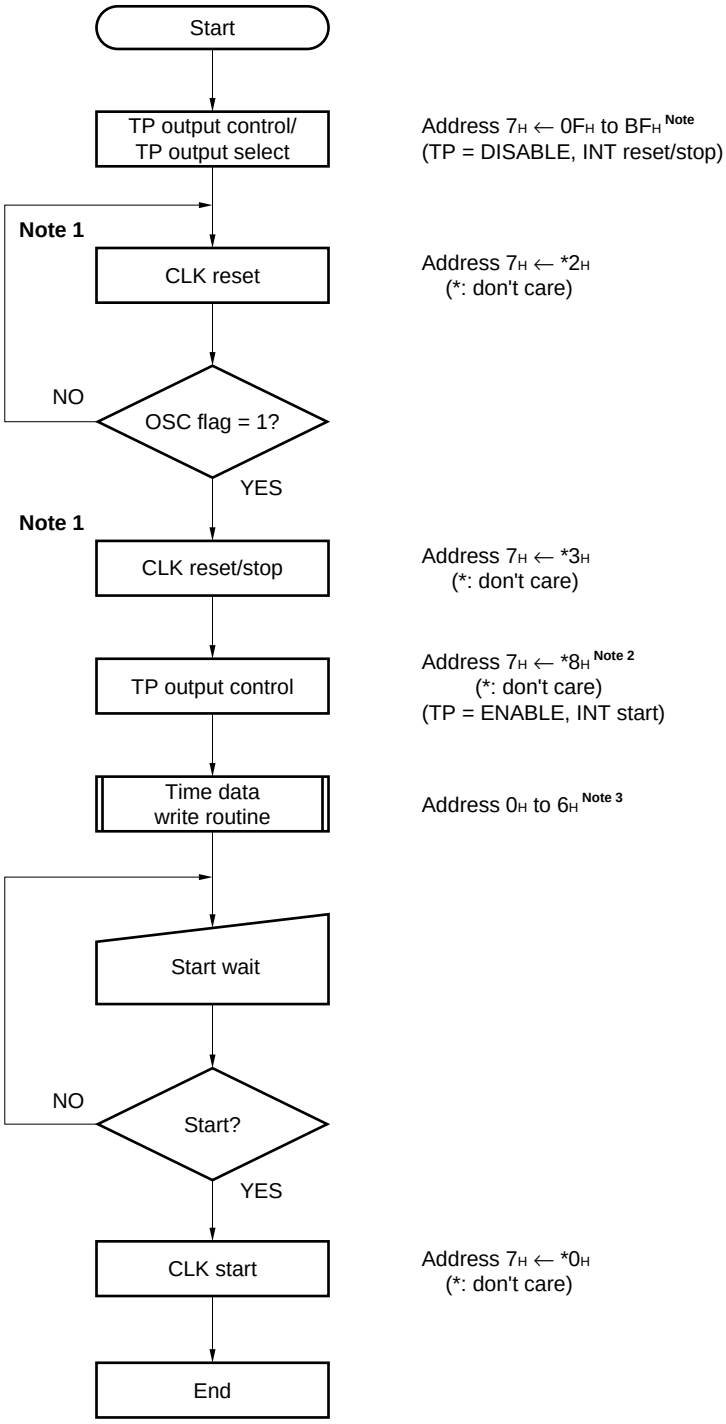


Figure 3-8. Setting when OSC Is “0”



Notes 1. It is necessary to write the CLK reset/stop flag after writing the CLK reset flag.

2. This is not necessary when TP output is not used.

3. It is not necessary to write data to the leap year counter if data is written to the low-order 2 digits of the year counter.

4. The usage shown above is on the assumption that it takes 1 second or more to set the time. Make sure that it takes 1 second or more to set the time (from CLK reset/stop to CLK start).

[MEMO]

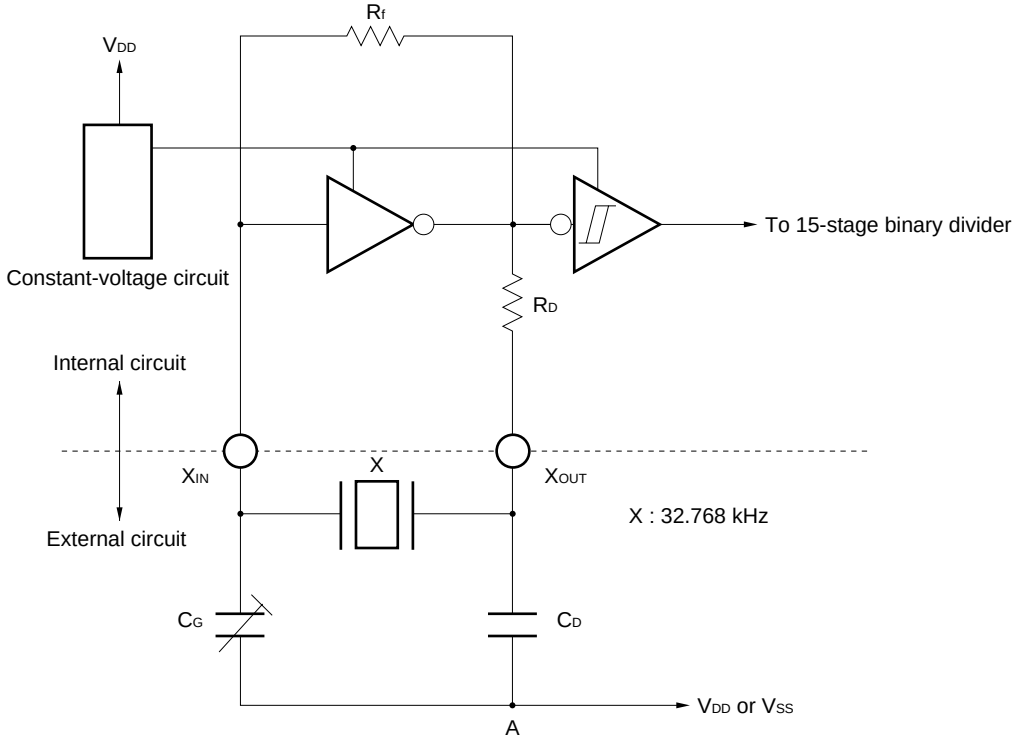
4.1 Crystal Oscillation Circuit

The μPD4992 uses an oscillation circuit that consists of a single-stage CMOS inverter, feedback resistor R_f, and oscillation stabilization resistor R_D.

Figure 4-1 shows the equivalent circuit of the oscillation circuit. The oscillation frequency of this circuit is determined by external load capacitances C_G and C_D, and crystal resonator.

Because the stray capacitances of X_{IN} and X_{OUT} must be taken into consideration in addition to C_G and C_D, either C_G or C_D must be fine-tuned.

Figure 4-1. Crystal Oscillation Circuit of μPD4992



Connect point A in Figure 4-1 to V_{DD} or V_{SS} of the μPD4992 (there is not much difference in characteristics regardless of whether this point is connected to V_{DD} or V_{SS}). Keep the wiring of the crystal resonator as short as possible. If the wiring length is too long, oscillation may not be stabilized and the accuracy of the RTC may be affected by external noise.

4.2 Oscillation Characteristics and Accuracy

The accuracy of the RTC function of the μPD4992 is determined by the accuracy of the oscillation frequency. The oscillation frequency is affected by the load capacitance and temperature.

4.2.1 Dependency on load capacitance

Figure 4-2 shows a circuit to test the dependency of the oscillation frequency on load capacitance under conditions of V_{DD} = +5 V, T_A = +25 °C. The test results are shown in the following figures.

Figure 4-3: Changes in frequency when C_G and C_D are changed at the same time
Figure 4-4: Changes in frequency when C_G is changed (C_D = 18 pF)
Figure 4-5: Changes in frequency when C_D is changed (C_G = 18 pF)

If C_G and C_D are too high (50 pF or more), the oscillation characteristics are affected. The characteristics are also affected by the crystal resonator actually used and the stray capacitance of the printed circuit board.

Figure 4-2. Test Circuit

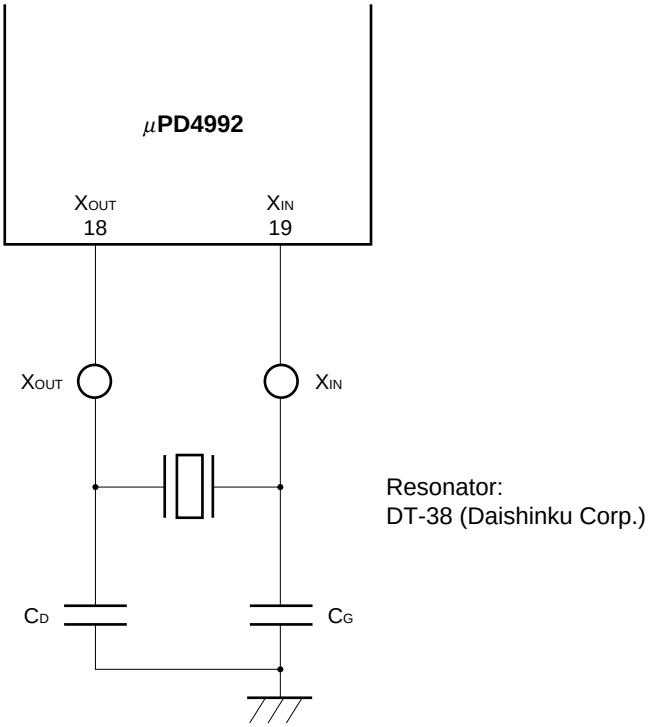


Figure 4-3. Changes in Frequency When C_G and C_D Are Changed at Same Time

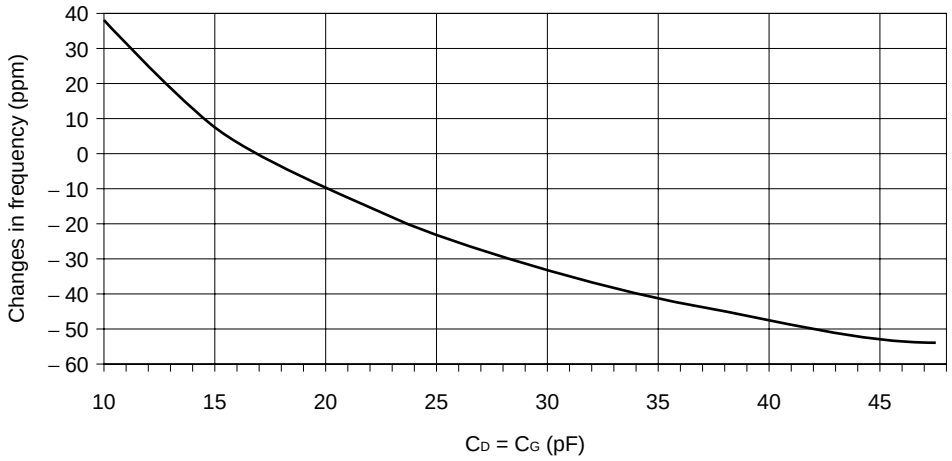


Figure 4-4. Changes in Frequency When C_G Is Changed (C_D = 18 pF)

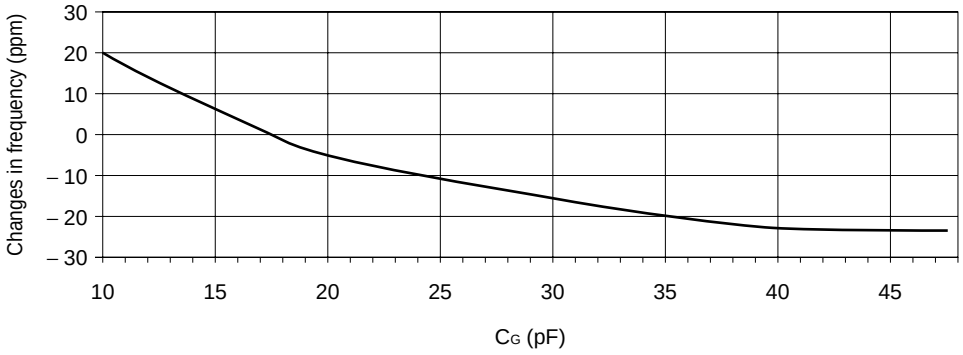
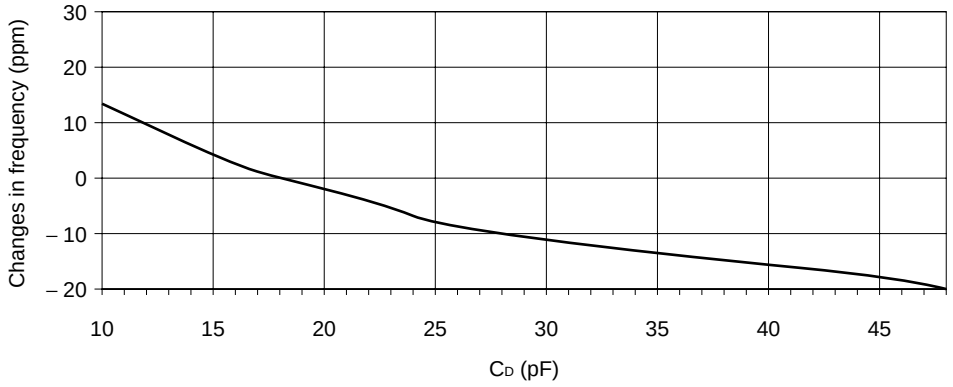


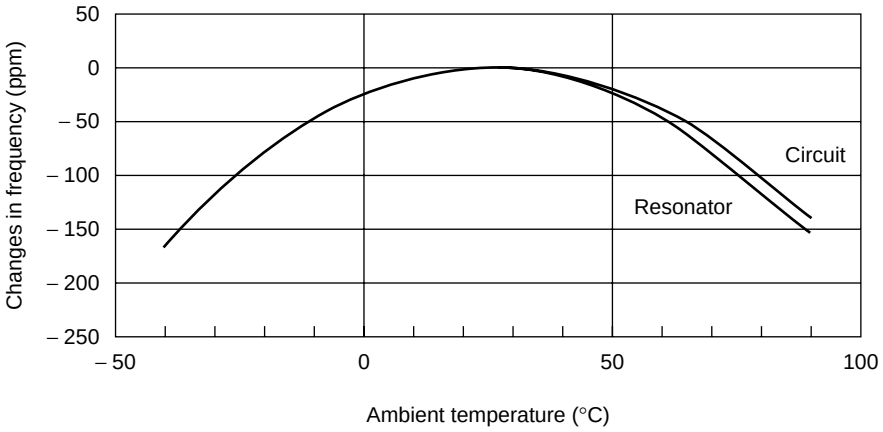
Figure 4-5. Changes in Frequency When C_D Is Changed (C_G = 18 pF)



4.2.2 Dependency on temperature

The oscillation frequency changes with ambient temperature. Figure 4-6 shows the ambient temperature vs. oscillation frequency characteristics. As can be seen, the temperature characteristic curve is of the negative second order with its summit at around 25 °C. This is the specific temperature characteristic of a tuning fork crystal resonator.

Figure 4-6. Temperature Characteristics of Crystal Resonator and μPD4992 (C_D = C_G = 18 pF)



4.3 Adjusting Oscillation Frequency

The accuracy of the RTC depends on the stability of the oscillation frequency. To improve the accuracy, therefore, the oscillation frequency must be adjusted.

Use C_G or C_D as a trimmer capacitor. Use the TP output pin for adjustment. Adjust the trimmer capacitor so that the measured value falls within the rated frequency range, while measuring the INT output by using a frequency counter.

Be sure to use the TP output pin for measurement. Using a test probe on the X_{IN} or X_{OUT} pin may stop oscillation or makes it impossible to measure an accurate value because the oscillation frequency is affected by the capacitance of the probe.

4.4 Backup Circuit

The μPD4992 can be backed up by low-capacity batteries because it is a CMOS IC that operates with low current consumption. Figure 4-7 shows an example of backing up the μPD4992 with a Ni-Cd battery, while Figure 4-8 shows an example of using a super capacitor (high-capacity, electric double layer capacitor).

Figure 4-7. Backup Circuit Example with Ni-Cd Battery

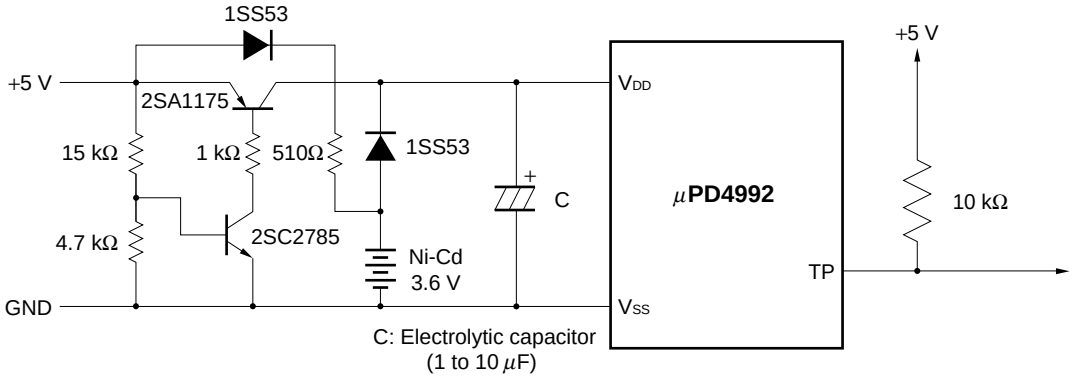
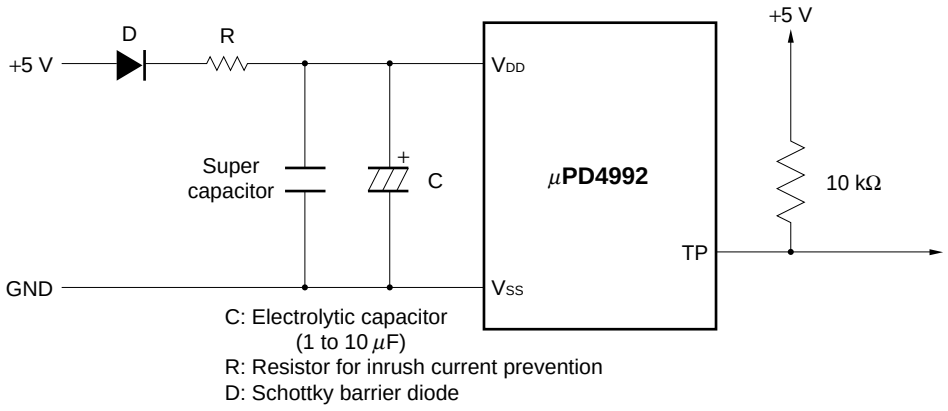


Figure 4-8. Backup Circuit Example with Super Capacitor



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

4.5 Power-Fail Circuit

While the μPD4992 is backed up, it is necessary to prohibit external access to the IC by fixing the CS_2 pin to the low level. The power-fail circuit, therefore, must fix CS_2 to the low level if the power supply to the system drops below the operating voltage of the CPU (e.g., 4.5 V or less), and keep CS_2 low until the CPU operates again (refer to **Figure 4-9**).

Figure 4-10 shows an example of a circuit that detects a drop in the system power supply and prohibits access to the internal circuits of the μPD4992. This circuit consists of a Zener diode and transistors.

Figure 4-9. Backup Status and CS_2 Pin Voltage

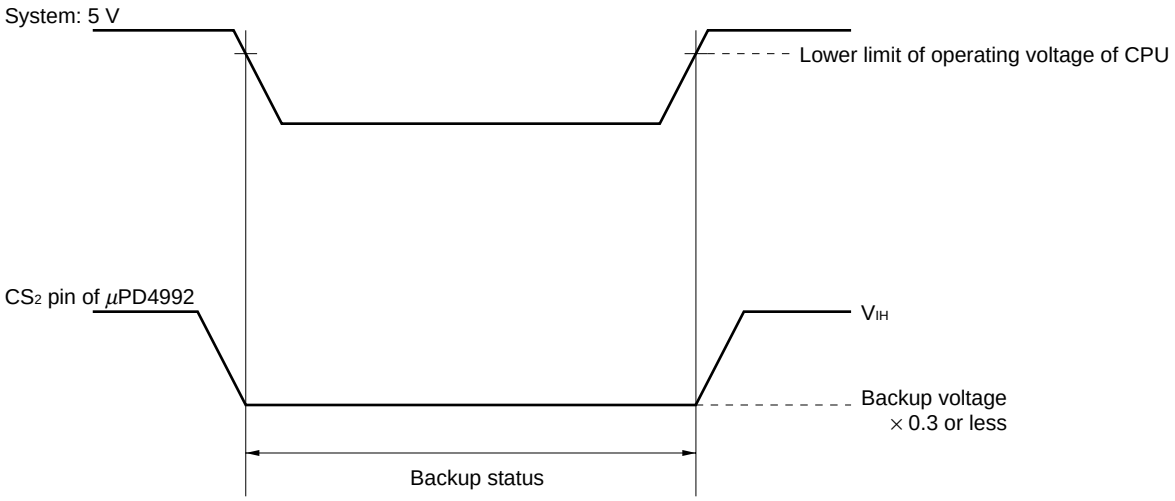
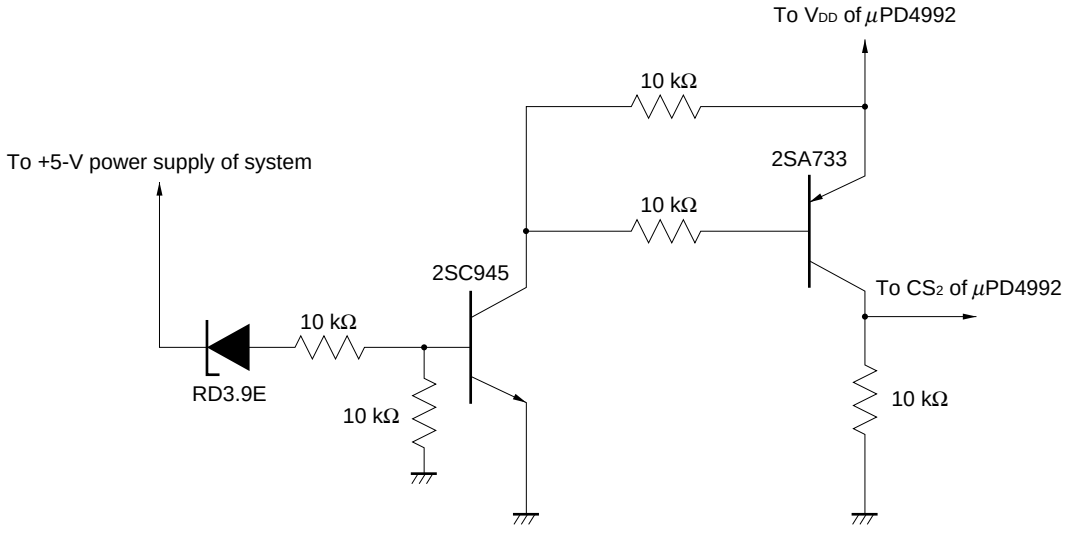


Figure 4-10. Example of Power-Fail Circuit



The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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