USER'S MANUAL

NEC

μPD42280

2-MBIT FIELD BUFFER

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

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Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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INTRODUCTION

Readers This manual is intended for user engineers who understand the functions of the μPD42280 and wish to design and develop its application systems.

Purpose This manual is designed to deepen your understanding of the following functions listed under Organization below.

Organization This manual is organized as follows.

- Outline
- Operation
- Restrictions
- Application examples
- Cautions

How to Read This Manual

It is assumed that readers of this manual have general knowledge of electric engineering, logic circuits, microcontrollers, and video signal processing.
For the electrical specifications of the μPD42280, refer to the separate Data Sheet.

Legend

Data significance	:	Left: higher digit, right: lower digit
Active low	:	$\overline{\times\times\times}$ (top bar over pin or signal name)
Note	:	Footnote explaining items marked with “Note” in the text
Caution	:	Description of point that requires particular attention
Remark	:	Supplementary information
Numerical representation:		Binary...×××× or ××××B
		Decimal...××××
		Hexadecimal...××××H

Related Document

Data Sheet: S11274E

Caution The contents of the above related document is subject to change without notice. Be sure to use the latest version for designing

[MEMO]

Contents

CONTENTS OF FIGURES

CONTENTS OF TABLES

[MEMO]

CHAPTER 1 GENERAL

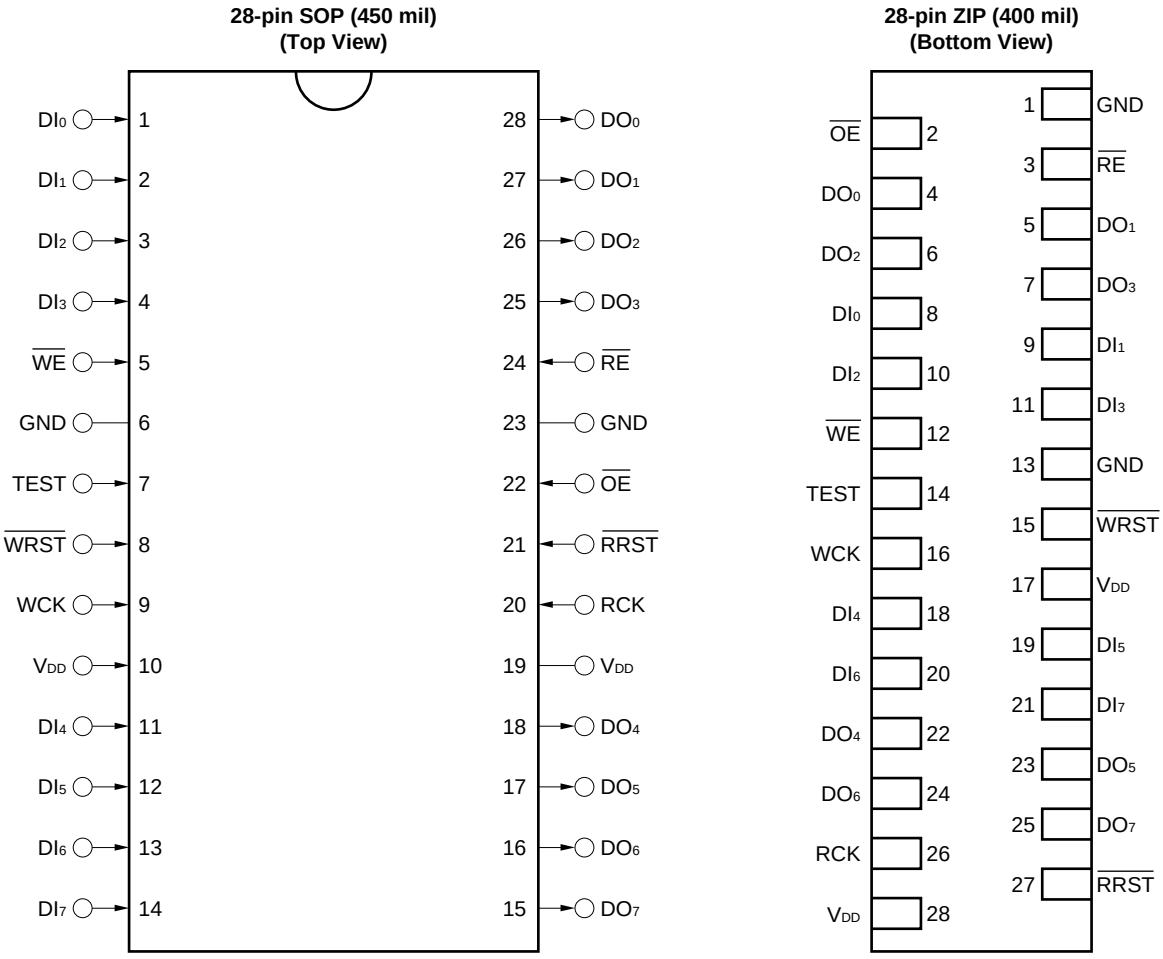
The μPD42280 is a high-speed field buffer with a 256 K × 8-bit (262,224 × 8 bits) FIFO organization.
It supports asynchronous operation and simultaneous read and write.
Use of the μPD42280 allows easy field delay, time-based conversion, and other types of processing.
This document provides mainly an outline of the operation of the μPD42280, using several concrete examples.

1.1 Ordering Information

Part Number	Package	Read Cycle Time	Access Time	Write Cycle Time
μPD42880GU-30	28-pin plastic SOP (450 mil)	30 ns	25 ns	30 ns
μPD42280GU-60	28-pin plastic SOP (450 mil)	60 ns	40 ns	60 ns
μPD42280V-30	28-pin plastic ZIP (400 mil)	30 ns	25 ns	30 ns
μPD42280V-60	28-pin plastic ZIP (400 mil)	60 ns	40 ns	60 ns

1.2 Pin Configuration

Figure 1-1 Pin Configuration of μPD42280



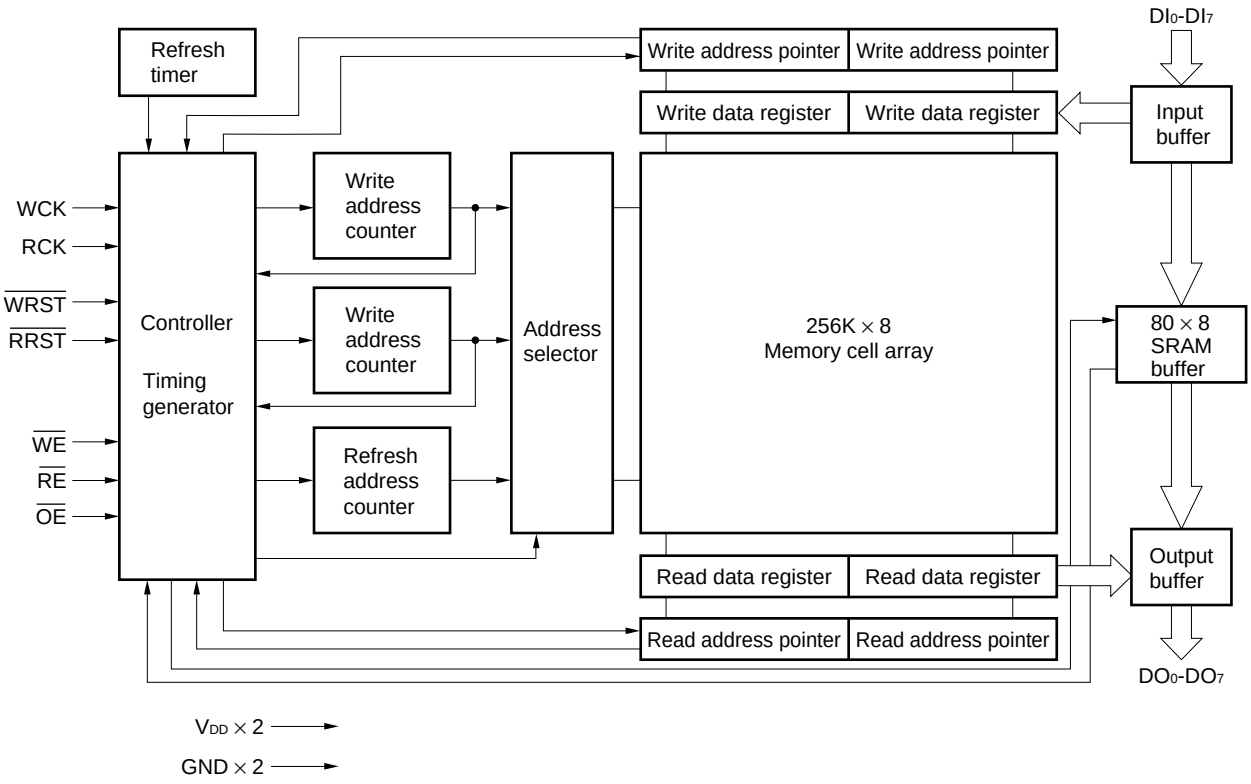
DI0-DI7 : Data input
DO0-DO7: Data output
WCK : Write clock input
RCK : Read clock input
$\overline{WE}$: Write enable input
$\overline{RE}$: Read enable input
$\overline{OE}$: Output enable input
$\overline{WRST}$: Write reset input
$\overline{RRST}$: Read reset input
TEST : Test pin
VDD : +5 V power supply
GND : Ground

Table 1-1 Pin Functions

Pin Name	I/O	Function
DI_0-DI_7	I	Write data input. Data is fetched at the back rising edge of the WCK input cycle, and the setup and hold times (t_{DS}, t_{DH}) are specified against the edge.
DO_0-DO_7	0 (3-state)	Read data output. The access time is specified from the front rising edge of the RCK cycle, and determined with t_{AC}. These are 3-state output pins.
$\overline{WRST}$	I	Reset input for initializing write addresses. The reset signal is asserted at the front rising edge of the WCK input cycle, and the setup and hold times (t_{RS}, t_{RH}) are specified.
$\overline{RRST}$	I	Reset input for initializing read addresses. The reset signal is asserted at the front rising edge of the RCK input cycle, and the setup and hold times (t_{RS}, t_{RH}) are specified.
$\overline{WE}$	I	Write control input. When high level, internal write is disabled and the write address pointer stops in its current location. The $\overline{WE}$ signal is asserted at the front rising edge of the WCK input cycle.
$\overline{RE}$	I	Read control input. When high level, internal write is performed, but the read address pointer stops in its current location. The $\overline{RE}$ signal is asserted at the front rising edge of the RCK input cycle.
$\overline{OE}$	I	Read data control input. When high level, DO_0-DO_7 become high impedance. Regardless of the $\overline{OE}$ signal input level, the read address pointer is incremented in synchronism with the RCK. The $\overline{OE}$ signal is asserted at the front rising edge of the RCK input cycle.
WCK	I	Write clock input. Write is performed in synchronism with the write clock when $\overline{WE}$ is low level, and the write address pointer is incremented simultaneously.
RCK	I	Read clock input. Read is performed in synchronism with the read clock. When $\overline{RE}$ is low level, the read address pointer is also incremented simultaneously.
TEST	I	Test pin. Fix to low level.
V_{DD}	–	Power supply pin
GND	–	Ground pin

1.3 Block Diagram

Figure 1-2 Block Diagram of μPD42280



The internal memory of the μPD42280 consists of an 80-byte SRAM buffer and a 256-Kbyte DRAM. The SRAM buffer is used to hold 80 words of data immediately after reset. The data past beyond the 80th word is held in the DRAM cells.

The SRAM buffer supports high-speed read/write. Input data is directly written to the SRAM buffer via the input buffer. During read, data is directly read from SRAM and output via the output buffer.

High-speed access of DRAM cells being difficult, direct data read/write cannot be done. Therefore, the μPD42280 is designed to perform read/write via write data registers and read data registers.

In this way, FIFO operation is realized.

CHAPTER 2 OPERATION

2.1 Basic Operation

The general operation of data read/write from/to DRAM cells via write data registers and read data registers is explained below.

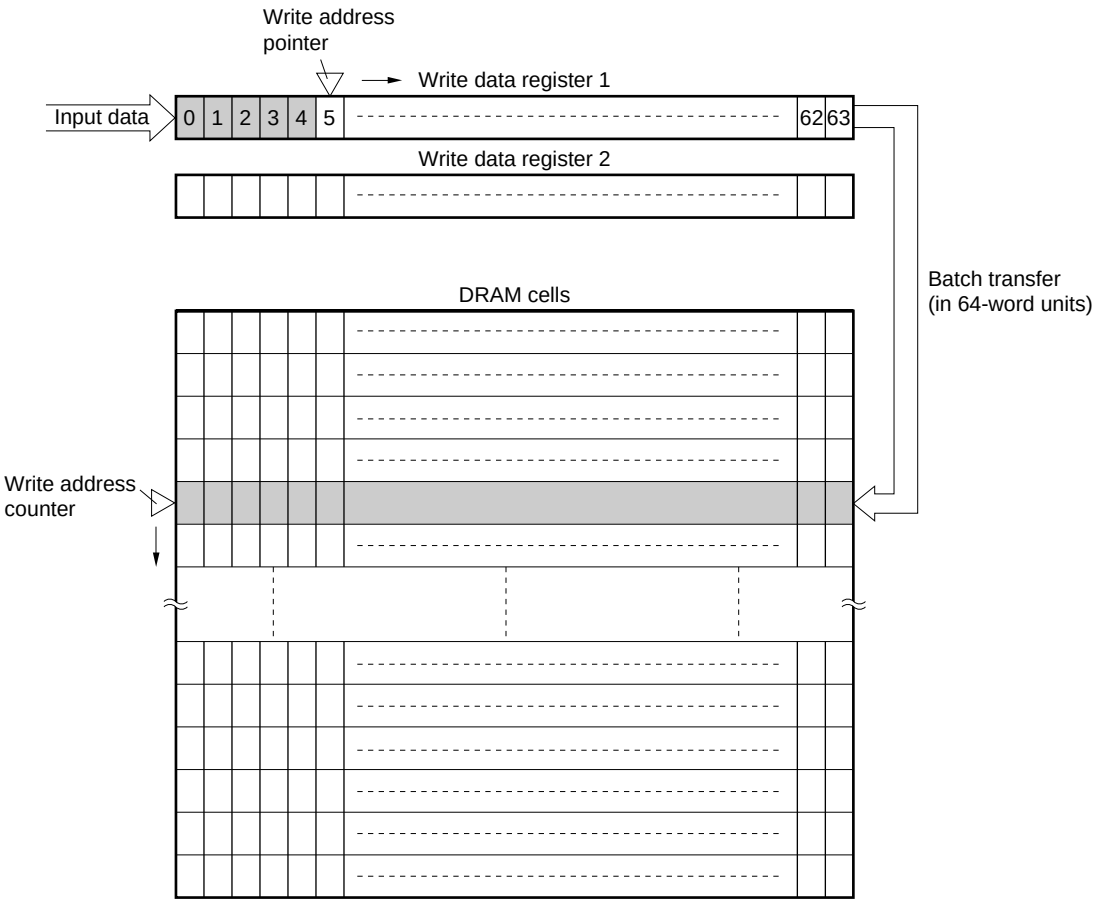
2.1.1 Basic internal operation during write

Input data is first stored in a write data register via the input buffer.

Each write data register can hold 64 words. The μPD42280 has two write data registers, which work on an alternate basis.

When one of the write data registers becomes filled with 64 words of input data, these 64 words of data are loaded at one time to DRAM memory cells.

Figure 2-1 Write Data Register Operation



Each write data register can hold 64 words, assigned addresses from 0 to 63. The address in the write data register to which serially input data is to be stored is indicated by the write address pointer.

In the example shown in Figure 2-1, the write address pointer is at address 5, indicating that the data written next will be stored to address 5 of the write data register. In this example, addresses 0 to 4 are already filled with data.

The write address pointer is incremented by 1 at each data input, i. e. at each WCK input. When a write data register becomes full with data in this way, its 64 words of data are loaded at one time to DRAM cells.

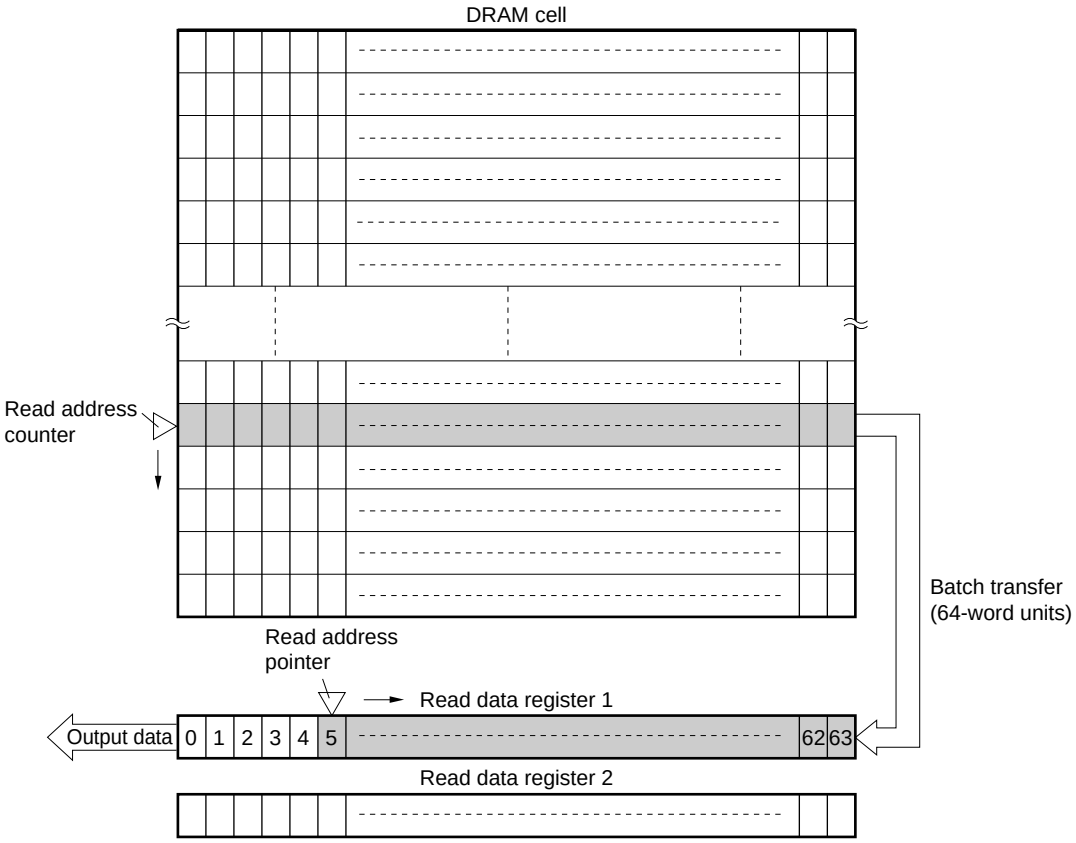
At this time, the write address counter indicates a low address of DRAM as the send destination. The write address counter is incremented by 1 at each data transfer to the DRAM cells of the write data register.

When the write data register 1 becomes full and batch transfer of its data starts, the data input next is stored to write data register 2. In this way, the two write data registers work on an alternate basis, allowing data to be input continuously.

2.1.2 Basic internal operation during read

During read, data is read in the reverse procedure of the write procedure.

Figure 2-2 Read Data Register Operation



The 64 words of data corresponding to one low address line in DRAM are transferred at one time to a read data register. At this time, the low address in DRAM from which the data is transferred is indicated by the read address counter. The read address counter is incremented by 1 at each data transfer from DRAM cells to the read data register.

Data is sequentially output from the read data register to the address indicated by the read address pointer. The read address pointer is incremented by 1 at each data input, i.e. at each RCK input. When all 64 words of data are output and the read data register is empty, data is again batch transferred from DRAM cells to the read data register.

When read data register 1 becomes empty and batch transfer data from DRAM cells is input, the read data is output from read data register 2 (at this time, read data is already transferred from DRAM cells). In this way, the two read data registers work on an alternate basis, and data can be output continuously.

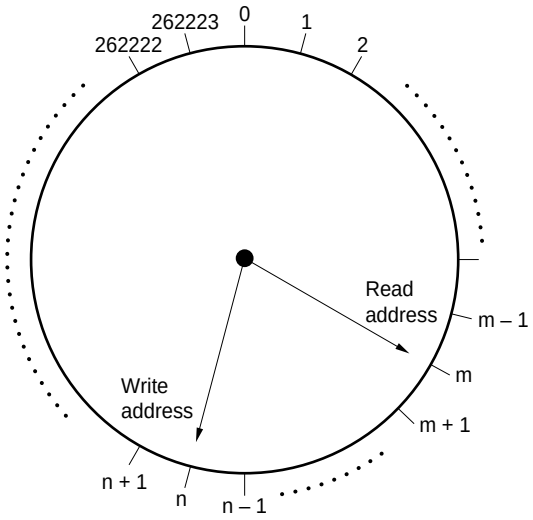
2.1.3 Concept of addresses in μPD42280

The μPD42280 internal location to which input data is stored is determined with the address pointers and address counters in the IC. However, considering the FIFO organization of the μPD42280, consecutive data write and read to/from the 262,224 memory cells corresponding to addresses 0 to 262,223 of the μPD42280 is a very natural concept and presents no problem.

The addresses in the μPD42280 are based on this concept. In other words, serially input data is written sequentially to address 0, 1, 2 and so on; During read, this data is output sequentially from addresses 0, 1, 2 and so on. Based on this, the notation address n, cycle n is employed.

In the μPD42280, when write or read addresses reach the last address 262,223, the address number is reset to 0. In other words, the 262, 224 addresses of the μPD42280 can be thought of as linked into a circular pattern. Write addresses and read addresses advance inside this circle like the hands of a watch.

Figure 2-3 Conceptual Drawing of μPD42280



Write and read addresses are incremented according to WCK and RCK input, respectively. In other words, the hands shown in Figure 2-3 advance one number at a time clockwise.

$\overline{WE}$ and $\overline{RE}$ function to stop the progression of addresses, or, in other words, the hands of the watch.

$\overline{OE}$ becomes high impedance without affecting the read address pointer.

Moreover, $\overline{WRST}$ and $\overline{RRST}$ function to return their respective watch hand to 0. Based on this concept of addresses, addresses 0 to 79 correspond to the SRAM buffer, and addresses from 80 to 262,223 correspond to DRAM cells.

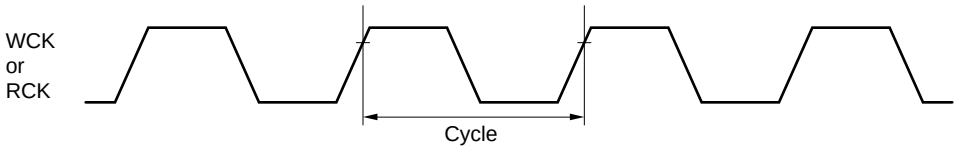
2.2 Write/Read Operation

2.2.1 Cycle

In the μPD42280, data read and write are basically controlled with the write clock (WCK) and read clock (RCK). The WCK and RCK cycles are referred to as 1 cycle, and this concept of cycles is employed in the specification of each operation.

Cycles designate the time interval between one rising edge to the following rising edge. Therefore, the interval of one cycle contains 2 rising edges. The rising edge following a given cycle is thus the first rising edge of the next cycle.

Figure 2-4 Cycle



Cycle n indicates the cycle during which the data of address n will be written, in the case of a write cycle, or the cycle during which the data of address n will be read, in the case of a read cycle.

In the μPD42280, input data is fetched and the $\overline{WE}$ and $\overline{WRST}$ signals are asserted in synchronism with the rising edge of WCK. Therefore, these signals must be input so as to satisfy the setup time and hold time for the rising edge of WCK.

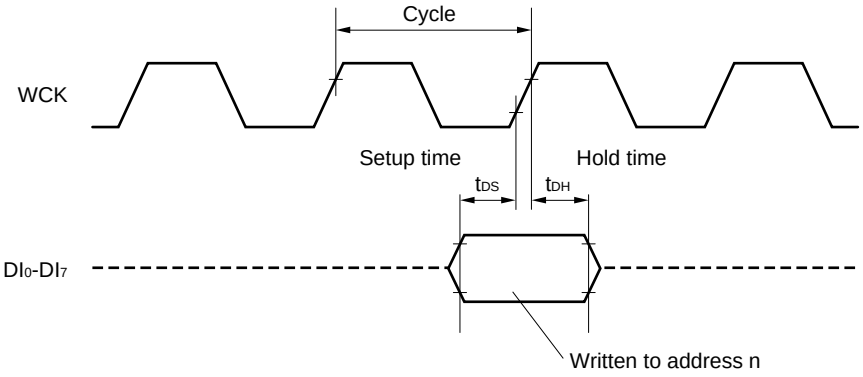
Similarly, the $\overline{RE}$, $\overline{OE}$, and $\overline{RRST}$ signals are asserted in synchronism with the rising edge of RCK. Therefore, these signals must be input so as to satisfy the setup time and hold time for the rising edge of RCK.

2.2.2 Write operation

(1) Basic operation

When the $\overline{WE}$ signal is low level, write is performed in synchronism with WCK input in 8-bit units per cycle. The write address is also incremented in synchronism with WCK input. Taking a look at a given write cycle, the input data is fetched following the next rising edge. Therefore, write data must be input so as to satisfy the setup time and hold time for the back rising edge of the WCK input cycle.

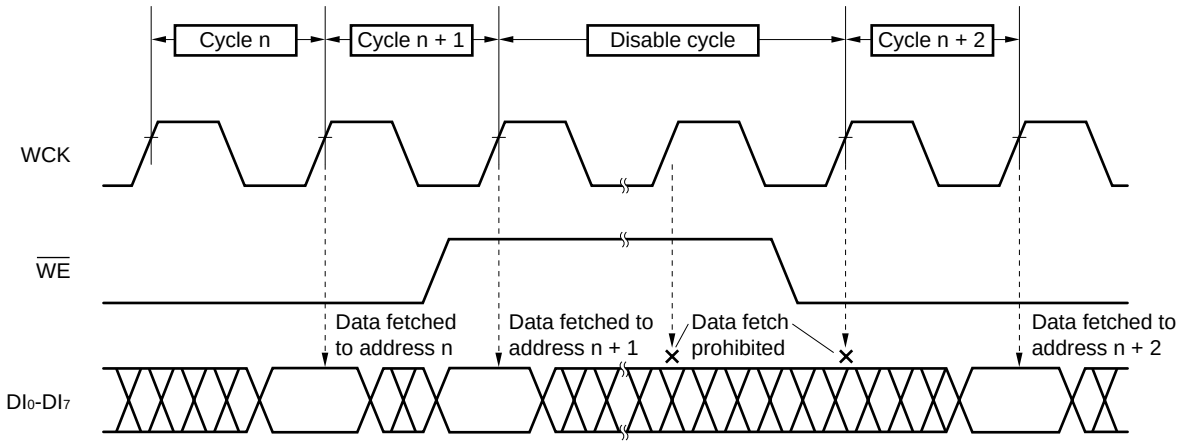
Figure 2-5 Basic Write Operation



(2) Write Disable Using $\overline{WE}$

When $\overline{WE}$ input become high level, write is disabled, and the pointer stops at the write address when the high level was input. When a low level is subsequently input, operation starts from the address where the pointer stopped. Write disable can be implemented any time, but the $\overline{WE}$ signal must be input so as to satisfy the setup time and hold time for the rising edge of WCK.

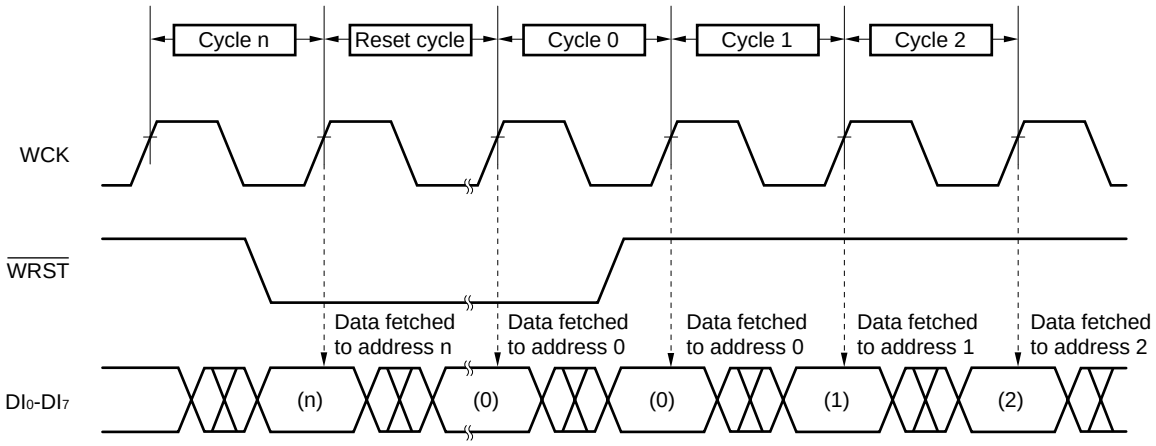
Figure 2-6 Write Disable Using $\overline{WE}$



(3) Write reset

The write address can be reset to address 0 by inputting a low level to $\overline{\text{WRST}}$. The $\overline{\text{WRST}}$ signal can be input any time, but it must be input so as to satisfy the setup time and hold time for the rising edge of WCK. Moreover, initialization of the write address using write reset can be performed independently of read reset.

Figure 2-7 Write Reset



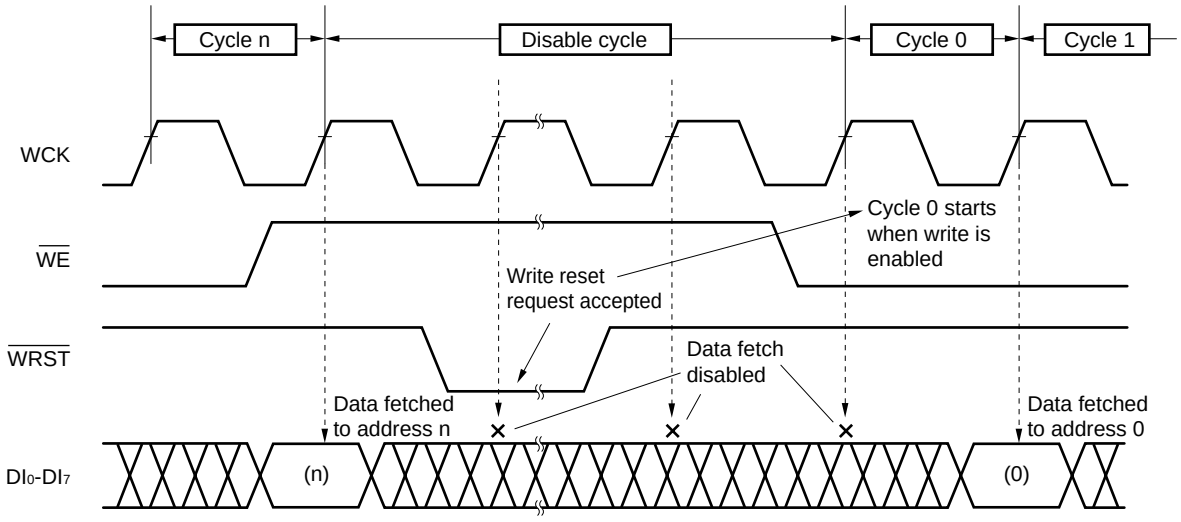
If write reset is extended over several cycles, new data is written one after the next to address 0 according to WCK input. Although the reset cycle and cycle 0 are represented as separate in Figure 2-7, they can actually be thought of as the same thing for practical purposes.

(4) $\overline{WE}$ and $\overline{WRST}$ contention

If a low-level signal is input to $\overline{WRST}$ while $\overline{WE}$ is write-disabled after input of a high-level signal, a reset request is accepted, but reset is not executed while write is disabled.

When $\overline{WE}$ becomes low level and write becomes enabled, write reset is executed and the pointer is reset to address 0.

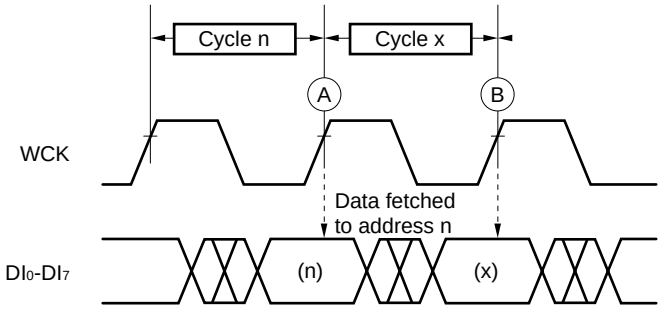
Figure 2-8 $\overline{WE}$ and $\overline{WRST}$ Contention



(5) Write cycle concept

Taking a look at a given write cycle, the $\overline{WE}$ and $\overline{WRST}$ signals are latched at the front rising edge.
In other words, in Figure 2-9, the type of cycle x that follows write cycle n depends on the status of the $\overline{WE}$ and $\overline{WRST}$ signals at point A, which is the rising edge preceding cycle x. For example, if the $\overline{WE}$ signal is a high level at point A, cycle x becomes a disable cycle. Or, if $\overline{WRST}$ is a low level, cycle x becomes a reset cycle, and the data that is input at point B, which is the following rising edge, is written to address 0.

Figure 2-9 Write Cycle



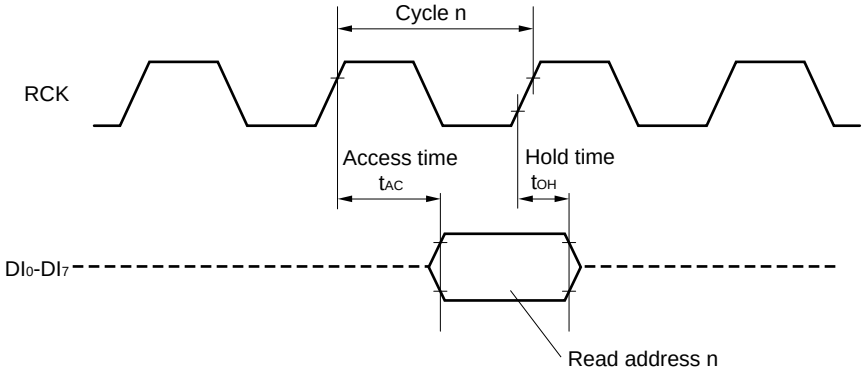
If at point A the $\overline{WE}$ and $\overline{WRST}$ signals are high and low level, respectively, cycle x becomes a disable cycle. At this time, input of a low-level $\overline{WRST}$ signal causes a write reset request to be accepted, $\overline{WE}$ becomes low level and write is executed from the point where it is enabled.

2.2.3 Read Operation

(1) Basic operation

When both $\overline{RE}$ input and $\overline{OE}$ input are low level, read is performed at the rate of 8 bits per cycle in synchronism with RCK input. The read address is also incremented in synchronism with RCK input. Taking a look at a given read cycle, read data is output following the lapse of the access time (t_{AC}) from the front rising edge of the RCK input.

Figure 2-10 Basic Read Operation

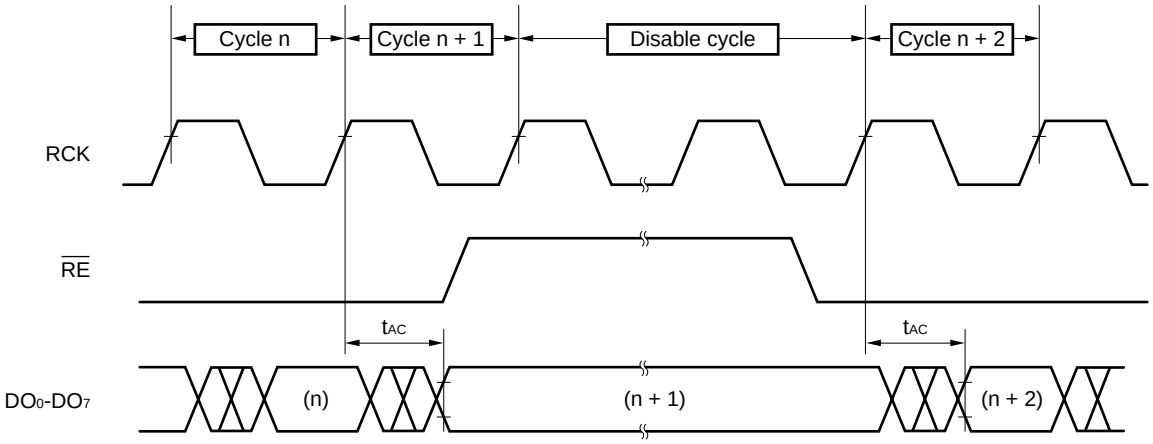


(2) Read address disable using $\overline{RE}$

When $\overline{RE}$ input becomes high level, the read address pointer stops at the address when the high level was input. While the pointer is stopped at a read address, the data of that address continues to be output. At this time, on the write side, even if the data of the stopped address is overwritten, the original data continues to be output as the read data.

When a low level is input, read resumes from the address where it stopped.

Figure 2-11 Read Address Stop Using $\overline{RE}$



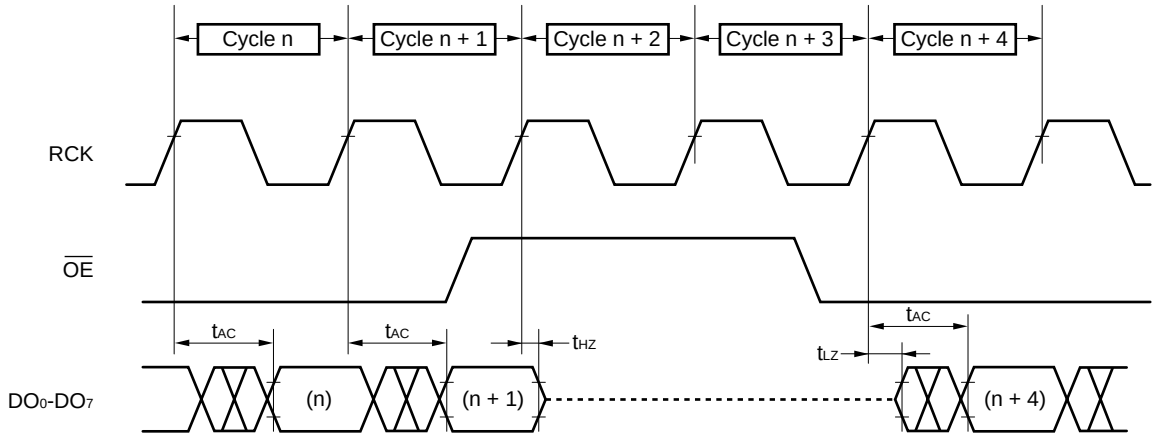
Read address stop can be executed any time, but the $\overline{RE}$ signal must be input so as to satisfy the setup time and hold time for the rising edge of RCK.

(3) Data output disable using $\overline{OE}$

When $\overline{OE}$ input becomes high level, output becomes high impedance. At this time, the read address is incremented in synchronism with RCK input, regardless of the $\overline{OE}$ signal input level.

Read disable can be executed any time, but the $\overline{OE}$ signal must be input so as to satisfy the setup time and hold time for the rising edge of RCK.

Figure 2-12 Data Output Disable Using $\overline{OE}$

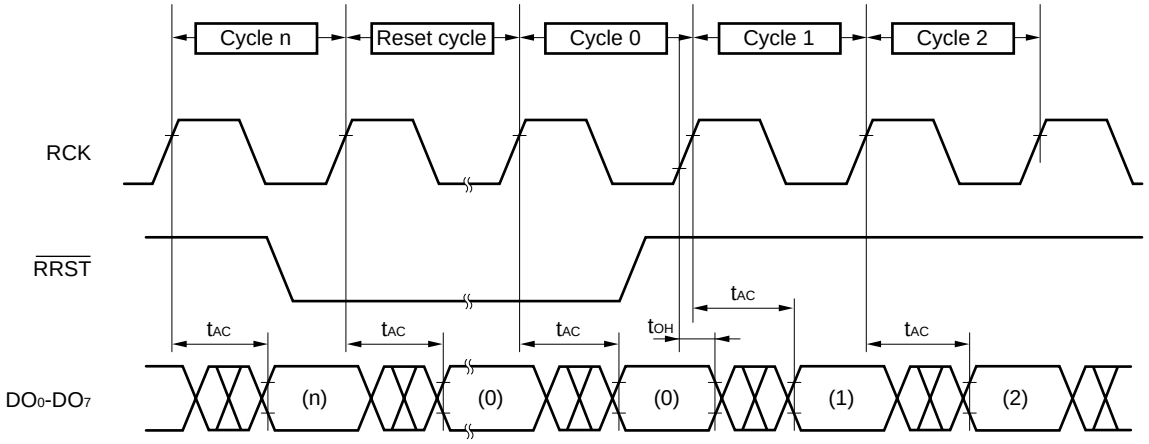


Caution In the μPD42280, output enable/disable using $\overline{OE}$ is performed in synchronism with RCK. It cannot be selected with the $\overline{OE}$ signal level only.

(4) Read reset

The read address can be reset to address 0 by inputting a low level to $\overline{\text{RRST}}$. The $\overline{\text{RRST}}$ signal can be input any time, but it must be input so as to satisfy the setup time and the hold time for the rising edge of RCK. Moreover, initialization of the read address using read reset can be performed independently of write reset.

Figure 2-13 Read Reset

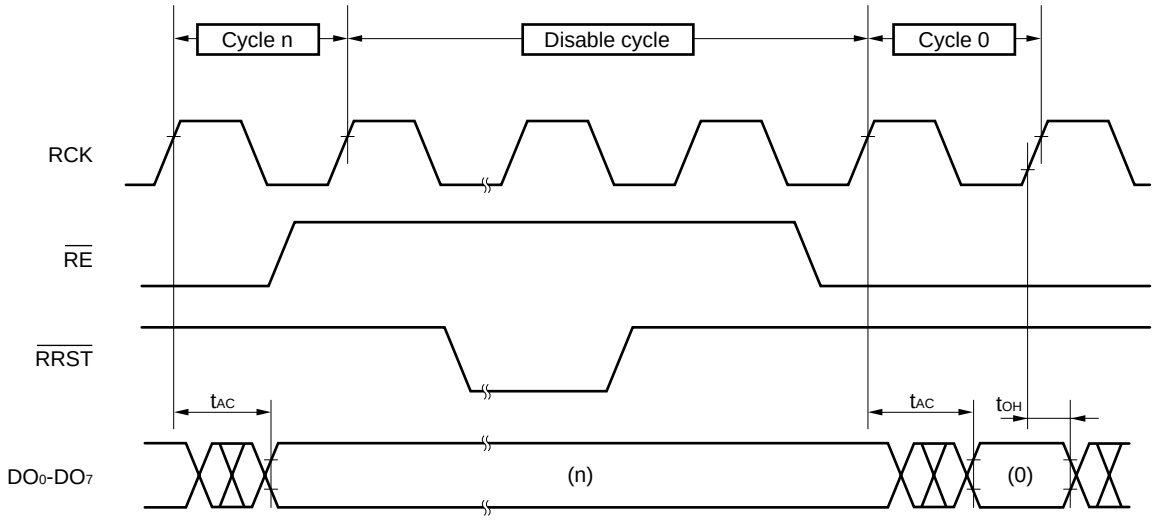


If read reset is extended over several cycles, address 0 data is read repeatedly. Therefore, when data overwrite is performed on the write side, overwritten data is output from the point when written data becomes read enabled.

(5) $\overline{RE}$ and $\overline{RRST}$ contention

If a low level is input to $\overline{RRST}$ when a high level is input to $\overline{RE}$ and the read address is stopped, the reset request is accepted, but reset is not executed. Reset is performed and the address pointer is reset to address 0 when $\overline{RE}$ becomes low level and the read address stop is cancelled.

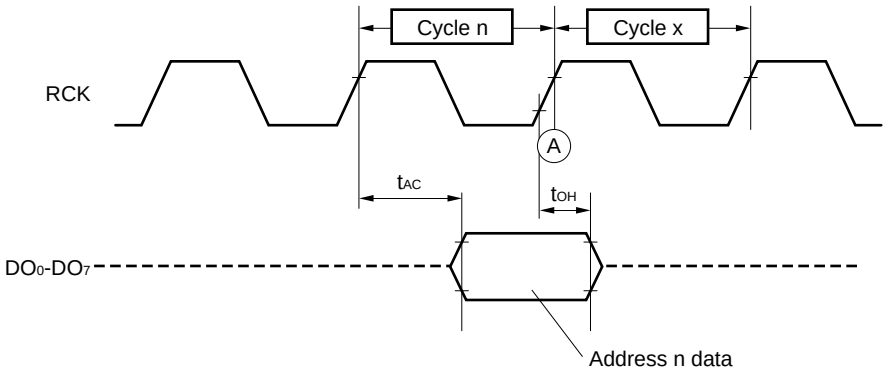
Figure 2-14 $\overline{RE}$ and $\overline{RRST}$ Contention



(6) Read cycle concept

Taking a look at a given read cycle, the $\overline{RE}$, $\overline{OE}$ and $\overline{RRST}$ signals are latched at the front rising edge. In Figure 2-15, if $\overline{RE}$ is high level, cycle x becomes a disable cycle. If $\overline{RRST}$ is low level, cycle x becomes a reset cycle.

Figure 2-15 Read Cycle



If at point A the $\overline{RE}$ and $\overline{RRST}$ signals are high and low level, respectively, cycle x becomes a disable cycle. At this time, low-level $\overline{RRST}$ input causes the read reset request to be accepted, and read reset is executed when $\overline{RE}$ becomes low level and the read address stop is cancelled.

When performing design using complex timing or verification, first take a look at the clock on the timing chart and divide the clock frequency into cycles. Then check the status of control signals ($\overline{WRST}$, $\overline{WE}$, $\overline{RRST}$, $\overline{RE}$, $\overline{OE}$) at the front and back rising edges of each cycle, and set the address of each cycle.

Doing the above will facilitate understanding of operations using complex timing.

2.2.4 New data and old data

The data flow in the μPD42280 is: Input → Write Data Register → DRAM cell → Read Data Register → Output. A certain period of time is required until data written to an address can be read. If read is attempted before the required period of time elapses, the old data written to the cell before write was performed will be read.

The last data written to an address is called new data.

Moreover, the data stored in a memory cell immediately before new data is written, in other words the data that was written to the same address before new data was written, is called old data. Expressed in a different way, the data that is overwritten when new data is written is called old data.

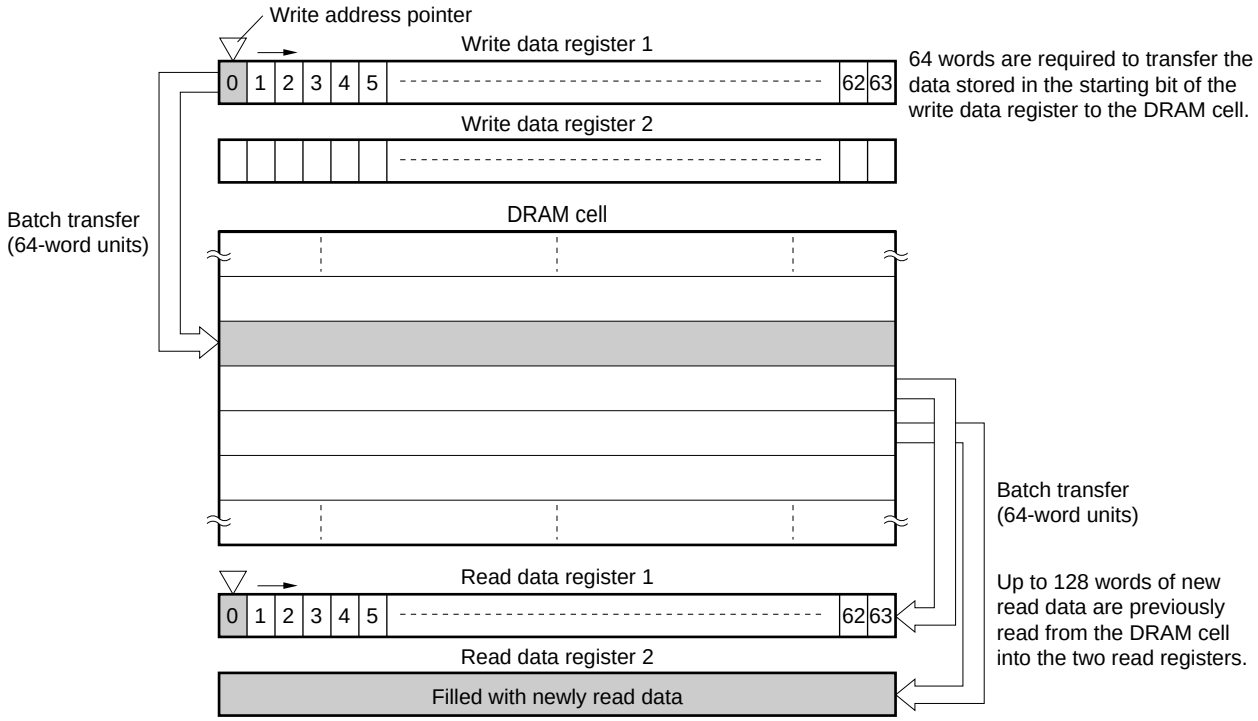
(1) New data read

To be sure to read new data, the write address must precede the read address by 200 cycles or more, but less than 262,224 cycles.

If using the watch example shown in Figure 2-3, new data read is possible if 200 cycles or more are placed between write address n and read address m (The maximum of less than 262,224 is set because if it were exceeded, one full address rotation would result, and the read address would then precede the write address).

Let us apply this to the internal operation described in section **2.1 Basic Operation**.

Figure 2-16 Conditions for μPD42280 Internal Data Operation and New Data Read



Data processed during write is first written to a write data register. However, the write data register must be filled with 64 words of data before its data can be transferred to memory cells, and therefore as many as 64 cycles are required in the worst case.

On the read side, the 64 words of data in the read data register to be read next are previously transferred from the memory cells. Therefore, up to 128 words of read data may already have been transferred from DRAM cells to the read data register. In other words, the number of cycles required to read data transferred to DRAM cells is 128 cycles in the worst case.

In consideration of the time required for actual data transmission, 8 cycles are needed in addition to the 192 cycles for the write and read operations above, and thus a total of 200 preceding cycles must be provided.

(2) Old data read

To read old data, there must be a difference of 0 cycles between the write address and the read address (write address and read address are the same).

As described above, access of DRAM cells is performed via the data registers, and therefore some time is required to read new data that has been written. In contrast, for SRAM addresses 0 to 79, after write is completed, read becomes possible after a short interval. Therefore, to be sure to read old data, the conditions described above must be observed.

2.2.5 Device initialization at power-on

At power-on, after the rated power supply voltage is reached, operation starts following a wait period of 100 μs or more. During this time, the internal pointer is undefined. Therefore perform initialization using $\overline{\text{WRST}}$ and $\overline{\text{RRST}}$, then set $\overline{\text{WE}}$ and $\overline{\text{RE}}$ to low level, and implement a timing cycle of 82 cycles or more. Normal write/read can then be performed following subsequent resets using $\overline{\text{WRST}}$ and $\overline{\text{RRST}}$.

Caution Data written or read before initialization is completed is not guaranteed.

[MEMO]

CHAPTER 3 RESTRICTIONS

The μPD42280 has the following restrictions. When using the μDP42280, be very careful to observe these restrictions.

(1) To read new data, the write address must precede the read address by 200 cycles or more and less than 262,224 cycles. To read old data, there must be 0 cycle difference between the write address and the read address (Refer to section **2.4.4 New data and old data**).

(2) The μPD42280 performs data transfer between the data registers and memory cell array in 64-word units. Therefore, when a low-level $\overline{\text{WRST}}$ signal is input to an address n higher than address 80, the old data of addresses higher than address n and up to address m indicated in the formula below is not guaranteed.

$$m = 143 + \text{int}\left[\frac{n - 80}{64}\right] \times 64$$

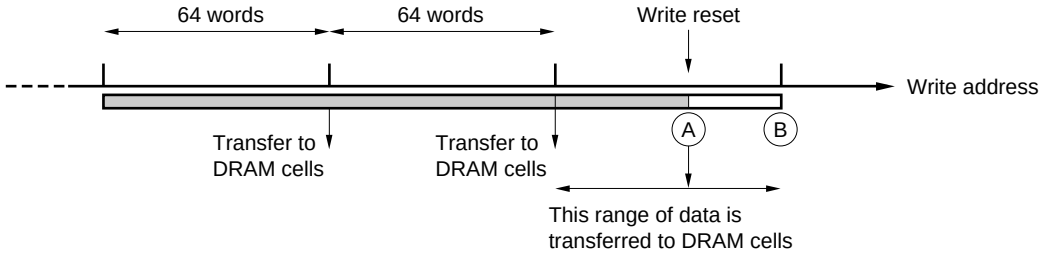
Remark $\text{int}\left[\frac{n - 80}{64}\right]$: Indicates only the integral part of the result of n – 80 divided by 64.

Example: If n = 280 $\rightarrow$ 3

Therefore, m = 335 and old data from address 280 to address 335 is not guaranteed.

This restriction applies to internal operation during write reset. When write reset is executed by inputting a low level to $\overline{\text{WRST}}$, the contents of the write data register at that moment are transferred to DRAM cells.
Figure 3-1 shows the data transmission from the write data register to DRAM chronologically. Data transfer from the write data register to DRAM is performed in units of 64 words.

Figure 3-1 Data Transfer During Write Reset



In Figure 3-1, when write reset is applied at point A, the data after point A up to point B is also transferred to DRAM. In other words, the old data stored in the transfer destination of this portion of data is overwritten by this portion of data.

(3) After write is started by inputting a low-level $\overline{\text{WRST}}$ signal, input the next low-level $\overline{\text{WRST}}$ signal 82 or more addresses apart.

Although this is highly improbable in actual practice, if no reset is executed but the operation transits from address 262,223 to address 0, this will be interpreted as a reset.

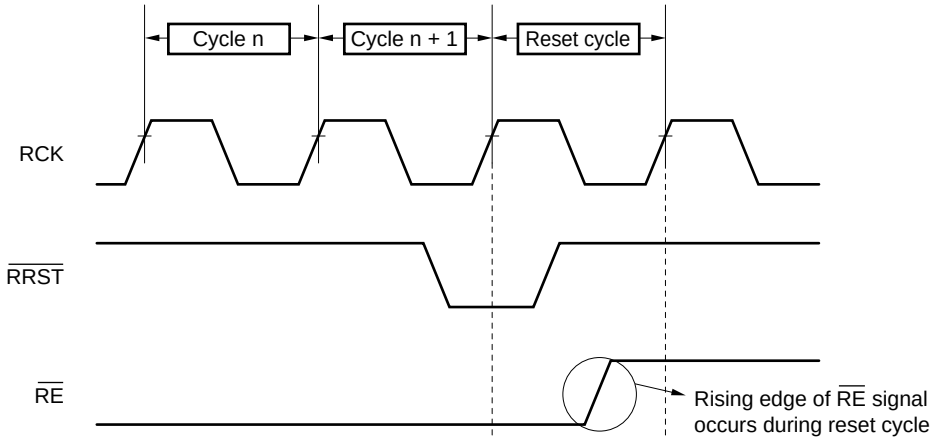
(4) After read is started by inputting a low-level $\overline{\text{RRST}}$ signal, input the next low-level $\overline{\text{RRST}}$ signal 82 or more addresses apart.

At the same time as (3) above, if no reset is executed but the operation transits from address 262,223 to address 0, this will be interpreted as a reset.

(5) Do not raise the $\overline{\text{RE}}$ signal from low level to high level at address 0 or during a reset cycle.

This is a restriction particular to internal device operation. Be sure not to perform the operation described in Figure 3-2.

Figure 3-2 Violation of Restriction (5)



Thus it can be seen that due to restriction (5), it is not possible to use $\overline{\text{RE}}$ to stop the read address at address 0 using RE.

To stop the read address at address 0, continue inputting low levels to $\overline{\text{RRST}}$. However, in this case, the data of address 0 is newly output each time RCK is input. Therefore, when new data is written to address 0 on the write side, and the written data becomes readable, new data is read.

CHAPTER 4 APPLICATION EXAMPLES

4.1 Data Buffer Application

To temporarily save serially input data and then read it again, write and read are executed independently. The processing sequence is generally described below.

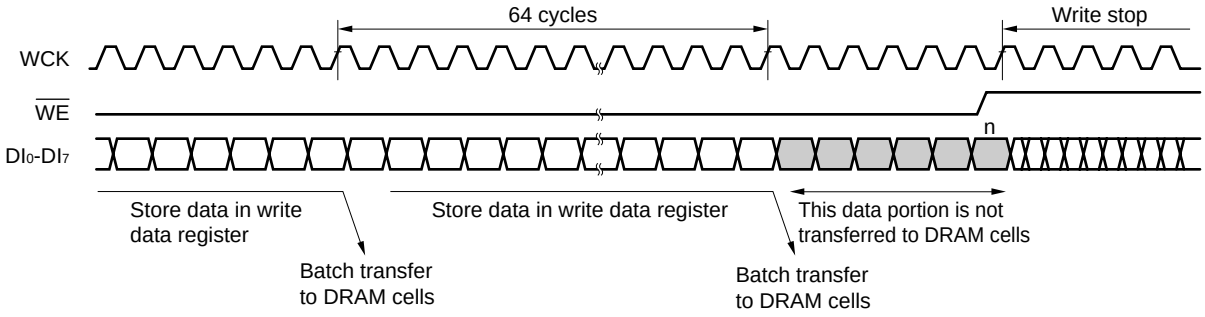
<1> Apply write reset and write data sequentially from address 0.
<2> When the required number of words of data is written, stop write.
<3> Apply read reset and read data sequentially from address 0.

4.1.1 Stopping write

To stop write after the required number of words of data is written, two methods can be employed. One is to terminate the WCK clock input, the other is to use the $\overline{WE}$ input. At this time, if write is stopped after finishing to write just the required number of words, up to 64 words max. of the data last written cannot be read.

This phenomenon is due to the internal operation of the μPD42280. In the μPD42280, the input data is stored once in a write data register, and then transferred to DRAM cells in units of 64 words. Therefore, when write is stopped at a certain point, the data stored in the write data register at that point is not transferred to DRAM cells and remains in the write data register. As a result, this data cannot be read.

Figure 4-1 Operation During Write Stop

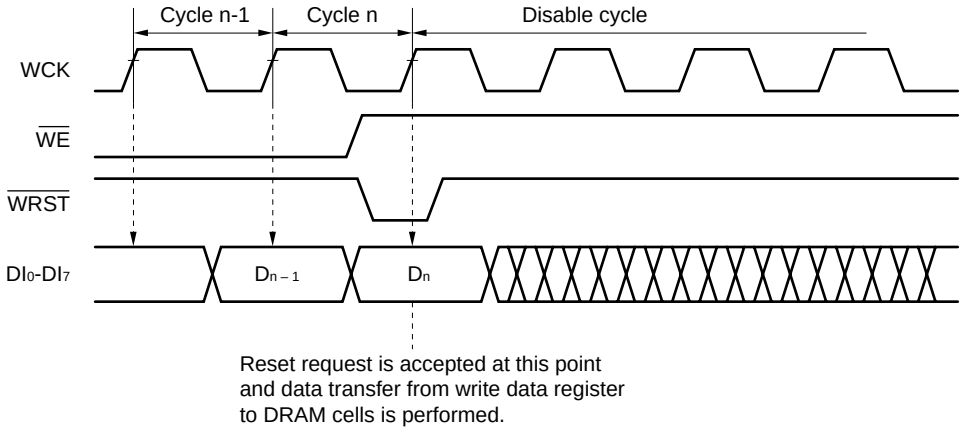


The following methods can be used to avoid this problem.

<1> Make $\overline{\text{WRST}}$ low level and apply it.

All the data that is input can be read-enabled by inputting a low level to $\overline{\text{WRST}}$ and transferring the data stored in the write data register at one time to DRAM cells. In this case, data transfer is independent of the status of $\overline{\text{WE}}$ and is performed at the rising edge of WCK when low-level input of $\overline{\text{WRST}}$ is accepted. Actually, when write reset is performed, data is input to address 0 at the cycle during which reset is applied, and the data in address 0 gets overwritten. Therefore, to protect the data in address 0, a high-level $\overline{\text{WE}}$ signal must be input to disable write before the low-level $\overline{\text{WRST}}$ is input.

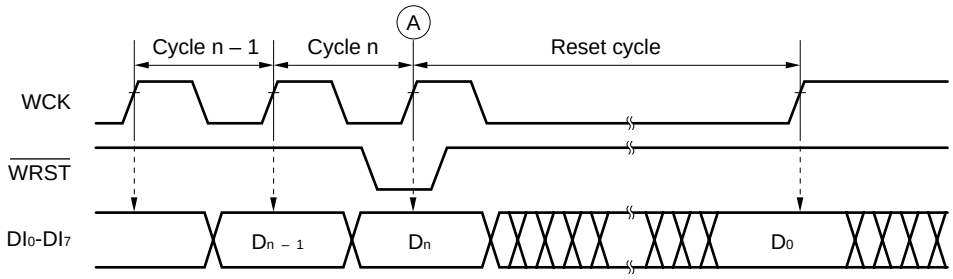
Figure 4-2 Write Stop Using $\overline{\text{WRST}}$ and $\overline{\text{WE}}$



Keep in mind that in this case, due to restriction (2) (refer to **CHAPTER 3 RESTRICTIONS**), a portion of old data of addresses higher than address n are not guaranteed. In the example shown in Figure 4-2, write reset is executed when $\overline{\text{WE}}$ becomes low level again, and write to address 0 is performed.

Figure 4-3 shows the implementation of the same operation by using WCK. Data fetch during writing is performed at the back rising edge of the cycle, thus in this example data is not overwritten to address 0.

Figure 4-3 Write Stop by Disabling WCK



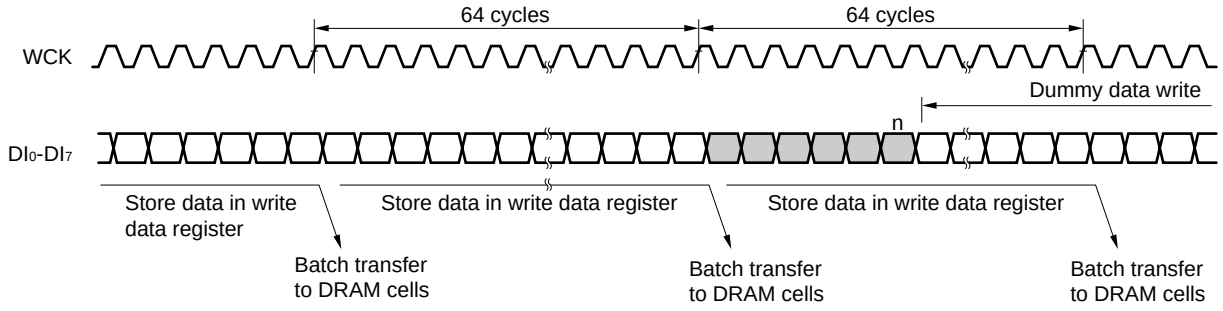
In this state, the reset cycle can be viewed as slow-footed. Data fetch is performed at the back rising edge of the cycle, thus data overwriting to address 0 while WCK is stopped cannot be performed. Data transfer from the write data register to DRAM cells using reset is performed at the rising edge of point A when the $\overline{\text{WRST}}$ low level is accepted.

At the point when the clock is input again and the last rising edge of the reset cycle is input, the data input to the DI pin is written to address 0.

<2> Write dummy data.

After writing the required number of words of data, write 64 or more words of dummy data. This ensures that all the required data will be transferred to DRAM cells.

Figure 4-4 Data Transfer to Memory Cells Using Dummy Data Write



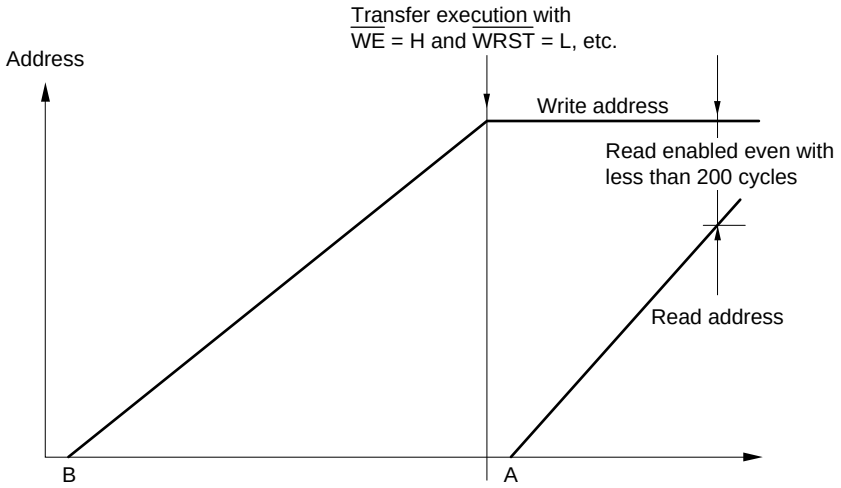
4.1.2 New data read conditions according to data buffer purpose

In this kind of application example, the write address remains stopped. At this time, the read address is incremented each time RCK is input, and gradually grows closer to the write address.

The operation at this time corresponds to new data read, but the new data read conditions mentioned earlier (the write address must precede the read address by 200 cycles or more) are not applied.

If read is performed in an entirely different time after write is completed (if write and read are not performed simultaneously), new data is unconditionally readable (actually, some time is required for data transfer from the write data register to DRAM cells, but read starts from address 0 and in the process of the read address being incremented, the write data always becomes readable).

Figure 4-5 New Data Read Conditions When Write and Read are Independent

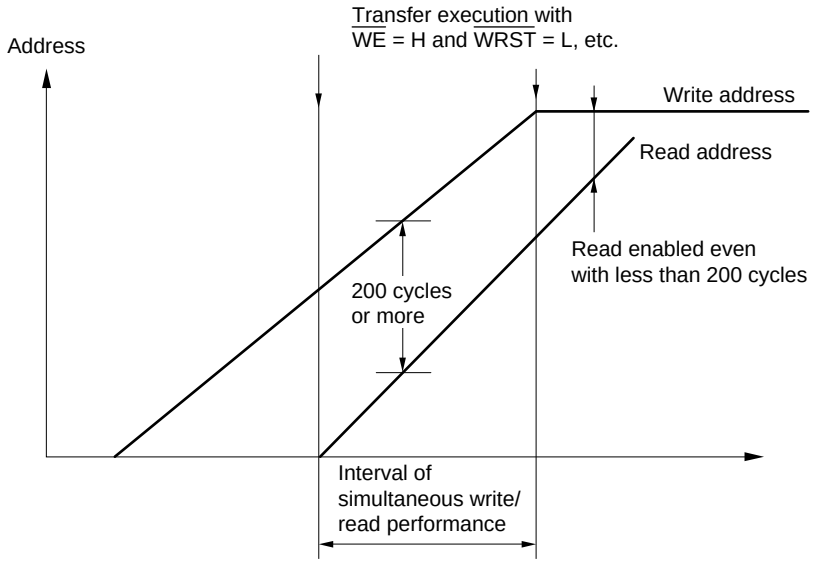


At this time, perform read reset by inputting a low-level $\overline{\text{RRST}}$ signal immediately before point A when read is started.

For example, if new data write is not performed at point B, when a low-level $\overline{\text{RRST}}$ signal is input at this time, the data before new data was written to the read data register gets transferred, and as a result, old data may wind up being read.

If read is started after a set delay time after write starts, the write address must precede the read address by 200 cycles or more while write and read are performed simultaneously.

Figure 4-6 New Data Read Conditions During Interval of Write/Read Contention



After data transfer is performed from the write data register to DRAM cells and write is stopped, data read is possible unconditionally. In this case, perform low-level input to $\overline{\text{RRST}}$ immediately before starting read.

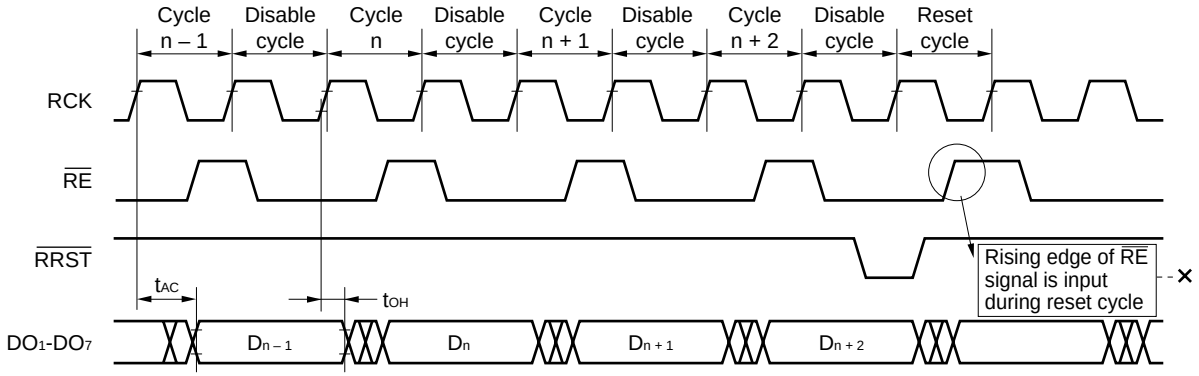
As a result of the above, if the RCK cycle is longer compared to the WCK cycle (the WCK frequency is higher than the RCK frequency), and if the write address precedes the read address by 200 cycles or more when write stops, this means that the new data that was written is read-enabled.

4.2 Intermittent Read Operation Using $\overline{RE}$ Function

In the case of a system using the μPD42280 with a single system clock, an application system in which the intervals between reads are controlled using the $\overline{RE}$ function can be designed.

Such an application example has the advantage that the interval between data reads can be changed through manipulation of the $\overline{RE}$ signal while inputting a fixed-frequency system clock to RCK. However, this will inevitably result in violation of restriction (5) (refer to **CHAPTER 3 RESTRICTIONS**). Figure 4-7 shows an example where data read is performed using $\overline{RE}$ and the rate of 1/2 RCK.

Figure 4-7 Intermittent Read Using $\overline{RE}$



In this way extending the read data of address 0 violates restrictions.

In the μPD42280, data write and read are basically controlled with WCK and RCK. Therefore, for application examples such as the one described above, implementing control using the clock signal using a method such as feeding the $\overline{RE}$ signal to RCK is recommended.

4.3 Delay Line Application

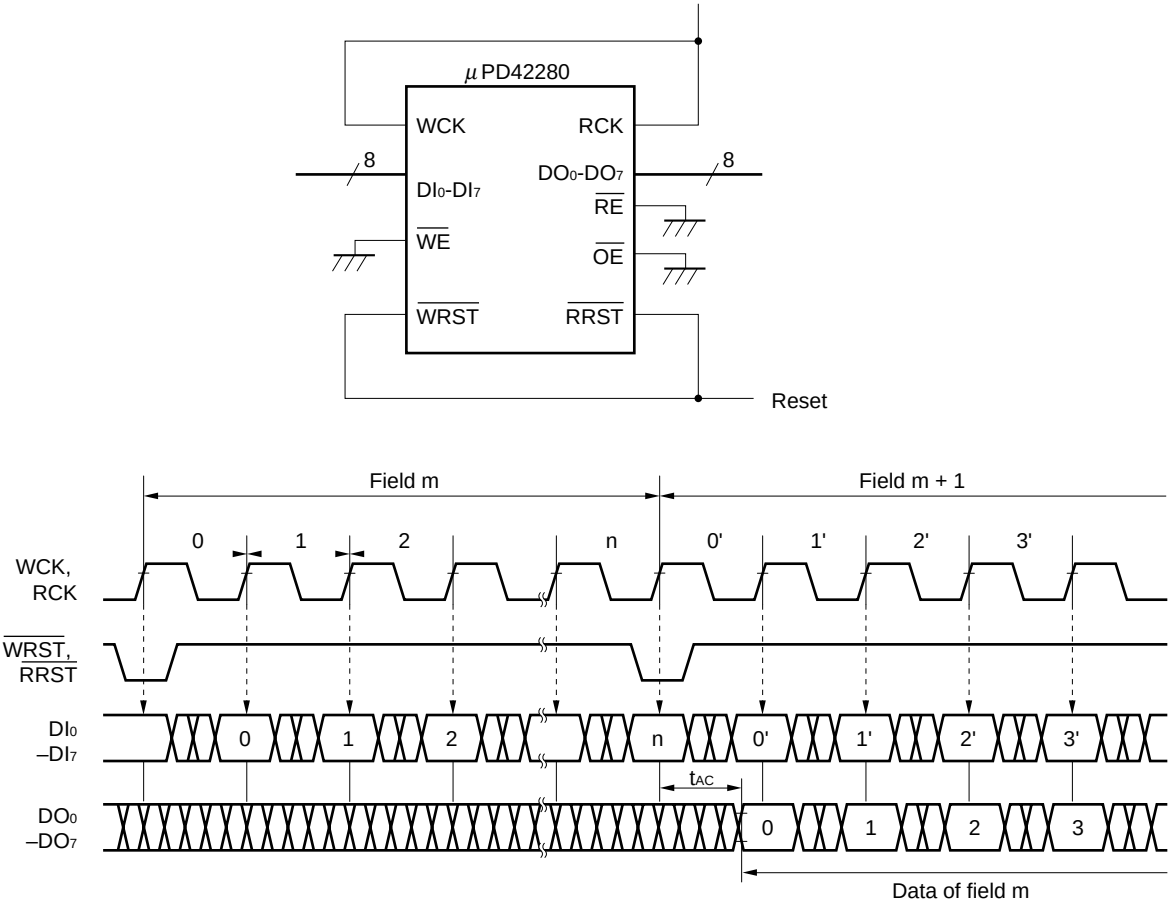
This purpose of this type of application is to implement a fixed delay for continuous data sampled with a constant clock. It is suited for realizing field delay of digitized TV signals. Two methods can be employed to realize a delay line, one using old data read, and the other using new data read.

4.3.1 Method using old data read

Input a common sampling clock to WCK and RCK, and simultaneously input a low level to $\overline{\text{WRST}}$ and $\overline{\text{RRST}}$ using an interval corresponding to the delay time.

In this way, if the difference between the write address and the read address is 0, old data is read.

Figure 4-8 1 Field Delay Line

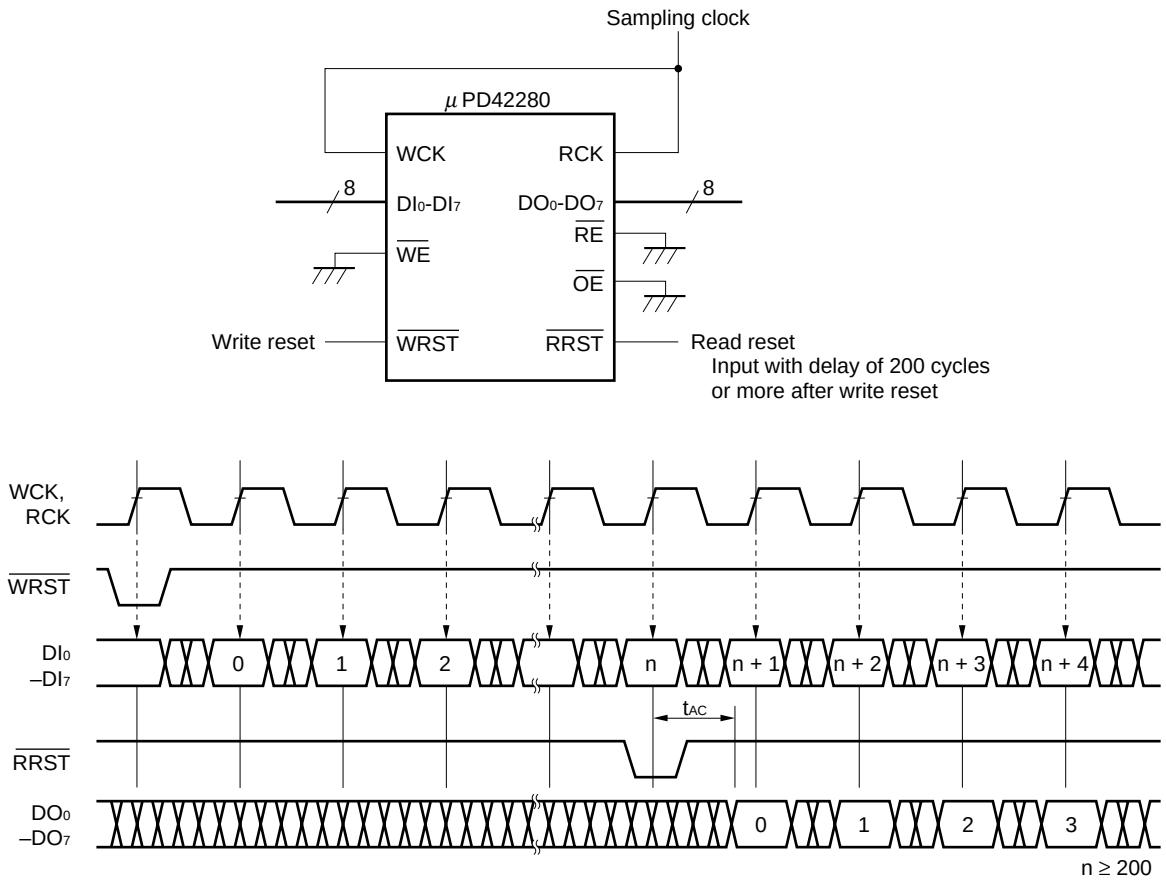


In this case, the delay that can be set is 82 or more, and up to 262,224 cycles (refer to restrictions (4) and (5) in **CHAPTER 3 RESTRICTIONS**).

4.3.2 Method using new data read

If read reset is input 200 or more cycles after write reset, the data written immediately before (new data) can be read. Figure 4-9 shows a delay line using new data read.

Figure 4-9 Delay Line Using New Data Read



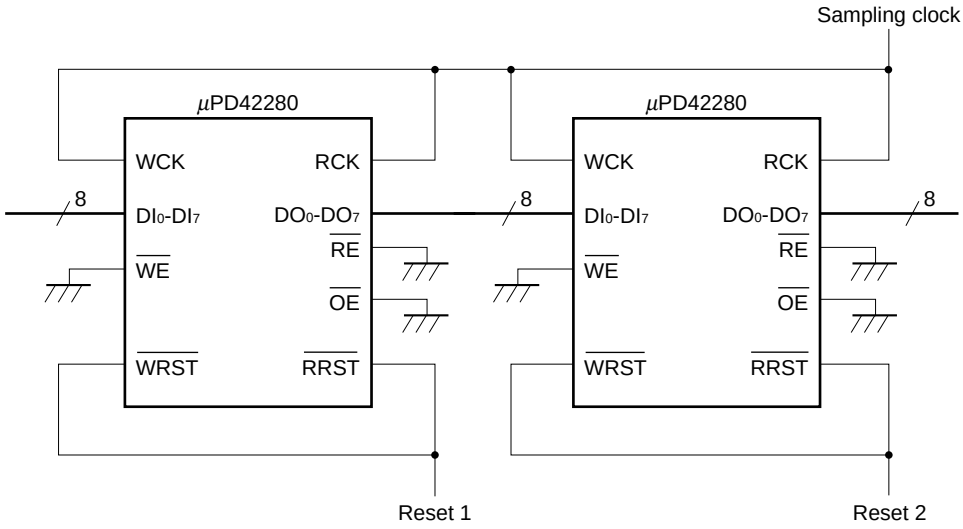
In this case, the delay that can be set is 200 cycles or more, up to 262,223 cycles.

Control of the delay line using old data read is easy. This method is suited for a fixed delay line. For applications that call for a variable delay line, control of the delay line using new data read is recommended.

Application examples such as a delay line require the application of read and write resets at set intervals, and automatically satisfy device initialization conditions (however, data read and written immediately after power-on when initialization conditions are not yet satisfied are not guaranteed).

A delay exceeding 262,224 cycles can be implemented by connecting two or more μPD42280s in cascade.

Figure 4-10 Delay Line Cascade Connection (Old Data Read)



[MEMO]

CHAPTER 5 CAUTIONS

5.1 Data Contention in SRAM Area

In case of write/read contention in the SRAM area for the same address in the IC, the data may be destroyed.

As described earlier, the memory structure of the μPD42280 consists of an 80-byte SRAM from addresses 0 to 79 and DRAM starting from address 80.

Read and write from/to the DRAM area are performed via data registers, but are controlled so that no contentions arise due to internal data transfer, and asynchronous write/read is performed.

On the other hand, in the SRAM area, data is directly written and read. The internal SRAM of the μPD42280 supports dual access and thus can be simultaneously read and written.

Write to a write address in the SRAM area is executed unconditionally. Therefore, write and read are performed completely asynchronously, and if at the same time that data is read from an address in SRAM, data is being written to the same address, the read data will be switched midway and may be destroyed (data that is neither old or new will be read).

[MEMO]

CHAPTER 6 FREQUENT Q&A

Q1. What happens (read data) when the difference between the write address and the read address is between 1 and 199 cycles?

A1. Old data is read because 200 cycles are required in order to read data that has been written to addresses 80 to 262223 of DRAM.
In addresses 0 to 79 of SRAM, following write completion, new data becomes read-enabled after a short time so that new data may be read.
To ensure that old data in SRAM will be read, the interval between the write address and the read address must be 0 cycle (write address and read address are the same).

Q2. What happens when, after starting write (read) by inputting a low-level $\overline{\text{WRST}}$ ($\overline{\text{RRST}}$) signal, the next input of low-level $\overline{\text{WRST}}$ ($\overline{\text{RSST}}$) is separated by less than 82 addresses (violation of restrictions (3) and (4))?

A2. Various malfunctions such as data destruction and failure to perform normal reset may occur.
Moreover, when reset is performed within 81 addresses, (violation of restrictions (3) and (4)), there is no particular problem regarding subsequent data if reset is performed after an interval of 82 address or more.
Since these restrictions specifically apply to internal operation of the device, be careful not to violate them.

Q3. Must a clock be input for the refresh timer operation?

A3. No external clock needs to be input.
In the μPD42280, the refresh timer clock is generated internally when power is applied, therefore, as long as the power is not turned off, the refresh timer goes on functioning (the refresh timer continues operating even without WCK and RCK inputs)

Q4. During device initialization at power-on, is there a problem if $\overline{\text{WE}}$ and $\overline{\text{RE}}$ are changed to high level during the execution of 82 or more dummy cycles?

A4. This is not a problem as long as 82 or more dummy cycles are executed.
Moreover, the write and read sides being asynchronous, separately initializing them is not a problem.
Keep in mind that data written/read before initialization is completed is not guaranteed.

Q5. What happens if restriction (5) is violated?

A5. Various problems can occur, such as address 0 or address 1 being skipped.
Therefore, please design the timing so as not to violate restriction (5).
Figure 6-1 shows timing chart examples violating restriction (5).

Q6. Why should the write address precede the read address by 200 cycles or more when new data is read?

A6. Data processed during write is first written to a write data register. However, the write data register must be filled with 64 words of data before its data can be transferred to memory cells, and therefore as many as 64 cycles are required in the worst case.
On the read side, the 64 words of data in the read data register to be read next are previously transferred from the memory cells. Therefore, up to 128 words of read data may already have been transferred from DRAM cells to the read data register. In other words, the number of cycles required to read data transferred to DRAM cells is 128 cycles in the worst case.
In consideration of the time required for actual data transmission, 8 cycles are needed in addition to the 192 cycles for the write and read operations above, and thus a total of 200 preceding cycles must be provided. Refer to section **2.2.4 New data and old data** (page 21) for detail.

Q7. If "invalid" data was read after a write operation, what step(s) could the user have missed that may have caused this error?

A7. 1) Check if more than 82 dummy cycles of write/read were applied during the initialization procedure. This is part of initializing the circuitry of the SRAM buffer and must be performed initially to guarantee valid data output. Refer to section **2.2.5 Device initialization at power-on** (page 21) for the initialization procedure.

2) Make sure that the restrictions on this device listed in **Chapter 3** were not violated.

Q8. After writing 200 bytes of data and asserting RE control, can the first byte of data be available on the same clock cycle as the RE assertion?

A8. The first byte of data is available on the next clock cycles after the RE assertion. This is due to the need of satisfying the t_{AC} parameter timing. Refer to the timing diagram in **Figure 2-14 $\overline{\text{RE}}$ and $\overline{\text{RRST}}$ Contention** (page 18).

Q9. What is the power consumption of the μPD42280?

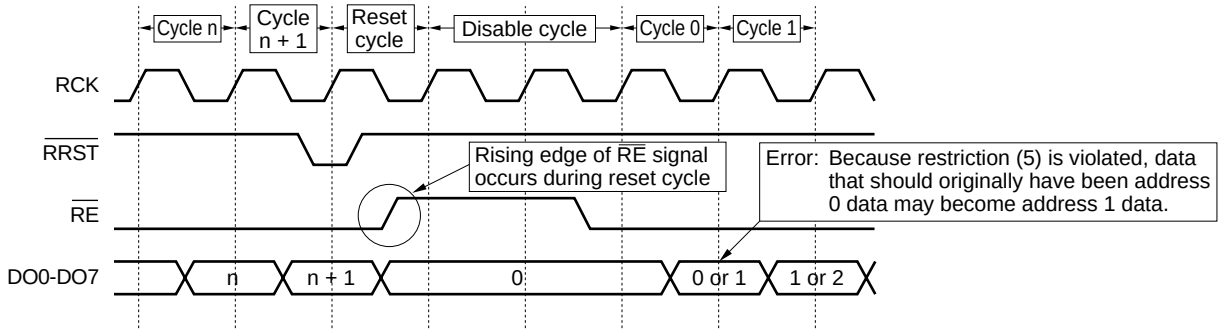
A9. The power consumption depends on the device read cycle time, as follows.
Power consumption (t_{WCK}, t_{RCK} = 30 ns) = $V_{DD\ max}$ * $I_{CC1\ max}$ = 495 mW Max.
Power consumption (t_{WCK}, t_{RCK} = 60 ns) = $V_{DD\ max}$ * $I_{CC2\ max}$ = 330 mW Max.

Q10. What is the significance of the TEST pin to the user?

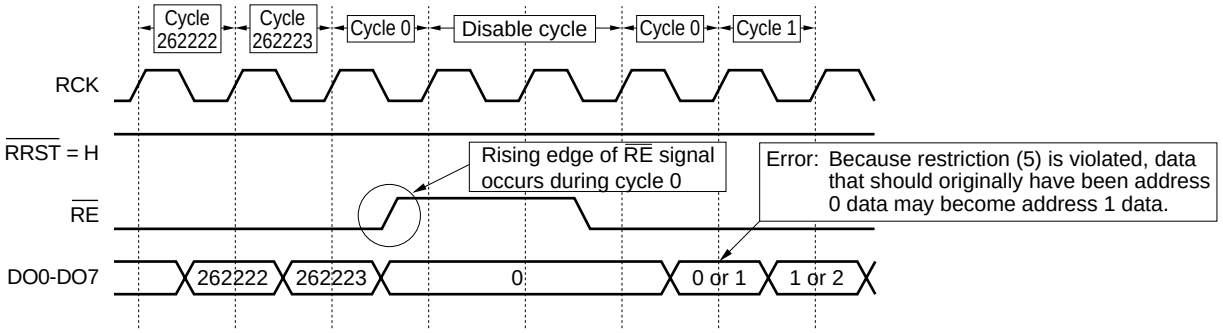
A10. This pin is only used for NEC's internal testing. It should be tied to a ground level or logic low (–1.0 V to +0.8 V).

Figure 6-1 Restriction (5) Violation Examples

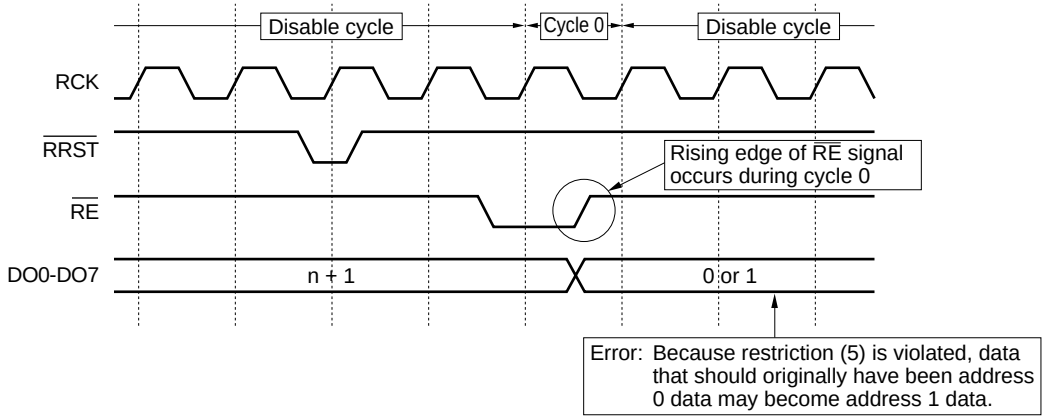
- **Restriction (5) Violation Example 1**



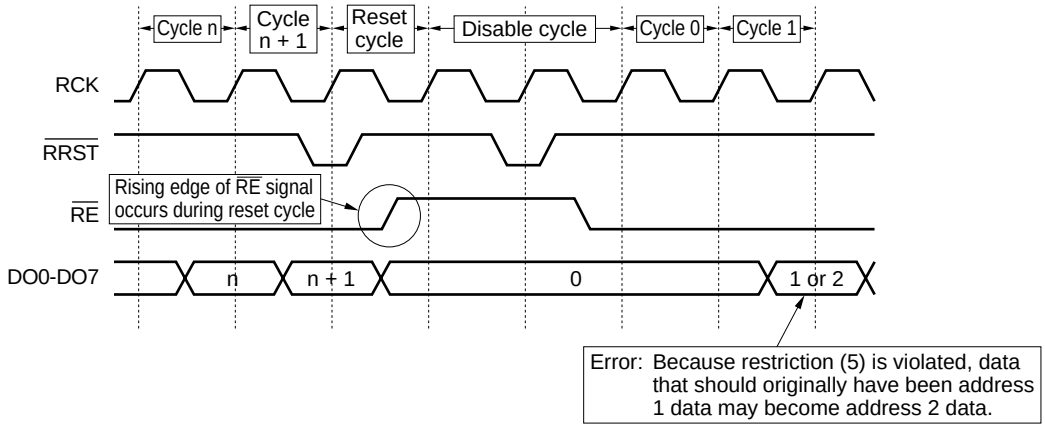
- **Restriction (5) Violation Example 2**



- **Restriction (5) Violation Example 3**



- **Restriction (5) Violation Example 4**



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