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April 1st, 2010
Renesas Electronics Corporation

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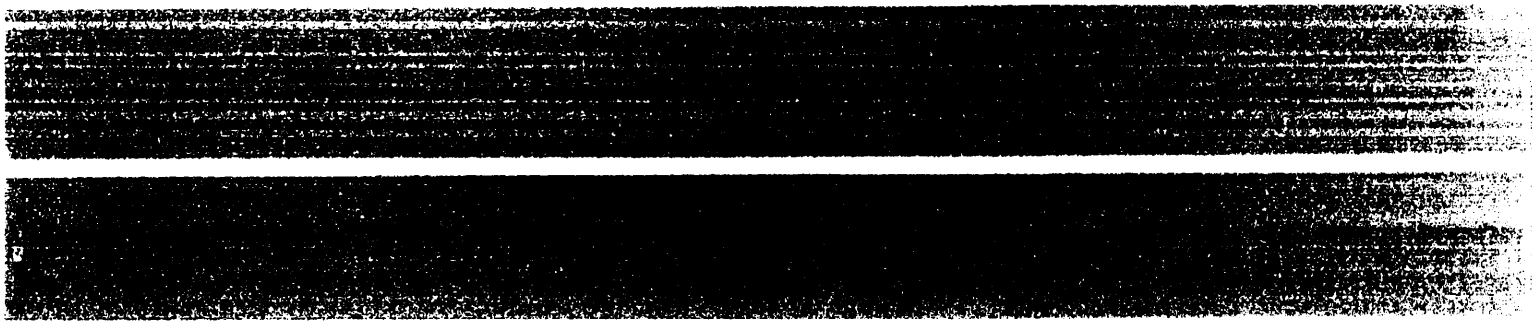
Phase-out/Discontinued

μPD1700 SERIES
EV-1709
USER'S MANUAL



NEC Corporation

C001

Phase-out/Discontinued

μPD1700 SERIES
EV-1709
USER'S MANUAL

NEC Corporation

C002

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CHAPTER 1. INTRODUCTION

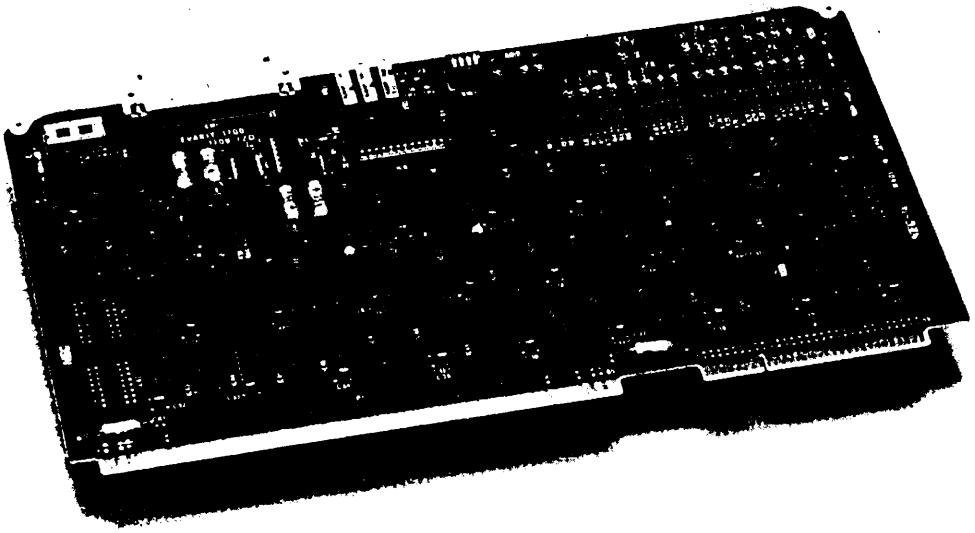
EV-1709 is designed for developing programs for μPD1709 and μPD1716 using the EVAKIT-1700 and SE-1700 option I/O board.

The μPD1709 functions handled by EV-1709 include the PB_0 to PB_3, PC_2 to PC_3, AD, CGP, and serial I/O functions.

Since μPD1716 has functions similar to μPD1709 functions, this user's manual has been prepared for use in developing programs for both devices, but with main emphasis on μPD1709.

When using EV-1709/EV-1716, also refer to the EVAKIT-1700 User's Manual and SE-1700 Operation Manual (EEP-554 and EEP-1004 respectively).

The EV-1709 board



EV-1709 Accessories

1. One 34-pin socket and cable for CN1
2. One 16-pin IC socket and cable for CN2

CHAPTER 2. SPECIFICATIONS

Product name	EV-1709
Functions	μPD1709 and μPD1716 I/O emulation
Operating temperature range	0 to 40 °C
Storage temperature range	−10 to 50 °C (but without condensation)
Power supply	+5 V 1A MAX.
	+15 V 100mA MAX.
	−15 V 100mA MAX.
Board dimensions	304.8 x 171.5 x 12.7mm
	(12.00 x 6.75 x 0.5 inches)

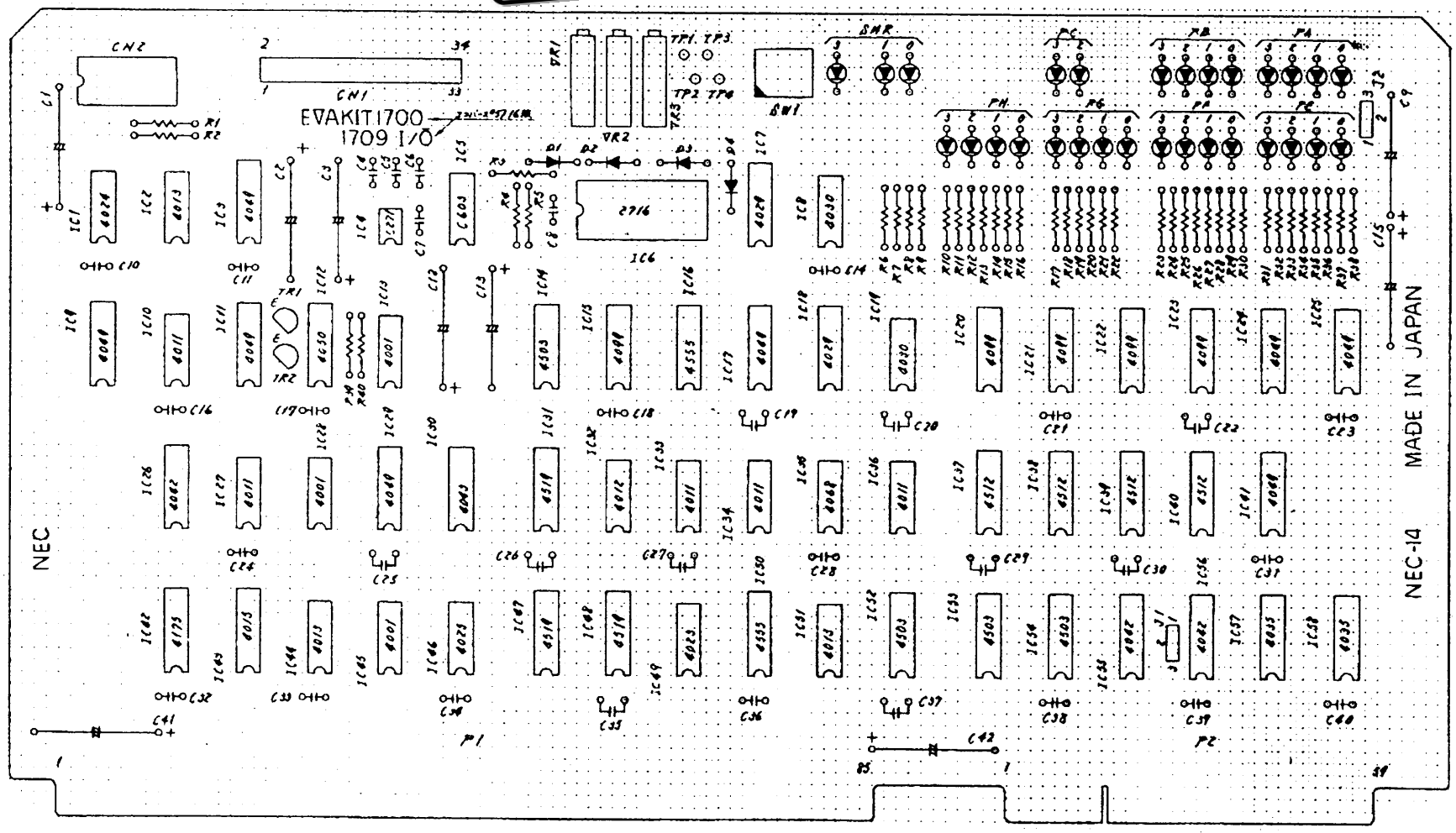
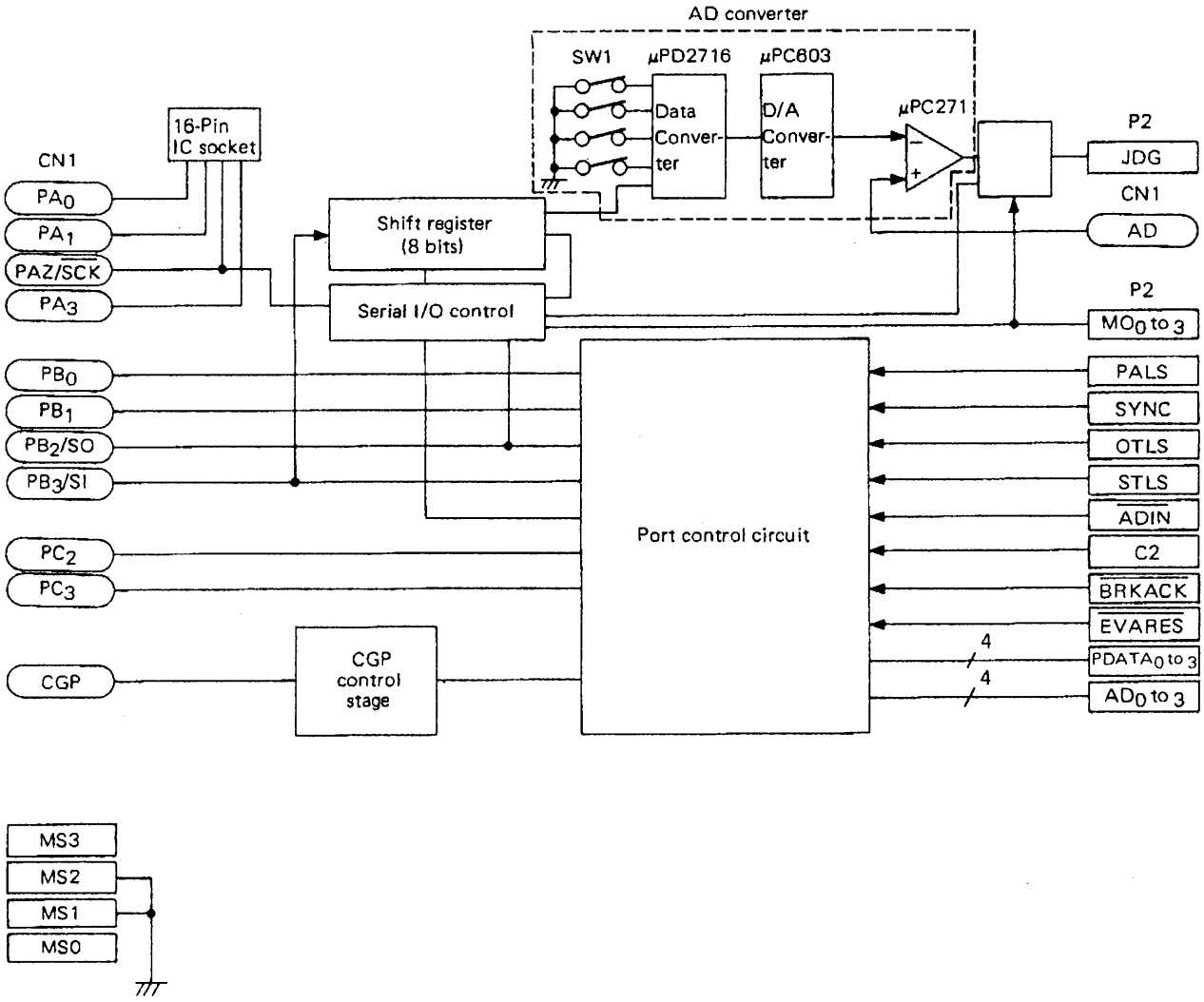


Fig. 2-1 EV-1709 Component Layout

CHAPTER 3. BLOCK DIAGRAM



CHAPTER 4. OPERATING PROCEDURES

4.1 EV-1709 USED FOR μPD1709 WITH EVAKIT-1700

When used for μPD1709 with EVAKIT-1700, set up EV-1709 in the following way.

(1) Jumper settings (EVAKIT-1700 CPU board)

Short-circuit the J2 (2–3) jumper on the CPU board to put the CPU board KEY input circuit into 1709 mode.

(2) Jumper settings (EVAKIT-1700 PLA board)

Short-circuit the J1 (1–15, 2–16, 3–17, 4–18, 5–19, 6–20, and 7–21) jumpers on the PLA board to put the segment output into CMOS push-pull mode.

Although the μPD1709 segment output is the N-ch open drain, the EVAKIT-1700 PLA board is not equipped with a corresponding output circuit. Therefore, the PLA board segment output is put into CMOS push-pull mode before connecting the external N-ch open drain driver. Details on this external driver circuit are given in Section 4.5.

(3) Jumper settings (EV-1709 board)

Short circuit J2 (1–2) to connect the power supply to the LED used to indicate port status on the board. Note that since there is an increase in electrical noise on the board when the LED is on, short-circuiting J1 (2–3) can turn the LED off when AD converter is used.

To set the circuit used to initialize the PB and PC ports, short-circuit J1 (2–3).

(4) SW1 setting (EV-1709 board)

Set all 4 bits in this switch to the on position.

(5) Slot mounting

The EVAKIT-1700 has six slot positions. EV-1709 can be mounted in either of the top two vacant slots.

(6) Connector connections (EVAKIT-1700 and EV-1709)

Use the accessory 16-pin flat cable to connect the EVAKIT-1700 CPU board CN4 connector (16-pin IC socket) to CN2 located in the top left hand corner of EV-1709.

This connection carries PA_0 to PA_3 signals from the CPU board to EV-1709.

(7) Connections to target system

Connections to the target system are made via the following four connectors.

① CPU board CN1 (cable supplied with EVAKIT-1700)

1 to 4.	(Not used)
5.	CE (input)
6.	(Not used)
7.	INT (input)
8 to 11.	(Not used)
12 to 16.	GND

② CPU board CN3 (cable supplied with EVAKIT-1700)

1 to 2.	(Not used)
3.	FM (VCOH input)
4.	GND
5.	PSC (output)

6. GND
7 to 8. (Not used)
9. EO_1 (output)
10. GND
11 to 12. (Not used)

③ PLA board CN1 (cable supplied with EV-1700)

An external N-ch open drain driver must be connected to the segment and digit outputs. See Section 4.5 for details on this external driver circuit.

1. GND
2. Sa (output)
3. Sb (output)
4. Sc (output)
5. Sd (output)
6. Se (output)
7. Sf (output)
8. Sg (output)
9 to 10. (not used)
11. D_3 (output) . . . . . Used as D_2
12. D_4 (output) . . . . . Used as D_3
13 to 16. (Not used)

④ EV-1709 CN1 (cable supplied with EV-1709)

1 to 2. (Not used)
3. $PA_2/\overline{SCK}$ (input/output)
4. PA_3 (input/output)
5. PB_0 (input/output)
6. PB_1 (input/output)
7. PB_2/SO (input/output)
8. PB_3/SI (input/output)
9. PC_2 (output)
10. PC_3 (output)
11. CGP (output)
12 to 14. GND
15. AD_0 (input)
16. GND
17 to 34. (Not used)

4.2 EV-1709 USED FOR μPD1716 WITH EVAKIT-1700

When used for μPD1716 with EVAKIT-1700, set up EV-1709 in the following way.

(1) Jumper settings (EVAKIT-1700 CPU board)

Short-circuit the J2 (2–3) jumper on the CPU board to put the CPU board KEY input circuit into 1716 mode.

(2) Jumper settings (EVAKIT-1700 PLA board)

Short-circuit the J1 (1–15, 2–16, 3–17, 4–18, 5–19, 6–20, and 7–21) jumpers on the PLA board to put the segment output into CMOS push-pull mode.

(3) Jumper settings (EV-1709 board)

Short circuit J2 (1–2) to connect the power supply to the LED used to indicate port status on the board. Note that since there is an increase in electrical noise on the board when the LED is on, short-circuiting J1 (2–3) can turn the LED off when AD converter is used.

To set the circuit used to initialize the PB and PC ports, short-circuit J1 (2–3).

(4) SW1 setting (EV-1709 board)

Set all 4 bits in this switch to the on position.

(5) Slot mounting

The EVAKIT-1700 has six slot positions. EV-1709 can be mounted in either of the top two vacant slots.

(6) Connector connections (EVAKIT-1700 and EV-1709)

Use the accessory 16-pin flat cable to connect the EVAKIT-1700 CPU board CN4 connector (16-pin IC socket) to CN2 located in the top left hand corner of EV-1709.

This connection carries PA_0 to PA_3 signals from the CPU board to EV-1709.

(7) Connections to target system

Connections to the target system are made via the following four connectors.

① CPU board CN1 (cable supplied with EVAKIT-1700)

1 to 4.	(Not used)
5.	CE (input)
6.	(Not used)
7.	INT (input)
8 to 11.	(Not used)
12 to 16.	GND

② CPU board CN3 (cable supplied with EVAKIT-1700)

To emulate the μPD1716 VCOH (FM) input pin, an external prescaler μPB553AC must be connected using the following FM and PSC pins. See Section 4.6 for details on this external driver circuit.

1.	AM (AM VCO input)
2.	GND
3.	FM (FM VCO input)
4.	GND
5.	PSC (output)
6.	GND
7 to 8.	(Not used)
9.	EO_1 (output)
10.	GND
11.	EO_2 (output)
12.	GND

③ PLA board CN1 (cable supplied with EV-1700)

1.	GND
2 to 9.	(Not used)
10.	D_2 (output) ..... Used as D_1
11.	D_3 (output) ..... Used as D_2
12.	D_4 (output) ..... Used as D_3
13 to 16.	(Not used)

④ EV-1709 CN1 (cable supplied with EV-1709)

1.	PA_0	(input/output)
2.	PA_1	(input/output)
3.	$PA_2/\overline{SCK}$	(input/output)
4.	PA_3	(input/output)
5.	PB_0	(input/output)
6.	PB_1	(input/output)
7.	PB_2/SO	(input/output)
8.	PB_3/SI	(input/output)
9.	PC_2	(output)
10.	PC_3	(output)
11.	(Not used)	
12 to 14.	GND	
15.	AD_0	(input)
16.	GND	
17 to 34.	(Not used)	

4.3 EV-1709 USED FOR μPD1709 WITH SE-1700

When used for μPD1709 with SE-1700, set up EV-1709 in the following way.

(1) Jumper settings (SE-1700)

J1	Short (8–9, 10–11, 12–13, 14–15, 16–17, 18–19, and 20–21)
J2	Short (1–2)
J3	Short (1–2)
J4	Short (1–2)
J5	Short (1–2)
J6	Short (1–2)
J7	Short (1–2)
J8	Short (3–5 and 4–6)
J9	Open
J10	Open

(2) SPLSEL switch setting

Although the SPLSEL value can be set by CL command or when the PLA object is loaded in cases where EVAKIT-1700 is used, this value is set by an on-board switch when SE-1700 is used. After first checking the source list, set to 2 or 3.

On the object board, the SPLSEL takes a value obtained by subtracting 1 from the actual value. That is, SPLSEL is 2 if the actual value is 3, and 1 if the actual value is 2. This change is made automatically by the assembler.

This must be kept in mind, therefore, when setting the SPLSEL switch after checking the object code value.

(3) PROM mounting

The PROM used is the 2716 device. Programs are written divided into eight high order bits (PROG–HIGH) and eight low order bits (PROG–LOW) mounted to the respective IC26 and IC25 sockets. The segment PLA (SEG–PLA) is connected to IC17, and the digit PLA (DIG–PLA) is connected to IC5 socket.

Refer to Chapter 5 of the SE-1700 Instruction Manual (EEP–1004) for details on PROM writing procedures.

(4) Jumper settings (EV-1709 board)

Short circuit J1 (1–2) to connect the power supply to the LED used to indicate port status on the board. Note that since there is an increase in electrical noise on the board when the LED is on, short-circuiting J1 (2–3) can turn the LED off when AD converter is used.

To set the circuit used in initializing (Hi–Z) the PB and PC ports, short-circuit J2 (2–3).

(5) SW1 setting (EV-1709 board)

Set all 4 bits in this switch to the on position.

(6) Rack mounting

The rack used with SE-1700 contains four slots. The SE-1700 and EV-1709 boards may be mounted in any slots.

(7) Connections SE-1700 and EV-1709

Used the accessory 16-pin flat cable to connect the SE-1700 CN4 connector (16-pin IC socket) to CN2 located in the top left hand corner of EV-1709.

This connection carries PA_0 to PA_3 signals from the CPU board to EV-1709.

(8) Connections to target system

Connections to the target system are made via the following four connectors.

① SE-1700 board CN1 (cable supplied with SE-1700)

1 to 4.	(Not used)
5.	CE (input)
6.	(Not used)
7.	INT (input)
8 to 11.	(Not used)
12 to 16.	GND

② SE-1700 board CN3 (cable supplied with SE-1700)

1 to 2.	(Not used)
3.	FM (FM VCO input)
4.	GND
5.	PSC (input)
6.	GND
7 to 8.	(Not used)
9.	EO_1 (output)
10.	GND
11 to 12.	(Not used)

③ SE-1700 CN2 (cable supplied with SE-1700)

With only digit outputs, the N-ch open drain driver must be connected externally. See Section 4.5 for details on the external driver circuit. Unlike EVAKIT-1700, SE-1700 is equipped with the built-in N-ch open drain driver circuit. Therefore, an external driver circuit is not required for segment outputs.

1.	GND
2.	Sa (output)
3.	Sb (output)
4.	Sc (output)
5.	Sd (output)
6.	Se (output)

7. Sf (output)
8. Sg (output)
9 to 10. (Not used)
11. D_3 (output) ..... Used as D_2
12. D_4 (output) ..... Used as D_3
13 to 16. (Not used)

④ EV-1709 CN1 (cable supplied with EV-1709)

1 to 2. (Not used)
3. $PA_2/\overline{SCK}$ (input/output)
4. PA_3 (input/output)
5. PB_0 (input/output)
6. PB_1 (input/output)
7. PB_2/SO (input/output)
8. PB_3/SI (input/output)
9. PC_2 (output)
10. PC_3 (output)
11. CGP (output)
12 to 14. GND
15. AD_0 (input)
16. GND
17 to 34. (Not used)

(9) Power connections

The power supply voltages are +5V, +15V and −15V. Using the cables supplied with SE-1700, connect to the connectors below the racks.

+5V: Main power supply for SE-1700 and EV-1709
±15V: Power supply for AD converter

4.4 EV-1709 USED FOR μPD1716 WITH SE-1700

When used for μPD1716 with SE-1700, set up EV-1709 in the following way.

(1) Jumper settings (SE-1700)

J1 Short (8–9, 10–11, 12–13, 14–15, 16–17, 18–19, and 20–21)
J2 Short (1–2)
J3 Short (1–2)
J4 Short (1–2)
J5 Short (1–2)
J6 Short (1–2)
J7 Short (1–2)
J8 Short (3–5 and 4–6)
J9 Open
J10 Open

(2) PROM mounting

The PROM used is a 2716 device. Programs are written divided into eight high order bits (PROG–HIGH) and eight low order bits (PROG–LOW) mounted to the respective IC26 and IC25 sockets. And the digit PLA (DIG–PLA) is connected to IC5 socket.

Refer to Chapter 5 of the SE-1700 Operation Manual (EEP–1004) for details on PROM writing procedures.

(3) Jumper settings (EV-1709 board)

Short circuit J1 (1–2) to connect the power supply to the LED used to indicate port status on the board. Note that since there is an increase in electrical noise on the board when the LED is on, short-circuiting J1 (2–3) can turn the LED off when an A/D converter is used.

To set the circuit used in initializing (Hi–Z) the PB and PC ports, short-circuit J2 (2–3).

(4) SW1 setting (EV-1709 board)

Set all 4 bits in this switch to the on position.

(5) Rack mounting

The rack used with SE-1700 contains four slots. The SE-1700 and EV-1709 boards may be mounted in any slots.

(6) Connector connections (SE-1700 and EV-1709)

Use the accessory 16-pin flat cable to connect the SE-1700 CN4 connector (16-pin IC socket) to CN2 located in the top left hand corner of EV-1709.

This connection carries PA_0 to PA_3 signals from the CPU board to EV-1709.

(7) Connections to target system

Connections to the target system are made via the following four connectors.

① SE-1700 board CN1 (cable supplied with SE-1700)

1 to 4.	(Not used)
5.	CE (input)
6.	(Not used)
7.	INT (input)
8 to 11.	(Not used)
12 to 16.	GND

② SE-1700 board CN3 (cable supplied with SE-1700)

To emulate the μPD1716 VCOH (FM) input pin, an external prescaler μPB553AC must be connected using the following FM and PSC pins. See Section 4.6 for details on this external driver circuit.

1.	AM (AM VCO input)
2.	GND
3.	FM (FM VCO input)
4.	GND
5.	PSC (output)
6.	GND
7 to 8.	(Not used)
9.	EO_1 (output)
10.	GND
11.	EO_2 (output)
12.	GND

③ SE-1700 CN2 (cable supplied with SE-1700)

1.	GND
2 to 9.	(Not used)
10.	D_2 (output) ..... Used as D_1
11.	D_3 (output) ..... Used as D_2
12.	D_4 (output) ..... Used as D_3
13 to 16.	(Not used)

④ EV-1709 CN1 (cable supplied with EV-1709)

1.	PA_0	(input/output)
2.	PA_1	(input/output)
3.	$PA_2/\overline{SCK}$	(input/output)
4.	PA_3	(input/output)
5.	PB_0	(input/output)
6.	PB_1	(input/output)
7.	PB_2/SO	(input/output)
8.	PB_3/SI	(input/output)
9.	PC_2	(output)
10.	PC_3	(output)
11.	(Not used)	
12 to 14.	GND	
15.	AD_0	(input)
16.	GND	
17 to 34.	(Not used)	

4.5 EXTERNAL DRIVER CIRCUIT

Whereas μPD1709 is equipped with both segment and digit outputs, μPD1716 only has digit outputs. The respective output waveforms differ, and direct connections between EVAKIT-1700/SE-1700 and target systems are not possible in some cases (see Table 4-1).

Although the μPD1709 segment output is N-ch open drain, the EVAKIT-1700 PLA board segment output is only P-ch open drain and CMOS Push-Pull where N-ch open drain cannot be selected.

The SE-1700 segment output, on the other hand, has been designed to permit selection of N-ch open drain.

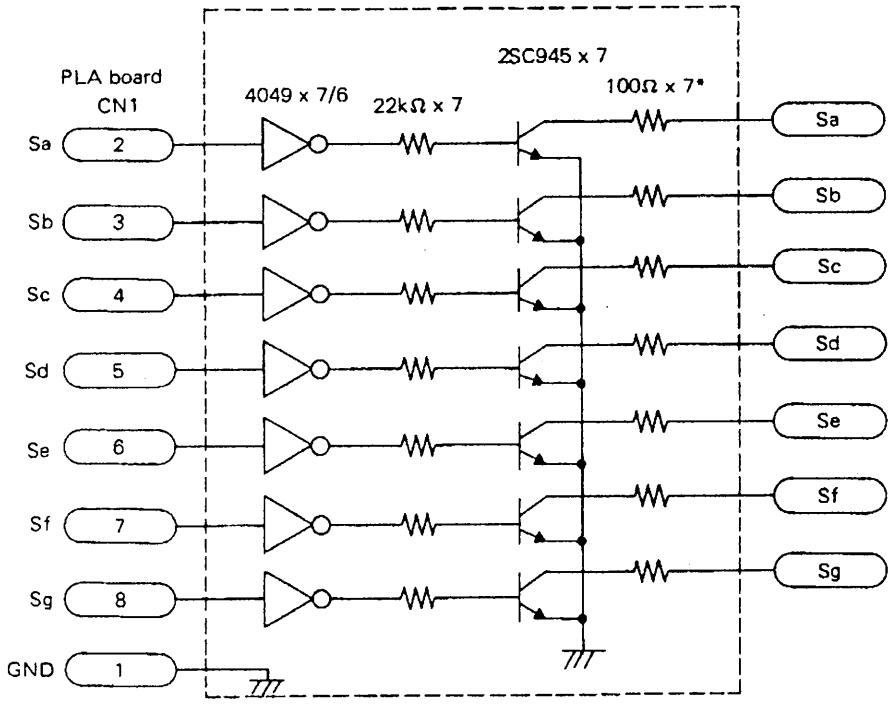
And although the μPD1709 digit output is also N-ch open drain, it cannot be selected on the EVAKIT-1700 PLA board and SE-1700 board.

Although EV-1709 does not require an external driver when used as μPD1716 (see Table 4-1), the driver circuit outlined in Figure 4-1 has to be connected when used as μPD1709.

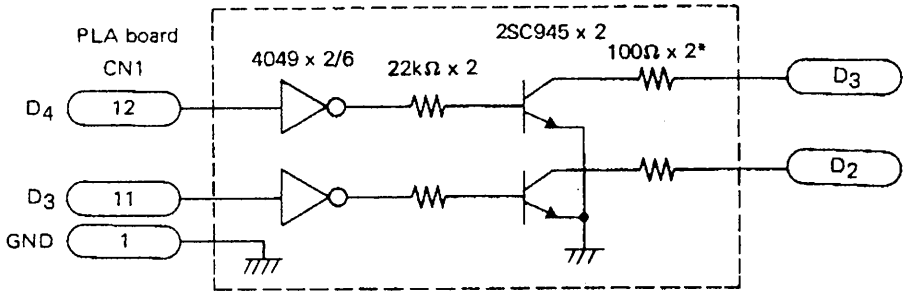
Table 4-1 Target System Direct Connections

	EVAKIT-1700	SE-1700
μPD1709 segment output (N-ch Open)	Not permitted	Permitted
μPD1709 digit output (N-ch Open)	Not permitted	Not permitted
μPD1716 digit output (Push-Pull)	Permitted	Permitted

(1) Segment driver (EV-1709 used as μPD1709 with EVAKIT-1700)



(2) Digit driver (EV-1709 used as μPD1709 with EVAKIT-1700)



(3) Digit driver (EV-1709 used as μPD1709 with SE-1700)

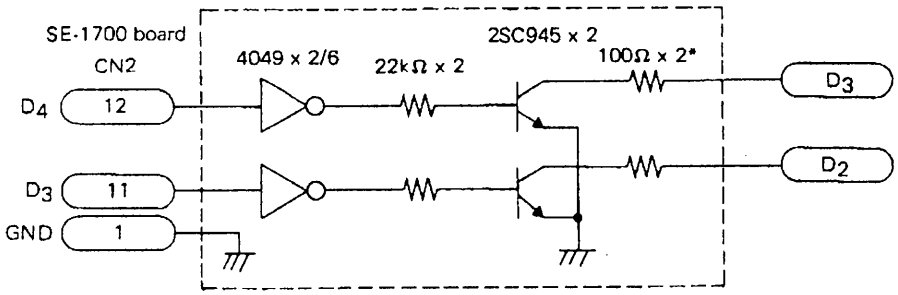


Fig. 4-1 External Driver Circuit (segment/digit)

*The 100 Ω connected to the 2SC945 collector is a current limiter resistance which may not be required with some user circuits.

4.6 EXTERNAL PRESCALER CIRCUIT

The μPB553AC prescaler must be connected externally to emulate the μPD1716 VCOH (FM) input pin. Although the EVAKIT-1700 and SE-1700 boards are equipped with a pin (FM150M) for built-in prescaler devices, this pin cannot be used with μPD1716. Therefore, an external prescaler circuit like that shown in Figure 4-2 must be prepared.

Also note that μPD1716 is not equipped with the HF and VHF instructions used in μPD1708 and μPD1713. If these instructions are executed, the result is equivalent to executing the NOP instruction without effecting EVAKIT-1700 or SE-1700, but without any guarantee of operation on the actual chip. Therefore, in addition to keeping this fact in mind when instructions are entered in batches, also make sure that the HF and VHF instructions have not been used when a mask is ordered.

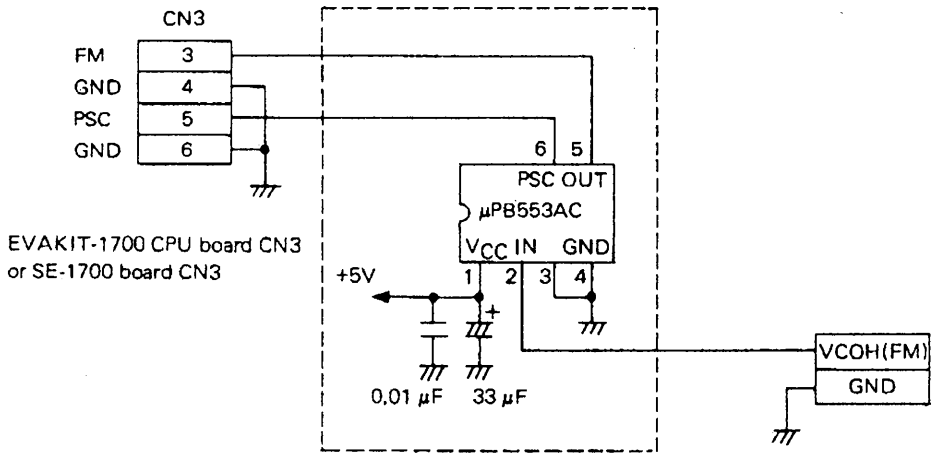


Fig. 4-2 External Prescaler Circuit

4.7 OPERATIONAL PRECAUTIONS

Take careful note of the following precautions when using EV-1709.

(1) EV-1709 is used in combination with EVAKIT-1700 or SE-1700. But because of the 2048-steps ROM and the built-in 256-words RAM, check the source list to ensure that the area being used does not exceed the specified limits. Also note that EV-1709 can be operated by instructions not included in μPD1709 and μPD1716.

(2) SIO instructions cannot be skipped by skip instructions (ADS, AIS, etc). Program operation cannot be guaranteed if these instructions are preceded by a skip instruction. And also make sure that none of these instructions is located at the point of return by RTS instruction.

Although there is no such restriction on the actual chip, it is necessary to keep this fact in mind from the beginning when designing for program evaluation by EV-1709.

(3) The A/D converter consists of a D/A converter (IC5) and comparator (IC4). The resolution and linearity are not exactly the same as in an actual chip. And because of the possible effects of on-board digital noise, evaluate by carefully observing the waveforms of the basic voltage (pin 3) and input voltage (pin 2) of the comparator (IC4) by oscilloscope.

(4) The port and RAM status are initially unstable when the power is switched on. The initialized status of the EVAKIT-1700 and SE-1700 boards vary, and the desired initialized state may be achieved accidently without specific initialization by program. Therefore, since there is a limit to external evaluation, the source list must always be checked.

When evaluating with EVAKIT-1700, note that the RD instruction (Randomize Data) which destroys RAM contents can be used.

(5) Although μPD1709 pin functions are emulated by EVAKIT-1700, SE-1700, and EV-1709, the electrical characteristics differ on each board.

(6) For PLL-related evaluations, carefully observe the VCO output level, frequency, and the degree of distortion, and check that the PLL is properly locked. Note that the PLL can also be locked by higher harmonics even if the divisor value N is incorrectly set by program.

CHAPTER 5. DESCRIPTION OF EV-1709 OPERATION

The μPD1709 functions emulated by the EV-1709 board include PB and PC ports, serial I/O, A/D converter, and CGP output functions. All other functions are handled by EVAKIT-1700 or SE-1700 where the evaluation chip is mounted. EV-1709 operations are outlined below with reference to the circuit diagrams in the Appendix.

5.1 PB AND PC PORTS

PB is a 4-bits input/output port and PC is a 2-bits dedicated N-ch open drain output port with a 2SC945 device used as the driver. These ports are connected to EVAKIT-1700 or SE-1700 via PDATA0–3 of P2. The PDATA0–3 output port addresses are latched according to PALS (Port Address Latch Strobe) timing, and the contents of the output port data on PDATA0–3 are latched according to OTLS (Output Latch Strobe) timing. And when used as an input, the port status is transferred to EVAKIT-1700 or SE-1700 via PDATA0–3 according to $\overline{\text{ADIN}}$ timing.

The PB ports are switched to input mode and the PC ports are all switched to high impedance (Hi–Z) when the EVACHIP is reset by switching the power on, when the R (Reset) command is executed by EVAKIT, and when the clock is stopped.

Since the PB and PC internal output latch status is unstable when the power is switched on, always initialize the ports by program.

5.2 SERIAL I/O

The following three pins are related to serial I/O.

SI	(also used as PB_3) :	Serial data input pin
SO	(also used as PB_2) :	Serial data output pin
$\overline{\text{SCK}}$	(also used as PA_2) :	Shift clock input/output pin

The serial I/O shift register consists of 4035 devices (IC57 and IC58) connected to the PF (IC57) and PE (IC58) internal ports. These shift register outputs are also used as A/D converter data.

When an internal clock is used as the shift clock, use is made of a 15 kHz signal obtained by dividing the $\overline{\text{ADIN}}$ (30 kHz) output signal from the EVAKIT-1700 or SE-1700 EVACHIP by a 4013 device (IC2). When SMR3 is 1, pin 15 of the 4503 device (IC54) is changed to low level, and a 15 kHz clock is passed to the $PA_3/\overline{\text{SCK}}$ pin. If both SMR0 and SMR1 are 1 at this time, the shift register contents are transferred sequentially beginning with the MSB from the PB_2/SO pin synchronized with the clock signal. When 8 pulses of the clock are counted by the 4024 device (IC1), pin 8 of 4011 (IC10) is changed to low level, resulting in suspension of the $\overline{\text{ADIN}}$ input, and automatic stopping of clock generation.

5.3 A/D CONVERTER

The A/D converter consists of the 6-bits μPC603 D/A converter (IC5) and the μPC271 comparator (IC4). The AD input pin is applied directly to pin 2 of the comparator. The 4-bits data PE_3 to PE_0, on the other hand, is passed to the D/A converter (IC5) with the resultant output voltage being applied as a comparison voltage to pin 3 of the comparator (IC4) where it is compared with the input voltage from the AD input pin. The comparator output on pin 7 is low if the AD input voltage is higher than the comparison voltage, and high if lower than that voltage. This comparison result is transferred as the JDG signal (pin 28 of P2) to EVAKIT-1700 or SE-1700 when the TADT or TADF instruction is executed.

The input stage of the μPC603 D/A converter (IC5) includes a data converting device μPD2716 (IC6). Whereas the PE internal port output is "active high", the μPC603 input is "active low". The data is therefore inverted by IC6. The A/D converter also includes 15 data patterns for converter adjustment purposes, the patterns being selected by the 4-bits SW1. Normally, all SW1 bits are switched to the on position.

The A/D converter adjustment procedure is described below. Three variable resistance controls (VR1, VR2,

and VR3) are mounted on the board. (a) First, all SW1 bits are switched OFF to obtain maximum D/A converter (IC5) output voltage (V_{ref}). A voltmeter is connected to TP1 (IC5 output) and adjusted to read 10.0V by turning VR2 (500Ω). (b) The voltmeter is then connected to TP2 (IC4 input) and adjusted to read 5.0V by turning VR1 (100kΩ). (c) VR3 (5MΩ) is used for adjusting linearity, and with the voltmeter still connected to TP2 the SW1 settings are changed to obtain the voltages shown in Table 5-1. Since the V_{ref} adjusted in step (a) is altered when VR3 is adjusted, steps (a) and (c) are repeated until no further adjustment is necessary. Note that all SW1 bits must be in the ON position when the adjustment is completed.

Since precise adjustment of the linearity is very time consuming, run the following program and make the necessary adjustments while observing the TP2 waveform in an oscilloscope. (Simplified adjustment)

```
PORTE   EQU     0
DATA    EQU     00H
LOOP:   BANK1
        OUT     PORTE, DATA
        BANK0
        A1      DATA, 1
        JMP     LOOP
```

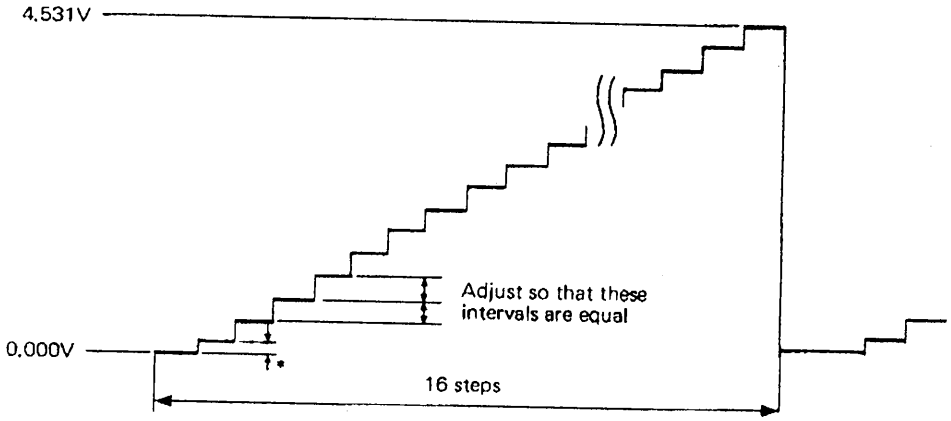


Fig. 5-1 TP2 Oscilloscope Waveform

*The width of the first step only is half the width of the other steps.

Table 5-1 SW1 Settings

(0 = ON 1 = OFF)

SW1 status #3	#2	#1	#0	IC6 output (2716)	TP2 voltage (X V_{ref})	V (V_{ref} = 5V)	
0	0	0	0	Dependent on PE status	←	←	← Normal setting
0	0	0	1	7F	0/16	0.000	← MIN. value
0	0	1	0	7B	0.5/16	0.156	
0	0	1	1	73	1.5/16	0.469	
0	1	0	0	6B	2.5/16	0.781	
0	1	0	1	63	3.5/16	1.094	
0	1	1	0	5B	4.5/16	1.406	
0	1	1	1	53	5.5/16	1.719	
1	0	0	0	4B	6.5/16	2.031	
1	0	0	1	43	7.5/16	2.344	
1	0	1	0	3B	8.5/16	2.656	
1	0	1	1	33	9.5/16	2.969	
1	1	0	0	1B	12.5/16	3.906	
1	1	0	1	13	13.5/16	4.219	
1	1	1	0	0B	14.5/16	4.531	← MAX. value
1	1	1	1	00	16/16	5.000	← V_{ref} value

5.4 CGP OUTPUT

The CGP (Clock Generator Port) is equipped with both VDP (Variable Duty Pulse) generator and SG (Signal Generator) functions, and can be controlled by the PG and PH internal ports. The CGP can exist in four modes which are specified by PG_0 and PG_1.

The CGP circuit employs 4029 (IC7 and IC18) as a presettable down-counter. When in VDP mode, an XOR stage is inserted prior to the preset data input to set the high level and low level intervals. The SG mode reference clock may be either 18kHz or 180kHz, the 18kHz being obtained by dividing the C2 signal (90kHz) by 5 in 4015 (IC43). The 180kHz clock is obtained by ORing the C2 signal (90kHz) with the three signals PALS, SYNC, and OTLS (all 30kHz and all mutually out of phase from each other).

The CGP output is CMOS push-pull with 4049 used as the driver. The CGP output is switched to high level when the EVACHIP is switched power on or reset, when the R (reset) command is executed in the EVAKIT, and when the clock is stopped.

And since the CGP output internal latch (PG and PH) status is unsteady when the power is first switched on, always initialize the output by program.

CHAPTER 6. CONNECTOR PIN TABLES

6.1 CN1 PIN TABLE

Board connector Yamaichi Electronics Co., Ltd. FAP-34-07#2
Cable connector Yamaichi Electronics Co., Ltd. FAS-34-17

No.	Pin name	Input/output	No.	Pin name	Input/output
1	PA_0	Input/output	2	PA_1	Input/output
3	$PA_2/\overline{SCK}$	Input/output	4	PA_3	Input/output
5	PB_0	Input/output	6	PB_1	Input/output
7	PB_2/SO	Input/output	8	PB_3/SI	Input/output
9	PC_2	Output	10	PC_3	Output
11	CGP	Output	12	GND	
13	GND		14	GND	
15	AD	Input	16	GND	
17			18		
19			20		
21			22		
23			24		
25			26		
27			28		
29			30		
31			32		
33			34		

(1) Since GND (16) has been mounted specifically for the A/D converter, it is to be isolated from other ground lines. This analog GND is connected to digital GND at a single point on the EV-1709 board.

(2) Note that driving capacity of the port outputs (PA_0 to PA_3, PB_0 to PB_3, PC_2 to PC_3, and CGP) differs from that on actual chips.

6.2 μPD1709 CORRESPONDENCE TABLE (WHEN EV-1709 IS USED WITH EVAKIT-1700)

μPD1709			EVAKIT-1700		
No.	Pin name	Input/output	Board	Pin No.	Input/output device
1	Sa	Output	PLA	*1	2SC945
2	Sb	Output	PLA	*1	2SC945
3	Sc	Output	PLA	*1	2SC945
4	Sd	Output	PLA	*1	2SC945
5	Se	Output	PLA	*1	2SC945
6	Sf	Output	PLA	*1	2SC945
7	Sg	Output	PLA	*1	2SC945
8	GND				
9	PB_0	Input/output	EV-1709	CN1–5	4503, 4519
10	PB_1	Input/output	EV-1709	CN1–6	4503, 4519
11	PB_2/SO	Input/output	EV-1709	CN1–7	4503, 4519
12	PB_3/SI	Input/output	EV-1709	CN1–8	4503, 4519
13	AD-IN	Input	EV-1709	CN1–15	μPC271
14	V_{DD}				
15	EO	Output	CPU	CN3–9	EVACHIP
16	CE	Input	CPU	CN1–5	EVACHIP
17	XI	Input			
18	XO	Output			
19	$\overline{INT}$	Input	CPU	CN1–7	EVACHIP
20	PSC	Output	CPU	CN3–5	EVACHIP
21	IN	Input	CPU	CN3–3	EVACHIP
22	CGP	Output	EV-1709	CN1–11	4049
23	PC_2	Output	EV-1709	CN1–9	2SC945
24	PC_3	Output	EV-1709	CN1–10	2SC945
25	D_2	Output	PLA	*2	2SC945
26	D_3	Output	PLA	*2	2SC945
27	$PA_2/\overline{SCK}$	Input/output	EV-1709	CN1–3	EVACHIP
28	PA_3	Input/output	EV-1709	CN1–4	EVACHIP

(1) *1 and *2 denote connection via external driver circuit to be added. See Section 4.5 for details.

(2) Since the A/D converter GND has been included specifically for CN1–16, it is to be isolated from other ground lines. This analog GND is connected to other digital GND at a single point on the EV-1709 board.

(3) Other GND connections are to be made to the GND pins in the respective connectors.

6.3 μPD1709 CORRESPONDENCE TABLE (WHEN EV-1709 IS USED WITH SE-1700)

μPD1709			SE-1700		
No.	Pin name	Input/output	Board	Pin no.	Input/output device
1	Sa	Output	SE-1700	CN2–2	2SC945
2	Sb	Output	SE-1700	CN2–3	2SC945
3	Sc	Output	SE-1700	CN2–4	2SC945
4	Sd	Output	SE-1700	CN2–5	2SC945
5	Se	Output	SE-1700	CN2–6	2SC945
6	Sf	Output	SE-1700	CN2–7	2SC945
7	Sg	Output	SE-1700	CN2–8	2SC945
8	GND				
9	PB_0	Input/output	EV-1709	CN1–5	4503, 4519
10	PB_1	Input/output	EV-1709	CN1–6	4503, 4519
11	PB_2/SO	Input/output	EV-1709	CN1–7	4503, 4519
12	PB_3/SI	Input/output	EV-1709	CN1–8	4503, 4519
13	AD-IN	Input	EV-1709	CN1–15	μPC271
14	V_{DD}				
15	EO	Output	SE-1700	CN3–9	EVACHIP
16	CE	Input	SE-1700	CN1–5	EVACHIP
17	XI	Input			
18	XO	Output			
19	$\overline{INT}$	Input	SE-1700	CN1–7	EVACHIP
20	PSC	Output	SE-1700	CN3–5	EVACHIP
21	IN	Input	SE-1700	CN3–3	EVACHIP
22	CGP	Output	EV-1709	CN1–11	4049
23	PC_2	Output	EV-1709	CN1–9	2SC945
24	PC_3	Output	EV-1709	CN1–10	2SC945
25	D_2	Output	SE-1700	*1	2SC945
26	D_3	Output	SE-1700	*1	2SC945
27	$PA_2/\overline{SCK}$	Input/output	EV-1709	CN1–3	EVACHIP
28	PA_3	Input/output	EV-1709	CN1–4	EVACHIP

(1) *1 denotes connection via external driver circuit to be added. See Section 4.5 for details.

(2) Since the A/D converter GND has been included specifically for CN1–16, it is to be isolated from other ground lines. This analog GND is connected to other digital GND at a single point on the EV-1709 board.

(3) Other GND connections are to be made to the GND pins in the respective connectors.

6.4 μPD1716 CORRESPONDENCE TABLE (WHEN EV-1709 IS USED WITH EVAKIT-1700)

μPD1716			EVAKIT-1700		
No.	Pin name	Input/output	Board	Pin no.	Input/output device
1	PA_3	Input/output	EV-1709	CN1–4	EVACHIP
2	$PA_2/\overline{SCK}$	Input/output	EV-1709	CN1–3	EVACHIP
3	PA_1	Input/output	EV-1709	CN1–2	EVACHIP
4	PA_0	Input/output	EV-1709	CN1–1	EVACHIP
5	GND				
6	PB_3/SI	Input/output	EV-1709	CN1–8	4503, 4519
7	PB_2/SO	Input/output	EV-1709	CN1–7	4503, 4519
8	PB_1	Input/output	EV-1709	CN1–6	4503, 4519
9	PB_0	Input/output	EV-1709	CN1–5	4503, 4519
10	GND				
11	A/D	Input	EV-1709	CN1–15	μPC271
12	V_{DD}				
13	$\overline{INT}$	Input	CPU	CN1–7	EVACHIP
14	V_{DD}				
15	CE	Input	CPU	CN1–5	EVACHIP
16	XI	Input			
17	XO	Output			
18	V_{DD}	Output			
19	EO_1	Output	CPU	CN3–9	EVACHIP
20	EO_2	Output	CPU	CN3–11	EVACHIP
21	GND				
22	VCOH (FM)	Input	CPU	*1	μPB553A
23	VCOL (AM)	Input	CPU	CN3–1	EVACHIP
24	D_1	Output	PLA	CN1–9	4050
25	D_2	Output	PLA	CN1–10	4050
26	D_3	Output	PLA	CN1–11	4050
27	PC_2	Output	EV-1709	CN1–9	2SC945
28	PC_3	Output	EV-1709	CN1–10	2SC945

(1) *1 denotes connection via external prescaler circuit to be added. See Section 4.6 for details.

(2) Since the EV-1709 PC_2 and PC_3 outputs are passed out via the 2SC945 open collector, they must be pulled up externally (by about 33kΩ) by +5V.

(3) Since the A/D converter GND has been included specifically for CN1–16, it is to be isolated from other ground lines. This analog GND is connected to other digital GND at a single point on the EV-1709 board.

(4) Other GND connections are to be made to the GND pins in the respective connectors.

6.5 μPD1716 CORRESPONDENCE TABLE (WHEN EV-1709 IS USED WITH SE-1700)

μPD1716			SE-1700		
No.	Pin name	Input/output	Board	Pin no.	Input/output device
1	PA_3	Input/output	EV-1709	CN1–4	EVACHIP
2	$PA_2/\overline{SCK}$	Input/output	EV-1709	CN1–3	EVACHIP
3	PA_1	Input/output	EV-1709	CN1–2	EVACHIP
4	PA_0	Input/output	EV-1709	CN1–1	EVACHIP
5	GND				
6	PB_3/SI	Input/output	EV-1709	CN1–8	4503, 4519
7	PB_2/SO	Input/output	EV-1709	CN1–7	4503, 4519
8	PB_1	Input/output	EV-1709	CN1–6	4503, 4519
9	PB_0	Input/output	EV-1709	CN1–5	4503, 4519
10	GND				
11	A/D	Input	EV-1709	CN1–15	μPC271
12	V_{DD}				
13	$\overline{INT}$	Input	SE-1700	CN1–7	EVACHIP
14	V_{DD}				
15	CE	Input	SE-1700	CN1–5	EVACHIP
16	XI	Input			
17	XO	Output			
18	V_{DD}	Output			
19	EO_1	Output	SE-1700	CN3–9	EVACHIP
20	EO_2	Output	SE-1700	CN3–11	EVACHIP
21	GND				
22	VCOH (FM)	Input	SE-1700	*1	μPB553A
23	VCOL (AM)	Input	SE-1700	CN3–1	EVACHIP
24	D_1	Output	SE-1700	CN2–9	4050
25	D_2	Output	SE-1700	CN2–10	4050
26	D_3	Output	SE-1700	CN2–11	4050
27	PC_2	Output	EV-1709	CN1–9	2SC945
28	PC_3	Output	EV-1709	CN1–10	2SC945

(1) *1 denotes connection via external prescaler circuit to be added. See Section 4.6 for details.

(2) Since the EV-1709 PC_2 and PC_3 outputs are passed out via the 2SC945 open collector, they must be pulled up externally (by about 33kΩ) by +5V.

(3) Since the A/D converter GND has been included specifically for CN1–16, it is to be isolated from other ground lines. This analog GND is connected to other digital GND at a single point on the EV-1709 board.

(4) Other GND connections are to be made to the GND pins in the respective connectors.

APPENDIX I P1 AND P2 PIN TABLES

P1 pin table

	P1 (component mounting side)			P1 (soldering side)		
1	1	GND		2	GND	
2	3	+5V		4	+5V	
3	5	+5V		6	+5V	
4	7	+12V		8	+12V	
5	9			10		
6	11	GND		12	GND	
7	13	BCLK	*	14	$\overline{\text{INIT}}$	*
8	15	BPRN	*	16	$\overline{\text{BPRO}}$	*
9	17	$\overline{\text{BUSY}}$	*	18	$\overline{\text{BREQ}}$	*
10	19	$\overline{\text{MEMR}}$	*	20	$\overline{\text{MWTC}}$	*
11	21	$\overline{\text{IOR}}$	*	22	$\overline{\text{IOWC}}$	*
12	23	$\overline{\text{XACK}}$	*	24	$\overline{\text{INH1}}$	*
13	25			26	$\overline{\text{INH2}}$	*
14	27	$\overline{\text{BHEN}}$	*	28	$\overline{\text{AD10}}$	*
15	29	$\overline{\text{CBRQ}}$	*	30	$\overline{\text{AD11}}$	*
16	31	$\overline{\text{CCLK}}$	*	32	$\overline{\text{AD12}}$	*
17	33	$\overline{\text{INTA}}$	*	34	$\overline{\text{AD13}}$	*
18	35	$\overline{\text{INT6}}$	*	36	$\overline{\text{INT7}}$	*
19	37	$\overline{\text{INT4}}$	*	38	$\overline{\text{INT5}}$	*
20	39	$\overline{\text{INT2}}$	*	40	$\overline{\text{INT3}}$	*
21	41	$\overline{\text{INT0}}$	*	42	$\overline{\text{INT1}}$	*
22	43	$\overline{\text{ADRE}}$	*	44	$\overline{\text{ADRF}}$	*
23	45	$\overline{\text{ADRC}}$	*	46	$\overline{\text{ADRD}}$	*
24	47	$\overline{\text{ADRA}}$	*	48	$\overline{\text{ADRB}}$	*
25	49	$\overline{\text{ADR8}}$	*	50	$\overline{\text{ADR9}}$	*
26	51	$\overline{\text{ADR6}}$	*	52	$\overline{\text{ADR7}}$	*
27	53	$\overline{\text{ADR4}}$	*	54	$\overline{\text{ADR5}}$	*
28	55	$\overline{\text{ADR2}}$	*	56	$\overline{\text{ADR3}}$	*
29	57	$\overline{\text{ADR0}}$	*	58	$\overline{\text{ADR1}}$	*
30	59			60		
31	61			62		
32	63			64		
33	65			66		
34	67	$\overline{\text{DB6}}$	*	68	$\overline{\text{DB7}}$	*
35	69	$\overline{\text{DB4}}$	*	70	$\overline{\text{DB5}}$	*
36	71	$\overline{\text{DB2}}$	*	72	$\overline{\text{DB3}}$	*
37	73	$\overline{\text{DB0}}$	*	74	$\overline{\text{DB1}}$	*
38	75	GND		76	GND	
39	77			78		
40	79	−12V	*	80	−12V	*
41	81	+5V		82	+5V	
42	83	+5V		84	+5V	
43	85	GND		86	GND	

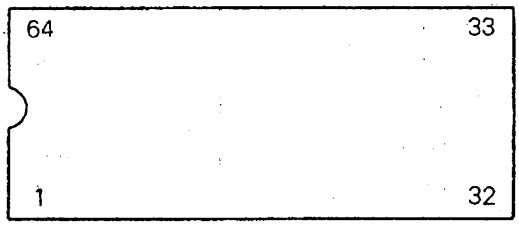
Note: Signals marked by an asterisk are not used by EV-1709.

P2 pin table

	P2 (component mounting side)		P2 (soldering side)	
1	1	GND	2	GND
2	3	MS0	4	MS1
3	5	MS2	6	MS3
4	7	C2 (φ2)	8	$\overline{\text{ADIN}}$ (M2)
5	9	PALS (M1·φ1)	10	PDATA0
6	11	PDATA1	12	PDATA2
7	13	PDATA3	14	STLS (M1·φ2)
8	15	OTLS (M3·φ1)	16	SGLS (M3·φ1)
9	17	SEGCUT *	18	SEGSEL2 *
10	19	SEGSEL3 *	20	SYNC (M2·φ1)
11	21	GND (analog)	22	GND (analog)
12	23	+15V	24	+15V
13	25	−15V	26	−15V
14	27	$\overline{\text{LCD}}$ *	28	JDG
15	29	$\overline{\text{EVARES}}$	30	AD0
16	31	AD1	32	AD2
17	33	AD3	34	AD4 *
18	35	AD5 *	36	AD6 *
19	37	AD7 *	38	AD8 *
20	39	AD9 *	40	AD10 *
21	41	AD11 *	42	AD12 *
22	43	AD13 *	44	AD14 *
23	45	AD15 *	46	MO0
24	47	MO1	48	MO2
25	49	MO3	50	DIG0 *
26	51	DIG1 *	52	DIG2 *
27	53	DIG3 *	54	DIGCUT *
28	55	LCDG0 *	56	LCDG1 *
29	57	LCDG2 *	58	LCDG3 *
30	59	$\overline{\text{BRKACK}}$	60	CE *

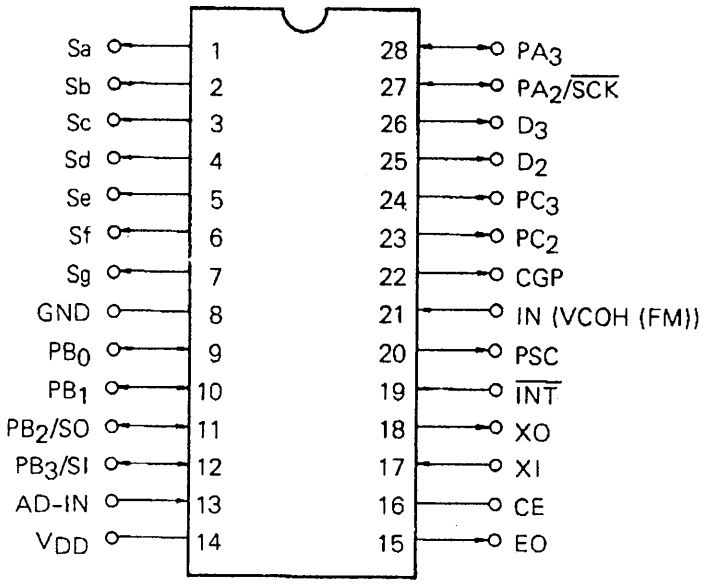
Note: Since the P2 bus is specifically for use by EV-1709, it is not compatible with the IEEE 796 bus.
Signals marked by an asterisk are not used by EV-1709.

APPENDIX II μPD1700B PIN CONNECTION DIAGRAM

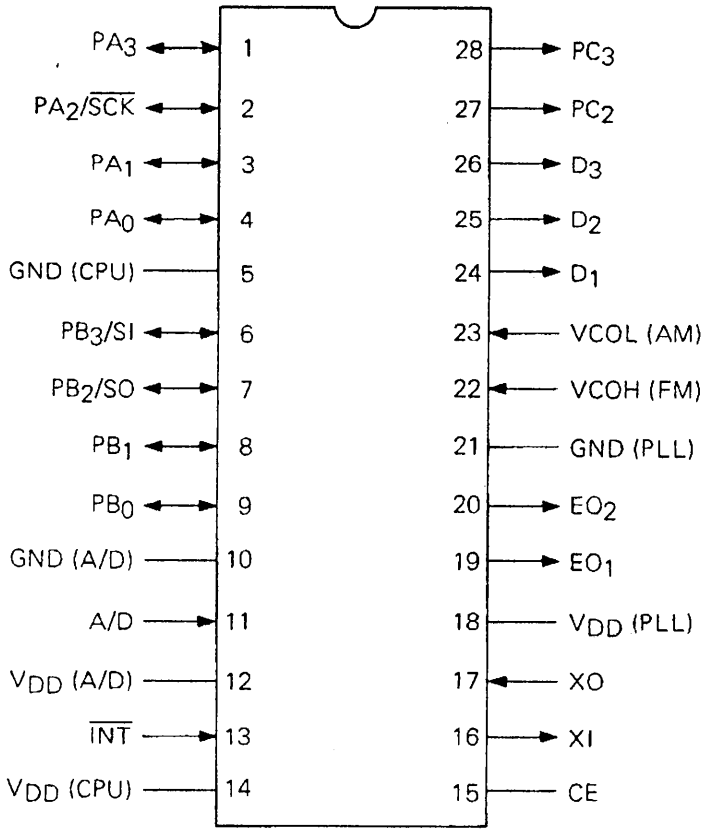


Pin no.	Pin name	I/O	Pin no.	Pin name	I/O
1	CE	I	33	GND	
2	SD	I	34	$PDATA_3$	I/O
3	$\overline{INT}$	I	35	$PDATA_2$	I/O
4	DIG CUT	O	36	$PDATA_1$	I/O
5	DIG_3	O	37	$PDATA_0$	I/O
6	DIG_2	O	38	PALS	O
7	DIG_1	O	39	STLS	O
8	DIG_0	O	40	OTLS	O
9	K_3	I	41	PA_3	I/O
10	K_2	I	42	PA_2	I/O
11	K_1	I	43	PA_1	I/O
12	K_0	I	44	PA_0	I/O
13	BRKACK	O	45	$SEGSEL_2$	O
14	RWE	O	46	$SEGSEL_3$	O
15	SYNC	O	47	SGLS	O
16	C_2	O	48	SEG CUT	O
17	$\overline{ADIN}$	O	49	AD_0	I/O
18	STACK3/$\overline{1}$	I	50	AD_1	I/O
19	RAMR/$\overline{W}$	I	51	AD_2	I/O
20	RUN/$\overline{BRK}$	I	52	AD_3	I/O
21	$\overline{RES}$	I	53	AD_4	I/O
22	CKSEL	I	54	AD_5	I/O
23	DEVSEL	I	55	AD_6	I/O
24	f_V	O	56	AD_7	I/O
25	X_1	I	57	AD_8	I/O
26	X_0	O	58	AD_9	I/O
27	PSC	O	59	AD_{10}	I/O
28	FM	I	60	AD_{11}	I/O
29	AM	I	61	AD_{12}	I/O
30	EO_1	O	62	AD_{13}	I/O
31	EO_2	O	63	AD_{14}	I/O
32	V_{DD}		64	AD_{15}	I/O

APPENDIX III μPD1709 PIN CONNECTION DIAGRAM



APPENDIX IV μPD1716 PIN CONNECTION DIAGRAM



APPENDIX V μPD1709 INSTRUCTION SET

b_{13} b_{12} b_{11} b_{10} \ b_{15} b_{14}		00	01	10	11
		0	1	2	3
0 0 0 0	0	NOP SIO N	———	DIG r	ST M, r
0 0 0 1	1	SPB P, N SS N_1 BANK1 EI STC	ORI M, I	SEG D_H, r	MVRS M, r
0 0 1 0	2	JMP ADDR (page 1)	MVI M, I	OUT P, r	IN r, P
0 0 1 1	3	PPB P, N RS N_1 BANK0 DI RSC	ANI M, I	CKSTP	MVRD r, M
0 1 0 0	4	RT	AI M, I	MVSR M_1, M_2	AD r, M
0 1 0 1	5	RTS	SI M, I	EXL r, M	SU r, M
0 1 1 0	6	JMP ADDR (page 0)	AIC M, I	LD r, M	AC r, M
0 1 1 1	7	CAL ADDR (page 0)	SIB M, I	———	SB r, M
1 0 0 0	8	SBK0 TPF P, N TSF N_2 TCEF TITF	AIN M, I	TSET TSEF TADT TADF	ADN r, M
1 0 0 1	9	SBK1 TPT P, N TST N_2 TCET TITT	SIN M, I	TTM TIP	SUN r, M
1 0 1 0	A	TMF M, N	AICN M, I	TUL	ACN r, M
1 0 1 1	B	TMT M, N	SIBN M, I	PLL M, r	SBN r, M
1 1 0 0	C	SLTI M, I	AIS M, I	SLT r, M	ADS r, M
1 1 0 1	D	SGEI M, I	SIS M, I	SGE r, M	SUS r, M
1 1 1 0	E	SEQI M, I	AICS M, I	SEQ r, M	ACS r, M
1 1 1 1	F	SNEI M, I	SIBS M, I	SNE r, M	SBS r, M

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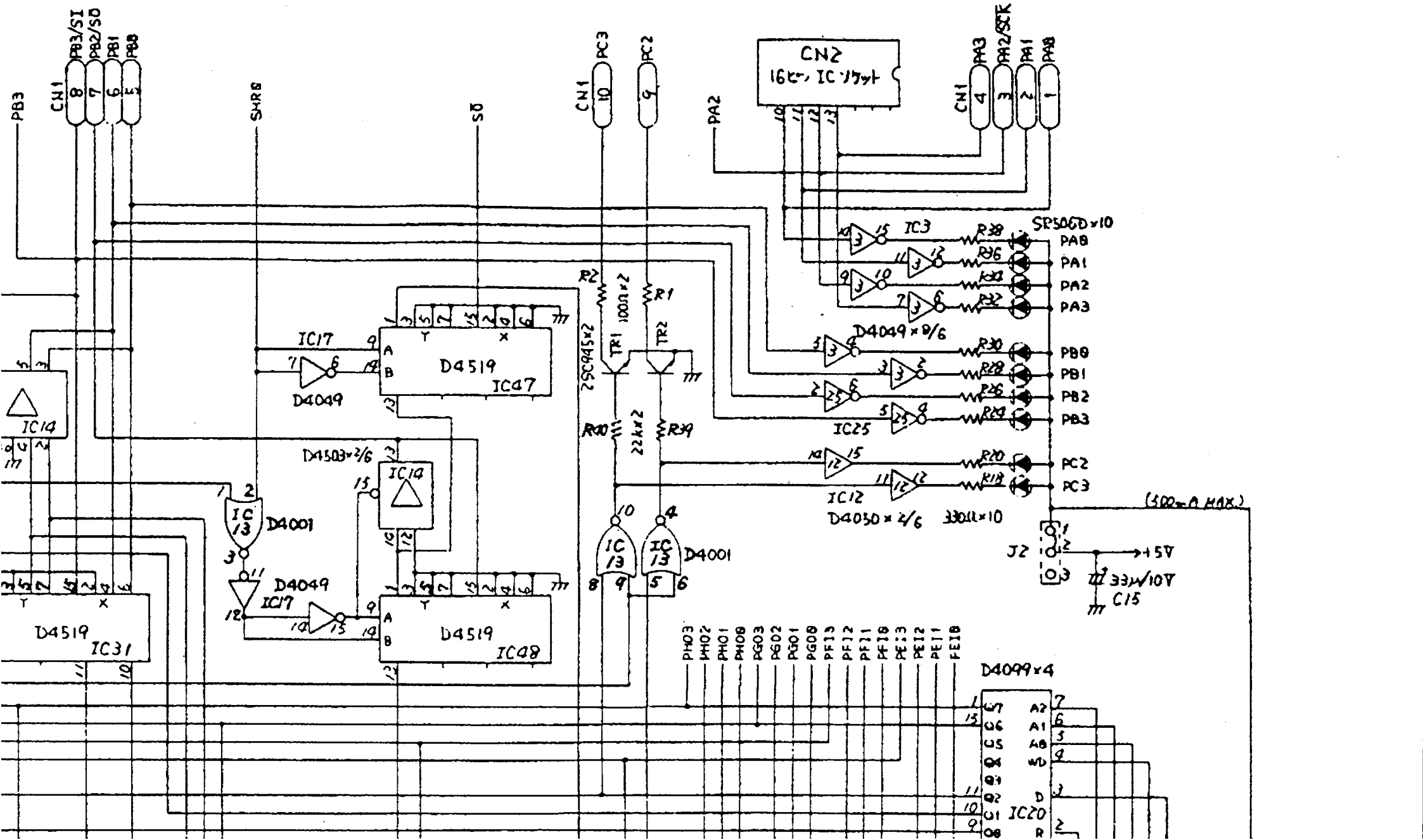

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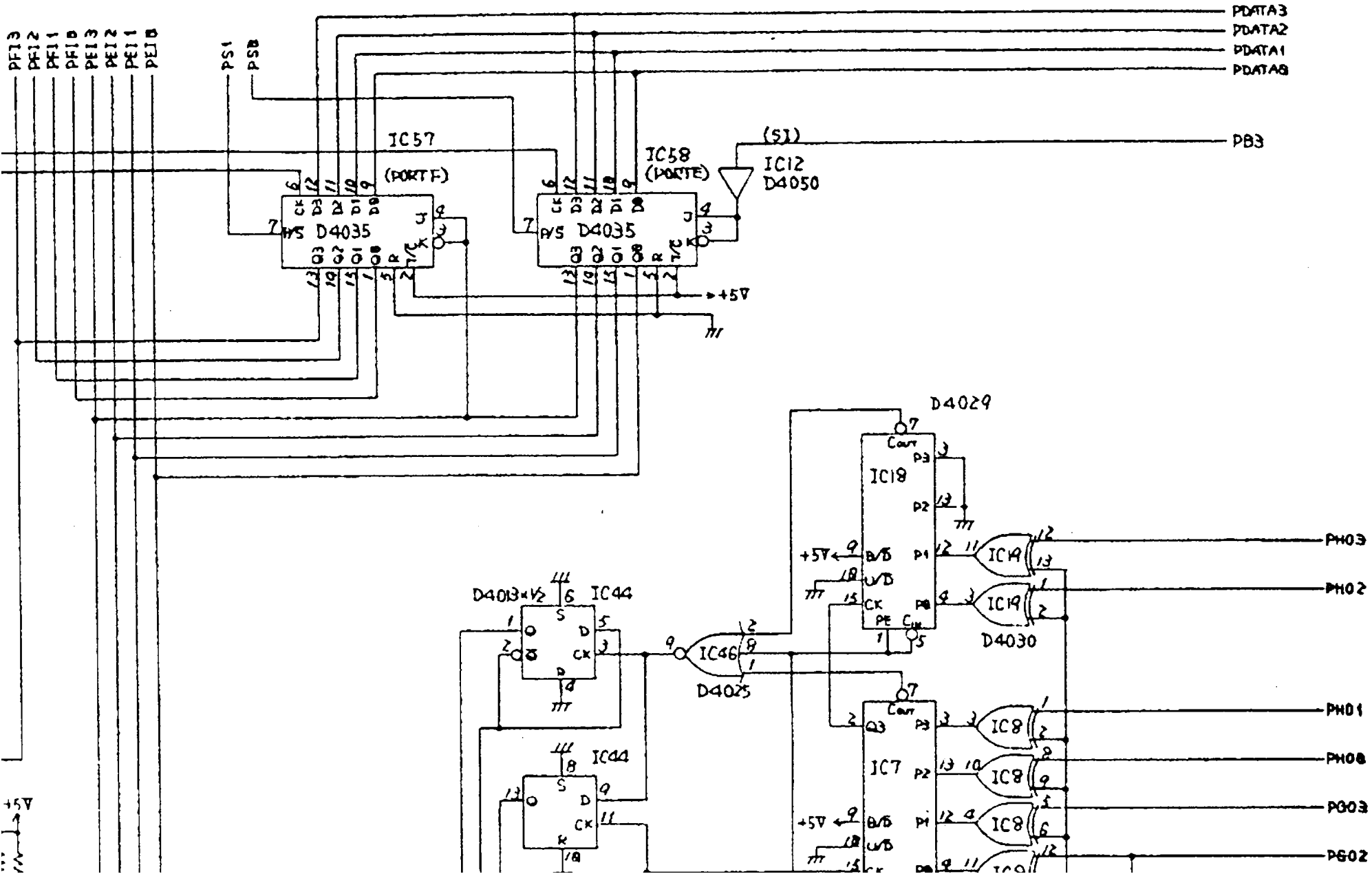
Phase-out/Discontinued



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