User Manual

DA7280 Daughterboard 359-06-X

UM-HA-003

Abstract

This document describes the functionality of DA7280 haptic driver daughterboard. This board can be used standalone or attached to a DA728X motherboard for evaluation.

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Tables

1   Terms and Definitions

NOTE: "X" can denote different version of boards such as A and B variants

359-05-x	DA728x Motherboard, containing LRA as well as the digital and analogue accelerometer circuitry
359-06-x	DA7280 Daughterboard
359-07-x	DA7281 Daughterboard
359-08-x	DA7282 Daughterboard
359-09-x	DA7283 Daughterboard
DA7280	Dialog Semiconductor's haptic driver integrated circuit
DA7281	DA7280 variant with I2C address select
DA7282	DA7280 variant with ultra-low power shutdown
DA7283	DA7280 variant without I2C control and with ultra-low power shutdown
DUT	Device under test
ERM	Eccentric Rotating Mass
GUI	Graphical User Interface
I²C	Inter-Integrated Circuit Communication Standard
LRA	Linear Resonant Actuator
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
BEMF	Back Electro-Motive Force
GPI	General purpose input
PCB	Printed circuit board
DCDC	Direct current to direct current convertor
IRQ	Interrupt request

2   References

[1]   DA7280, Datasheet, Dialog Semiconductor.

[2]   DA7281, Datasheet, Dialog Semiconductor.

[3]   DA7282, Datasheet, Dialog Semiconductor.

[4]   DA7283, Datasheet, Dialog Semiconductor.

[5]   UM-HA-003, DA7280 Daughterboard User Manual, User Manual, Dialog Semiconductor.

[6]   UM-HA-004, DA7281 Daughterboard User Manual, User Manual, Dialog Semiconductor.

[7]   UM-HA-005, DA7282 Daughterboard User Manual, User Manual, Dialog Semiconductor.

[8]   UM-HA-006, DA7283 Daughterboard User Manual, User Manual, Dialog Semiconductor.

[9]   DA728x GUI software

[10]   UM-HA-001, DA728x Motherboard 359-05-A User Manual, User Manual, Dialog Semiconductor.

[11]   UM-HA-002, DA728x Generating LRA configuration script

3   Introduction

This document describes the use and connections of 359-06-X DA7280 daughterboard to allow evaluation of the DA7280 device. A layout is shown in Figure 1 and details of all jumper connections are listed in Table 1.

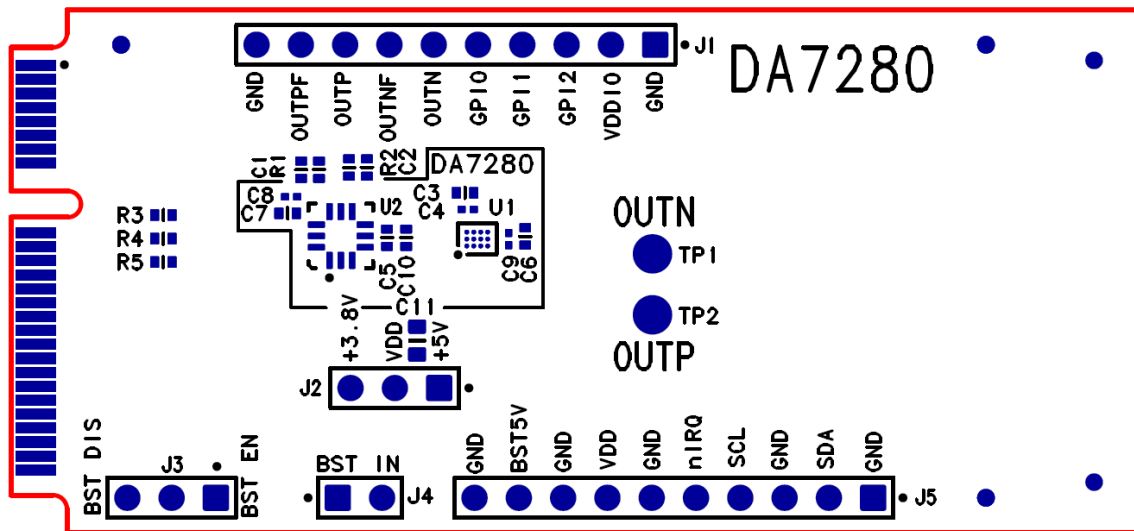# 4   359-06-X PCB Layout and Connections

Figure 1: 359-06-X PCB

DA7280 Daughterboard 359-06-X

Table 1: Jumper Connections and Descriptions

Jumper/ Test Point	Pin/Connection	Description
J1	GND	Ground connection
	VDDIO	VDDIO supply for digital logic Supply range = 1.35 V to 5.5 V, 1.8 V typical
	GPI2	General purpose input pin 2
	GPI1	General purpose input pin 1
	GPI0	General purpose input pin 0
	OUTN	Negative output for LRA connection - TP1 can also be used
	OUTNF	Filtered version of negative output Bandwidth limited to 3.38 kHz for output waveform analysis via an oscilloscope
	OUTP	Positive output for LRA connection - TP2 can also be used
	OUTPF	Filtered version of positive output Bandwidth limited to 3.38 kHz for output waveform analysis via an oscilloscope
	GND	Ground connection
J2	SHORT 1 to 2 (default)	Selects VDD supply to device to be from the boost output at 5 V
	SHORT 2 to 3	Selects VDD supply to device to be from J5-VDD or J4-pin 2
J3	SHORT 1 to 2 (default)	Selects on board boost DCDC to be enabled
	SHORT 2 to 3	Selects on board boost DCDC to be disabled
J4	SHORT (default)	Selects on board boost DCDC input supply to be driven from main motherboard (3V8) when the daughter board is inserted
	OPEN	Removes power to the on-board DCDC from motherboard Pin 1 can be used for direct supply of the DCDC if standalone operation is required
J5	GND	Ground connection
	SDA	I2C Data line, pullup (R3) fitted with a 2K2 resistor as default
	GND	Ground connection
	SCL	I2C Clock line, pullup (R4) fitted with a 2K2 resistor as default
	nIRQ	Interrupt request output, 5K6 (R5) pullup fitted, driven low when IRQ triggered
	GND	Ground connection
	VDD	VDD supply line to device Supply range = 2.8 V to 5.5 V input
	GND	Ground connection
	BST5V	On board DCDC output voltage for monitoring, set to 5V as default
	GND	Ground connection

Jumper/ Test Point	Pin/Connection	Description
TP1	TP1	Test point for OUTN
TP2	TP2	Test point for OUTP

5 Board Setup for VDD Supply to Device

5.1 Standalone Operation
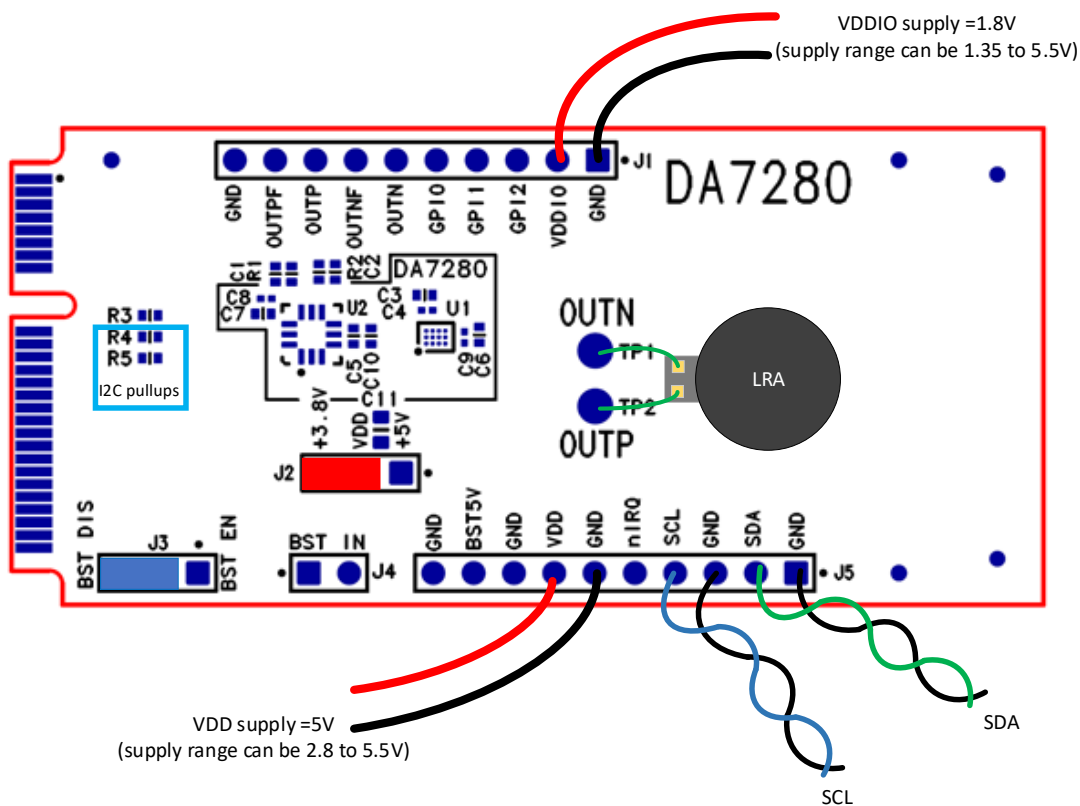
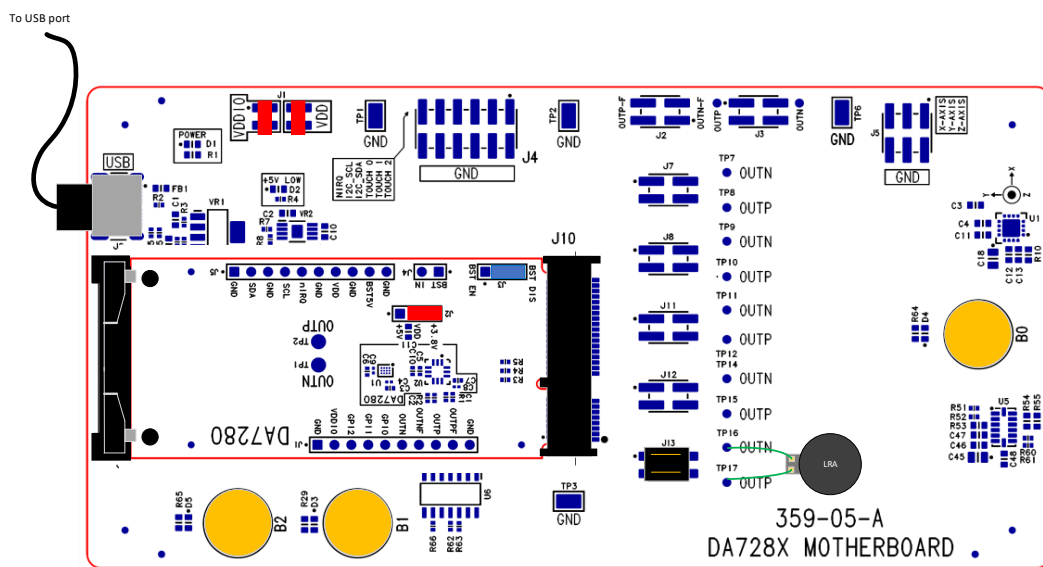**Figure 2: Standalone Operation from VDD Supply**

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5.2   Motherboard Setup

Figure 3: Motherboard Operation with VDD Supply

6 Board Setup for BOOST Supply to Device

6.1 Standalone Operation

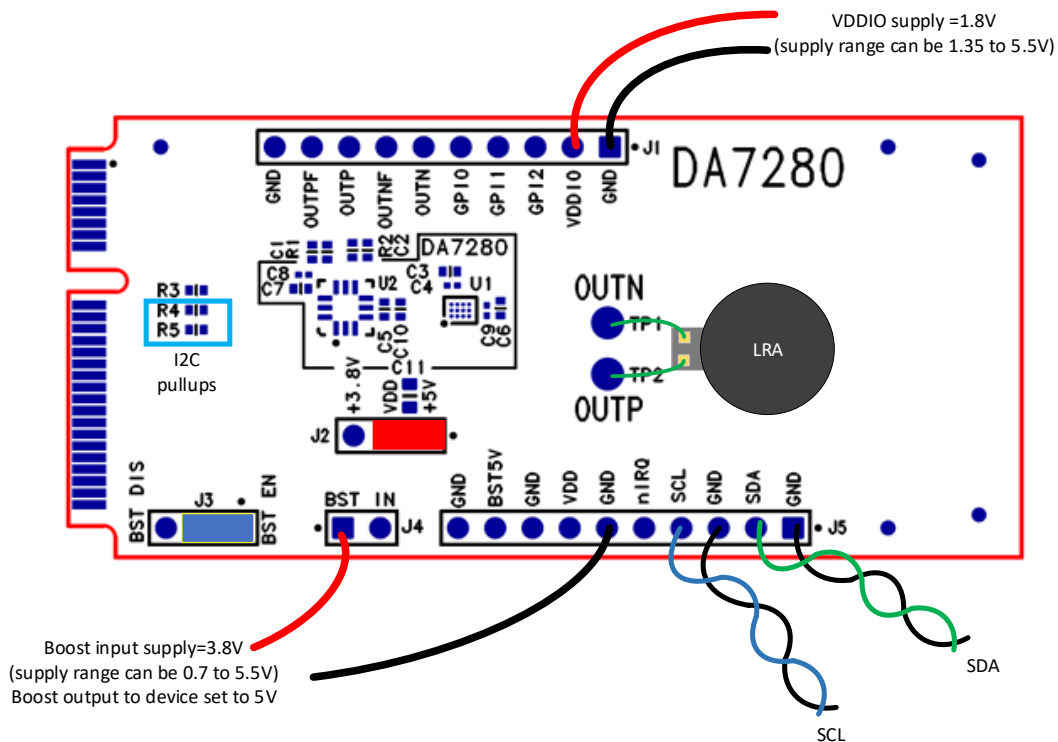**Figure 4: Standalone Operation from BOOST Supply**

6.2 Motherboard Setup

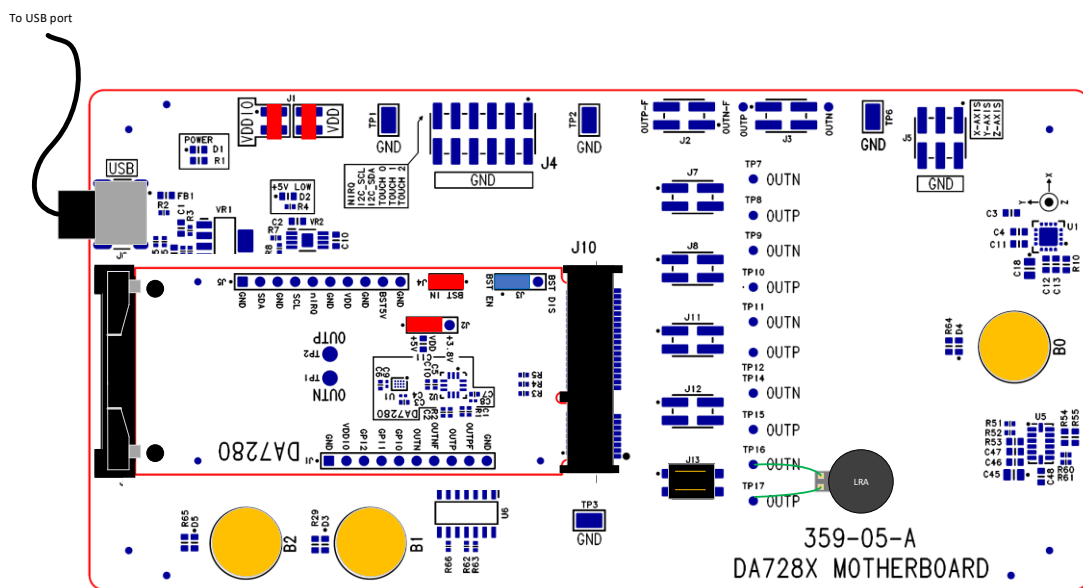**Figure 5: Motherboard Operation from BOOST Supply**

7 359-06-X Schematic

Figure 6: 359-06-X Schematic

8   359-06-X Layout
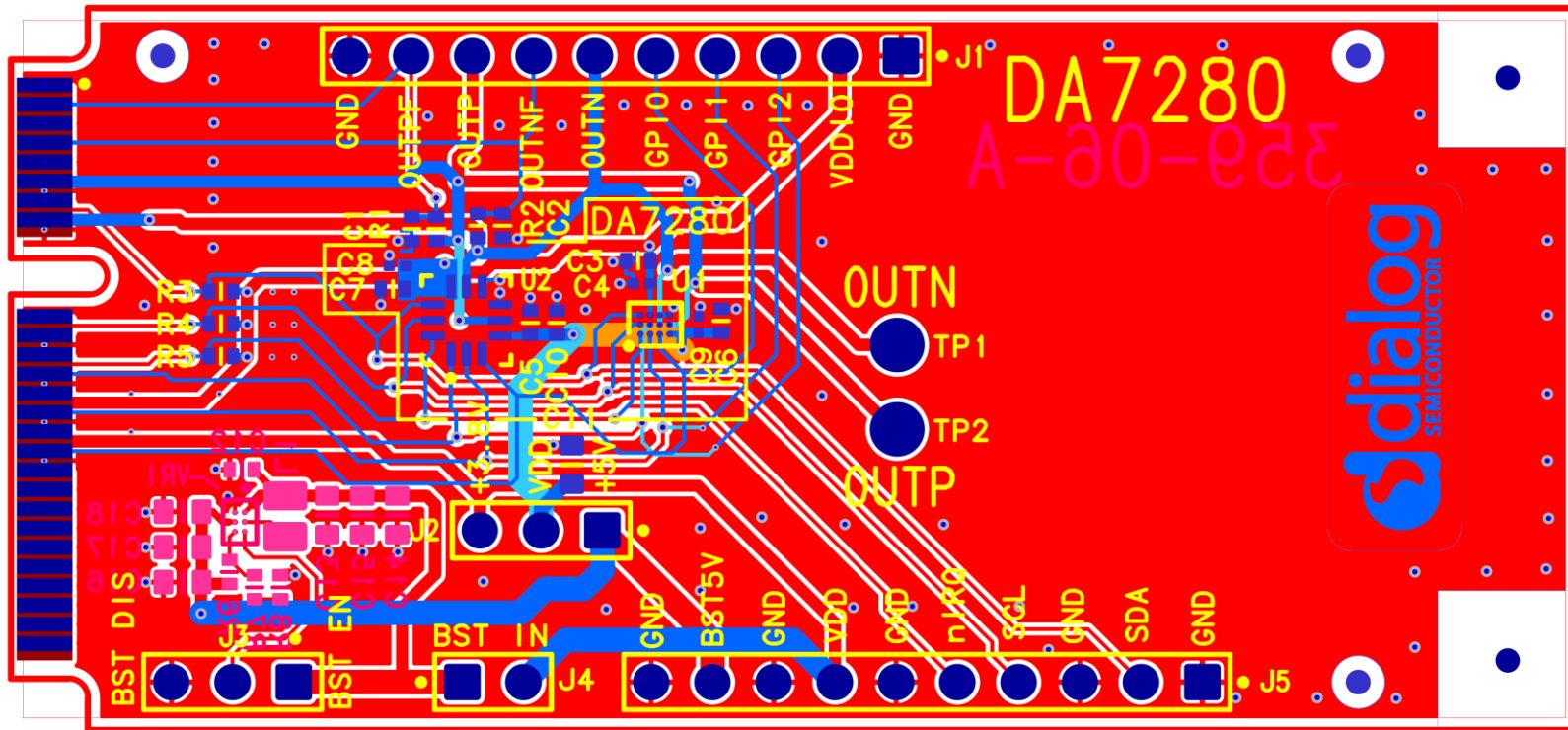
Figure 7: 359-06-X Composite View

DA7280 Daughterboard 359-06-X
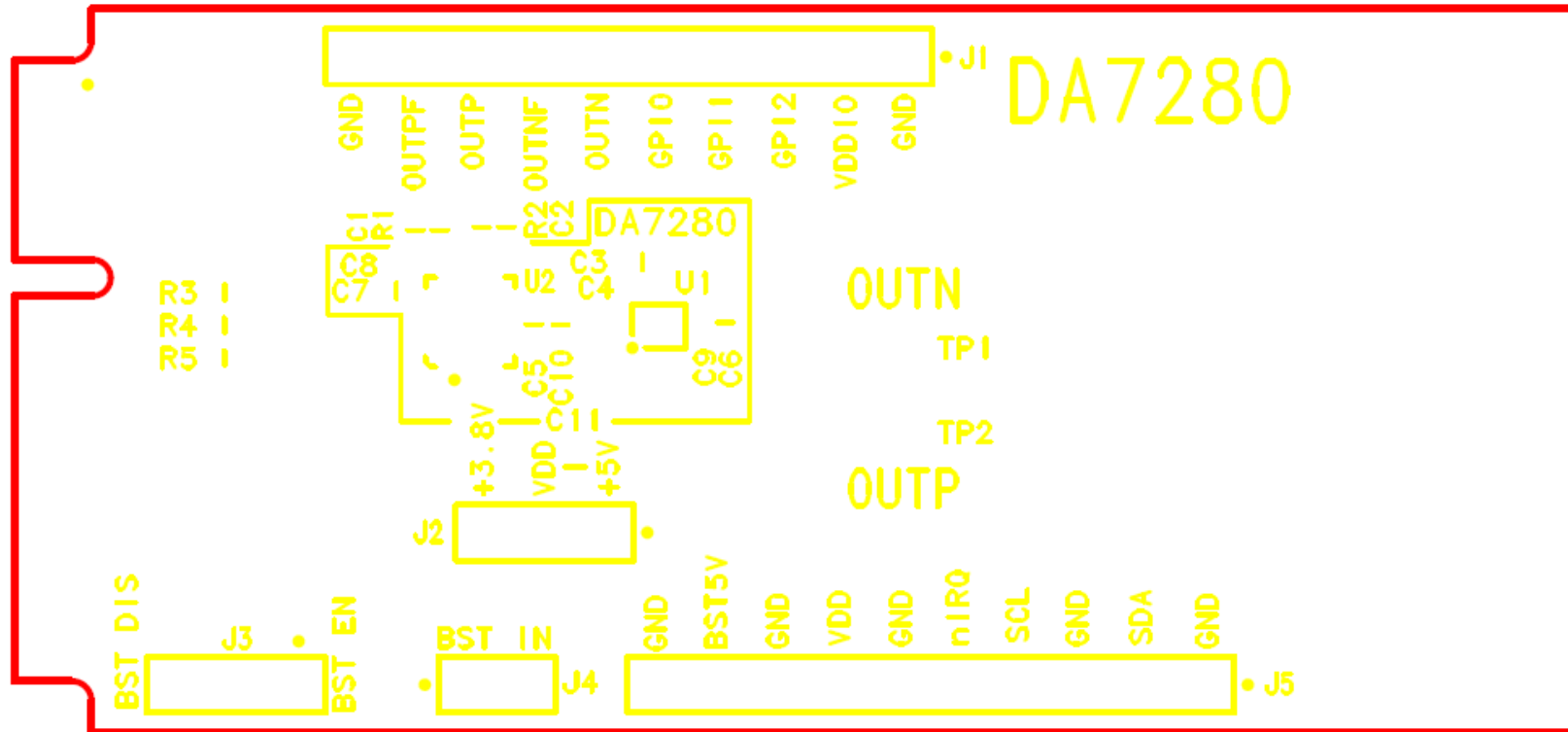
Figure 8: 359-06-X Top Layer Silkscreen

DA7280 Daughterboard 359-06-X
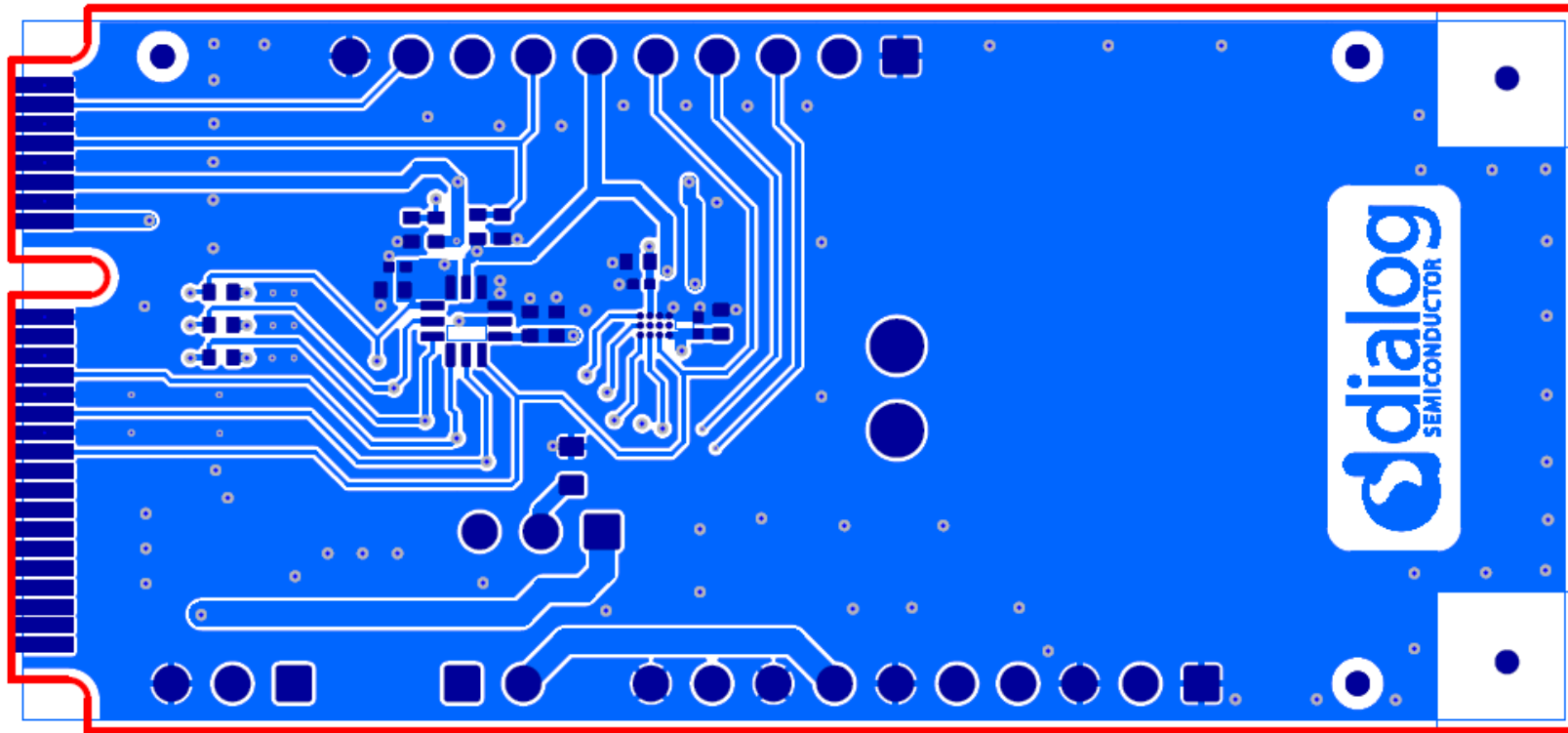
Figure 9: 359-06-X Top Layer Routing

DA7280 Daughterboard 359-06-X
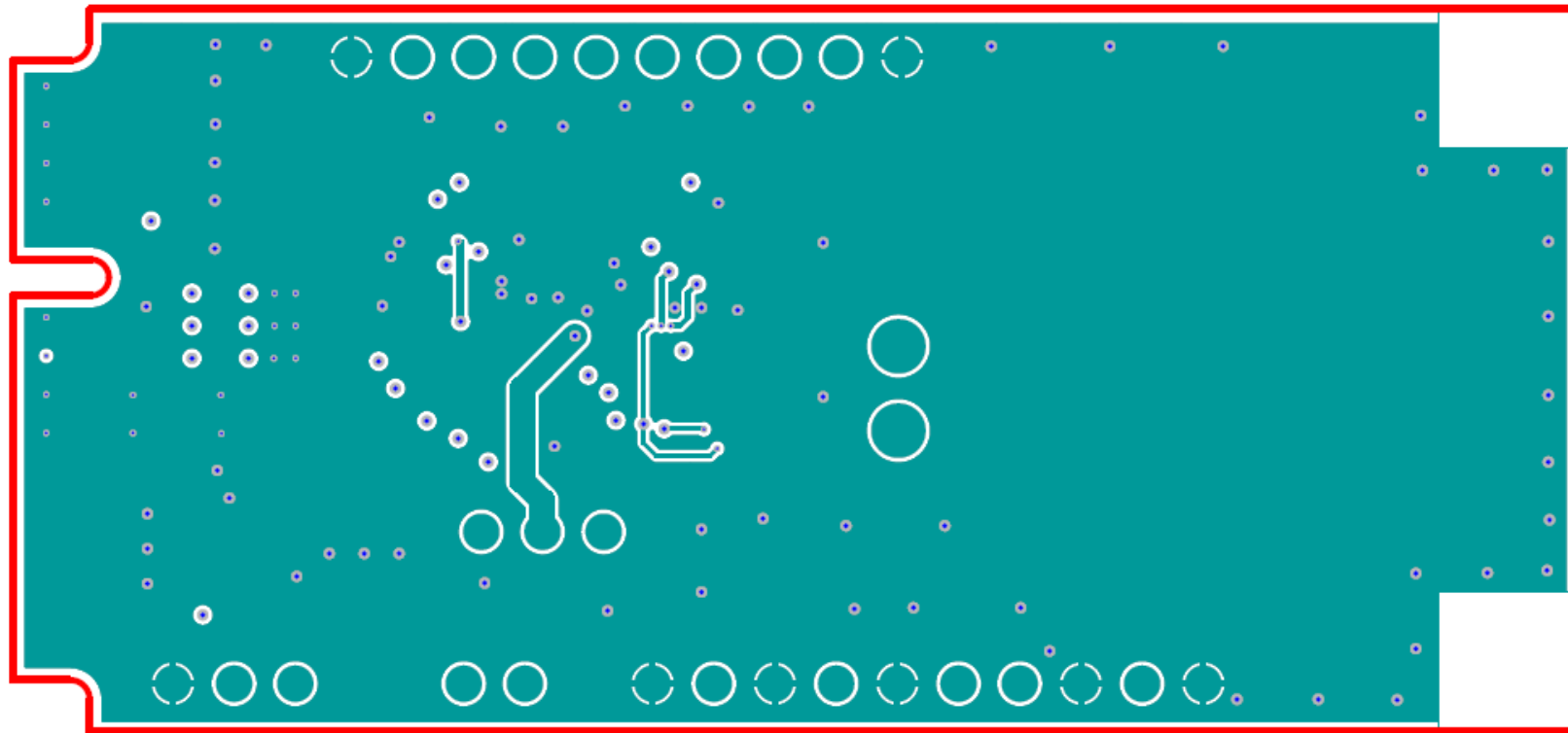
Figure 10: 359-06-X Inner Layer 2

DA7280 Daughterboard 359-06-X

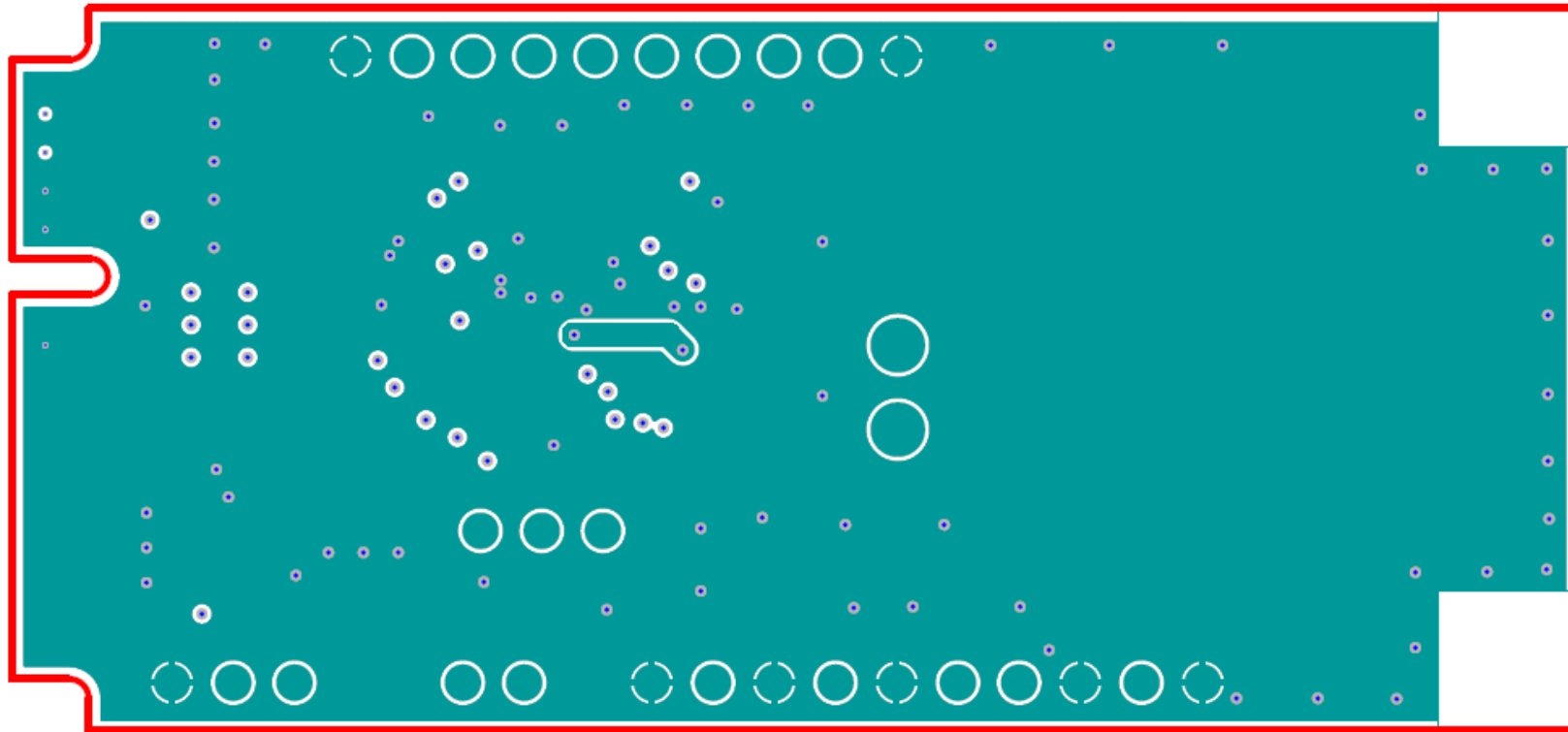
Figure 11: 359-06-X Inner Layer 3
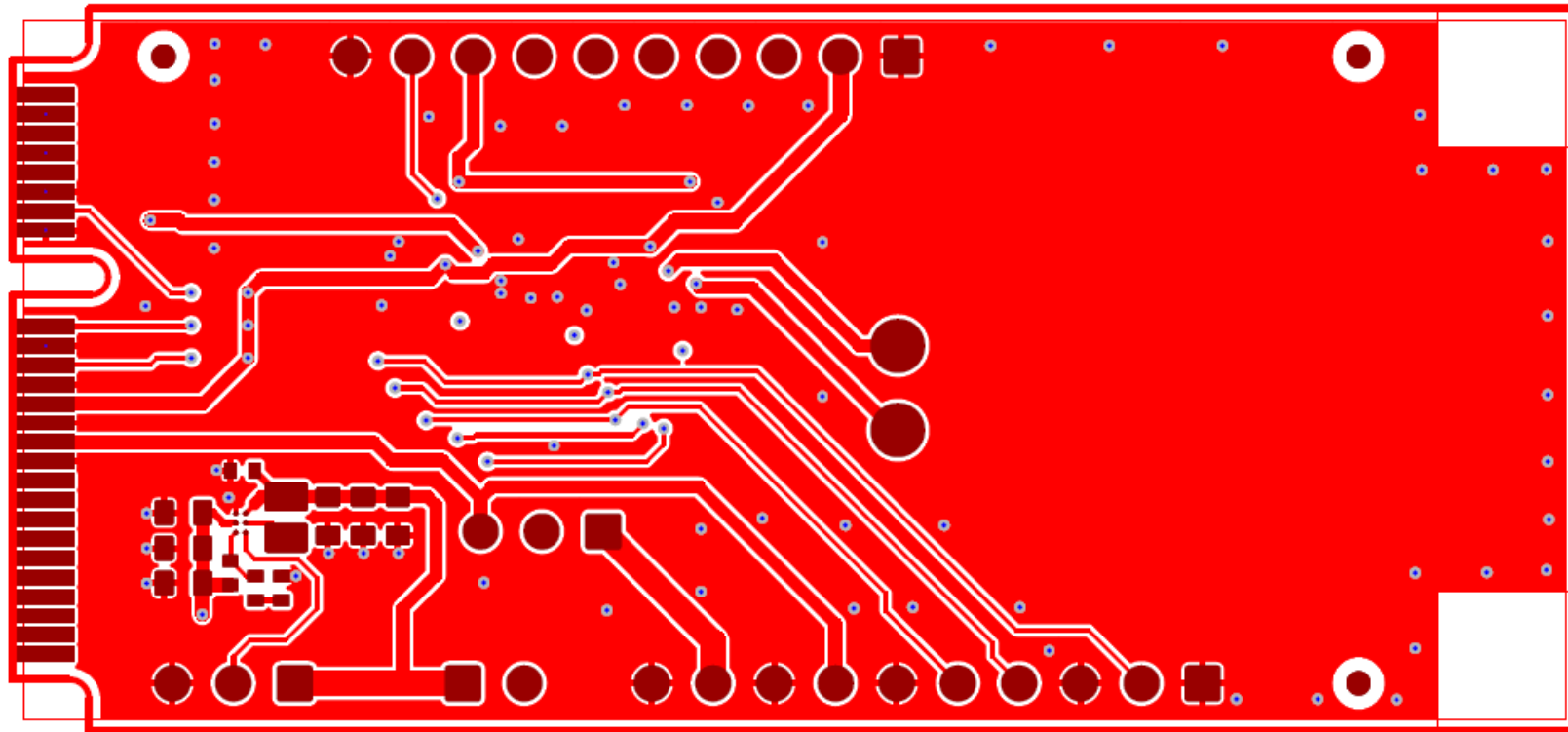
DA7280 Daughterboard 359-06-X

Figure 12: 359-06-X Bottom Layer Routing
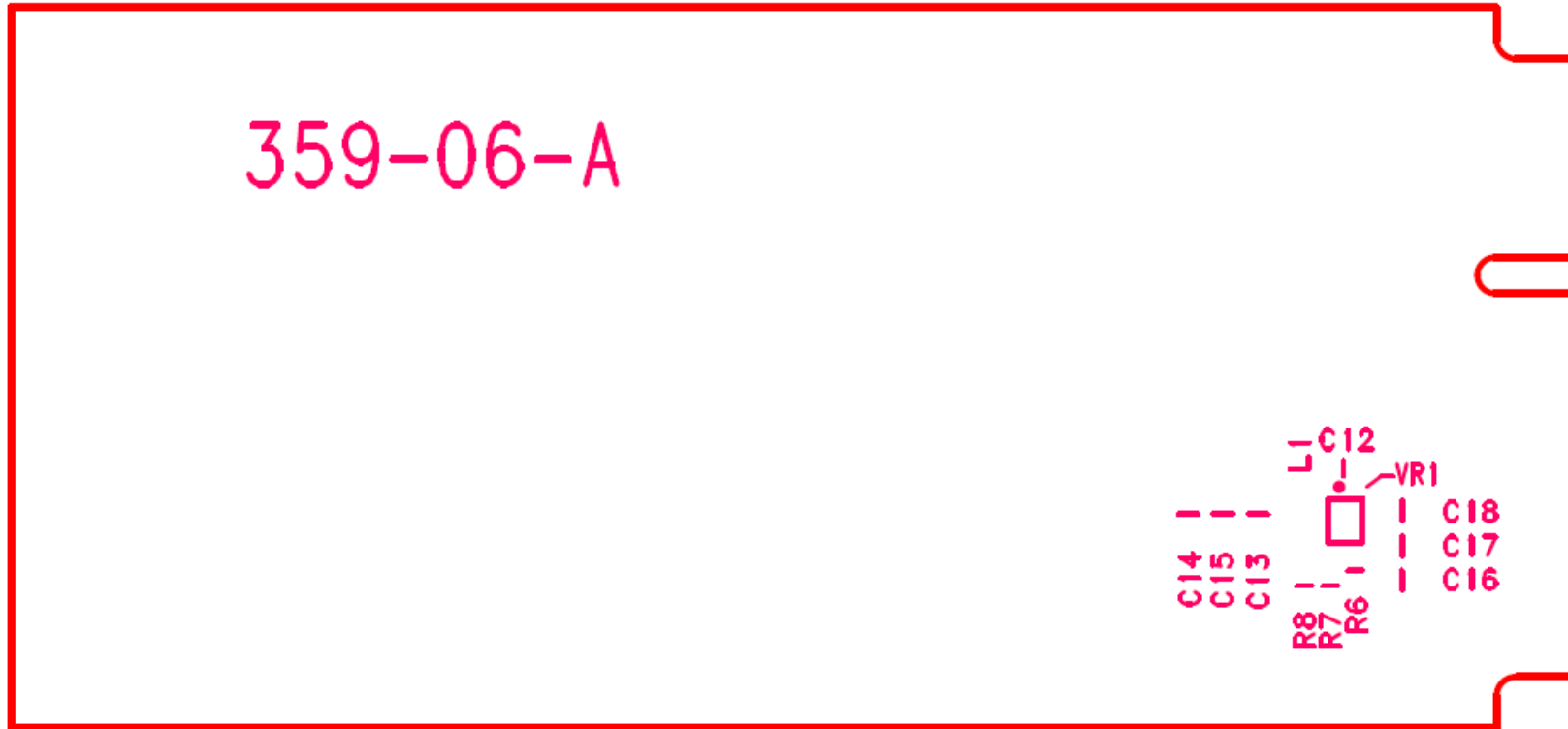
Figure 13: 359-06-X Bottom Layer Silkscreen

Revision History

Revision	Date	Description
1.1	08-Jun-2022	Rebranded to Renesas.
1.0	15-Apr-2020	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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