User Manual

DA1468x Development Kit - Basic

UM-B-066

Abstract

This document outlines the system design, configuration options and supported features of DA1468x Basic Development Kit, rev-E (224-18-E).

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Tables

1 Terms and definitions

DCR	Direct Current Resistance
DCXO	Digitally Controlled Crystal Oscillator
HW	hardware
IFA	Inverted-F Antenna
JTAG	Join Test Action Group (test interface)
LED	Light Emitting Diode
LDO	Low-Dropout
RF	Radio Frequency
SMD	Surface Mounted Device
SOC	System on Chip
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

2 References

[1] DA14681 Datasheet, Dialog Semiconductor

[2] AN-B-041, DA14681 Development kit - Basic: UART with HW handshake, Application note, Dialog Semiconductor

3 Introduction

This document describes the DA14681 Basic Development kit. This kit offers a low cost development board with basic functionality. The development kit is implemented on a single PCB:

- DA14681 Basic: DA14681-00 Basic Kit / 224-18-E

4 System overview

4.1 Features

- Highly integrated Dialog Semiconductor DA1468x SoC
- DA1468x access over UART and/or JTAG without additional external hardware
- Access on all GPIOs provided from the chip, when no sensor board is plugged in
- Push-button for RESET function
- General purpose LED and button
- Current measurement point (pin header)
- Powered from either USB port or coin-cell battery (primary type only, not rechargeable)
- QSPI Flash memory up to 96 MHz clock frequency
- On-board printed inverted-F antenna
- Mechanical switch for conducted RF measurements
- Breakout headers for expansion and signal monitoring
- Integrated programming and debugging interfaces (JTAG/UART)

4.2 General description

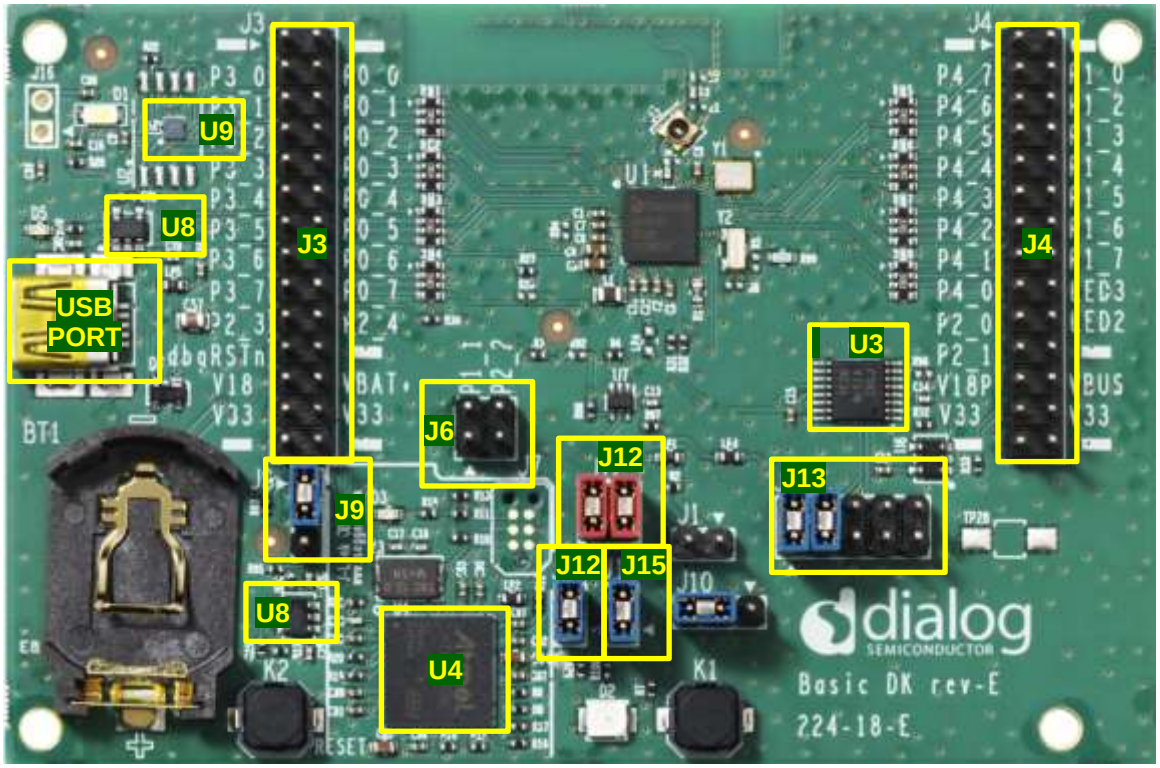

Figure 1 - DA1468x Basic development kit

The Basic development kit is based on the DA1468x SoC in an aQFN60 package. The highlighted sections of the system are:

1. DA1468x Dialog Semiconductor processor and interfaces.
2. QSPI Flash memory (U9 or U2): only for DA14681 devices.
3. USB port (USB2) with mini-USB connector. This is the evaluation, power supply and debugging port of the development kit. It provides the power to the development kit and the data bus for the Segger debugging processor.
4. Debugging processor (U4): This is an Atmel SAM3U2CA microcontroller that establishes the communication between the Dialog SoC and the user's PC.
5. Voltage translation (U3): It is used for translating the voltage level of SoC debugging signals to the voltage level of the debugging processor. In this way any leakage currents are minimised.
6. Breakout headers
    a. J3/J4: Most DA1468x GPIO signals are routed here.
    b. J6: Ports P1_1 and P2_2 are routed here.
7. Power management section.

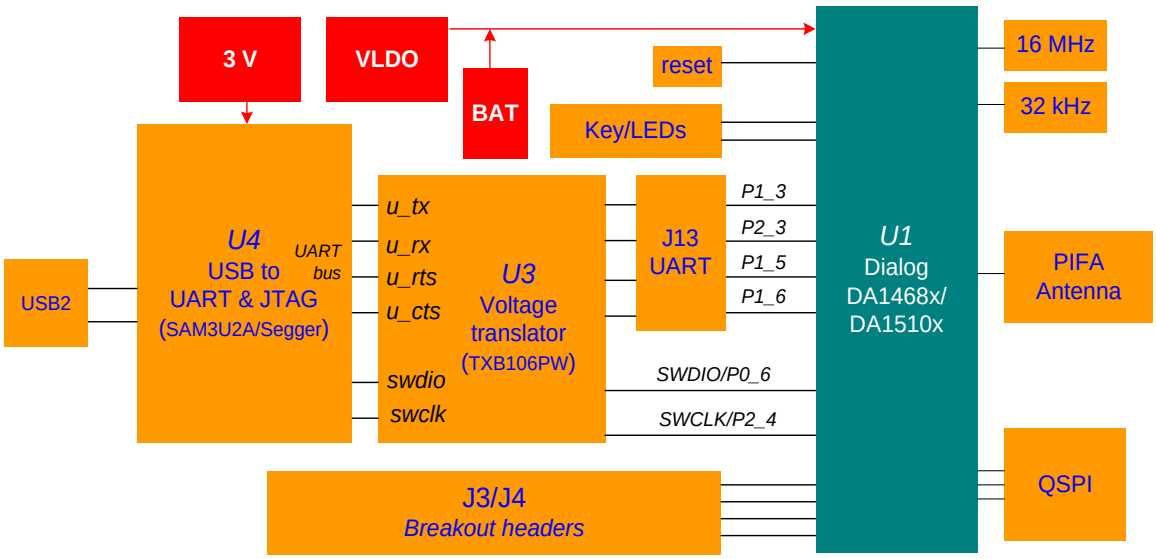

Figure 2 - Block diagram of DA1468x Basic development kit

The Basic development kit supports, DA14681 SoCs from Dialog Semiconductor. This is achieved by using the same board layout and populating different versions of the SoC.

5 Basic development kit system

5.1 Overview

Board name / number:

- DA146x DevKT-B_vE / 224-18-E

SoC:

- DA1468x in an aQFN60 package

Flash memory:

- W25Q80EW (8Mbit) QSPI Flash Memory, WLCSP package - **default**
- W25Q16DW (16M-bit) QSPI Flash Memory, (not populated) - *optional*
- 1.8 V power supply (default)
- 3.0 V power supply (optional)

Clock inputs:

- 16 MHz crystal
- 32 kHz crystal

Ports:

- USB port for debugging purposes (no charging)

Interfaces:

- UART - JLink CDC UART Port (listed under Ports in Device Manager)
- JTAG - JLink Driver (listed under Universal Serial Bus Controllers in Device Manager)

Connectivity – Expansion connectors:

- DA1468x Sensor board can be plugged directly on breakout headers J3, J4, J6.

Power source selection:

- LDO with options for 1.8 V, 3.0 V (default) or 3.3 V (USB powered)
- CR2032 coin-cell battery

5.2 DA1468x system

The DA1468x is a flexible System-on-Chip combining an application processor, memories, cryptography engine, power management unit, digital and analog peripherals and a radio transceiver.

The DA1468x is based on an ARM® Cortex®-M0 CPU delivering up to 84 DMIPS and provides a flexible memory architecture, enabling code execution from embedded memory (RAM, ROM) or non-volatile memory (OTP or external Quad-SPI Flash memory for DA14681). The advanced power management unit of the DA1468x enables it to run from primary and secondary batteries, as well as provide power to external devices.

An on-chip PLL enables on-the-fly tuning of the system clock between 32 kHz and 96 MHz to meet high processing requirements.

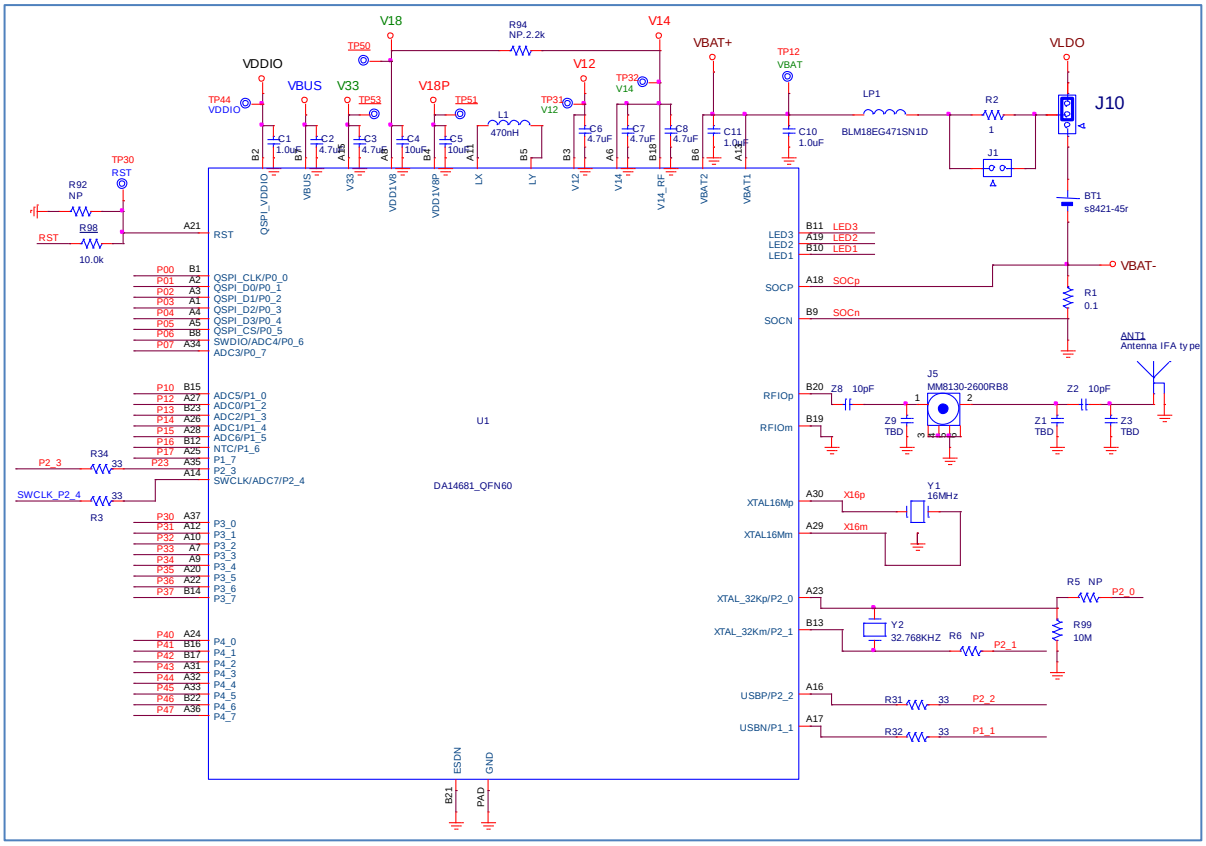

Figure 3: DA1468x system schematic

The DA1468x SoC power management subsystem consists of:

VBUS: Battery charger input as well as USB bus voltage. A decoupling capacitor equal or less than 4.7 µF is placed close to VBUS pin.

VBAT1: Battery connection. A 1 µF decoupling capacitor (C10), is required close to the pin (0402 package, 6.3 V). Voltage range for VBAT1 is 1.7 V to 4.75 V.

VBAT2: Input of the SIMO DC-DC converter. It is shorted externally with VBAT1. A 1 µF decoupling capacitor (C11) is required next to the pin (0402 package, 6.3 V).

V33: Output voltage rail (3.3 V). A ceramic decoupling capacitor of 4.7 µF (C3), (0402 package, 6.3 V) is placed. V33 cannot be turned off.

SIMO DC-DC converter outputs: V18, V18P, V12, V14. The inductor needed for DC-DC operation is placed externally. A low DCR inductor (L1) of 470 nH, 0805 is connected on LX/ LY pins.

V18, V18P: Power rails (1.8 V) for supplying external devices, even when the system is in sleep mode. Decoupling ceramic capacitors (C4, C5) of 10 µF (0603 package, 16 V), are placed as close

as possible to the V18, V18P pins. V18 is assigned to the external Flash memory. The current delivery capability of the V18, V18P power rails in active mode is 75 mA, whereas in sleep mode it is 2 mA.

V12: Power rail that supplies the digital core of the DA1468x and delivers up to 50 mA at 1.2 V when in active mode. A 4.7 µF decoupling capacitor (C6), is used (0402 package, 6.3 V).

V14: Power rail that delivers up to 20 mA at 1.4 V and should **not** be used for supplying external devices. A 4.7 µF decoupling capacitor (C7) is placed close to the V14 pin (0402 package, 6.3 V).

V14_RF: Supply voltage input. It is shorted to V14 on the PCB layout. V14_RF powers the RF circuits via a number of dedicated internal LDOs. A 4.7 µF decoupling capacitor (C8) is placed as close to the V14_RF pin as possible.

VDDIO: QSPI Flash interface supply voltage. It is connected to the same power rail as the Flash memory. A 1 µF decoupling capacitor (C1) is added. (0402 package, 6.3 V).

5.3 DA1468x pin assignment

All available signals are utilised or extracted on the breakout connectors.

Table 1 provides the pin assignment of the breakout connectors on the Basic development board and the related pin name on the aQFN60 package of the DA1468x.

Table 1: Basic development kit pin assignment

AQFN60 pin name	Development kit signal	Header pin	Comments
P0_0	FL_CLK	J3.4	Only for DA14681SoC.
P0_1	FL_D0	J3.6	
P0_2	FL_D1	J3.8	
P0_3	FL_D2	J3.10	
P0_4	FL_D3	J3.12	
P0_5	FL_CS	J3.14	
P0_6	SWDIO	J3.16	
P0_7	GPIO	J3.18	
P1_0	GPIO	J4.4	
P1_1	GPIO	J6.2	
P1_2	GPIO	J4.6	
P1_3	UTX	J4.8	
P1_4	GPIO	J4.10	
P1_5	LED (D2)	J4.12	Also RTS (through jumper on J13)
P1_6	BUTTON (K1)	J4.14	Also CTS (through jumper on J13)
P1_7	GPIO	J4.16	
P2_0	XTAL32P		Option to connect to J4.19 (place R5)
P2_1	XTAL32M		Option to connect to J4.21 (place R6)
P2_2	GPIO	J6.4	
P2_3	URX	J3.19	
P2_4	SWCLK	J3.20	
P3_0	GPIO	J3.3	
P3_1	GPIO	J3.5	

AQFN60 pin name	Development kit signal	Header pin	Comments
P3_2	GPIO	J3.7	
P3_3	GPIO	J3.9	
P3_4	GPIO	J3.11	
P3_5	GPIO	J3.13	
P3_6	GPIO	J3.15	
P3_7	GPIO	J3.17	
P4_0	GPIO	J4.17	
P4_1	GPIO	J4.15	
P4_2	GPIO	J4.13	
P4_3	GPIO	J4.11	
P4_4	GPIO	J4.9	
P4_5	GPIO	J4.7	
P4_6	GPIO	J4.5	
P4_7	GPIO	J4.3	
LED1	LED1		On-board LED, not monitored on a break-out header pin.
LED2	LED2	J4.20	
LED3	LED3	J4.18	

5.4 Basic development kit jumper settings

Table 2: Default jumper settings on Basic development kit

Header	Jumper position	Function
J1	Not mounted	Pin header for current monitoring. Either measure directly the voltage drop on R2, or remove R2 and insert an ampere meter probe on the 2-pin header.
J16	Not mounted, No jumper allowed	Monitoring for system voltages V12 (core) V14 (Analog/RF).
J9	Mounted 1-2	Mounted 1-2: VLDO produces 3.0 V. Mounted 2-3: VLDO produces 3.3 V. Not Mounted: VLDO produces 1.8 V.
J10	Mounted 2-3	Mounted 2-3: DA1468x supplied from VLDO. Mounted 1-2: DA1468x supplied from battery.
J12	Mounted 1-2 & 3-4	Mounted: connects JTAG signals to debugging processor.
J13	Mounted 1-2 & 3-4	UART connection to Segger JLink serial port. To enable UART hardware handshakes (RTS/CTS), mount instead the provided jumper block.
J14	Mounted	P1_5 to LED D2. Remove jumper to use for RTS or other purpose.
J15	Mounted	Mounted: P1_6 to K1 (button). Remove jumper to use for CTS or other purpose.

5.5 Booting from UART

There is only one boot loader option for booting from UART using pins P1_3 (UTX) and P2_3 (URX). Please note that UART-booting does not support hardware handshake signals (RTS/CTS).

The settings for UART booting are:

- Baud rate 57600 Bd
- 8 bits
- No parity
- 1 stop bit

For more details on booting with UART hardware handshakes enabled, check application note *AN-D-041* (Ref. [2]).

5.6 Crystals

DA1468x SoC has two Digitally Controlled Crystal Oscillators (DCXO), one at 16 MHz (XTAL16M) and a second at 32.768 kHz (XTAL32K). The 32.768 kHz oscillator has no trimming capabilities and is used as the clock of the Extended/Deep Sleep modes. The 16 MHz oscillator can be trimmed.

The crystals used on the basic development kit are specified in Table 3 and Table 4.

Table 3: Y1 (16 MHz crystal) characteristics

Reference designator	Value
Part Number	7M-16.000MEEQ-T
Frequency	16 MHz
Accuracy	±10 ppm
Load Capacitance (C_L)	10 pF
Shunt Capacitance (C_0)	3 pF
Equivalent Series Resistance (ESR)	100 Ω
Drive Level (P_D)	50 µW

Table 4: Y2 (32 kHz crystal) characteristics

Reference designator	Value
Part Number	ABS07-32.768KHZ-7-T
Frequency	32.768 kHz
Accuracy	±20 ppm
Load Capacitance (C_L)	7 pF
Shunt Capacitance (C_0)	0.9 pF to 1.2 pF
Equivalent Series Resistance (ESR)	70 kΩ
Drive Level (P_D)	0.5 µW

5.7 RF port

DA1468x provides a single-ended RFIO port, matched to 50 Ω. The RF port consists of the RFIOp and RFIOm pins, where RFIOm is connected to ground. A copper trace with an impedance of 50 Ω interconnects the RF port and the antenna. A pi-network (Z1, Z2, Z3) is added for antenna matching purposes.

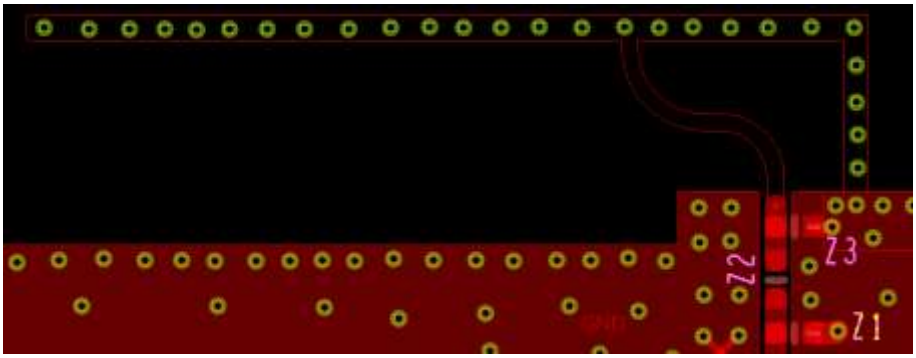

Figure 4: RF matching circuit must be placed as close as possible to the antenna

The Basic development kit provides an SMD RF switch in series with the printed IFA antenna. The SMD RF switch is used for conducted RF evaluation/testing. The RF switch type is MM8130-2600 supplied by Murata. Verification of the circuit performance is accomplished by inserting an external plug in the board-mounted receptacle. This action re-directs the circuit from normal condition to the plug side. Removing the plug restores the circuit back to its normal condition. Murata offers several options for a mating plug, MXHS83QH3000 is one possible pigtail option.

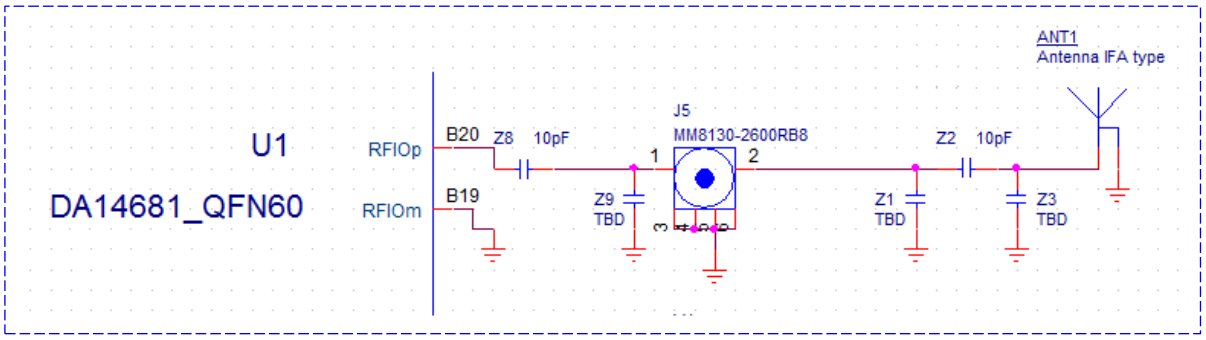

Figure 5: RF port, printed antenna and RF switch

5.8 QSPI Data Flash memory (U9 or U2)

The DA1468xBasic development kit includes an external QSPI Data Flash memory from Winbond. The W25Q80EW Flash memory supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clock instruction cycle Quad Peripheral Interface (QPI), Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1(D0), I/O2 (/WP) and I/O3(/HOLD). QSPI supply is selectable (V33 or V18) and the same supply voltage is also connected to the DA1468x VDDIO pin.

Please note that there are two package options available on the Basic development board. Only one of these must be assembled:

- U9 (default): W25Q80EW. 8 Mbit, lower power and form factor option.
- U2 (optional): W25Q16DWSSIG. 16 Mbit QSPI Data Flash memory in a SOIC package.

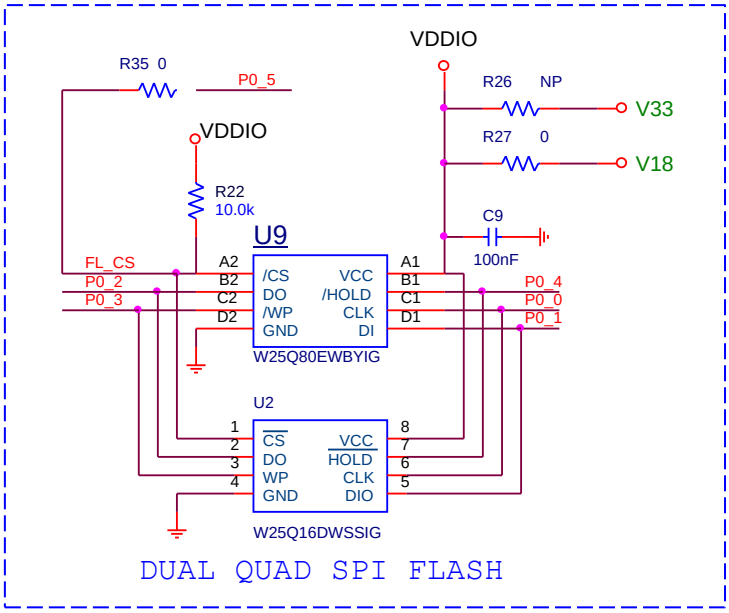

Figure 6: QSPI Data Flash V33 or V18 selectable power supply

The DA14681 uses the external Flash memory for directly executing code with some help from the internal cache, or simply for mirroring the contents in RAM during booting (option selectable via the binary image header).

Termination resistors are placed between the processor and Flash memory. These resistors are not required, but they are placed there to mitigate any signal integrity issues when additional loads are present (e.g. logic analyser probes on the breakout headers).

5.9 Push buttons and user controlled LEDs

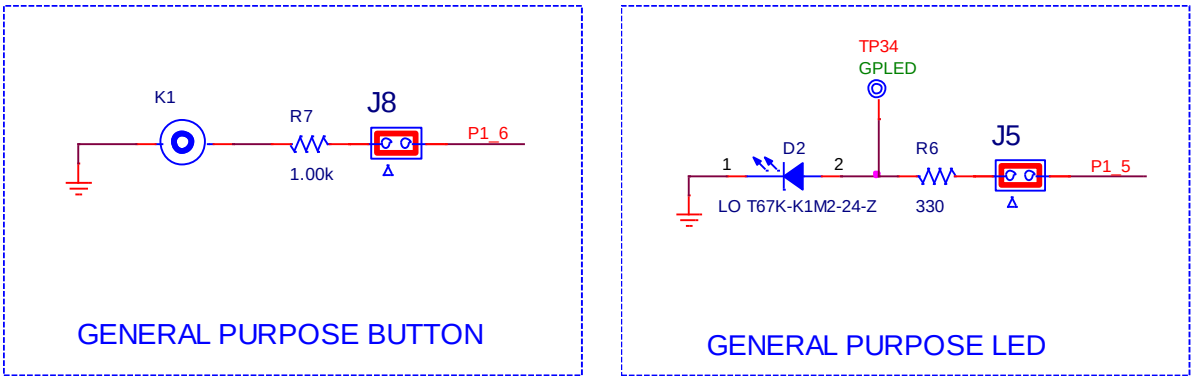

Figure 7: Push button and general purpose LED schematic

- K1 is connected to P1_6 through a jumper on header J8. Please note that via header J13, P1_6 is also connected to CTS.
- K2 is connected to the RESET line of the SoC.
- D1 (White LED): driven from LED1. LED1 is controlled directly from the DA1468x SoC.
- D2 (Orange LED): driven from P1_5 through header J5. Please notice that via header J13, P1_5 is connected also to RTS.

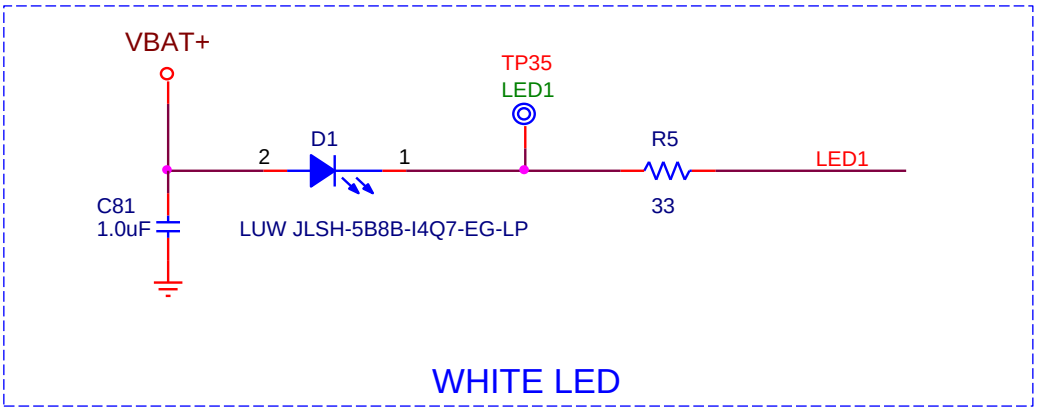

Figure 8: White LED

5.10 Debugging processor (U4)

The debugging port of the DA1468x Basic development kit is USB2. Two debugging ports (JTAG and UART) are used on the DA1468x SoC.

The USB-to-JTAG and USB-to-UART functions are implemented by the SAM3U2CA processor (U4), running the Segger JLink-OB firmware. The functions served by U4 are:

- Connectivity of PC to DA1468x JTAG port.
- Connectivity of PC to DA1468x UART port (full UART is possible but must be enabled on the PC driver).
- Hardware RESET capability through T_RESET signal. Note that the signal T_RESET is active LOW and therefore is inverted by U7 before reaching the RST pin on DA1468x.

The JTAG operating status is indicated via LED D3.

The SAM3U2CA chip is supplied with 3.3 V from U8. The U8 power status is indicated by LED D5.

J7 is the programming port of U4. The user does not need to access this port. It is only used in production for programming the Segger firmware and serial number.

Headers J13 and J12, for UART and JTAG respectively, interconnect the debugging processor with the DA1468x processor.

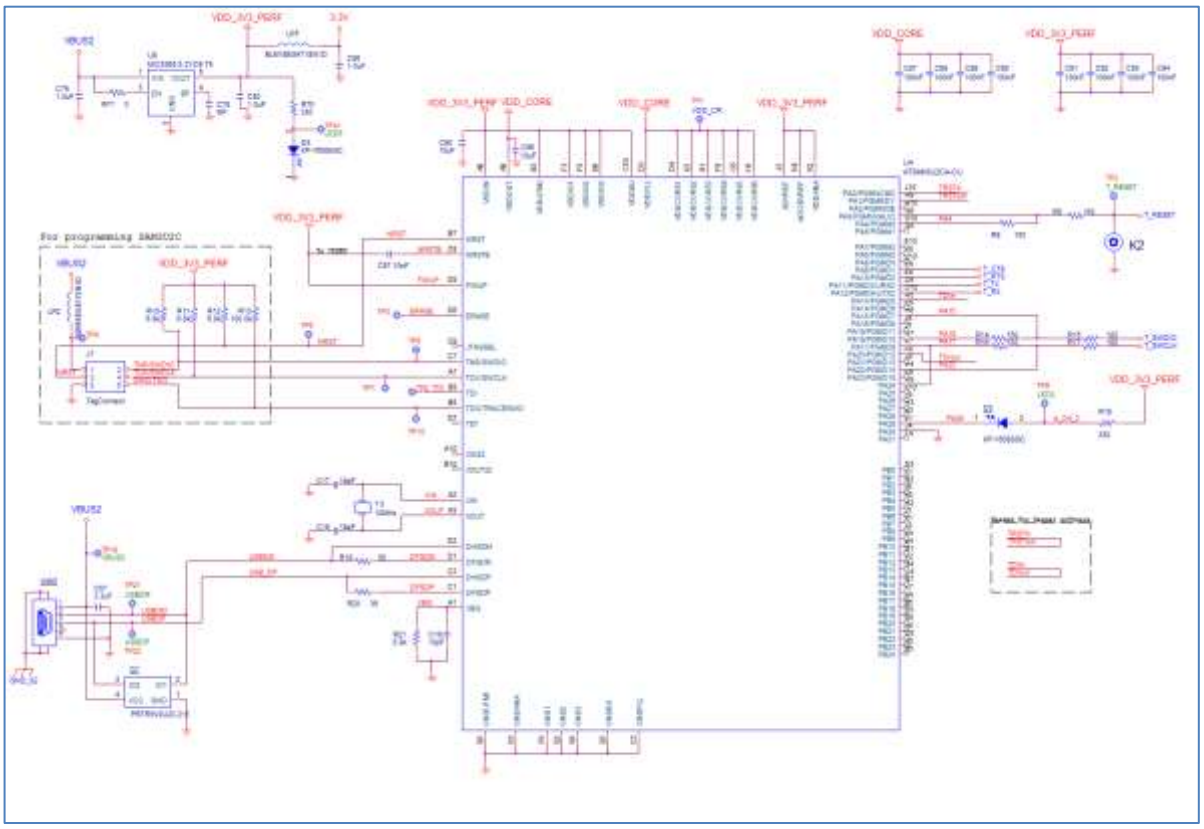

Figure 9: Debugging processor

5.11 Voltage level translation

The debugging processor U4 is supplied with 3.3 V. When the SoC I/O voltage rail is significantly less than 3.3 V, a miscommunication may occur, e.g. when a discharged battery supplies the SoC.

To avoid this problem a voltage translation circuitry has been added. The selected chip (TXB0106) is a 6-bit Bidirectional Voltage Level Translator with automatic direction detection.

Please note that this arrangement presumes that JTAG and UART pins on the DA1468x are always kept on the default (V33) I/O supply and not for some reason switched to the (optional) V18P levels.

Table 5: Signals using a voltage level translation/isolation chip

Pin name	Signal name
P0_6	SWDIO
P2_4	SWCLK
P1_3	UTX
P2_3	URX
P1_5	RTS
P1_6	CTS

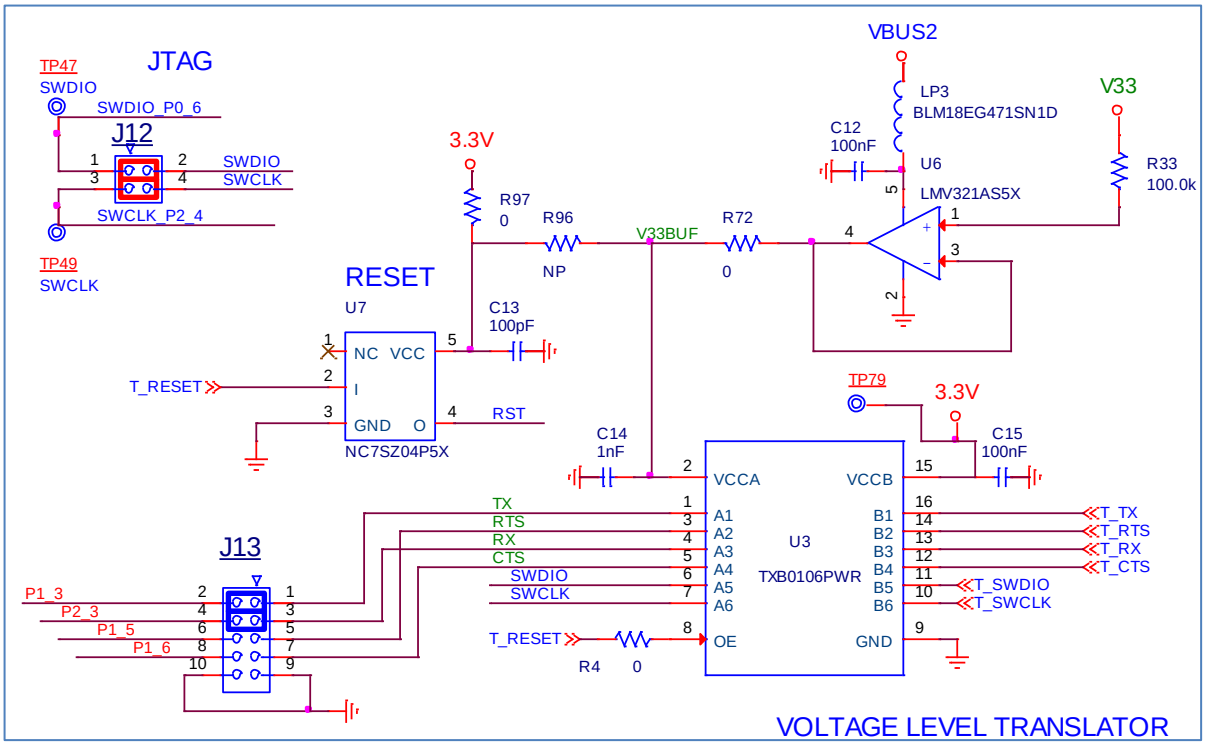

Figure 10: Level translator circuit

5.12 Leakage currents during power measurement

Leakage currents can occur through the UART and JTAG interface pins during sleep mode. For measuring the real power consumption during sleep modes (especially Hibernation mode), the UART and JTAG can be isolated from the rest of the (debugging) circuit by removing the jumpers from **J13** and **J12** for UART and JTAG respectively.

5.13 UART header (J13)

J13 interconnects DA1468x SoC UART signals with U4, the debugging processor.

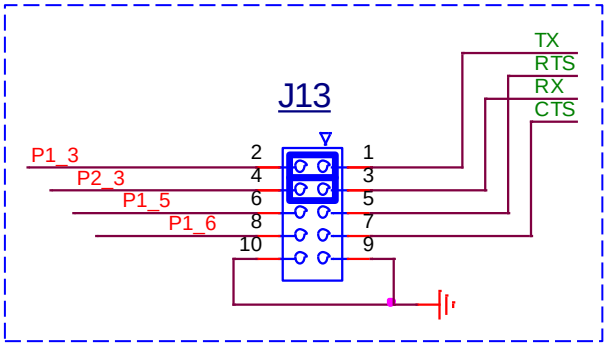

Figure 11: UART header (J13)

By default, only UTX and URX signals are placed/enabled. RTS and CTS are multiplexed with other functions. For a full UART functionality, a jumper block must be placed on top of J13. For more details, please refer to application note *AN-B-041* (Ref. [2]).

Table 6: DA1468x pin assignment of UART signal

aQFN60 pin name	Development kit signal	Also used for
P1_3	UTX	
P2_3	URX	
P1_5	RTS	LED via J14
P1_6	CTS	K1 push button via J15

Full UART configuration is supported by connecting RTS and CTS, with a special jumper block placed on top of J13. In this configuration, jumpers should be removed from J14 and J15. In this way signals P1_5 and P1_6 are removed from LED D2 and key K1 (see Figure 12)

Please note that full handshake UART is not supported for booting. For more details, refer to application note *AN-B-041* (Ref. [2]).

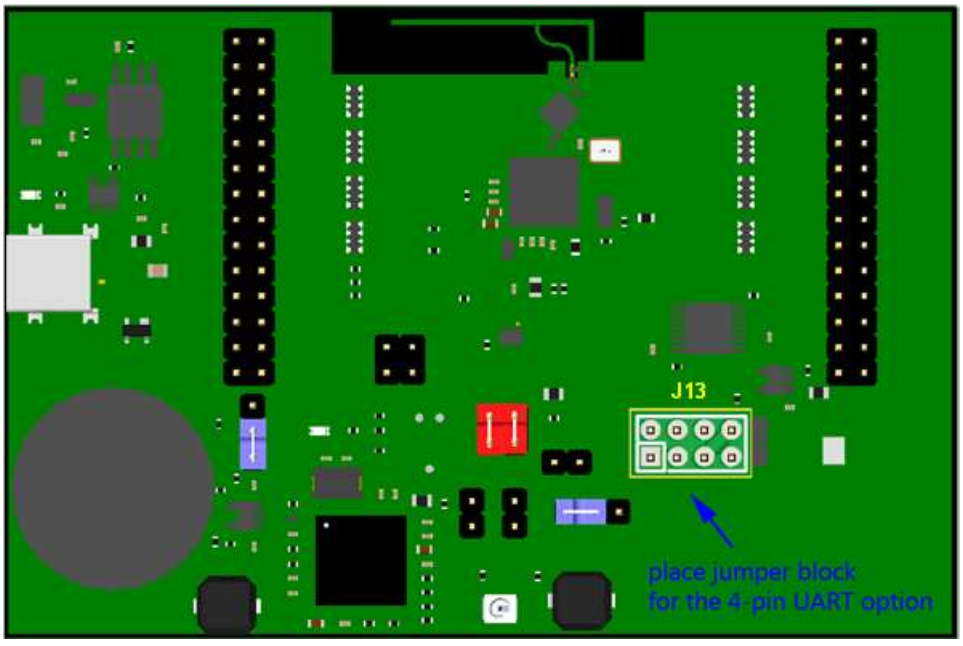

Figure 12: Full UART hardware configuration

5.14 Power section

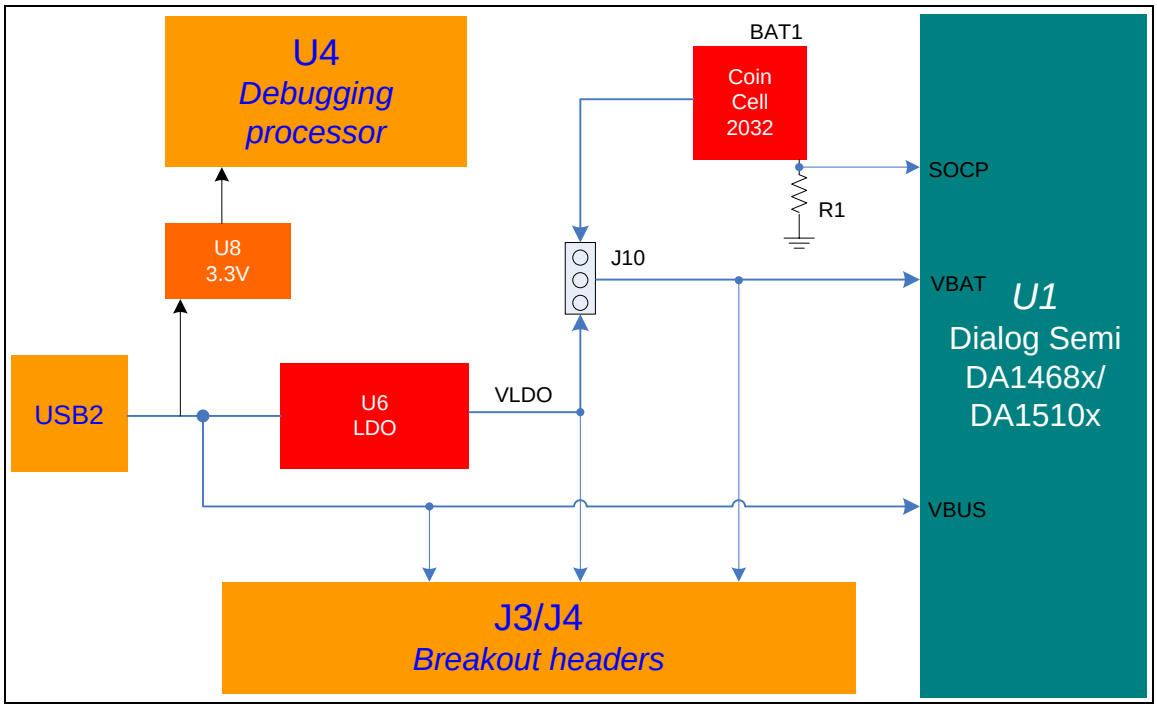

Figure 13: Basic development kit power section

- DA1468x basic development kit can be supplied either from USB port or Coin Cell battery. For USB port power options are:
- Through VLDO voltage regulator U5. The voltage regulator feeds VBAT pin of SoC.
- Though VBUS pin of SoC. In this case, nothing must be connected on the VBAT port.

Power input is set from header J10 jumper position.

Table 7: DA1468x SoC power options

J10 Header	DA1468x SoC power input	Comments
Mounted 1-2	VBAT supplied from Coin Battery	CR2032 coin cell battery.
Mounted 2-3	VBAT supplied from VLDO	3.3 V, 3.0 V or 1.8 V

USB port: Mini-USB connector. This is the evaluation, power supply and debugging port of the development kit. It provides power to the development kit and the data bus for the Segger debugging processor.

U5: This LDO can generate an output voltage of 3.3 V, 3.0 V or 1.8 V. For 1.8 V remove the jumper on header J9 (see Figure 14). By default the output voltage (VLDO) is 3.0 V.

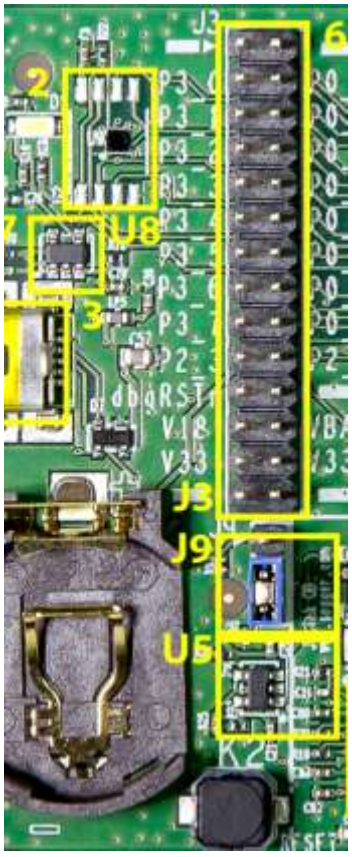

Figure 14: Location of jumper J9 and LDOs U5, U8

All voltages can be monitored by probing breakout headers J3 and J4.

Note: The coin cell battery does **not** supply the debugging processor. So when the USB cable is unplugged, no debugging ports will be available (JTAG or UART).

5.14.1 Battery options

The Basic development kit uses a CR2032 coin cell battery (primary, non-rechargeable battery). It is possible to externally connect other voltage sources or batteries, as long as the voltage is within the operating range of VBAT. Please note that charging a rechargeable battery is **not** supported.

Figure 15: Typical CR2032 (non-rechargeable) coin cell battery

To insert the battery, first slide it under the metal clip of the battery holder. Then push down the battery to secure it. See Figure 16.

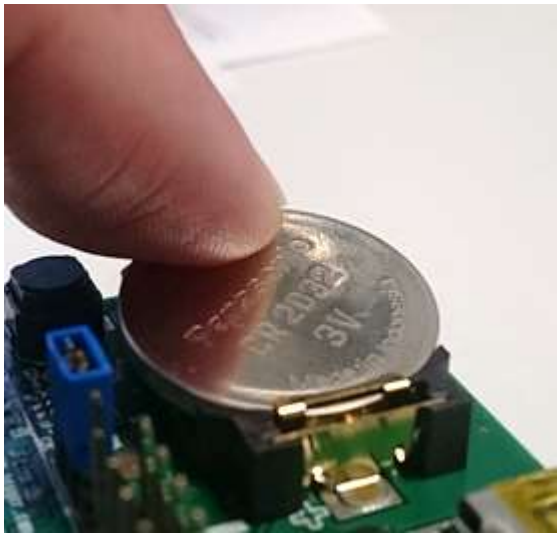

Figure 16: Coin cell battery placement

For battery replacement/removal, pull back the metallic clip (blue rectangle) and the battery will pop out by the spring of the battery holder (red rectangle). See. Figure 17.

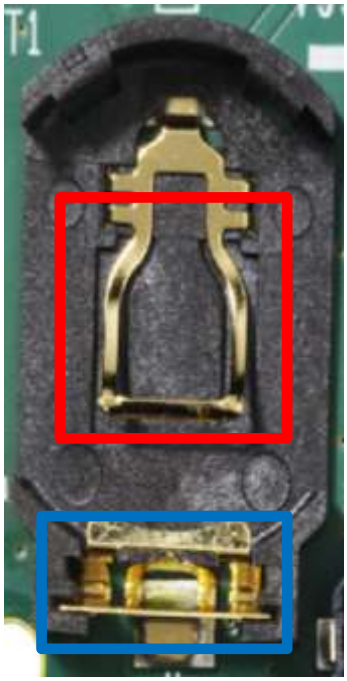

Figure 17: Removing the coin cell battery

6 Revision history

Revision	Date	Description
1.0	11-May-2016	Initial version.
1.1	26-May-2016	Improved pictures
1.2	10-June-2016	Updated to Rev.E
1.3	19-August-2016	Minor modifications to adapt to the DA1468x version
1.4	26-March-2018	Format changes
1.5	24-Dec-2021	Updated logo, disclaimer, copyright.

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Dialog Semiconductor complies to European Directive 2001/95/EC and from 2 January 2013 onwards to European Directive 2011/65/EU concerning Restriction of Hazardous Substances (RoHS/RoHS2).
Dialog Semiconductor's statement on RoHS can be found on the customer portal https://support.diasemi.com/. RoHS certificates from our suppliers are available on request.