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User's Manual

SuperH™ Family E10A Emulator

Additional Document for User's Manual

SH7618 E10A HS7618KCM02HE Renesas Microcomputer Development Environment System SuperH™ Family / SH7600 Series Specific Guide for the SH7618 E10A Emulator

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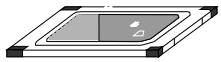
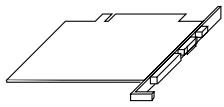
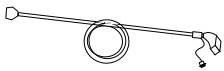
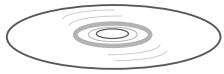
Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The SH7618 E10A emulator supports the SH7618. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator (HS7618KCM01H or HS7618KCI01H)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Card emulator	 (PCMCIA) or  (PCI)	1	HS7618KCM01H (PCMCIA: 14-pin type): Depth: 85.6 mm, Width: 54.0 mm, Height: 5.0 mm, Mass: 27.0 g HS7618KCI01H (PCI: 14-pin type): Depth: 144.0 mm, Width: 105.0 mm, Mass: 93.0 g
	User system interface cable		1	HS7618KCM01H (PCMCIA: 14-pin type): Length: 80 cm, Mass: 45.0 g HS7618KCI01H (PCI: 14-pin type): Length: 150 cm, Mass: 86.0 g
Soft-ware	SH7618 E10A emulator setup program, SuperH™ Family E10A Emulator User's Manual, and Specific Guide for the SH7618 E10A Emulator		1	HS7618KCM01SR, HS0005KCM01HJ, HS0005KCM01HE, HS7618KCM02HJ, and HS7618KCM02HE (provided on a CD-R)

1.2 Connecting the E10A Emulator with the User System

To connect the E10A emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU. In addition, read the E10A emulator user's manual and hardware manual for the related device.

Table 1.2 shows the type number of the E10A emulator and the corresponding connector type.

Table 1.2 Type Number and Connector Type

Type Number	Connector
HS7618KCM01H, HS7618KCI01H	14-pin connector

1.3 Installing the H-UDI Port Connector on the User System

Table 1.3 shows the recommended H-UDI port connectors for the emulator.

Table 1.3 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
14-pin connector	2514-6002	Minnesota Mining & Manufacturing Ltd.	14-pin straight type

Note: Do not install any components within 3 mm of the H-UDI port connector.

1.4 Pin Assignments of the H-UDI Port Connector

Figure 1.1 shows the pin assignments of the H-UDI port connector.

Note: Note that the pin number assignments of the H-UDI port connector shown below differ from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*[1]	SH7618 Pin No.	Note
1	TCK	Input	N10	
2*[2]	/TRST	Input	M11	
3	TDO	Output	N11	
4	Not connected	—	—	
5	TMS	Input	P11	
6	TDI	Input	R11	
7*[2]	/RES	Output	R12	
11	Not connected	—	—	
8 to 10 12 to 13	GND	—	—	
14*[3]	GND	Output	—	

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether the user system is connected or not.

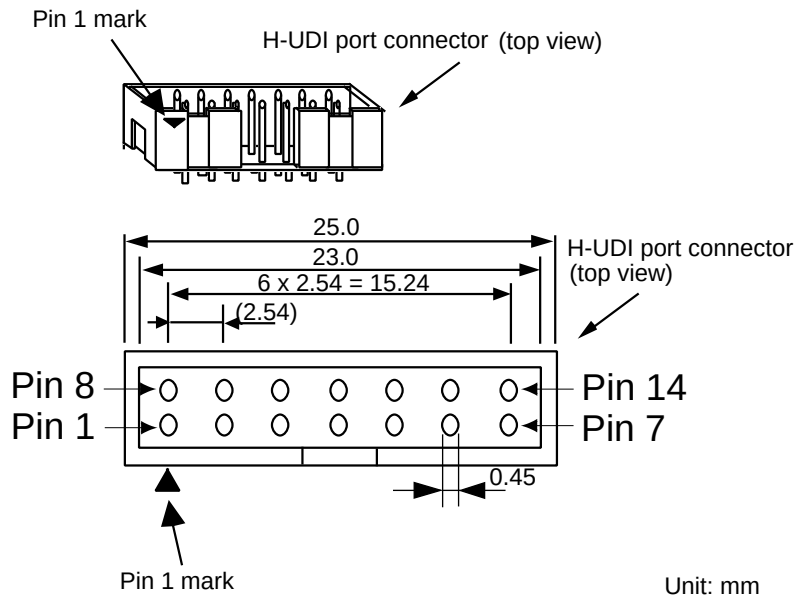


Figure 1.1 Pin Assignments of the H-UDI Port Connector

1.5 Recommended Circuit between the H-UDI Port Connector and the MPU

1.5.1 Recommended Circuit

Figure 1.2 shows a recommended circuit between the H-UDI port connector and the MPU.

Notes: 1. Do not connect anything to the N.C. pin of the H-UDI port connector.

2. The processing of the /ASEMD pin differs depending on whether the emulator is used or not. As the emulator does not control this pin, it must be controlled by a switch on the board.
   (1) When the emulator is used: /ASEMD = low (ASE mode)
   (2) When the emulator is not used: /ASEMD = high (normal mode)
3. The reset signal in the user system is input to the /RES pin of the SH7618. Connect this signal to the H-UDI port connector as the output from the user system.
4. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
5. The pattern between the H-UDI connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. The resistance values shown in figure 1.2 are recommended.
7. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related device.

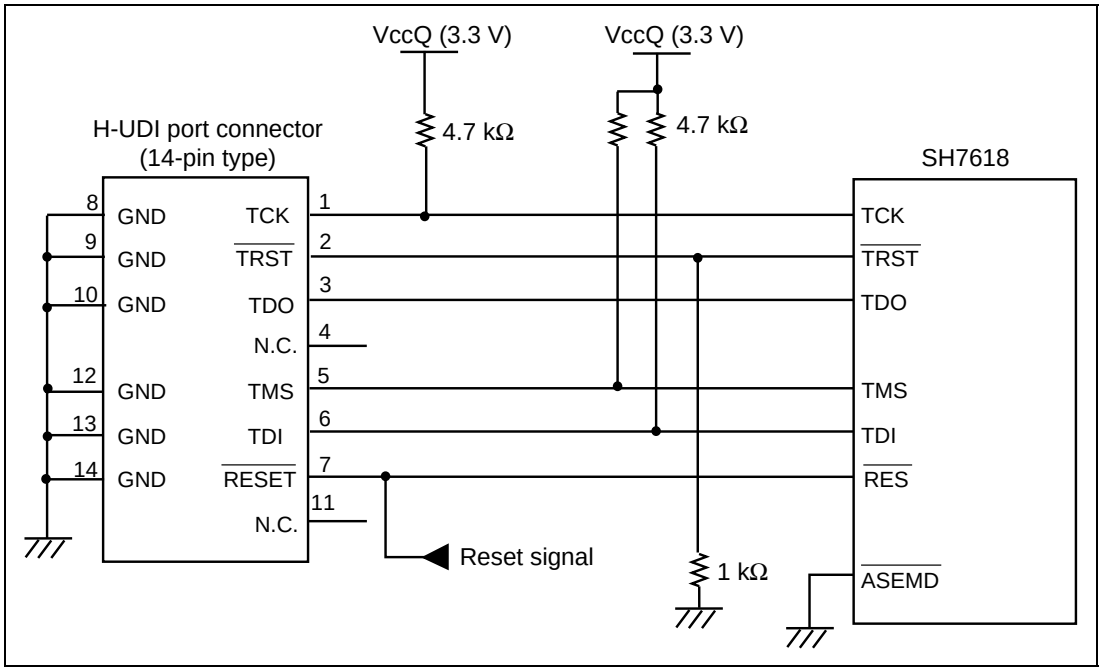


Figure 1.2 Recommended Circuit for Connection between the H-UDI Port Connector and MPU

Section 2 Specifications of the SH7618 E10A Emulator's Software

2.1 Differences between the SH7618 and the Emulator

- When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the actual SH7618 registers are undefined.

Table 2.1 Register Initial Values at Emulator Power-On

Register	Emulator at Power-on
R0 to R14	H'00000000
R15 (SP)	SP in the vector address
PC	PC in the vector address
SR	H'000000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000

- The emulator uses the H-UDI; do not access the H-UDI.

- Low-Power States (Sleep and Standby)

For low-power consumption, the SH7618 has sleep and standby states.
The sleep and standby states are switched using the SLEEP instruction. When the emulator is used, only the sleep state can be cleared with either the normal clearing function or with the [Stop] button, and a break will occur.

Note: The memory must not be accessed or modified in sleep state.

- Reset Signals

The SH7618 reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are input from the user system in command input wait state, they are not sent to the SH7618.

Note: Do not break the user program when the /RES and /WAIT signals are being low. A TIMEOUT error will occur. If the /WAIT signal is fixed to low during break, a TIMEOUT error will occur at memory access.

- Memory Access during User Program Execution

When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the E10A emulator to access the memory. Therefore, realtime emulation cannot be performed.

The stopping time of the user program is as follows:

Environment:
Host computer: 650 MHz (Pentium® III)
SH7618: 50 MHz
JTAG clock: 3.75 MHz

When a one-byte memory is read from the command-line window, the stopping time will be about 20 ms.

- Memory Access during User Program Break

The emulator can download the program for the flash memory area. Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

- Cache Operation during User Program Break

When cache is enabled, the emulator accesses the memory by the following methods:

— At memory write: Writes through the cache, then writes to the memory.
— At memory read: Does not change the cache write mode that has been set.

Therefore, when memory read or write is performed during user program break, the cache state will be changed.

- UBC

When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.

Do not use the UBC in the user program as it is used by the E10A emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

- Loading Sessions

Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be as follows:
When HS7618KCI01H is used: TCK = 4.125 MHz
When HS7618KCM01H is used: TCK = 3.75 MHz

- [IO] Window

  — Display and modification

  Do not change values of the user break controller because it is used by the emulator.

  For each watchdog timer register, there are two registers to be separately used for write and read operations.

Table 2.2 Watchdog Timer Register

Register Name	Usage	Register
WTCSR(W)	Write	Watchdog timer control/status register
WTCNT(W)	Write	Watchdog timer counter
WTCSR(R)	Read	Watchdog timer control/status register
WTCNT(R)	Read	Watchdog timer counter

- The watchdog timer operates only when the user program is executed. Do not change the value of the frequency change register in the [IO] window or [Memory] window.

- The internal I/O registers can be accessed from the [IO] window. After the I/O-register file is created, the MPU's specification may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. Note that, however, the E10A emulator does not support the bit-field function.

- Verify

In the [IO] window, the verify function of the input value is disabled.

- Illegal Instructions

If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

2.2 Specific Functions for the SH7618 E10A Emulator

The SH7618 E10A emulator does not support the following function:

- MMU-related functions (The SH7618 does not mount the MMU.)
  - VPMAP-related command
  - Virtual and Physical specification in the [Configuration] window
  - Virtual and Physical specification on the command-line function
  - Virtual and Physical specification in the [Breakpoint] window
  - LDTLB instruction execution break function
  - MEMORYAREA_SET command
- Profiler function
- Performance measurement function
- AUD trace function

2.2.1 Emulator Driver Selection

Table 2.3 shows drivers which are selected in the [E10A Driver Details] dialog box.

Table 2.3 Type Number and Driver

Type Number	Driver
HS7618KCM01H	E10A PC Card Driver 3
HS7618KCI01H	E10A PCI Card Driver 3

2.2.2 Break Condition Functions

In addition to BREAKPOINT functions, the emulator has Break Condition functions. Three types of conditions can be set under Break Condition 1, 2, 3. Table 2.4 lists these conditions of Break Condition.

Table 2.4 Types of Break Conditions

Break Condition Type	Description
Address bus condition (Address)	Breaks when the SH7618 address bus value or the program counter value matches the specified value.
Data bus condition (Data)	Breaks when the SH7618 data bus value matches the specified value. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings: Read/Write condition: Breaks when the SH7618 RD or RDWR signal level matches the specified condition. Bus state condition: Breaks when the operating state in an SH7618 bus cycle matches the specified condition. Types of buses that can be specified are listed below. • L-bus (CPU-ALL): Indicates an instruction fetch and data access, including a hit to the cache memory. • L-bus (CPU-Data): Indicates a data access by the CPU, including a hit to the cache memory. • I-bus (CPU.DMA): Indicates a CPU cycle when the cache memory is not hit, and a data access by the DMA.
Internal I/O break condition	Breaks when the SH7618 accesses the internal I/O.
Count	Breaks when the conditions set are satisfied the specified number of times.

Note: When U-RAM is accessed from the P0 space, the I-bus must be selected, and when accessed from the P2 space, the L-bus must be selected. When cache fill cycle is acquired, the I-bus must be selected.

Table 2.5 lists the combinations of conditions that can be set under Break Condition 1, 2, 3.

Table 2.5 Dialog Boxes for Setting Break Conditions

	Type				
Dialog Box	**Address Bus Condition (Address)**	**Data Bus Condition (Data)**	**Bus State Condition (Bus Status)**	**Count Condition (Count)**	**Internal I/O Break**
[Break Condition 1] dialog box	O	O	O	O	X
[Break Condition 2] dialog box	O	X	O	X	X
[Break Condition 3] dialog box	X	X	X	X	O

Note: O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2.2.3 Trace Functions

The SH7618 E10A emulator supports the trace functions listed in table 2.6.

Table 2.6 Trace Functions

Function	**Internal Trace**
Branch trace	Supported (four branches)
Range memory access trace	Not supported
Software trace	Not supported

Internal Trace Function: This function is activated by selecting the [Internal trace] radio button in the [Trace type] group box of the [Trace mode] page. This function traces and displays the branch instructions. The branch source address and branch destination address for the four latest branch instructions are displayed.

Notes: 1. If an interrupt is generated at the program execution start or end, including a step execution, the emulator address may be acquired. In such a case, the following message will be displayed. Ignore this address because it is not a user program address.

*** EML ***

2. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
3. Trace information cannot be acquired for the following branch instructions:
   - The BF and BT instructions whose displacement value is 0
   - Branch to H'A0000000 by reset
4. When [User] is specified in the [UBC mode] list box in the [Configuration] window, the internal trace is not acquired. In this case, exit the [Trace] window.
5. The SH7618 E10A emulator does not display the source code on the [Trace] window.

2.2.4 Note on Using the JTAG Clock (TCK)

Set the JTAG clock (TCK) frequency to less than the frequency of the SH7618 peripheral module clock (CKP).

2.2.5 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the internal RAM area. However, a BREAKPOINT cannot be set to the following addresses:
   - An area other than CS0 to CS6 and the internal RAM
   - An instruction in which Break Condition 2 is satisfied
   - A slot instruction of a delayed branch instruction
3. During step execution, BREAKPOINTs are disabled.
4. Conditions set at Break Condition 2 are disabled when an instruction to which a BREAKPOINT has been set is executed. Do not set a BREAKPOINT to an instruction in which Break Condition 2 is satisfied.
5. When execution resumes from the address where a BREAKPOINT is specified, single-step execution is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.

6. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
7. When a BREAKPOINT is set to the cacheable area, the cache block containing the BREAKPOINT address is filled immediately before and after user program execution.
8. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Editor] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the break condition, the mark ● disappears.

2.2.6 Notes on Setting the [Break Condition] Dialog Box and BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Break Condition 2 are disabled.
2. Break Condition 2 is disabled when an instruction to which a BREAKPOINT has been set is executed. Accordingly, do not set a BREAKPOINT to an instruction which satisfies Break Condition 2.
3. When a Break Condition is satisfied, emulation may stop after two or more instructions have been executed.
4. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.
5. Note that a break occurs with a break satisfaction condition by an instruction that has been cancelled due to the generation of an exception.
6. Use the sequential break or count break with the L-bus condition. If such break is used with the I-bus condition, it will not operate correctly.
7. A break will not occur with the execution counts specified on the execution of the multi-step instruction.

2.2.7 Notes on Setting the UBC_MODE Command

In the [Configuration] window, if [User] is set while the [UBC mode] list box has been set, the STEP-type commands that use Break Condition 2 for implementation cannot be used.

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Additional Document for User's Manual
Specific Guide for the SH7618 E10A Emulator

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