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Renesas Electronics Corporation

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User's Manual

SH-4A, SH4AL-DSP E200F Emulator

Additional Document for User's Manual Supplementary Information on Using the SH7318

Renesas Microcomputer Development Environment System
SuperH™ Family / SH7318 Series

E200F for SH7318 R0E873180EMU00E

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Contents

Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The E200F emulator supports the SH7318. Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

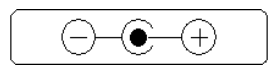
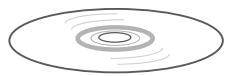
Classification	Component	Appearance	Quantity	Remarks
Hardware	Emulator main unit		1	R0E0200F0EMU00: Depth: 185.0 mm, Width: 130.0 mm, Height: 45.0 mm, Mass: 321.0 g
	AC adapter (serial numbers: 0081 or before)		1	Input: 100 to 240 V Output: 12 V 4.0 A Depth: 120.0 mm, Width: 72.0 mm, Height: 27.0 mm, Mass: 400.0 g 
	AC adapter (serial numbers: 0082 or after)		1	Input: 100 to 240 V Output: 12 V 3.0 A Depth: 99.0 mm, Width: 62.0 mm, Height: 26.0 mm, Mass: 270.0 g 
	AC cable		1	Length: 200 mm
	USB cable		1	Length: 1500 mm, Mass: 50.6 g

Table 1.1 Components of the Emulator (cont)

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware (cont)	External probe (serial numbers: 0081 or before)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
	External probe (serial numbers: 0082 or after)		1	Length: 500 mm, Pins 1 to 4: probe input pins, T: trigger output pin, G: GND pin
Soft-ware	E200F emulator setup program, SH-4A, SH4AL-DSP E200F Emulator User's Manual, Supplementary Information on Using the SH7318*		1	R0E0200F0EMU00S, R0E0200F0EMU00J, R0E0200F0EMU00E, R0E873180EMU00J, R0E873180EMU00E (provided on a CD-R)

Note: Additional document for the MPUs supported by the emulator is included. Check the target MPU and refer to its additional document.

1.2 Connecting the Emulator with the User System

To connect the E200F emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MPU.

It is impossible to connect the emulator to the 14-pin type connector that is recommended for the E10A-USB emulator. The 36-pin type connector is the same as that of the E10A-USB emulator. When designing the user system, read the E200F emulator user's manual and hardware manual for the related device.

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. This connector type is not available for the E200F emulator; the E10A-USB emulator is available.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.2 shows the recommended H-UDI port connectors for the emulator.

Table 1.2 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type

Note: When designing the 36-pin connector layout on the user board, do not place any other signals under the H-UDI connector to reduce cross-talk noises, etc.

1.4 Pin Assignments of the H-UDI Port Connector

Figure 1.1 shows the pin assignments of the 36-pin H-UDI port connector.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following page differs from those of the connector manufacturer.

Pin No.	Signal	Input/ Output *1	SH7318 Pin No.	Note	Pin No.	Signal	Input/ Output *1	SH7318 Pin No.	Note
1	AUDCK	Output	E10		19	TMS	Input	F11	
2	GND	—			20	GND	—		
3	AUDATA0	Output	C7		21	/TRST *2	Input	C10	
4	GND	—			22	(GND) *4	—		
5	AUDATA1	Output	F8		23	TDI	Input	C11	
6	GND	—			24	GND	—		
7	AUDATA2	Output	E9		25	TDO	Output	D12	
8	GND	—			26	GND	—		
9	AUDATA3	Output	D11		27	/ASEBRK *2 /BRKACK	Input/ output	F10	
10	GND	—			28	GND	—		
11	/AUDSYNC *2	Output	H6		29	UVCC	Output		
12	GND	—			30	GND	—		
13	NC	—			31	/RESETP *2	Output	F7	User reset
14	GND	—			32	GND	—		
15	NC	—			33	GND *3	Output		
16	GND	—			34	GND	—		
17	TCK	Input	C9		35	NC	—		
18	GND	—			36	GND	—		

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the user system interface cable is connected to this pin and the MPMD pin is set to 0, do not connect to GND but to the MPMD pin directly.

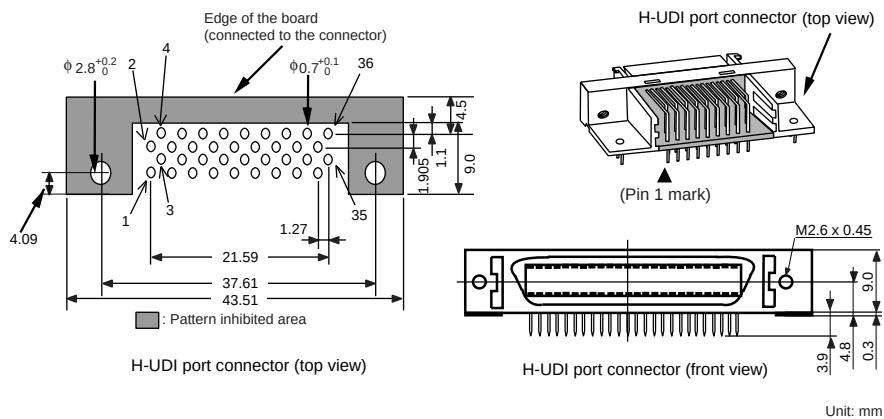


Figure 1.1 Pin Assignments of the H-UDI Port Connector (36 Pins)

1.5 Recommended Circuit between the H-UDI Port Connector and the MPU

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.2 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the MPU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. The MPMD pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
   (1) When the emulator is used: MPMD = 0
   (2) When the emulator is not used: MPMD = 1
   Figure 1.2 shows an examples of circuits that allow the MPMD pin to be GND (0) whenever the emulator is connected by using the user system interface cable.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The /TRST pin must be at the low level for a certain period when the power is supplied whether the H-UDI is used or not. Reduce the power supplied to the /TRST pin by pulling the pin down by a resistance of 1 kilo-ohm and setting PUL10 = 0 in the PULCR register after a reset.
5. The pattern between the H-UDI port connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. Since the H-UDI and the AUD of the MPU operate with the Vcc, supply only the Vcc to the UVCC pin.
7. The resistance values shown in figure 1.2 are reference.
8. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MPU.
9. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MPU at GND level.

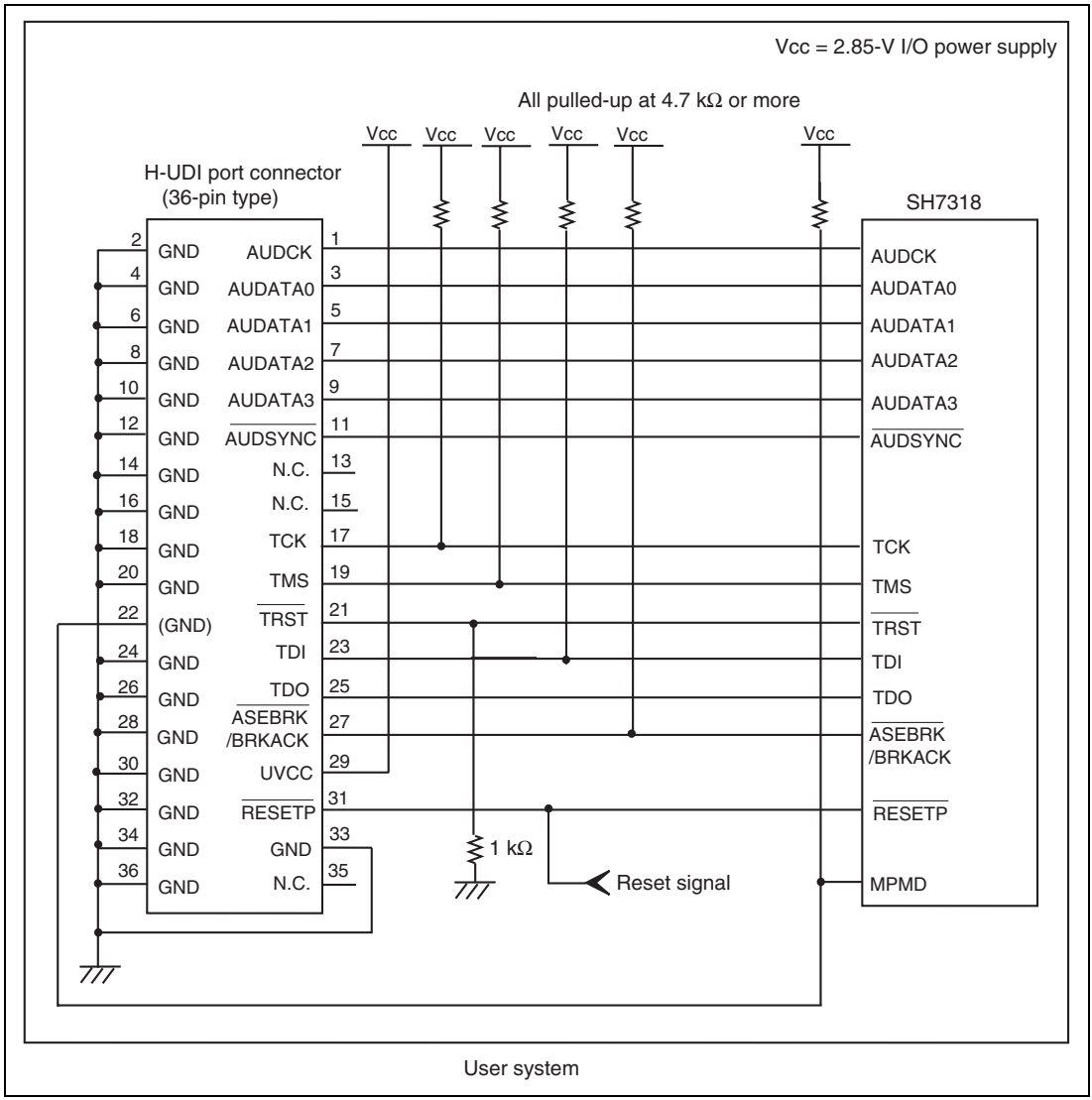


Figure 1.2 Recommended Circuit for Connection between the H-UDI Port Connector and MPU when the Emulator is in Use (36-Pin Type)

Section 2 Software Specifications when Using the SH7318

2.1 Differences between the SH7318 and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the actual SH7318 registers are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 2.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	H'A0000000
R0_BANK to R7_BANK	H'00000000
PC	H'A0000000
SR	H'700000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
SPC	H'00000000
SSR	H'000000F0
RS	H'00000000
RE	H'00000000
MOD	H'00000000
A0G, A1G	H'00000000
A0, A1	H'00000000
X0, X1	H'00000000
Y0, Y1	H'00000000
M0, M1	H'00000000
DSR	H'00000000

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States (Sleep, Software Standby, Module Standby, U Standby, and R Standby)

   For low-power consumption, the SH7318 has sleep, software standby, module standby, U standby, and R standby states.

   The sleep, software standby, and module standby states are switched using the SLEEP instruction. When the emulator is used, the sleep state can be cleared with either the normal clearing function or with the [STOP] button, and a break will occur.

Note: The memory must not be accessed or modified in sleep state.

4. Reset Signals

   The SH7318 reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the SH7318.

Note: Do not break the user program when the /RESETP, /BREQ, or /WAIT signal is being low. A TIMEOUT error will occur. If the /BREQ or /WAIT signal is fixed to low during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the emulator to access the memory. Therefore, realtime emulation cannot be performed.

   The stopping time of the user program is as follows:

   Environment:

   Host computer: 800 MHz (Pentium® III)
   JTAG clock: 30 MHz (TCK clock)

   When a one-byte memory is read from the command-line window, the stopping time will be about 45 ms.

7. Memory Access during User Program Break

   The emulator can download the program for the flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

8. Cache Operation during User Program Break

   When cache is enabled, the emulator accesses the memory by the following methods:

   - At memory write: Writes through the cache, then issues a single write to outside. The LRU is not updated.
   - At memory read: Reads memory from the cache. The LRU is not updated.

   Therefore, when memory read or write is performed during user program break, the cache state does not change.

   - At breakpoint set: Disables the instruction cache.

9. Port G

   The AUD pin is multiplexed as shown in table 2.2.

Table 2.2 Multiplexed Functions

Port	Function 1	Function 2
G	PTG4 input/output (port)*	/AUDSYNC (AUD)
G	PTG3 input/output (port)*	AUDATA3 (AUD)
G	PTG2 input/output (port)*	AUDATA2 (AUD)
G	PTG1 input/output (port)*	AUDATA1 (AUD)
G	PTG0 input/output (port)*	AUDATA0 (AUD)

Note: Function 1 can be used when the AUD pins of the device are not connected to the emulator. When the AUD trace function is enabled, the emulator changes settings so that function 2 is forcibly used.

10. UBC

    When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.
    Do not use the UBC in the user program as it is used by the emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

11. MFI

    When the MFI boot mode is used, be sure to activate the emulator by setting the RESETOUT signal as a trigger for the MFI transfer from the base-band side.
    In the active-through mode, the emulator does not operate during break.

12. Using RWDT

    At power-on reset, the operation of RWDT is enabled. When RWDT is not used, be sure to disable the operation of RWDT at the top of the user-reset program.
    The RWTCSR.TME bit is masked as 0 during break. Therefore, 0 is always displayed in the [IO] and [Memory] windows.

13. Memory Access during Break

    In the enabled MMU, when a memory is accessed and a TLB error occurs during break, it can be selected whether the TLB exception is controlled or the program jumps to the user exception handler in [TLB Mode] in the [Configuration] dialog box. When [TLB miss exception is enable] is selected, a “Communication Timeout error” will occur if the TLB exception handler does not operate correctly. When [TLB miss exception is disable] is selected, the program does not jump to the TLB exception handler even if a TLB exception occurs. Therefore, if the TLB exception handler does not operate correctly, a “Communication Timeout error” will not occur but the memory contents may not be correctly displayed.

14. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be 1.25 MHz.

15. [IO] window

    - Display and modification

      Do not change values of the User Break Controller because it is used by the emulator.

      For each RWDT register, there are two registers to be separately used for write and read operations.

Table 2.3 RWDT Register

Register Name	Usage	Register
RWTCSR(W)	Write	RWDT control/status register
RWTCNT(W)	Write	RWDT counter
RWTCSR(R)	Read	RWDT control/status register
RWTCNT(R)	Read	RWDT counter

The RWDT operates only when the user program is executed. Do not change the value of the frequency change register in the [IO] window or [Memory] window.

The internal I/O registers can be accessed from the [IO] window. However, note the following when accessing the SDMR register of the bus-state controller. Before accessing the SDMR register, specify addresses to be accessed in the I/O-register definition file (SH7318.IO) and then activate the High-performance Embedded Workshop. After the I/O-register definition file is created, the MPU’s specifications may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. Note that, however, the E200F emulator does not support the bit-field function.

- Verify

  In the [IO] window, the verify function of the input value is disabled.

16. Illegal Instructions

    If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

17. [Reset CPU] and [Reset Go] in the [Debug] Menu

    When a reset is issued from [Reset CPU] or [Reset Go] in the [Debug] menu, the clock pulse generator or system controller is not initialized.

2.2 Specific Functions for the Emulator when Using the SH7318

In the SH7318, a reset must be input when the emulator is activated.

2.2.1 Notes on Using the Trace Functions

The emulator supports the trace functions listed in table 2.4.

Table 2.4 Trace Functions

Function	Internal Trace	AUD Trace	Memory Output Trace
Branch trace	Supported (eight branches)	Supported	Supported
Range memory access trace	Supported (eight events)	Supported	Supported
Software trace	Supported (eight events)	Supported	Supported

Internal Trace Function: This function is activated by selecting the [Internal trace] radio button in the [Trace type] group box of the [Trace mode] page. Set the trace condition to be used.

Notes: 1. If an interrupt is generated at the program execution start or end, including a step operation, the emulator address may be acquired. In such a case, the following message will be displayed. Ignore this address because it is not a user program address.
*** EML ***

2. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
3. Trace information cannot be acquired for the following branch instructions:
   - The BF and BT instructions whose displacement value is 0
   - Branch to H'A0000000 by reset

AUD Trace Function: This function is operational when the AUD pin of the device is connected to the emulator. It is activated by selecting the [AUD trace] radio button in the [Trace type] group box of the [Trace mode] page.

Notes: 1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.

2. The AUD branch trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previously output address is the same as the upper 16 bits, the lower

16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.

3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 524288 lines. However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot be always acquired.
6. The AUD trace acquisition is not available when [User] is selected in the [UBC mode] list box of the [Configuration] dialog box. In this case, close the [Trace] window.
7. Do not use the AUD full-trace mode for the VIO function.
8. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.

Memory Output Trace Functions: This function is activated by selecting the [Use Memory trace] radio button in the [Trace type] group box of the [Trace mode] page.
In this function, write the trace data in the specified user memory range.
Specify the start address to output a trace for the [Start] edit box in the [User memory area] group box, and the end address for the [End Address] edit box.

Notes: 1. Use only the following addresses in the memory range for which trace is output:
<External memory area>
CS0, CS2, CS4, CS5A, CS5B, CS6A, and CS6B
<Internal memory area>
URAM: H'055E0000 to H'0561FFFF
XRAM: H'05007000 to H'05008FFF
YRAM: H'05017000 to H'05018FFF
Note that this address is on the system bus and not supported for the MMU or cache.

2. In the memory range for output, do not specify the ranges that the user program has been downloaded or the user program accesses.
3. The range for trace output must be 1 MB or less.

2.2.2 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the SH7318 peripheral module clock (CKP).
2. Set the AUD clock (AUDCK) frequency to 108 MHz or lower. If the frequency is higher than 108 MHz, the emulator will not operate normally.
3. The set value of the JTAG clock (TCK) is initialized by executing [Reset CPU] or [Reset Go].

2.2.3 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the internal RAM area. However, a BREAKPOINT cannot be set to the following addresses:
   - ROM areas in CS0 to CS6
   - Areas other than CS0 to CS6
   - Areas other than the internal RAM
   - A slot instruction of a delayed branch instruction
   - An area that can be only read by MMU
3. During step operation, BREAKPOINTs are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified, single-step operation is performed at the address and execution is continued from the next PC value. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
6. Note on DSP repeat loop:
   A BREAKPOINT is equal to a branch instruction. In some DSP repeat loops, branch instructions cannot be set. For these cases, do not set BREAKPOINTs. Refer to the hardware manual for details.
7. When the [Normal] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address or a virtual address according to the SH7318 MMU status during command input when the VPMAP_SET command setting is disabled. The ASID value of the SH7318 PTEH register during command input is used. When VPMAP_SET command setting is enabled, a BREAKPOINT is set to a physical address into which address translation is made according to the VP_MAP table. However, for addresses out of the range of the VP_MAP table, the address to which a BREAKPOINT is set depends on the SH7318 MMU status during command input. Even

when the VP_MAP table is modified after BREAKPOINT setting, the address translated when the BREAKPOINT is set valid.

8. When the [Physical] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address. A BREAKPOINT is set after disabling the SH7318 MMU upon program execution. After setting, the MMU is returned to the original state. When a break occurs at the corresponding virtual address, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
9. When the [Virtual] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a virtual address. A BREAKPOINT is set after enabling the SH7318 MMU upon program execution. After setting, the MMU is returned to the original state. When an ASID value is specified, the BREAKPOINT is set to the virtual address corresponding to the ASID value. The emulator sets the BREAKPOINT after rewriting the ASID value to the specified value, and returns the ASID value to its original value after setting. When no ASID value is specified, the BREAKPOINT is set to a virtual address corresponding to the ASID value at command input.
10. An address (physical address) to which a BREAKPOINT is set is determined when the BREAKPOINT is set. Accordingly, even if the VP_MAP table is modified after BREAKPOINT setting, the BREAKPOINT address remains unchanged. When a BREAKPOINT is satisfied with the modified address in the VP_MAP table, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.
11. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

2.2.4 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.
3. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.

2.2.5 Note on Setting the UBC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [UBC mode] list box has been set, Ch10 (IA_OA_R) and Ch11 (OA_OA_CT_R) of Event Condition cannot be used.

2.2.6 Note on Setting the PPC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [PPC mode] list box has been set, Ch1 and Ch2 of the performance analysis function and options 1 and 2 of the profile function cannot be used.

Section 3 I/O Analyzer Function

The emulator supports the function that is used to trace or analyze the state of the specific I/O. For SH7318, the emulation function specific to Multi Function Interface (MFI) is supported.

3.1 Overview of the MFI Trace Functions

(1) Displaying the states of pins and settings of MFI

The latest state is always displayed during a break or running. The following pins and states are displayed.

Table 3.1 MFI Pin States

No.	Pin and State	Display Contents
1	MFI Mode	Displays mode that the MPU has been started up. General: Normal boot mode. During MFI boot: Downloading to MFRAM is not completed. Branch to MFRAM: Preparation of boot from MFRAM is completed. Extend through: Extended through mode and normal boot mode.
2	MFI Bit Mode	Displays the current MFI bus width.
3	MFI MFRAM Endian	Displays the endian when accessing the MFRAM from the on-chip CPU.
4	MFI Bus Order	Displays the byte order in MFIDATA31 to MFIDATA0 data; the byte order corresponds to the MFIADR1 and MFIADR0 bits.
5	MFI INTERRUPT	Displays that an interrupt by the MFIINT pin has occurred.
6	MFI Register (MFIGSR)	Displays the value of the MFIGSR register that has been read from or written to via MFI.
7	MFI Register Access (MFIxxxx)	Displays whether or not the MFIxxxx register has been accessed via MFI. The following register names are displayed: MFIDEVCR, MFISW4, MFIBCR, MFIDATA, MFIADR, MFIEICR, MFIICR, MFIMCR, MFISCR, and MFIGSR
8	Signal xxxxxxx (MFI Connector)	Displays the state of the xxxxxx pin that is connected to the MFI connector. The following pin names are displayed: STATUS0, PDSTATUS, and RESETP
9	Signal xxxxxxx	Displays the state of the xxxxxx pin for MFI that is connected to the MFI connector. The following pin names are displayed: THEXT, MFIMD, MFIE//WR, MFIRW//RD, /THCS, /MFICS, /MFIINT, THMSK, THMDCH, THA3, MFIRS/THA2, and THA1

(2) Tracing the data transfer via MFI

The following pins and states are acquired by a trace.

Table 3.2 Contents Traced via MFI

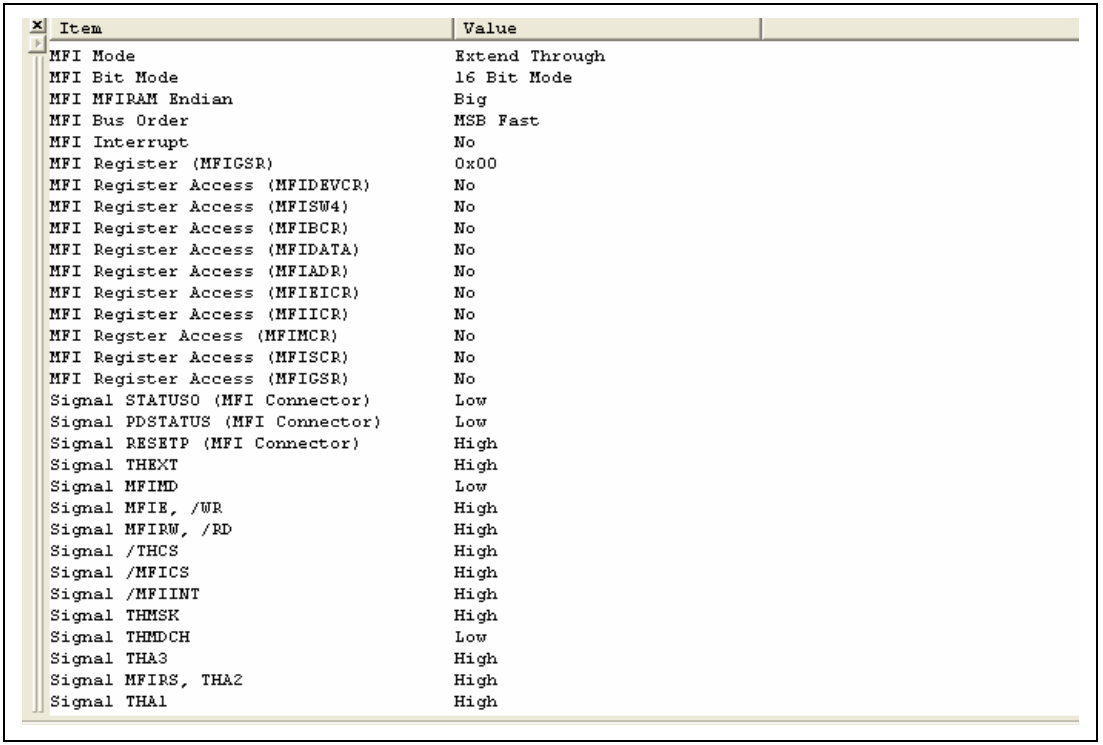
No.	Pin and State	Header of the [Trace] Window	Description
1	Transfer data	Data	Displays the value of transfer data.
2	Read or write	R/W	Displays the type of read of write.
3	Access	Instruction	Displays the access type. Index register access: Access to the MFIIDX register. MFI register access: Access to the internal register of MFI. Through register access: Access to the through register. SH bus register access: Access to the MPU directly connected to the SH bus.
4	Pin states	MFICS-THCS-THA3-THA2-THA1-THMDCH-MFIINT	Displays the states of MFICS, THCS, THA3, THA2, THA1, THMDCH, and MFIINT.
5	Time stamp	Timestamp	Displays the time stamp.
		Timestamp-Difference	Displays the difference between the previous trace data.

Note: If [NOP] or [Invalid access] is displayed on the [Instruction] column, connection failure may occur.

3.2 Using the MFI Trace Functions

(1) Using the function to display the states of pins and settings of MFI

The states are displayed in the [Extended Monitor] window that is opened by selecting [Extended Monitor] from [CPU] of the [View] menu.



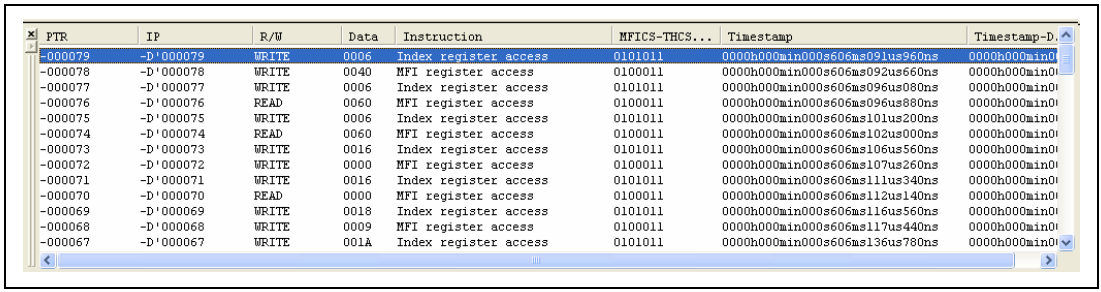
Item	Value
MFI Mode	Extend Through
MFI Bit Mode	16 Bit Mode
MFI MFIRAM Endian	Big
MFI Bus Order	MSB Fast
MFI Interrupt	No
MFI Register (MFIGSR)	0x00
MFI Register Access (MFIDEVCR)	No
MFI Register Access (MFISW4)	No
MFI Register Access (MFIBCR)	No
MFI Register Access (MFIDATA)	No
MFI Register Access (MFIADR)	No
MFI Register Access (MFIEICR)	No
MFI Register Access (MFIICR)	No
MFI Regster Access (MFIMCR)	No
MFI Register Access (MFISCR)	No
MFI Register Access (MFIGSR)	No
Signal STATUS0 (MFI Connector)	Low
Signal PDSTATUS (MFI Connector)	Low
Signal RESETP (MFI Connector)	High
Signal THEXT	High
Signal MFIMD	Low
Signal MFIE, /WR	High
Signal MFIRW, /RD	High
Signal /THCS	High
Signal /MFICS	High
Signal /MFIINT	High
Signal THMSK	High
Signal THMDCH	Low
Signal THA3	High
Signal MFIRS, THA2	High
Signal THA1	High

Figure 3.1 [Extended Monitor] Window

When [Properties…] is selected from the popup menu that is opened by right-clicking on the [Extended Monitor] window, the [Extended Monitor Configuration] dialog box is displayed. In this dialog box, items to be displayed can be selected.

(2) Using the function to trace the data transfer via MFI

The [Trace Window Type] dialog box is displayed by selecting [Trace] from [Code] of the [View] menu. Select [BUS/MFI Trace] to open the [BUS/MFI Trace] window.



PTR	IP	R/W	Data	Instruction	MFICS-THCS...	Timestamp	Timestamp-D.
-000079	-D'000079	WRITE	0006	Index register access	0101011	0000h000min000s606ms091us960ns	0000h000min0
-000078	-D'000078	WRITE	0040	MFI register access	0100011	0000h000min000s606ms092us660ns	0000h000min0
-000077	-D'000077	WRITE	0006	Index register access	0101011	0000h000min000s606ms096us080ns	0000h000min0
-000076	-D'000076	READ	0060	MFI register access	0100011	0000h000min000s606ms096us880ns	0000h000min0
-000075	-D'000075	WRITE	0006	Index register access	0101011	0000h000min000s606ms101us200ns	0000h000min0
-000074	-D'000074	READ	0060	MFI register access	0100011	0000h000min000s606ms102us000ns	0000h000min0
-000073	-D'000073	WRITE	0016	Index register access	0101011	0000h000min000s606ms106us560ns	0000h000min0
-000072	-D'000072	WRITE	0000	MFI register access	0100011	0000h000min000s606ms107us260ns	0000h000min0
-000071	-D'000071	WRITE	0016	Index register access	0101011	0000h000min000s606ms111us340ns	0000h000min0
-000070	-D'000070	READ	0000	MFI register access	0100011	0000h000min000s606ms112us140ns	0000h000min0
-000069	-D'000069	WRITE	0018	Index register access	0101011	0000h000min000s606ms116us560ns	0000h000min0
-000068	-D'000068	WRITE	0009	MFI register access	0100011	0000h000min000s606ms117us440ns	0000h000min0
-000067	-D'000067	WRITE	001A	Index register access	0101011	0000h000min000s606ms136us780ns	0000h000min0

Figure 3.2 [BUS/MFI Trace] Window

The MFI trace cannot be used with the bus trace. It is required that [MFI trace] has been selected in the [BUS/MFI acquisition] dialog box.

The following describes how to change and check the trace settings.

Select [Set] from the popup menu that is displayed by right-clicking the [Trace] window. The [BUS/MFI acquisition] dialog box is displayed.

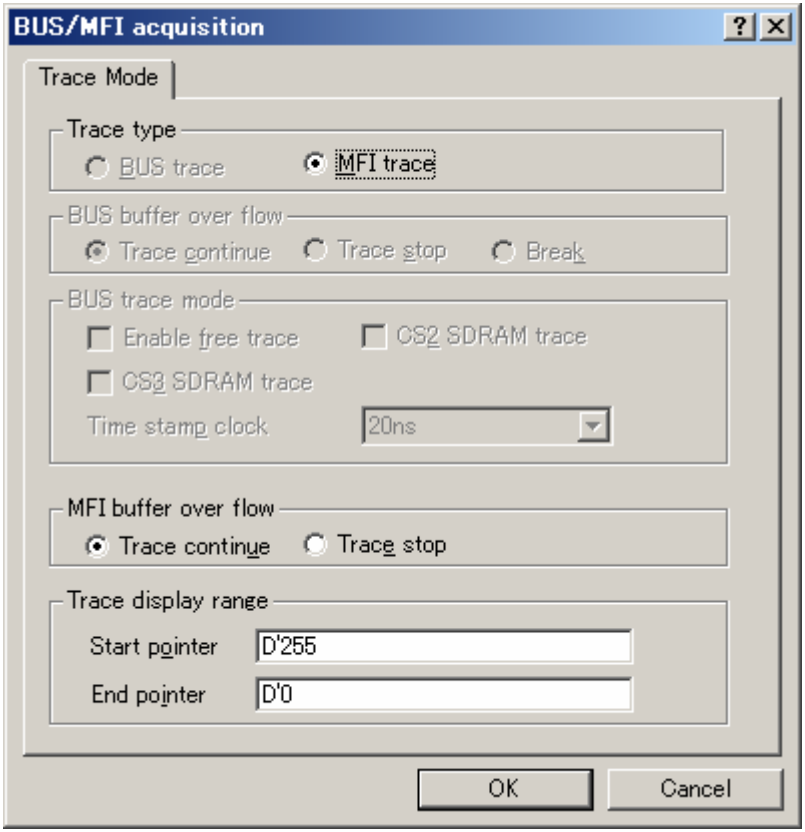


Figure 3.3 [BUS/MFI acquisition] Dialog Box

(a) To view the MFI setting information when the MFI or MPU is booted:

Accessing via MFI will have been completed when the emulator has been activated. The emulator polls the /RESETOUT pin that shows the completion of reset within the MPU, and acquires the MFI access by a trace without any conditions when the state of the /RESETOUT pin becomes high.

After the emulator is activated, select [MFI trace] on the [BUS/MFI acquisition] dialog box and display the [BUS/MFI Trace] window. It is possible to select [Halt] from the popup menu of the [BUS/MFI Trace] window. When [Halt] is selected, the acquired trace information is displayed on the [BUS/MFI Trace] window.

(b) To view the MFI access during a break:

Select [MFI trace] on the [BUS/MFI acquisition] dialog box and display the [BUS/MFI Trace] window. It is possible to select [Halt] or [Restart] from the popup menu of the [BUS/MFI Trace] window. When [Halt] is available, trace information has been acquired. When [Halt] is selected here, the acquired trace information is displayed.

When [Restart] is available, trace acquisition has not been started. When [Restart] is selected here, acquiring the trace information is started.

(c) To view the MFI access during execution of the user program:

The start of execution of the user program and acquisition of the trace information does not occur at the same time. To start acquiring the trace information, select [Restart].

It is possible to select [Halt] from the popup menu of the [BUS/MFI Trace] window. When [Halt] is selected, the acquired trace information is displayed and [Restart] becomes available.

When [Restart] is selected, acquiring the trace information is started at that time.

(d) Filter or find function for the data acquired by a trace:

When [Filter] or [Find] is selected from the popup menu of the [BUS/MFI Trace] window, the dialog box for that purpose is displayed. The data displayed on the [BUS/MFI Trace] window can be filtered or found with a data value.

(e) To specify the data to be acquired by a trace:

It is possible to set acquiring the required MFI trace data on the [Other event] sheet of the [Event] window.

- MFI Ch1 and Ch2

  The MFI trace can be started or halted by using the condition that has been set for these channels.

  It is also possible that only the condition is acquired by a trace or output as a trigger when the condition is satisfied.

  Figure 3.4 shows the dialog box to set the condition.

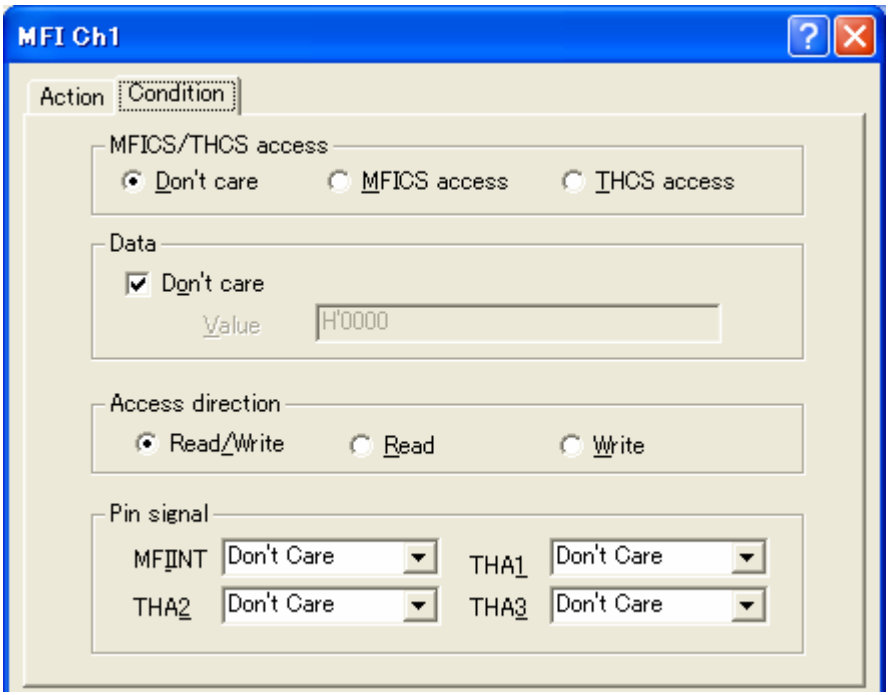


Figure 3.4 [MFI Ch1] Dialog Box

Conditions can be set on the [Condition] sheet. The operation when the condition is satisfied can be set on the [Action] sheet.

3.3 Connecting the Emulator with the User System

To use the MFI trace function, the emulator must be connected to the user system with the MFI trace cable. Install the MFI trace connector on the user system to connect the MFI trace cable, referring to section 3.4, Installing the MFI Trace Connector, in this manual. When designing the user system, read the E200F emulator user's manual and hardware manual for the related MPU.

3.4 Installing the MFI Trace Connector

3.4.1 MFI Trace Connector Installed on the User System

Table 3.3 shows the recommended MFI trace connector.

Table 3.3 Recommended Connector

Type Number	Manufacturer	Specification
QSH-030-01-L-D-A	Samtec, Inc.	QSH series, 0.5-mm pitch, 60 pins

Notes: 1. To connect the connector on the MFI trace cable, do not place any components within 6 mm of the MFI trace connector.

2. When the optional external bus trace unit is used, there are restrictions on the position to install the MFI trace connector. For details, refer to section 3.4.3, Layout of the MFI Trace Connector.

3.4.2 Pin Assignments of the MFI Trace Connector

Table 3.4 and figure 3.5 show the pin assignments of the MFI trace connector.

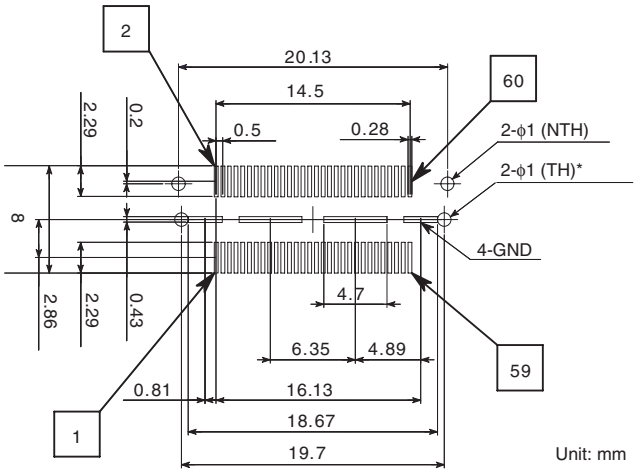
Table 3.4 Pin Assignments of the MFI Trace Connector

Pin No.	Signal	Input/ Output	SH7318 Pin No.	Note	Pin No.	Signal	Input/ Output	SH7318 Pin No.	Note
1	GND	-			29	THMDCH	Output	G18	29
2	GND	-			30	/THMSK*2	Output	F22	
3	STATUS2*5	Output	C4		31	/MFIINT*2	Output	K19	
4	GND	-			32	/MFICS*2	Output	H22	
5	GND	-			33	/THCS*2	Output	H19	
6	MFID0	Output	M20		34	GND	-		
7	MFID1	Output	N19		35	GND	-		
8	MFID2	Output	N18		36	MFIRW/RD	Output	J21	
9	MFID3	Output	N20		37	MFIE/WR	Output	K21	
10	MFID4	Output	M21		38	MFIMD	Output	G22	
11	MFID5	Output	M22		39	THEXT	Output	J18	
12	MFID6	Output	P22		40	/RESETP*2,*3	Output	F7	User reset
13	MFID7	Output	P19		41	STATUS0*4	Output	E8	
14	GND	-			42	/RESETOUT*2,*6	Output	D10	
15	GND	-			43	PDSTATUS*7	Output	C8	
16	MFID8	Output	L19		44	GND	-		
17	MFID9	Output	K18		45	GND	-		
18	MFID10	Output	L18		46	N.C.*10	-		
19	MFID11	Output	L20		47	N.C.*10	-		
20	MFID12	Output	J22		48	N.C.*10	-		
21	MFID13	Output	L21		49	N.C.*10	-		
22	MFID14	Output	K22		50	N.C.*10	-		
23	MFID15	Output	L22		51	N.C.*10	-		
24	GND	-			52	N.C.*10	-		
25	GND	-			53	N.C.*10	-		
26	THA1	Output	H18		54	GND	-		
27	MFIRS (THA2)	Output	K20		55	GND	-		
28	THA3	Output	J19		56	GND*8	Output		Connection detection

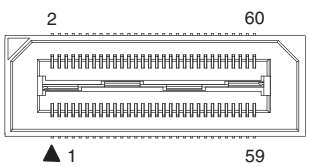
Table 3.4 Pin Assignments of the MFI Trace Connector (cont)

Pin No.	Signal	Input/ Output	SH7318 Pin No.	Note	Pin No.	Signal	Input/ Output	SH7318 Pin No.	Note
57	GND	-			59	VCC_MFI*9	Output	J23, K23	MFI VCC voltage detection
58	GND	-			60	VCC_MFI*9	Output	J23, K23	MFI VCC voltage detection

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. Connect the signal to the /RESETP pin of SH7318.
4. Connect the signal to the STATUS0 pin of SH7318.
5. Connect the signal to the STATUS2 pin of SH7318.
6. Connect the signal to the /RESETOUT pin of SH7318.
7. Connect the signal to the PDSTATUS pin of SH7318.
8. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
9. Connect the signal to the Vcc_MFI pin of SH7318.
10. Do not connect anything to the N.C. pins.



Recommended foot pattern for the MFI trace connector (top view)



MFI trace connector (top view)

Note: To install the connector manually on the board, solder the GND of the connector to the GND pad after the solder has appeared on the surface via TH from the rear of the board.

Figure 3.5 Pin Assignments of the MFI Trace Connector

3.4.3 Layout of the MFI Trace Connector

When designing the user system, there are restrictions on the position to install the MFI trace connector. Figures 3.6 and 3.7 show the position to install the MFI trace connector and the restriction on using the optional trace unit, respectively.

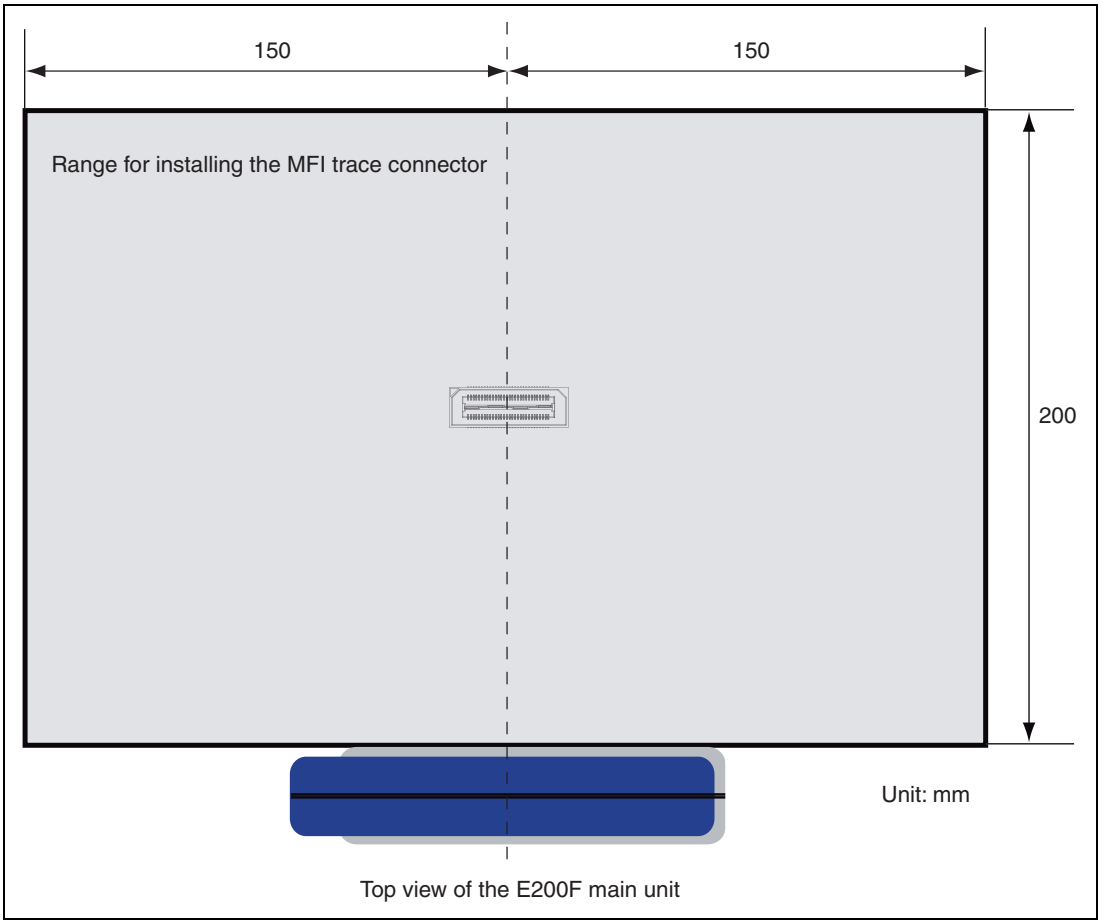


Figure 3.6 Position to Install the MFI Trace Connector (when the Trace Unit Not Used)

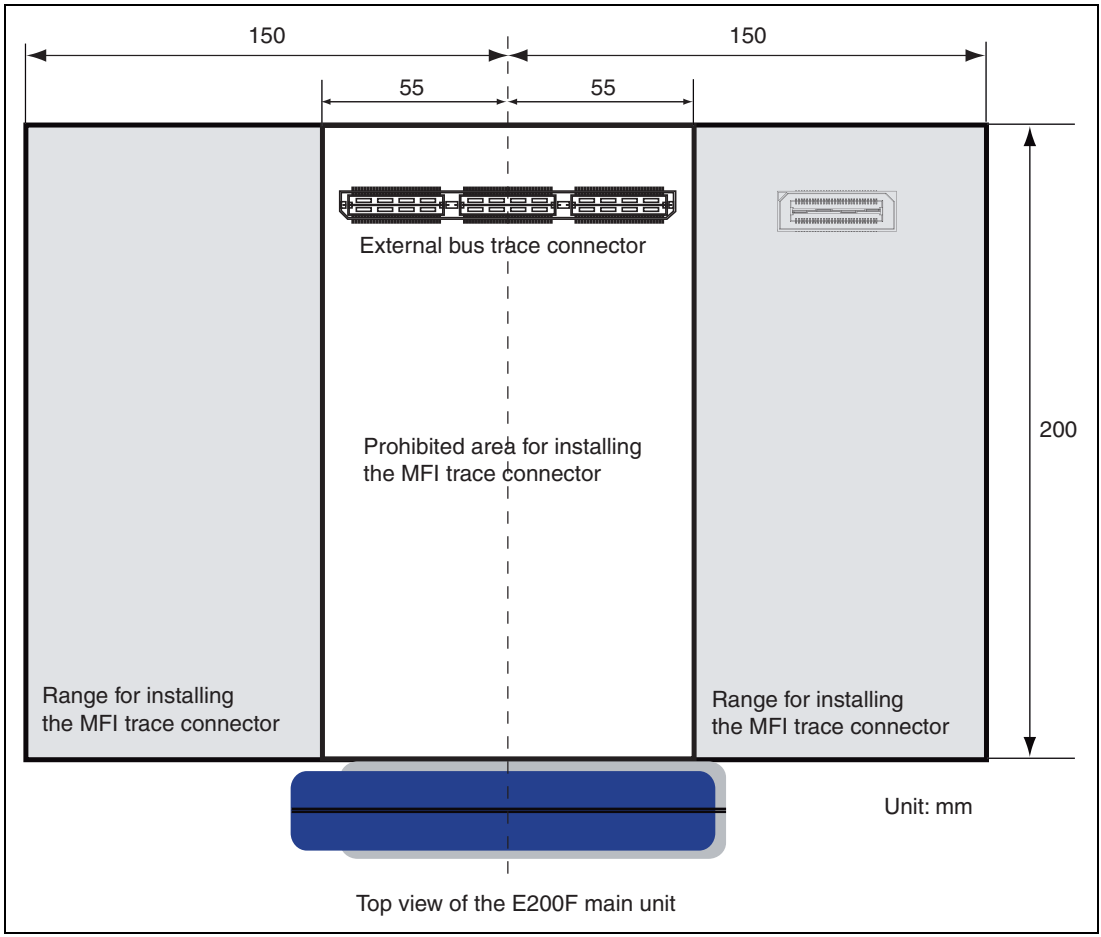


Figure 3.7 Position to Install the MFI Trace Connector (when the Trace Unit Used)

3.4.4 Recommended Circuit between the MFI Trace Connector and the MPU

Figure 3.8 shows a recommended circuit for connection between the MFI trace connector and the MPU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the MFI trace connector.
2. The pattern between the MFI trace connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
3. Since the MFI operates with the Vcc_MFI voltage, supply only Vcc_MFI to the Vcc_MFI pin.
4. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MPU.

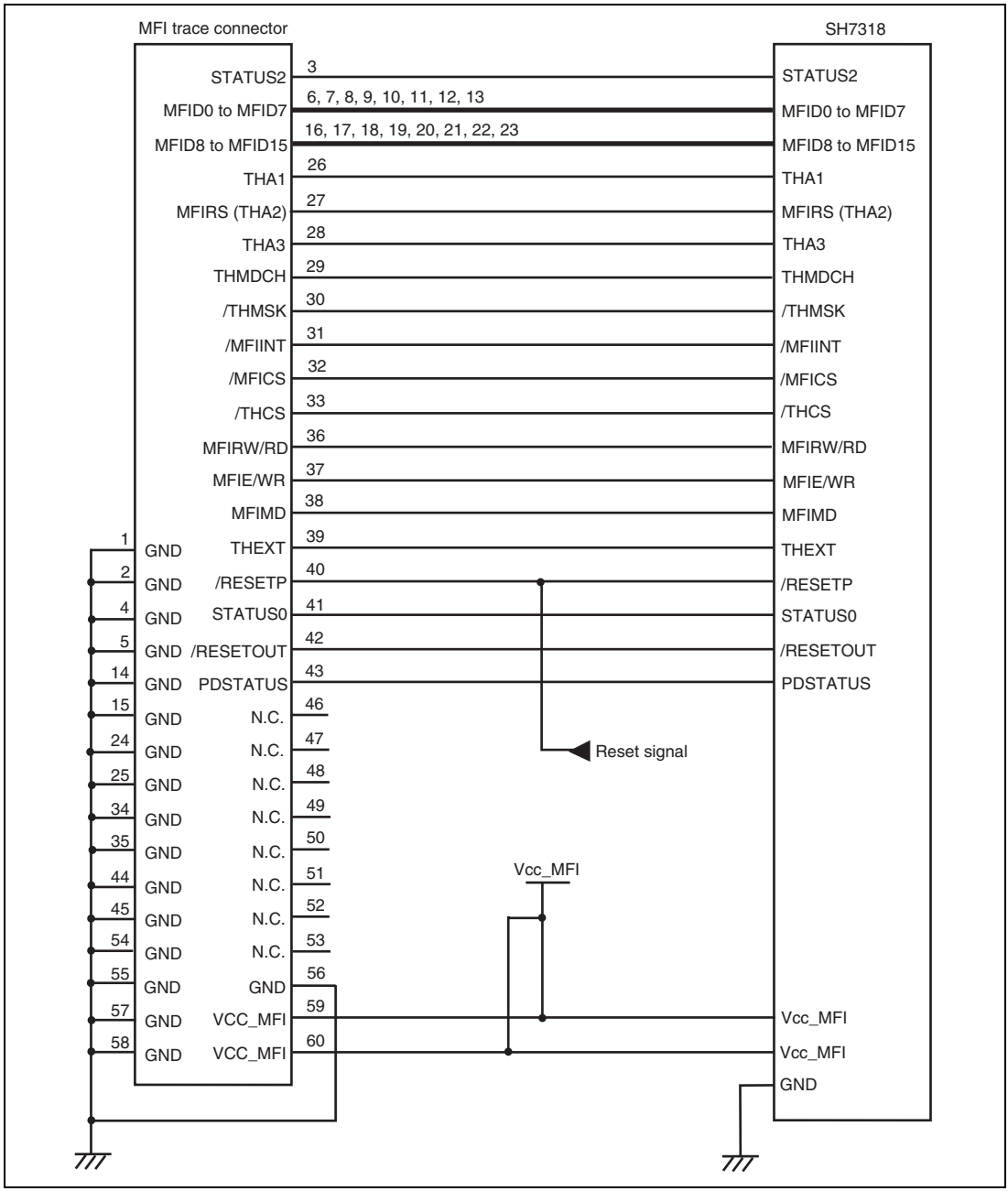


Figure 3.8 Recommended Circuit for Connection between the MFI Trace Connector and MPU

3.5 Restrictions on the MFI Trace and MFI Extended Monitor for I/O Analyzer Function

(1) When the emulator is booted with the 68 interface of the extended-through mode, the extended monitor will show a message [Standard through mode in MFI boot].

(2) For MFI trace, [DMA_MFRAM access] is only displayed at accessing MFRAM after bits LOCKW, DWTW, and WT in MFISCRR and MFISCRW have been set via the MFI bus. If these bits are set in the SH-Mobile user program, [MFI Register access] will be displayed after MFRAM is accessed.

(3) When MFIDREQ is transferred to MFIRAM, it may not be reflected on the extended monitor. It is because the assert timing of MFIDREQ is short and MFIDREQ is not sampled at the updated timing for the extended monitor.

Section 4 Preparing to Connect the Trace Unit

4.1 Connecting the E200F Trace Unit with the User System

To use the external bus trace function in the emulator, the emulator and the user system must be connected via the external bus trace unit (R0E0200F0ETU00). Install the trace unit connector on the user system for connection of the trace unit, referring to section 4.2, Installing the Trace Unit Connector, in this manual. When designing the user system, read the SH-4A, SH4AL-DSP E200F Emulator User's Manual and hardware manual for the related MPU.

4.2 Installing the Trace Unit Connector

4.2.1 Trace Unit Connector Installed on the User System

Table 4.1 shows the recommended trace unit connector.

Table 4.1 Recommended Connector

Type Number	Manufacturer	Specification
QTH-090-04-L-D-A	Samtec, Inc.	QTH series, 0.5-mm pitch, 180 pins

Notes: 1. To connect the connector on the trace unit, do not place any components within 6 mm of the trace unit connector.

2. When the optional MFI trace connector is used, there are restrictions on the position to install the trace unit connector. For details, refer to section 3.4.3, Layout of the MFI Trace Connector.

4.2.2 Pin Assignments of the User System Connector

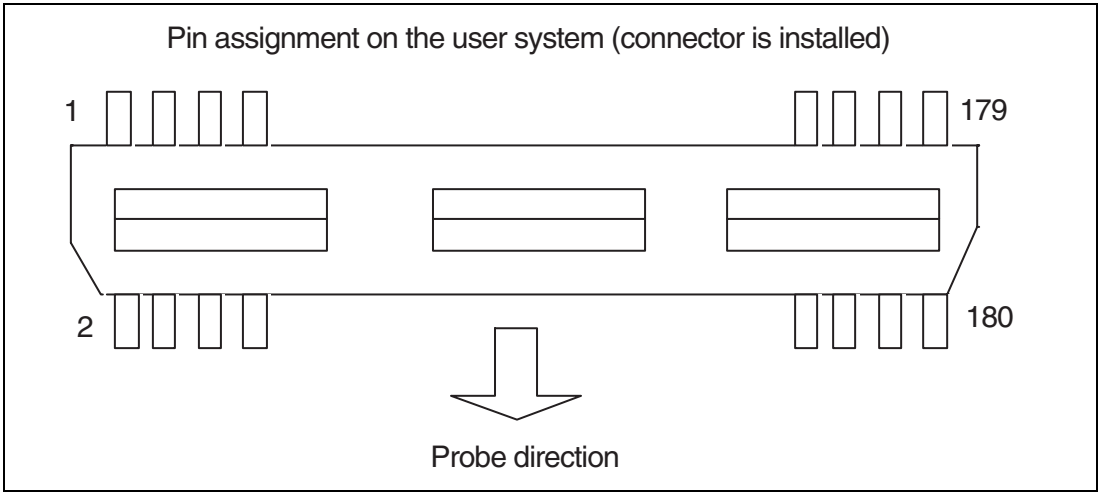


Figure 4.1 Pin Assignments of the User System Connector

4.2.3 Recommended Foot Pattern

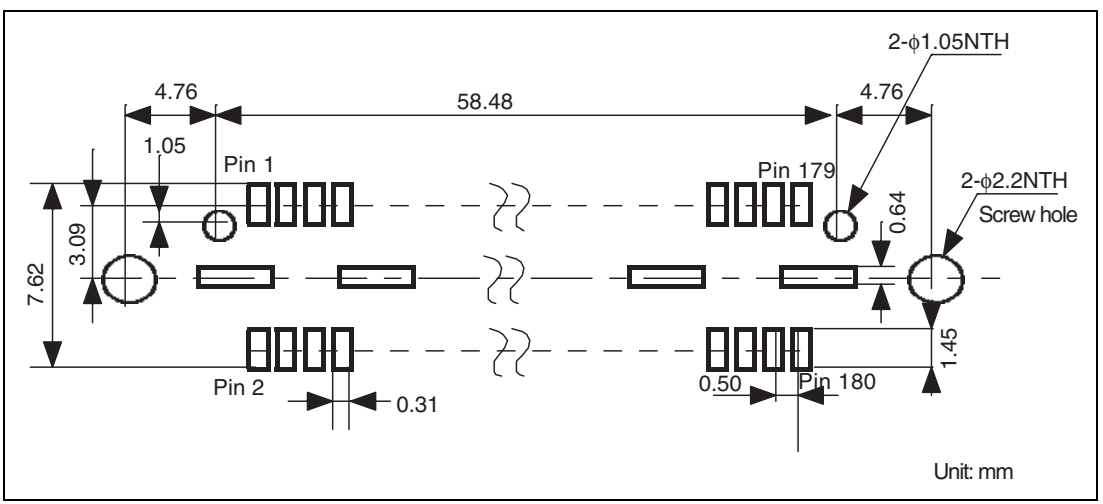


Figure 4.2 Recommended Foot Pattern (on which the Connector is Installed)

4.2.4 Restrictions on Component Installation

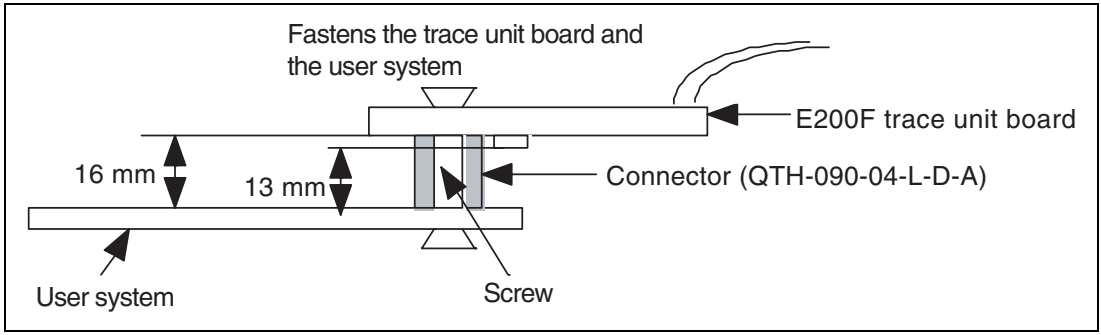


Figure 4.3 Restrictions on Component Installation

4.2.5 Pin Assignments of the Trace Unit Connector

Table 4.2 shows the pin assignments of the trace unit connector.

Table 4.2 Pin Assignments of the Trace Unit Connector

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
1		UA-P0	PTR0/CS5A/ A0	1.8 V/ 2.85 V	Port/address bus/ chip select 5A	Connect the address bus of the MPU.
2		UA-P1	A1	1.8 V/ 2.85 V	Address bus	Connect the address bus of the MPU.
3		UA-P2	A2	1.8 V/ 2.85 V	Address bus	Connect the address bus of the MPU.
4		UA-P3	A3	1.8 V/ 2.85 V	Address bus	Connect the address bus of the MPU.
5		UA-P4	A4/DV_D0	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
6		UA-P5	A5/DV_D1	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
7		UA-P6	A6/DV_D2	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
8		UA-P7	A7/DV_D3	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
9		GND	GND			
10		GND	GND			
11		UA-P8	A8/DV_D4	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
12		UA-P9	A9/DV_D5	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
13		UA-P10	A10/DV_D6	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
14		UA-P11	A11/FW E/DV_D7	1.8 V/ 2.85 V	Address bus/ NAND-AND flash-write enable/ pixel data	Connect the address bus of the MPU.
15		UA-P12	A12/FSC/ DV_D8	1.8 V/ 2.85 V	Address bus/ NAND-AND flash-read enable/ pixel data	Connect the address bus of the MPU.
16		UA-P13	A13/F0E/ DV_D9	1.8 V/ 2.85 V	Address bus/ NAND-AND flash address latch/ pixel data	Connect the address bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
17		UA-P14	A14/FCDE/ DV_D10	1.8 V/ 2.85 V	Address bus/ NAND-AND flash command latch/ pixel data	Connect the address bus of the MPU.
18		UA-P15	A15/DV_D11	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
19		GND	GND			
20		GND	GND			
21		UA-P16	A16/DV_D12	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
22		UA-P17	A17/DV_D13	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
23		UA-P18	A18/DV_D14	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
24		UA-P19	A19/DV_D15	1.8 V/ 2.85 V	Address bus/ pixel data	Connect the address bus of the MPU.
25		UA-P20	A20/DV_CLK	1.8 V/ 2.85 V	Address bus/ pixel clock output (13.5 MHz)	Connect the address bus of the MPU.
26		UA-P21	A21/ DV_HSYNC	1.8 V/ 2.85 V	Address bus/ pixel horizontal-synchronization signal	Connect the address bus of the MPU.
27		UA-P22	A22/ DV_VSYNC	1.8 V/ 2.85 V	Address bus/ pixel vertical-synchronization signal	Connect the address bus of the MPU.
28		UA-P23	PTR1/A23/ DMCAS	1.8 V/ 2.85 V	Port/address bus/ SDRAM RAS	Connect the address bus of the MPU.
29		GND	GND			
30		GND	GND			
31		UA-P24	PTR2/A24/ DMRAS	1.8 V/ 2.85 V	Port/address bus/ SDRAM RAS	Connect the address bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
32		UA-P25	PTR3/A25/ CKO	1.8 V/ 2.85 V	Port/external access clock/ address bus	Connect the address bus of the MPU.
33		UA-P26	GND			
34		UA-P27	GND			
35		UA-P28	GND			
36		UA-P29	GND			
37		UA-P30	GND			
38		UA-P31	GND			
39		GND	GND			
40		GND	GND			
41	IO	UD-P0	D0/NAF0	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
42	IO	UD-P1	D1/NAF1	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
43	IO	UD-P2	D2/NAF2	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
44	IO	UD-P3	D3/NAF3	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
45	IO	UD-P4	D4/NAF4	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
46	IO	UD-P5	D5/NAF5	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
47	IO	UD-P6	D6/NAF6	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.
48	IO	UD-P7	D7/NAF7	1.8 V/ 2.85 V	Data bus/NAND-AND flash data bus	Connect the data bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
49		GND	GND			
50		GND	GND			
51	IO	UD-P8	D8	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
52	IO	UD-P9	D9	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
53	IO	UD-P10	D10	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
54	IO	UD-P11	D11	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
55	IO	UD-P12	D12	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
56	IO	UD-P13	D13	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
57	IO	UD-P14	D14	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
58	IO	UD-P15	D15	1.8 V/ 2.85 V	Data bus	Connect the data bus of the MPU.
59		GND	GND			
60		GND	GND			
61	IO	UD-P16	LPD0	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
62	IO	UD-P17	LPD1	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
63	IO	UD-P18	LPD2	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
64	IO	UD-P19	LPD3	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
65	IO	UD-P20	LPD4	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
66	IO	UD-P21	LPD5	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
67	IO	UD-P22	LPD6	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
68	IO	UD-P23	LPD7	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
69		GND	GND			
70		GND	GND			
71	IO	UD-P24	LPD8	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
72	IO	UD-P25	LPD9	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
73	IO	UD-P26	LPD10	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
74	IO	UD-P27	LPD11	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
75	IO	UD-P28	LPD12	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
76	IO	UD-P29	LPD13	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
77	IO	UD-P30	LPD14	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
78	IO	UD-P31	LPD15	1.8 V	SDRAM data bus	Connect the SDRAM data bus of the MPU.
79		GND	GND			
80		GND	GND			
81	IO	UD-P32	PTT0/LPD16	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
82	IO	UD-P33	PTT1/LPD17	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
83	IO	UD-P34	PTT2/LPD18	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
84	IO	UD-P35	PTT3/LPD19	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
85	IO	UD-P36	PTT4/LPD20	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
86	IO	UD-P37	PTT5/LPD21	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
87	IO	UD-P38	PTT6/LPD22	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
88	IO	UD-P39	PTT7/LPD23	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
89		GND	GND			
90		GND	GND			
91	IO	UD-P40	PTU0/LPD24	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
92	IO	UD-P41	PTU1/LPD25	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
93	IO	UD-P42	PTU2/LPD26	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
94	IO	UD-P43	PTU3/LPD27	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
95	IO	UD-P44	PTU4/LPD28	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
96	IO	UD-P45	PTU5/LPD29	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
97	IO	UD-P46	PTU6/LPD30	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
98	IO	UD-P47	PTU7/LPD31	1.8 V	Port/SDRAM data bus	Connect the SDRAM data bus of the MPU.
99		GND	GND			
100		GND	GND			
101	IO	UD-P48	LPA1	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
102	IO	UD-P49	LPA2	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
103	IO	UD-P50	LPA3	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
104	IO	UD-P51	LPA4	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
105	IO	UD-P52	LPA5	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
106	IO	UD-P53	LPA6	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
107	IO	UD-P54	LPA7	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
108	IO	UD-P55	LPA8	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
109		GND	GND			
110		GND	GND			
111	IO	UD-P56	LPA9	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
112	IO	UD-P57	LPA10	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
113	IO	UD-P58	LPA11	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
114	IO	UD-P59	LPA12	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
115	IO	UD-P60	LPA13	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
116	IO	UD-P61	LPA14	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
117	IO	UD-P62	LPA15	1.8 V	SDRAM address bus	Connect the SDRAM address bus of the MPU.
118	IO	UD-P63	GND			
119		GND	GND			
120		GND	GND			
121	I	UCONT-P0	WE0/ DMDQM0	1.8 V/ 2.85 V	Lower byte write signal (D7-D0)/ SDRAM data mask or write enable	Connect the WE0/ DMDQM0 signal of the MPU.
122	I	UCONT-P1	WE1/ DMDQM1	1.8 V/ 2.85 V	Upper byte write signal (D15-D8)/ SDRAM data mask or write enable	Connect the WE1/ DMDQM1 signal of the MPU.
123	I	UCONT-P2	LPDQM0	1.8 V	SDRAM data mask 0	Connect the LPDQM0 signal of the MPU.
124	I	UCONT-P3	LPDQM1	1.8 V	SDRAM data mask 1	Connect the LPDQM1 signal of the MPU.
125	I	UCONT-P4	PTV2/ LPDQM2/ IRQ6	1.8 V	Port/SDRAM data mask 2/ IRQ6	Connect the LPDQM2/interrupt signal of the MPU.
126	I	UCONT-P5	PTV3/ LPDQM3/ IRQ7	1.8 V	Port/SDRAM data mask 3/ IRQ7	Connect the LPDQM3/interrupt signal of the MPU.
127	I	UCONT-P6	GND			
128	I	UCONT-P7	GND			
129	I	UCONT-P8	GND			
130	I	UCONT-P9	GND			

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
131	I	UCONT-P10	RDWR	1.8 V/ 2.85 V	Read/write signal	Connect the RDWR signal of the MPU.
132	I	UCONT-P11	RD	1.8 V/ 2.85 V	Read signal	Connect the RD signal of the MPU.
133	I	UCONT-P12	RESETP	2.85 V	Power-on reset	Connect the RESETP signal of the MPU.
134	I	UCONT-P13	LPRAS	1.8 V	SDRAM RAS	Connect the LPRAS signal of the MPU.
135	I	UCONT-P14	LPCAS	1.8 V	SDRAM CAS	Connect the LPCAS signal of the MPU.
136	I	UCONT-P15	LPRDWR	1.8 V	SDRAM WE	Connect the LPRDWR signal of the MPU.
137	I	UCONT-P16	PTH4/WAIT/ LCDLCLK	1.8 V/ 2.85 V	Port/external LCD clock-source input/ external wait input	Connect the wait signal of the MPU. When WAIT is not used, this is N.C.
138	I	UCONT-P17	PTJ7/ STATUS0	2.85 V	Port/ status output	Connect the STATUS0 signal of the MPU.
139	I	UCONT-P18	PTJ6/ STATUS2	2.85 V	Port/ status output	Connect the STATUS2 signal of the MPU.
140	I	UCONT-P19	PTJ5/ PDSTATUS	2.85 V	Port/ status output	Connect the PDSTATUS signal of the MPU.
141	I	UCONT-P20	NMI	2.85 V	NMI	Connect the NMI signal of the MPU.
142	I	UCONT-P21	PTJ2/IRQ0	2.85 V	Port/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
143	I	UCONT-P22	PTJ3/IRQ1	2.85 V	Port/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
144	I	UCONT-P23	PTF5/ SIOMCK/ IRQ2	1.8 V/ 2.85 V	Port/SIO master clock/interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
145	I	UCONT-P24	PTQ0/ SIOFMCK/ IRQ3/ SIUBMCK	1.8 V/ 2.85 V	Port/SIOF master clock/ SIU port B master clock input/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
146	I	UCONT-P25	SCPT4/SCL2/IRQ4	2.85 V	Port/I2C serial clock IO/ interrupt request	Connect the interrupt request signal. When interrupt is not used, this is N.C.
147	I	UCONT-P26	SCPT5/SDA2/IRQ5	2.85 V	Port/I2C serial data IO interrupt request	
148	I	UCONT-P27	N.C.*1			
149	I	UCONT-P28	N.C.*1			
150	I	UCONT-P29	N.C.*1			
151	I	UCONT-P30	N.C.*1			
152	I	UCONT-P31	N.C.*1			
153	I	GND	GND			
154	I	GND	GND			
155	I	CKO	CKO		Port/external access clock/ address bus	Connect the CK0 clock.
156	I	GND	GND			
157	I	GND	GND			

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
158	I	DDRCLK-P/ ASECK-P	LPCLK (CK)	1.8 V	SDRAM clock/ Mobile DDR clock	Connect the SDRAM clock.
159	I	GND	GND			
160	I	DDRCLK-N/ ASETS-N	GND			
161	I	GND	GND			
162	I	GND	GND			
163	I	CS0IN-N	CS0	1.8 V/ 2.85 V	Chip select 0	Connect CS (chip select). Fix the unused CS pin to high level.
164	I	CS1IN-N	PTE2/CS2/ FCE	1.8 V/ 2.85 V	Port/chip select 2/NAND-AND flash chip enable	Connect CS (chip select). Fix the unused CS pin to high level.
165	I	CS2IN-N	LPCS3	1.8 V	SDRAM chip select (CS3)	Connect CS (chip select). Fix the unused CS pin to high level.
166	I	CS3IN-N	PTR4/CS4	1.8 V/ 2.85 V	Port/chip select 4	Connect CS (chip select). Fix the unused CS pin to high level.
167	I	CS4IN-N	PTR0/CS5A/ A0	1.8 V/ 2.85 V	Port/ address bus/ chip select 5A	Connect CS (chip select). Fix the unused CS pin to high level.
168	I	CS5IN-N	PTR5/CS5B/D MCKE	1.8 V/ 2.85 V	Port/SDRAM clock enable/ chip select 5B	Connect CS (chip select). Fix the unused CS pin to high level.
169	I	CS6IN-N	PTE3/CS6A	1.8 V/ 2.85 V	Port/ chip select 6A	Connect CS (chip select). Fix the unused CS pin to high level.

Table 4.2 Pin Assignments of the Trace Unit Connector (cont)

Pin No.	I/O (CONT)	Connector Pin Name	SH7318 Signal Name	Voltage	Meaning of Signal	Note
170	I	CS7IN-N	PTR6/CS6B/ LCDS2	1.8 V/ 2.85 V	Port/LCD select/ chip select 6B	Connect CS (chip select). Fix the unused CS pin to high level.
171	I	CS8IN-N	N.C.*1			Connect CS (chip select). Fix the unused CS pin to high level.
172	I	CS9IN-N	N.C.*1			Connect CS (chip select). Fix the unused CS pin to high level.
173	O	EM0OUT-N	EM0OUT-N	1.8 V/ 2.85 V	Emulation-memory select output	Connect this signal instead of CS of the MPU when an emulation memory is used.*2
174	O	EM1OUT-N	N.C.*1			
175	O	EM2OUT-N	N.C.*1			
176	O	EMEN-P	N.C.*1			
177	I	UVCC1	Vcc_SL	1.8 V/ 2.85 V	I/O power supply for SRAM interface (1.8 V/ 2.85 V)	Connect the power supply.
178	I	UVCC2	VccQ3	1.8 V	I/O power supply for SDRAM (1.8 V)	Connect the power supply.
179	I	UVCC3	Power supply for user system: 2.85 V	2.85 V	Power supply 2.85 V	Connect the power supply.
180	I	UCNN-N	Connect to user connector	0 V	GND	Connect this signal to GND on the user system.

Notes: 1. Do not connect anything to this pin.
2. Refer to section 4.2.8, Description of Emulation Memory Control Signal.

4.2.6 Layout of the Trace Unit Connector

When designing the user system, there are restrictions on the position to install the trace unit connector. Figure 4.4 shows the external dimensions of the trace unit.

The size of the printed-circuit board of the E200F trace unit is 90 mm × 125 mm. The size of components around the user system connector must not exceed the limit on component installation (the height must be 10 mm or less).

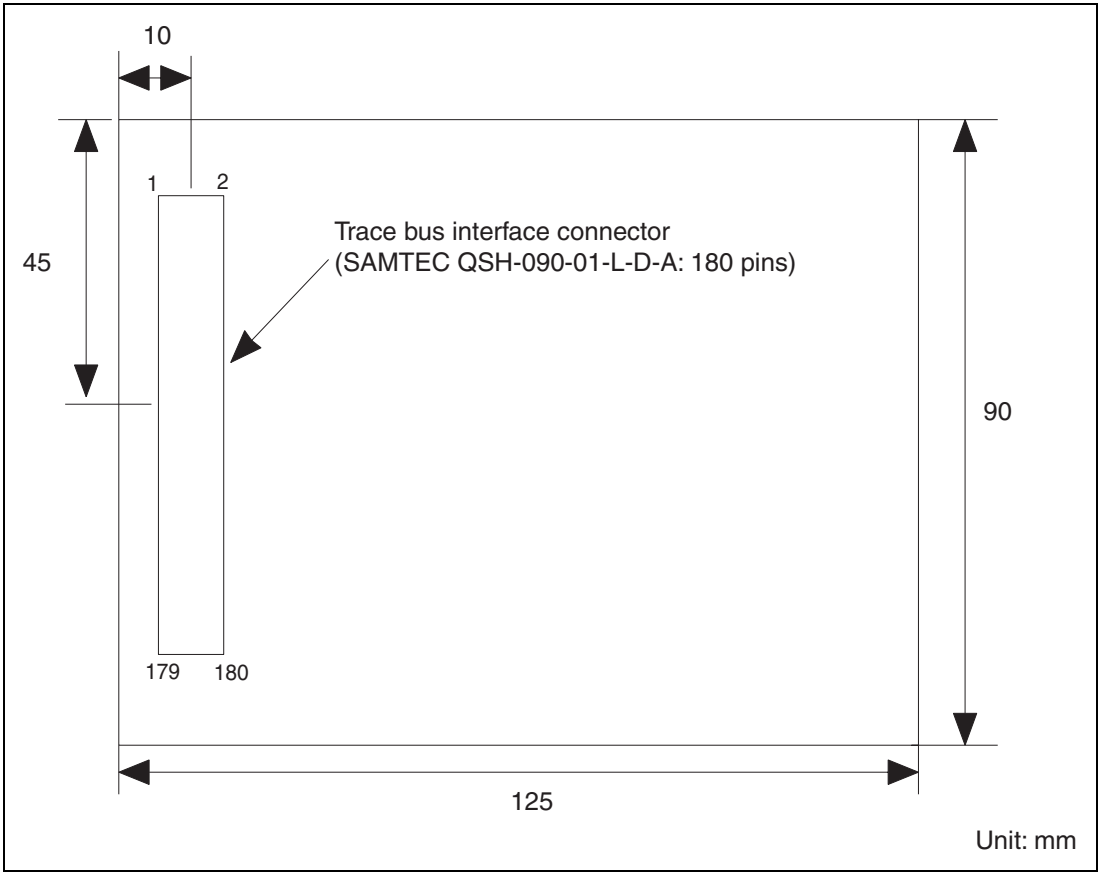


Figure 4.4 External Dimensions of the Trace Unit (on which the Connector is Installed)

Notes: 1. The external bus trace interface connector installed on the user system must be as close to the MPU as possible.

2. Wiring pattern of clock lines (CKO)
   The followings are notes on wiring of clock lines for the E200F trace interface signals. Take them into consideration when designing the user system to embed suitable clock lines.
   (a) Clock lines must be as short as possible.
   (b) Clock lines must be surrounded by the GND pattern for protection so that the signals will be of low-impedance.
   (c) Other layers next to the layer with clock line wiring should have solid patterns of GND/VCC so that the signals will be of low-impedance.
   (d) To prevent affect by the crosstalk noise, other signal patterns must not be embedded along with the clock lines.

4.2.7 Restrictions on Using the Trace Unit

(1) This trace unit supports the external bus memory interfaces of SH7318; SRAM interface, byte-selection SRAM interface (except for SRAM page mode), and SDRAM interface. For burst ROM interface, bus trace acquisition and bus event detection are not supported.

(2) When the sequential trace stop condition or delay-count trace stop condition is specified, trace acquisition will stop after several cycles have been passed from the stop condition match cycle.

(3) During break mode, a timestamp value of the external bus trace information that has been acquired by a trace is not counted up.

(4) In tracing the SDRAM access cycle in area 3, the row-address and column-address output cycles are traced and the trace result of the address bus is displayed. Therefore, if the address bus value is not output as the row address or column address, it will not be correctly displayed by a trace.
Table 4.3 shows areas that the accessed addresses are not correctly displayed by a bus trace.

(5) In tracing the SDRAM burst read cycle in area 3, the LPC3 signal traces the values of LPD31 to LPD0 during assert period. Therefore, the read data for the CAS latency cycle in the last half of the burst read cycle will not be correctly displayed by a trace.

(6) If the SDRAM read access cycle in area 3 occurs immediately before the user program break, the values of LPD31 to LPD0 will not be correctly displayed by a trace.

Table 4.3 Accessing the CS3 Area (16- or 32-bit Bus Width)

				Read/Write Address							
ROW	COL	SDCR (H'FE400008)		H'AC00000	H'ACFFFFFC	H'AD000000	H'ADFFFFFC	H'AE000000	H'AEFFFFFC	H'AF000000	H'AFFFFFFC
12	8	00400808	ROW	0000xxxx	7FFExxxx	0000xxxx	7FFExxxx	0000xxxx	7FFExxxx	0000xxxx	7FFEFFFF
			COL	0400xxxx	7FFExxxx	0400xxxx	7FFExxxx	0400xxxx	7FFExxxx	0400xxxx	7FFEFFFF
			Trace display	0C000000	0CFFFFFC	0C000000	0CFFFFFC	0C000000	0CFFFFFC	0C000000	0CFFFFFC
	9	00408009	ROW	0000xxxx	3FFExxxx	4000FFFF	7FFExxxx	0000xxxx	3FFExxxx	4000xxxx	7FFEFFFF
			COL	0400xxxx	3FFExxxx	4400FFFF	7FFExxxx	0400xxxx	3FFExxxx	4400xxxx	7FFEFFFF
			Trace display	0C000000	0CFFFFFC	0D000000	0DFFFFFC	0C000000	0CFFFFFC	0D000000	0DFFFFFC
13	9	00400811	ROW	0000xxxx	3FFExxxx	4000FFFF	7FFExxxx	0000xxxx	3FFExxxx	4000xxxx	7FFEFFFF
			COL	0400xxxx	3FFExxxx	4400FFFF	7FFExxxx	0400xxxx	3FFExxxx	4400xxxx	7FFEFFFF
			Trace display	0C000000	0CFFFFFC	0D000000	0DFFFFFC	0C000000	0CFFFFFC	0D000000	0DFFFFFC
	10	00400812	ROW	0000xxxx	1FFExxxx	2000FFFF	3FFExxxx	4000xxxx	5FFExxxx	6000FFFF	7FFExxxx
			COL	0400xxxx	1FFExxxx	2400FFFF	3FFExxxx	4400xxxx	5FFExxxx	6400FFFF	7FFExxxx
			Trace display	0C000000	0CFFF7FC	0D000000	0DFFF7FC	0E000000	0EFFF7FC	0F000000	0FFFF7FC

Note: : The accessed addresses are not correctly displayed by a bus trace.

(7) When an emulation memory is used, it is not possible to access the memory on the user system which is in the same area as an area where the emulation memory has been set.

(8) When an emulation memory is accessed, at least six wait cycles are required. Set the number of wait cycles by using bits WR3 to WR0 in the CS0 area wait control register (CS0WCR).

(9) The CKO pin of the SH7318 is multiplexed with PTR3 or A25. Be sure to select the CKO function with the pin function controller when the trace unit is used. The trace unit operates only when the CKO output is selected. The CKO function is set as follows:
- Set '00' for PSC13 (bit 13) in the pin select register C (H'A4050144) and select CKO.
- Set '00' for PR3MD0 and PR3MD1 bits in the port R control register (H'A405011E) and select [Other functions].

(10) The emulator occupies the CS0 area where the emulation memory has been set. Accordingly, it is not possible to access the memory in the user system side of that area.

(11) This trace unit is available for the external 8- or 16-bit data bus width. When the data bus width is 8 bits, unused data bus pins D15 to D8 of the trace unit connector must be fixed to high or low level. In addition, when area 0 is used with the emulation memory, the bus width of the emulation memory needs to be set. For details, refer to section 5.1.8, Changing the Memory Map Setting, in the SH-4A, SH4AL-DSP E200F Emulator User's Manual.

4.2.8 Description of Emulation Memory Control Signal

When the CS signal of the MPU is connected directly to the memory or used to generate the CS signal of the memory, connect the EM0OUT-N signal (pin 173) of the external bus connector instead of the CS signal of the MPU.

Even if the emulator is not used, prepare the jumper pins as shown in figure 4.5 so that connection of the CS signal can be easily changed.

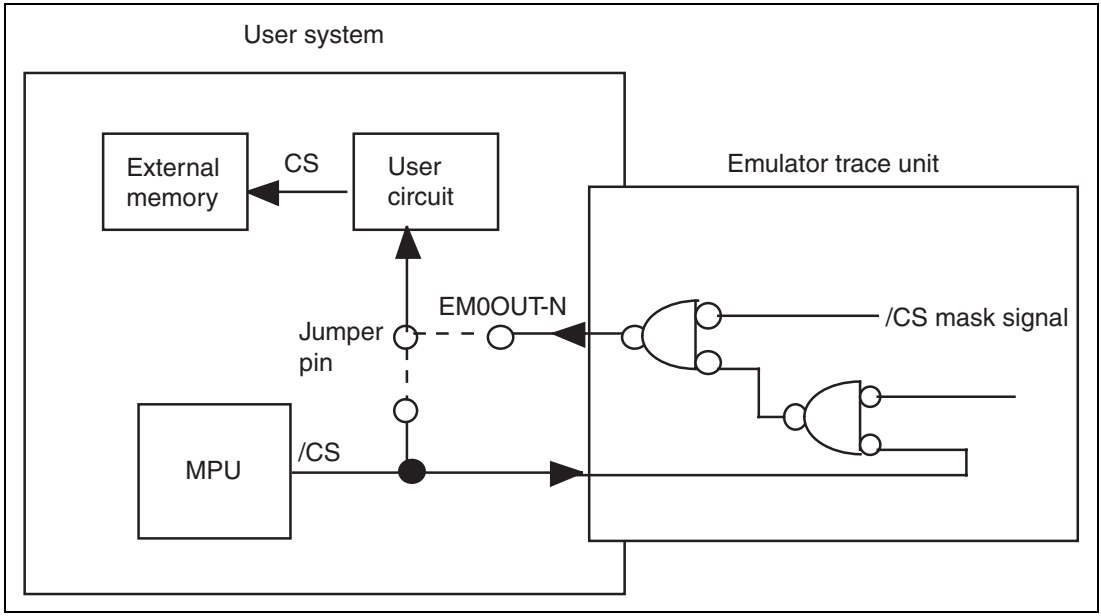


Figure 4.5 EM0OUT-N Signal (Pin 173)

SH-4A, SH4AL-DSP E200F Emulator
Additional Document for User's Manual
Supplementary Information on Using the SH7318

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