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USER'S MANUAL

μPD4990A

SERIAL I/O REAL TIME CLOCK IC

Document No. IEU-1210 (1st edition)
Date Published March 1997 P
Printed in Japan

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CHAPTER 1 INTRODUCTION

The μPD4990A is a CMOS LSI developed to input/output calendar and clock data serially to/from the micro-computer system.

The including data items are hour, minute, second, year, month, day, and day of week.

Data format is BCD except month. Data format of month is hexadecimal (1 ~ 0 CH).

The μPD4990A is useful for personal computer, electronic cash register, photo-copier, facsimile etc. what require calendar and clock data.

1.1 FEATURE

(1) Calendar (year, month, day, day of week) & clock (hour, minute, second) data.

(2) Leap years are determined automatically.

(3) Data format is BCD (only month is hexadecimal).

(4) TP output selectable
Timing pulse is 64, 256, 2048 or 4096 Hz
Interval timer is 1, 10, 30 or 60 sec.

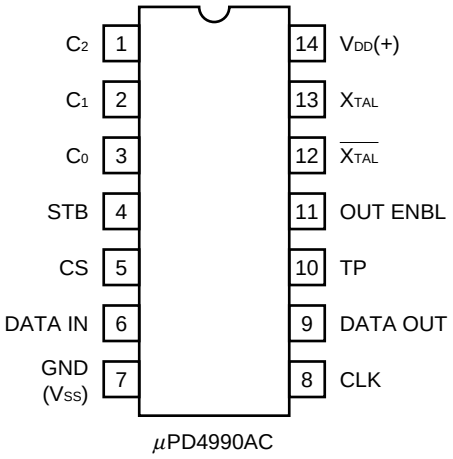
(5) Wide operating supply voltage 2.0 – 5.5 V
The μPD4990A can use dry battery, N_i-C_d battery etc.

(6) Data input/output is serially by external clock.

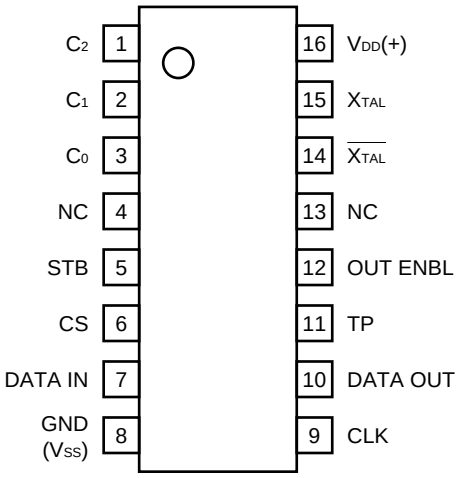
(7) The crystal frequency is 32.768 kHz

(8) CMOS structure

1.2 PIN CONNECTION DIAGRAM (Top View)



μPD4990AC



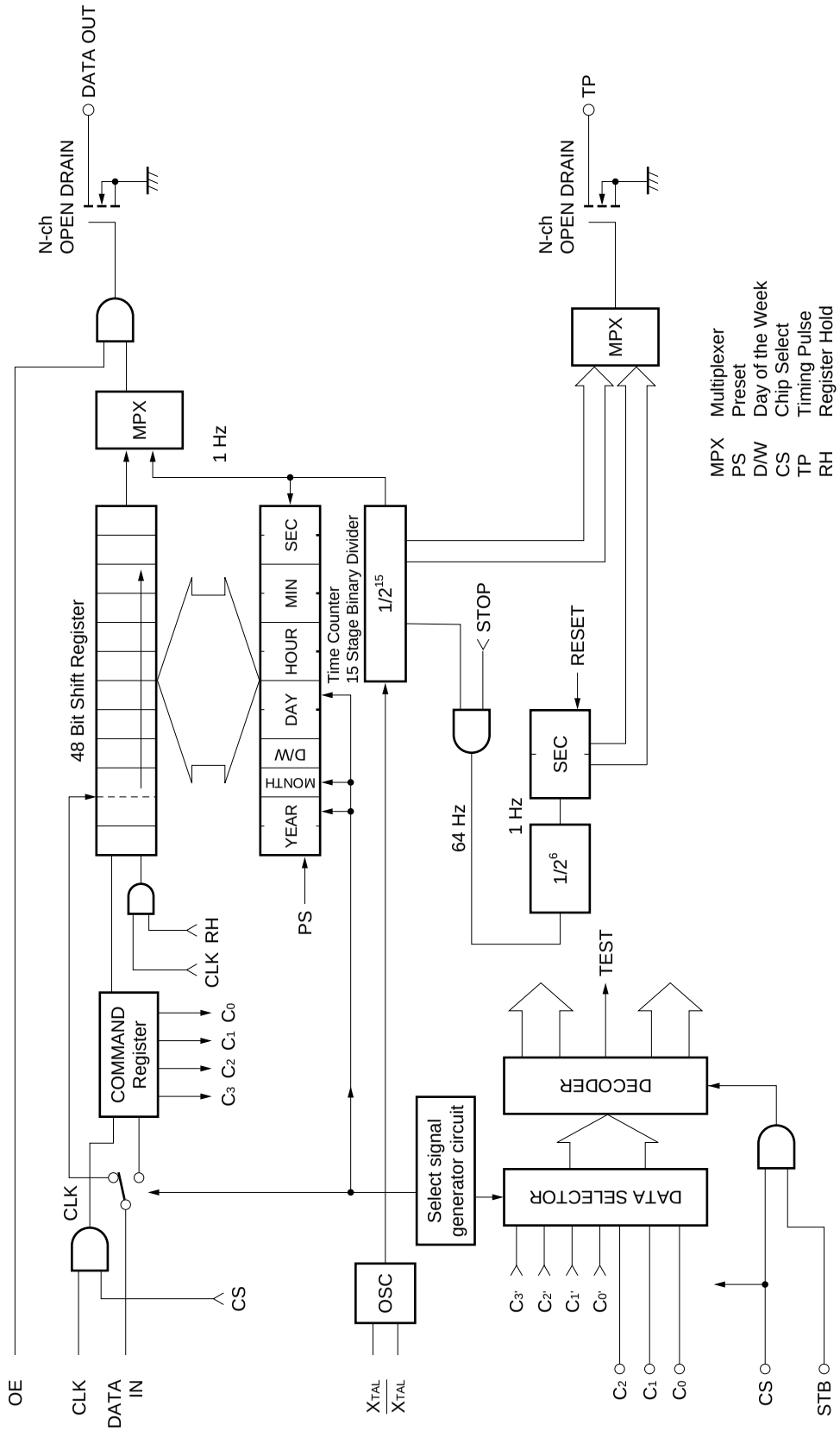
μPD4990AG

1.3 PIN FUNCTION

SYMBOL	PIN NAME	PIN No. DIP/SOP	FUNCTION
DATA IN	DATA INPUT	6/7	Input of 40/52 bit Shift Register
CLK	CLOCK INPUT	8/9	Data is shifted on positive edge of CLK.
C_0	COMMAND INPUT	3/3	Parallel command input
C_1		2/2	
C_2		1/1	
STB	LATCH STROBE	4/5	μPD4990A load command to command register when STB is high.
CS	CHIP SELECT	5/6	CLK and STB are enable while CS is high.
OUT ENBL	OUTPUT ENABLE	11/12	DATA OUT is enable while OUT ENBL is high. DATA OUT is high impedance while OUT ENBL is low.*
TP	TIMING PULSE	10/11	Output of interval timer or timing pulse (Nch Open Drain)
X_{TAL}	Crystal	13/15	Oscillator input
$\overline{X_{TAL}}$		12/14	Oscillator output

***NOTE**: DATA OUT is not high impedance while μPD4990A is Test mode. Please confirm “2.2.2 Parallel command mode. (7) Test command.”

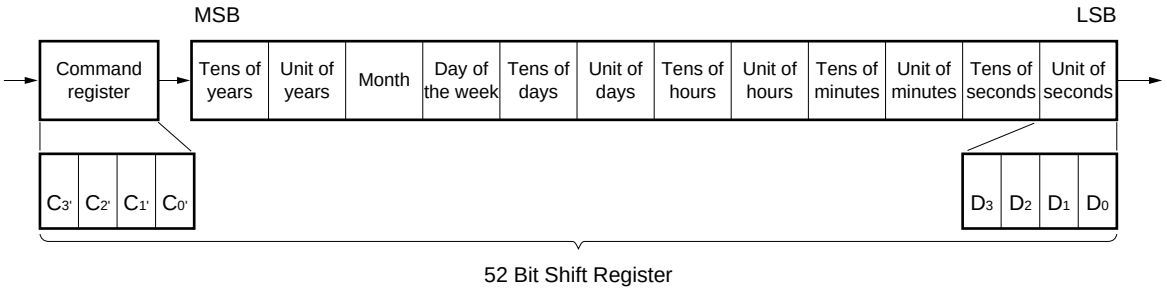
1.4 BLOCK DIAGRAM



1.5 SHIFT REGISTER

The register of μPD4990A consists of 4 bit register that read command and 48 bit register that input/output data. Total bit of register is 52 bit.

Fig. 1-1 52 bit Shift Register



* DATA of 52 Bit Shift Register appears on DATA OUT terminal from LSB of second.

Table 1-1 48 bit Shift Register Construction

Counter	48 bit Shift Register	Location of Shift Register	Value of Time Counter	Counter	48 bit Shift Register	Location of Shift Register	Value of Time Counter
	B0	D0			B24	D24	
Units	B1	D1	0 ~ 9	Units	B25	D25	0 ~ 9
second	B2	D2	(BCD)	day	B26	D26	(BCD)
	B3	D3			B27	D27	
	B4	D4			B28	D28	
Tens	B5	D5	0 ~ 5	Tens	B29	D29	0 ~ 3
second	B6	D6	(BCD)	day	B30	D30	(BCD)
	B7	D7			B31	D31	
	B8	D8			B32	D32	
Units	B9	D9	0 ~ 9	Day of	B33	D33	0 ~ 6*
minute	B10	D10	(BCD)	week	B34	D34	(BCD)
	B11	D11			B35	D35	
	B12	D12			B36	D36	
Tens	B13	D13	0 ~ 5	Month	B37	D37	1 ~ C
minute	B14	D14	(BCD)		B38	D38	(Hexadecimal)
	B15	D15			B39	D39	
	B16	D16			B40	D40	
Units	B17	D17	0 ~ 9	Units	B41	D41	0 ~ 9
hour	B18	D18	(BCD)	year	B42	D42	(BCD)
	B19	D19			B43	D43	
	B20	D20			B44	D44	
Tens	B21	D21	0 ~ 2	Tens	B45	D45	0 ~ 9
hour	B22	D22	(BCD)	year	B46	D46	(BCD)
	B23	D23			B47	D47	

***Note**: The relationship of day of week counter and day of week is free. For example, if Sunday is “0”. Monday is “1”, ..., and Saturday is “6”.

1.6 TIME COUNTER

Count clock and calendar

This part is able to transfer data to/from 48 bit shift register.

1.7 15 STAGES DIVIDER

This part divides clock from oscillator and supplies 1 Hz to time counter.

1.8 DATA INPUT/OUTPUT

Start bit of shift register is units of seconds LSB (B_0).

B_{40} ~ B_{47} of 48 bit shift register are enable on serial command mode. Please confirm "2.2 COMMAND SPECIFICATION."

Fig. 1-2 Data INPUT/OUTPUT

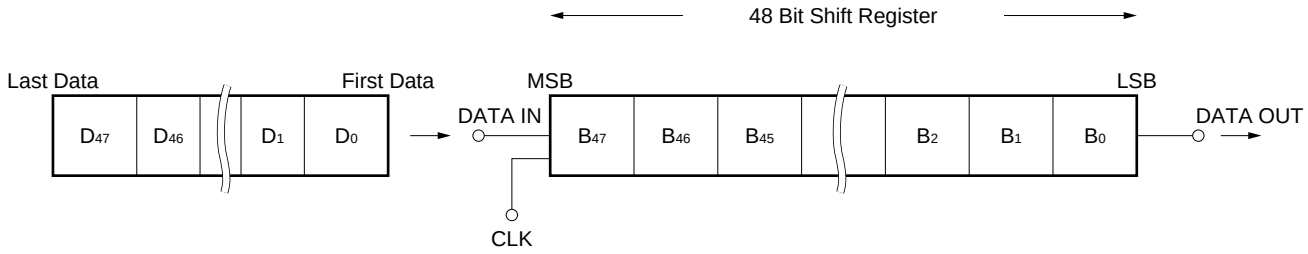


Fig. 1-3 Data Write Action

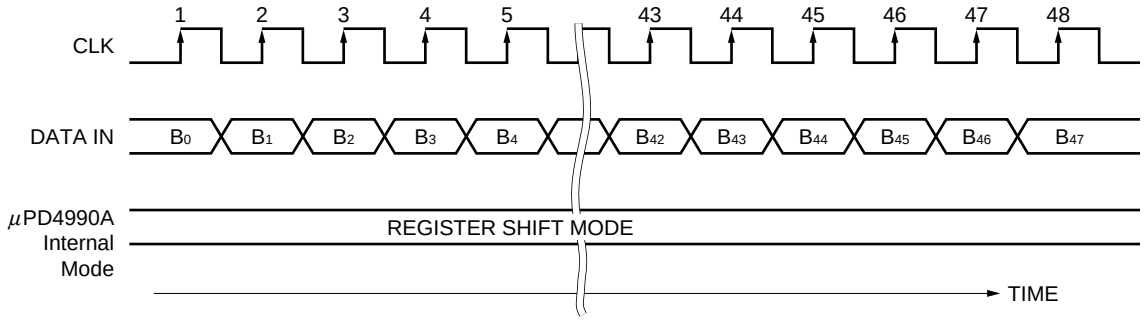
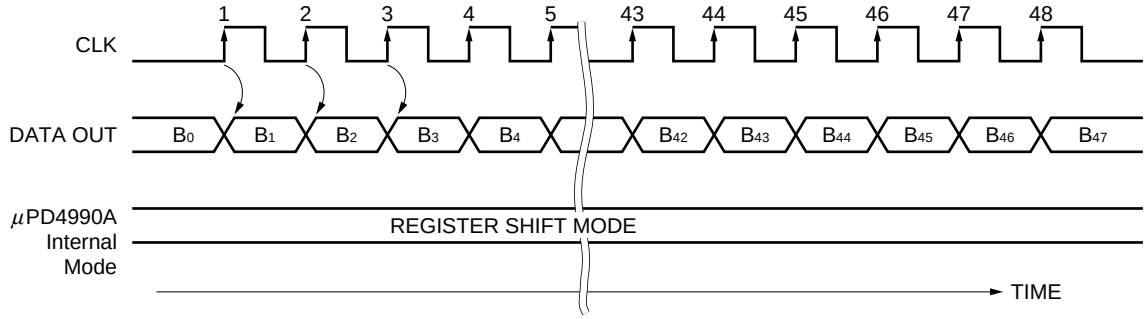


Fig. 1-4 Data Read Action



[MEMO]

CHAPTER 2 FUNCTION SPECIFICATION

2.1 COMMAND SETTING

The μPD4990A has parallel command mode using C_0, C_1, C_2 and serial command mode transferring data serially.

2.1.1 Parallel Command Mode

C_0, C_1 and C_2 are used on this mode. This mode is compatible μPD1990A except TEST COMMAND (C_0, C_1, C_2 = 1, 1, 1). Same software for μPD1990A can be used for μPD4990A except TEST COMMAND. But this mode has not year count, leap year and interval timer. Please show Table 2-1, Fig. 2-1.

2.1.2 Serial Command Mode

While C_0, C_1, and C_2 is high, command is set serially to DATA IN.

Command is consist of 4 bit. Command is transferred from C_0' (LSB) to C_3' by positive edge of CLK, and while STB is high, μPD4990A read command. When STB is low, μPD4990A latches command. This mode has year count, leap year, timing pulse, and interval timer.

Table 2-1 Parallel Command

- Commands input from C_0, C_1, and C_2 terminals (1 ... H, 0 ... L)
  Shift register 40 bit (The year function is ineffective.)
  (Operates as the existing μPD1990AC in other than test mode)

C_2	C_1	C_0	FUNCTION	
0	0	0	REGISTER HOLD	DATA OUT = 1 Hz
0	0	1	REGISTER SHIFT	DATA OUT = [LSB] = 0 or 1
0	1	0	TIME SET & COUNTER HOLD	DATA OUT = [LSB] = 0 or 1
0	1	1	TIME READ	DATA OUT = 1 Hz
1	0	0	TP = 64 Hz	
1	0	1	TP = 256 Hz	
1	1	0	TP = 2048 Hz	
1	1	1	SERIAL COMMAND TRANSFER MODE	

* The test mode is cancelled by [C_2, C_1, C_0] = [0, 0, 0] to [1, 1, 0]

Table 2-2 Serial Command

- Serial data commands
  Set [C_2, C_1, C_0] = [1, 1, 1] at all time
  Shift register 52 bit (The year function is effective.)

C_3'	C_2'	C_1'	C_0'	FUNCTION	
0	0	0	0	REGISTER HOLD	DATA OUT = 1 Hz
0	0	0	1	REGISTER SHIFT	DATA OUT = [LSB] = 0 or 1
0	0	1	0	TIME SET & COUNTER HOLD	DATA OUT = [LSB] = 0 or 1
0	0	1	1	TIME READ	DATA OUT = 1 Hz
0	1	0	0	TP = 64 Hz	
0	1	0	1	TP = 256 Hz	
0	1	1	0	TP = 2048 Hz	
0	1	1	1	TP = 4096 Hz	
1	0	0	0	TP = 1 s INTERVAL SET (COUNTER RESET & START)	
1	0	0	1	TP = 10 s INTERVAL SET (COUNTER RESET & START)	
1	0	1	0	TP = 30 s INTERVAL SET (COUNTER RESET & START)	
1	0	1	1	TP = 60 s INTERVAL SET (COUNTER RESET & START)	
1	1	0	0	INTERVAL RESET	
1	1	0	1	INTERVAL START	
1	1	1	0	INTERVAL STOP	
1	1	1	1	TEST MODE SET	

Remark: TEST MODE is cancelled by (C_3', C_2', C_1', C_0') = (0, 0, 0, 0), (0, 1, 0, 0) to (1, 1, 1, 0).

2.1.3 Caution of Command Setting

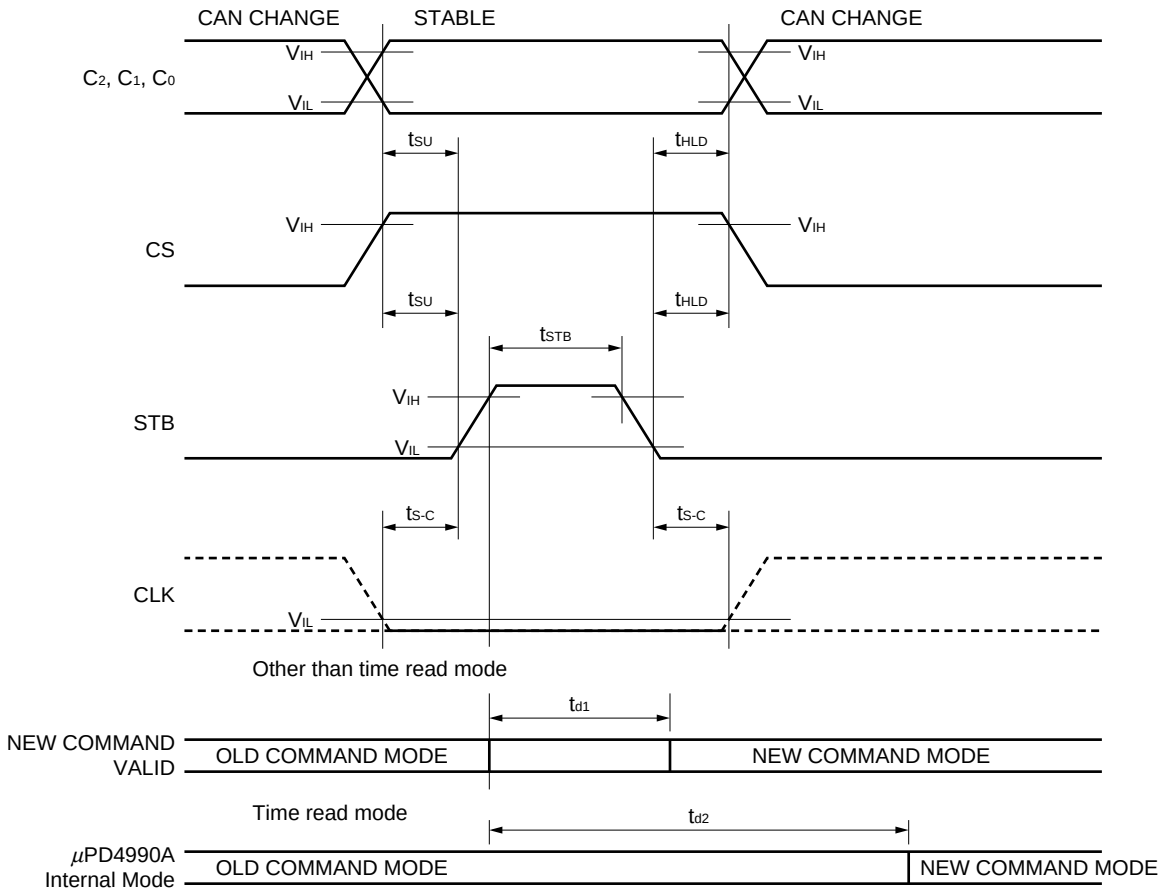
After μPD4990A reads command (STB is L to H), Internal mode of μPD4990A becomes new mode. This delay time is STB LATCH Delay time (t_{d1}, t_{d2}). Please wait t_{d1} before setting new command. But STB LATCH Delay time (t_{d2}) after TIME READ COMMAND is 20 μs min. For example, if REGISTER SHIFT COMMAND is set, after TIME READ COMMAND, wait 20 μs min. before transferring data.

Please see Fig. 2-1, Fig. 2-2.

Fig. 2-1 is Parallel command timing chart.

Fig. 2-2 is Serial command timing chart.

Fig. 2-1 Parallel Command Timing (C_0, C_1, C_2)

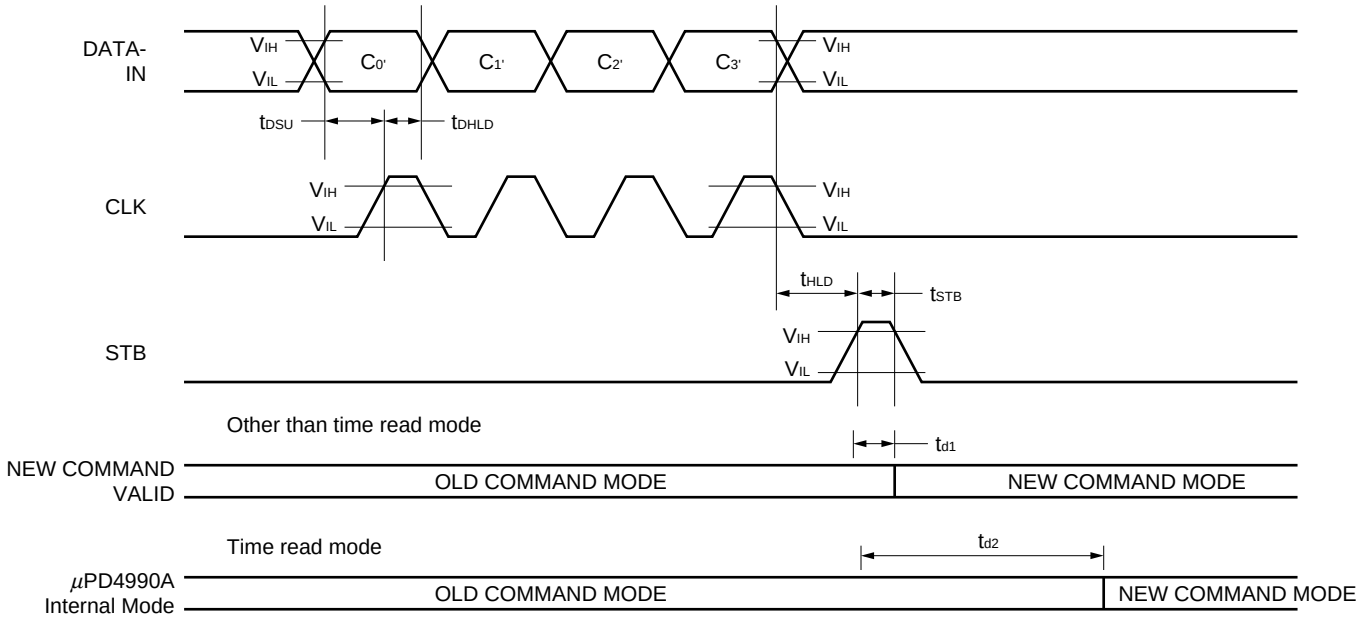


V_{DD}-V_{SS} = 2.0 V

t_{SU}	= 1 μs MIN.
t_{HLD}	= 1 μs MIN.
t_{STB}	= 1 μs MIN.
t_{d1}	= 1 μs MAX. (Other than time read mode)
t_{d2}	= 20 μs MAX. (Time read mode)
t_{S-C}	= 1 μs MIN.

Note: A mode is latched by STB and held until another mode in the same group is set.

Fig. 2-2 Serial Command Timing (C_0', C_1', C_2', C_3')



V_{DD}-V_{SS} = 2.0 V

t_{DSU}	= 1 μs MIN.
t_{DHLD}	= 1 μs MIN.
t_{HLD}	= 1 μs MIN.
t_{STB}	= 1 μs MIN.
t_{d1}	= 1 μs MAX. (Other than time read mode)
t_{d2}	= 20 μs MAX. (Time read mode)

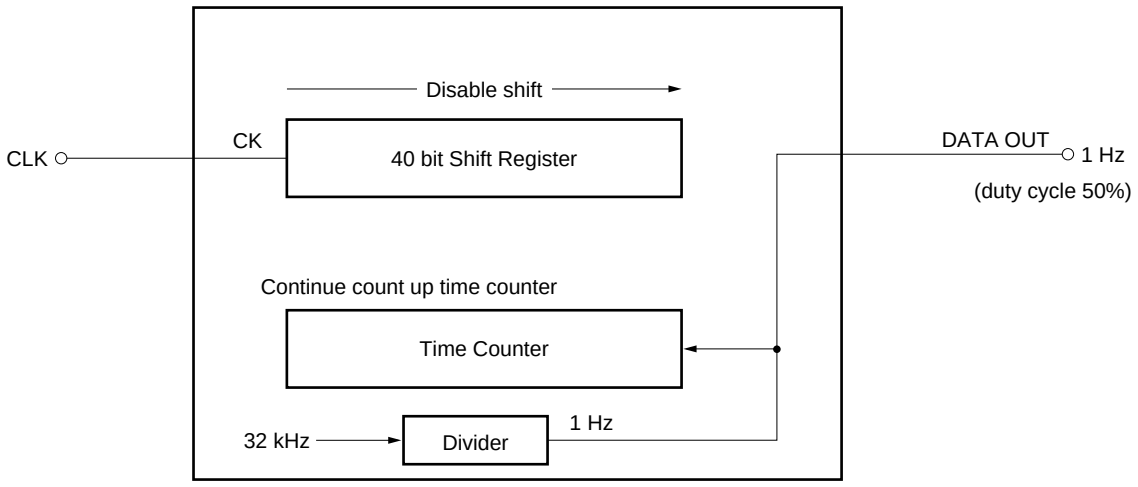
Note: Command (C_2, C_1, C_0) is held (1, 1, 1) at all time.
CS = “H”
A mode is latched by STB and held until another mode in the same group is set.

2.2 COMMAND SPECIFICATION

2.2.1 Parallel Command Mode

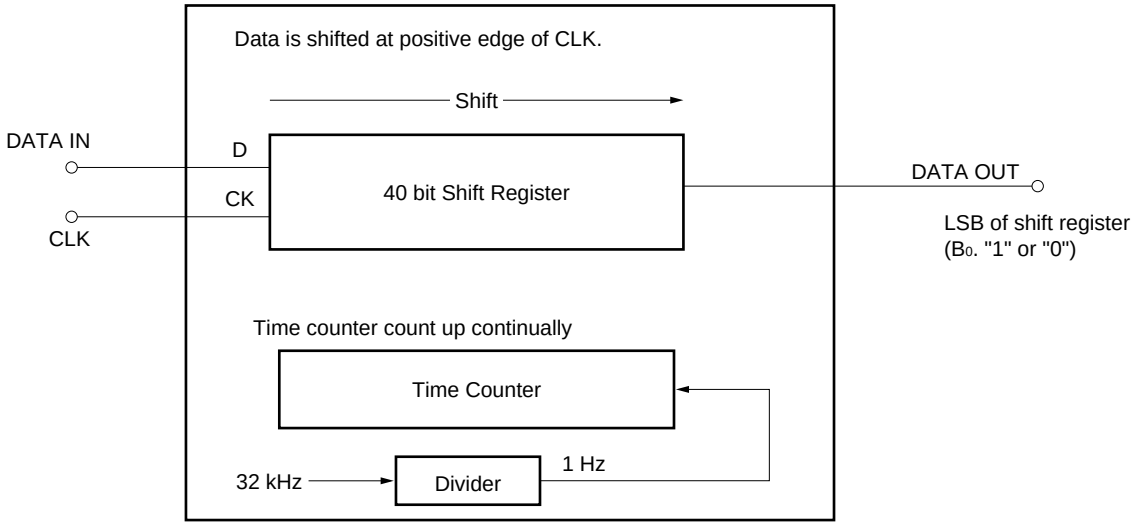
(1) REGISTER HOLD COMMAND (C_2, C_1, C_0 = 0, 0, 0)

The 40 bit shift register is held. If CLK is entered, Data doesn't shift. 1 Hz (Duty = 50 %) appears to DATA OUT and 64 Hz appeares to TP. If μPD4990A's mode is TEST MODE, TEST MODE is canceled when REGISTER SHIFT COMMAND is read.



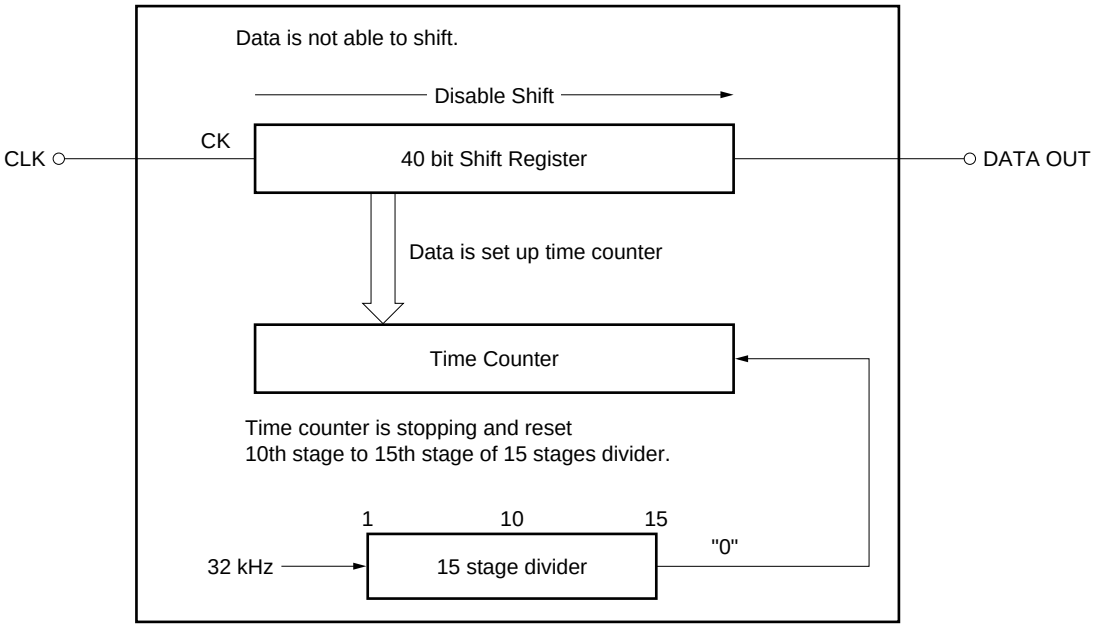
(2) REGISTER SHIFT COMMAND (C_2, C_1, C_0 = 0, 0, 1)

It is able to shift data of 40 bit shift register. Data of DATA IN is loaded to shift register at positive edge of CLK. B_1 of shift register is shifted to B_0 and appeares to DATA OUT.



(3) TIME SET & COUNTER HOLD COMMAND (C_2, C_1, C_0 = 0, 1, 0)

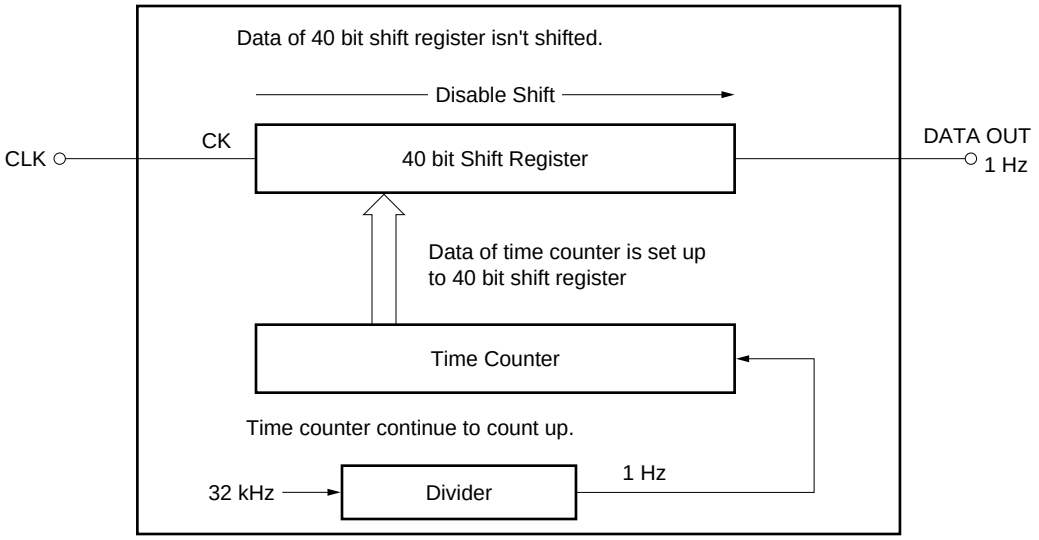
Data of 40 bit shift register is set up time counter and 10th stage to 15th stage of 15 stages divider are reset. After command is read, data of 40 bit shift register doesn't shift and time counter is stopping. Time counter begin to count up when next command is read. The error of setting up is ±15.625 ms.* LSB of 40 bit shift register (B_0) appears to DATA OUT.



* In case of μPD1990A, the error of setting up is ±31.25 ms.

(4) TIME READ COMMAND (C_2, C_1, C_0 = 0, 1, 1)

Data of time counter is transferred to 40 bit shift register. Data is fixed when next command is read. 40 bit shift register is held, and 1 Hz* (Duty = 50 %) appeares to DATA OUT.



* 0.5 Hz appeares in case of μPD1990A.

(5) TIMING PULSE CONTROL COMMAND

It can be selected TP frequency, 64 Hz, 256 Hz, or 2048 Hz appeares to TP.

Table 2-3 Timing Pulse Control Command

TP Frequency	Function	C_2, C_1, C_0
64 Hz	Output 64 Hz TP	1, 0, 0
256 Hz	Output 256 Hz TP	1, 0, 1
2048 Hz	Output 2048 Hz TP	1, 1, 0

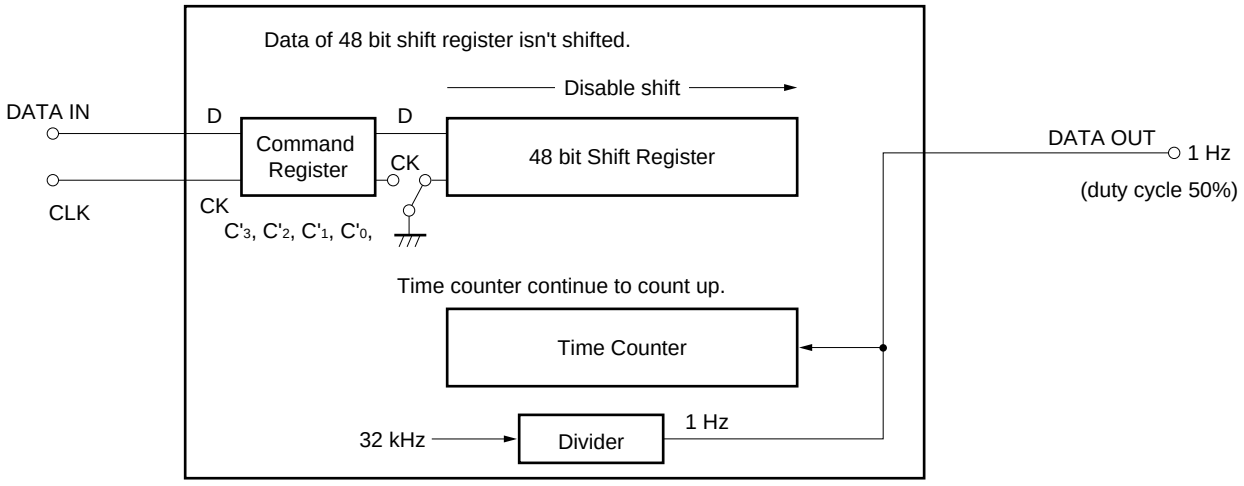
If REGISTER HOLD COMMAND is read, then TP forcibly is 64 Hz Output.

2.2.2 Serial Command Mode

(1) REGISTER HOLD COMMAND (C_3', C_2', C_1', C_0', = 0, 0, 0, 0)

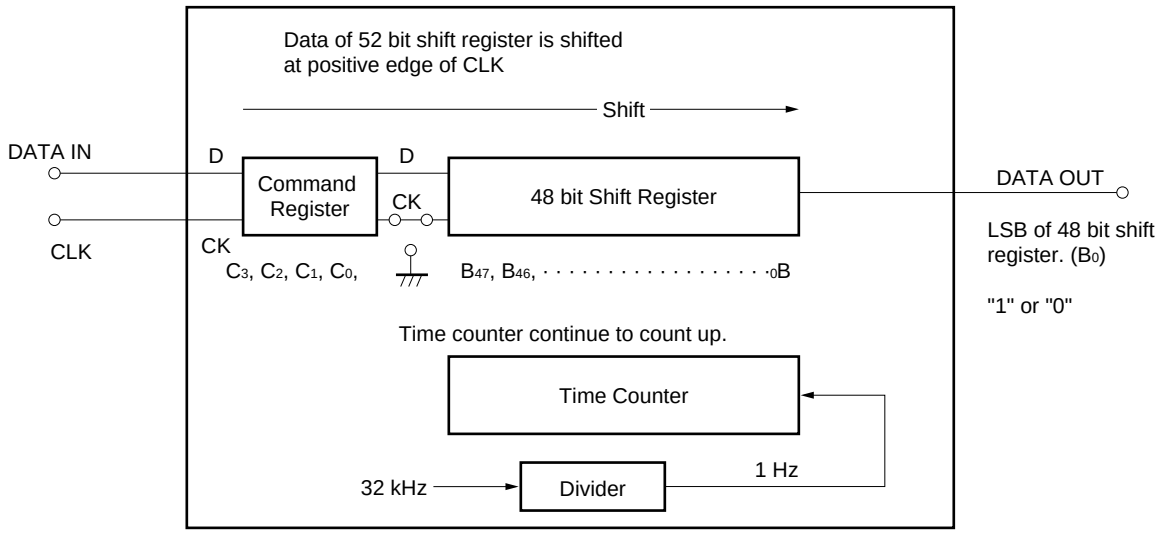
48 bit shift register is held. If CLK is entered, Data of DATA IN is read to C_3' of command register and data of command register is shifted.

1 Hz appeares to DATA OUT and 64 Hz appeares to TP. If μPD4990A's mode is TEST MODE, TEST MODE is canceled when REGISTER HOLD COMMAND is read.



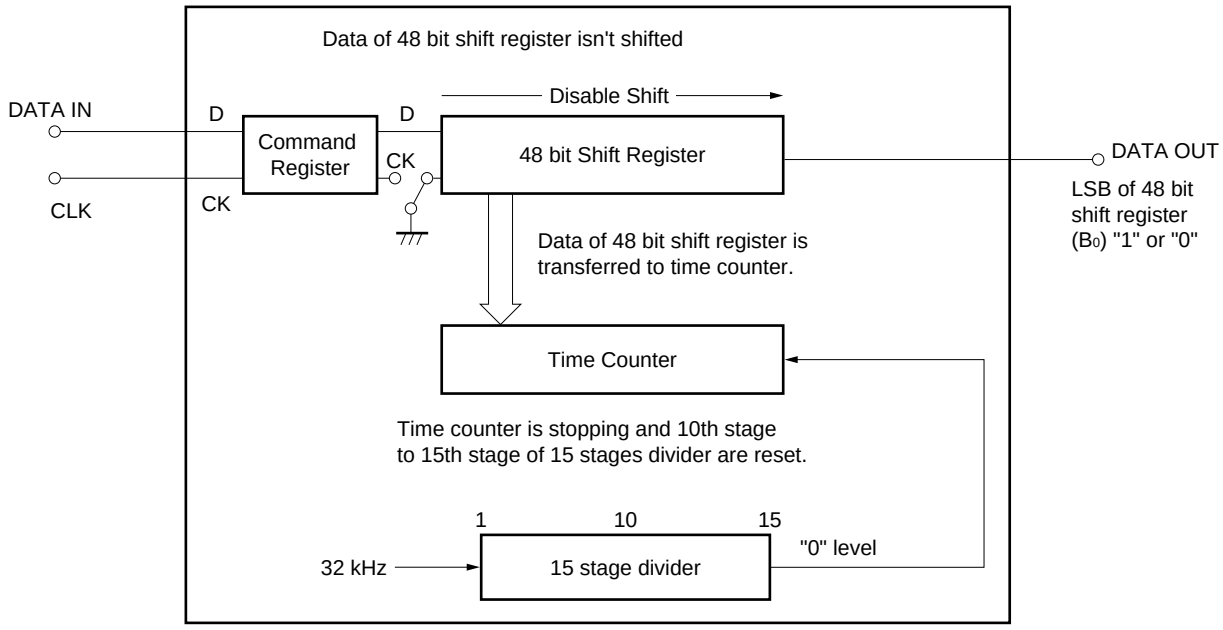
(2) REGISTER SHIFT COMMAND (C_3', C_2', C_1', C_0' = 0, 0, 0, 1)

Data of 48 bit shift register and 4 bit command register is equal 52 bit shift register C_0' of command register is connected input of 48 bit shift register. Data of DATA IN is read at positive edge of CLK and LSB of 48 bit shift register (B_0) appeares to DATA OUT.



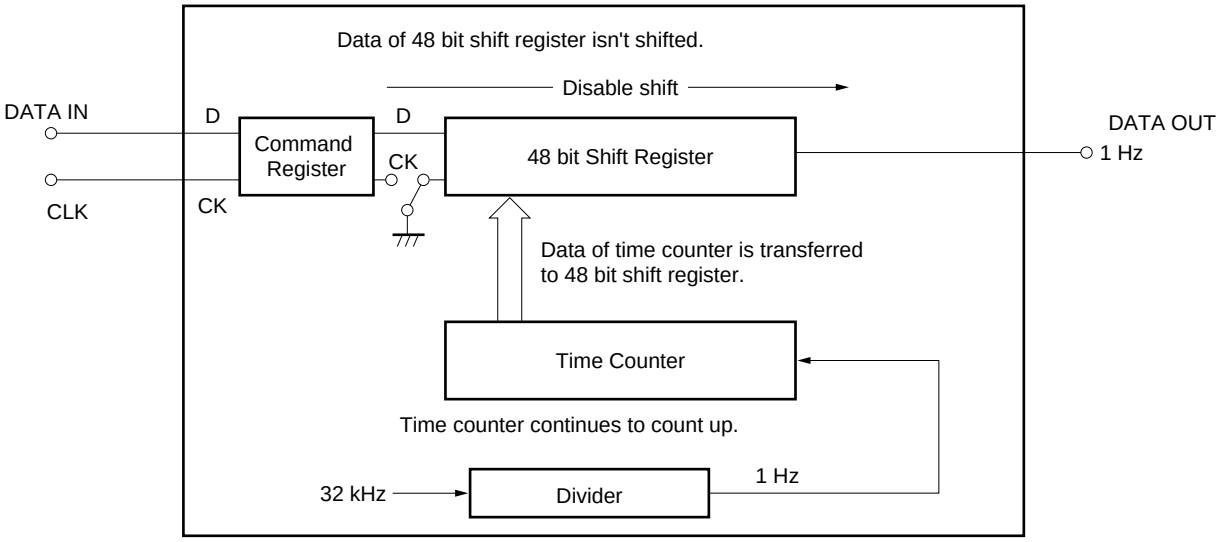
(3) TIME SET & COUNTER HOLD COMMANDS (C_3', C_2', C_1', C_0' = 0, 0, 1, 0)

Data of 48 bit shift register is set up to time counter, and 10th stage to 15th stage of 15 stages divider are reset. After command is read, shift register is held and time counter is stopping. Time counter begin to count up after next command is read. And the error of setting up is ±15.625 ms. LSB of 48 bit shift register (B_0) appeares to DATA OUT.



(4) TIME READ COMMAND (C_3', C_2', C_1', C_0' = 0, 0, 1, 1)

Data of time counter is transferred to 48 bit shift register. Data of shift register is fixed after next command is read. After this command is read. 48 bit shift register is held. 1 Hz appeares to DATA OUT.



(5) TIMING PULSE CONTROL COMMAND

It can be selected TP frequency. 64 Hz, 256 Hz, 2048 Hz, or 4096 Hz appeares to TP.

Table 2-4 Timing Pulse Control Command

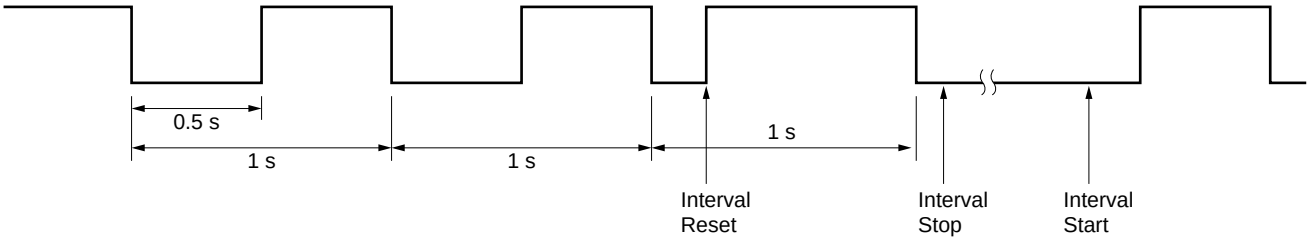
Command name	Function	C_3', C_2', C_1', C_0'
TP64	Output of 64 Hz timing pulse	0, 1, 0, 0
TP256	Output of 256 Hz timing pulse	0, 1, 0, 1
TP2048	Output of 2048 Hz timing pulse	0, 1, 1, 0
TP4096	Output of 4096 Hz timing pulse	0, 1, 1, 1

(6) INTERVAL TIMER CONTROL COMMAND

It can be selected interval timer period and interval timer stop, reset or start. The setting error of interval timer is ±15.625 ms.

Command name	Function	C_3', C_2', C_1', C_0'
INT 1 s INT 10 s INT 30 s INT 60 s	Output of 1 sec interval timer Output of 10 sec interval timer Output of 30 sec interval timer Output of 60 sec interval timer	1, 0, 0, 0 1, 0, 0, 1 1, 0, 1, 0 1, 0, 1, 1
Interval Reset	Interval timer is reset. (TP output is high impedance)	1, 1, 0, 0
Interval Start	Interval timer is started (Timer isn't reset.)	1, 1, 0, 1
Interval Stop	Interval timer is stopped. (TP output status is continued.)	1, 1, 1, 0

For example (INT 1 s)



Note: After REGISTER HOLD COMMAND is read, Timing pulse of 64 Hz forcibly appeares to TP.

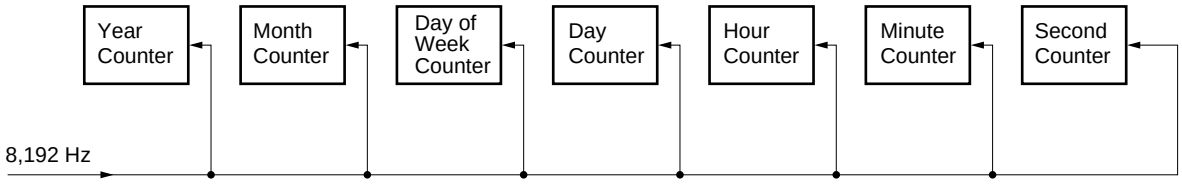
(7) TEST COMMAND (TEST MODE)

Time counter is input 8 192 Hz*. So time counter count up at 8 192 times speed. TEST MODE has two mode. While OUT ENBL is low, μPD4990A is operated TEST MODE 1. While OUT ENBL is high, μPD4990A is operated TEST MODE 2. TEST MODE is canceled after REGISTER HOLD COMMAND is read.

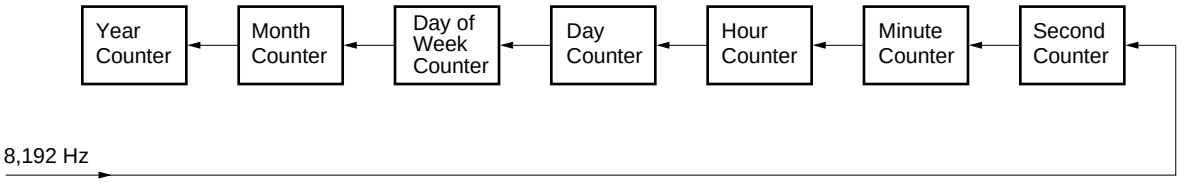
***Note.** μPD1990A is 1024 Hz.

- TEST MODE 1 (OUT ENBL = L)

  Each counters (sec, min, hour, day, day of week, month, year) are entered 8 192 Hz. Carry of counter isn't transferred to next counter.



- TEST MODE 2 (OUT ENBL = H)
  Second counter is entered 8 192 Hz. Carry of counter is transferred to next counter.



COMMAND	DATA OUT	TP	NOTE	
REGISTER HOLD	1 Hz	64 Hz	TEST MODE is canceled.	
REGISTER SHIFT	SHIFT REGISTER [LSB]	32 Hz	TEST MODE	TIME COUNTER 8 192 Hz Enter
TIME SET	SHIFT REGISTER [LSB]	L Level		
TIME READ	1 Hz	32 Hz		TIME COUNTER 8 192 Hz Enter

When REGISTER HOLD COMMAND is read, TEST MODE is canceled and timing pulse of 64 Hz appeares to TP. Command before TEST COMMAND should be REGISTER SHIFT COMMAND. In case of REGISTER HOLD COMMAND, TEST COMMAND is canceled.

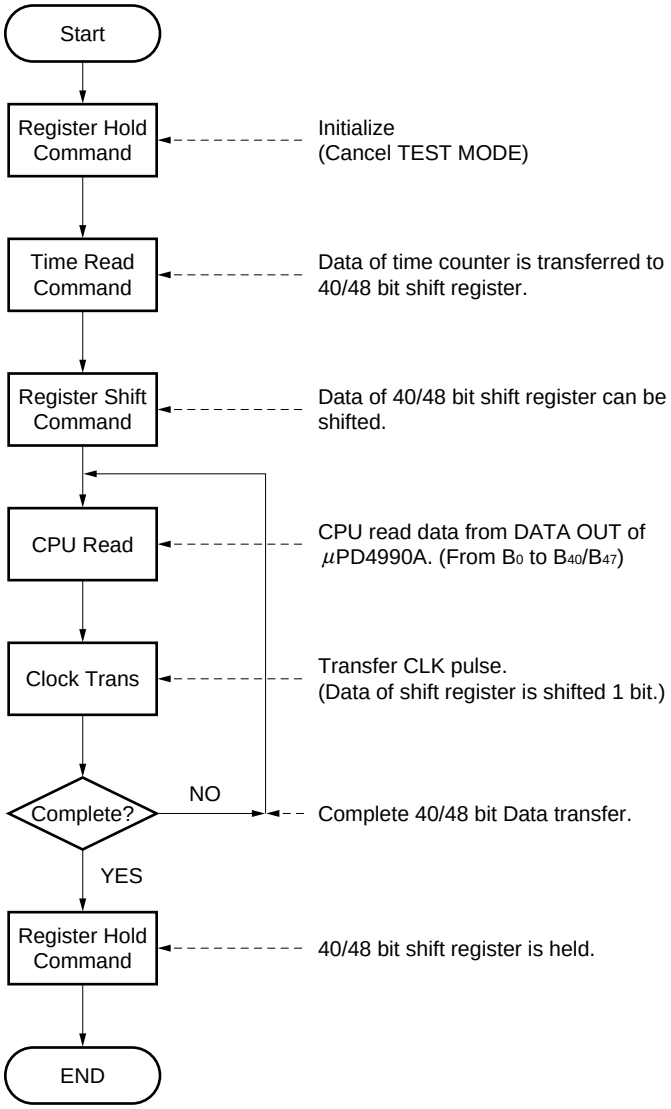
[MEMO]

CHAPTER 3 ACCESS SEQUENCE

3.1 HOW TO READ DATA OF CLOCK

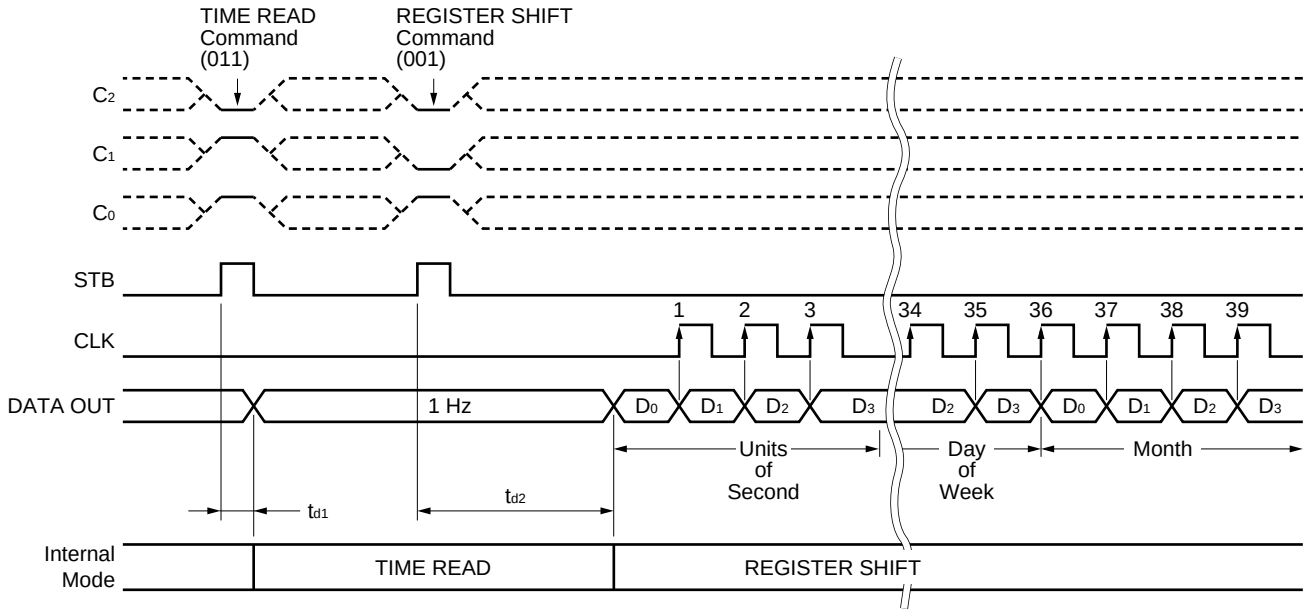
This section shows how to read data of clock using flow chart and timing-chart.

Fig. 3-1 Read Data Flow-chart



(1) Parallel Command Mode

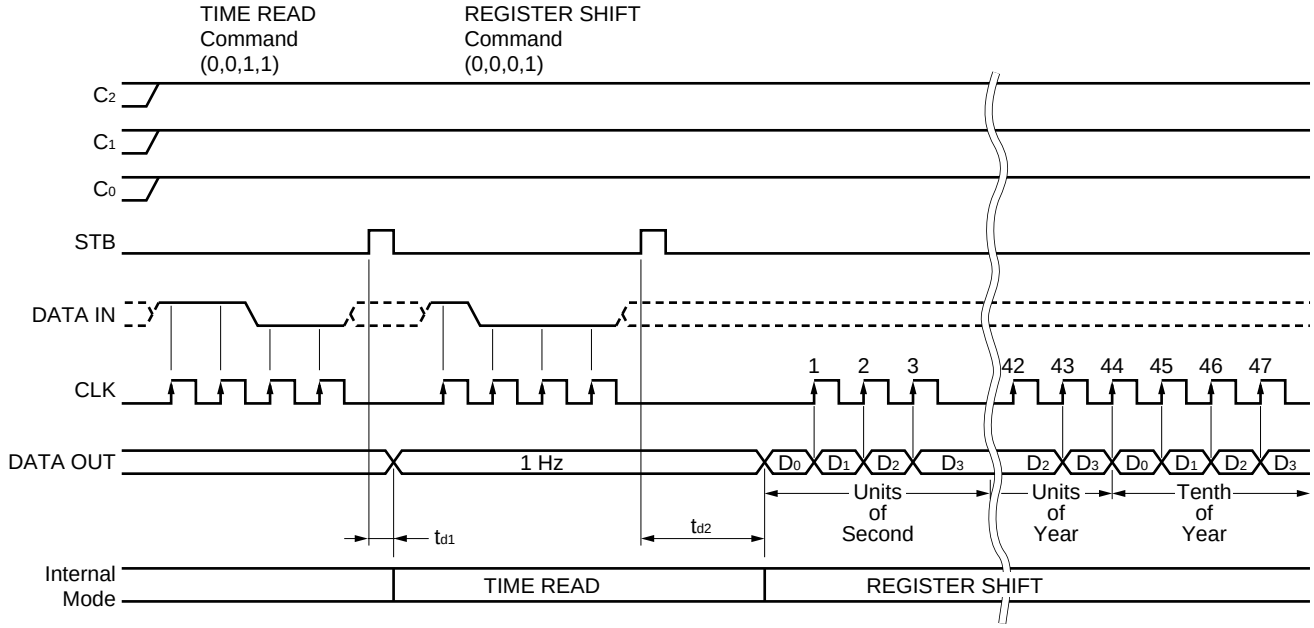
Fig. 3-2 Read Data Timing-chart (Using C_0, C_1, C_2)



Note: t_{d1} = 1 μs MAX. (Normal)
t_{d2} = 20 μs MAX. (After 'TIME READ')

(2) Serial Command Mode

Fig. 3-3 Read Data Timing-chart (Using C_0', C_1', C_2', C_3')

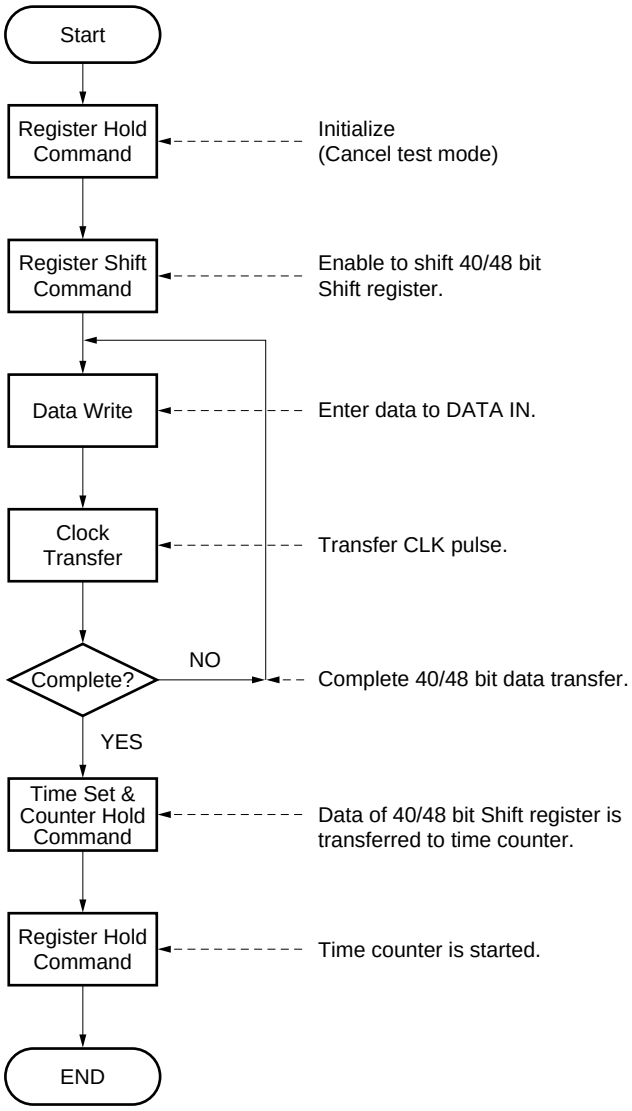


Note: t_{d1} = 1 μs MAX. (Normal)
t_{d2} = 20 μs MAX. (After 'TIME READ')

3.2 HOW TO WRITE DATA OF CLOCK

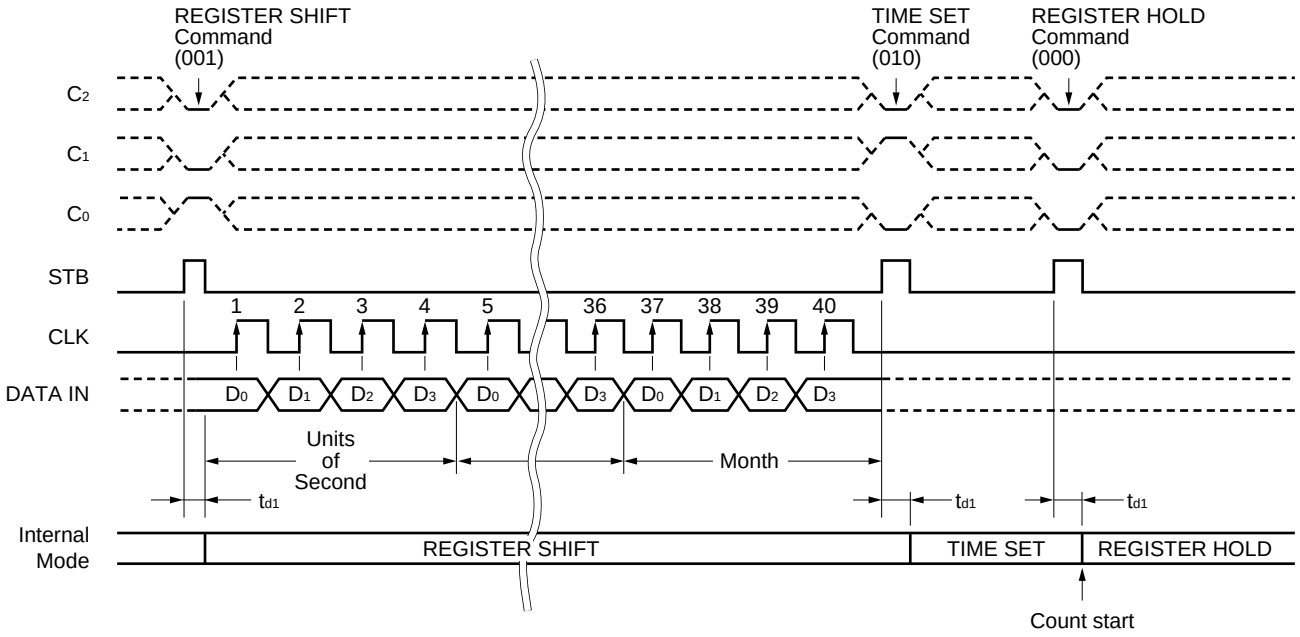
This section shows how to write data using flow-chart and timing-chart.

Fig. 3-4 Write Data Flow-chart



(1) Parallel Command Mode

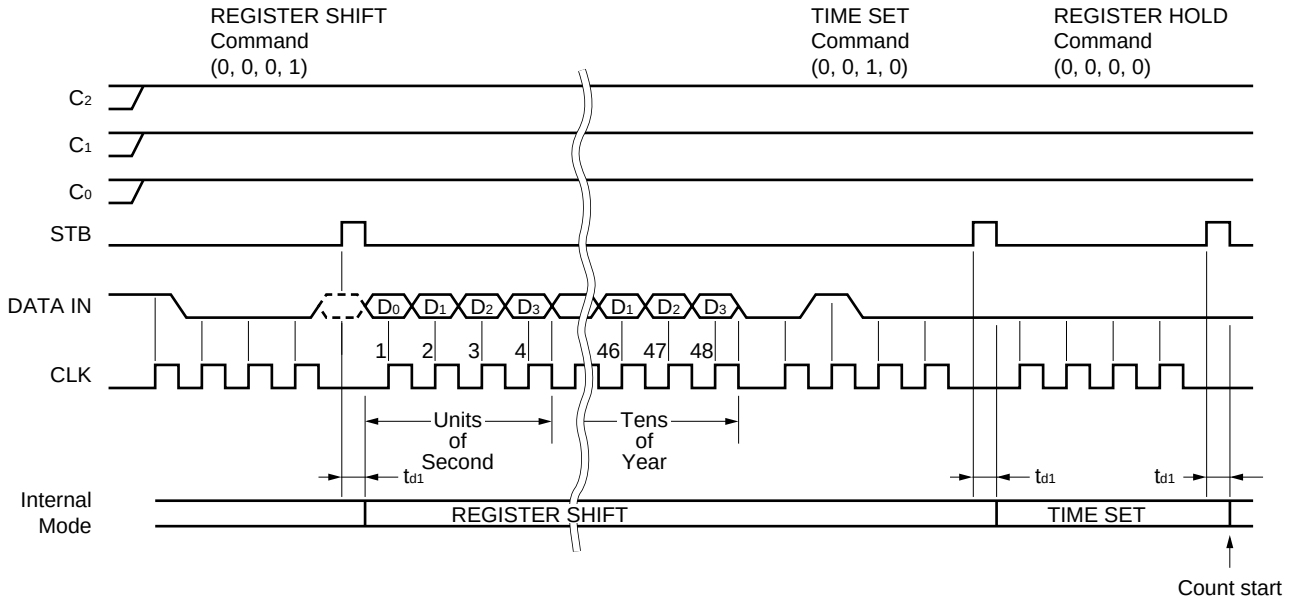
Fig. 3-5 Write Data Timing-chart (Using C_2, C_1, C_0)



Note: t_{d1} = 1 μs MAX.

(2) Serial Command Mode

Fig. 3-6 Write Data Timing-chart (Using C_3,' C_2', C_1', C_0')



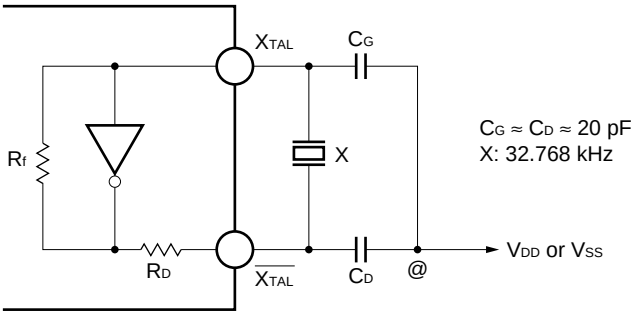
Note: t_{d1} = 1 μs MAX.

CHAPTER 4 EXPLANATION OF ELECTRICAL CHARACTERISTICS

4.1 CRYSTAL OSCILLATOR

This crystal oscillator of μPD4990A is consisted a CMOS inverter, a feedback resistor R_f, and a stabilization resistor R_D. ($R_f \simeq 1$ MΩ, $R_D = 100$ kΩ) X'$_{TAL}$ and $\overline{X_{TAL}}$ are connected C_G or C_D. Value of C_G and C_D should be adjusted for user's system.

Fig. 4-1 Crystal Oscillator



Please adjust value of C_D or C_G.

Wire length around C_G, C_D, crystal and μPD4990A should be short length.

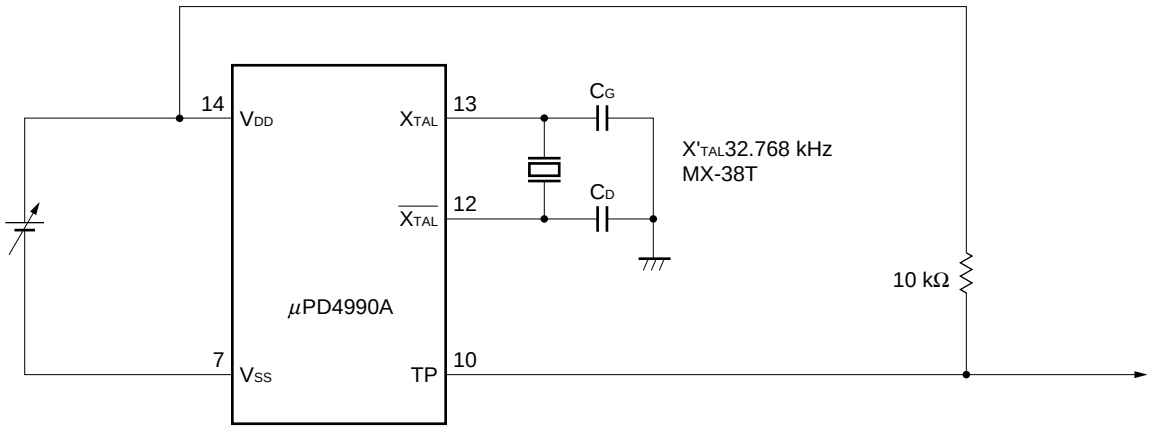
4.2 HOW TO ADJUST OSCILLATION FREQUENCY

To adjust oscillation frequency, TP is connected to a frequency counter or a period counter. And Timing Pulse should appeare to TP.

4.3 OSCILLATION CHARACTERISTICS

Measurement circuit of oscillation characteristics is shown Fig. 4-2.

Fig. 4-2 Measurement Circuit of Oscillation Characteristics



4.3.1 Temperature Characteristics

Fig. 4-3 and Fig. 4-4 show temperature characteristics is crystal characteristics.

Fig. 4-3 Temperature Characteristics

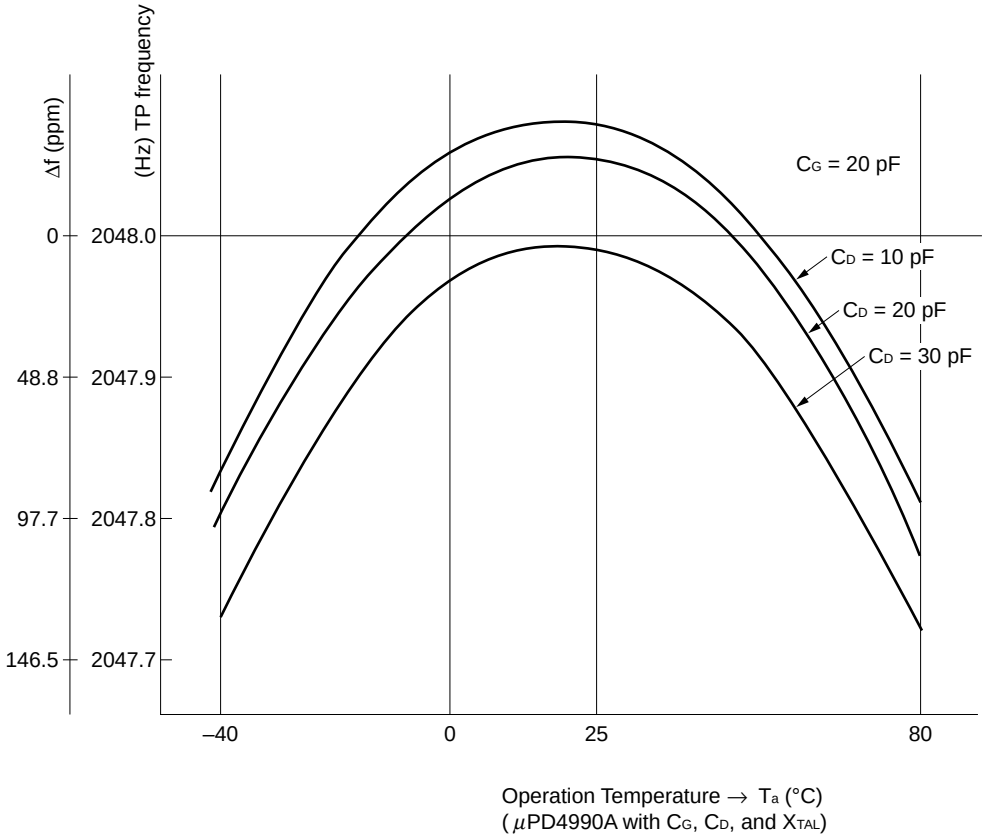
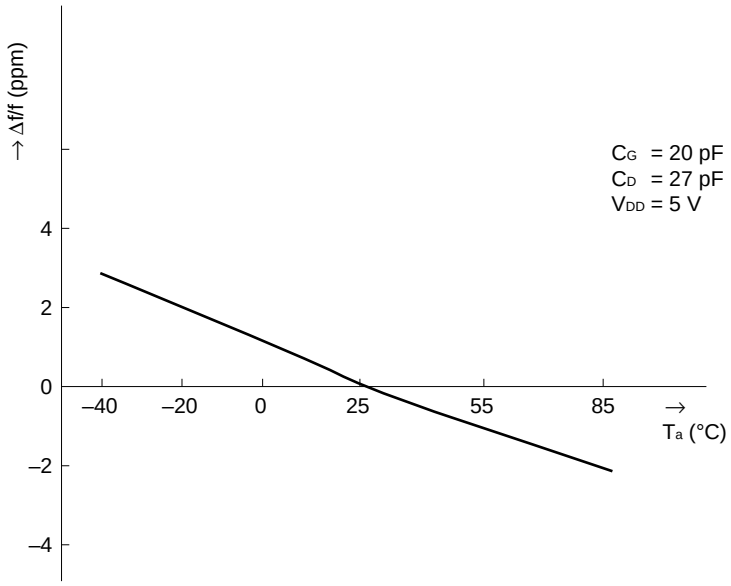
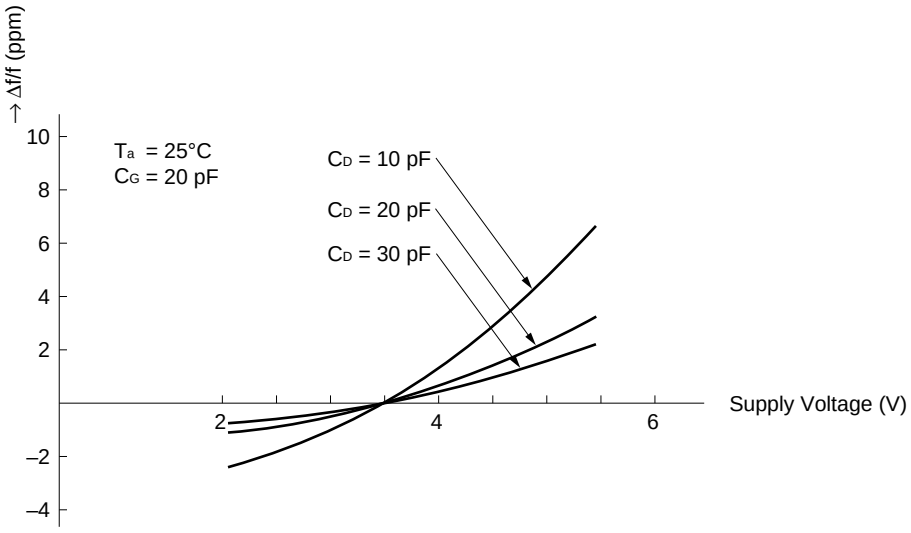


Fig. 4-4 Temperature Characteristics (Only μPD4990A)



(CG, CD, and X'TAL Temperature is 25°C constant.)

4.3.2 Supply Voltage Characteristics



4.4 SUPPLY CURRENT CHARACTERISTICS

Measurement circuit of supply current and characteristics are shown Fig. 4-5 and Fig. 4-6.

Fig. 4-5 Measurement Circuit

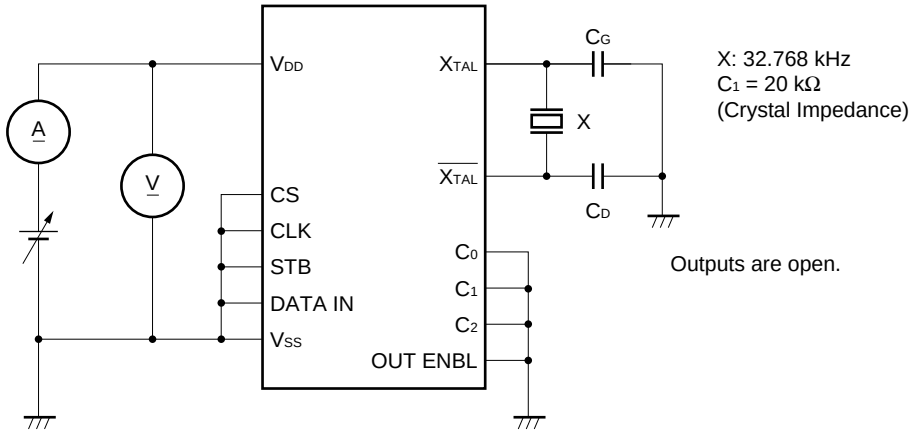
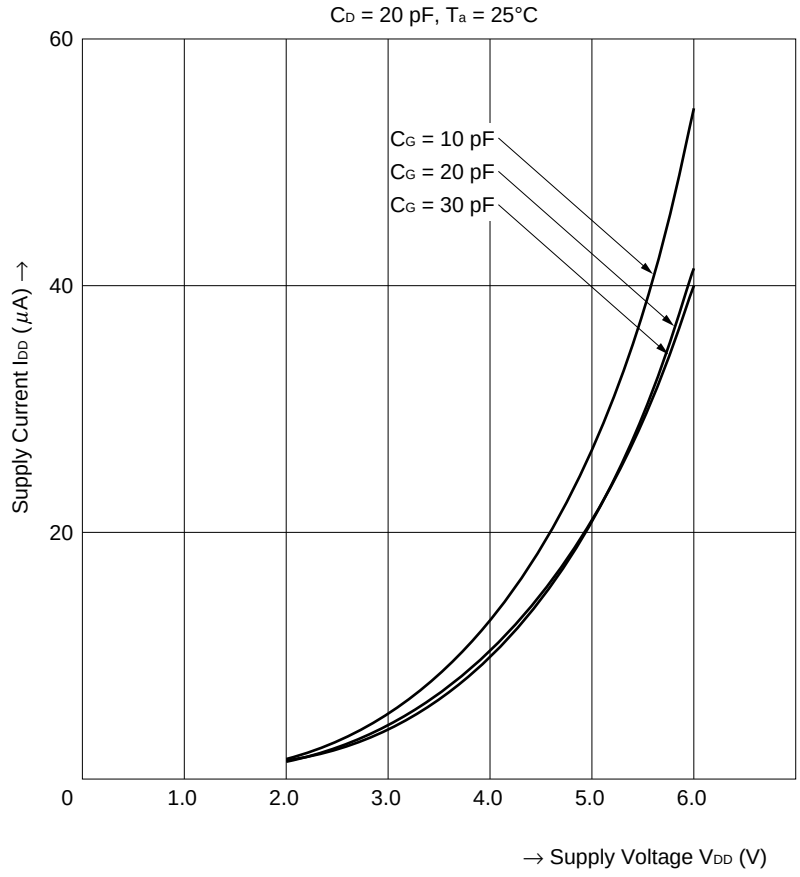


Fig. 4-6 Supply Current Characteristics

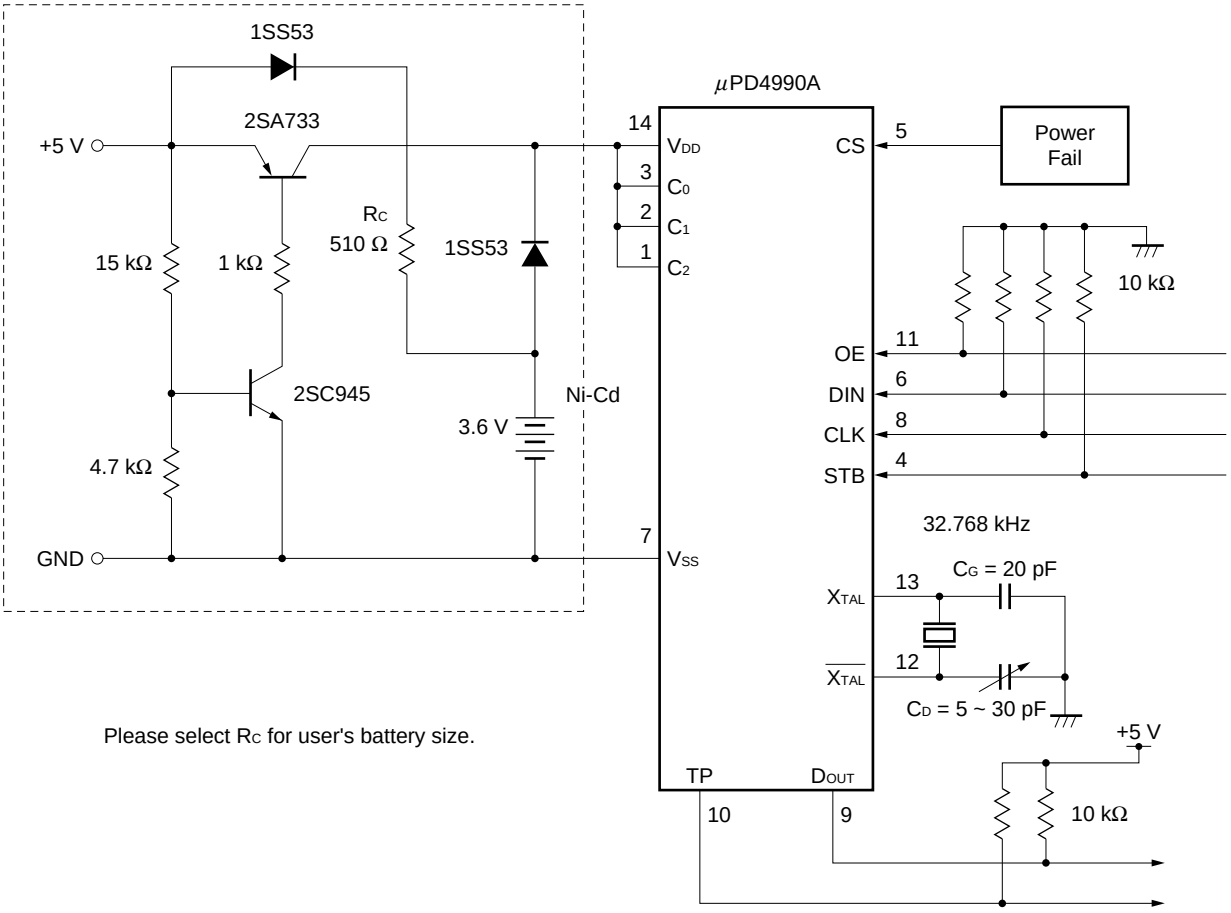


CHAPTER 5 INTERFACE

5.1 POWER SUPPLY CIRCUIT

(1) Using transistor and Ni-Cd battery.
Application circuit is shown Fig. 5-1.

Fig. 5-1 Application Circuit No. 1



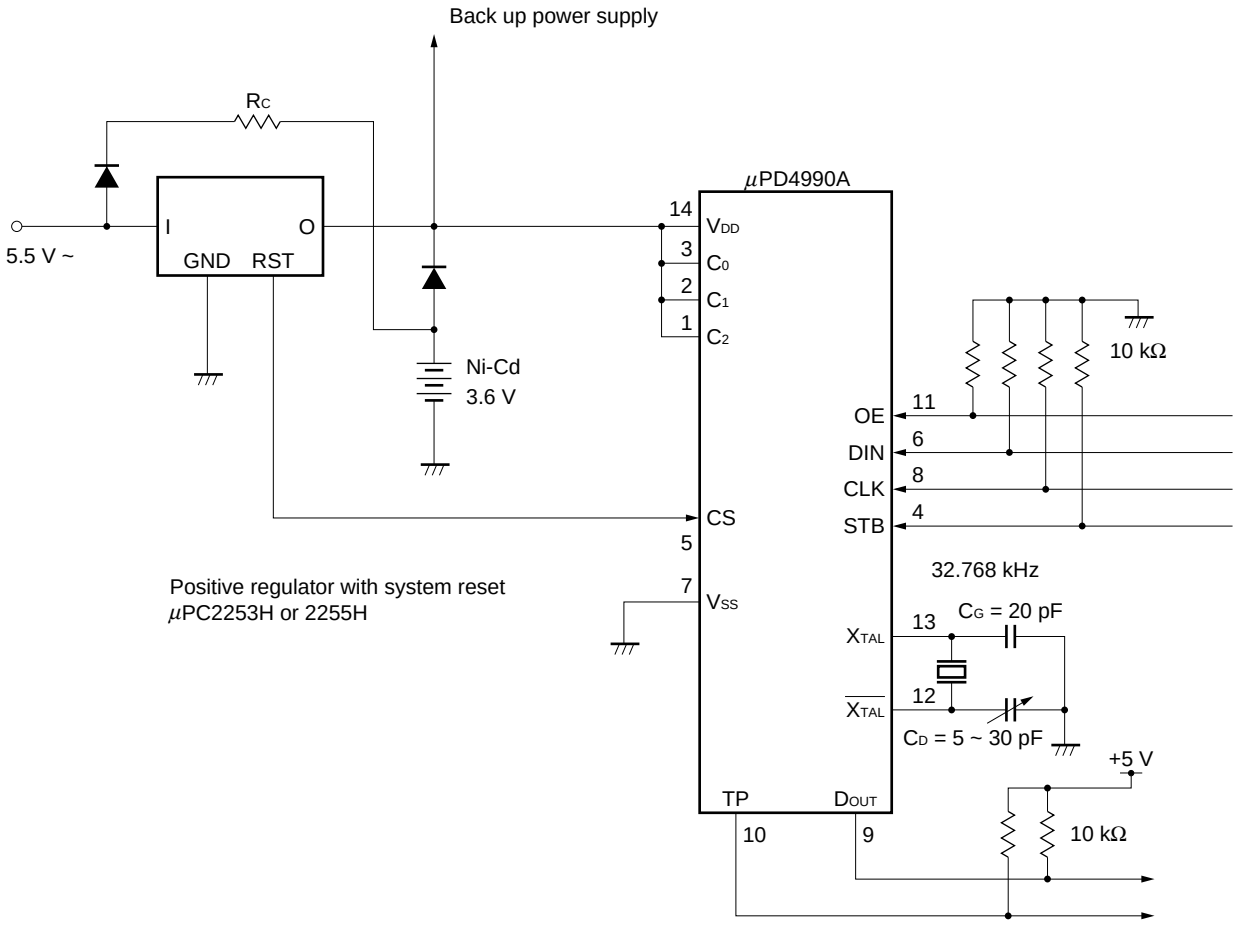
Please select RC for user's battery size.

(2) Using positive regulator with system reset

Application circuit is shown Fig. 5-2.

This application circuit is consist of system reset circuit (as power fail circuit). So this circuit will be better cost performance than Fig. 5-1.

Fig. 5-2 Application Circuit No. 2



(3) Application for constant supply voltage

The circuits of Fig. 5-1 and Fig. 5-2 aren't constant supply voltage. When system is active, supply voltage of μPD4990A is 5 V. But when system is down (back up), supply voltage of μPD4990A is 2-5 V. Fig. 5-3 will be less time error than Fig. 5-1 and Fig. 5-2. But level shifters are necessary.

Fig. 5-3 (a) Application Circuit (Using 74LS07)

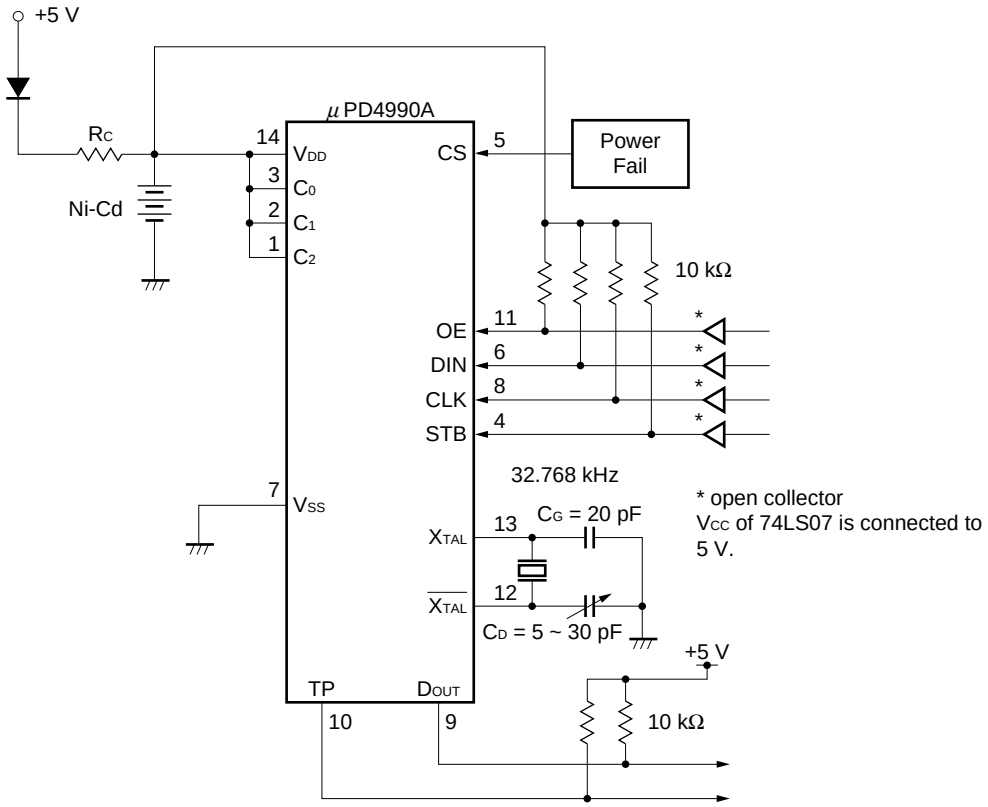
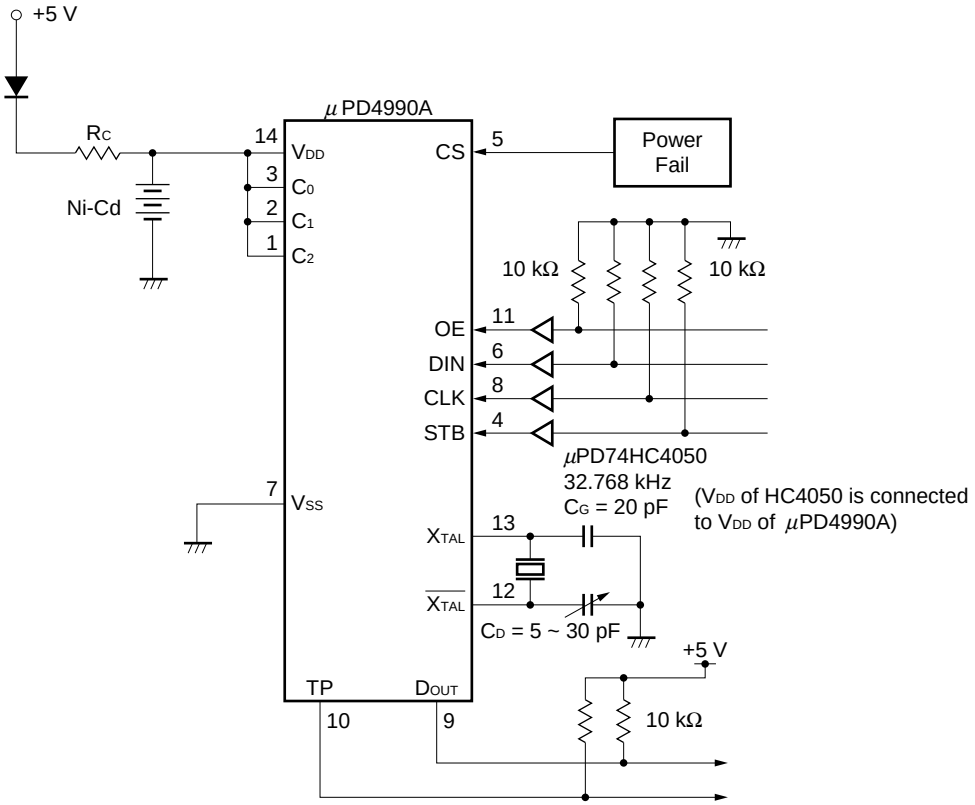


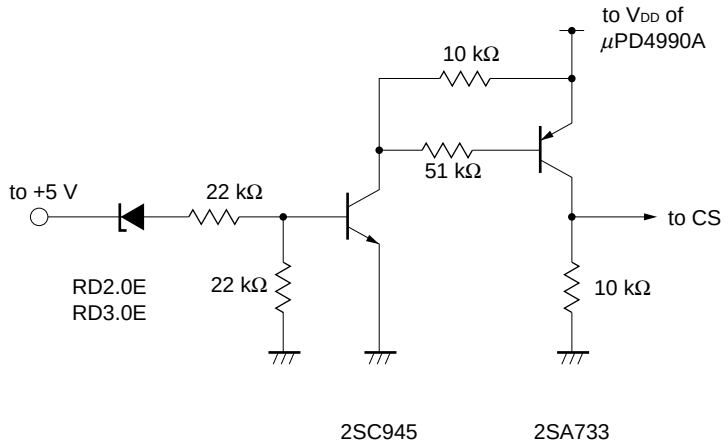
Fig. 5-3 (b) Application Circuit (Using 74HC4050)



5.2 POWER FAIL CIRCUIT

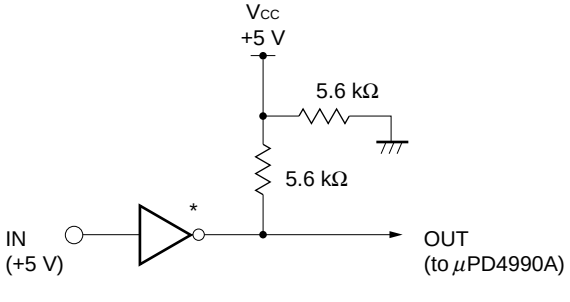
If main power supply is down, CS should be low level as illegal data or command aren't set to μPD4990A. The output of circuit shown Fig. 5-4 is low while V_{DD} is less than 4.4 to 3.4 V.

Fig. 5-4 Power Fail Circuit



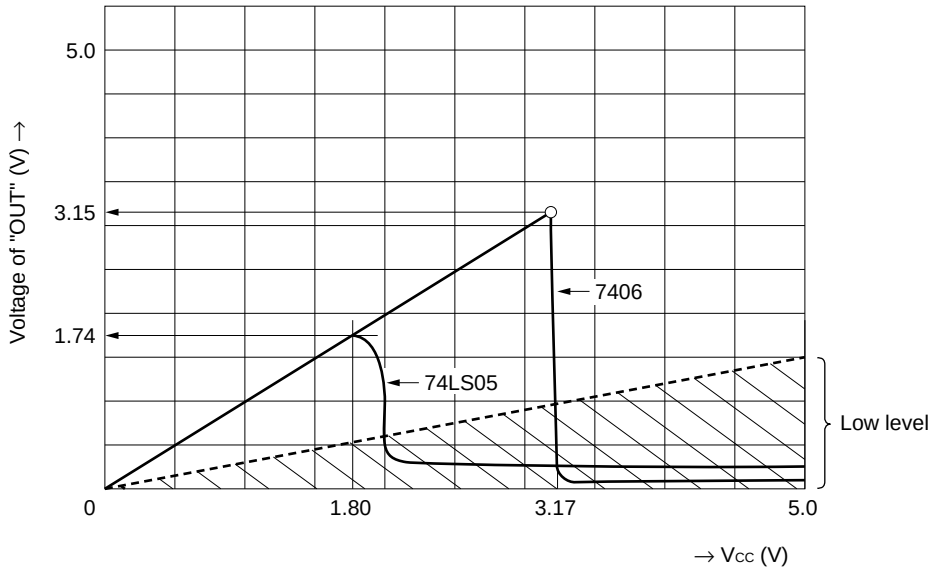
Don't use TTL for power fail circuit. Because the output of TTL is unknown while V_{DD} is less than 4.5 V. Fig. 5-5 is a faulty example.

Fig. 5-5 Faulty Example



The circuit of Fig. 5-5 isn't low level until V_{DD} is 0 V.

Fig. 5-6 Characteristics of Fig. 5-5



[MEMO]

CHAPTER 6 APPLICATION CIRCUIT & SOFTWARE

This section is shown some application circuits and softwares for some CPUs.

6.1 μCOM-75X (4 BIT SINGLE CHIP CPU)

Fig. 6-1 is a example of circuit and List 6-1 is a example of software.

Fig. 6-1 Application Circuit for μCOM-75X

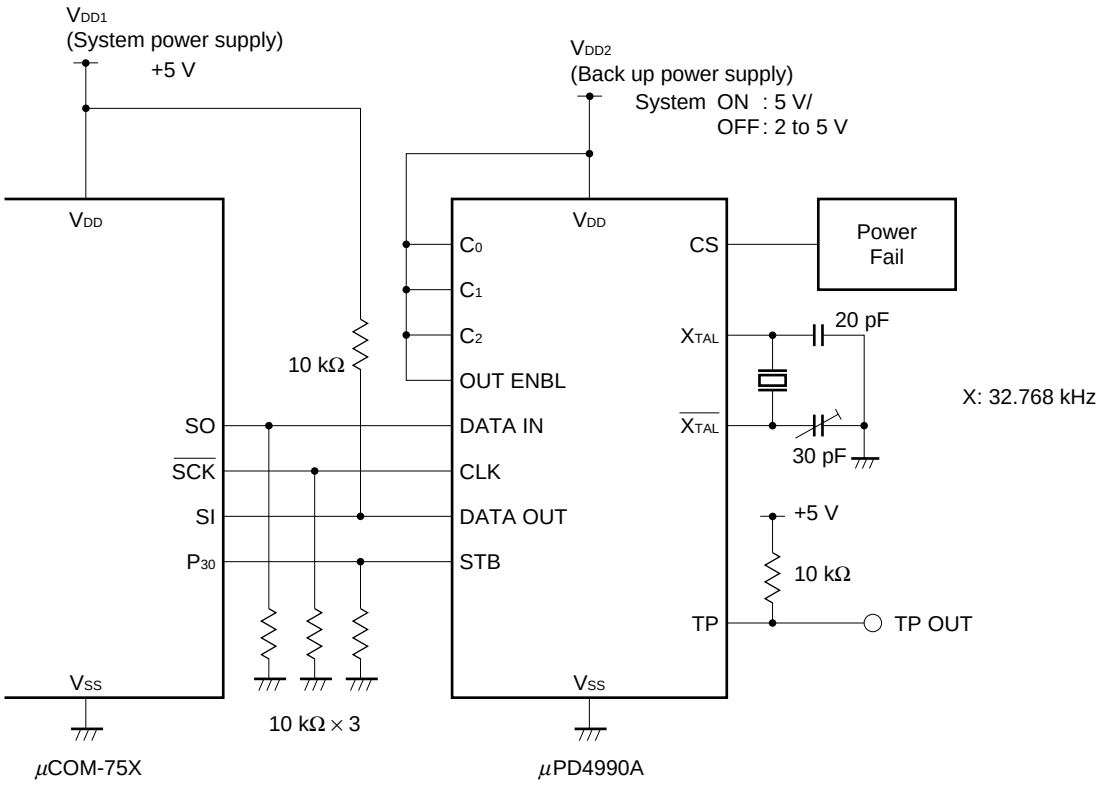


Table 6-1 Application Software for μCOM-75X

```
;Initialize routine
;
INIT:     SEL      MB15
          MOV      A, #0011B
          MOV      PCC, A          ; φ = fXX/4 mode
          CLR1     PORT3.0
          MOV      XA, #0FH
          MOV      PMGA, XA        ; PORT3
          MOV      XA, #11100111B
          MOV      SIOM, XA        ; Serial I/E set
          DI       IESIO
          MOV      XA, #0
          CALL     CMDTX           ; Register Hold command
          RET
;
;
;Wait routine
;
WAIT:     DECS     A
          BR       WAIT
          RET
;
CMDTX:    SEL      MB15
          MOV      SIO, XA
          SET1     SIOM.3
LOOPC:    SKTCLR   IRQSIO
          BR       LOOPC
          SET1     PORT3.0
          CLR1     PORT3.0
          RET
;
;
;Time read routine
;
TMRD:     PUSH     HL
          SEL      MB15
          MOV      XA, #30H
          CALL     CMDTX           ; Time Read command
          MOV      XA, #10H
          CALL     CMDTX           ; Register Shift command
          MOV      A, #19
          CALL     WAIT            ; WAIT 20 μs
          MOV      B, #5
```

```
LOOP1:    SEL       MB15
          SET1      SIOM.3
LOOPR:    SKTCLR    IRQSIO
          BR        LOOPR
          MOV       XA, SIO
          SEL       MB0
          MOV       @HL, XA          ; (HL) ← XA
          INCS      HL
          INCS      HL
          DECS      B
          BR        LOOP1
          POP       HL
          RET
;Time write routine
;
TMWR:     PUSH      HL
          SEL       MB15
          MOV       XA, #10H
          CALL      CMDTX
          MOV       XA, HL
          ADDS      XA, #12
          XCH       XA, HL
          MOV       @HL, #2
          XCH       XA, HL
          DECS      HL
          MOV       B, #6
LOOPW:    SEL       MB0
          MOV       XA, @HL
          SEL       MB15
          MOV       SIO, XA
          SET1      SIOM.3
LOOP2:    SKTCLR    IRQSIO
          BR        LOOP2
          INCS      HL
          INCS      HL
          DECS      B
          BR        LOOPW
          SET1      PORT3.0
          CLR1      PORT3.0
          POP       HL
          RET
;
;
;TMST:    MOV       XA, #0
          CALL      CMDTX
          RET
```

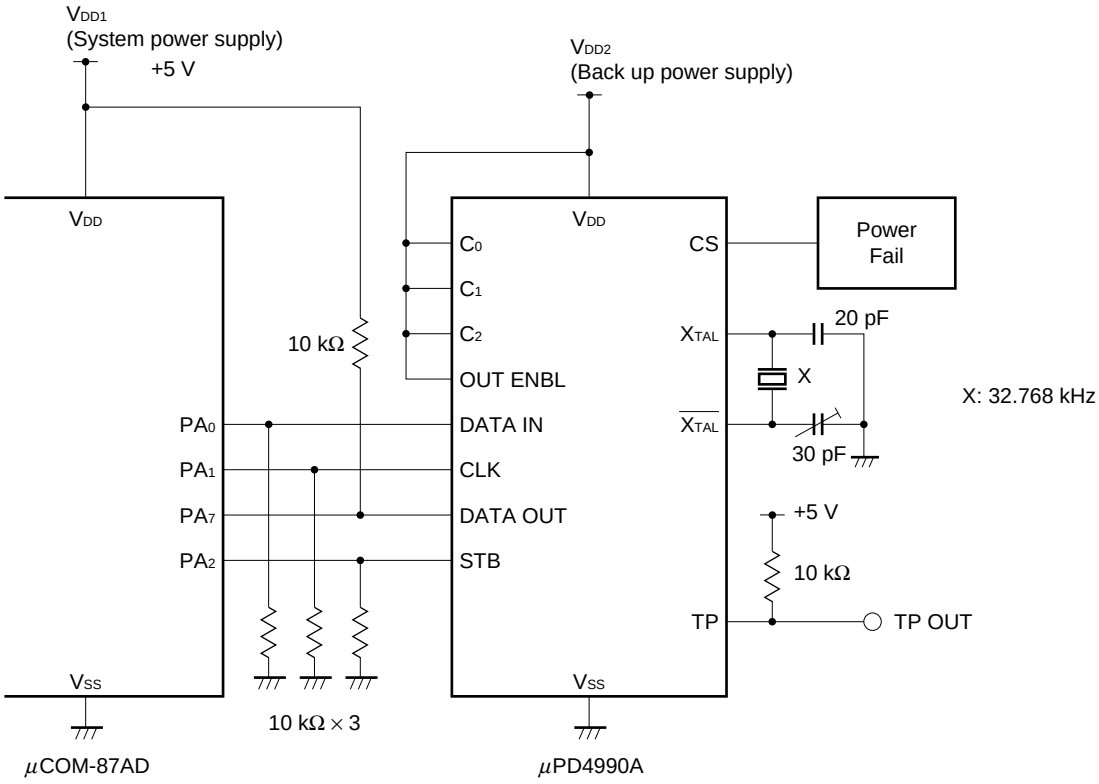
Data Table

	Upper	Lower
(HL):	Tens of second	Units of second
(HL+1):	Tens of minute	Units of minute
(HL+2):	Tens of hour	Units of hour
(HL+3):	Tens of day	Units of day
(HL+4):	Month	Day of week
(HL+5):	Tens of year	Units of year

6.2 μCOM-87AD (8 BIT SINGLE CHIP CPU)

Application circuit is shown Fig. 6-2 and Application software is shown List 6-2.

Fig. 6-2 Application Circuit for μCOM-87AD



PA0 ~ PA2 : Output port
PA7 : Input port

List 6-2 Application Software for μCOM-87AD

```
;Intilize routine
;
;
INIT:   MVI     PA, 0
        MVI     A, 7
        MOV     MA, A           ; Port A Setting
        MVI     A, 0
        CALL    CMDTX           ; Register Hold Command
;
CMDTX:  MVI     C, 3
LOOPC:  MVI     B, 0
        SLR     A
        SKN     CY
        MVI     B, 1
        MOV     PA, B
        ORI     PA, 2
        XRI     PA, 2           ; CLK Pulse
        DCR     C
        JR      LOOPC
        MVI     PA, 4
        MVI     PA, 0           ; STB Pulse
        RET
;
;
;Time read routine
;
TMRD:   PUSH    H
        MVI     A, 3
        CALL    CMDTX           ; Time Read Command
        MVI     A, 1
        CALL    CMDTX           ; Register Shift Command
        MVI     A, 9
LOOPW:  DCR     A
        JR      LOOPW           ; 20 μs Wait
        MVI     B, 5
        MVI     C, 7
LPRXD:  PUSH    B
LPRXB:  MOV     A, PA           ; 1 bit Read
        SLL     A
        RLR     B
        MVI     PA, 2
        MVI     PA, 0           ; CLK Pulse
        DCR     C
        JR      LPRXB           ; 1 byte Transfer
        MOV     A, B
        STAX    H+              ; 1 byte Store
```

```
            POP     B
            DCR     B
            JR      LPRXD       ; 6 byte Transfer Loop
            POP     H
            RET
;Time write routine
;
TMWR:       PUSH    H
            MVI     A, 1
            CALL    CMDTX       ; Register Shift Command
            MVI     C, 5
LPTXD:      LDAX    H+
            MVI     B, 7
LPBTW:      SLR     A
            SK      CY
            MVI     PA, 0
            SKN     CY
            MVI     PA, 1
            ORI     PA, 2
            XRI     PA, 2       ; CLK Pulse
            DCR     B
            JR      LPBTW       ; 1 byte Transfer Loop
            DCR     C
            JR      LPTXD       ; 6 byte Transfer Loop
            MVI     A, 2
            CALL    CMDTX
            POP     H
            RET

TMST:       MVI     A, 0
            CALL    CMDTX
            RET
```

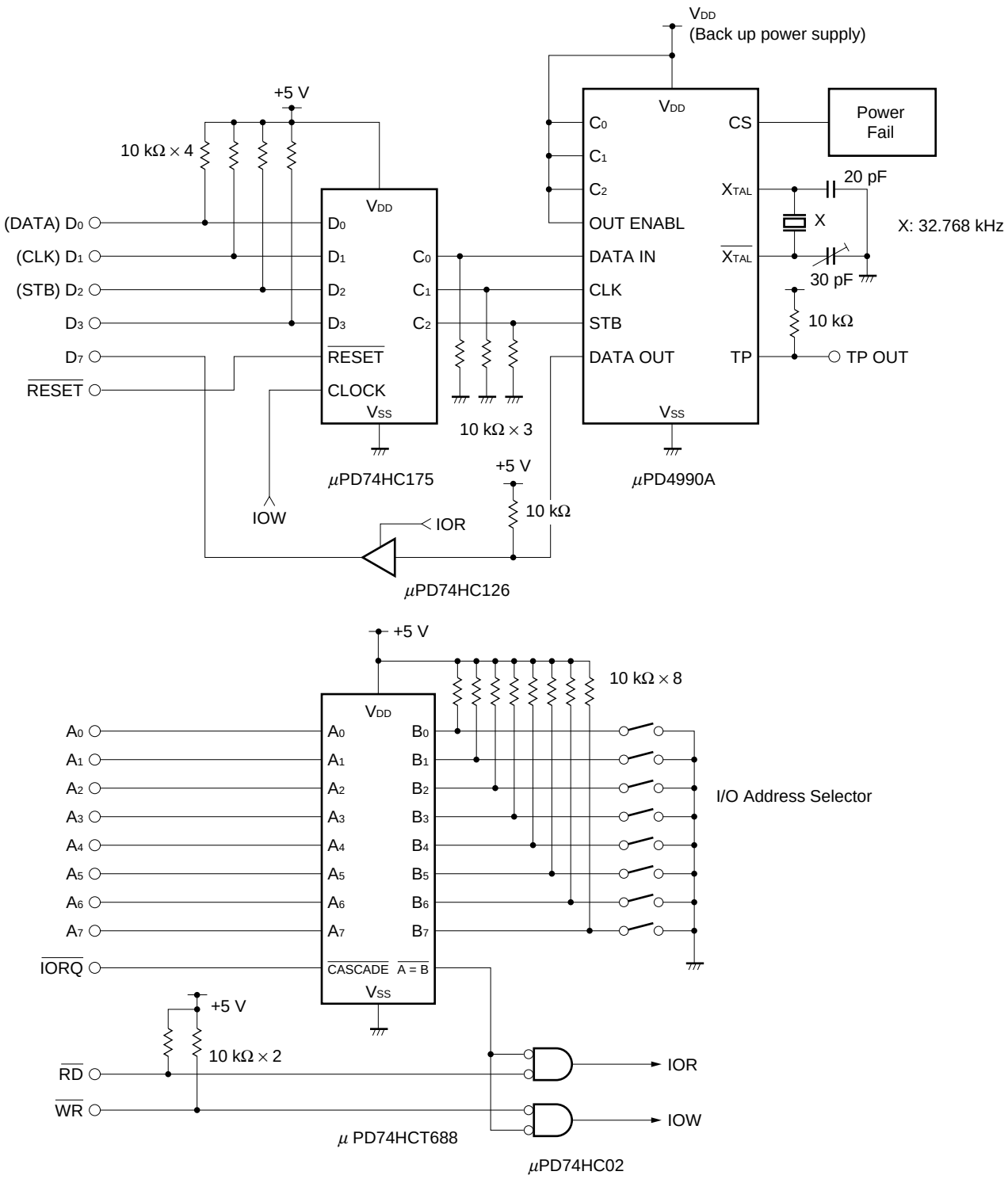
Data Table

	Upper	Lower
(HL):	Tens of second	Units of second
(HL+1):	Tens of minute	Units of minute
(HL+2):	Tens of hour	Units of hour
(HL+3):	Tens of day	Units of day
(HL+4):	Month	Day of week
(HL+5):	Tens of year	Units of year

6.3 80 SERIES MULTI CHIP CPU

Application circuit for μPD780A/μPD70008A is shown Fig. 6-3.
Application software is shown List 6-3.

Fig. 6-3 Application Circuit (Back Up Power Supply)



List 6-3 Application Software for μPD780A/μPD70008A

```
;Initialize routine
;
INIT:    LD      A, 0
         OUT     IO, A
         LD      A, 0
         CALL    CMDTX       ; Register Hold Command
         RET
;
CMDTX:   LD      C, IO
         LD      E, 4
LOOPC:   LD      D, 0
         SRA     A
         JR      NC, TXCLK
         LD      D, 1
TXCLK:   OUT     (C), D
         SET     1, D
         OUT     (C), D
         RES     1, D
         OUT     (C), D      ; CLK Pulse
         DEC     E
         JR      NZ, LOOPC
         SET     2, D
         OUT     (C), D
         RES     2, D        ; STB Pulse
         OUT     (C), D
         RET
;
;
;Time read routine
;
TMRD:    PUSH    HL
         LD      A, 3
         CALL    CMDTX       ; Time Read Command
         LD      A, 1
         CALL    CMDTX       ; Register Shift Command
LOOPR:   LD      B, 9
         DJNZ    LOOPR       ; Wait 20 μs
         LD      E, 6
         LD      C, IO
LPRXD:   LD      B, 8
LPBTR:   IN      A, (C)      ; 1 bit Read
         LD      D, 2
         OUT     (C), D
         LD      D, 0        ; CLK Pulse
         OUT     (C), D
         SRA     A
```

```
            DJNZ    LPBTR       ; 1 byte Transfer Loop
            LD      (HL), A
            INC     HL
            DEC     E
            JR      NZ, LPRXD   ; 6 byte Transfer Loop
            LD      (HL), A
            INC     HL
            DEC     E
            JR      NZ, LPRXD   ; 6 byte Transfer Loop
            POP     HL
            RET
;Time write routine
;
TMWR:       PUSH    HL
            LD      A, 1
            CALL    CMDTX       ; Register Shift Command
            LD      E, 6
            LD      C, IO
LPTXD:      LD      A, (HL)
            INC     HL
            LD      B, 8
LPBTW:      LD      D, 0
            SRA     A
            JR      NC, TXCLK1
            LD      D, 1
TXCLK1:     OUT     (C), D
            SET     1, D
            OUT     (C), D
            RES     1, D
            OUT     (C), D      ; CLK Pulse
            DJNZ    LPBTW       ; 1 byte Transfer Loop
            DEC     E
            JR      NZ, LPTXD   ; 6 byte Transfer Loop
            POP     HL
            LD      A, 2
            CALL    CMDTX
            RET

TMST:       LD      A, 0
            CALL    CMDTX
            RET
```

Note: I/O I/O Port Address

CHAPTER 7 CONVERTING μPD1990A TO μPD4990A

7.1 SPECIFICATION DIFFERENCE

Table 7-1 SPECIFICATION DIFFERENCE

ITEM		μPD1990A	μPD4990A
Supply current (V_{DD} = 3.6 V)		50 μA max.	20 μA max.
CLK frequency (V_{DD} = 2 V)		100 kHz max.	500 kHz max.
STB pulse width		2 μs min.	1 μs min.
STB latch delay (After Time Read)		40 μs max.	20 μs max.
Value of C_D and C_G		30 pF	20 pF
DATA OUT while time read		0.5 Hz	1 Hz
(C_0, C_1, C_2) = (1, 1, 1) command		Test Command	Serial command mode
Error of time set		±31.25 ms	±15.625 ms
DATA OUT/TP while test mode	Register Shift	LSB/32 Hz	LSB/32 Hz
	Time Set	LSB/32 Hz	LSB/“L”
	Time Read	512 Hz/32 Hz	1 Hz/32 Hz
Count frequency while test mode		1024 Hz	8192 Hz

7.2 DIFFERENCE OF OSCILLATOR

Fig. 7-1 Oscillator of μPD4990A and μPD1990A

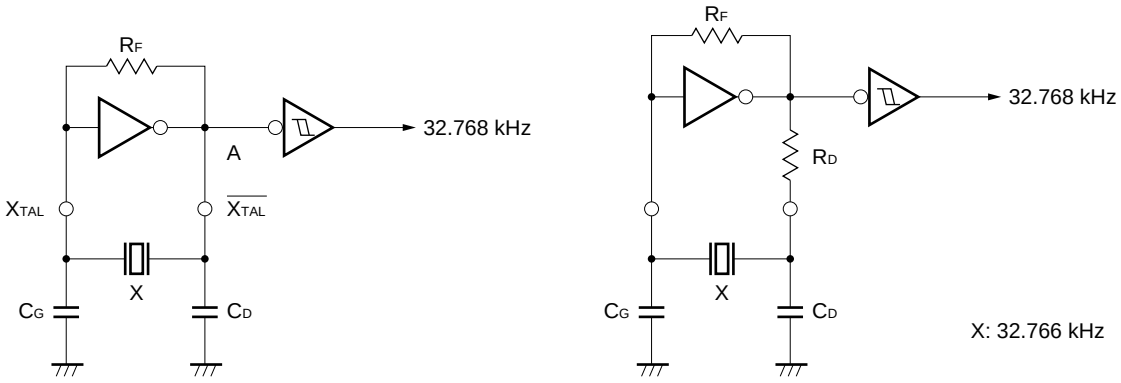
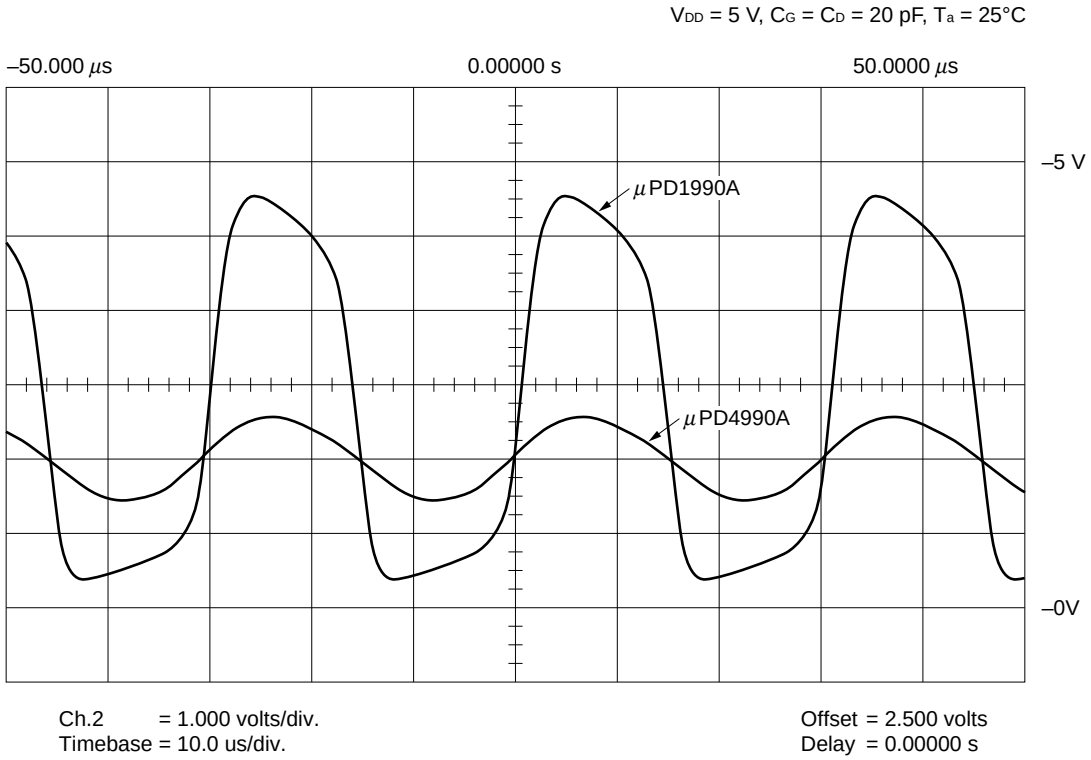


Fig. 7-2 Oscillation Wave of μPD4990A and μPD1990A



APPENDIX μPD4990A SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	V_{DD}-V_{SS}	7.0	V
Input Voltage	V_{IN}	V_{SS}–0.3 to V_{DD} +0.3	V
Operating Temperature Range	T_{opt}	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +125	°C
Output Terminal Voltage	V_{OUT}	7.0	V

ELECTRICAL CHARACTERISTICS (f = 32.768 kHz, C_G = C_D = 20 pF, CI = 20 kΩ, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	$V_{DD} – V_{SS}$	2.00		5.50	V	
Current Consumption	I_{DD}		8	20	μA	$V_{DD} – V_{SS}$ = 3.60 V
				100	μA	$V_{DD} – V_{SS}$ = 5.50 V
Low Level Output Voltage	V_{OL}			0.4*	μA	$V_{DD} – V_{SS}$ = 2.0 to 5.5 V I_{OL} = 500 μA
CLK Input Frequency	f_{CLK}	DC		500	kHz	$V_{DD} – V_{SS}$ = 2.0 V, Duty 50 %
Input Leakage Current	I_{IN}			1	μA	$V_{DD} – V_{SS}$ = 5.50 V
High Level Input Voltage	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	V_{SS}		0.3 V_{DD}	V	

***** TP and DATA OUT are N-channel open drain output.

A.C. ELECTRICAL CHARACTERISTICS (FOR REFERENCE – NOT SPECIFIED)
(F = 32.768 kHz, $V_{DD} – V_{SS}$ = 2.0 V, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{0-2}, CS-STB Set-up Time	t_{SU}	1			μs	
STB Pulse Width	t_{STB}	1			μs	
C_{0-2}, CS-STB Hold Time	t_{HLD}	1			μs	
STB LATCH Delay Time	t_{d1}			1**	μs	except Time Read mode
CLK-DATA OUT Delay time	$t_{d(c-o)}$			1	μs	R_L = 33 kΩ, C_L = 15 pF
DATA IN Set-up Time	t_{DSU}	1			μs	
DATA IN Hold Time	t_{DHLD}	1			μs	

**** Note:** When a function mode is Time Read mode (other than Test mode), STB LATCH delay time is 20 μs MAX. (t_{d2}).

[MEMO]