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# USER'S MANUAL

RENESAS

Phase-out/Discontinued

# SE-17202

17K SERIES

Document No. EEU-1275B
(O. D. No. EEU-679A)
Date Published October 1992 P
Printed in Japan

# USER'S MANUAL

NEC

Phase-out/Discontinued

# SE-17202

17K SERIES

Major Revisions in This Edition

| Page | Contents |
|---|---|
| Throughout | Target chip changed from uPD17202 to uPD17202A |
| Throughout | Supply voltage range changed from +2 to 6 V, to +2.2 to 5.5 V |
| 4-1 | Addition of 4.1 Using Level Conversion Chip (uPD6705) |
| 4-12 to 4-15, 4-24 | Output file for AS17K changed from .HEX file to .ICE file |
| 4-29 | Addition of 4.6.8 LED1 and LED2 |

# INTRODUCTION

Readers: This manual is intended for users who evaluate a uPD17202A system by using SE-17202.

Organi-: This manual consists of the following:
zation
- o General
- o Specifications
- o Block diagrams
- o Use
- o Connector pin table
- o Probe and conversion socket dimensions

Purpose: SE-17202 is a uPD17202A evaluation board.
This manual is intended to introduce SE-17202 functions and applications.

Legend:
- * : Footnote
- Note : Points to be noted
- Remarks: Supplement

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# CHAPTER 1 GENERAL

SE-17202 is an evaluation board for a system using the 4-bit single-chip microcontroller uPD17202A. This board can be used by itself. However, when it is mounted in the in-circuit emulators for the 17K Series, IE-17K and IE-17K-ET*, the program can be debugged more efficiently and effectively.

Use uPD17202A to interface with the target system. Consequently, the SE-17202 functions are equivalent to those for the uPD17202A. To connect SE-17202 to the target system, use the optional EP-17202GF (uPD17202A: 64-pin plastic QFP probe).

Since SE-17202 is provided with an on-board level conversion chip, evaluation can be accomplished, even when the supply voltage to the uPD17202A is lower or higher than +5 V (in the +2.2 to 5.5 V range).

*: Low-cost model: model without power supply

Phase-out/Discontinued

# CHAPTER 2 SPECIFICATIONS

| | | |
|---|---|---|
| Product name | : | SE-17202 |
| Program memory | | o When mounted to IE-17K<br>uPD43256AC<br>o When using SE-17202 alone<br>Write the program to uPD27C256AD and mount it to SE-17202. As a factory-set condition, uPD43256AC is mounted. |
| Data memory | : | Internal memory for uPD17202A (112 x 4 bits) |
| Oscillation frequency | : | 32 kHz, 4 MHz (with crystal oscillator) |
| Instruction cycle | : | 4 us (with a 4-MHz crystal oscillator) |
| Operating temperature | : | +10 to +40°C |
| Storage temperature | : | -10 to +50°C (without condensation) |
| Power requirements | : | Two power supplies, one each for uPD17202A and SE-17202, are necessary (when the level conversion chip is used).<br>o For uPD17202A ($V_{DD}$): +2.2 to 5.5 V Supplied from probe (EP-17202GF) or CN12 pin<br>o For SE-17202 ($V_{CC}$): +5 V$\pm$5% Supplied from IE-17K, when SE-17202 is mounted to IE-17K. When SE-17202 is used by itself, supplied from CN11 pin |
| Current dissipation | : | 200 mA (max.)<br>(with uPD27C256AD as program memory and without load) |
| Dimensions | : | 150 x 174 x 30 mm |

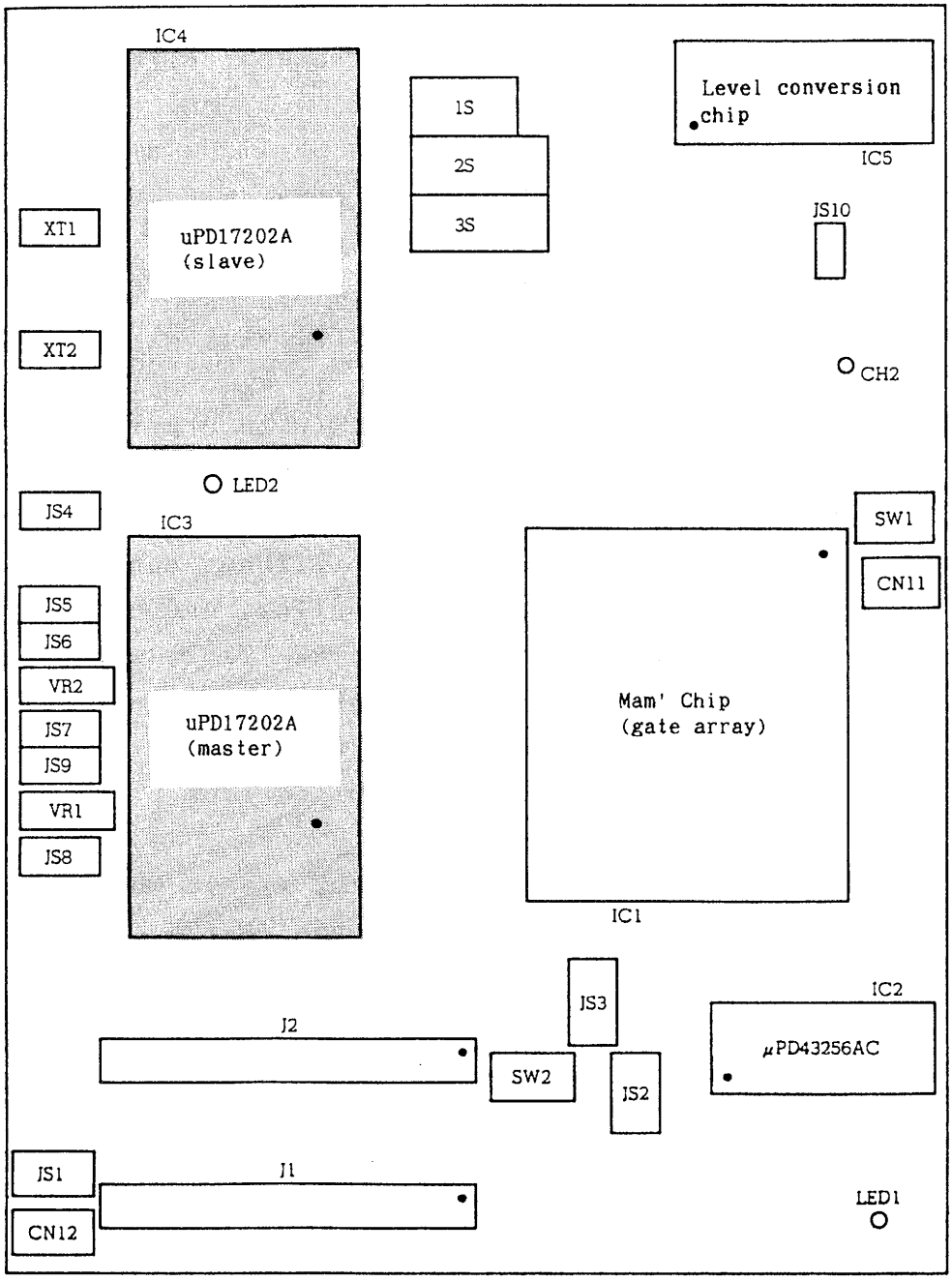



Fig. 2-1 SE-17202 Components Layout

# CHAPTER 3 BLOCK DIAGRAM

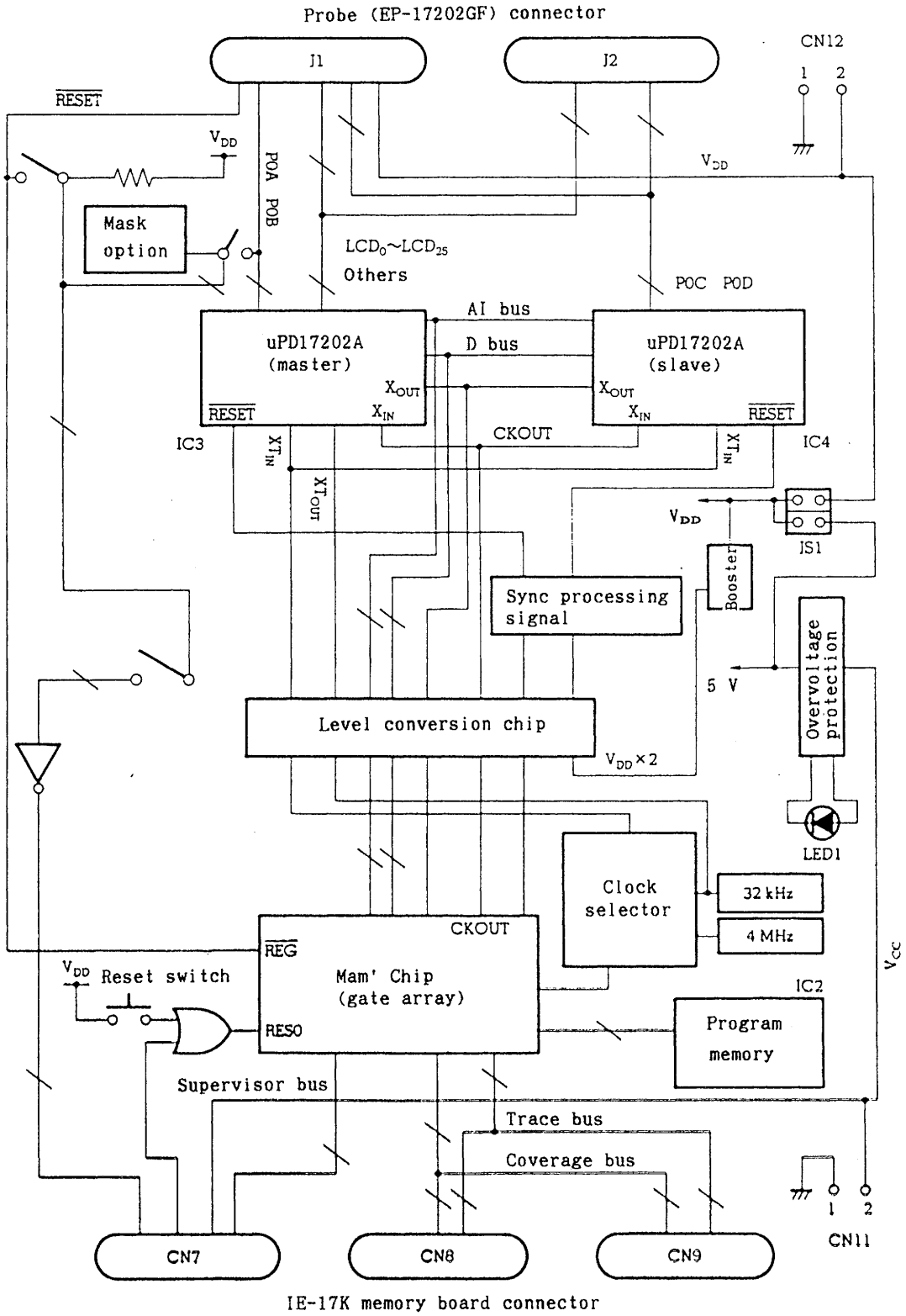



Fig. 3-1 SE-17202 Block Diagram

# CHAPTER 4 HOW TO USE

## 4.1 Using Level Conversion Chip (uPD6705)

### 4.1.1 Level conversion chip outline

When your target system's operating voltage is different from the voltage for the SE board ($V_{DD} \neq V_{CC}$, $V_{CC}$ = + 5 V), the level conversion chip converts the target system voltage level into voltage on which the SE board operates, or vice versa. Therefore, even when the operating voltage for the target system is different from that for the SE board, signals can be smoothly transferred between the system and the board.

Remarks:
1. $V_{DD}$ is the supply voltage of your target system. The voltage of the target system can be supplied to the level conversion chip on the SE board from pin CN12 or a probe, so that debugging can be executed in environments close to the actual environments.
2. $V_{CC}$ is the voltage on which the SE board operates (except this chip) and is always +5 V. If SE-17202 is mounted on IE-17K, this voltage is automatically supplied from IE-17K. When SE-17202 operates in the standalone mode, this voltage is supplied from CN11.

### 4.1.2 Using level conversion chip

- Set jumper switch JS1 to the $V_{DD}$ side.
- When a voltage other than +5 V is supplied from a probe or CN12, the level conversion chip automatically converts the voltage level to the level at which the target chip operates.

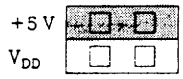
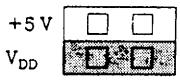
## 4.2 Supplying Voltage to SE Board

Voltages are supplied from two sources to the SE board. One source supplies the voltage on which the SE board (except the target chip) operates ($V_{CC}$). The other source supplies the voltage to operate the target chip ($V_{DD}$). $V_{CC}$ must always be ; 5 V. $V_{DD}$ can be +2.2 to 5.5 V, in which range the uPD17202A can operate. The $V_{DD}$ supply source is specified by jumper switch JS1.
Jumper switch JS2 is connected as a factory-set condition for shipment. Do not change this setting.

### 4.2.1 Jumper switch selecting supply voltage to SE board (JS1)

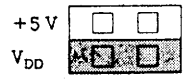
Jumper switch JS1 specifies whether the voltage supplied to the SE board (+5 V) is also supplied to the target chip, or the voltage supplied from a probe or CN12 pin is supplied to the target chip. Tables 4-1 and 4-2 illustrate the functions of this jumper switch.
If your target system's supply voltage is +5 V, set JS1 to the +5 V side, so that +5 V CN11 is supplied to the target chip, when the SE board is used by itself, and so that +5 V is supplied from IE-17K, when the SE board is mounted on IE-17K. This JS1 function facilitates voltage supply. If the supply voltage for the target system is other than +5 V, the target system voltage can be supplied to the target chip from a probe or CN12 pin by setting JS1 to the $V_{DD}$ side, so that evaluation can be executed in environments close to actual environments.

Table 4-1 JS1 Functions with SE-17202 Mounted on IE-17K

| JS1 Setting \ Voltage source | Voltage supplied to target chip ($V_{DD}$) | Voltage to operate SE board (except target chip) ($V_{CC}$) |
|---|---|---|
| JS1<br>+5 V<br>$V_{DD}$  | +5 V is supplied from IE-17K. | +5 V is supplied from IE-17K. |
| JS1<br>+5 V<br>$V_{DD}$  | Voltage must be supplied from probe or CN12 pin. | |

Remarks: ■ : selected switch position

Table 4-2 JS1 Functions When SE Board Alone Is Used

| JS1 Setting \ Voltage source | Voltage supplied to target chip ($V_{DD}$) | Voltage to operate SE board (except target chip) ($V_{CC}$) |
|---|---|---|
| JS1<br>+5 V<br>$V_{DD}$  | +5 V is supplied from CN11. | +5 V is supplied from CN11. |
| JS1<br>+5 V<br>$V_{DD}$  | Voltage must be supplied from probe or CN12 pin. | |

Remarks: ■ : selected switch position

### 4.2.2 Power supply pins

SE-17202 pins supply power to the board from external sources. It is necessary to use these pins according to the evaluation environments. Table 4-3 shows the functions for these pins.

Table 4-3 Power Supply Pins and Their Functions

| Pin | Type of power source (voltage range) | Function |
|---|---|---|
| CN11 | $V_{CC}$ (+5 V±5%) | Supplies voltage on which SE board (except the target chip) operates, when SE board is used by itself.<br>Always supply +5 V to this pin.<br>When SE board is mounted on IE-17K, power is automatically supplied from IE-17K to SE board; therefore, it is not necessary to supply voltage to this pin. |
| CN12 | $V_{DD}$ (+2.2 to 5.5 V) | If your target system's supply vltage is $V_{CC}$ = 5 V (with JS1 at the $V_{DD}$ side), this pin supplies any voltage in a range in which the target chip can operate. |
| Probe ($V_{DD}$ pin and GND pin) | $V_{DD}$ (+2.2 to 5.5 V) | The function for the probe and GND pin is the same as that for CN12.<br>Since CN12 and the power supply pin of the probe is connected on SE board, select one of the power sources. |

Remarks: Pin 1 is GND and pin 2 is power supply pin for CN11 and CN12 pins. To supply power, use the power cable supplied as an accessory.

### 4.2.3 Actual use examples

(1) To mount SE-17202 to IE-17K

(a) To operate on $V_{DD} = V_{CC} = +5$ V
Set JS1 to the +5 V side. $V_{CC}$ and $V_{DD}$ are supplied from IE-17K.

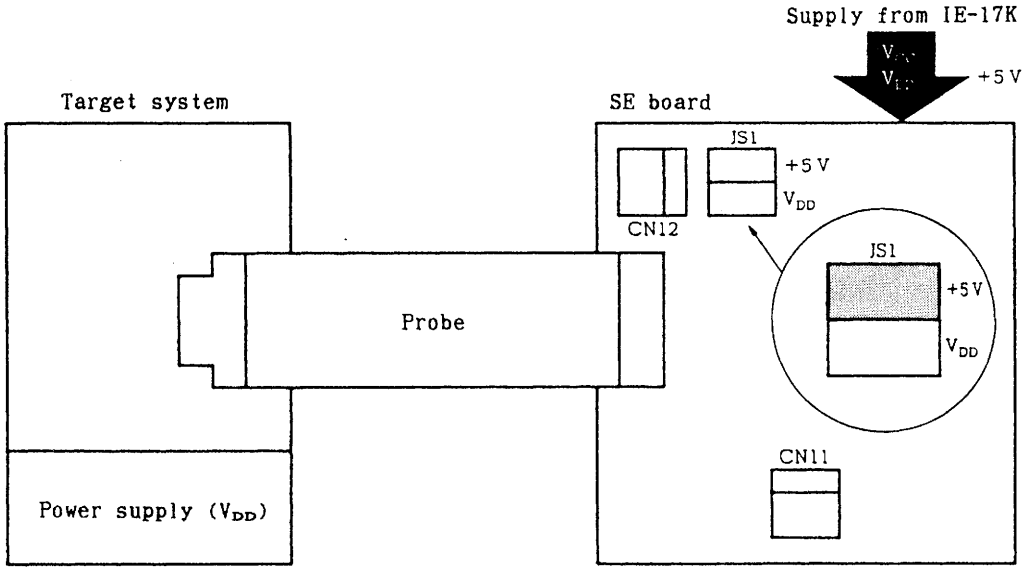



Fig. 4-1 To Supply $V_{DD}$ from IE-17K

(b) To operate on $V_{DD} \neq V_{CC}$, $V_{CC}$ = +5 V

Set JS1 to the $V_{DD}$ side. $V_{CC}$ is supplied from IE-17K, and $V_{DD}$ is supplied from CN12 or probe.

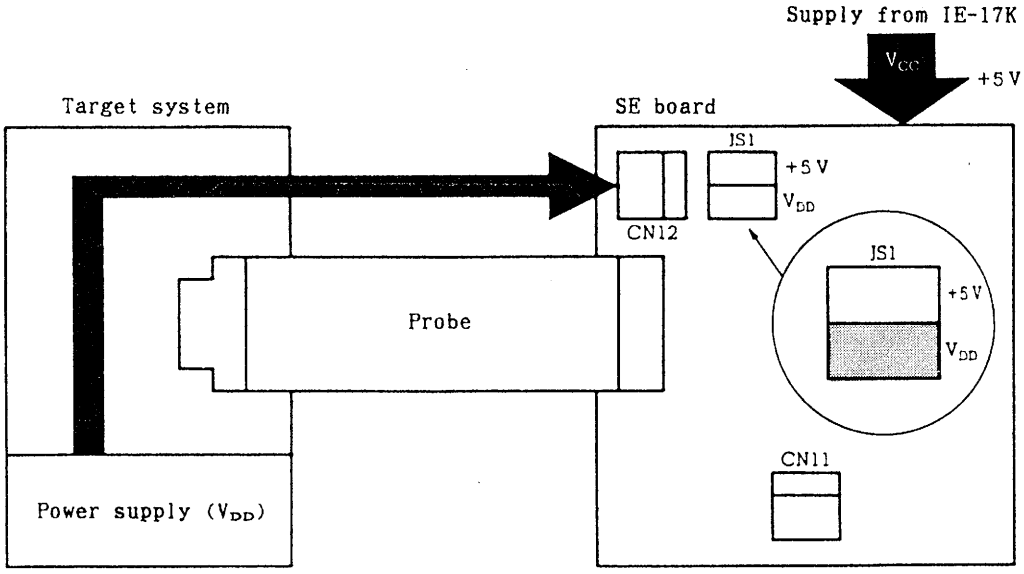



Fig. 4-2 To Supply $V_{DD}$ from CN12

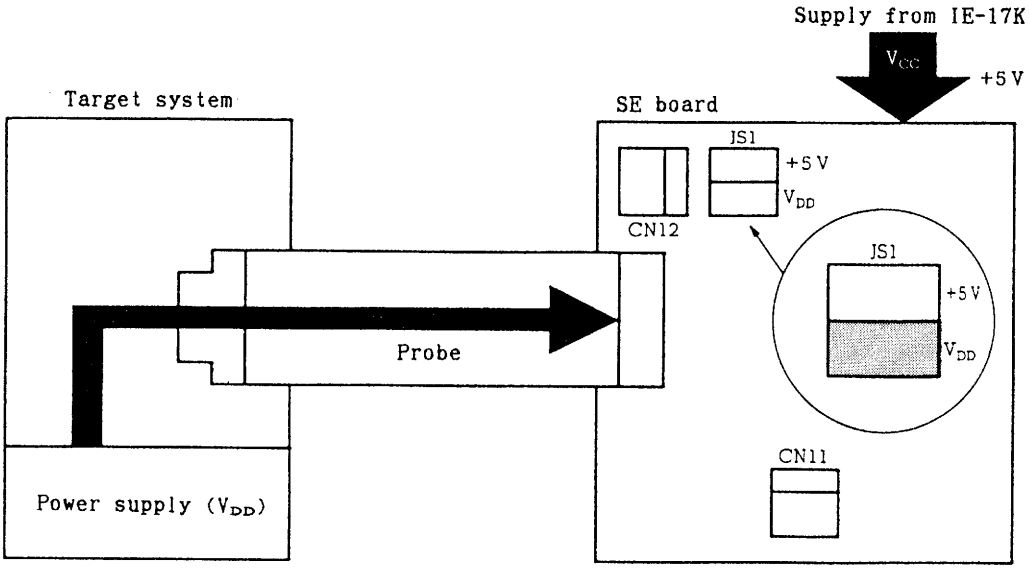



Fig. 4-3 To Supply $V_{DD}$ from Probe

(2) To use SE board alone

(a) To operate on $V_{DD}$ = $V_{CC}$ = +5 V

Set JS1 to the +5 V side. $V_{CC}$ and $V_{DD}$ are supplied from CN11.

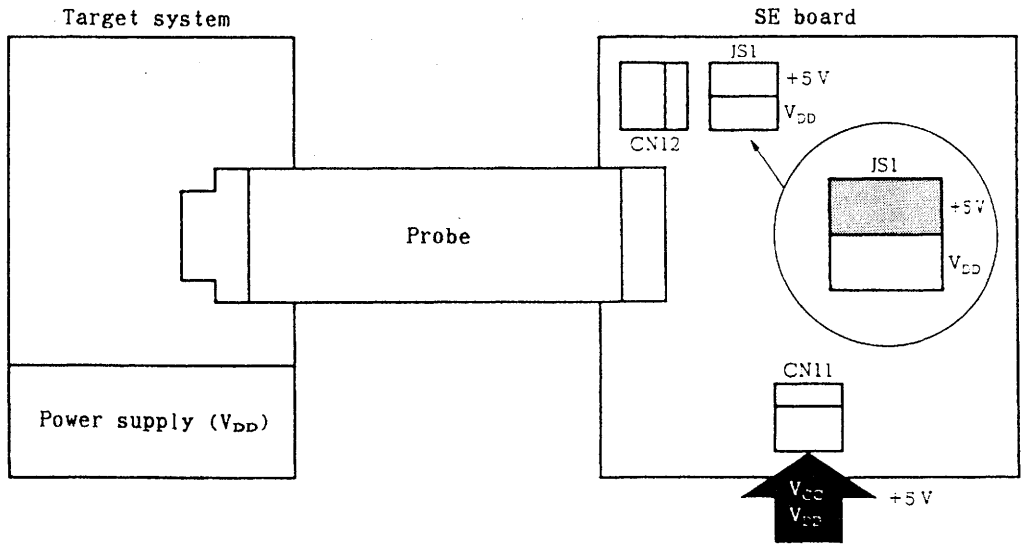



Fig. 4-4 To Supply $V_{DD}$ from CN11

(b) To operate on $V_{DD} \neq V_{CC}$, $V_{CC}$ = +5 V
Set JS1 to the $V_{DD}$ side. $V_{CC}$ is supplied from CN11, and $V_{DD}$ is supplied from CN12 or probe.

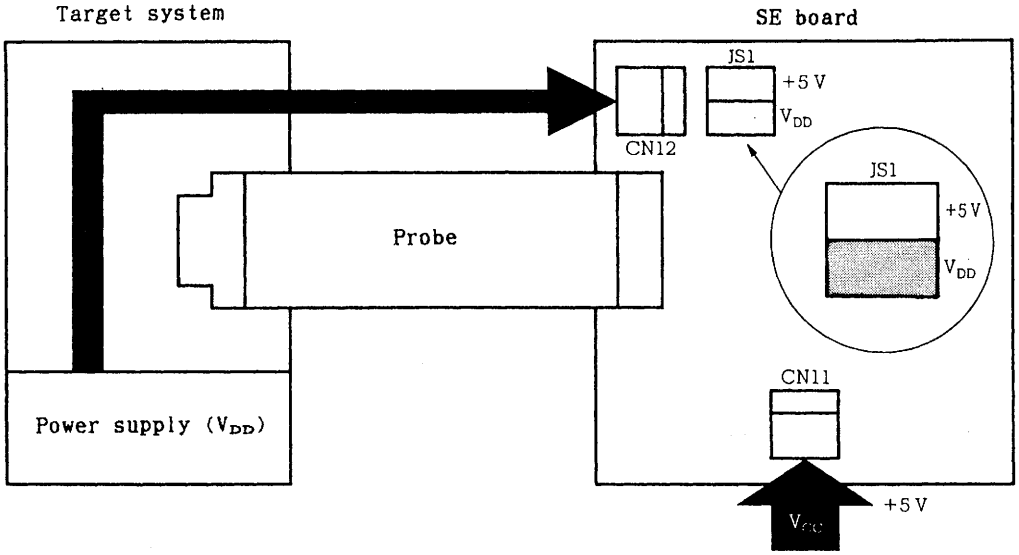



Fig. 4-5 To Supply $V_{DD}$ from CN12

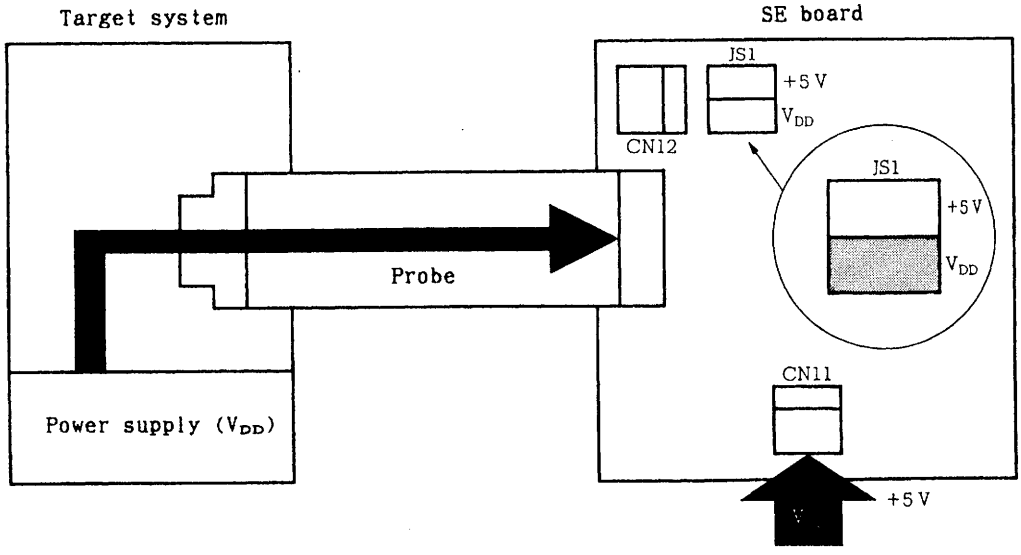



Fig. 4-6 To Supply $V_{DD}$ from Probe

## 4.3 Mounting SE-17202 to IE-17K

### 4.3.1 Mounting RAM

As the SE-17202 program memory, mount RAM (uPD43256AC). Use the RAM mounted as a factory-set condition.
To use another RAM, make sure that the RAM satisfies the following conditions:

$t_{ACC}$ < instruction cycle time/4

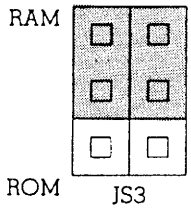
$t_{ACC}$: address setting → data output delay time

Instruction cycle time: 4 us (4 MHz) to 500 us (32 kHz)

Any of uPD43256AC-10, 12, and 15 can be used.

### 4.3.2 Setting ROM/RAM selector jumper switch (JS3)

Set JS3 to the RAM side as shown in Fig. 4-7.




Remarks: Connect the shaded portion.

Fig. 4-7 Setting JS3 (with SE-17202 mounted on IE-17K)

### 4.3.3 Setting option switch

Set the uPD17202A mask option by the SE-17202 option switch. For setting details , refer to 4.5 Setting Option Switch.

### 4.3.4 Setting target circuit on SE board

To use the target circuit on the SE board, it is necessary to set the jumper switches on the SE board (JS4, JS5, JS6, JS7, JS8, JS9, JS10, and DIP switch (SW2)). For details on the setting, refer to 4.6 Setting Target Circuit on SE Board.

### 4.3.5 Mounting and Removing to/from IE-17K

To mount SE-17202 to IE-17K, first remove the IE-17K outer and inner covers, as shown in Fig. 4-8.
When the inner cover has been removed, the memory board is visible. Three connectors are mounted on this board. Connect the connectors at the bottom of SE-17202 (CN7, 8, and 9) to these connectors (see Fig. 4-9).
Be sure to connect the SE-17202 connectors by pushing them from above.
To remove SE-17202 from IE-17K, lift the board vertically (see Fig. 4-9).

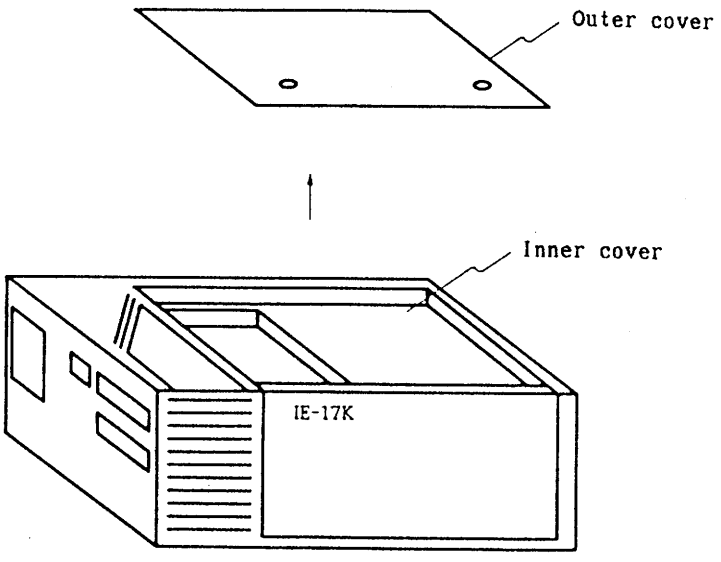



Fig. 4-8 IE-17K Appearance (with outer cover removed)

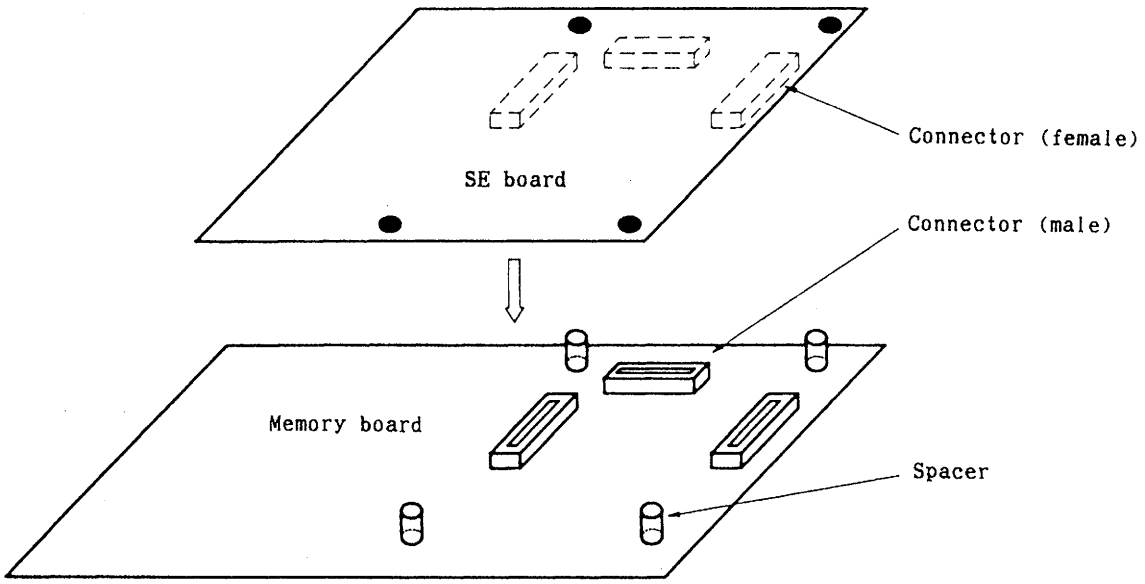



Fig. 4-9 Mounting and Removing SE-17202

After mounting SE-17202, turn on power to IE-17K. Confirm that LED1 on SE-17202 lights (for details, refer to 4.3.6 Supplying power).
Next, connect the probe (EP-17202GF) to SE-17202 connectors J1 and J2, to connect the target system.
Then, attach the inner and outer covers, in this sequence.

### 4.3.6 Supplying power

After mounting SE-17202 to IE-17K, supply power to IE-17K before attaching the inner and outer covers to IE-17K. Confirm that LED1 on SE-17202 lights.
If this indicator does not light, possible causes are as follows:

- The IE-17K power cable is not connected.
- Overcurrent flow through SE-17202 (More than 500 mA. Up to about 500 mA current flow is okey).
- SE-17202 is not correctly mounted.

If the indicator does not light, turn off power to IE-17K, and mount SE-17202 correctly. If the indicator still does not light, SE-17202 may be defective. Consult NEC.
If the operating voltage for your target system is not +5 V, the operating voltage for the target system can be supplied from CN12 or probe to the SE board. For details, refer to 4.1 Using Level Conversion Chip (uPD6705) or 4.2 Supply Voltage to SE Board.

### 4.3.7 Transferring ICE file to IE-17K

IE-17K is connected to a host machine, such as a PC-9800 Series personal computer, to debug the hardware and software for the target system. For IE-17K operations, refer to IE-17K User's Manual.
This section focuses on the procedure to follow, when checking whether or not SE17202 is correctly mounted on IE-17K.
IE-17K is started by applying power to it or, when the power is already applied, by pressing its reset switch, and displays a prompt (@@@>) indicating that it is ready to accept a command. When this happens, load the ICE file (.ICE) for the uPD17202A program, created with an assembler (AS17K), or the ICE file output by using .SP0, and .SP1 commands, to IE-17K by executing the .LP0 or .LP1 command. IE-17K does not operate until this ICE file is loaded. If SE-17202 is correctly mounted to IE-17K at this time, IE-17K displays the following message and prompt BRK>,

indicating that IE-17K is ready to operate as the sole-use in-circuit emulator for the uPD17202A:

Example: When ICE file for uPD17202A is loaded

```
OK
D17202A
BRK>
```

If the above message is not displayed, possible causes are as follows:

- o A target chip other than uPD17202A is mounted to SE-17202.
- o An SE board other than SE-17202 is mounted.
- o An ICE file other than that for uPD17202A has been loaded.
- o SE-17202 is not correctly mounted to IE-17K.
- o The option switch setting is different from that specified by the program.

### 4.3.8 Error messages and remedial actions

IE-17K and SE-17202 displays error messages, if an error, such as an incorrect combination of mounted target chip and ICE file, occurs.
To ensure accurate debugging, an SE board number is registered to SE-17202, and a device number is registered to uPD17202A.
These registration numbers and error messages and remedial actions are described below.

Table 4-4 Device Number and SE Board Number

| Evaluated device | Device number | SE board number |
|---|---|---|
| uPD17202A | 1D | 0C |

Remarks:
1. The device number is the target chip registration number.
2. The SE board number is the SE board registration number.
3. The device number and SE board number are also included in the ICE file data to be loaded. They are used by IE-17K to check the development environments, when the ICE file is loaded. For example, the ICE file, assembled using AS17202, includes a 1D device number and a 0C SE board number.

(1) Error message and remedial action, when a chip other than uPD17202A is mounted to SE-17202

Example:

? IDI INVALID DEVICE ID NUMBER [xx-△△]

xx in this error message indicates the device number for the target chip mounted to the SE board, and △△ indicates the device number included in the loaded ICE file.
If this message is output, check the target chip on the SE board. If a wrong chip is mounted, turn off power to IE-17K once, replace the chip with the correct one, and load the ICE file from the beginning.
If a wrong device file was selected, when the source file was assembled, assemble the source file again, using the correct device file, and load the ICE file.

(2) Error message and remedial action, when an SE board other than SE-17202 is mounted and when an ICE file for a device other than uPD17202A is loaded

Example:

? ISE INVALID SE BOARD NUMBER [□□-▽▽]

□□ in this error message indicates the SE board number for the SE board actually mounted, and ▽▽ indicates the SE board number included in the loaded ICE file. In the case of SE-17202, □□ is 0C, and when the ICE file for uPD17202A is loaded, ▽▽ is 0C.
If this error message has been output, check the SE board and loaded ICE file.

(3) When there is no response from IE-17K

(a) The chances are that SE-17202 is not correctly mounted to IE-17K. Correctly mount the SE board.
(b) Your target system is not correctly connected to the SE board with the probe (EP-17202GF). Check and correct the connection.
(c) The reset circuit for your target system may not operate correctly. In this case, the SE board cannot be accurately reset. Therefore, IE-17K cannot return a response.

(4) When the option switch setting is different from that specified by the program

Example:

? IOS INVALID OPTION SWITCH AT 000x

x in this error message indicates the SE-17202 hardware address, set by the option switch is different from the address specified by the program.
If this error message has been output, correct the option switch setting or the program mask option specification, and load the program.
For details on setting the option switch and address, refer to 4.5 Setting Option Switch.

If any of the above errors (1) to (4) has occurred, immediately take an appropriate remedial action by correcting your target system or source program.

### 4.3.9 Note

- To apply power, first turn on power to IE-17K, and then power to the target system.
- To mount SE-17202 to IE-17K, do not use the SE-17202 reset switch (SW1). Use the IE-17K reset switch to reset SE-17202.

## 4.4 Using SE Board Alone

### 4.4.1 Mounting PROM

To use SE-17202 alone, mount PROM (uPD27C256AD) as the program memory.
Use a PROM that satisfies the following conditions:

$t_{ACC}$ < instruction cycle time/4

$t_{ACC}$: address setting → data output delay time

Instruction cycle time: 4 us (4 MHz) to 500 us (32 kHz)

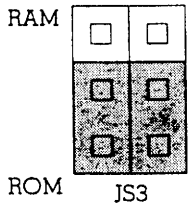
Any of uPD27C256AD-15, 20, and 25 can be used.
It is necessary to write any of the following output files as a program to the PROM:

(1) PROM file (.PRO) for uPD17202A output with the 17K Series assembler (AS17K)
(2) File output for PROM by the .XS0 or .XS1 command of IE-17K

Note: 1. Do not write HEX file (.HEX) output by AS17K for IE-17K to the PROM.
2. The last address in the uPD17202A program memory is 07FFH.

### 4.4.2 Setting ROM/RAM selector jumper switch (JS3)

Set JS3 to the ROM side, as shown in Fig. 4-10.




Remarks: Connect the shaded portion.

Fig. 4-10 Setting JS3 (when SE board alone used)

### 4.4.3 Setting option switch

Set the uPD17202A mask option by the SE-17202 option switch. For details on the setting, refer to 4.5 Setting Option Switch.

### 4.4.4 Setting target circuit on SE board

To use the target circuit on the SE board, it is necessary to set the jumper switches on the SE board (JS4, JS5, JS6, JS7, JS8, JS9, JS10, and DIP switch (SW2)). For details on the setting, refer to 4.6 Setting Target Circuit on SE Board.

### 4.4.5 Supplying power

Be sure to supply +5 V$\pm$5% ($V_{CC}$) from an external power source to SE-17202 through CN11.
When $V_{CC}$ is correctly supplied, LED1 on SE-17202 lights.
If this indicator does not light, possible causes are as follows:

- Power is not supplied.
- Overcurrent flowing through SE-17202 (More than 500 mA. Up to about 500 mA current flow is okey).

If the indicator does not light, check to see if the external power supply (+ side) and GND are correctly connected. There is also a possibility of overcurrent; therefore, measure the current. The normal value is 200 mA max. without a load.
If the your target system's operating voltage is not +5 V, the target system operating voltage can be supplied from CN12 or probe to the SE board. For details, refer to 4.1 Using Level Conversion Chip (uPD6705) or 4.2 Supply Voltage to SE Board.

### 4.4.6 Executing program

Connect SE-17202 and the target system, as shown in Fig. 4-11. When power to the target system is turned on, the power is supplied to SE-17202, power-ON reset function is effected, and the program written to PROM is executed, starting from address 0. When the reset switch (SW1) on SE-17202 is pressed, forced reset function is effected, and the program written to the PROM is executed, starting from address 0, the same as when power-ON reset is effected.

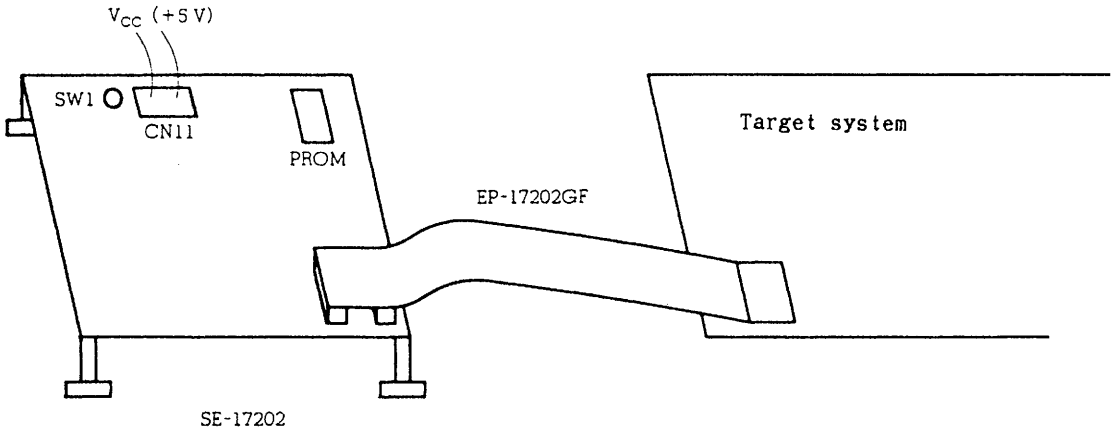



Fig. 4-11 Connection When SE-17202 Alone Is Used

### 4.4.7 Reset switch (SW1) Function

SW1 resets SE-17202, when the SE board alone is used.
Do not press this switch, when SE-17202 is mounted on IE-17K.

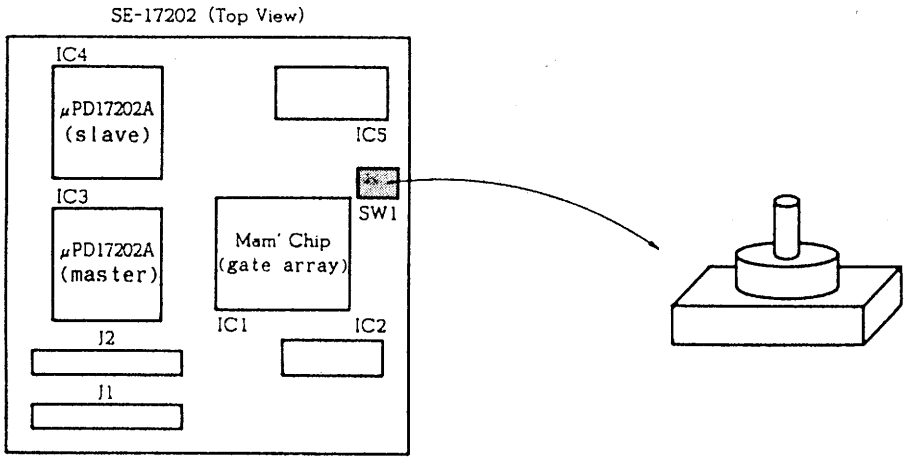



Fig. 4-12 SW1

## 4.5 Setting Option Switch

uPD17202A has the following mask options, which can be selected by the SE-17202 option switch :

| Mask option | Selected value |
|---|---|
| $\overline{\text{RESET}}$ pin | ① No internal resistor ② Pull-up resistor connected |
| System clock | ① System clock is 32 kHz after reset<br>② System clock is 4 MHz after reset |
| 32-kHz oscillator circuit | ① 32-kHz oscillator circuit is used<br>② 32-kHz oscillator circuit is not used |
| $P0A_0$-$P0A_3$ pin<br>$P0B_0$-$P0B_3$ pin | ① No internal resistor ② Pull-up resistor connected |

The uPD17202A, with the following mask options, is mounted to SE-17202:

- o $\overline{\text{Reset}}$ pin
  No internal resistor
- o System clock
  System clock is 4 MHz after reset.
- o 32-kHz oscillator circuit
  32-kHz oscillator circuit is used.
- o $P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$ pin
  No internal resistor

The option switch is located on SE-17202, as shown in Fig. 4-13.

SE-17202 (Top View)

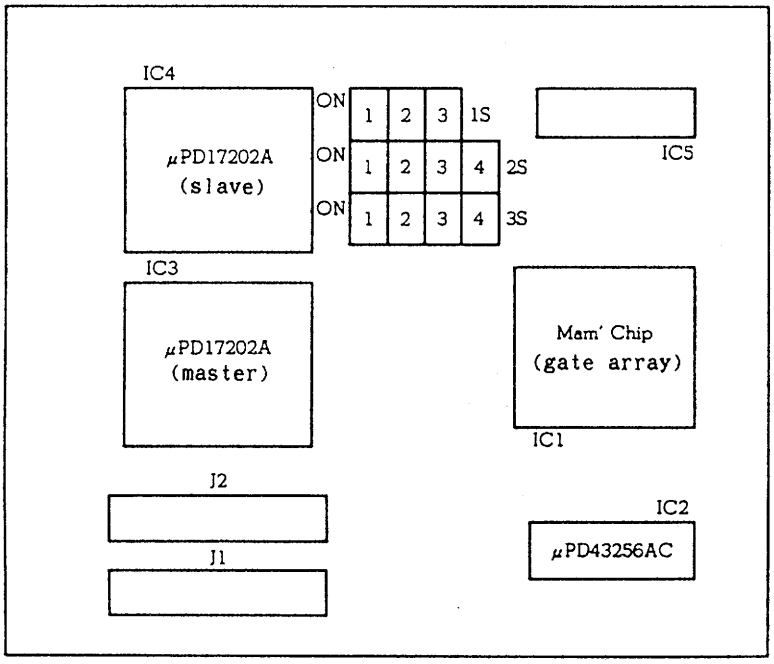



Fig. 4-13 Option Switch Location

The option switch specifies mask options according to Table 4-5.

Table 4-5 Setting Option Switch

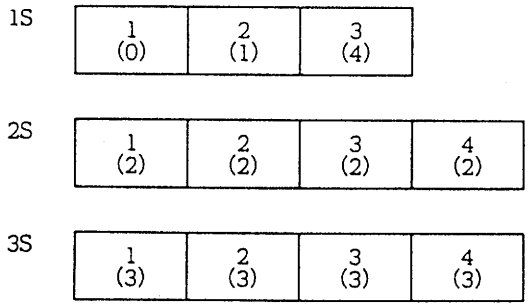
| Switch no. | | ON | OFF |
|---|---|---|---|
| 1S | 1 | Pulls up $\overline{\text{RESET}}$ pin | Does not pull up $\overline{\text{RESET}}$ pin |
| | 2 | Uses 32-kHz system clock after reset | Uses 4-MHz system clock after reset |
| | 3 | Does not use 32-kHz clock | Uses 32-kHz clock |
| 2S | 1 | $POA_0$ pin is connected to pull-up resistor | $POA_0$ pin is not connected to pull-up resistor |
| | 2 | $POA_1$ pin is connected to pull-up resistor | $POA_1$ pin is not connected to pull-up resistor |
| | 3 | $POA_2$ pin is connected to pull-up resistor | $POA_2$ pin is not connected to pull-up resistor |
| | 4 | $POA_3$ pin is connected to pull-up resistor | $POA_3$ pin is not connected to pull-up resistor |
| 3S | 1 | $POB_0$ pin is connected to pull-up resistor | $POB_0$ pin is not connected to pull-up resistor |
| | 2 | $POB_1$ pin is connected to pull-up resistor | $POB_1$ pin is not connected to pull-up resistor |
| | 3 | $POB_2$ pin is connected to pull-up resistor | $POB_2$ pin is not connected to pull-up resistor |
| | 4 | $POB_3$ pin is connected to pull-up resistor | $POB_3$ pin is not connected to pull-up resistor |

Note: When 1S2 is set to ON (to use the 32-kHz system clock after reset), 1S3 must not be set to ON (to not use the 32-kHz clock).

With the 17K Series Assembler (AS17K), the specifications for the mask option are described on the source program. The .LP0 or .LP1 command for IE-17K tests whether or not the SE-17202 option switch setting coincides with the setting specified by the program, when the ICE file is loaded. If a discrepancy is found, IE-17K displays the following error message:

? IOS INVALID OPTION SWITCH AT 000x

This error message indicates that the value for the option switch at address x on the SE-17202 hardware does not agree with the mask option specified by the program (refer to Fig. 4-14).
If this message is output, correct the setting for the option switch and the program specification , and load the program.




Remarks: Figures in ( ) indicate addresses for the option switch on hardware.

**Fig. 4-14 Option Switch Address**

## 4.6 Setting Target Circuit on SE Board

SE-17202 is equipped with a target circuit for some uPD17202A pins. To use the SE-17202 target circuit, it is necessary to set jumper switches JS4, JS5, JS6, JS7, JS8, JS9, and JS10, and DIP switch SW2. These jumper switches are factory-set, not to use the SE-17202 target circuit. Figure 4-15 shows the layout for the jumper switches and DIP switch on SE-17202.

SE-17202 (Top View)

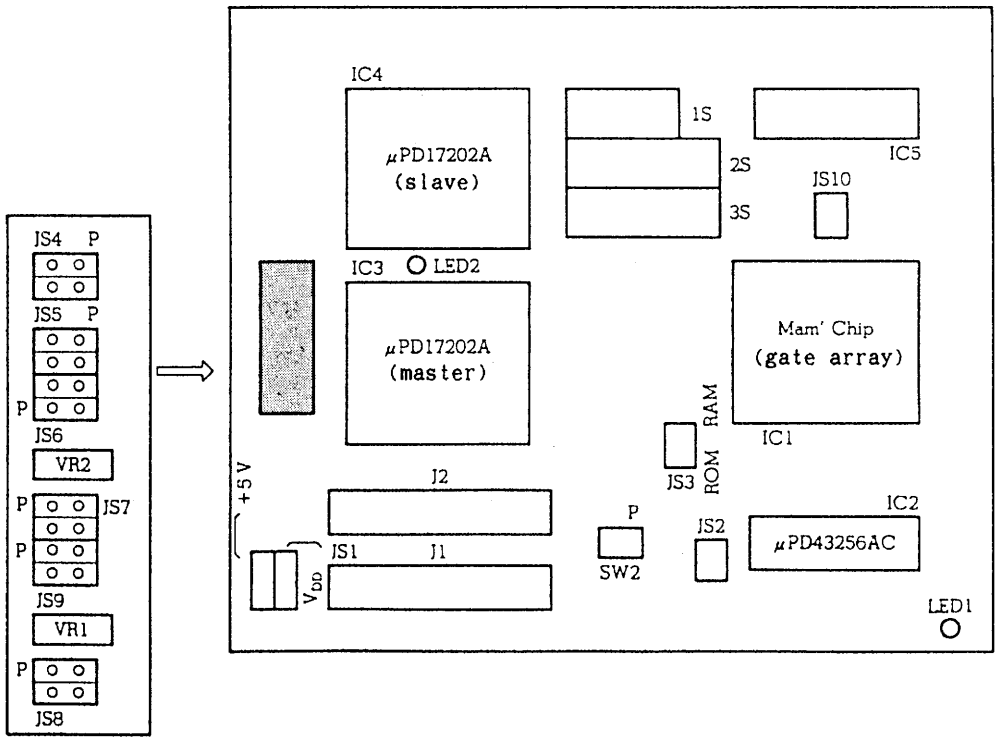



Fig. 4-15 Jumper Switches Layout

### 4.6.1 Setting jumper switch JS4

Jumper switch JS4 is connected to the capacitor side (opposite side from to P), when a 0.47-uF capacitor is connected to the $V_{LCD2}$ pin for uPD17202A on SE-17202.

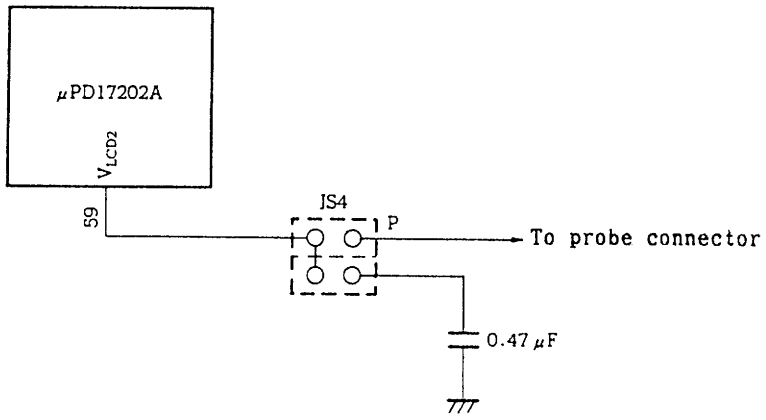



Fig. 4-16 Circuit Related to JS4

### 4.6.2 Setting jumper switch JS5

Jumper switch JS5 is connected to the capacitor side (opposite side from P), when a 0.47-uF capacitor is connected to the $V_{LCD1}$ pin for uPD17202A on SE-17202.

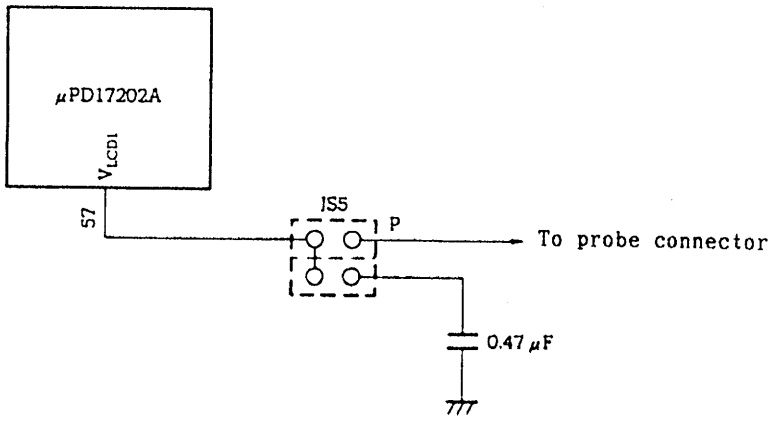



Fig. 4-17 Circuit Related to JS5

### 4.6.3 Setting jumper switches JS6 and JS7

Jumper switch JS6 is connected to the capacitor side (opposite side from P), when a 0.47-uF capacitor is connected to the $V_{LCD0}$ pin for uPD17202A on SE-17202.
When jumper switch JS7 is connected to the circuit side (opposite side from P), adjust the LCD display voltage, using variable resistor VR2 (2 MΩ) on SE-17202.

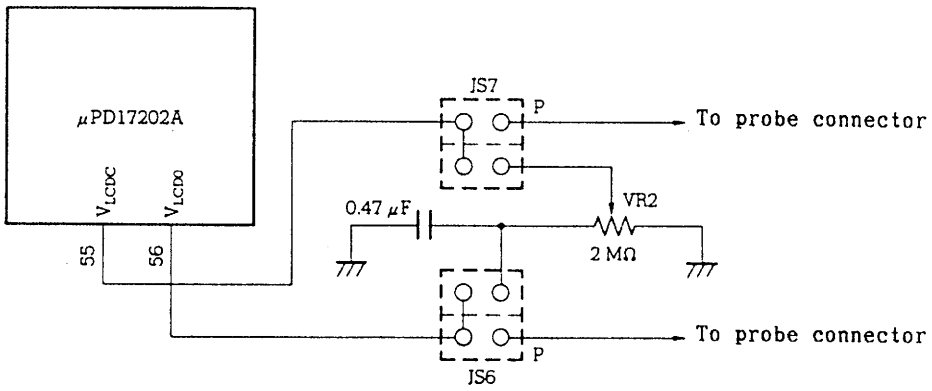



Fig. 4-18 Circuit Related to JS6 and JS7

### 4.6.4 Setting jumper switch JS8

Jumper switch JS8 is connected to the SE-17202 circuit side (opposite side from P) when the low-voltage detection adjuster circuit for uPD17202A is used. At this time, adjust the detection voltage, using variable resistor VR1 (2 MΩ) on SE-17202.

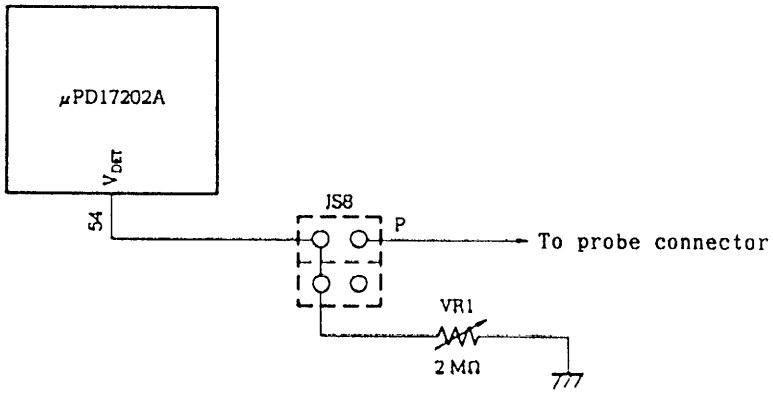



Fig. 4-19 Circuit Related to JS8

### 4.6.5 Setting jumper switch JS9

Jumper switch JS9 is connected to the capacitor side (opposite side from P), when a 0.1-uF capacitor is connected to the $V_{REG}$ pin for uPD17202A on SE-17202.

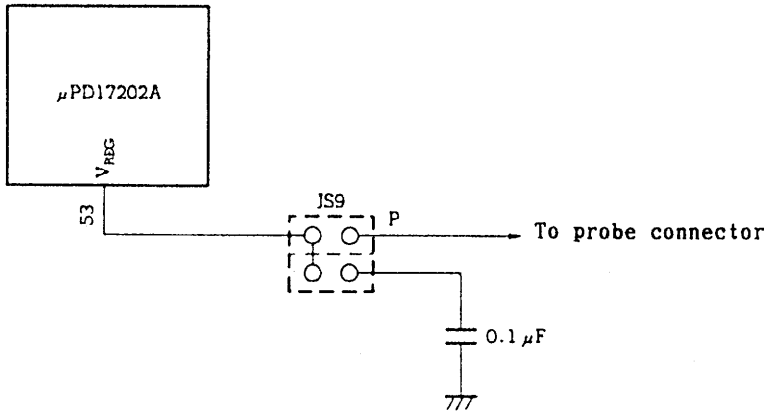



Fig. 4-20 Circuit Related to JS9

### 4.6.6 Setting jumper switch JS10

Jumper switch JS10 is used to reset uPD17202A to SE-17202 using the uPD17202A $\overline{WDOUT}$ pin output. When this jumper switch is connected, and when the $\overline{WDOUT}$ pin goes low, SE-17202 inputs a reset signal to uPD17202A. When the jumper switch is opened, SE-17202 does not reset uPD17202A with the $\overline{WDOUT}$ pin output.

### 4.6.7 Setting DIP switch SW2

DIP switch SW2 is set to the circuit side (opposite side from P) to add a 0.47-uF booster capacitor between uPD17202A CAPH and CAPL pins. When this switch is turned ON/OFF, SW2-1 and SW2-2 in the following figure also turn ON/OFF:

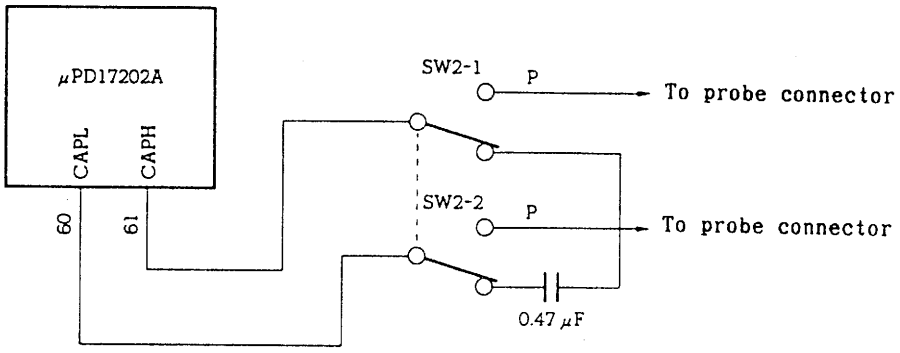



Fig. 4-21 Circuit Related to SW2

### 4.6.8 LED1 and LED2

(1) LED1

LED1 is used to monitor the SE-17202 power supply status.

- o When it lights : Power is correctly supplied.
- o When it goes off: Power is not correctly supplied.

For details, refer to 4.3.6 Supplying power and 4.4.5 Supplying power.

(2) LED2

LED2 is used to monitor the XEN flag status for the system clock control register.

- o When it lights : Main clock oscillation is stopped (XEN = 0).
- o When it goes off: Main clock oscillation is enabled (XEN = 1).

Note: Main clock oscillation stoppage cannot be monitored in STOP mode with LED2.

## 4.7 Changing Oscillation Frequency

To replace the crystal oscillator (4 MHz) mounted on SE-17202 for main clock (X) oscillation, use a crystal oscillator, as illustrated in Fig. 4-22.
To measure the oscillation frequency, use the CH2 pin on SE-17202.

SE-17202 (Top View)

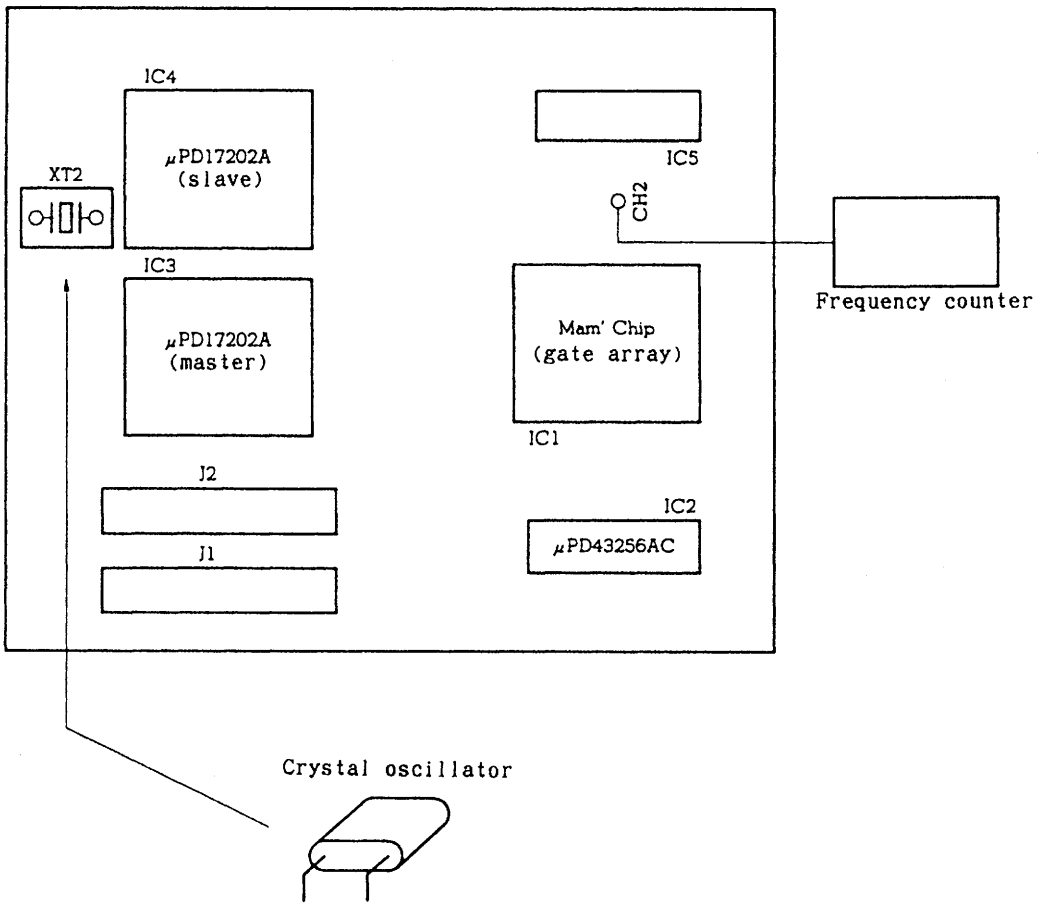
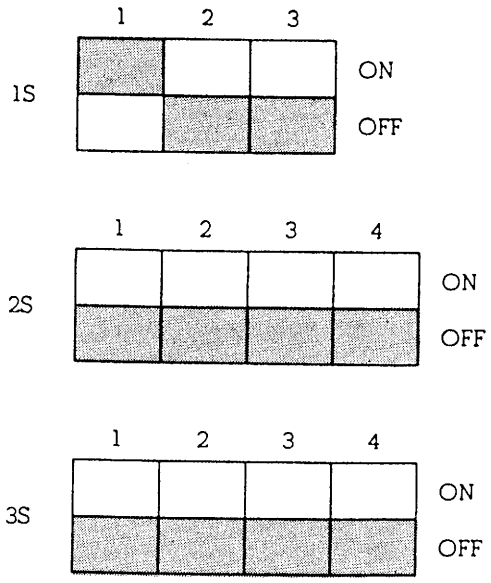



Fig. 4-22 Changing Oscillation Frequency

## 4.8 Factory-Set Conditions

As a factory-set condition for shipment, the IC2 (program memory), jumper switches, option switches, and crystal oscillator for SE-17202 are set as follows:

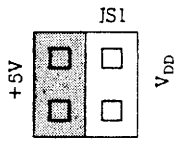
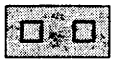
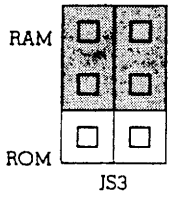
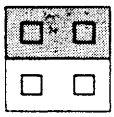
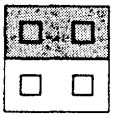
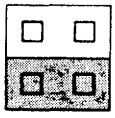
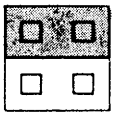
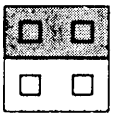
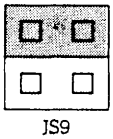
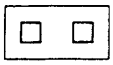
- o IC2 (program memory)
  RAM (uPD43256AC-12) is mounted.
- o Jumper switches
  Set as shown in Table 4-6.
- o DIP switch (SW2)
  Set to ON (probe connector side).
- o Option switches (1S to 3S)
  All 1S to 3S, except 1 for 1S, are set to OFF.




Remarks: ▩ : set side

- o Crystal oscillator
  A 32-kHZ oscillator is connected to XT1, and a 4-MHz crystal oscillator is connected to XT2.

Table 4-6 Setting Jumper Switches

| Jumper switch | Factory-set condition |
|---|---|
| JS1   | Set to +5 V side. |
| JS2   | Mounted. |
| JS3   | Set to RAM side. |
| JS4   | Set to probe connector side. |
| JS5   | Set to probe connector side. |
| JS6   | Set to probe connector side. |
| JS7   | Set to probe connector side. |
| JS8   | Set to probe connector side. |
| JS9   | Set to probe connector side. |
| JS10   | Not mounted |

Remarks: ▭ : Connected

# CHAPTER 5 CONNECTOR PINS

## 5.1 Probe Connector (J1)

| J1 pin no. | Pin name (IC pin no.) | J1 pin no. | Pin name (IC pin no.) | J1 pin no. | Pin name (IC pin no.) |
|---|---|---|---|---|---|
| 1 | GND | 21 | GND | 41 | $V_{REG}$ (53) |
| 2 | $LCD_2$ (23) | 22 | $LCD_{21}$ (4) | 42 | GND |
| 3 | GND | 23 | $LCD_{23}$ (2) | 43 | NC |
| 4 | $LCD_6$ (19) | 24 | GND | 44 | $XT_{OUT}$ |
| 5 | $LCD_7$ (18) | 25 | $COM_3/LCD_{24}$ (1) | 45 | GND |
| 6 | GND | 26 | NC | 46 | $XT_{IN}$ |
| 7 | NC | 27 | GND | 47 | $\overline{RESET}$ (49) |
| 8 | $LCD_{18}$ (7) | 28 | $COM_2/LCD_{25}$ (64) | 48 | GND |
| 9 | GND | 29 | CAPH (61) | 49 | $X_{OUT}$ |
| 10 | $LCD_{11}$ (14) | 30 | GND | 50 | NC |
| 11 | $LCD_{12}$ (13) | 31 | NC | 51 | GND |
| 12 | GND | 32 | $V_{LCD2}$ (59) | 52 | $X_{IN}$ |
| 13 | $LCD_{14}$ (11) | 33 | GND | 53 | REM (45) |
| 14 | NC | 34 | $V_{LCD1}$ (57) | 54 | GND |
| 15 | GND | 35 | $V_{LCD0}$ (56) | 55 | $POD_3$ (43) |
| 16 | $LCD_{16}$ (9) | 36 | GND | 56 | TMOUT/LED (44) |
| 17 | $LCD_9$ (16) | 37 | $V_{LCDC}$ (55) | 57 | GND |
| 18 | GND | 38 | NC | 58 | $POD_2$ (42) |
| 19 | NC | 39 | GND | 59 | $V_{DD}$ (46) |
| 20 | $LCD_{20}$ (5) | 40 | $V_{DET}$ (54) | 60 | GND |

## 5.2 Probe Connector (J2)

| J2 pin no. | Pin name (IC pin no.) | J2 pin no. | Pin name (IC pin no.) | J2 pin no. | Pin name (IC pin no.) |
|---|---|---|---|---|---|
| 1 | $LCD_5$ (20) | 21 | GND | 41 | $POC_2$ (38) |
| 2 | $LCD_8$ (17) | 22 | $LCD_0$ (25) | 42 | GND |
| 3 | GND | 23 | $COM_1$ (63) | 43 | NC |
| 4 | $LCD_{10}$ (15) | 24 | GND | 44 | $POB_3$ (35) |
| 5 | $LCD_4$ (21) | 25 | $COM_0$ (62) | 45 | GND |
| 6 | GND | 26 | NC | 46 | $POB_1$ (33) |
| 7 | NC | 27 | GND | 47 | $POA_0$ (28) |
| 8 | $LCD_{13}$ (12) | 28 | CAPL (60) | 48 | GND |
| 9 | GND | 29 | INT (27) | 49 | $POA_3$ (31) |
| 10 | $LCD_3$ (22) | 30 | GND | 50 | NC |
| 11 | $LCD_{15}$ (10) | 31 | NC | 51 | GND |
| 12 | GND | 32 | $POD_1$ (41) | 52 | $POA_1$ (29) |
| 13 | $LCD_{17}$ (8) | 33 | GND | 53 | $POB_2$ (34) |
| 14 | NC | 34 | NC | 54 | GND |
| 15 | GND | 35 | $POC_3$ (39) | 55 | $POB_0$ (32) |
| 16 | $LCD_{19}$ (6) | 36 | GND | 56 | $POA_2$ (30) |
| 17 | $LCD_1$ (24) | 37 | $POD_0$ (40) | 57 | GND |
| 18 | GND | 38 | NC | 58 | $POC_0$ (36) |
| 19 | NC | 39 | GND | 59 | $\overline{WDOUT}$ (50) |
| 20 | $LCD_{22}$ (3) | 40 | $POC_1$ (37) | 60 | GND |

# CHAPTER 6 PROBE AND CONVERSION SOCKET DIMENSIONS

## 6.1 Probe Appearance

Product name: EP-17202GF

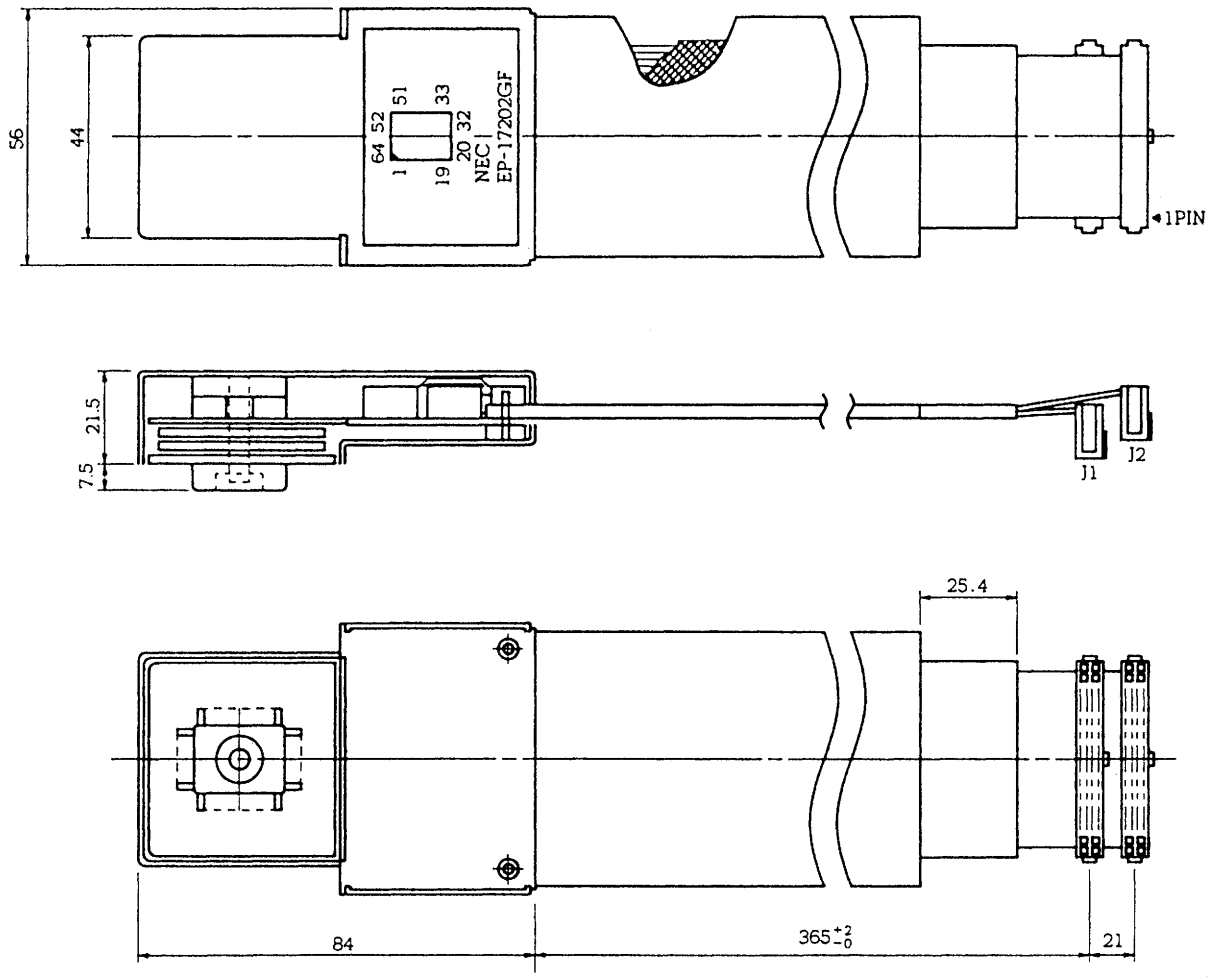



Fig. 6-1 Probe Appearance

## 6.2 Conversion Socket (EV-9200G-64) Appearance and Recommended Pattern on PC Board

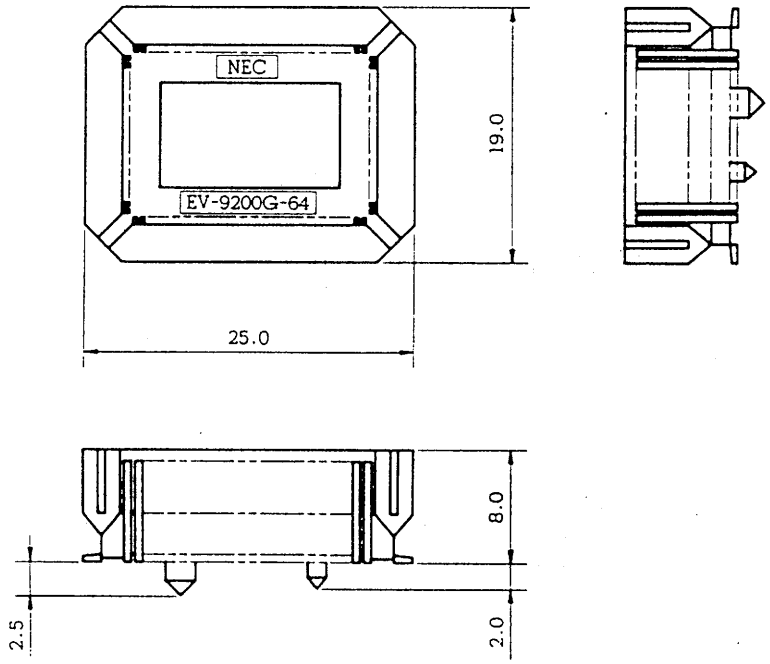



Fig. 6-2 EV-9200G-64 Appearance

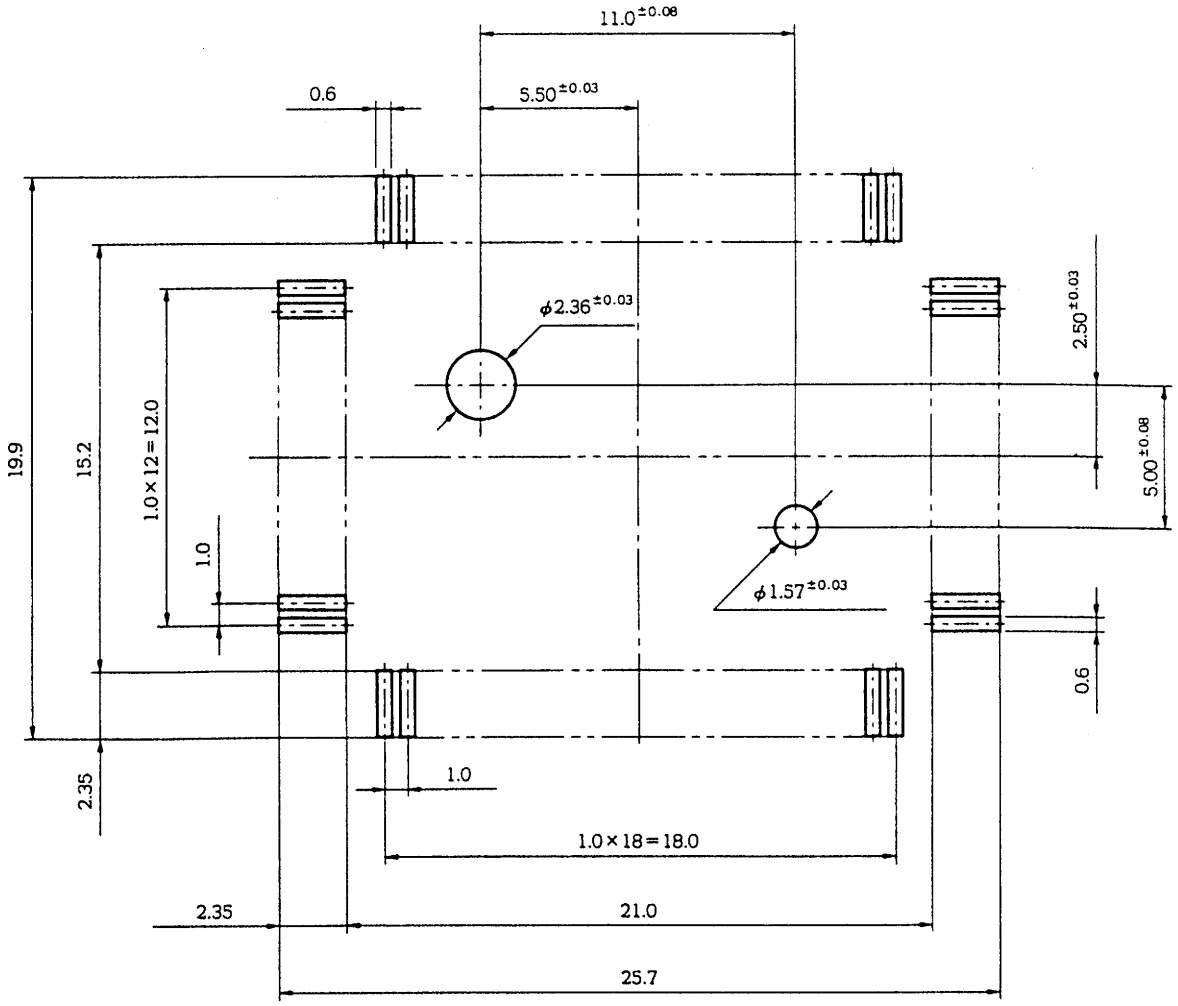



Fig. 6-3 Recommended Pattern for EV-9200G-64 on PC Board

Phase-out/Discontinued

Phase-out/Discontinued