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RENESAS

USER'S MANUAL

Phase-out/Discontinued

SE-17001

17K SERIES

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USER'S MANUAL

NEC

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SE-17001

17K SERIES

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Phase-out/Discontinued

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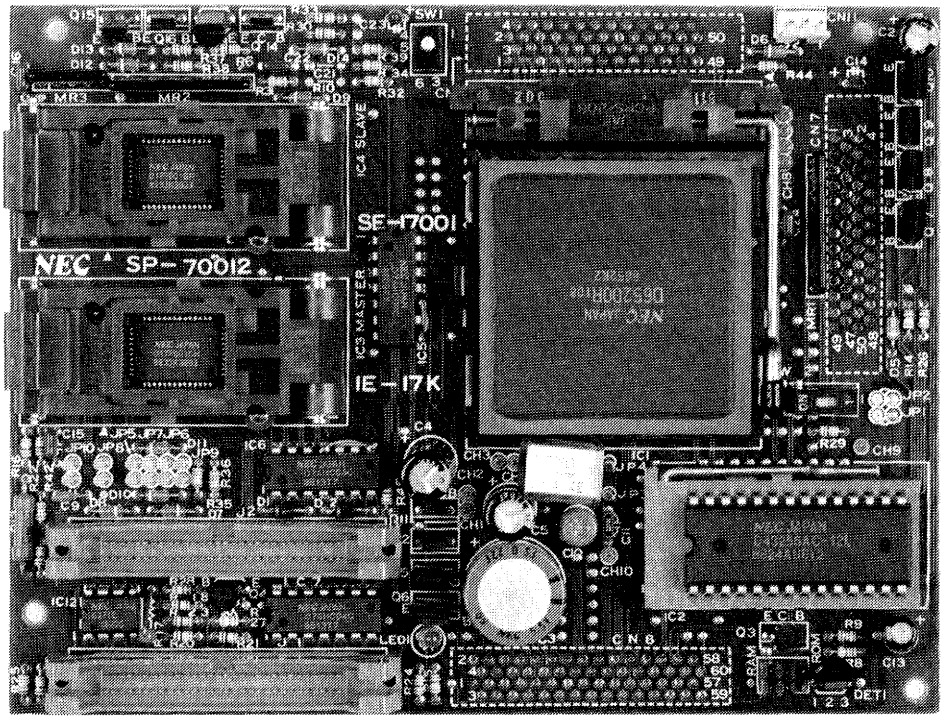
CHAPTER 1 INTRODUCTION

SE-17001 is a system evaluation board for 4-bit single chip microcomputer μPD17001GH. SE-17001 can be used with the 17K series common in-circuit emulator IE-17K, and also SE-17001 can be used alone.

μPD17001GH is used as an interface with the target system. Therefore, the function of SE-17001 is the same as μPD17001GH.

In case of connecting SE-17001 to the target system, use the option EP-17001GH (80 pins flat package for μPD17001GH).

Fig. 1-1 External Appearance



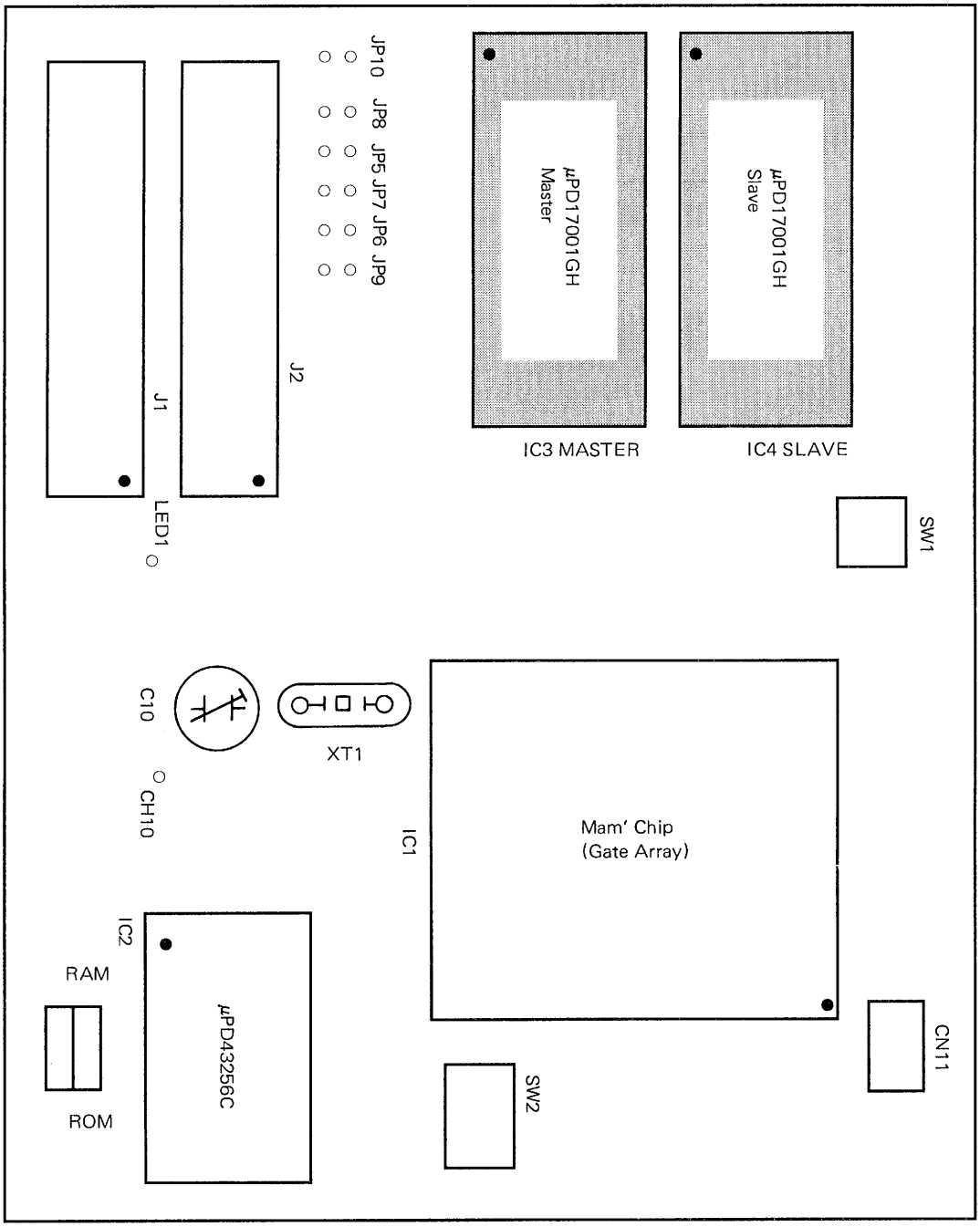
Phase-out/Discontinued

CHAPTER 2 SPECIFICATIONS

Model name	:	SE-17001
Program memory	:	• using SE-17001 with IE-17K μPD43256C • using SE-17001 alone μPD27C256D μPD43256C is mounted as shipped.
Data memory	:	bult-in RAM of μPD17001GH (4 bits x 224)
Oscillating frequency	:	4.5 MHz (using crystal oscillator) 4.5 MHz crystal oscillator is installed as shipped
Instruction cycle	:	4.44 μs
Operating temperature	:	+10 to +40 °C
Storage temperature	:	−10 to +50 °C (but without condensation)
Power supply	:	5 V ± 5 % • When using SE-17001 with IE-17k, the power is supplied from IE-17k. • When using SE-17001 alone, the power is supplied from the probe (EP-17001GH) or the connector CN11 on SE-17001.
Current consumption	:	150 mA (MAX.) (no load, using μPD27C256D as a program memory)
Board dimensions	:	150 mm x 114 mm x 35 mm

Phase-out/Discontinued

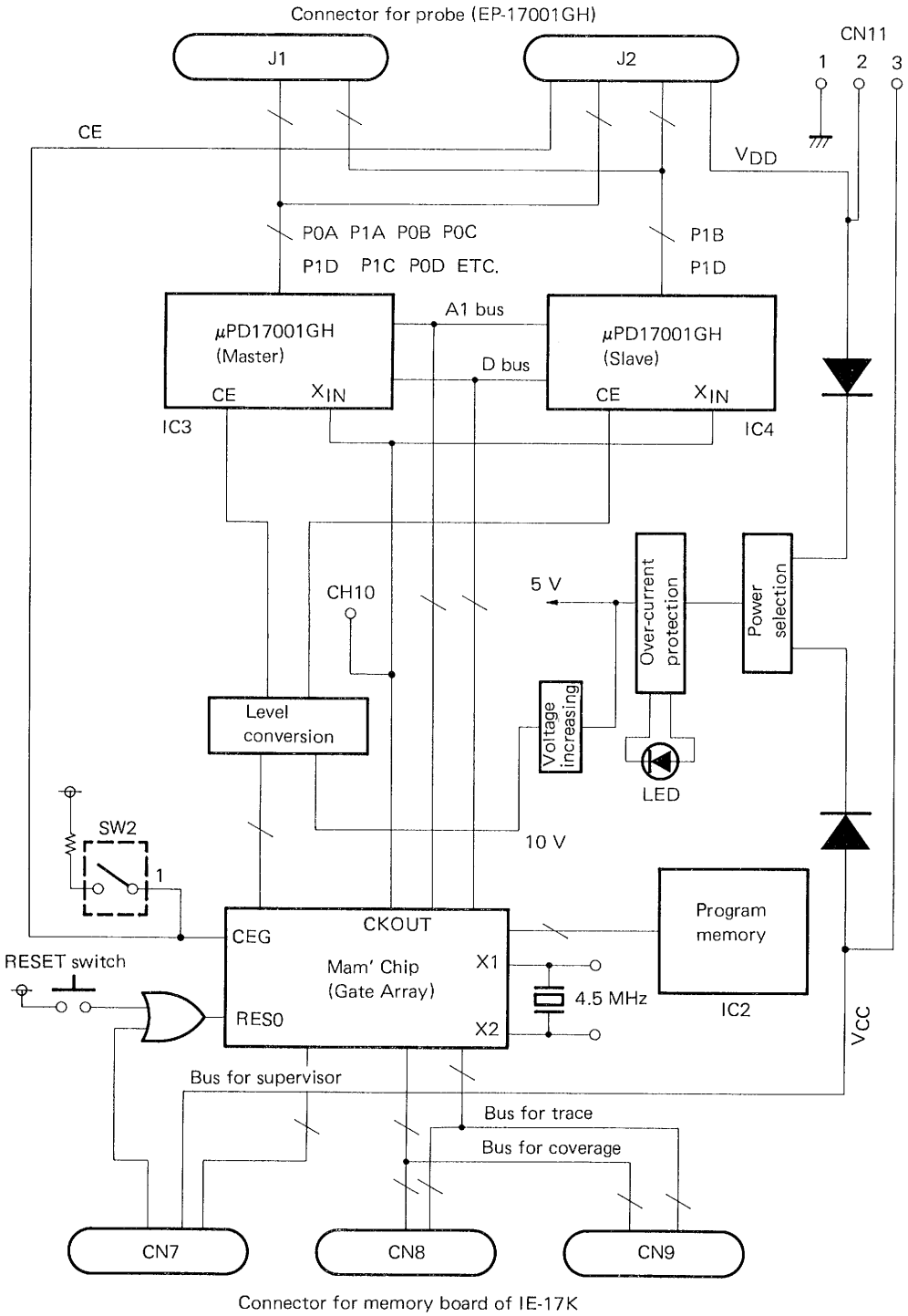
Fig. 2-1 SE-17001 Component Layout



Phase-out/Discontinued

CHAPTER 3 BLOCK DIAGRAM

Fig. 3-1 Block Diagram of SE-17001



Phase-out/Discontinued

CHAPTER 4 OPERATING PROCEDURES

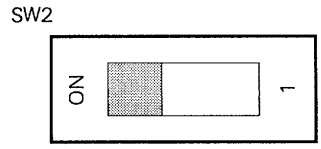
4.1 HOW TO USE SE-17001 WITH IE-17K

(1) DIP SWITCH(SW2) SETTING

The DIP switch(SW2) selects that the CE signal of μPD17001GH is pulled up or not. When pulled up, it is set as shown in Fig. 4-1. When not pulled up, it is set as shown in Fig. 4-2.

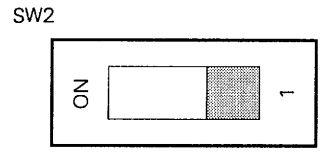
Pull up the CE signal when using SE-17001 without the target system or when the CE signal is not supplied from the target system. The CE signal need not be pulled up when the CE signal is supplied from the target system.

Fig. 4-1 SW2 Setting (when pulled up)



NOTE: ▒▒ is the setting side.

Fig. 4-2 SW2 Setting (when not pulled up)



NOTE: ▒▒ is the setting side.

Phase-out/Discontinued

When SE-17001 is shipped, the DIP switch(SW2) is set as shown in Fig. 4-2.

(2) RAM mounting

Mount the RAM (μPD43256C) as a program memory.

Use the RAM mounted on SE-17001 as shipped.

When using the RAM other than μPD43256C, mount the RAM that accepts the following condition.

$t_{ACC} < 1.11\ \mu s$

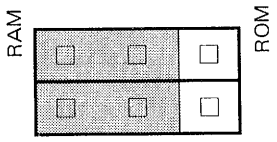
(t_{ACC} : Address setting → Data output delay time)

μPD43256C-10, 12 and 15 are available.

(3) ROM/RAM change jumper switch settings

Set the ROM/RAM change jumper switches to the RAM side as shown in Fig. 4-3.

Fig. 4-3 ROM/RAM Change Jumper Switch Setting



NOTE: ▒ is the connecting position.

(4) Installation and removal of SE-17001 into and from IE-17K

To install SE-17001 into IE-17K, firstly remove the external cover and the inside cover. Fig. 4-4 shows the external view of IE-17K after removing the external cover.

Removing the inside cover, the memory board can be seen. Three connectors are located on the memory board. SE-17001 can be installed into IE-17K by putting three connectors (CN7, 8 and 9) on SE-17001 into three connectors on IE-17K. (See Fig. 4-5)

When installing SE-17001, push it down vertically and check if three connectors are connected firmly.

SE-17001 can be removed from IE-17K by lifting it up vertically. (See Fig. 4-5)

Phase-out/Discontinued

Fig. 4-4 External View of IE-17K (after removing the external cover)

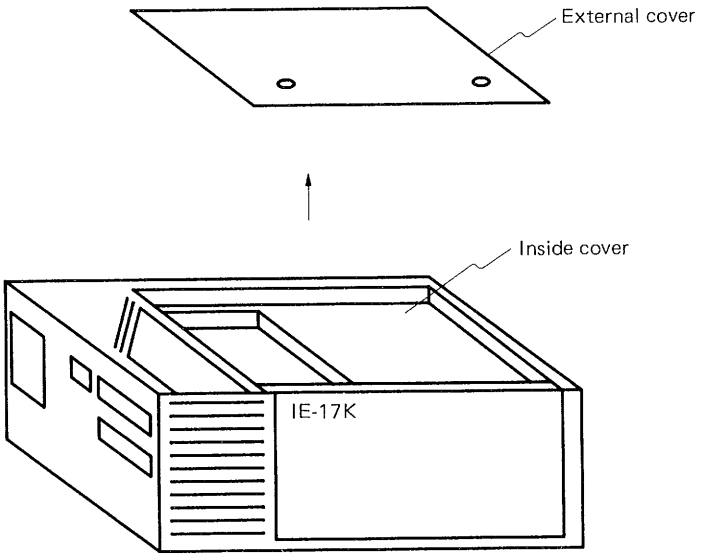
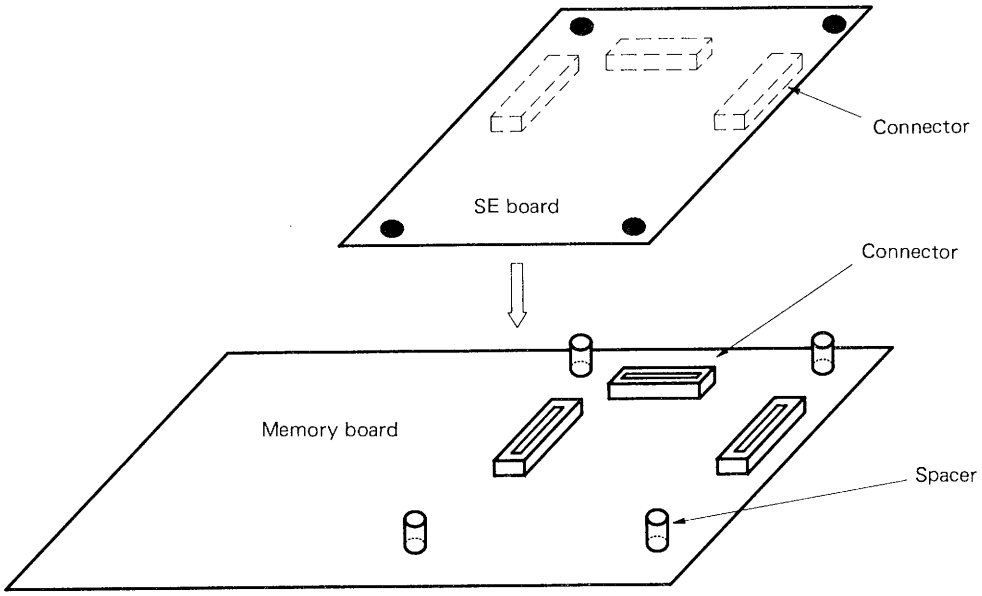


Fig. 4-5 Installation and Removal of SE-17001



Phase-out/Discontinued

After installing SE-17001, turn on the power of IE-17K before installing the inside cover and the external cover. And check if the LED on SE-17001 lights.

The LED does not light in the following cases.

- No connection of the IE-17K power cord
- Over-current in SE-17001 (about 500 mA and more)
- Incorrect installing of SE-17001

If the LED does not light, turn off the power of IE-17K and take out SE-17001 and then reinstall it. If it does not light yet, the trouble may occur.

Next, connect the probe (EP-17001GH) to the connectors J1 and J2 on SE-17001 in order to connect to the target system.

Finally, install the inside cover and the external cover.

(5) Use of IE-17K

Connecting IE-17K to the host machine of PC-9800 series and so on, IE-17K can be used to debug the hardware and the software of the target system. With regard to the operation of IE-17K, refer to "IE-17K USER'S MANUAL".

The procedure to check if SE-17001 is correctly installed is described below.

By turning on the power or pressing the RESET switch of IE-17K when the power is already supplied, IE-17K is activated and displays a prompter (@@@>) which indicates the command is acceptable. Next, by .LP command load the HEX file (.HEX) of the μPD17001GH program made by the assembler (AS17K) or the HEX file output by .SP command. IE-17K does not operate till the HEX file is loaded. If SE-17001 is correctly installed to IE-17K, the following messages are displayed and a prompter is "BRK>".

And then IE-17K becomes the in-circuit emulator for μPD17001GH.

```
OK
D17001

BRK>
```

When the above messages are not displayed, the causes seem as follows.

- If the device other than μPD17001GH is mounted on SE-17001, the following error message is displayed.

```
? IDI INVALID DEVICE ID NUMBER [XX-03]
```

"03" indicates the device number of μPD17001GH and "XX" indicates the actually mounted device number.

- If the SE board other than SE-17001 is installed, the following error message is displayed.

```
? ISE INVALID SE BOARD NUMBER [XX-03]
```

"03" indicates the SE board of SE-17001 and "XX" indicates the actually installed SE board number.

- If the HEX file other than the μPD17001GH is loaded, the following error message is displayed.

```
? IDI INVALID SE BOARD NUMBER [03-XX]
```

"03" indicates the SE board of SE-17001 and "XX" indicates the SE board number of SE board that corresponds to the loaded HEX file.

- In case that SE-17001 is not installed to IE-17K correctly. When loading the HEX file by .LP command, after for a while, without the response from IE-17K, there is a possibility of the incorrect installing of SE-17001.

In case of the incorrect installing of SE-17001, reinstall it correctly. And also when loading the HEX file other than the μPD17001GH, load the HEX file of the μPD17001GH again.

Phase-out/Discontinued

(6) NOTE

- When turning on the power, turn on the power to IE-17K and then the target system.
- Never use the RESET switch on SE-17001. When resetting IE-17K, use the RESET switch on IE-17K.

Phase-out/Discontinued

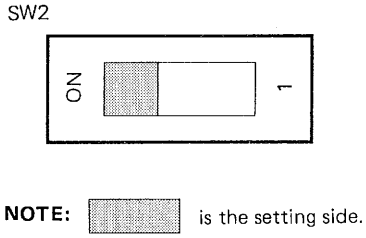
4.2 HOW TO USE SE-17001 ALONE

(1) DIP SWITCH(SW2) SETTING

The DIP switch(SW2) selects that the CE signal of μPD17001GH is pulled up or not. When pulled up, it is set as shown in Fig. 4-6. When not pulled up, it is set as shown in Fig. 4-7.

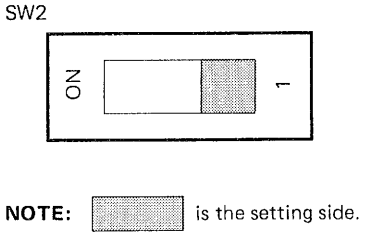
Pull up the CE signal when the CE signal is not supplied from the target system. The CE signal need not be pulled up when the CE signal is supplied from the target system.

Fig. 4-6 SW2 Setting (when pulled up)



NOTE: ▒▒▒ is the setting side.

Fig. 4-7 SW2 Setting (when not pulled up)



NOTE: ▒▒▒ is the setting side.

When SE-17001 is shipped, the DIP switch(SW2) is set as shown in Fig. 4-7.

Phase-out/Discontinued

(2) PROM mounting

When using SE-17001 alone, mount the PROM (μPD27C256D) as a program memory. Mount the PROM that accepts the following condition.

$t_{ACC} < 1.11\ \mu s$

(t_{ACC} : Address setting → Data output delay time)

μPD27C256D-15, 20 and 25 are available.

It is required to write whichever output file as below into the PROM as a program.

- PROM file (.PRO) for μPD17001GH made by the assembler (AS17K) for μPD17000 series.
  Never write the HEX file (.HEX) made by AS17K into the PROM.
- File for the PROM made by .XS command of IE-17K.

[Note for PROM writing]

The last program memory address of the μPD17001GH is 0EFBH. However, when using SE-17001 alone, the program memory up to the address 0FFFH are available.

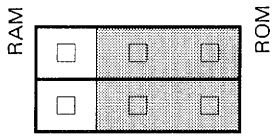
When making the mask ROM, the part of the program memory that address higher than the address 0EFBH is eliminated.

Assure that the last program memory address is 0EFBH, when writing the program into the PROM that corresponds to the mask ROM.

(3) ROM/RAM change jumper switch settings

Set the ROM/RAM change jumper switches to the ROM side as shown in Fig. 4-8.

Fig. 4-8 ROM/RAM Change Jumper Switch Setting



NOTE: ▒▒▒ is the connecting position.

(4) Power supply

SE-17001 is supplied with the power from the target system via the probe (EP-17001GH) or from the CN11 on SE-17001.

When using the CN11, two ways are provided. When the power that is supplied from the CN11 would be supplied to the target system, connect the power source (+side) to the pin No. 2 of the CN11 and GND to the pin No. 1 of the CN11. At this time the power is also supplied to the target system via the probe.

When the power that is supplied from the CN11 would not be supplied to the target system, connect the power source (+side) to the pin No. 3 of the CN11 and GND to the pin No. 1 of the CN11.

The power supply voltage must be 5 V ± 5 %.

When the power is supplied normally, the LED on SE-17001 lights.

The LED does not light in the following cases.

- No supplying power to SE-17001
- Over-current in SE-17001 (about 500 mA and more)

Phase-out/Discontinued

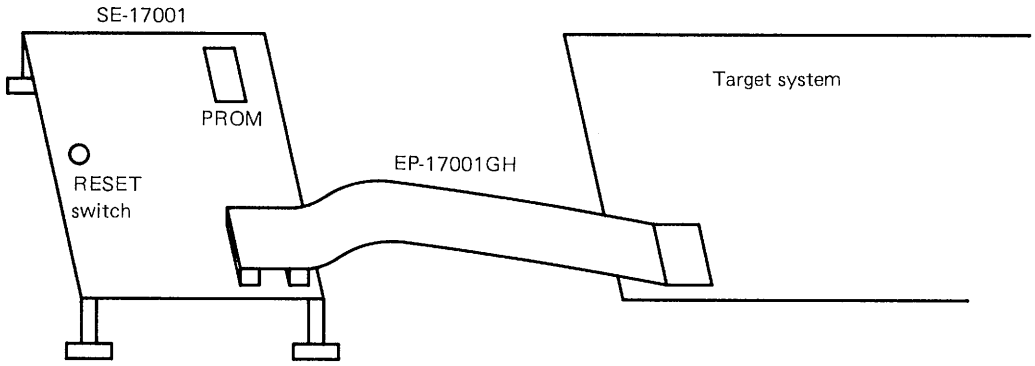
(5) Program executing

Connect the target system to SE-17001 as shown in Fig. 4-9.

Starting to supply the power to target system, the power is supplied to SE-17001 and the POWER-ON-RESET procedure is activated and the program written in the PROM is executed from the location 0.

By pressing the RESET switch on SE-17001, SE-17001 is reset forcely. As same as the POWER-ON-RESET procedure, the program written in the PROM is executed from the location 0.

Fig. 4-9 Example of Connection of SE-17001 to the Target System

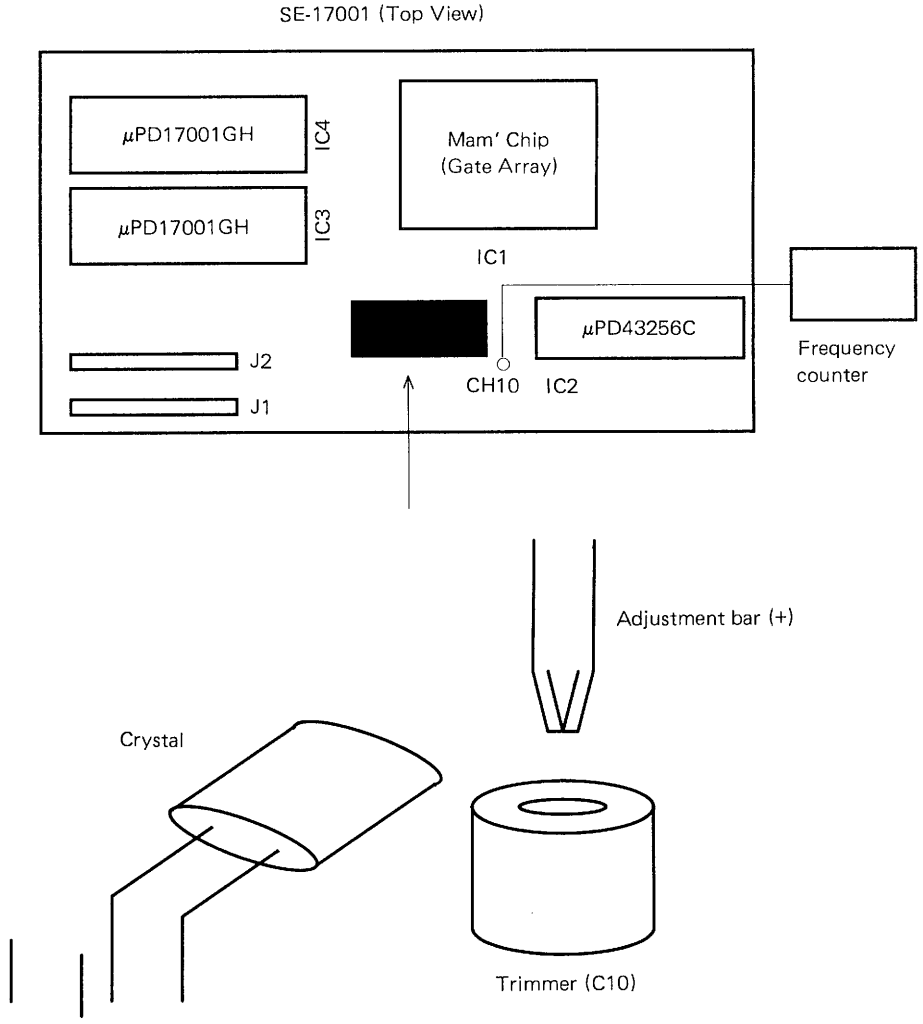


Phase-out/Discontinued

4.3 ADJUSTING OF OSCILLATING FREQUENCY

The oscillating frequency is set to 4.5 MHz ± 20 ppm as shipped. When the adjusting of oscillating frequency would be performed, adjust it by using the trimmer capacitor (C10) on SE-17001. With regard to the measurement of oscillating frequency, use the CH11 pin on SE-17001.

Fig. 4-10 Adjusting of Oscillating Frequency



Phase-out/Discontinued

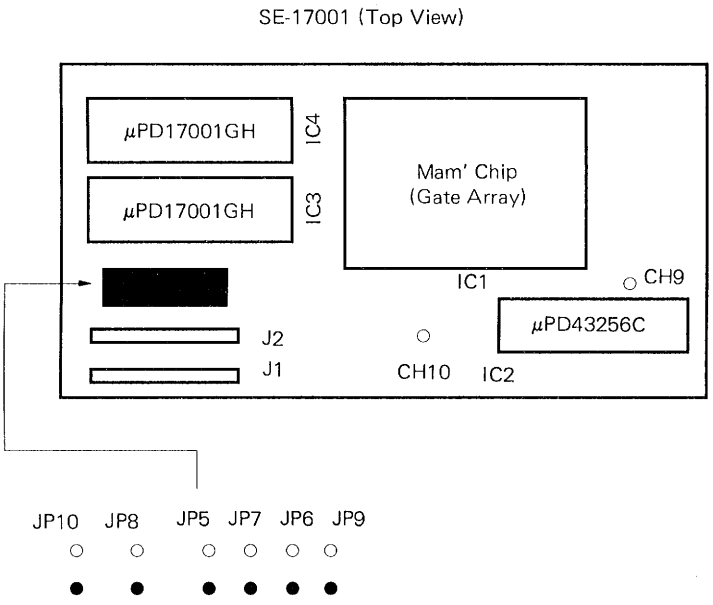
4.4 MONITOR PINS

On SE-17001 the monitor pins are provided in order to examine the status of the following pins of μPD17001GH. The monitor pin layout shows in Fig. 4-11.

Monitor Pin Name	Pin Name of IC (Pin No.)
JP5	VCOH (42)
JP6	VCOL (41)
JP7	$P1A_3$/FMIFC (39)
JP8	$P1A_2$/AMIFC (38)
CH9	CE (5)
CH10	CKOUT (μPD65200)

JP5, JP6, JP7 or JP8 and their GND pins are located in pairs.

Fig. 4-11 Monitor Pin Layout



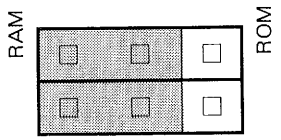
NOTE: ● is GND.

Phase-out/Discontinued

4.5 SETTINGS AS SHIPPED

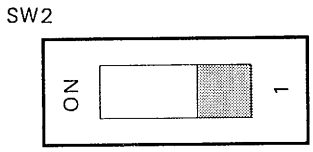
When SE-17001 is shipped, the settings of IC2 (the program memory), the ROM/RAM change jumper switches, SW2 and the crystal oscillator are as below.

- IC2 (Program memory)
  The RAM (μPD43256C-12) is mounted.
- ROM/RAM change jumper switches
  They are set so as to use the RAM as a program memory



NOTE: ▒▒ is the connecting position.

- SW2
  It is set so that the CE signal is not pulled up.



NOTE: ▒▒ is the setting side.

- Crystal oscillator
  It is adjusted to 4.5 MHz ± 20 ppm.

Phase-out/Discontinued

CHAPTER 5 CONNECTOR PIN TABLES

5.1 CONNECTOR (J1) FOR PROBE

J1 Pin No	Pin Name (Pin No of IC)	J1 Pin No	Pin Name (Pin No of IC)	J1 Pin No	Pin Name (Pin No of IC)
1	GND	21	GND	41	GND
2	NC	22	NC	42	$P0B_0/SI_1$ (23)
3	GND	23	GND	43	GND
4	NC	24	NC	44	$P0B_1$ (24)
5	GND	25	GND	45	GND
6	NC	26	$P1D_0$ (15)	46	NC
7	GND	27	GND	47	GND
8	NC	28	$P1D_1$ (16)	48	NC
9	GND	29	GND	49	GND
10	$P1B_2$ (9)	30	$P1D_2$ (17)	50	$P0B_2$ (25)
11	GND	31	GND	51	GND
12	$P1B_3$ (10)	32	$P1D_3$ (18)	52	$P0B_3$ (26)
13	GND	33	GND	53	GND
14	$P1C_0/CGP$ (11)	34	$P0A_0/SDA$ (19)	54	$P0C_0$ (27)
15	GND	35	GND	55	GND
16	$P1C_1/PWM_0$ (12)	36	$P0A_1/SCL$ (20)	56	$P0C_1$ (28)
17	GND	37	GND	57	GND
18	$P1C_2/PWM_1$ (13)	38	$P0A_2/\overline{SCK_1}$ (21)	58	$P0C_2$ (29)
19	GND	39	GND	59	GND
20	$P1C_3/PWM_2$ (14)	40	$P0A_3/SO_1$ (22)	60	$P0C_3$ (30)

Phase-out/Discontinued

5.2 CONNECTOR (J2) FOR PROBE

J2 Pin No	Pin Name (Pin No of IC)	J2 Pin No	Pin Name (Pin No of IC)	J2 Pin No	Pin Name (Pin No of IC)
1	GND	21	GND	41	GND
2	$P1B_0$/FCG (7)	22	EO_1 (48)	42	$P1A_2$/AMIFC (38)
3	GND	23	GND	43	GND
4	$P1B_1$ (8)	24	EO_0 (47)	44	GND
5	GND	25	GND	45	GND
6	CE (5)	26	X_{IN} (46)	46	$P1A_1/ADC_5$ (36)
7	GND	27	GND	47	GND
8	INT (6)	28	X_{OUT} (45)	48	$P1A_0/ADC_4$ (35)
9	GND	29	GND	49	GND
10	LPF_{OUT} (3)	30	CLKOUT (44)	50	NC
11	GND	31	GND	51	GND
12	GND_{LPF} (4)	32	GND	52	NC
13	GND	33	GND	53	GND
14	LPF_{IN} (1)	34	VCOH (42)	54	$P0D_3/ADC_3$ (34)
15	GND	35	GND	55	GND
16	V_{LPF} (2)	36	VCOL (41)	56	$P0D_2/ADC_2$ (33)
17	GND	37	GND	57	GND
18	NC	38	V_{DD} (40)	58	$P0D_1/ADC_1$ (32)
19	GND	39	GND	59	GND
20	NC	40	$P1A_3$/FMIFC (39)	60	$P0D_0/ADC_0$ (31)

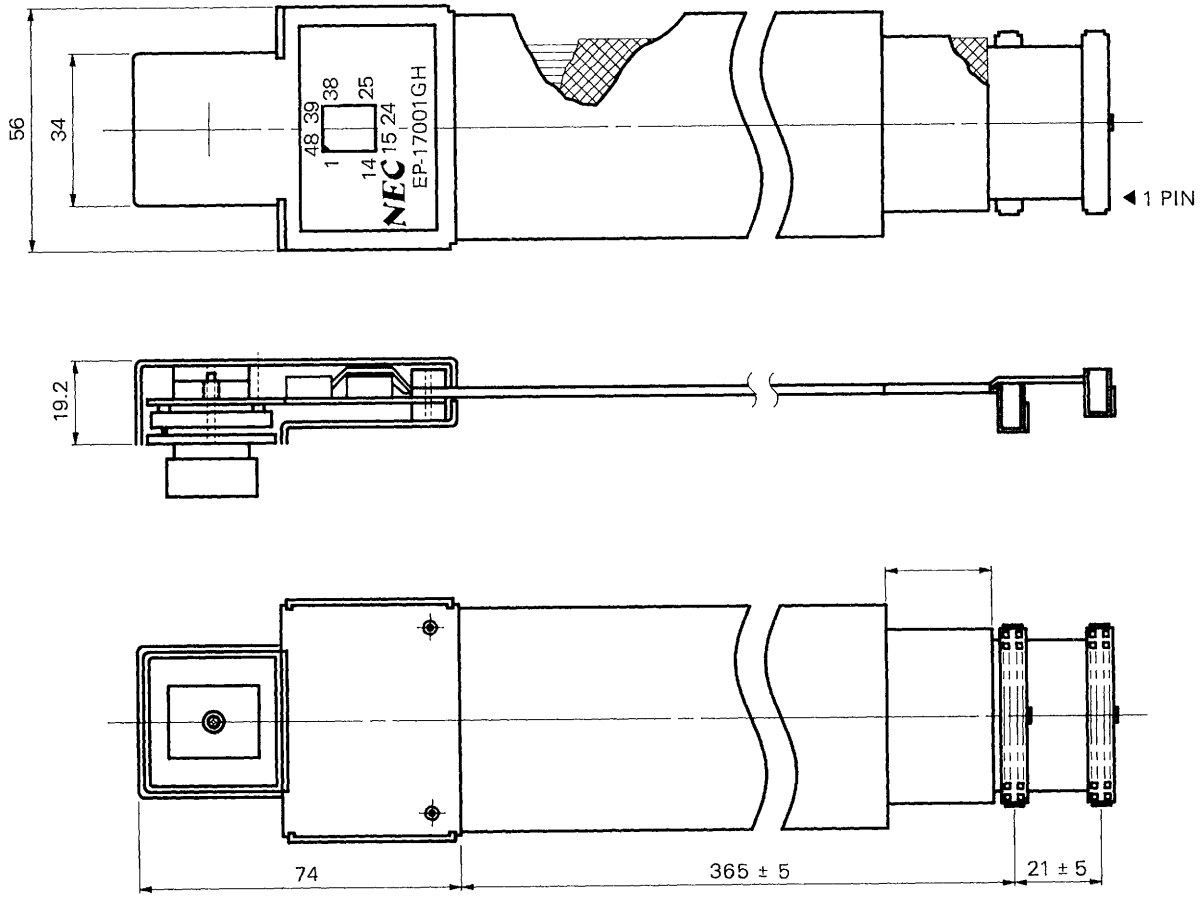
Phase-out/Discontinued

CHAPTER 6 EXTERNAL FORM OF PROBE AND RECEPTACLE

6.1 EXTERNAL FORM OF PROBE

Model name EP-17001GH

Fig. 6-1 External form of Probe

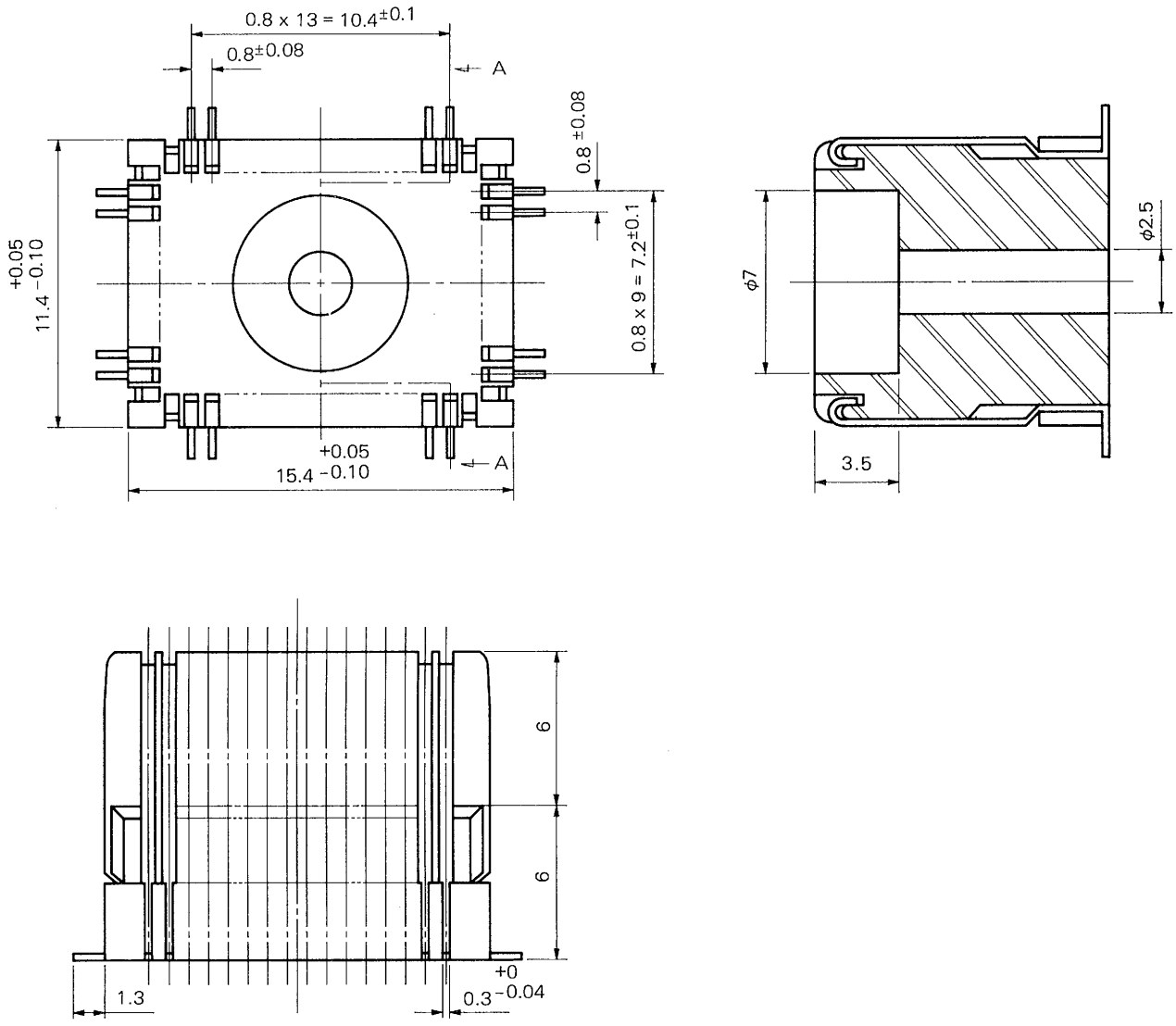


Phase-out/Discontinued

6.2 EXTERNAL FORM OF RECEPTACLE

Model name EV-9200G-48

Fig. 6-2 External form of Receptacle



Phase-out/Discontinued

Phase-out/Discontinued

NEC