User's Manual

RZ/N2L Industrial Network SOM Kit YCONNECT-IT-RZN2L

User's Manual

RENESAS MPU
RZ/N2L

Rev .1.0
March 30, 2023

Renesas Electronics
www.renesas.com

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarter

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

List of Abbreviations and Acronyms

Abbreviation	Full Form
CPU	Central Processing Unit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
EtherCAT	Ethernet for Control Automation Technology
Hi-Z	High Impedance
I/O	Input / Output
I2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
IRQ	Interrupt Request
J-Link®	SEGGER debug probe (Emulator)
MCU	Micro controller Unit
MPU	Micro Processor Unit
OTG	On The Go
PCB	Printed Circuit Board
PMIC	Power Management Integrated Circuit
PMOD	Peripheral module interface
QSPI	Quad Serial Peripheral Interface
SPI	Serial Peripheral Interface
NVM	Non Volatile Memory

Table of Contents

Table of Figures

Index of Tables

1. Introduction

1.1 Scope of this document

RZ/N2L Industrial Network SOM Kit (YCONNECT-IT-RZN2L) is described in this manual, including an overview of the functional principle, components, and connections in system.

1.2 Overview

The purpose of RZ/N2L Industrial Network SOM Kit is a reference design for SoM (system-on-module) and carrier board for industrial Ethernet solution. This reference design targets industrial application with network card having industrial Ethernet function.

This SOM Kit consist of two boards as follows. SoM module is soldered on Carrier Board as if it's 'stamp'. SoM module is called 'stamp module' in this document. Components for fundamental functions like memory and Ethernet PHY are implemented on stamp module, and components for additional functions depending on use case are on carrier board.

The reference design can reduce time-to-market, development, and their risk. The following listed industrial protocols are (or are to be) supported.

- PROFINET
- EtherNet/IP
- EtherCAT
- Modbus TCP
- OPC UA

1.3 Features

Features for stamp module and carrier board are shown as follows.

1. **Stamp Module (EU140SOMSTAMPPOC1Z):**
    - 128Mbit QSPI flash, 256Mbit SDRAM and 16kbit EEPROM
    - Power Management IC (PMIC)
    - 2x Ethernet Gbit PHY
    - 120 castellated pads for connecting Carrier Board
    - Small footprint

2. **Carrier Board (EU140CARRIERPOC1Z):**
    - Power Supply from either 24V_{DC} connector, USB, or Arduino Host Board
    - RJ45 connector for dual port
    - 2x PMOD female connectors assuming to use Quick Connect IoT Sensors
    - Arduino dual use:
        - Host to carry Arduino Shield via female pins
        - Shield via male connectors
    - USB 2.0 host/function with micro type-AB connector
    - Debug interface: USB micro type-B connector for Segger J-Link OB, or 10-pin half pitch connector for connecting external emulator
    - Serial Host Interface (HSPI) pins, and option pins for standard Industrial Ethernet synchronous use
    - 15 LEDs and 16 dip switches controlled by I2C

1.4 Appearance

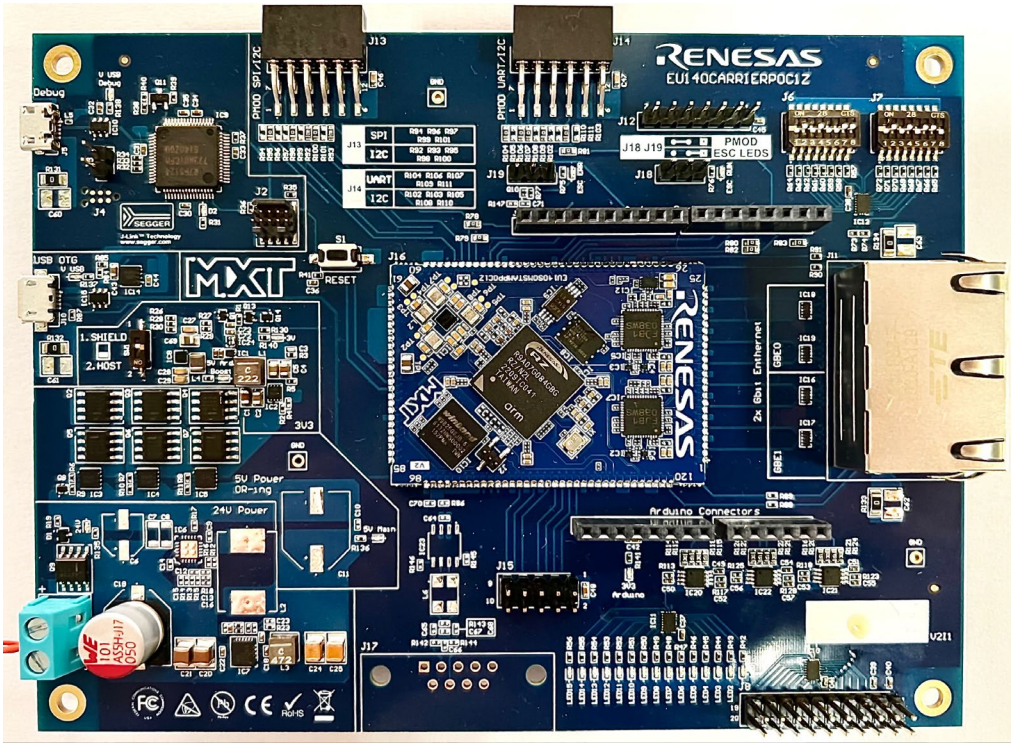


Figure 1-1 Appearance of RZ/N2L Industrial Network SOM Kit (Carrier Board + Stamp Module)

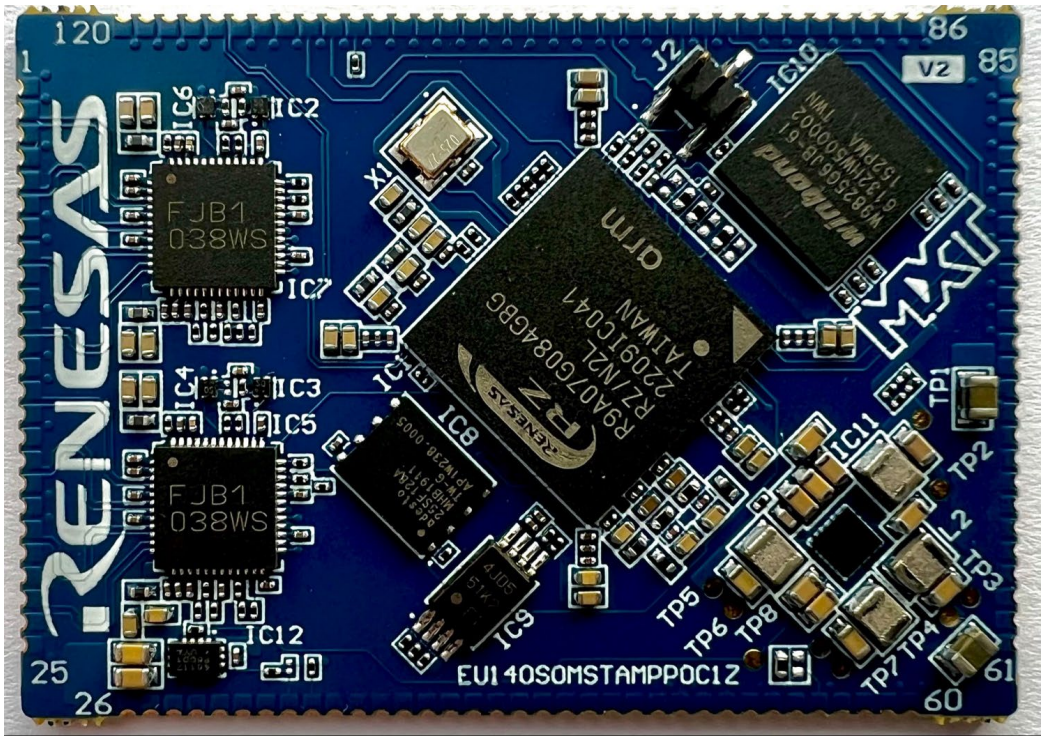


Figure 1-2 Appearance of Stamp Module

1.5 Components Arrangement

1.5.1 Carrier Board

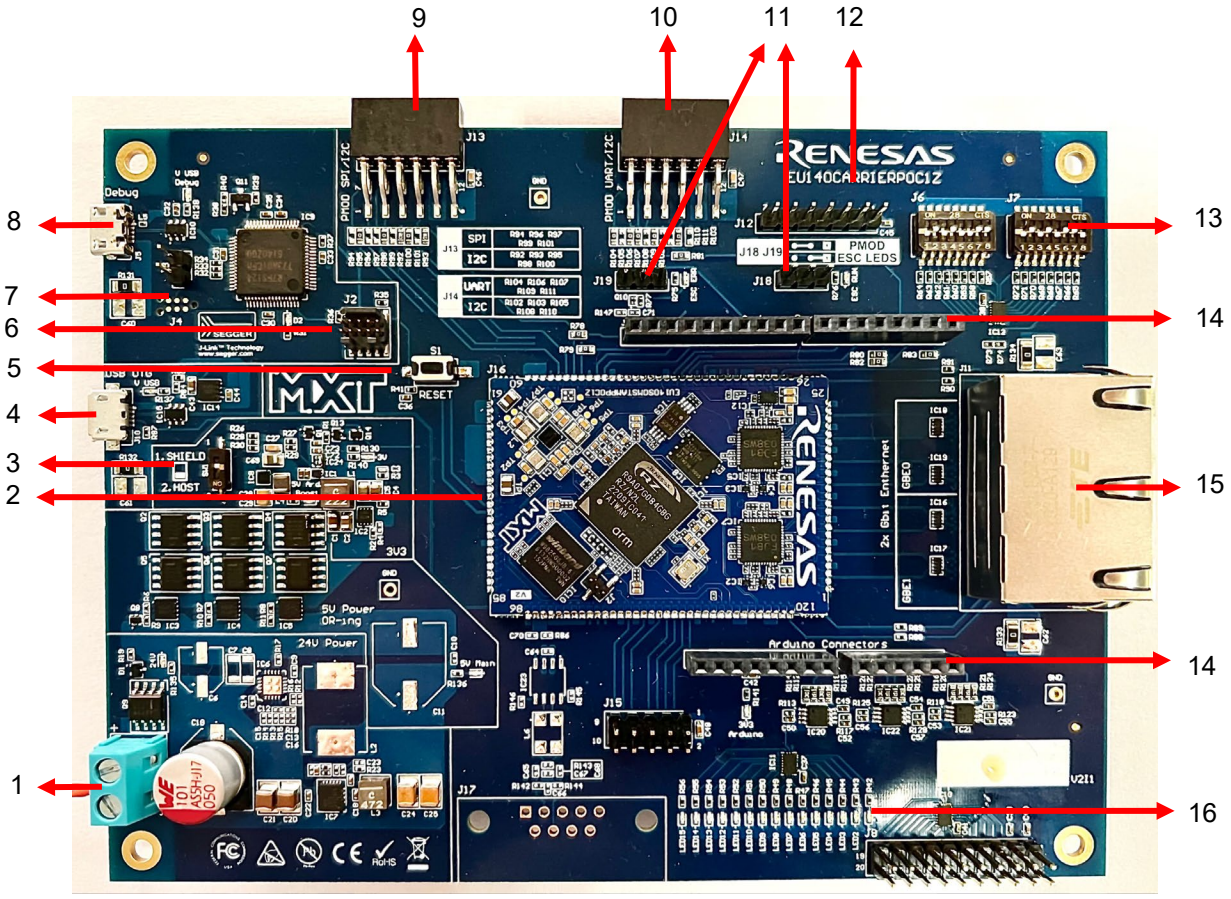


Figure 1-3 Carrier Board component placement

1) 24V Terminal Connector (J1)
2) Stamp Module
3) Host/Shield Arduino power switch slider (SW1)
4) USB micro type-AB Connector (J10)
5) Reset Button
6) JTAG Debug Connector (J2)
7) Integrated Segger J-Link Needle Adapter
8) Debug USB micro type-B Connector (J5)
9) PMOD SPI/I2C Renesas Connector (J13)
10) PMOD UART/I2C Renesas Connector (J14)
11) 2 x ESC LEDs or PMOD Pins Selector (J18, J19)
12) 7-Pin ESC Interface Connector (J12)
13) 2 x 8 - User Switch Slider (J6, J7)
14) Arduino Connector with both options:
    - Female on top side (used as host)
    - Male on bottom side (used as shield)
15) 2 x Gigabit Ethernet Connectors (J11)
16) 15 x User LEDs
17) 20-pins User Connector (J8)
18) 10-pins HSPI Interface Connector (J15)

1.5.2 Stamp Module

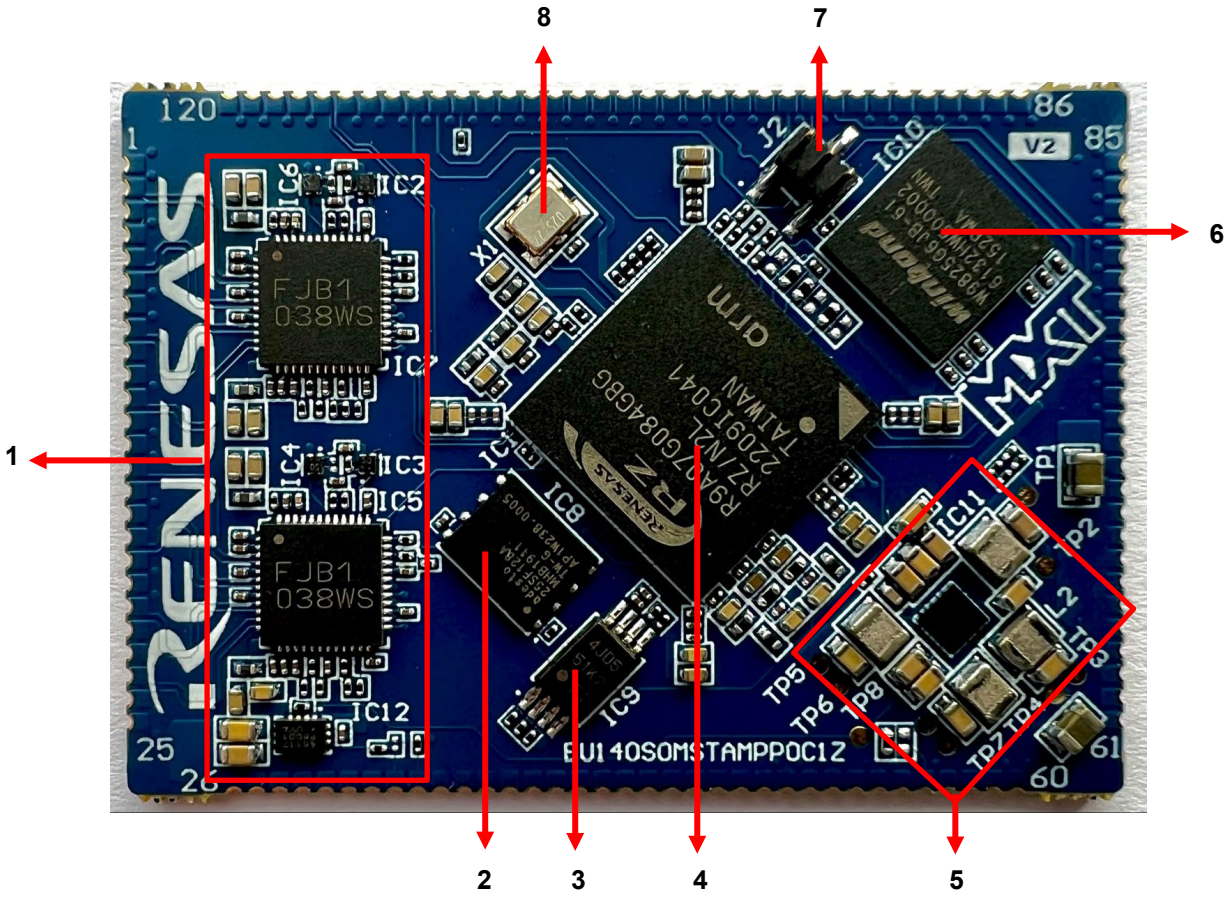


Figure 1-4 Stamp Module Key Components

1) 2x Gigabit Ethernet PHYs (VSC8531XMW-01)
2) 128Mbit NOR Flash (AT25SF128A-MHB-T)
3) 16Kbit Serial EEPROM (R1EX24016ATAS0I#S0)
4) RZ/N2L (R9A07G084M04GBG) - 1 Core 32-Bit 400MHz ARM® Cortex®-R52 Ethernet communication MPU
5) High Current, Highly Configurable System PMIC (DA9083)
6) 256Mbit SDRAM (W9825G6JB)
7) Selection header for pin P14_5 between HSPI and SDRAM (J2)
8) 25MHz HCMOS Oscillator (XLH336025.000000I)

2. Power Supply

- **Three Power Source for RZ/N2L Industrial Network SOM Kit:**
  - Operation from 24V via screw terminal (J1)
  - Operation from 5V USB connectors (J5)
  - Operation from 5V USB connectors (J10)
  - Operation from 3.3V Arduino pins *1 (see Table 3-9 Arduino Interface Pin Assignment (Connector: J9))

*1 SW1 OFF setting is required when power is supplied from Arduino Host.

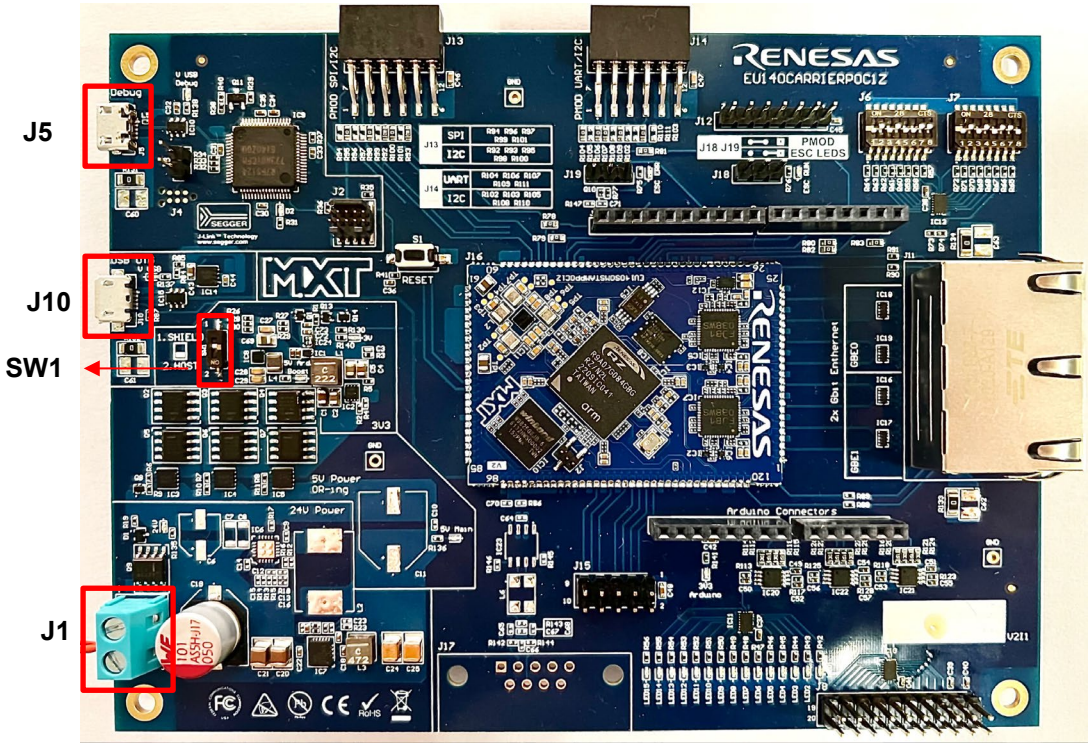


Figure 2-1 Power supply connector

The following figure shows how power supply to Stamp Module from Carrier board.

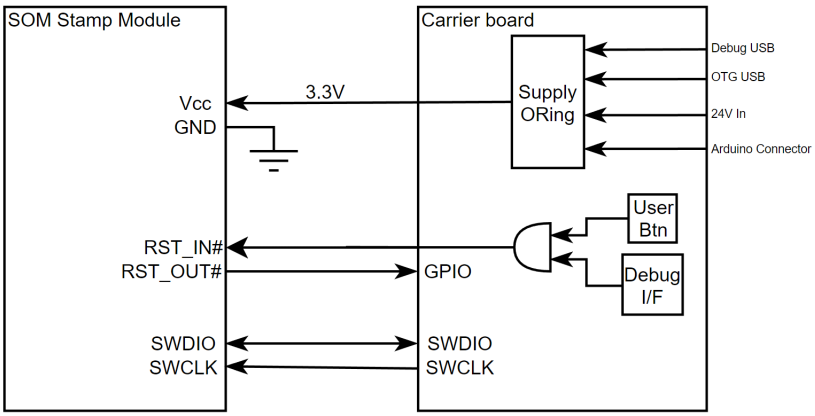


Figure 2-2 Connection to Carrier board

3. Interface

3.1 Jumper Settings

3.1.1 SDRAM Setting

The following jumper settings are required to use SDRAM.

Table 3-1 SDRAM Jumper Setting

Jumper	Pin number	Configuration	Description
J2	1-2	OPEN	Enable BSC_CS3# signal
	2-3	SHORT	

3.1.2 EtherCAT Setting

The following jumper settings are required to use EtherCAT.

Table 3-2 EtherCAT Jumper Settings

Jumper	Pin number	Configuration	Description
J18	1-2	SHORT	Enable EtherCAT Run LED
	2-3	OPEN	
J19	1-2	SHORT	Enable EtherCAT Error LED
	2-3	OPEN	

3.1.3 HSPI Setting

The following jumper settings are required to use HSPI interfaces.

Table 3-3 HSPI Jumper Setting

Jumper	Pin number	Configuration	Description
J2	1-2	SHORT	Enable HSPI_INT# signal
	2-3	OPEN	

3.1.4 Pmod Settings

The following jumper settings are required to use Pmod (J14) interfaces.

Table 3-4 Pmod Jumper Settings

Jumper	Pin number	Configuration	Description
J18	1-2	OPEN	Enable Pmod (J14) Pin 9 connection
	2-3	SHORT	
J19	1-2	OPEN	Enable Pmod (J14) Pin 10 connection
	2-3	SHORT	

3.2 Gigabit Ethernet Interfaces

3.2.1 Overview

With two RJ45 network connectors, the Carrier Board is ready for external connection in several network topologies. The internal PHY layers in the Stamp Module can handle different industrial communication protocols and support 10/100/1000BASE-T.

3.2.2 Hardware Specification

The Ethernet ports have the following pin assignment:

Table 3-5 Ethernet Port Pin Assignment

Pin	Signal	I/O	Description
1	MDI0-	I/O	Tx/Rx channel A negative signal
2	MDI0+	I/O	Tx/Rx channel A negative signal
3	MDI1-	I/O	Tx/Rx channel B negative signal
4	MDI1+	I/O	Tx/Rx channel B negative signal
5	MDI2-	I/O	Tx/Rx channel C negative signal
6	MDI2+	I/O	Tx/Rx channel C negative signal
7	MDI3-	I/O	Tx/Rx channel D negative signal
8	MDI3+	I/O	Tx/Rx channel D negative signal

The Ethernet ports support 1000 Mbits/s with auto negotiation.

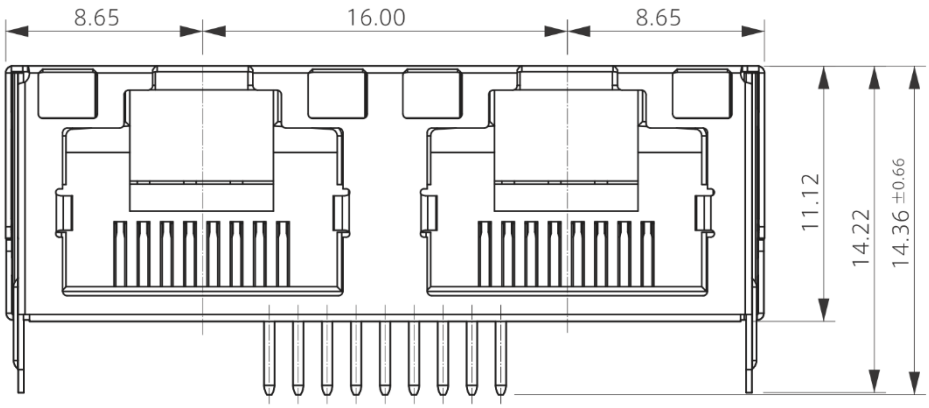


Figure 3-1 Ethernet Port Drawings (2 Ports)

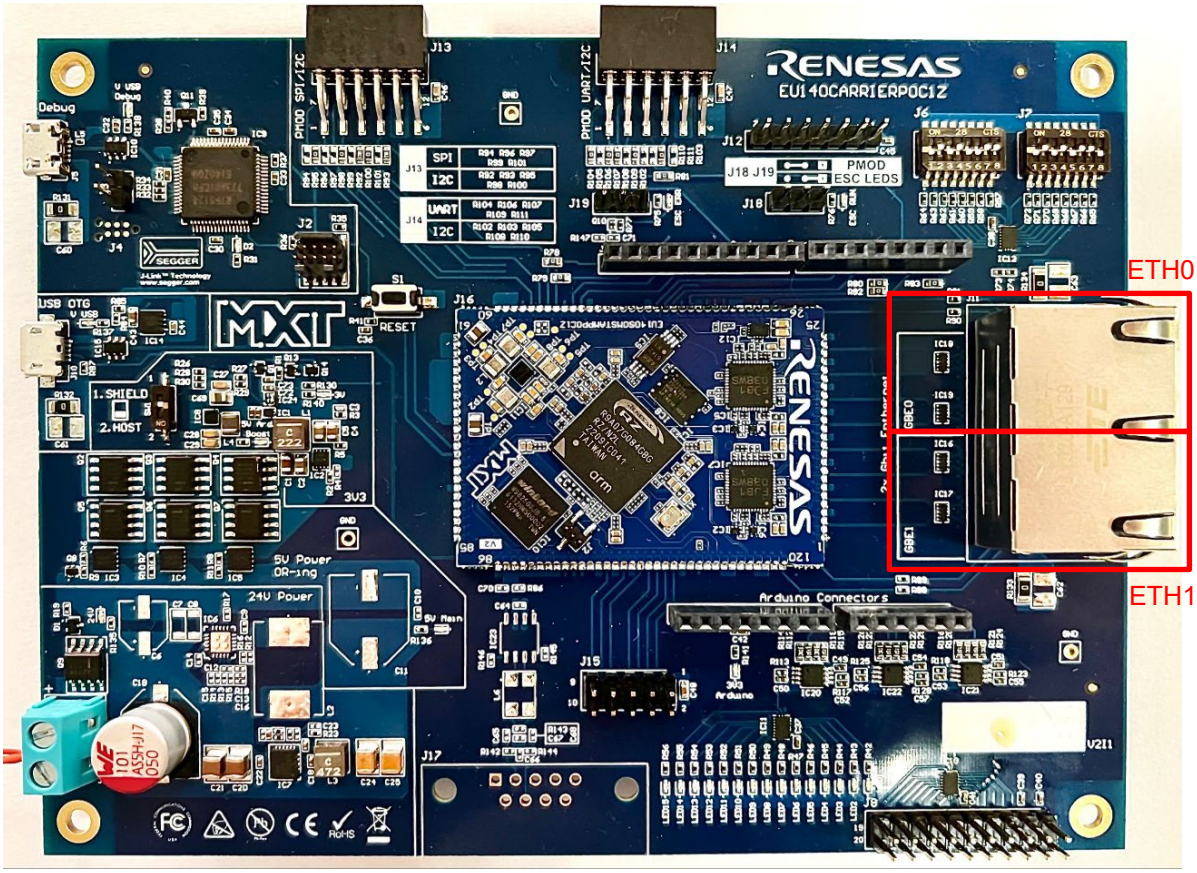


Figure 3-2 Ethernet Port (2 Ports)

3.2.3 LED Status Specification

The Carrier Board has two RJ45 Ethernet ports and requires two LEDs per RJ45 jack, as follows:

- Module Status Indicator
- Network Status Indicator

Both indicators must be implemented separately from the RZ/N2L MPU and controlled by the application.

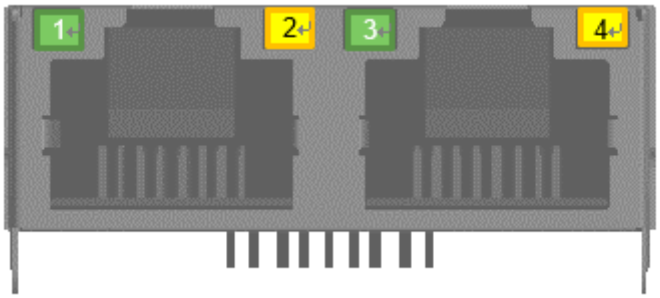


Figure 3-3 Link and Activity LEDs

3.2.4 Ethernet PHY

Two Ethernet controller ICs (Ethernet PHYs: VSC8531XMW-01) are fitted to the Stamp Module and are connected to the MPU Ethernet peripherals.

Table 3-6 Ethernet PHY Address Settings

Port	Part	PHY address setting
ETH0	IC5	0
ETH1	IC7	1

Table 3-7 Ethernet Connections (Port 0)

MPU on Stamp Module			**IC5**
Pin	Port	Ethernet signal	Pin
M7	P09_6	ETH0_TXD0	TXD0
N7	P09_5	ETH0_TXD1	TXD1
M6	P09_4	ETH0_TXD2	TXD2
R4	P09_3	ETH0_TXD3	TXD3
L7	P09_7	ETH0_TXCLK	TX_CLK
N8	P10_0	ETH0_TXEN	TX_CTL
M8	P10_1	ETH0_RXD0	RXD0
L8	P10_2	ETH0_RXD1	RXD1
L9	P10_3	ETH0_RXD2	RXD2
N4	P08_4	ETH0_RXD3	RXD3
M5	P08_6	ETH0_RXCLK	RX_CLK
P3	P08_5	ETH0_RXDV	RX_CTL
R3	P09_1	ETH0_REFCLK	XTAL1
N5	P08_7	GMAC_MDC	GMAC_MDC
P4	P09_0	GMAC_MDIO	GMAC_MDIO
B2	P01_2	ETH0_MDINT	MDINT
L12	P13_4	ETH_RESET#	NRESET

Table 3-8 Ethernet Connections (Port 1)

MPU on Stamp Module			**IC7**
Pin	Port	Ethernet signal	Pin
K4	P06_3	ETH1_TXD0	TXD0
M2	P06_2	ETH1_TXD1	TXD1
M1	P05_7	ETH1_TXD2	TXD2
L2	P06_0	ETH1_TXD3	TXD3
N1	P06_4	ETH1_TXCLK	TX_CLK
N2	P06_5	ETH1_TXEN	TX_CTL
L4	P06_6	ETH1_RXD0	RXD0
M3	P06_7	ETH1_RXD1	RXD1
P1	P07_0	ETH1_RXD2	RXD2
N3	P07_1	ETH1_RXD3	RXD3
M4	P07_3	ETH1_RXCLK	RX_CLK

P2	P07_2	ETH1_RXDV	RX_CTL
L3	P06_1	ETH1_REFCLK	XTAL1
N5	P08_7	GMAC_MDC	GMAC_MDC
P4	P09_0	GMAC_MDIO	GMAC_MDIO
C15	P18_6	ETH1_MDINT	MDINT
L12	P13_4	ETH_RESET#	NRESET

3.2.5 EtherCAT

RZ/N2L has EtherCAT Slave Controller (ESC) and EtherCAT communication can be used on this SOM Kit. Some EtherCAT signals are available on the connector J12.

Table 3-9 EtherCAT Connections

MPU on Stamp Module			**Connect to**
Pin	Port	Ethernet signal	
P4	P09_0	ESC_MDIO	Ethernet PHY
N5	P08_7	ESC_MDC	Ethernet PHY
D8	P20_2	ESC_LEDRUN	Run LED
D9	P20_4	ESC_LEDERR	Error LED
J13	P14_4	ESC_IRQ	Connector J12-4
D1	P02_1	ESC_SYNC0	Connector J12-1
M13	P13_6	ESC_SYNC1	Connector J12-2
D2	P01_6	ESC_LATCH0	Connector J12-6
M11	P13_7	ESC_LATCH1	Connector J12-5
L12	P13_4	ESC_RESETOUT#	Ethernet PHY
L10	P13_2	ESC_I2CCLK	EEPROM
N12	P13_3	ESC_I2CDATA	EEPROM
M9	P10_4	ESC_PHYLINK0	Ethernet PHY
K2	P05_5	ESC_PHYLINK1	Ethernet PHY

3.3 USB Interface

The Carrier Board features a USB2.0 interface, available on the microUSB connector J10.

Table 3-10 USB Interface Pin Assignment (microUSB connector: J10)

MPU on Stamp Module			**J10**	
Pin	Port	Signal	Pin	Signal

-	-	-	1	VCC
P13	-	USB DM	2	D-
R13	-	USB DP	3	D+
E3	P02_0	USB_OTGID	4	ID
-	-	-	5	GND

IMPORTANT:

In default, this board assume to connect non-standard USB cable which ID pin has not GND for OTG use. To allow RZ/N2L to be OTG Host in that condition, USB_OTGID signal has pull-down resistor R87.

If use standard OTG cable and OTG Device, remove resistor R87 and configure port P02_0 with internal pull-up. If don't use OTG, nothing to do because ID pin can be ignored.

3.4 Debug Interface

There are two options for debug interface, J-Link OB via USB or external emulator via 10-pin connector.

3.4.1 USB Debug Interface

The Carrier Board features an on-board Segger JLink debugger circuit, implemented on a S124 Synergy MCU, used for debugging of the main RZ/N2L MPU on the Stamp Module.

Access to the debug interface is done through the microUSB connector J5.

3.4.2 External Debugger Interface

The Carrier Board also features a standard 10-pin SWD connector (J2), which enables the user to use an external debug tool. The two debug interfaces cannot be used at the same time.

Table 3-11 Debug Interface Pin Assignment (10-pin SWD connector: J2)

MPU			**J2**	
Pin	Port	Signal	Pin	Signal
-		-	1	VTref
F5	P02_6	TMS	2	SWDIO/TMS
-		-	3	GND
F1	P02_7	TCK	4	SWCLK/TDO
-		-	5	GND
-		-	6	SWO/TDO
-		-	7	-
-		-	8	TDI
-		-	9	NC
P6	-	RES#	10	nRESET

3.5 High Speed CAN Interface

The Carrier Board features a CAN-FD interface that complies with ISO 11898-1 (2015) Standards. CANFD transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier is hereafter referred to as ID) and extended ID (29 bits).

The CAN-FD pins are shared with Arduino connector (J9), pins 26 and 28.

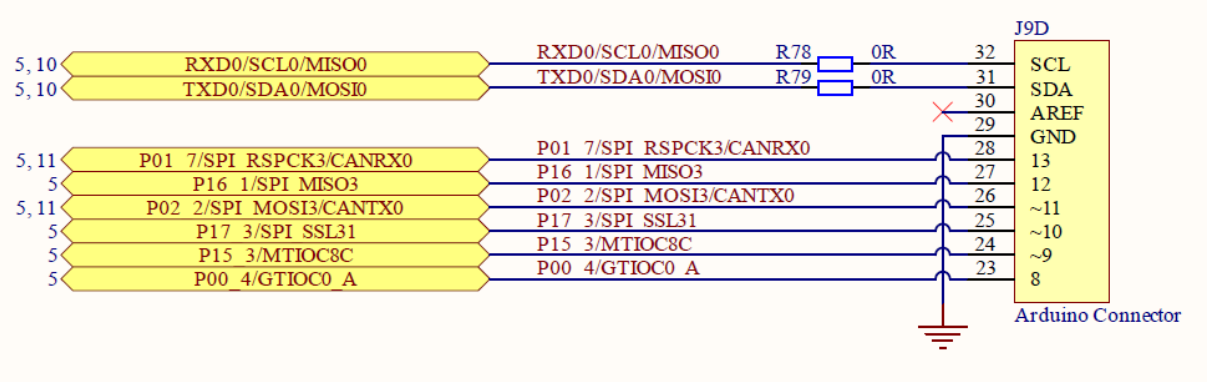


Figure 3-4 Implementation of CAN Interface

Table 3-12 CAN Interface Pin Assignment (Connector: J9)

MPU on Stamp Module			**J9**	
Pin	Port	Signal	Pin	Signal
C1	P02_2	P02_2/SPI_MOSI3/CAN TX0	26	CAN TX0
F3	P01_7	P01_7/SPI_RSPCK3/CAN RX0	28	CAN RX0

3.6 Arduino Interface

Another interface with the external boards is the Arduino UNO hardware compatibility pins, with dual functionality:

- Host mode via female connectors on the top side for carrying standard Arduino shields.
  - Analog, I2C, SPI master, UART, PWM, GPIO, Power (3.3V output)
  - Configure SW1 = ON
- Shield mode via male connectors on the bottom side where the stamp and baseboard can behave like a shield.
  - I2C, GPIO. Power (3.3V input)
  - Configure SW1 = OFF

IMPORTANT:

For this connection the user should select the power source using switch slider (SW1) in correlation with the used mode. If no Arduino compatible board is connected, the SW1 must be in HOST mode.

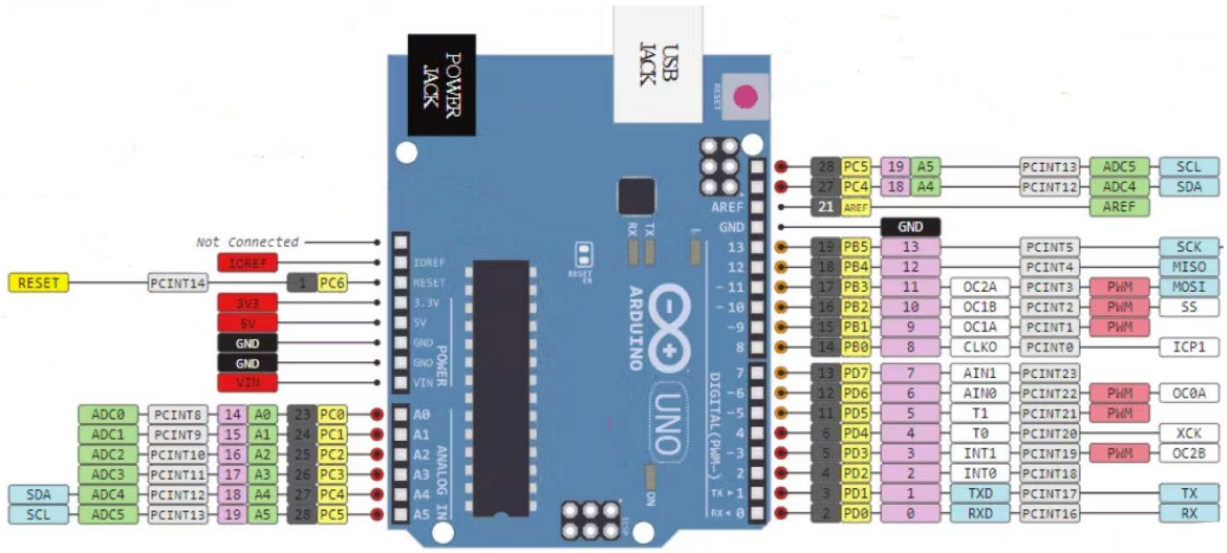


Figure 3-5 General Arduino UNO Interface

Table 3-13 Arduino Interface Pin Assignment (Connector: J9)

MPU			J9	
Pin	Port	Signal	Pin	Signal
-	-	-	NC	NC
-	-	-	IOREF	NC
P6	-	RESET#	RESET	RST_IN#
-	-	-	3V3	-
-	-	-	5V	NC
-	-	-	GND	-
-	-	-	GND	-
-	-	-	VIN	NC
B13	-	AN000	A0	ARD_AN000
C12	-	AN001	A1	ARD_AN001
B14	-	AN002	A2	ARD_AN002
C13	-	AN003-	A3	ARD_AN003
B12	-	AN100	A4	ARD_AN100
A14	-	AN101	A5	ARD_AN101
G11	P16_6	RXD0/SCL0/MISO0	SCL	RXD0/SCL0/MISO0
H15	P16_5	TXD0/SDA0/MOSI0	SDA	TXD0/SDA0/MOSI0
-	-	-	AREF	NC
-	-	-	GND	-
C1	P01_7	P01_7/SPI_RSPCK3/CANRX0	13	P01_7/SPI_RSPCK3/CANRX0
H11	P16_1	P16_1/SPI_MISO3	12	P16_1/SPI_MISO3
F3	P02_2	P02_2/SPI_MOSI3/CANTX0	~11	P02_2/SPI_MOSI3/CANTX0
F14	P17_3	P17_3/SPI_SSL31	~10	P17_3/SPI_SSL31
K11	P15_3	P15_3/MTIOC8C	~9	P15_3/MTIOC8C
A4	P00_4	P00_4/GTIOC0_A	8	P00_4/GTIOC0_A
M13	P13_6	P13_6/ESC_SYNC1/ETHSW_PTPOUT0	7	P13_6/ESC_SYNC1/ETHSW_PTPOUT0

D1	P02_1	P02_1/ESC_SYNC0/ETHSW_PTPOUT1	~6	P02_1/ESC_SYNC0/ETHSW_PTPOUT1
G15	P17_6	P17_6/GTIOC1A/MTIOC3B	~5	P17_6/GTIOC1A/MTIOC3B
D14	P18_2	P18_2/GTIOC2B	4	P18_2/GTIOC2B
A3	P00_2	P00_2	~3	P00_2
E13	P18_3	P18_3/IRQ0	2	P18_3/IRQ0
E14	P18_0	TXD3/SDA3/MOSI3	TX	TXD3/SDA3/MOSI3
E15	P17_7	RXD3/SCL3/MISO3	RX	RXD3/SCL3/MISO3

3.7 PMOD Interfaces

The 2 x PMOD connectors provide enable interfacing with various PMOD Expansion Board, with the possibility of configuring PMOD Type by soldering/desoldering resistors. It is important to only fit a single channel set.

3.7.1 SPI/I2C Interfaces

The J13 connector provides Type 2A (Extended SPI) and Type 6A (Extended I2C) Pmod interface.

Default register soldering can be used for Type 2A (Extended SPI) interface.

It is possible to change the PMOD interface type from 2A to 6A by removing and soldering the resistors.

Table 3-14 Pmod SPI/I2C Interface register soldering for Connector J13

Register	SPI Configuration	I2C Configuration
R92	OPEN	SHORT
R93	OPEN	SHORT
R94	SHORT	OPEN
R95	OPEN	SHORT
R96	SHORT	OPEN
R97	SHORT	OPEN
R98	OPEN	SHORT
R99	SHORT	OPEN
R100	OPEN	SHORT
R101	SHORT	OPEN

Table 3-15 Pmod SPI/I2C Interface Pin Assignment (Connector: J13 – Type 2A (Extended SPI))

MPU			J13 - Type 2A (Extended SPI)	
Pin	Port	Signal (SCI0)	Pin	Default Signal (SPI)
F12	P17_0	SS0#/CTS0#/RTS0#	1	CS
H15	P16_5	TXD0/SDA0/MOSI0	2	MOSI
G11	P16_6	RXD0/SCL0/MISO0	3	MISO
G14	P16_7	SCK0	4	SCLK
-	-	-	5	GND
-	-	-	6	VCC
A3	P00_2	P00_2	7	INT
H13	P15_4	P15_4	8	RESET
M12	P13_5	P13_5	9	GPIO
L13	P14_0	P14_0	10	GPIO
-	-	-	11	GND
-	-	-	12	VCC

Table 3-16 Pmod SPI/I2C Interface Pin Assignment (Connector: J13 – Type 6A (Extended I2C))

MPU			J13 - Type 6 (Extended I2C)	
Pin	Port	Signal (SCI0)	Pin	Alternative signal(I2C)

A3	P00_2	P00_2	1	INT
H13	P15_4	P15_4	2	RESET
G11	P16_6	RXD0/SCL0/MISO0	3	SCL
H15	P16_5	TXD0/SDA0/MOSI0	4	SDA
-	-	-	5	GND
-	-	-	6	VCC
	-	-	7	NC
	-	-	8	NC
M12	P13_5	P13_5	9	GPIO
L13	P14_0	P14_0	10	GPIO
-	-	-	11	GND
-	-	-	12	VCC

3.7.2 UART/I2C Interfaces

The J14 connector provides Type 3A (Extended UART) and Type 6A (Extended I2C) Pmod interface.

Default register soldering can be used for Type 3A (Extended UART) interface.

It is possible to change the PMOD interface type from 3A to 6A by removing and soldering the resistors.

Table 3-17 Pmod UART/I2C Interface register soldering for Connector J14

Register	SPI Configuration	I2C Configuration
R102	OPEN	SHORT
R103	OPEN	SHORT
R104	SHORT	OPEN
R105	OPEN	SHORT
R106	SHORT	OPEN
R107	SHORT	OPEN
R108	OPEN	SHORT
R109	SHORT	OPEN
R110	OPEN	SHORT
R111	SHORT	OPEN

Table 3-18 Pmod UART/I2C Interface Pin Assignment (Connector: J14 – Type 3A (Extended UART))

MPU			J14 - Type 3A (Extended UART)	
Pin	Port	Signal (SCI3)	Pin	Default Signal (UART)
F13	P17_4	CTS3#	1	CTS
E14	P18_0	TXD3/SDA3/MOSI3	2	TXD
E15	P17_7	RXD3/SCL3/MISO3	3	RXD
D15	P18_1	SS3#/CTS3#/RTS3#	4	RTS
-	-	--	5	GND
-	-	--	6	VCC

E13	P18_3	P18_3/IRQ0	7	INT
J14	P15_5	P15_5	8	RESET
D8	P20_2	P20_2/ESC_LEDRUN/ETHSW_TDMAOUT1	9	GPIO
D9	P20_3	P20_3/ESC_LEDERR/ETHSW_TDMAOUT2	10	GPIO
-	-	-	11	GND
-	-	-	12	VCC

Table 3-19 Pmod UART/I2C Interface Pin Assignment (Connector: J14 – Type 6A (Extended I2C))

MPU			**J14 - Type 6A (Extended I2C)**	
Pin	Port	Signal (SCI3)	Pin	Alternative Signal (I2C)
E13	P18_3	P18_3/IRQ0	1	INT
J14	P15_5	P15_5	2	RESET
E15	P17_7	RXD3/SCL3/MISO3	3	SCL
E14	P18_0	TXD3/SDA3/MOSI3	4	SDA
-	-	--	5	GND
-	-	--	6	VCC
-	-	-	7	NC
-	-	-	8	NC
D8	P20_2	P20_2/ESC_LEDRUN/ETHSW_TDMAOUT1	9	GPIO
D9	P20_3	P20_3/ESC_LEDERR/ETHSW_TDMAOUT2	10	GPIO
-	-	-	11	GND
-	-	-	12	VCC

3.8 General IO Interfaces

The Carrier Board features SLG46537V (GreenPAK) as general I/O interfaces.

Based on the internal NVM, the users can create their circuit design by configuring the interconnect logic, the micro cells, and the IO pins via I^2C commands. The carrier board features three SLG devices, each functionality being described in the following subchapters.

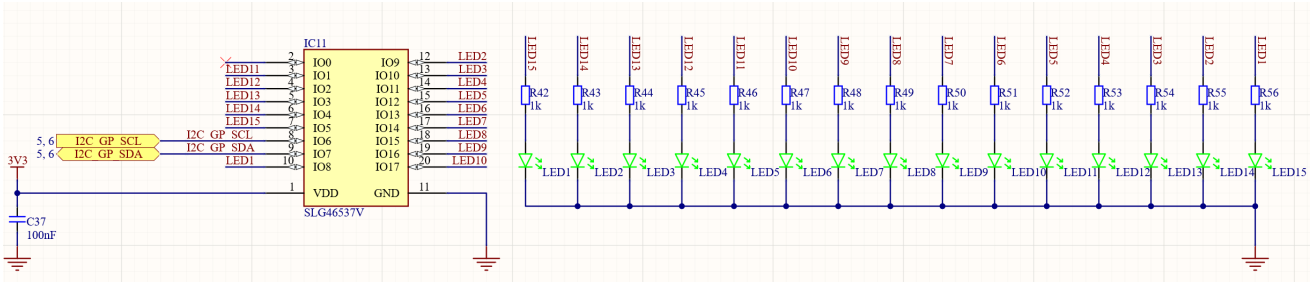
- Output Optical Configuration for User LEDs (LED1 ~ LED15)
- Input State Selector for User Switch Slider (J6, J7)
- General IO Connector for User Connector (J8)

All of SLG devices can be controlled by SCI-I2C channel 4.

3.8.1 Output Optical Configuration

- **Description:** IC11 acts as I/O expander. IC11 controls 15 small green LEDs.

Figure 3-6 SLG46537V (IC11) output schematic



- **Slave address:** 0010b
- **Internal configuration:**

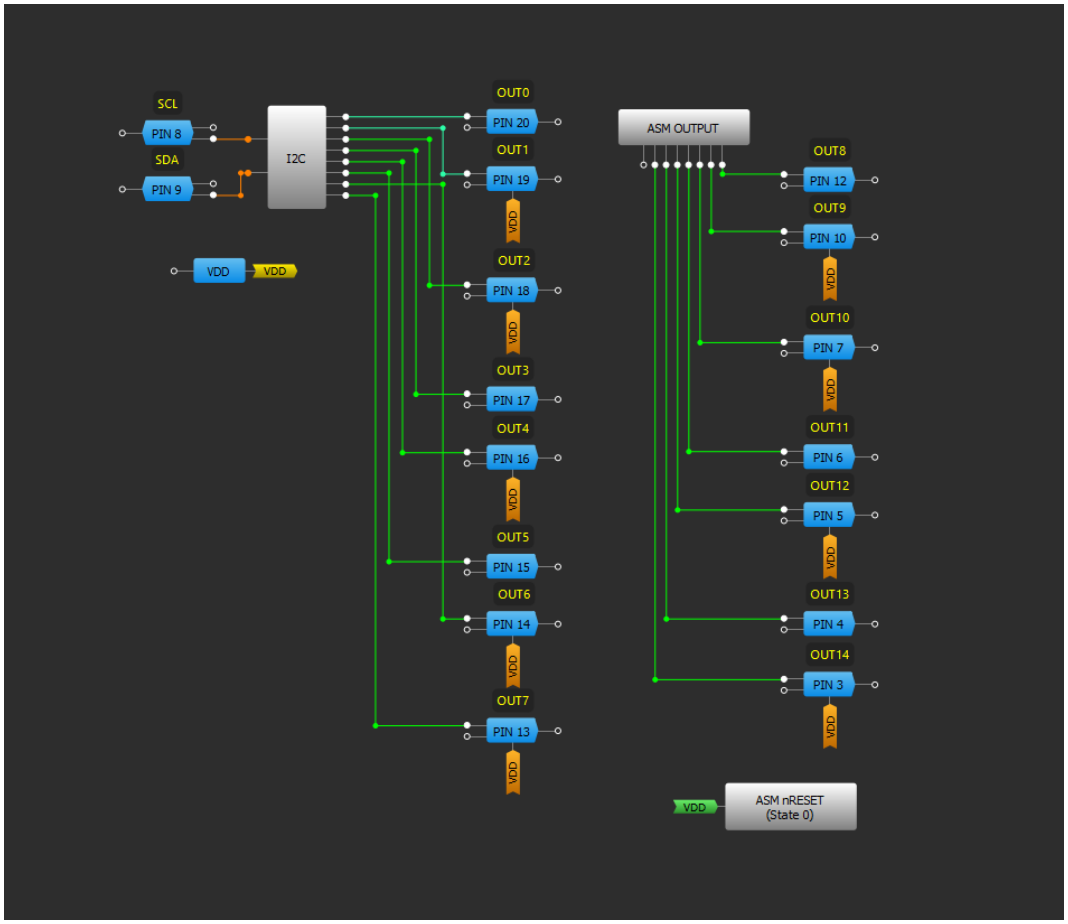


Figure 3-7 SLG46537V (IC11) output internal configuration

3.8.2 Input State Selector

- **Description:** IC12 acts as I/O expander. IC12 monitors 2 x 8-switch slider (J6 and J7).

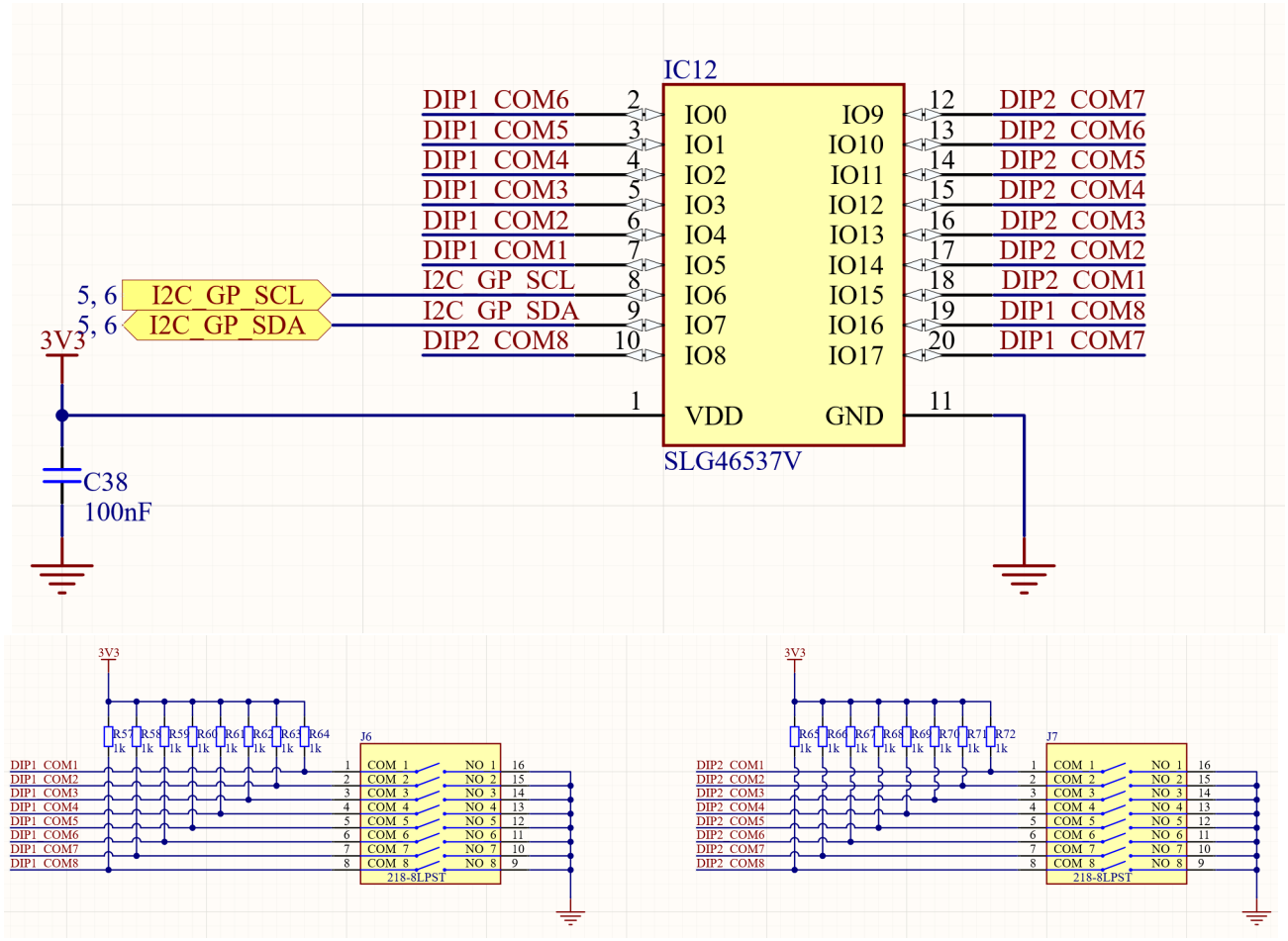


Figure 3-8 SLG46537V (IC12) input schematic

- **Slave address:** 0001b
- **Internal configuration:**

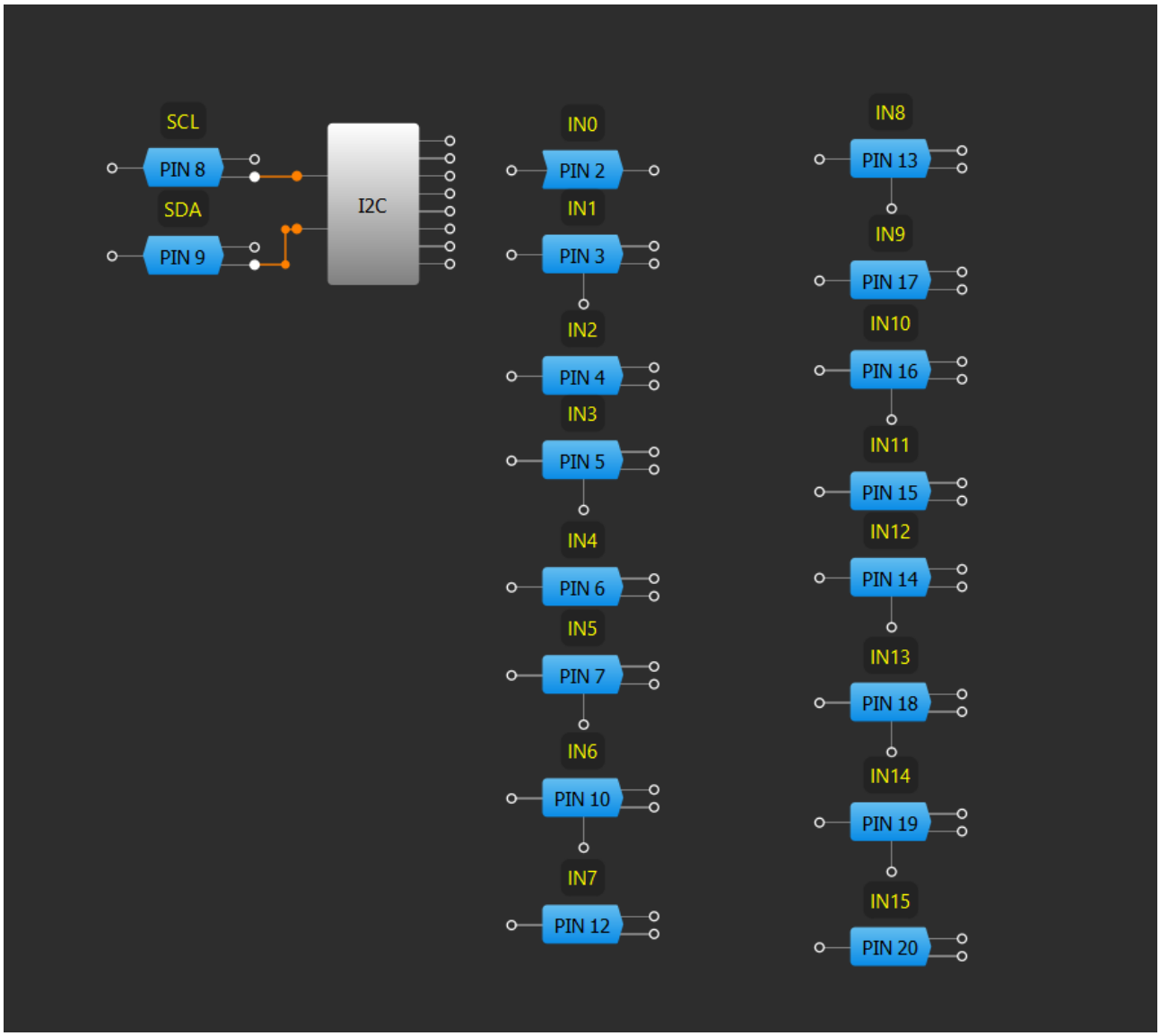


Figure 3-9 SLG46537V (IC12) input internal configuration.

3.8.3 General IO connector

- **Description:** IC13 acts as I/O expander. General 20-pins straight male connector (J8) is available for general input output external connections to IC13:

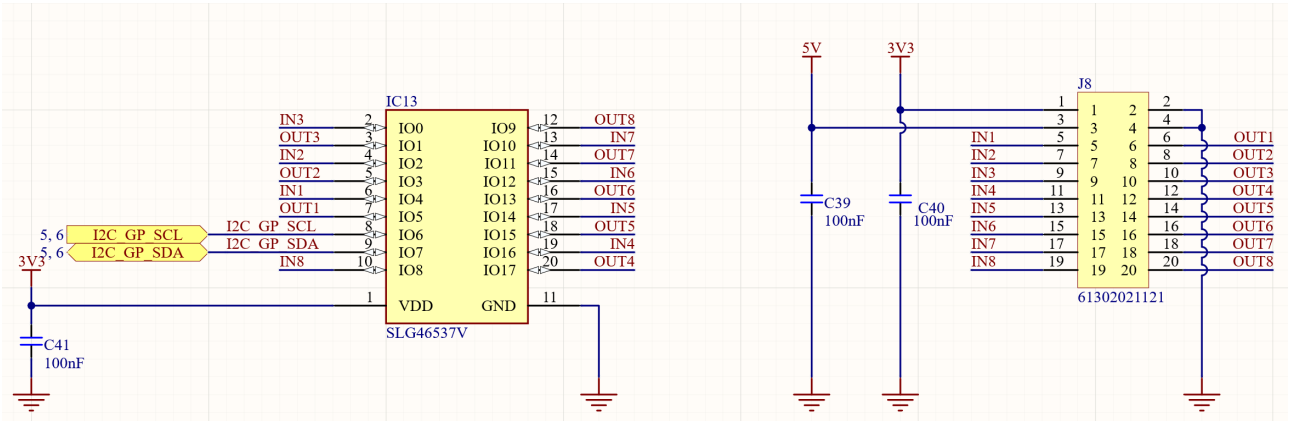


Figure 3-10 SLG46537V (IC13) input and output schematic

Table 3-20 General IO Connector pin (J8) information

Pin number (J8)	Pin state
1	3.3V power supply
2	GND
3	5V power supply
4	GND
5, 7, 9, 11, 13, 15, 17, 19	General input pins
6, 8, 10, 12, 14,16, 18, 20	General output pins

- **Slave address:** 0011b
- **Internal configuration:**

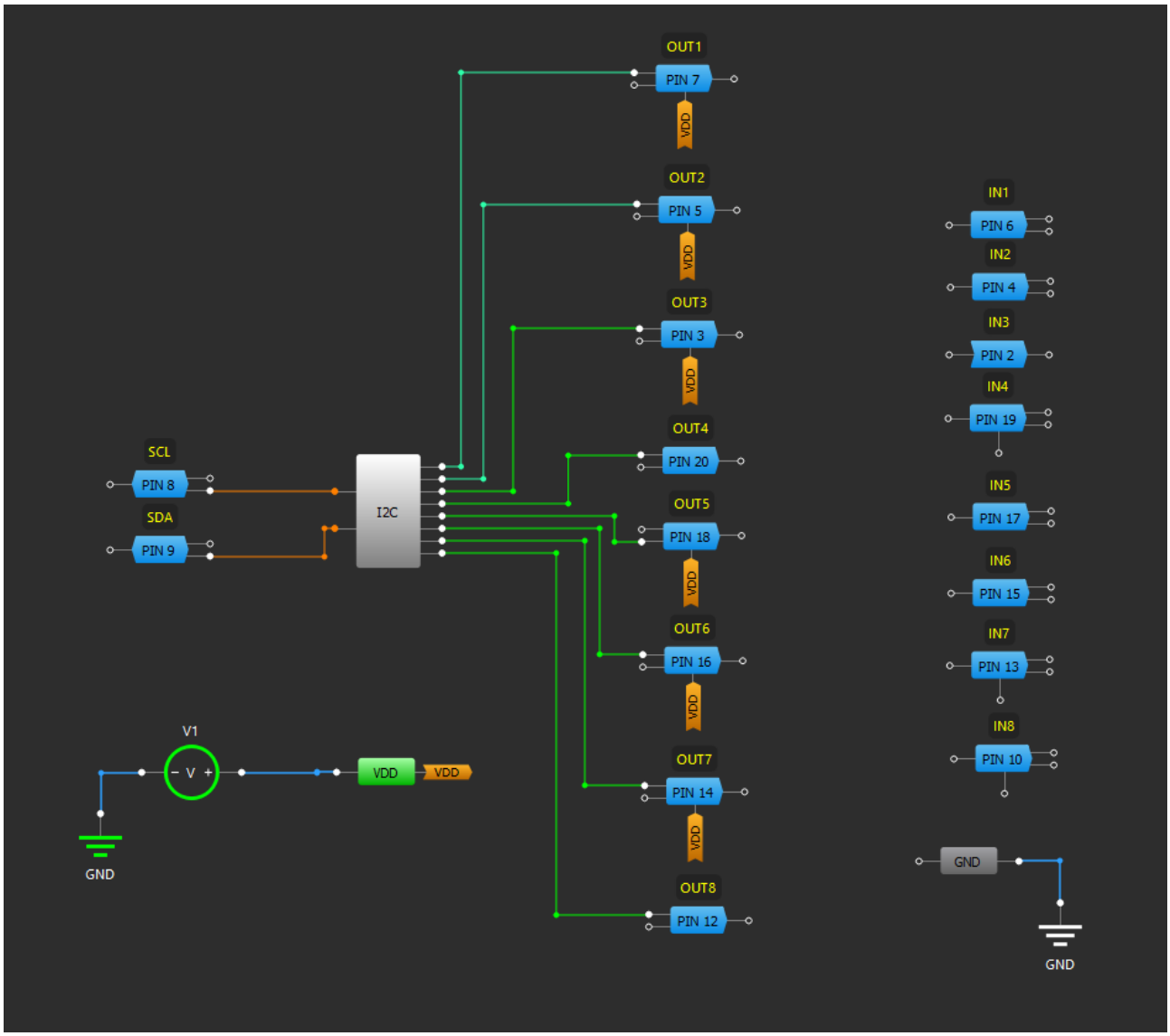


Figure 3-11 SLG46537V (IC13) input and output internal configuration.

3.9 HSPI Interface

The Carrier Board features a Serial Host Interface connector (J15). The serial host interface allows an external SPI master to access the internal resources (mainly System SRAM) of RZ/N2L directly. The Figure 3-12 shows the Serial Host Interface connector diagram.

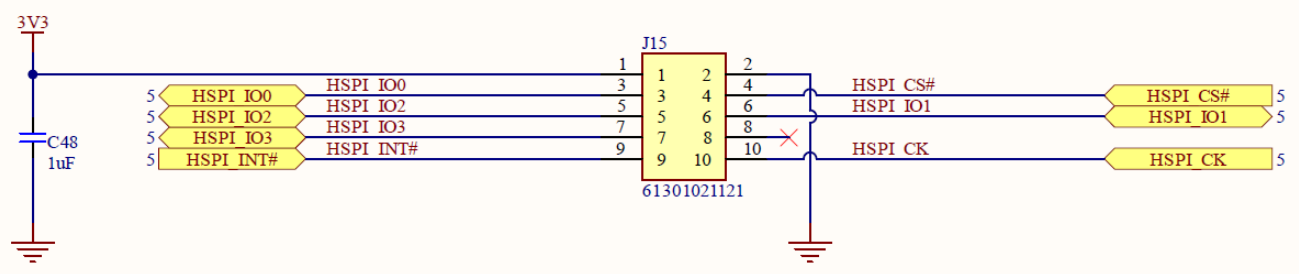


Figure 3-12 Serial Host Interface connector (J15)

Table 3-21 HSPI Interface Pin Assignment (Connector: J15)

MPU			J2	
Pin	Port	Signal	Pin	Signal
-	-	-	1	-
-	-	-	2	-
L14	P14_1	HSPI_IO0	3	HSPI_IO0
G13	P16_0	HSPI_CS#	4	HSPI_CS#
H14	P16_2	HSPI_IO2	5	HSPI_IO2
M14	P14_3	HSPI_IO1	6	HSPI_IO1
G12	P16_3	HSPI_IO3	7	HSPI_IO3
-	-	-	8	-
J12	P14_5	HSPI_INT#/BSC_CS3#	9	HSPI_INT#
K12	P14_2	HSPI_CK	10	HSPI_CK

4. Stamp Module

This chapter describe independent Stamp Module.

4.1 Block diagram

The Stamp Module is shown in outline as a block diagram below. For the pin assigment please refer to chapter 4.2

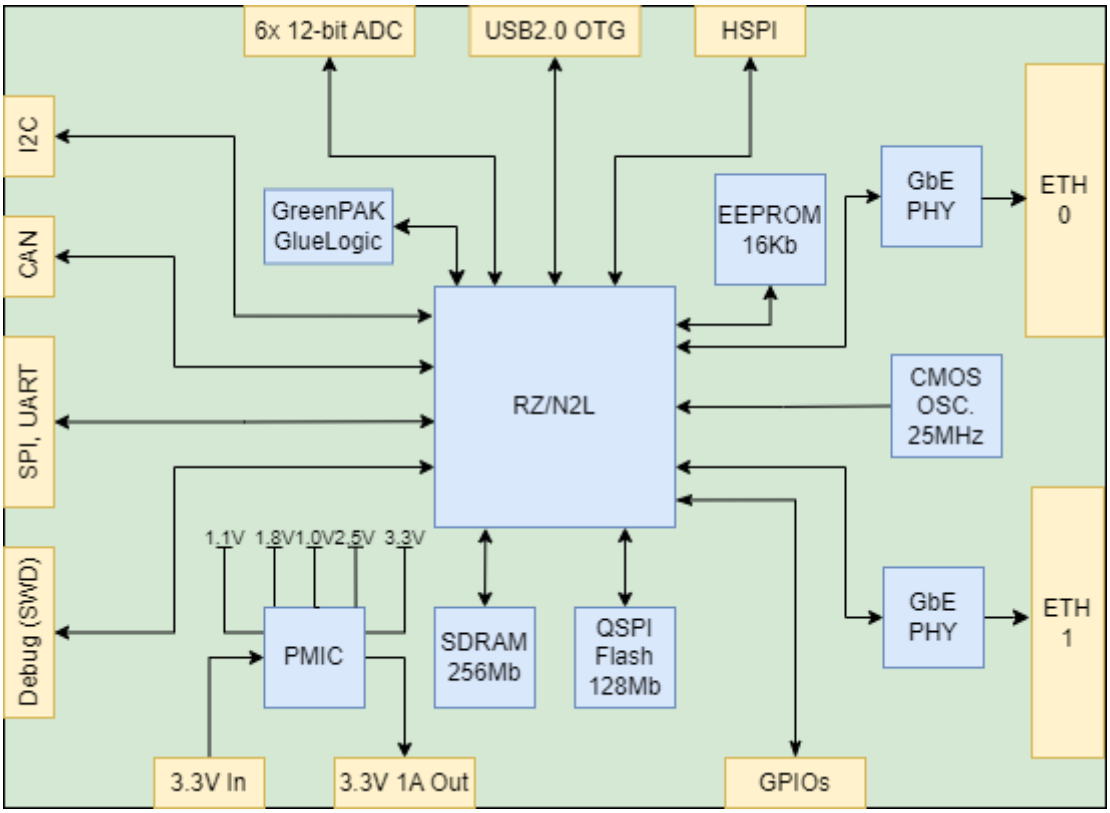


Figure 4-1 Stamp Module Block Diagram

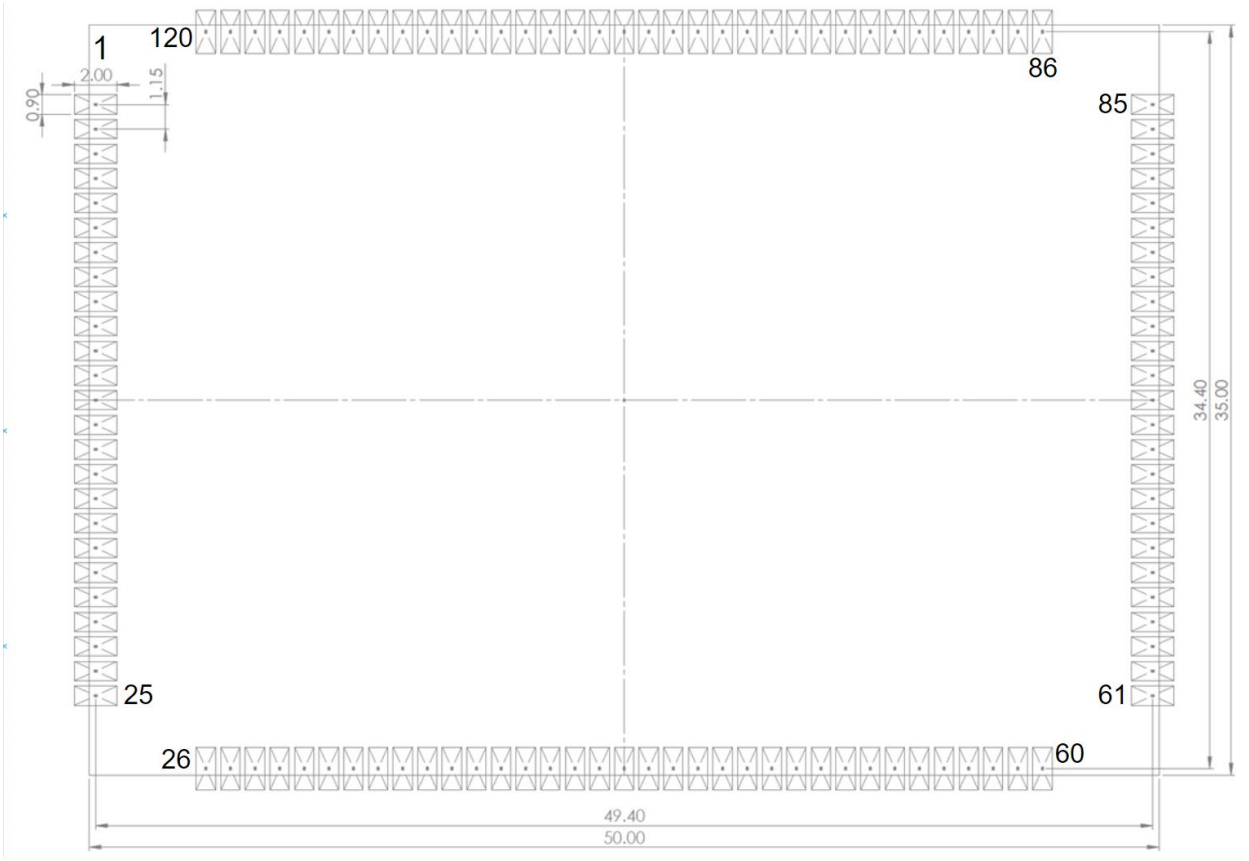


Figure 4-2 Land pattern (Top View)

4.2 Module Pads

The Stamp Module is interfaced via 120 castellated pads. Detailed pin functionality is described in the tables below.

Table 4-1 Stamp Module Pad Description

Pin	Signal	I/O	Description	Function Group	MPU Port
1	GND		Ground		
2	GBE1_MDI3-	I/O	PHY1 Tx/Rx channel D negative signal	GBE	
3	GBE1_MDI3+	I/O	PHY1 Tx/Rx channel D positive signal	GBE	
4	GND		Ground		
5	GBE1_MDI2-	I/O	PHY1 Tx/Rx channel C negative signal	GBE	
6	GBE1_MDI2+	I/O	PHY1 Tx/Rx channel C positive signal	GBE	
7	GND		Ground		
8	GBE1_MDI1-	I/O	PHY1 Tx/Rx channel B negative signal	GBE	
9	GBE1_MDI1+	I/O	PHY1 Tx/Rx channel B positive signal	GBE	
10	GND		Ground		
11	GBE1_MDI0-	I/O	PHY1 Tx/Rx channel A negative signal	GBE	
12	GBE1_MDI0+	I/O	PHY1 Tx/Rx channel A positive signal	GBE	
13	GND		Ground		
14	GBE0_MDI3-	I/O	PHY0 Tx/Rx channel D negative signal	GBE	
15	GBE0_MDI3+	I/O	PHY0 Tx/Rx channel D positive signal	GBE	
16	GND		Ground		
17	GBE0_MDI2-	I/O	PHY0 Tx/Rx channel C negative signal	GBE	
18	GBE0_MDI2+	I/O	PHY0 Tx/Rx channel C positive signal	GBE	
19	GND		Ground		
20	GBE0_MDI1-	I/O	PHY0 Tx/Rx channel B negative signal	GBE	
21	GBE0_MDI1+	I/O	PHY0 Tx/Rx channel B positive signal	GBE	
22	GND		Ground		
23	GBE0_MDI0-	I/O	PHY0 Tx/Rx channel A negative signal	GBE	
24	GBE0_MDI0+	I/O	PHY0 Tx/Rx channel A positive signal	GBE	
25	GND		Ground		
26	GBE0_LINK_1000#	O	LED output for PHY0 1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.	GBE	

Pin	Signal	I/O	Description	Function Group	MPU Port
27	GBE0_LINK_ACT#	O	LED output for PHY0 1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.	GBE	
28	GND		Ground		
29	RST_IN#	I	Inputs the reset signal. The MPU enters the reset state when this signal goes low.	Reset	
30	RST_OUT#	O	Outputs the reset signal externally	Reset	
31	GND		Ground		
32	GND		Ground		
33	P20_3/ESC_LEDSTERR/ETHSW/TDMAOUT2	I/O	General-purpose input/output pin*1	General	P20_3
34	P20_2/ESC_LEDRUN/ETHSW_TDMAOUT1	I/O	General-purpose input/output pin*1	General	P20_2
35	P17_3/SPI_SSL31	I/O	General-purpose input/output pin*1	General	P17_3
36	GND		Ground		
37	TXD3/SDA3/MOSI3	O	SCI3 Serial Communications Interface TX pin	General	P04_1
38	RXD3/SCL3/MISO3	I	SCI3 Serial Communications Interface RX pin	General	P04_0
39	P18_2/GTIOC2B	I/O	General-purpose input/output pin*1	General	P18_2
40	SS3#/CTS3#/RTS3#	I	SCI3 Serial Communications Interface Flow Control pin	General	P18_1
41	P17_6/GTIOC1A/MTIOC3B	I/O	General-purpose input/output pin*1	General	P17_6
42	GND		Ground		
43	AN001	I	Analog input pin for the A/D converter	Analog	AN002
44	AN003	I	Analog input pin for the A/D converter	Analog	AN003
45	AN002	I	Analog input pin for the A/D converter	Analog	AN002
46	AN101	I	Analog input pin for the A/D converter	Analog	AN101
47	AN000	I	Analog input pin for the A/D converter	Analog	AN000
48	AN100	I	Analog input pin for the A/D converter	Analog	AN100
49	GND		Ground		
50	P16_1/SPI_MISO3	I/O	General-purpose input/output pin*1	General	P16_1
51	P18_3/IRQ0	I/O	General-purpose input/output pin*1	General	P18_3

Pin	Signal	I/O	Description	Function Group	MPU Port
52	CTS3#	I	Input the start of transmission (asynchronous mode/clock synchronous mode) active-low	General	P17_4
53	TXD0/SDA0/MOSI0	O	SCI0 Serial Communications Interface TX pin	General	P16_5
54	RXD0/SCL0/MISO0	I	SCI0 Serial Communications Interface RX pin	General	P16_6
55	SCK0	I/O	Clock I/O pin (clock synchronous mode/simple SPI mode/smart card mode)	General	P16_7
56	SS0#/CTS0#/RTS0#	I	SCI0 Serial Communications Interface Flow Control pin	General	P17_0
57	P15_4	I/O	General-purpose input/output pin	General	P15_4
58	GND		Ground		
59	GND		Ground		
60	GND		Ground		
61	GND		Ground		
62	GND		Ground		
63	GND		Ground		
64	VIN		3.3V Input supply		
65	VIN		3.3V Input supply		
66	VIN		3.3V Input supply		
67	VIN		3.3V Input supply		
68	VIN		3.3V Input supply		
69	VIN		3.3V Input supply		
70	VIN		3.3V Input supply		
71	VIN		3.3V Input supply		
72	I2C_GP_SDA	I/O	Input/output of the General Purpose I2C data	General	P18_4
73	I2C_GP_SCL	I/O	Input/output of the General Purpose I2C clock	General	P18_5
74	SWDIO	I/O	SWD Serial Wire Data I/O	General	P02_6
75	SWDCLK	I	SWD Serial Wire Clock	General	P02_7
76	ESC_LATCH0	I	Input the EtherCAT LATCH signal	General	P01_6
77	ESC_LATCH1	I	Input the EtherCAT LATCH signal	General	P13_7 (*)
78	ESC_IRQ	O	Outputs the EtherCAT IRQ signal	General	P14_4
79	GND		Ground		
80	P02_1/ESC_SYNC0/ETHSW_PTPOUT1	I/O	General-purpose input/output pin*1	General	P02_1

Pin	Signal	I/O	Description	Function Group	MPU Port
81	P01_7/SPI_RSPCK3/ CANRX0	I/O	General-purpose input/output pin*1	General	P01_7
82	P02_2/SPI_MOSI3/CA NTX0	I/O	General-purpose input/output pin*1	General	P02_2
83	P00_4/GTIOC0_A	I/O	General-purpose input/output pin*1	General	P00_4
84	P15_3/MTIOC8C	I/O	General-purpose input/output pin*1	General	P15_3
85	P13_6/ESC_SYNC1/E THSW_PTPOUT0	I/O	General-purpose input/output pin*1	General	P13_6
86	GND		Ground		
87	VOUT_3V3		3.3V max. 1A output		
88	VOUT_3V3		3.3V max. 1A output		
89	GND		Ground		
90	GND		Ground		
91	GND		Ground		
92	GND		Ground		
93	GND		Ground		
94	P00_2	I/O	General-purpose input/output pin	General	P00_2
95	P13_5	I/O	General-purpose input/output pin	General	P13_5
96	P14_0	I/O	General-purpose input/output pin	General	P14_0
97	P15_5	I/O	General-purpose input/output pin	General	P15_5
98	GND		Ground		
99	HSPI_INT#	O	QSPI Interrupt output pin	HSPI	P14_5 (**)
100	GND		Ground		
101	HSPI_CK	I	QSPI Clock input pin	HSPI	P14_2
102	GND		Ground		
103	HSPI_IO3	I/O	QSPI Data3 input/output pin	HSPI	P16_3
104	HSPI_IO2	I/O	QSPI Data2 input/output pin	HSPI	P16_2
105	HSPI_IO1	I/O	QSPI Data1 input/output pin	HSPI	P14_3
106	HSPI_IO0	I/O	QSPI Data0 input/output pin	HSPI	P14_1
107	HSPI_CS#	I	QSPI Chip select input pin	HSPI	P16_0
108	GND		Ground		
109	USB_OVRCUR#	I	Inputs the overcurrent signal for USB	USB	P17_5
110	USB_VBUSEN	O	Outputs the VBUS power enable signal for USB	USB	P19_0
111	USB_OTGID	I	OTG ID pin	USB	P02_0

Pin	Signal	I/O	Description	Function Group	MPU Port
112	USB_VBUSIN	I	USB cable connection/disconnection detection input pin	USB	P07_4
113	GND		Ground		
114	GND		Ground		
115	USB_DP	I/O	USB bus D+ data I/O pin	USB	
116	USB_DM	I/O	USB bus D- data I/O pin	USB	
117	GND		Ground		
118	GND		Ground		
119	GBE1_LINK_1000#	O	LED output for PHY1 1: No link in 1000BASE-T. 0: Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.	GBE	
120	GBE1_LINK_ACT#	O	LED output for PHY1 1: No link in any speed on any media interface. 0: Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.	GBE	

(*) Multiplexed with MBX_HINT#. This signal may be useful for communication with host MCU.
(**) Shared with BSC_CS3#. Configured by jumper J2.

Note: MPU port has multiple functionalities which are described in detail in RZ/N2L User's Manual (*R01UH0955EJxxxx*).

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

The Table 3-1 provide the maximum electrical and environmental parameter for the complete Solution Kit. Functional operation above the recommended operating conditions is not guaranteed. Extended exposure to stress above the recommended operating conditions may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (24V) *	V_{CC24}	-0.2 to +40	V
Supply voltage (5V) *	V_{CC5}	4.4 to 5.25	V
Supply voltage (3.3V) *	V_{CC33}	-0.3 to 6.5	V
I/O voltage	VI/Vo	-0.3 to +3.6	V
Permissible output current *(all output pins)*	Io	12	mA
Total permissible output current *(sum of all output pins)*	ΣIo	80	mA
Storage temperature	T_{stg}	-40 to +85	°C

Caution:	**Product quality may suffer if any absolute maximum rating is even momentarily exceeded. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that these ratings are not exceeded.**
Remark:	**3.3 V must be applied to the I/O pins only after applying the power supply voltage.**

* For details on power supply, see chapter 2.

5.2 Operating Conditions

5.2.1 Power Supply

Table 5-2 Power Supply

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply (24V)	Vcc24	10	24	26.4	V
Power supply (5V)	Vcc5		5		V
Power supply (3.3V)	Vcc33	3.15	3.3	3.45	V

5.2.2 DC Characteristics

Table 5-3 DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage high	VIH	2.0		3.435	V
Input voltage low	VIL	-0.3		0.8	V
Output voltage high	VOH	2.735			V
Output voltage low	VOL			0.4	V
Output current low	IOL	2*			mA
Output current high	IOH	-2*			mA
Operating temperature	T_a	0		60	°C

* It can be changed by setting the driving ability control of the I/O port.

All further specifications and statements of timing assume the application of the above-mentioned operating conditions.

5.2.3 PMIC

The soldered Stamp Module features Renesas' DA9083 high-current highly configurable system PMIC, used to obtain all power rails and required timings.

The default power-up sequence described in and internal configuration can be adjusted via I2C_GP commands (address 0x1B) when resistors R71 and R72 are populated.

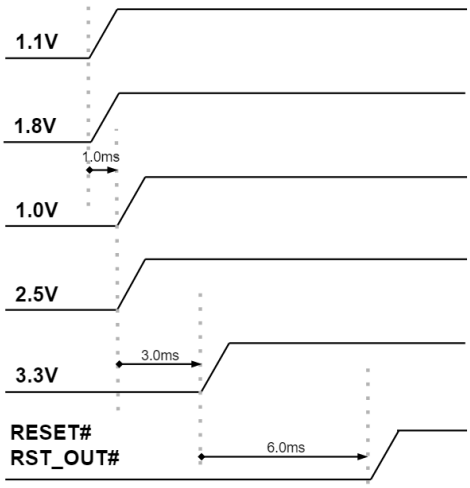


Figure 5-1 PMIC Power-Up sequence

5.2.4 Debug interface

Debugging of the soldered Stamp Module is done using a Serial Wire Debug interface, which requires only two signals in the following table. For a detail specification of the debug interface, see chapter 48.9 in RZ/N2L manual [1].

Table 5-4 Debug Interface Signal Description

Pin	Signal	Description
74	SWDIO	Bidirectional signal, sends and receives serial data from the target. Signal must be pulled HIGH on the target to keep the signal inactive when no debug unit is connected.
75	SWDCLK	Input to the target which clocks data into, and out of, the target device. Signal must be pulled LOW on the target to keep the signal inactive when no debug unit is connected.

5.2.5 I2C Specification

The Stamp Module offers a general-purpose I2C 2-wire serial interface, described below. For a detail specification of the I2C interface, see chapter 33 in RZ/N2L manual [1].

Table 5-5 I2C Signal Description

Pin	Signal	Description

72	I2C_GP_SDA	Serial data line (open-drain*)
73	I2C_GP_SCL	Serial clock line (open-drain*)

***Note**: Pull-up resistors available near PMIC if resistors R71 and R72 are populated. Otherwise, pull-up must be added on the carrier board.*

5.2.6 SPI Specification

The Stamp Module offers multiple configurable serial peripheral interfaces which use 4 signal lines in the following table.

Table 5-6 SPI Signal Description

Signal	Description
SCLK	Serial clock input (output from master)
MOSI	Master output slave Input, or master out slave in (data output from master)
MISO	Master input slave output, or master in slave out (data output from slave)
/SS	Slave select (active low, output from master)

For a detail specification of the SPI timing, see chapter 48.5.5.11 in the RZ/N2L manual [1] .

References

[1] RZ/N2L HW-UM R01UH0955EJxxxx RZ/N2L Group User's Manual: Hardware (renesas.com)

Revision History

Rev.	Date	Description	
		Page	Summary
1.0	30th March 2023	-	Initial version.