User's Manual

RZ/G2LC SMARC Module Board

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

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— Arm® Cortex®-A55
— Arm® Cortex®-M33
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

1.1 Purpose

The RZ/G2LC SMARC Module Board (hereafter referred to as “RZ/G2LC SMARC Module”) is a platform designed according to the SMARC 2.1 Specification to evaluate the Renesas RZ/G2LC microprocessor.

Basically, the RZ/G2LC SMARC Module is connected to the Renesas RZ SMARC Series Carrier Board (hereafter referred to as “RZ SMARC Carrier”) and used as the RZ/G2LC SMARC Evaluation Board Kit (hereafter referred to as “RZ/G2LC EVKIT”).

This guide includes system setup and configuration of the RZ/G2LC SMARC Module. It also provides detailed information on the overall design and use of this board from a hardware system perspective.

1.2 Configuration

Figure 1.1 shows an example of system configuration using the RZ/G2LC SMARC Module.

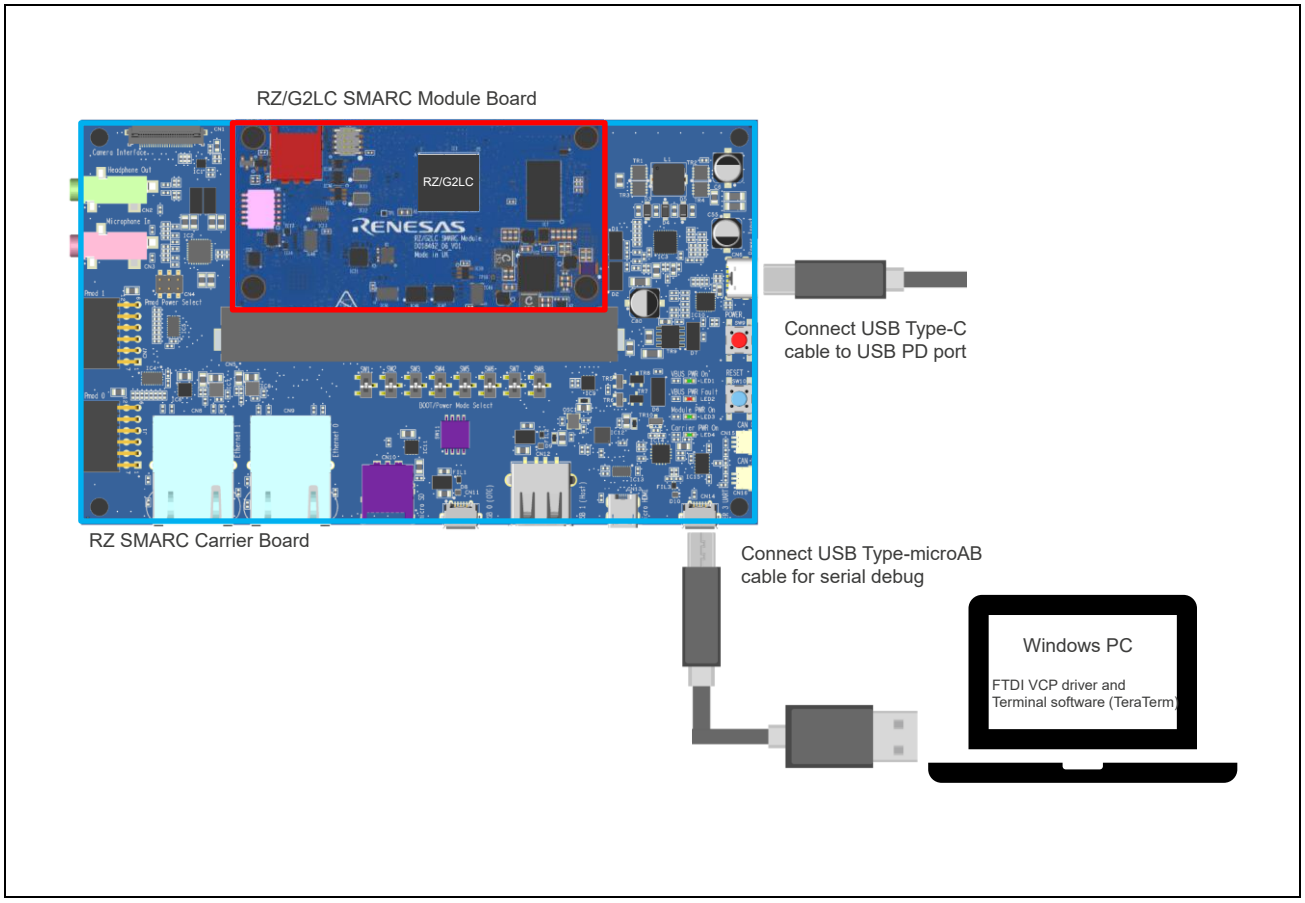


Figure 1.1 Example of System Configuration

1.3 Features

Table 1.1 lists the features of the RZ/G2LC SMARC Module.

Table 1.1 Features

Item	Details
MPU	RZ/G2LC: R9A07G044C22GBG or R9A07G044C26GBG Package: 361-pin LFBGA, 13 mm × 13 mm, 0.5-mm pitch
NOR Flash	Micron MT25QU512ABB8E12-0SIT 512-Mbit
DDR4	Micron MT40A512M16LY-062EIT:E 1-GB 512Mx16, supporting the data rate up to 1600 MT/s
Ethernet Interface	Ethernet PHY: KSZ9131RNXC
Clock	Clock generator: 5P35023B-629NLGI RZ/G2LC main: 24 MHz RZ/G2LC external clock 1 for audio: 11.2896 MHz RZ/G2LC external clock 2 for audio: 12.2880 MHz Ethernet PHY: 25 MHz Audio codec: 11.2896 MHz
Power Supply	PMIC: RAA215300A2GNP#HA0
Debug Interface	Connector: 10-pin with 1.27-mm pitch
eMMC	Micron MTFC64GASAQHD-IT 64-GB, supporting HS200 transfer modes
SD Interface	Connector: microSD card slot Support for default, high-speed, and UHS-I transfer modes, including SDR50 and SDR104
Switch	For mode setting and peripheral selection: 6-bit DIP switch
Boot Mode	Support for eSD, 1.8-V eMMC, 1.8-V SPI, and SCIF download mode
Circuit board specifications	Dimensions: 82 mm (W) × 50 mm (L) × 1.2 mm (H) Mount: Double-sided mounting (6 layers)

1.4 Block Diagram

Figure 1.2 shows a block diagram of the RZ/G2LC SMARC Module.

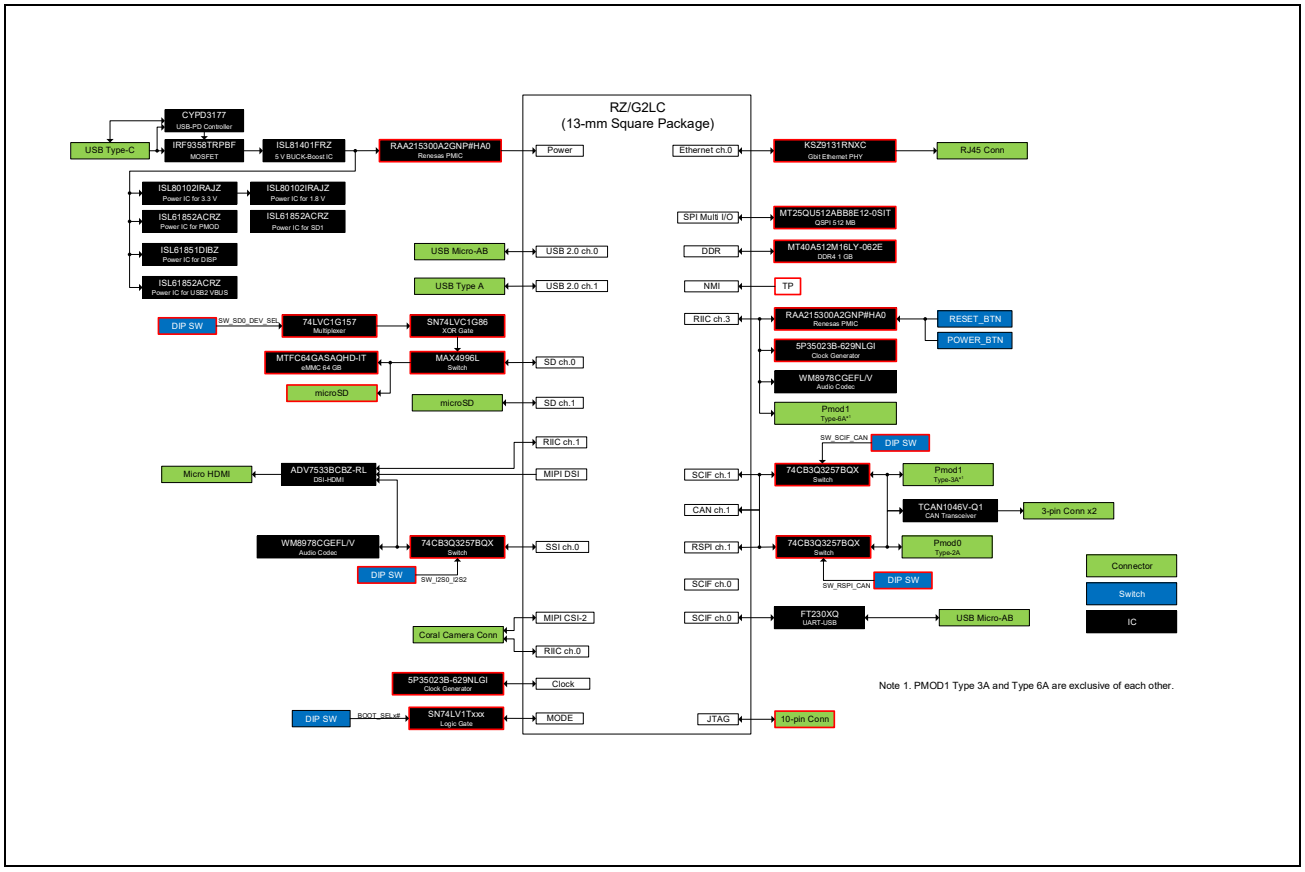


Figure 1.2 Block Diagram

1.5 Layout Components

Figure 1.3 and **Figure 1.4** show the component layouts on the top and bottom sides of the RZ/G2LC SMARC Module.

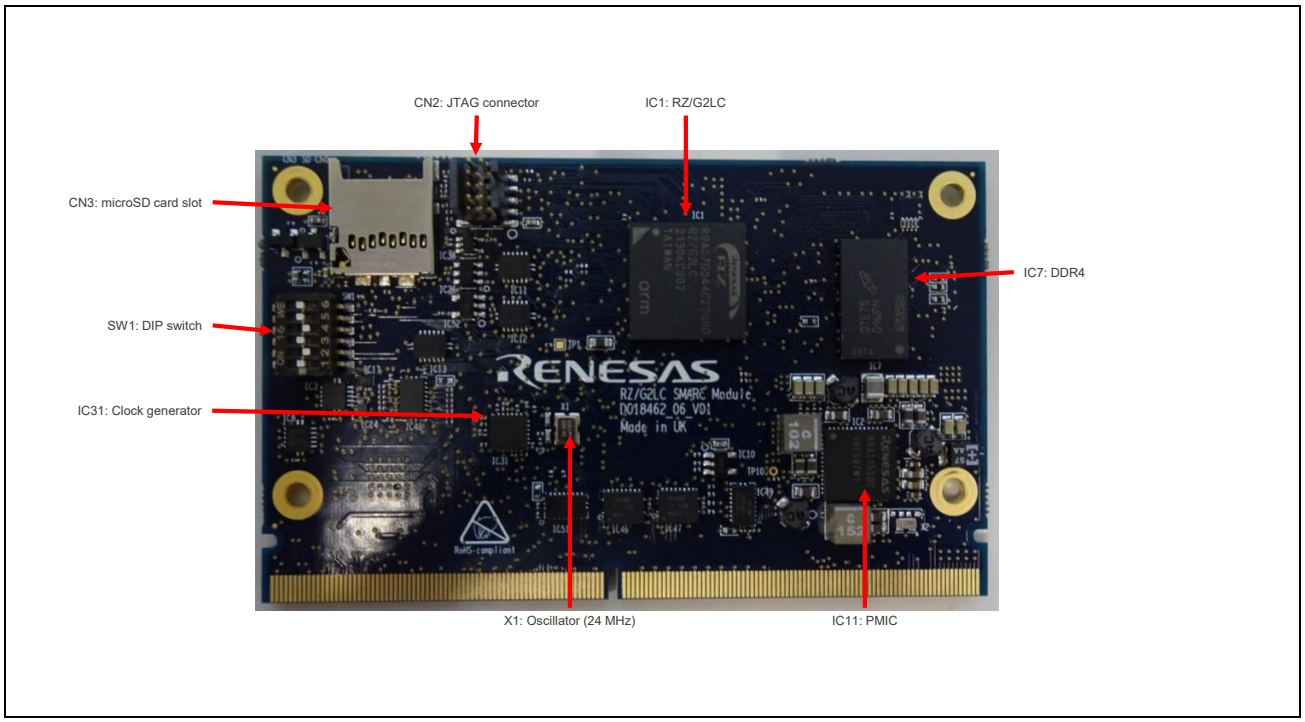


Figure 1.3 Component Layout (Top View)

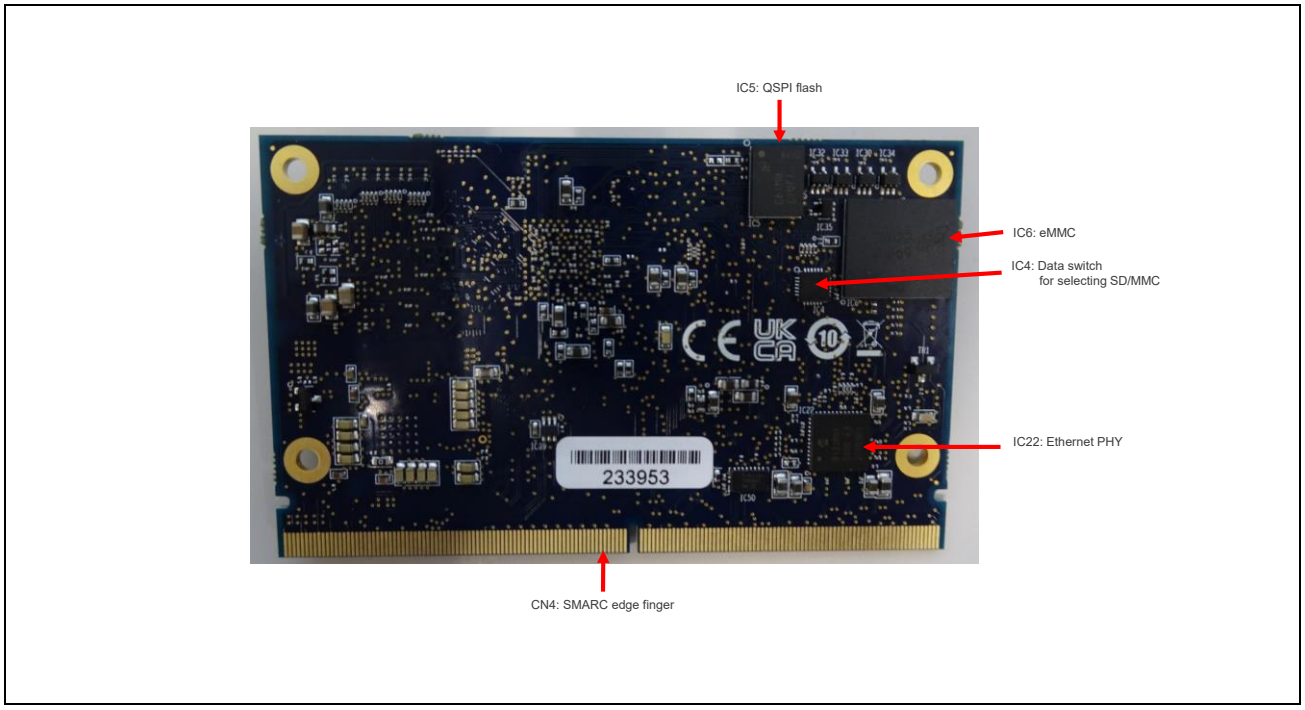


Figure 1.4 Component Layout (Bottom View)

1.6 Absolute Maximum Ratings

Table 1.2 lists the absolute maximum ratings of the RZ/G2LC EVKIT.

Table 1.2 Absolute Maximum Ratings

Symbol	Item	Rated Value	Note
VDD_IN	Power voltage	5.25 V	Reference: Vss
—	Maximum power consumption	3 A	Includes continuous RZ SMARC Carrier current consumption
Topr	Operating ambient temperature*1	0°C to 50°C	Do not expose to condensation or corrosive gases
Tstg	Storage temperature	-10°C to 60°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

1.7 Operating Condition

Table 1.3 lists the operating conditions of the RZ/G2LC EVKIT.

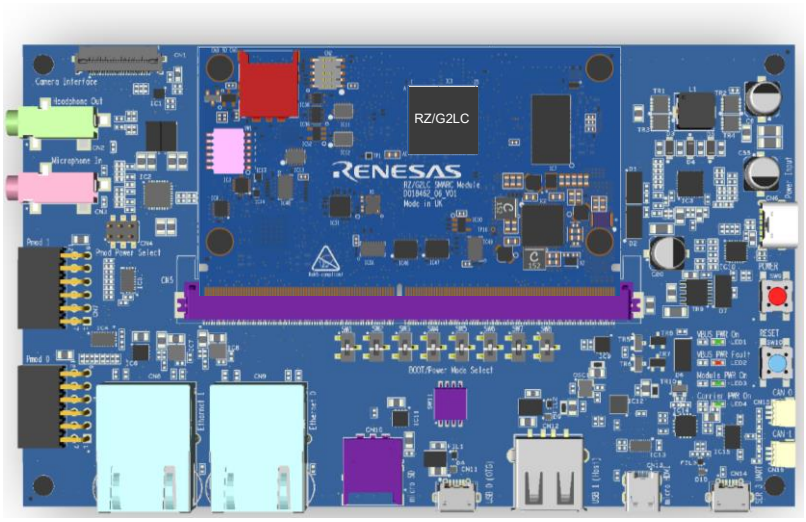
Table 1.3 Operating Conditions

Symbol	Item	Rated Value	Note
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. Ambient temperature is the air temperature at a position as close to the board as possible.

2. Box Contents

Figure 2.1 shows the components included in the box.



RZ/G2LC EVKIT

USB Type-A to micro B cable

Figure 2.1 RZ/G2LC EVKIT

3. Ordering Infomation

RZ/G2LC EVKIT orderable part numbers:

- RTK9744C22S01000BE
- RTK9744C26S01000BE

There are two types of RZ/G2LC EVKIT, as listed above.

RTK9744C22S01000BE is equipped with R9A07G044C22GBG (for which the security is not supported) as the microprocessor.

RTK9744C26S01000BE is equipped with R9A07G044C26GBG (for which the security is supported). RTK9744C26S01000BE can be evaluated the same as RTK9744C22S01000BE if you do not activate the security function.

4. Functional Specifications

4.1 MPU

4.1.1 Processor

The RZ/G2LC includes a dual ARM® Cortex®-A55 core with speeds up to 1.2 GHz, and a single Arm® Cortex®-M33 core with speeds up to 200 MHz.

The Arm® Mali™-G31 as 3D graphics and display output is supported for HMI applications. In addition, many interfaces such as camera input, single 1-Gbit/s Ethernet controllers, and USB 2.0 are supported.

The RZ/G2LC is useful for the following applications:

- Entry-class HMI, embedded devices with GUI capabilities, etc.

For details on the processor, refer to the “RZ/G2L Group, RZ/G2LC Group User’s Manual: Hardware”.

4.1.2 List of RZ/G2LC Pin Functions

Table 4.1 lists the pin functions of the RZ/G2LC for use with the RZ/G2LC SMARC Module.

Table 4.1 List of Pin Function Selections (1/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
F11	VDD18	VDD18	1.8 V	—	—
C11	ABG_NCP_OUT	ABG_NCP_OUT	Connected to VSS via the 1-µF bypass capacitor*1	—	—
B10	AUDIO_CLK1	AUDIO_CLK1	Input 11.2896 MHz from 5P35023 for generating the CD sampling rate (44.1 kHz)	—	—
B9	AUDIO_CLK2	AUDIO_CLK2	Input 12.2880 MHz from 5P35023 for generating the DVD sampling rate (48.0 kHz)	—	—
AC21	BSCANP	BSCANP	Initial setting: 0 (pull-down) It should be controllable by a resistor.	—	—
AC20	VSS	VSS	GND	—	—
AE13	CSI_CLKN	CSI_CLKN	24-pin FFC connector on the RZ SMARC Carrier	P4	CSI1_CLK-
AD13	CSI_CLKP	CSI_CLKP	24-pin FFC connector on the RZ SMARC Carrier	P3	CSI1_CLK+
AE14	CSI_DATA0_N	CSI_DATA0_N	24-pin FFC connector on the RZ SMARC Carrier	P8	CSI1_RX0-
AD14	CSI_DATA0_P	CSI_DATA0_P	24-pin FFC connector on the RZ SMARC Carrier	P7	CSI1_RX0+
AE12	CSI_DATA1_N	CSI_DATA1_N	24-pin FFC connector on the RZ SMARC Carrier	P11	CSI1_RX1-
AD12	CSI_DATA1_P	CSI_DATA1_P	24-pin FFC connector on the RZ SMARC Carrier	P10	CSI1_RX1+
AE15	CSI_DATA2_N	CSI_DATA2_N	24-pin FFC connector on the RZ SMARC Carrier	P14	CSI1_RX2-
AD15	CSI_DATA2_P	CSI_DATA2_P	24-pin FFC connector on the RZ SMARC Carrier	P13	CSI1_RX2+
AE11	CSI_DATA3_N	CSI_DATA3_N	24-pin FFC connector on the RZ SMARC Carrier	P17	CSI1_RX3-
AD11	CSI_DATA3_P	CSI_DATA3_P	24-pin FFC connector on the RZ SMARC Carrier	P16	CSI1_RX3+
Y10	CSI_VDD18	CSI_VDD18	1.8 V	—	—
Y9	CSI_VDD18	CSI_VDD18	1.8 V	—	—
E25	DDR_ADDR0	DDR_ADDR0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K25	DDR_ADDR1	DDR_ADDR1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P23	DDR_ADDR10	DDR_ADDR10	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H25	DDR_ADDR11	DDR_ADDR11	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
N23	DDR_ADDR12	DDR_ADDR12	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
D23	DDR_ADDR13	DDR_ADDR13	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H23	DDR_ADDR14	DDR_ADDR14	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
D25	DDR_ADDR15	DDR_ADDR15	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
C25	DDR_ADDR2	DDR_ADDR2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—

Table 4.1 List of Pin Function Selections (2/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C24	DDR_ADDR3	DDR_ADDR3	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K23	DDR_ADDR4	DDR_ADDR4	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B24	DDR_ADDR5	DDR_ADDR5	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
J25	DDR_ADDR6	DDR_ADDR6	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
A24	DDR_ADDR7	DDR_ADDR7	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
F25	DDR_ADDR8	DDR_ADDR8	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B25	DDR_ADDR9	DDR_ADDR9	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
E24	DDR_BA0	DDR_BA0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
L24	DDR_BA1	DDR_BA1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
F23	DDR_BA2	DDR_BA2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
A23	DDR_CALIBRATION	DDR_CALIBRATION	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
J24	DDR_CAS#	DDR_CAS#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
M25	DDR_CKE	DDR_CKE	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P24	DDR_CLK_N	DDR_CLK_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
P25	DDR_CLK_P	DDR_CLK_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
N24	DDR_CS0#	DDR_CS0#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
L23	DDR_CS1#	DDR_CS1#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
U23	DDR_DM0	DDR_DM0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y24	DDR_DM1	DDR_DM1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T24	DDR_DQ0	DDR_DQ0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y25	DDR_DQ1	DDR_DQ1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W23	DDR_DQ10	DDR_DQ10	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AD25	DDR_DQ11	DDR_DQ11	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AE23	DDR_DQ12	DDR_DQ12	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AA23	DDR_DQ13	DDR_DQ13	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AC24	DDR_DQ14	DDR_DQ14	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AE24	DDR_DQ15	DDR_DQ15	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
R24	DDR_DQ2	DDR_DQ2	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W24	DDR_DQ3	DDR_DQ3	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T25	DDR_DQ4	DDR_DQ4	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
U25	DDR_DQ5	DDR_DQ5	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
R25	DDR_DQ6	DDR_DQ6	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T23	DDR_DQ7	DDR_DQ7	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AD24	DDR_DQ8	DDR_DQ8	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AA24	DDR_DQ9	DDR_DQ9	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V24	DDR_DQS0_N	DDR_DQS0_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V25	DDR_DQS0_P	DDR_DQS0_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB25	DDR_DQS1_N	DDR_DQS1_N	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB24	DDR_DQS1_P	DDR_DQS1_P	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
M24	DDR_ODT0	DDR_ODT0	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
L25	DDR_ODT1	DDR_ODT1	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
H24	DDR_RAS#	DDR_RAS#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
B23	DDR_RESET#	DDR_RESET#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
AB23	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—

Table 4.1 List of Pin Function Selections (3/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
H20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
K20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
T20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
V20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
W20	DDR_VDDQ	DDR_VDDQ	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
G25	DDR_WE#	DDR_WE#	DDR4 SDRAM (MT40A512M16LY-062EIT:E)	—	—
Y18	DEBUGEN	DEBUGEN	DIP_SW (SW1)	—	—
AD19	DSI_CLKN	DSI_CLKN	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S135	DSI0_CLK-
AE19	DSI_CLKP	DSI_CLKP	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S134	DSI0_CLK+
AD18	DSI_DATA0_N	DSI_DATA0_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S126	DSI0_D0-
AE18	DSI_DATA0_P	DSI_DATA0_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S125	DSI0_D0+
AD20	DSI_DATA1_N	DSI_DATA1_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S129	DSI0_D1-
AE20	DSI_DATA1_P	DSI_DATA1_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S128	DSI0_D1+
AD17	DSI_DATA2_N	DSI_DATA2_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S132	DSI0_D2-
AE17	DSI_DATA2_P	DSI_DATA2_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S131	DSI0_D2+
AD21	DSI_DATA3_N	DSI_DATA3_N	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S138	DSI0_D3-
AE21	DSI_DATA3_P	DSI_DATA3_P	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S137	DSI0_D3+
Y14	DSI_VDD18	DSI_VDD18	1.8 V	—	—
Y15	DSI_VDD18	DSI_VDD18	1.8 V	—	—
N1	P28_1/ET0_LINKSTA	ET0_LINKSTA	Ethernet 0 PHY (KSZ9131RNXC)	—	—
T1	P27_1/ET0_MDC/RSPI1_SSL/MTIOC8D	ET0_MDC	Ethernet 0 PHY (KSZ9131RNXC)	—	—
R2	P28_0/ET0_MDIO	ET0_MDIO	Ethernet 0 PHY (KSZ9131RNXC)	—	—
N2	P24_1/ET0_RX_CTL_RX_DV/SSI1_RCK/POE4_N	ET0_RX_CTL_RX_DV	Ethernet 0 PHY (KSZ9131RNXC)	—	—
P2	P24_0/ET0_RXC_RX_CLK/SSI1_BCK/POE0_N	ET0_RXC_RX_CLK	Ethernet 0 PHY (KSZ9131RNXC)	—	—
N3	P25_0/ET0_RXD0/SSI1_TXD/POE8_N	ET0_RXD0	Ethernet 0 PHY (KSZ9131RNXC)	—	—
P3	P25_1/ET0_RXD1/SSI1_RXD/POE10_N	ET0_RXD1	Ethernet 0 PHY (KSZ9131RNXC)	—	—
R1	P26_0/ET0_RXD2/RSPI1_CK/MTIOC8A	ET0_RXD2	Ethernet 0 PHY (KSZ9131RNXC)	—	—
P1	P26_1/ET0_RXD3/RSPI1_MOSI/MTIOC8B	ET0_RXD3	Ethernet 0 PHY (KSZ9131RNXC)	—	—
L1	P20_1/ET0_TX_CTL_TX_EN/RSPI0_MOSI/CAN0_TX	ET0_TX_CTL_TX_EN	Ethernet 0 PHY (KSZ9131RNXC)	—	—

Table 4.1 List of Pin Function Selections (4/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
M2	P20_0/ET0_TXC_TX_CLK/RSPI0_CK/CAN_CLK	ET0_TXC_TX_CLK	Ethernet 0 PHY (KSZ9131RNXC)	—	—
L2	P20_2/ET0_TXD0/RSPI0_MISO/CAN0_RX	ET0_TXD0	Ethernet 0 PHY (KSZ9131RNXC)	—	—
K1	P21_0/ET0_TXD1/RSPI0_SSL/CAN0_TX_DATARATE_EN	ET0_TXD1	Ethernet 0 PHY (KSZ9131RNXC)	—	—
J1	P21_1/ET0_TXD2/CAN0_RX_DATARATE_EN	ET0_TXD2	Ethernet 0 PHY (KSZ9131RNXC)	—	—
J2	P22_0/ET0_TXD3/SSI0_BCK/CAN1_TX/MTCLKA	ET0_TXD3	Ethernet 0 PHY (KSZ9131RNXC)	—	—
M3	PVDD182533_0	PVDD182533_0	1.8 V	—	—
N6	PVDD182533_0	PVDD182533_0	1.8 V	—	—
AA3	EXCLK	EXCLK	Input 24 MHz from 5P35023 for generating system clock	—	—
T3	VDD18	VDD18	1.8 V	—	—
A4	MD_BOOT0	MD_BOOT0	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
C5	MD_BOOT1	MD_BOOT1	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
B5	MD_BOOT2	MD_BOOT2	Input BOOT_SEL0#, BOOT_SEL1#, BOOT_SEL3# logic states	P123, P124, P125	BOOT_SEL 0#,1#,2#
A21	MD_CLKS	MD_CLKS	Initial setting: 1 (pull-up) It should be controllable by a resistor.	—	—
C21	MD_OSCDRV0	MD_OSCDRV0	Initial setting: 0 (pull-down) It should be controllable by a resistor.	—	—
B21	MD_OSCDRV1	MD_OSCDRV1	Initial setting: 0 (pull-down) It should be controllable by a resistor.		
AD2	NMI	NMI	Connected to the test pin (TP1)	—	—
F14	OTP_VDD18	OTP_VDD18	1.8 V	—	—
M6	PLL1_AVDD18	PLL1_AVDD18	1.8 V	—	—
V3	PLL23_AVDD18	PLL23_AVDD18	1.8 V	—	—
W3	PLL23_AVDD18	PLL23_AVDD18	1.8 V	—	—
T6	PLL23_DVDD11	PLL23_DVDD11	1.1 V	—	—
U6	PLL23_DVDD11	PLL23_DVDD11	1.1 V	—	—
P20	PLL4_AVDD18	PLL4_AVDD18	1.8 V	—	—
Y11	PLL5_AVDD18	PLL5_AVDD18	1.8 V	—	—
Y13	PLL5_DVDD11	PLL5_DVDD11	1.1 V	—	—
F12	PLL6_AVDD18	PLL6_AVDD18	1.8 V	—	—
Y2	PRST#	PRST#	Input system reset signal from RAA215300	—	—

Table 4.1 List of Pin Function Selections (5/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
AC4	PVDD	PVDD	3.3 V	—	—
Y6	PVDD	PVDD	3.3 V	—	—
AC14	PVDD	PVDD	3.3 V	—	—
AD10	PVDD	PVDD	3.3 V	—	—
Y16	PVDD	PVDD	3.3 V	—	—
Y19	PVDD	PVDD	3.3 V	—	—
C3	PVDD	PVDD	3.3 V	—	—
F15	PVDD	PVDD	3.3 V	—	—
F17	PVDD	PVDD	3.3 V	—	—
F20	PVDD	PVDD	3.3 V	—	—
B8	QSPI_INT#	QSPI_INT#	Connected to a pull-up resistor by the SPI_PVDD power supply*1	—	—
A8	QSPI_RESET#	QSPI_RESET#	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
A7	QSPI_WP#	QSPI_WP#	Unused	—	—
B7	QSPI0_IO0	QSPI0_IO0	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
A6	QSPI0_IO1	QSPI0_IO1	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C8	QSPI0_IO1	QSPI0_IO1	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C7	QSPI0_IO2	QSPI0_IO2	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C6	QSPI0_IO3	QSPI0_IO3	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
A5	QSPI0_SPCLK	QSPI0_SPCLK	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
E1	QSPI0_SSL	QSPI0_SSL	QSPI flash memory (MT25QU512ABB8E12-0SIT)	—	—
C1	SD0_CLK	SD0_CLK	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
F3	SD0_CMD	SD0_CMD	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
E2	SD0_DATA0	SD0_DATA0	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
D1	SD0_DATA1	SD0_DATA1	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
B1	SD0_DATA2	SD0_DATA2	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
D2	SD0_DATA3	SD0_DATA3	eMMC memory (MTFC64GASAQHD-IT) or microSD ch. 0 card slot	—	—
C2	SD0_DATA4	SD0_DATA4	eMMC memory (MTFC64GASAQHD-IT)	—	—
D3	SD0_DATA5	SD0_DATA5	eMMC memory (MTFC64GASAQHD-IT)	—	—

Table 4.1 List of Pin Function Selections (6/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
E3	SD0_DATA6	SD0_DATA6	eMMC memory (MTFC64GASAQHD-IT)	—	—
F6	SD0_DATA7	SD0_DATA7	eMMC memory (MTFC64GASAQHD-IT)	—	—
H6	SD0_PVDD	SD0_PVDD	1.8 V/3.3 V	—	—
B2	SD0_RST#	SD0_RST#	eMMC memory (MTFC64GASAQHD-IT)	—	—
H3	SD1_CLK	SD1_CLK	microSD ch. 1 card slot on the RZ SMARC Carrier	P36	SDIO_CK
F2	SD1_CMD	SD1_CMD	microSD ch. 1 card slot on the RZ SMARC Carrier	P34	SDIO_CMD
G2	SD1_DATA0	SD1_DATA0	microSD ch. 1 card slot on the RZ SMARC Carrier	P39	SDIO_D0
G3	SD1_DATA1	SD1_DATA1	microSD ch. 1 card slot on the RZ SMARC Carrier	P40	SDIO_D1
G1	SD1_DATA2	SD1_DATA2	microSD ch. 1 card slot on the RZ SMARC Carrier	P41	SDIO_D2
H2	SD1_DATA3	SD1_DATA3	microSD ch. 1 card slot on the RZ SMARC Carrier	P42	SDIO_D3
J3	SD1_PVDD	SD1_PVDD	1.8 V/3.3 V	—	—
K6	SD1_PVDD	SD1_PVDD	1.8 V/3.3 V	—	—
B13	P38_1/SCIF0_RXD/ GTETRGB/CAN0_TX/ MTIOC4B/USB1_OV RCUR	SCIF0_RXD	Debug UART on the RZ SMARC Carrier	P141	SER3_RX
C13	P38_0/SCIF0_TXD/ GTETRGA/CAN_CLK /MTIOC4A/USB1_VB USEN	SCIF0_TXD	Debug UART on the RZ SMARC Carrier	P140	SER3_TX
AC22	VSS	VSS	GND	—	—
C22	VSS	VSS	GND	—	—
F10	SPI_PVDD	SPI_PVDD	1.8 V	—	—
F8	SPI_PVDD	SPI_PVDD	1.8 V	—	—
J13	VDD	VDD	1.1 V	—	—
M14	VSS	VSS	GND	—	—
P14	VSS	VSS	GND	—	—
P6	VSS	VSS	GND	—	—
R6	VSS	VSS	GND	—	—
U11	VDD	VDD	1.1 V	—	—
AD22	VSS	VSS	GND	—	—
T14	VSS	VSS	GND	—	—
U13	VDD	VDD	1.1 V	—	—
U2	TCK/SWDCLK	TCK/SWDCLK	Connected to the JTAG connector (CN2)	—	—
V6	VSS	VSS	GND	—	—
AE22	VSS	VSS	GND	—	—
F7	VSS	VSS	GND	—	—
J15	VDD	VDD	1.1 V	—	—
L15	VSS	VSS	GND	—	—
W2	TDI	TDI	Connected to the JTAG connector (CN2)	—	—
A9	VSS	VSS	GND	—	—
C23	VSS	VSS	GND	—	—
N15	VSS	VSS	GND	—	—
U15	VDD	VDD	1.1 V	—	—

Table 4.1 List of Pin Function Selections (7/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
V2	TDO	TDO	Connected to the JTAG connector (CN2)	—	—
C9	VSS	VSS	GND	—	—
E23	VSS	VSS	GND	—	—
J17	VDD	VDD	1.1 V	—	—
R15	VSS	VSS	GND	—	—
Y17	VSS	VSS	GND	—	—
AC15	VSS	VSS	GND	—	—
F9	VSS	VSS	GND	—	—
G23	VSS	VSS	GND	—	—
L17	VDD	VDD	1.1 V	—	—
V1	TMS/SWDIO	TMS/SWDIO	Connected to the JTAG connector (CN2)	—	—
F16	VSS	VSS	GND	—	—
J23	VSS	VSS	GND	—	—
K10	VSS	VSS	GND	—	—
N17	VDD	VDD	1.1 V	—	—
W1	TRST#	TRST#	Connected to the JTAG connector (CN2)	—	—
W6	VDD18	VDD18	1.8 V	—	—
R17	VDD	VDD	1.1 V	—	—
M10	VSS	VSS	GND	—	—
K16	VSS	VSS	GND	—	—
M23	VSS	VSS	GND	—	—
AC9	USB_AVDD18	USB_AVDD18	1.8 V	—	—
AC8	USB_RREF	USB_RREF	Connected to GND via the 1.8-Ω resistor	—	—
AC5	USB_VDD18	USB_VDD18	1.8 V	—	—
AC6	USB_VDD18	USB_VDD18	1.8 V	—	—
Y7	USB_VDD33	USB_VDD33	3.3 V	—	—
Y8	USB_VDD33	USB_VDD33	3.3 V	—	—
AD6	VSS	VSS	GND	—	—
AE6	VSS	VSS	GND	—	—
AC7	VSS	VSS	GND	—	—
AE9	VSS	VSS	GND	—	—
AE8	USB0_DM	USB0_DM	USB2.0 OTG on the RZ SMARC Carrier	P61	USB0-
AD8	USB0_DP	USB0_DP	USB2.0 OTG on the RZ SMARC Carrier	P60	USB0+
AD9	USB0_VBUSIN	USB0_VBUSIN	USB2.0 OTG on the RZ SMARC Carrier	P63	USB0_VBUS_DET
AE7	USB1_DM	USB1_DM	USB2.0 Host on the RZ SMARC Carrier	P66	USB1-
AD7	USB1_DP	USB1_DP	USB2.0 Host on the RZ SMARC Carrier	P65	USB1+
U17	VDD	VDD	1.1 V	—	—
M20	VDD	VDD	1.1 V	—	—
J9	VDD	VDD	1.1 V	—	—
L9	VDD	VDD	1.1 V	—	—

Table 4.1 List of Pin Function Selections (8/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
N9	VDD	VDD	1.1 V	—	—
R9	VDD	VDD	1.1 V	—	—
J11	VDD	VDD	1.1 V	—	—
U9	VDD	VDD	1.1 V	—	—
M16	VSS	VSS	GND	—	—
P10	VSS	VSS	GND	—	—
R23	VSS	VSS	GND	—	—
P16	VSS	VSS	GND	—	—
T10	VSS	VSS	GND	—	—
V23	VSS	VSS	GND	—	—
A1	VDD	VDD	1.1 V	—	—
F1	VSS	VSS	GND	—	—
H1	VSS	VSS	GND	—	—
U1	VSS	VSS	GND	—	—
AA1	VSS	VSS	GND	—	—
AC1	VSS	VSS	GND	—	—
AE1	VSS	VSS	GND	—	—
T2	VSS	VSS	GND	—	—
AC10	VSS	VSS	GND	—	—
AE10	VSS	VSS	GND	—	—
L11	VSS	VSS	GND	—	—
N11	VSS	VSS	GND	—	—
R11	VSS	VSS	GND	—	—
AC11	VSS	VSS	GND	—	—
A12	VSS	VSS	GND	—	—
K12	VSS	VSS	GND	—	—
T16	VSS	VSS	GND	—	—
AC16	VSS	VSS	GND	—	—
AD16	VSS	VSS	GND	—	—
AE16	VSS	VSS	GND	—	—
AC17	VSS	VSS	GND	—	—
F18	VSS	VSS	GND	—	—
AC18	VSS	VSS	GND	—	—
F19	VSS	VSS	GND	—	—
Y23	VSS	VSS	GND	—	—
AC23	VSS	VSS	GND	—	—
AD23	VSS	VSS	GND	—	—
D24	VSS	VSS	GND	—	—
F24	VSS	VSS	GND	—	—
G24	VSS	VSS	GND	—	—
K24	VSS	VSS	GND	—	—
U24	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function Selections (9/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A25	VSS	VSS	GND	—	—
AA2	VSS	VSS	GND	—	—
AC19	VSS	VSS	GND	—	—
AC2	VSS	VSS	GND	—	—
C20	VSS	VSS	GND	—	—
M12	VSS	VSS	GND	—	—
N25	VSS	VSS	GND	—	—
P12	VSS	VSS	GND	—	—
G20	VSS	VSS	GND	—	—
R3	VSS	VSS	GND	—	—
T12	VSS	VSS	GND	—	—
W25	VSS	VSS	GND	—	—
AA25	VSS	VSS	GND	—	—
J20	VSS	VSS	GND	—	—
U3	VSS	VSS	GND	—	—
Y12	VSS	VSS	GND	—	—
AC12	VSS	VSS	GND	—	—
AC25	VSS	VSS	GND	—	—
L20	VSS	VSS	GND	—	—
Y3	VSS	VSS	GND	—	—
B6	VSS	VSS	GND	—	—
G6	VSS	VSS	GND	—	—
F13	VSS	VSS	GND	—	—
L13	VSS	VSS	GND	—	—
N13	VSS	VSS	GND	—	—
R13	VSS	VSS	GND	—	—
N20	VSS	VSS	GND	—	—
R20	VSS	VSS	GND	—	—
U20	VSS	VSS	GND	—	—
Y20	VSS	VSS	GND	—	—
AE25	VSS	VSS	GND	—	—
AB3	VSS	VSS	GND	—	—
C4	VSS	VSS	GND	—	—
A22	VSS	VSS	GND	—	—
AC13	VSS	VSS	GND	—	—
B22	VSS	VSS	GND	—	—
J6	VSS	VSS	GND	—	—
K14	VSS	VSS	GND	—	—
L6	VSS	VSS	GND	—	—

Table 4.1 List of Pin Function Selections (10/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
C19	WDTOVF_PERROUT#	WDTOVF_PERROUT#	Input hardware reset signal from RAA215300	—	—
AB2	XIN	XIN	GND	—	—
AB1	XOUT	XOUT	Open	—	—
A19	RIIC1_SCL	RIIC1_SCL	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S139	I2C_LCD_CK
A20	RIIC1_SDA	RIIC1_SDA	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S140	I2C_LCD_DAT
B19	RIIC0_SDA	RIIC0_SDA	24-pin FFC connector on the RZ SMARC Carrier	S1	I2C_CAM1_CK
B20	RIIC0_SCL	RIIC0_SCL	24-pin FFC connector on the RZ SMARC Carrier	S2	I2C_CAM1_DAT
C12	P0_0/IRQ0/SCI0_RXD/GTIOC0A/MTIOC0A/SCIF3_TXD	IRQ0	Ethernet 0 PHY (KSZ9131RNXC)	—	—
B12	P0_1/IRQ1/SCI0_TXD/GTIOC0B/MTIOC0B/SCIF3_RXD	P0_1	24-pin FFC connector on the RZ SMARC Carrier	P109	GPIO1/CAM1_PWR#
B3	P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A	SD0_CD	microSD ch. 0 card slot	—	—
A3	P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B	P18_1	microSD ch. 0 card slot For switching the power of the card slot on or off	—	—
A2	P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA	SD1_CD	microSD ch. 1 card slot on the RZ SMARC Carrier	P35	SDIO_CD#
B4	P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL	P19_1	For selecting the device connected to the SD/MMC ch. 0 interface Input SD0_DEV_SEL signal to identify the device connected to the SD ch. 0 interface by software	—	—
K2	P22_1/ET0_TX_ERR/SSI0_RCK/CAN1_RX/MTCLKB	P22_1	PMOD0 Type-2A on the RZ SMARC Carrier	P114	GPIO6/TACHIN
L3	P23_0/ET0_TX_COL/SSI0_TXD/CAN1_TX_DATARATE_EN/MTCLKC	P23_0	PMOD0 Type-2A on the RZ SMARC Carrier	P115	GPIO7
K3	P23_1/ET0_TX_CRS/SSI0_RXD/CAN1_RX_DATARATE_EN/MTCLKD	P23_1	PMOD1 Type-6A on the RZ SMARC Carrier	S142	GPIO12
M1	P27_0/ET0_RX_ERR/RSPI1_MISO/MTIOC8C	P27_0	PMOD1 Type-6A on the RZ SMARC Carrier	S123	GPIO13
A13	P39_0/SCIF0_SCK/GTETRGC/CAN0_RX/MTIOC4C	P39_0	RAA215300 For selecting the voltage of the microSD ch. 0 card	—	—
B14	P39_1/SCIF0_CTS/GTETRGD/CAN0_TX_DATARATE_EN/MTIOC4D	P39_1	RAA215300 For selecting the voltage of the microSD ch. 1 card	—	—

Table 4.1 List of Pin Function Selections (11/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A14	P39_2/SCIF0_RTS/ CAN0_RX_DATARATE_EN	P39_2	microSD ch. 1 card slot on the RZ SMARC Carrier For switching the power of the card slot on or off	P37	SDIO_PWR_EN
AE5	P4_0/USB0_VBUSEN /SCIF2_TXD/MTIOC7A/ADC_TRG	USB0_VBUSEN	USB2.0 OTG on the RZ SMARC Carrier Include the gate USB0_VBUSEN state	P62	USB0_EN_OC#
AD5	P4_1/SCIF2_RXD/ MTIOC7B	P4_1	PMOD0 Type-2A on the RZ SMARC Carrier	P113	GPIO5/PWM_OUT#
C14	P40_0/SCIF1_TXD/ GTIOC6A/CAN1_TX/ MTIC5U/SCI0_RXD	SCIF1_TXD CAN1_TX	PMOD1 Type-3A or CAN transceiver ch. 1*2 on the RZ SMARC Carrier*2	P134 P145	SER1_TX CAN1_TX
B15	P40_1/SCIF1_RXD/ GTIOC6B/CAN1_RX/ MTIC5V/SCI0_TXD	SCIF1_TXD CAN1_RX	PMOD1 Type-3A or CAN transceiver ch. 1*2 on the RZ SMARC Carrier*2	P135 P146	SER1_RX CAN1_RX
C15	P40_2/SCIF1_SCK/ CAN1_TX_DATARATE_EN/MTIC5W/SCI0_SCK	P40_2	For selecting the device connected to the SD/MMC ch. 0 interface	—	—
A16	P41_0/SCIF1_CTS/ GTIOC7A/CAN1_RX_DATARATE_EN/GTIOC3A/SCI0_CTS_N_RTS_N	SCIF1_CTS	PMOD1 Type-3A on the RZ SMARC Carrier	P132	SER0_CTS#-
B16	P41_1/SCIF1_RTS/ GTIOC7B/GTIOC3B	SCIF1_RTS	PMOD1 Type-3A on the RZ SMARC Carrier	P131	SER0_RTS#-
AD3	P42_0/USB1_VBUSEN/RSPI2_CK/CAN_CLK/SCIF2_TXD/MTIOC7A	USB1_VBUSEN	USB2.0 Host on the RZ SMARC Carrier Include the gate USB1_OVRCUR state	P67	USB1_EN_OC#
AC3	P42_1/USB1_OVRCUR/RSPI2_MOSI/CAN0_TX/SCIF2_RXD/ MTIOC7B	USB1_OVRCUR	USB2.0 Host on the RZ SMARC Carrier Include the gate USB1_VBUSEN state	P67	USB1_EN_OC#
AE2	P42_2/ADC_TRG/ RSPI2_MISO/CAN0_RX/SCIF2_SCK/ MTIOC7C	P42_2	PMOD1 Type-3A on the RZ SMARC Carrier	P119	GPIO11
Y1	P42_3/RIIC2_SDA/ RSPI2_SSL/CAN0_TX_DATARATE_EN/SCIF2_CTS/MTIOC7D	RIIC2_SDA	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the RZ SMARC Carrier	S49	I2C_GP_DAT
AD1	P42_4/RIIC2_SCL/ CAM_FIELD/CAN0_RX_DATARATE_EN/ SCIF2_RTS	RIIC2_SCL	RAA215300 and 5P35023 PMOD1 Type-6A and audio codec on the RZ SMARC Carrier	S48	I2C_GP_CK
C16	P43_0/RSPI0_CK/ GTIOC4A/GTIOC6A/ IRQ4/MTIOC8A	IRQ4	PMOD0 Type-2A on the RZ SMARC Carrier	P112	GPIO4/ HAD_RST#
A15	P43_1/RSPI0_MOSI/ GTIOC4B/GTIOC6B/ IRQ5/MTIOC8B	P43_1	MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	P110	GPIO2

Table 4.1 List of Pin Function Selections (12/12)

Pin Location	Pin Name	Pin Function	Description	SMARC Pin No.	SMARC Pin Name
A17	P43_2/RSPI0_MISO/ GTIOC5A/IRQ6/MTIO C8C	P43_2	Unused	P108	GPIO0/CA M0_PWR#
B17	P43_3/RSPI0_SSL/ GTIOC5B/IRQ7/MTIO C8D	IRQ7	PMOD1 Type-3A on the RZ SMARC Carrier	P118	GPIO10
B18	P44_0/RSPI1_CK/ SSI1_BCK/CAN1_TX/ MTIOC3A/GTIOC6A	RSPI1_CK CAN_TX	PMOD0 Type-2A or CAN transceiver ch. 1*2 on the RZ SMARC Carrier	P56 P146	SPI1_CK CAN1_TX
C17	P44_1/RSPI1_MOSI/ SSI1_RCK/CAN1_RX /MTIOC3B/GTIOC6B	RSPI1_MOSI CAN1_RX	PMOD0 Type-2A or CAN transceiver ch. 1*2 on the RZ SMARC Carrier	P58 P145	SPI1_DO CAN1_RX
A18	P44_2/RSPI1_MISO/ SSI1_TXD/CAN1_TX _DATARATE_EN/MTI OC3C/GTIOC7A	RSPI1_MISO P44_2	PMOD0 Type-2A or PMOD Type-6A on the RZ SMARC Carrier	P57 P116	SPI1_DIN GPIO8
C18	P44_3/RSPI1_SSL/ SSI1_RXD/CAN1_RX _DATARATE_EN/MTI OC3D/GTIOC7B	RSPI1_SSL P44_3	PMOD0 Type-2A or CAN transceiver ch. 1*2 used as standby input or PMOD Type-6A on the RZ SMARC Carrier	P54 P117	SPI1_CS0# GPIO9
A10	P45_0/SSI0_BCK/ POE0_N/SCI1_RXD	SSI0_BCK	Audio codec or MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S42 S53	I2S0_CK I2S2_CK
C10	P45_1/SSI0_RCK/ POE4_N/SCI1_TXD	SSI0_RCK	Audio codec or MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S39 S50	I2S0_LRCK I2S2_LRCK
B11	P45_2/SSI0_TXD/ POE8_N/SCI1_SCK	SSI0_TXD	Audio codec or MIPI-DSI-to-HDMI transmitter on the RZ SMARC Carrier	S40 S51	I2S0_SDO UT I2S2_SDO UT
A11	P45_3/SSI0_RXD/ POE10_N/SCI1_CTS _N_RTS_N	SSI0_RXD	Audio codec on the RZ SMARC Carrier	S41 S52	I2S0_SDIN I2S2_SDIN
AD4	P5_0/USB0_OVRCU R/SCIF2_SCK/MTIOC 7C/SSI2_BCK	USB0_OVRCUR	USB 2.0 OTG on the RZ SMARC Carrier Include the gate USB0_OVRCUR state	P62	USB0_EN_ OC#
AE3	P5_1/USB0_OTG_ID/ SCIF2_CTS/MTIOC7 D/SSI2_RCK	USB0_OTG_ID	USB 2.0 OTG on the RZ SMARC Carrier USB0_OTG_ID state	P64	USB0_OTG _ID
AE4	P5_2/USB0_OTG_EX ICEN/SCIF2_RTS/ SSI2_DATA	P5_2	24-pin FFC connector on the RZ SMARC Carrier	P111	GPIO3/CA M1_RST#

NOTES

1. This pin is treated as open-circuit in the schematic, but this is incorrect.
2. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
   The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
   S.LOT# in the outer box label: 000251812 or later
   S.LOT# label on the carrier board: 251812 or later

4.2 Memory

QSPI flash memory and DDR4 SDRAM are mounted on the RZ/G2LC SMARC Module as external memory.

Refer to the following for details.

4.2.1 QSPI Flash Memory

Figure 4.1 shows a block diagram of the serial flash memory interface.

The QSPI flash memory is controlled by the SPI multi-I/O bus controller (SPIBSC) of the RZ/G2LC. This flash memory defaults to standard SPI mode and supports both single data rate (SDR) and double data rate (DDR) transfers at clock frequencies of 66 MHz and 50 MHz.

NOTE

For the pull-up resistor of the clock line “RZ_QSPI0_SPCLK”, place it wherever you want.

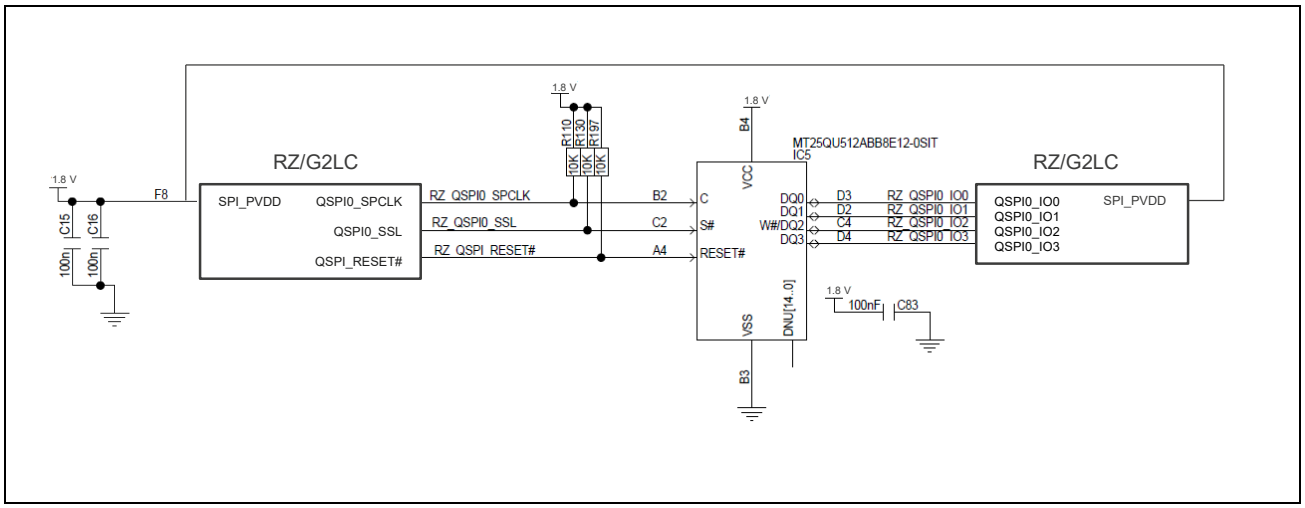


Figure 4.1 Block Diagram of Serial Flash Memory I/F

4.2.2 DDR4 SDRAM

Figure 4.2 shows a block diagram of the DDR4 SDRAM interface.

The DDR4 SDRAM is controlled by the memory controller (MEMC) of the RZ/G2LC. It supports a data bus width of 16 bits, a data transfer rate of 1600 Mbps, and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

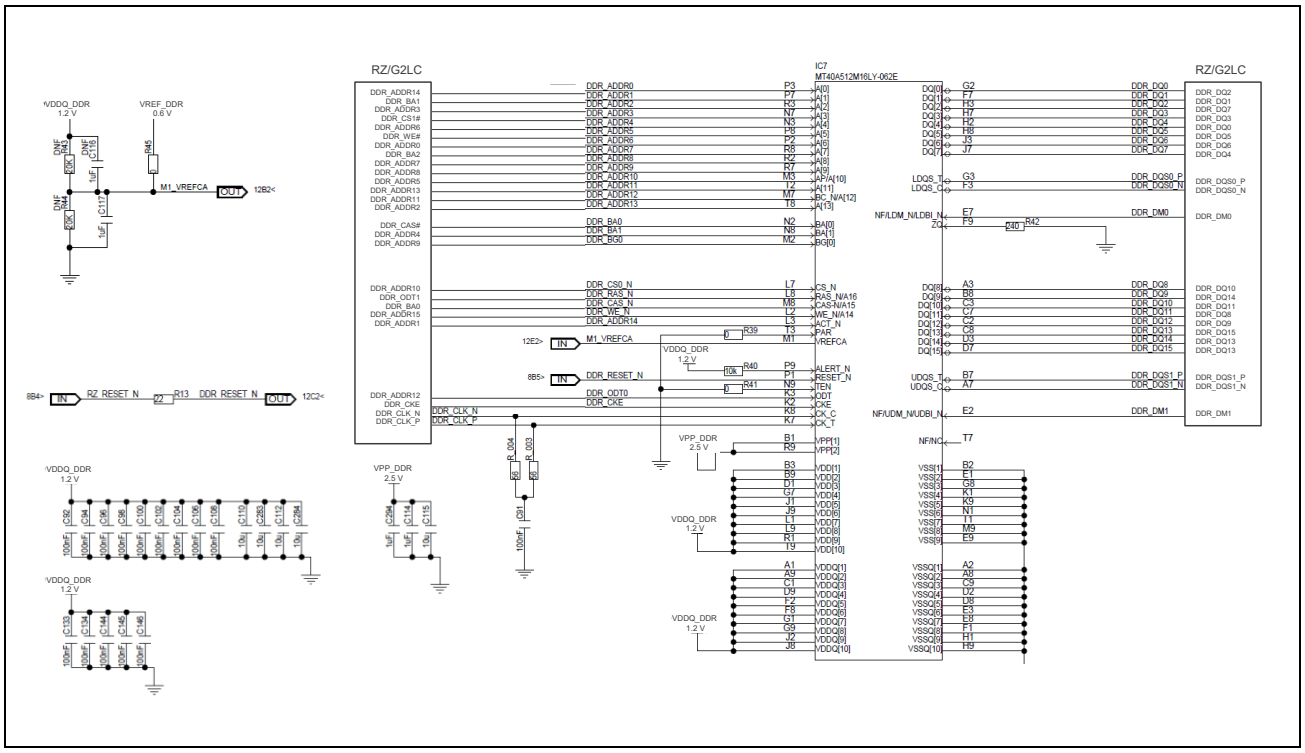


Figure 4.2 Block Diagram of DDR4 SDRAM I/F

4.3 Gigabit Ethernet Interface

Figure 4.3 shows a block diagram of the Gigabit Ethernet interface.

The Gigabit Ethernet interface is controlled by the Ethernet controller (E-MAC) of the RZ/G2LC. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

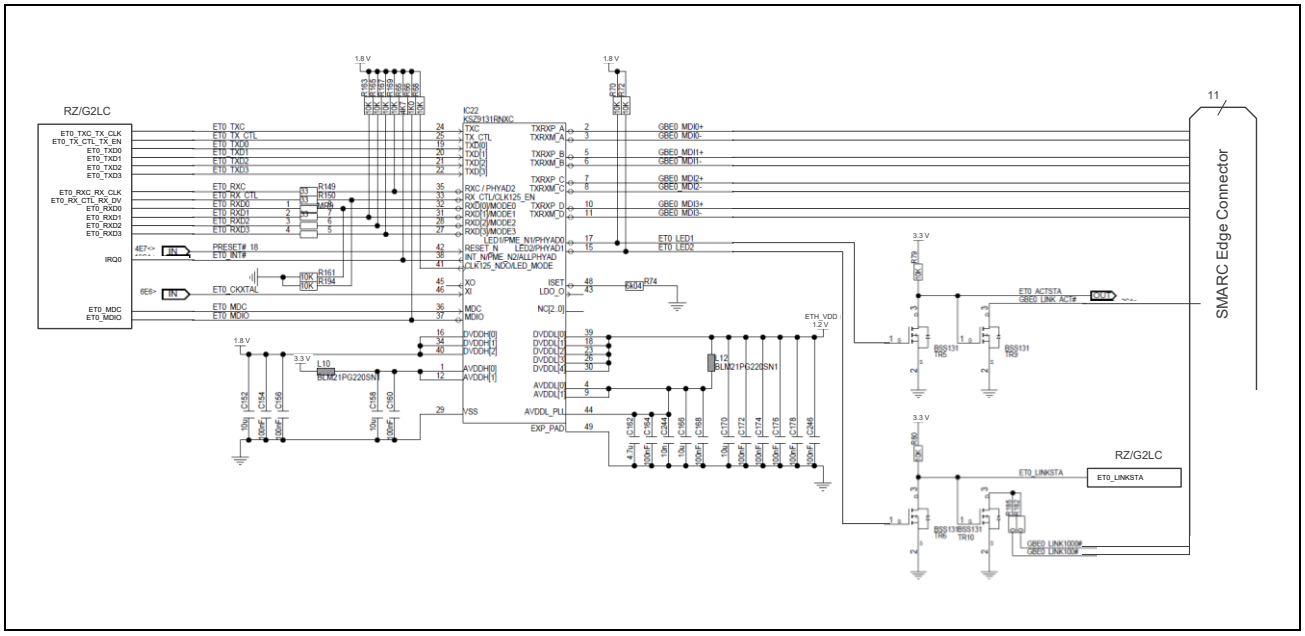


Figure 4.3 Block Diagram of Ethernet I/F

4.4 Clock Configuration

Figure 4.4 shows a block diagram of the clock configuration.

The clock generator (part number 5P35023B-629NLGI) provides the clock required for the RZ/G2LC and peripheral interfaces.

The 5P35023B is a Renesas VersaClock® 3S programmable clock generator that supports 6 unique frequency outputs. The 5P35023B-629NLGI uses a 24-MHz crystal as the reference input and provides one 24-MHz reference clock output for the RZ/G2LC, two 11.2896-MHz LVCMOS clock outputs for the RZ/G2LC and audio codec, one 25-MHz LVCMOS clock output for one Ethernet PHY, and one 12.2880-MHz LVCMOS clock output for the RZ/G2LC.

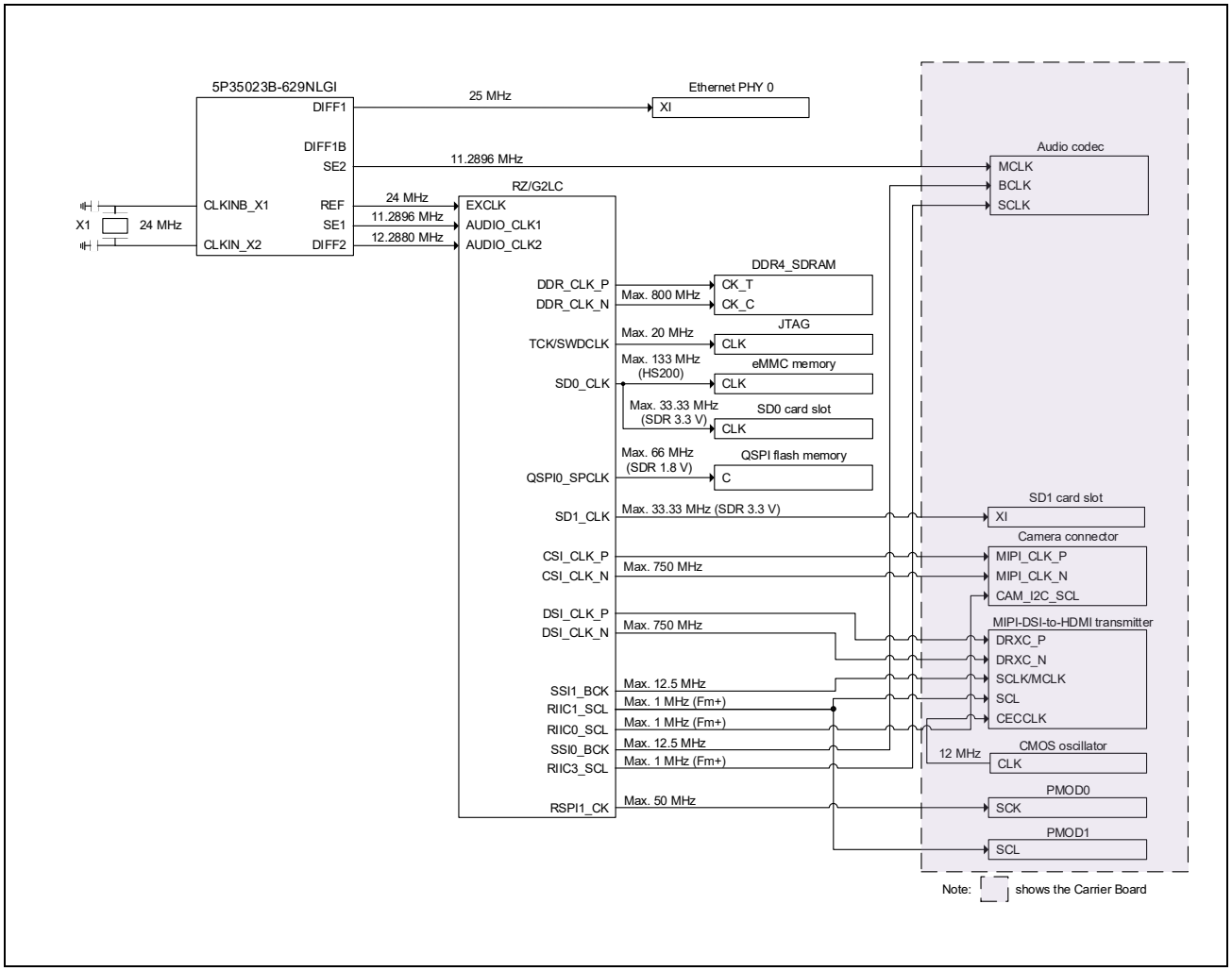


Figure 4.4 Block Diagram of Clock Configuration

4.5 Reset Control

Figure 4.5 shows a block diagram of reset control for the RZ/G2LC EVKIT.

Reset control for the RZ/G2LC and Ethernet PHY is handled by reset signals generated by the PMIC.

The DDR4 SDRAM, QSPI flash memory, and eMMC memory are reset by the RZ/G2LC through software control.

The external emulator can reset the RZ/G2LC via the debug interface.

There are two types of system reset: a power-on reset and a reset by the button switch.

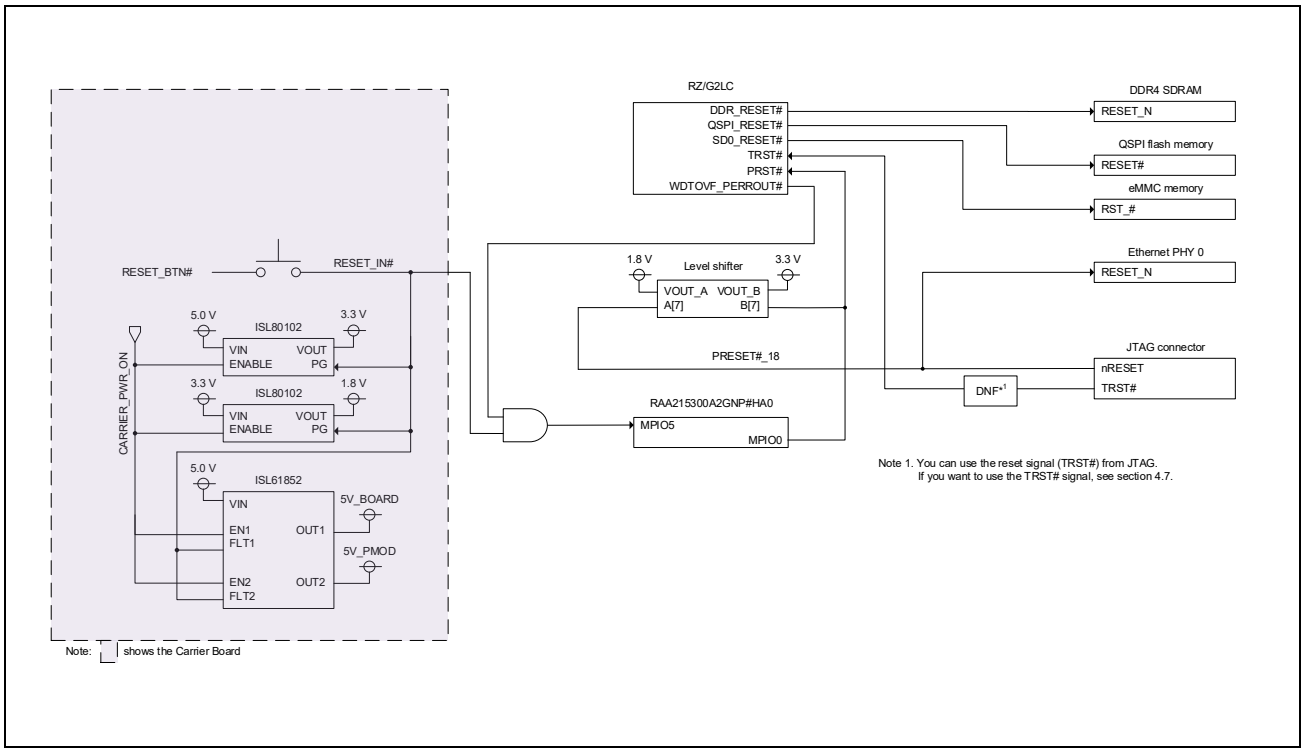


Figure 4.5 Block Diagram of Reset Control

4.6 Power Supply

4.6.1 Power Supply Configuration

Figure 4.6 shows a block diagram of the power configuration for the RZ/G2LC EVKIT.

This board has a USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected between 5 V and 9 V.

The default setting for controlling the input voltage level is 5 V (max. 3 A input) with SW11-4 turned on. When this switch is turned off, the input voltage is 9 V (max. 3 A input). SW11-4 is only turned off when thr RZ/G2LC EVKIT is connected to an external device that requires a lot of power and is expected to run out of power.

The 5-V power supply is supplied to the PMIC mounted on the RZ/G2LC SMARC Module, and the PMIC generates the power supply voltage for each interface.

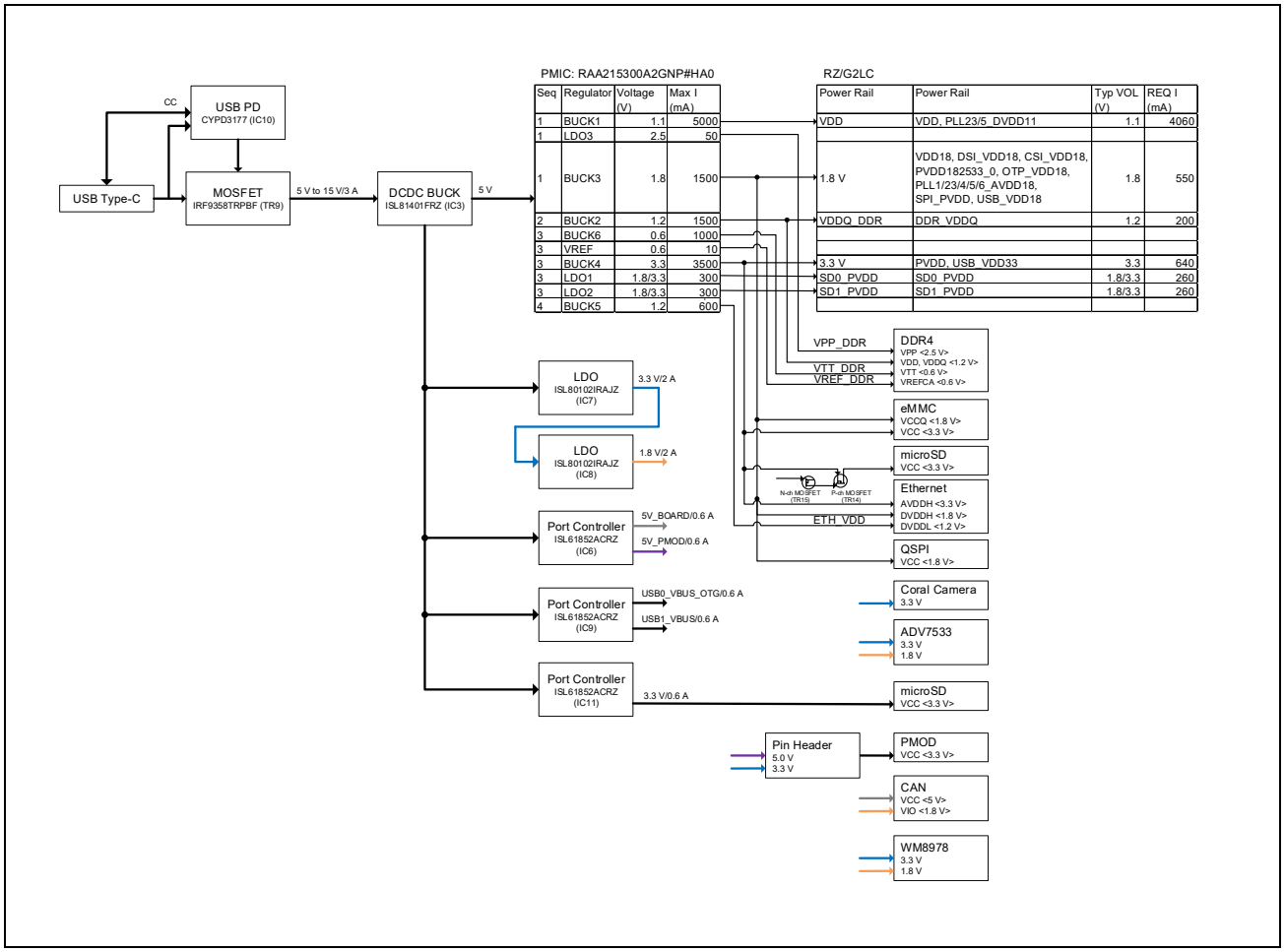


Figure 4.6 RZ/G2LC EVKIT Power Supply

4.6.2 PMIC

Figure 4.7 shows the RZ/G2LC pin assignment for the PMIC.

The RAA215300A2GNP#HA0 is used as the PMIC on the RZ/G2LC EVKIT to supply and manage power for the RZ/G2LC.

It integrates 6 synchronous buck regulators and 3 LDO regulators to support power distribution and power sequencing control required by the RZ/G2LC.

The LDO1 and LDO2 output voltage values are fixed by P39_0 and P39_1.

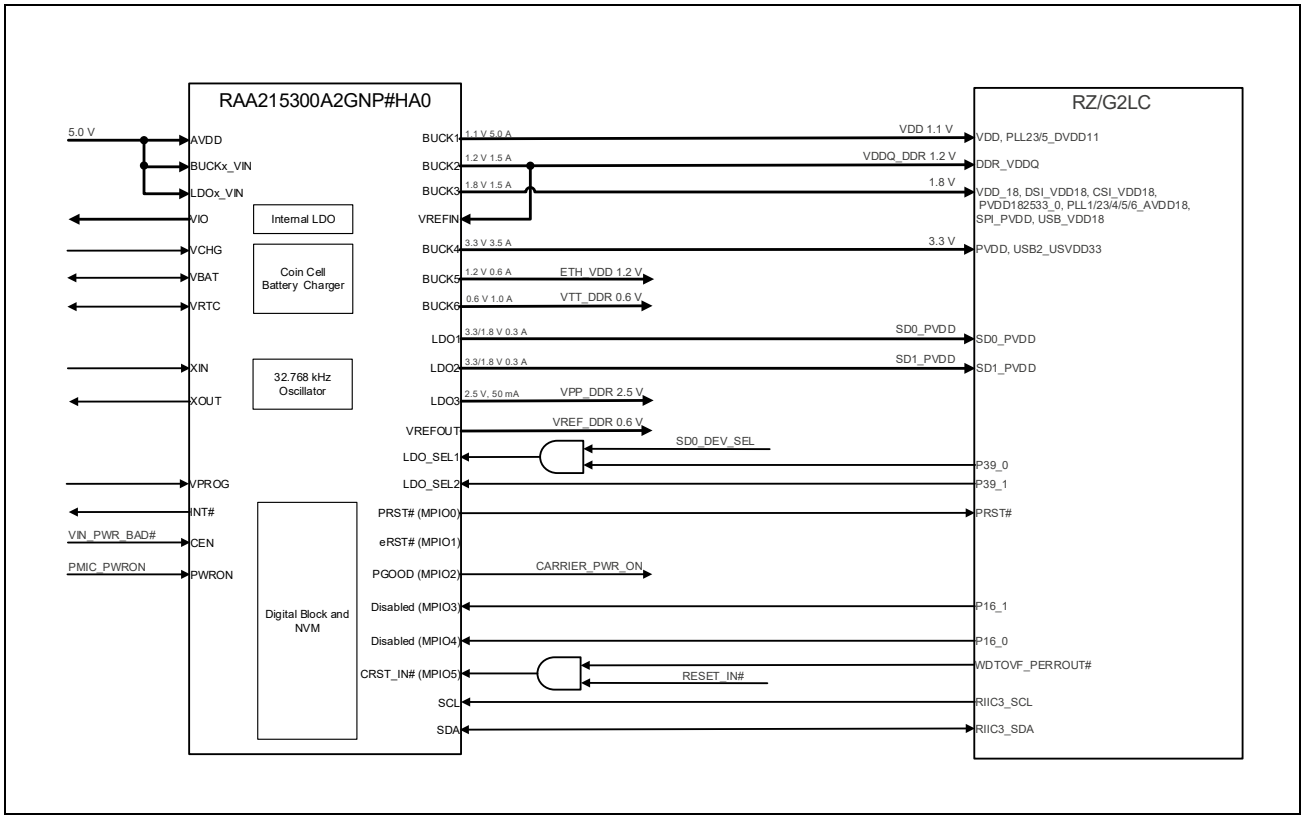


Figure 4.7 Block Diagram around PMIC

4.7 Debug Interface

Figure 4.8 shows a block diagram of the debug interface.

This interface provides supports for debugging and development of the RZ/G2LC.

It allows an external debugger to be connected for debugging operations such as CPU core debugging and register access.

In default operation, pin 9 of the debug interface is used for ground detection. Although with resistor (R20) fitting options, it is possible to use the same pin to independently drive the JTAG_TRST# signal.

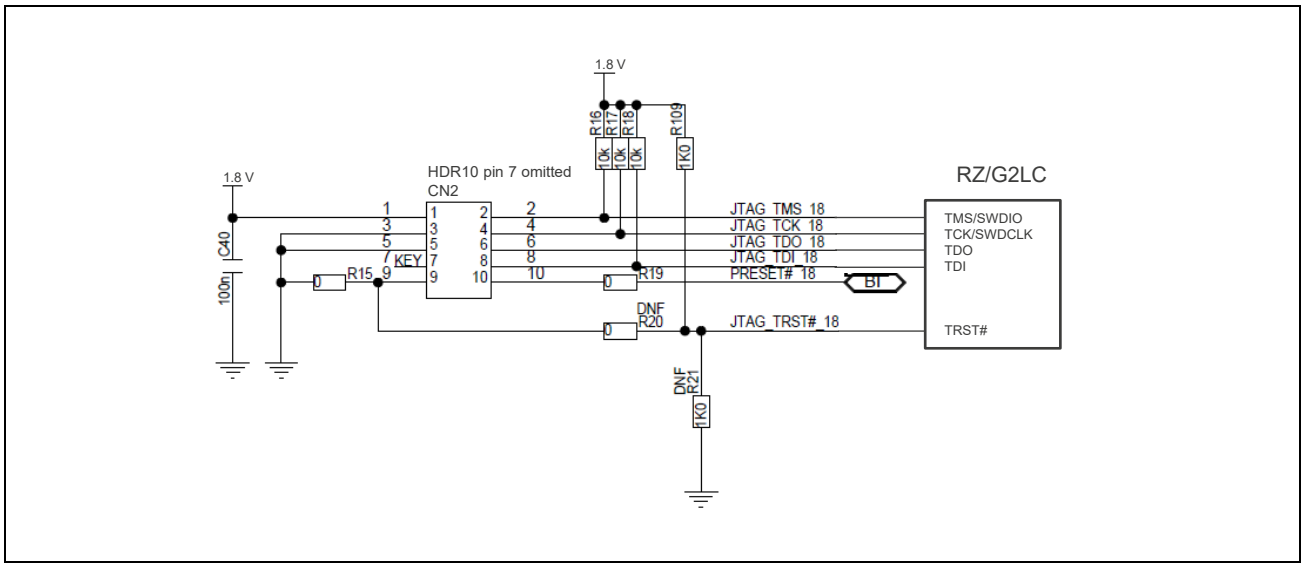


Figure 4.8 Block Diagram of Debug I/F

Table 4.2 Signal Connections of JTAG Connector (CN2)

Pin	Signal Name	MPU
1	1.8 V	—
2	JTAG_TMST_18	TMS/SWDIO
3	VSS	—
4	JTAG_TCK_18	TCK/SWDCLK
5	VSS	—
6	JTAG_TDO_18	TDO
7	—	—
8	JTAG_TDI_18	TDI
9	JTAG_TRST#_18	TRST#
10	PRESET#_18	PRST#

4.8 SD/MMC Interface

4.8.1 eMMC Memory

Figure 4.9 shows a block diagram of the MMC interface.

The eMMC memory is connected to channel 0 of the SD/MMC interface of the RZ/G2LC. This memory is used in conjunction with a microSD card.

The eMMC memory can be used when

- SW_SD0_DEV_SEL is enabled (SW1-2: Selection SD/MMC is OFF).

This interface complies with the JEDEC standard version 4.51 and supports HS200 mode.

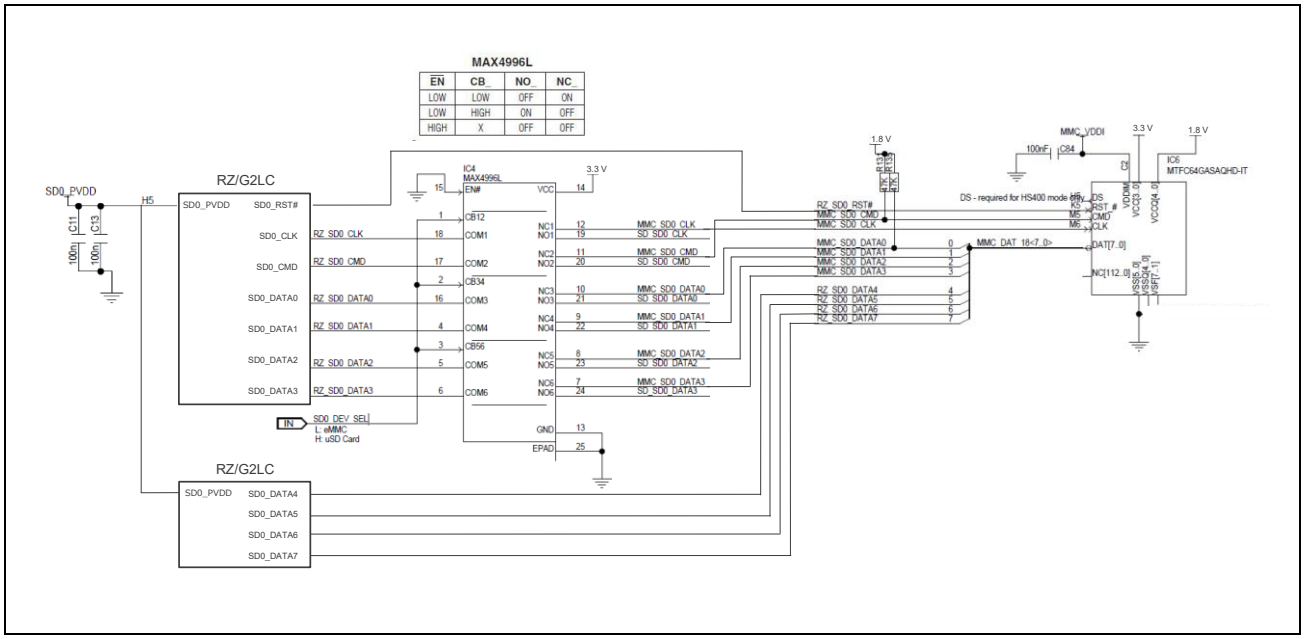


Figure 4.9 Block Diagram of eMMC I/F

4.8.2 microSD Card

Figure 4.10 shows a block diagram of the SDHI interface.

The microSD card is connected to channel 0 of the SD/MMC interface of the RZ/G2LC. This memory card is used in conjunction with eMMC memory.

The microSD card can be used when

- microSD is the selected boot mode*[1] (SW11-1: ON, SW11-2: ON, SW11-3: OFF), and
- SW_SD0_DEV_SEL is disabled (SW1-2: Selection SD/MMC is ON) and eMMC memory is not the selected boot mode (SW11-1: ON, SW11-2: OFF, SW11-3: OFF).

This interface complies with the memory card standard version 3.0 and supports UHS-I modes of 50 MB/s (SDR50) and 104 MB/s (SDR104).

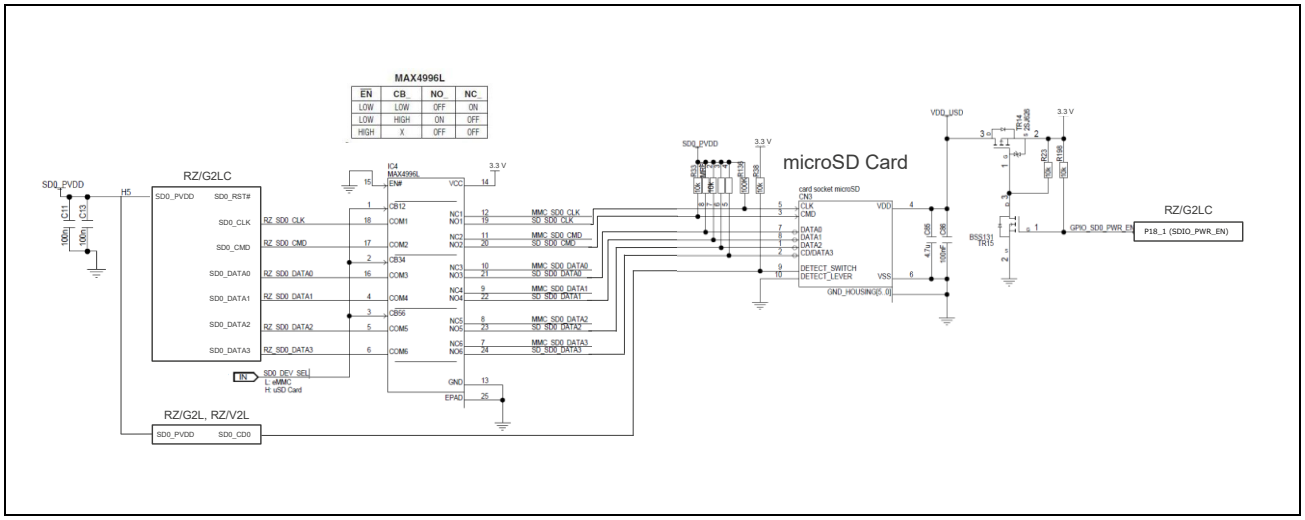


Figure 4.10 Block Diagram of SDHI I/F

Table 4.3 Signal Connections of SD Card Slot (CN4)

Pin	Signal Name	MPU
1	SD_SD0_DATA2	SD0_DATA2
2	SD_SD0_DATA3	SD0_DATA3
3	SD_SD0_CMD	SD0_CMD
4	3.3 V	P4_1 (Power supply control)
5	SD_SD0_CLK	SD0_CLK
6	VSS	—
7	SD_SD0_DATA0	SD0_DATA0
8	SD_SD0_DATA1	SD0_DATA1
9	RZ_SD0_CD	P18_0
10	—	—
—	SD0_PWR_SEL	P39_0 (IO voltage selection of SD0)

Note 1. Due to the circuit specifications, a reboot by pressing the reset button (SW10) is not supported during an eSD boot. In such cases, please use the power switch (SW9) to turn power to the board off and then back on again.

The following is an example of a circuit for executing a reboot during an eSD boot.

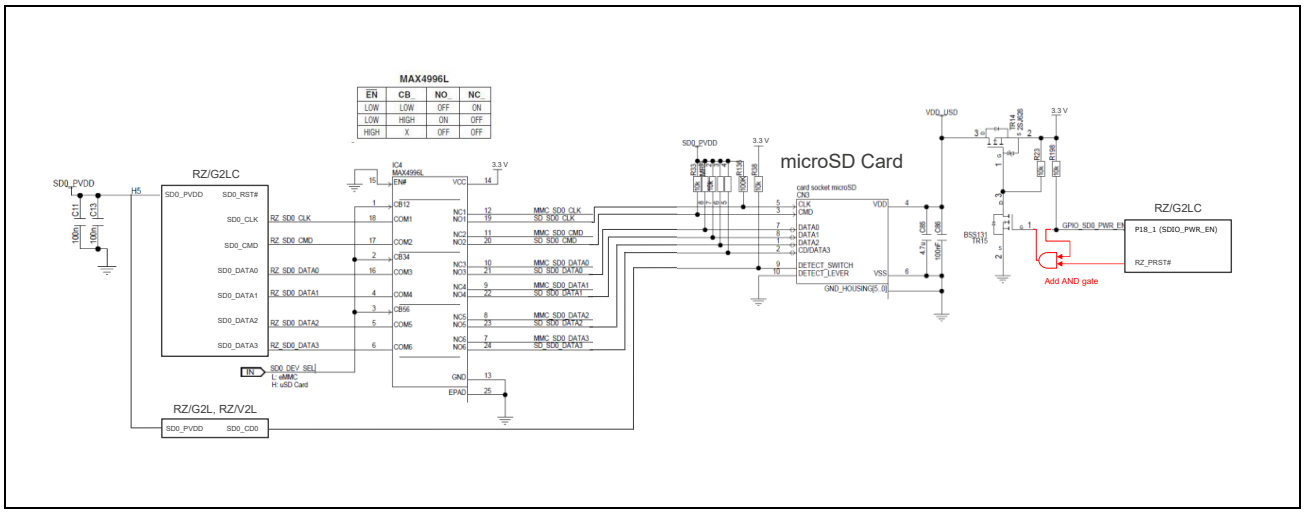


Figure 4.11 Proposed Block Diagram of SDHI I/F

4.9 SMARC Edge Finger

Figure 4.12 illustrates the layout of the edge finger for mating with the SMARC edge connector on the RZ SMARC Carrier.

The SMARC edge connector is a 314-pin, 0.5 mm-pitch, right angle part designed for use with 1.2-mm thick mating PCBs with the edge finger pattern. The SMARC edge connector has a Primary side (Pxx) and a Secondary side (Sxx). The SMARC signal names and edge connector pin numbers are listed in **section 4.1.2, List of RZ/G2LC Pin Functions** along with the G2L port pins (if applicable) and signal names.

For the pin assignment of the SMARC edge connector, please refer to “4 MODULE PIN-OUT MAP” of the document “SMARC module 2.1 Specification”.

Figure 4.12 Layout of Carrier Board Connecting Pins

4.10 Operation Components

4.10.1 Configuration at Shipment

Figure 4.13 illustrates the switch settings at the time of shipment.

Figure 4.13 Switch Settings at Shipment

4.10.2 Configuration by Switches and Mode Terminals

This board is equipped with DIP switches SW1 for selecting the functions. The functions set by the switches are explained below.

Figure 4.14 shows a block diagram around the mode terminals.

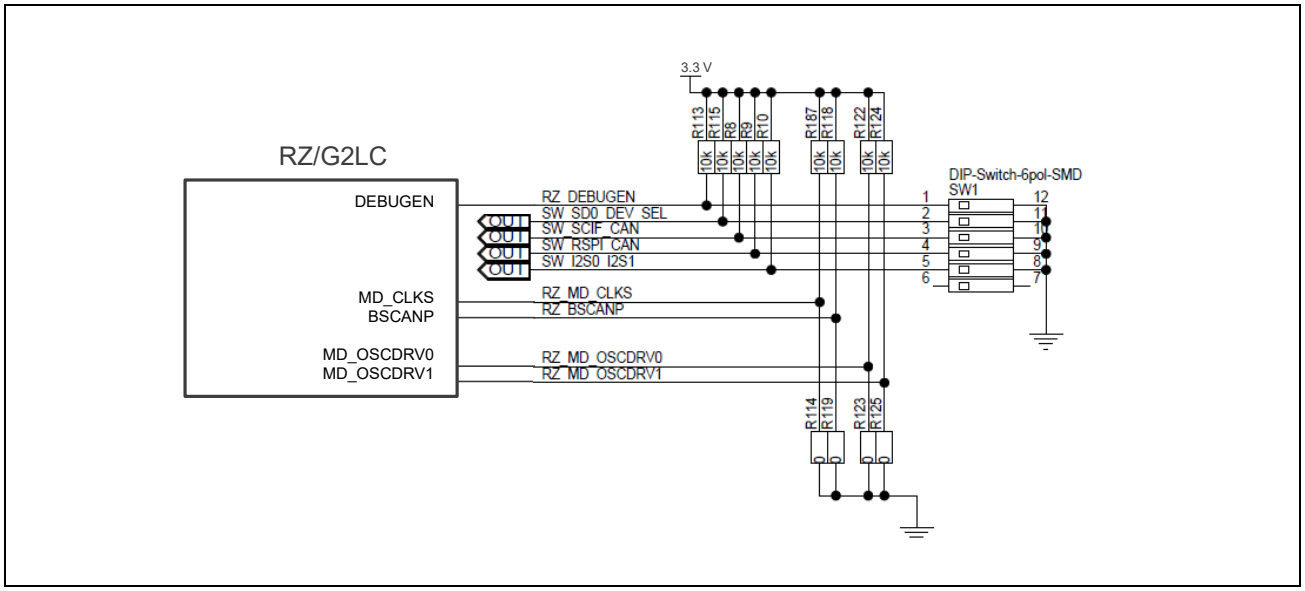


Figure 4.14 Block Diagram of System Setting I/F

Table 4.4 and **Table 4.5** list the functions of SW1 and the mode terminals, respectively. The default settings are highlighted.

Table 4.4 Functions of System Setting Switches (SW1)

No.	Setting		Function
SW1-1 DEBUGEN	OFF	DEBUGEN = “H”	Debugging with ARM debuggers
	ON	DEBUGEN = “L”	Normal operation
SW1-2 Selection of SD or MMC	OFF	Selection = “H”	Select eMMC memory
	ON	Selection = “L”	Select SD card
SW1-3 Selection of SCIF or CAN	OFF	Selection = “H”	Select CAN*1
	ON	Selection = “L”	Select SCIF
SW1-4 Selection of RSPI or CAN	OFF	Selection = “H”	Select CAN*1
	ON	Selection = “L”	Select RSPI
SW1-5 Selection of audio or display	OFF	Selection = “H”	Select display
	ON	Selection = “L”	Select audio

Note 1. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

Table 4.5 Functions of System Settings (Mode Terminals)

No.	Setting		Function
MD_CLKS	0	MD_CLKS = “L”	SSCG OFF
	1	MD_CLKS = “H”	SSCG ON
BSCANP	0	BSCANP = “L”	Normal operation
	1	BSCANP = “H”	Connection test between the LSIs on the customer’s board
MD_OSCDRV0	0	MD_OSCDRV0 = “L”	Adjust the drive capacity of the OSC buffer
	1	MD_OSCDRV0 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)
MD_OSCDRV1	0	MD_OSCDRV1 = “L”	Adjust the drive capacity of the OSC buffer
	1	MD_OSCDRV1 = “H”	Adjust the drive capacity of the OSC buffer (Not supported)

By setting SW1-3 and SW1-4 to the following settings, the RZ/G2LC SMARC Module can be used with various interfaces. **Table 4.6** and **Table 4.7** list the functions set by the combination of the DIP switches.

Table 4.6 GPIO Signals Set by the Combination of SW1-3 and SW1-4

		Setting			
		SW1-3 = "L"	SW1-3 = "L"	SW1-3 = "H"	SW1-3 = "H"
		SW1-4 = "L"	SW1-4 = "H"	SW1-4 = "L"	SW1-4 = "H"
Signal Name	P40_0	SCIF1_TXD	SCIF1_TXD	CAN1_TX*2	CAN1_TX*2
	P40_1	SCIF1_RXD	SCIF1_RXD	CAN1_RX*2	CAN1_RX*2
	P44_0	RSPI1_CK	CAN1_TX*2	RSPI1_CK	RSPI1_CK*1
	P44_1	RSPI1_MOSI	CAN1_RX*2	RSPI1_MOSI	RSPI1_MOSI*1
	P44_2	RSPI1_MISO	GPIO8*2	RSPI1_MISO	RSPI1_MISO*1
	P44_3	RSPI1_SSL	GPIO9*2	RSPI1_SSL	RSPI1_SSL*1

Note 1. IC13 is driven low regardless of the setting of SW1-4.
By removing R11, the setting of SW1-4 can be enabled.

Note 2. The CAN connector is implemented on the RZ SMARC Carrier, but it is not available as a CAN-FD interface because a CAN transceiver is not fitted on this board.
The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is already available.
S.LOT# in the outer box label: 000251812 or later
S.LOT# label on the carrier board: 251812 or later

Table 4.7 GPIO Signals Set by SW1-5

		Setting	
		SW1-5 = "L"	SW1-5 = "H"
Signal Name	SSI0_BCK	I2S0_CK	I2S2_CK
	SSI0_RCK	I2S0_LRCK	I2S2_LRCK
	SSI0_TXD	I2S0_SDOUT	I2S2_SDOUT
	SSI0_RXD	I2S0_SDIN	I2S2_SDIN

5. Appendix

5.1 How to Replace the SMARC Module Board

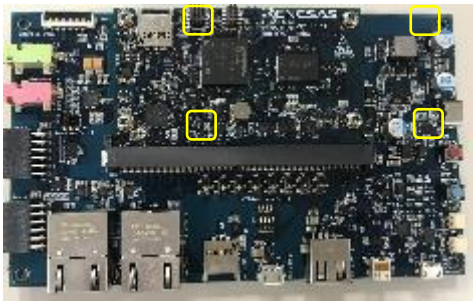
Take care with the following when replacing the board:

1. Remove the four screws.

NOTE

The screw head has a special shape, so be careful not to crush the screw head.

We recommend preparing a torx screwdriver with “T6” head size.



Specially shaped screw head

Figure 5.1 How to Remove the Screws

2. After removing the screws, the SMARC Module Board will stand up at an angle. Slide it out.

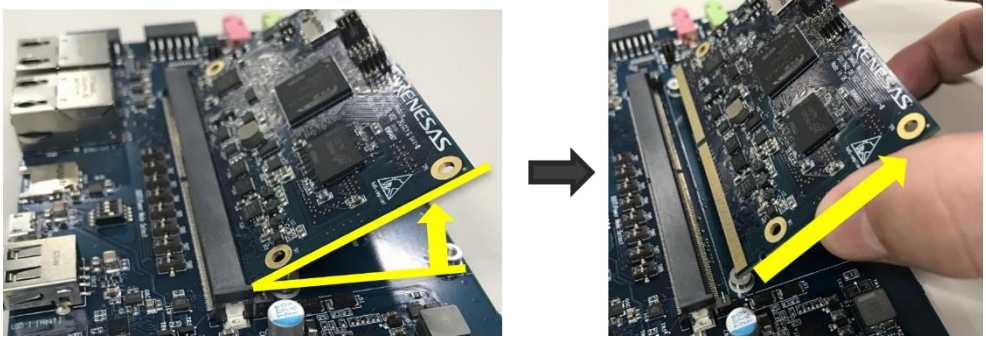


Figure 5.2 How to Remove the SMARC Module Board

3. Insert the replacement SMARC Module Board diagonally, then roll the board until it is parallel to the RZ SMARC Carrier and fix it in place with screws.

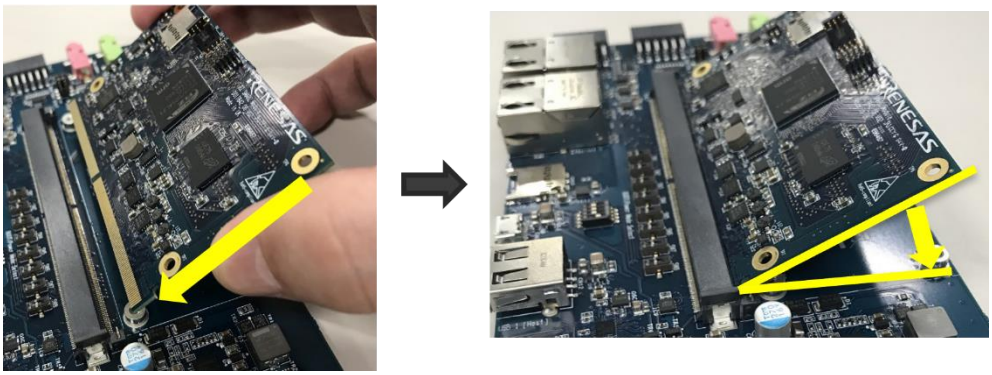


Figure 5.3 How to Install the SMARC Module Board

6. Certifications

The RZ/G2LC SMARC Module Board comprising the RZ/G2LC EVKIT meets the following certification/standards.

6.1 EMC/EMI Standards

- FCC Notice (Class A)

  This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

  [NOTE] — This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

  - Reorient or relocate the receiving antenna.
  - Increase the separation between the equipment and receiver.
  - Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
  - Consult the dealer or an experienced radio/television technician for help.

- Innovation, Science and Economic Development Canada ICES-003 Compliance:
  CAN ICES-3 (A)/NMB-3(A)

- CE Class A (EMC)

  This product is herewith confirmed to comply with the requirements set out in the Council Directives on the Approximation of the laws of the Member States relating to Electromagnetic Compatibility Directive 2014/30/EU.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

- UKCA Class A (EMC)

  This product is in conformity with the following relevant UK Statutory Instrument(s) (and its amendments): 2016 No. 1091 Electromagnetic Compatibility Regulations 2016.

  [Warning] — This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures to correct this interference.

6.2 Material Selection, Waste, Recycling and Disposal Standards

- EU RoHS
- WEEE Directive (2012/19/EU) & The Waste Electrical and Electronic Equipment Regulations 2013

For customers in the UK & European Union the WEEE (Waste Electrical and Electronic Equipment) regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled and disposed of in an environmentally sound manner.

Renesas Electronics Europe GmbH can take back end of life equipment. Register for this service at:
https://www.renesas.com/en/support/regional-customer-support/weee

6.3 Safety Standards

- UL 94V-0

REVISION HISTORY	RZ/G2LC SMARC Module Board User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 27, 2021	—	First edition issued
1.01	Jan. 28, 2022	ALL	A Figure of RTK9744L23C01000BE is changed to RTK9744C22C01000BE.
		—	Section 3.1 is removed.
		51	A setting table of SW1-5 is added.
1.10	Dec. 09, 2022	32 to 34, 51, 52	Restrictions on use are added. When used in combination with the RZ SMARC Series Carrier Board (P/N: RTR97X4XXXB00000BE), CAN1 interface cannot be used because a CAN transceiver is not fitted on the RTK97X4XXXB00000BE.
1.20	Apr. 01, 2024	17 to 28	For section 2.2.2 "List of RZ/G2LC Functions", the pin names, pin functions, and descriptions in the table are modified.
		28, 45, 46	Restrictions on use are modified. The CAN connector is implemented on the RZ SMARC Series Carrier Board (P/N: RTK97X4XXXB00000BE), but the CAN-FD interface cannot be used because a CAN transceiver is not fitted. The following carrier boards are equipped with a CAN transceiver and the CAN-FD interface is available already. S.LOT# in the outer box label: 000251812 or later S.LOT# label on the carrier board: 251812 or later
		31	For section 2.4 "Gigabit Ethernet Interface", the figure is modified.
		33	For section 2.6 "Reset Control", the figure is modified.
		34	For section 2.7 "Power Supply Configuration", the figure is modified.
		36	For section 2.8 "PMIC", the figure is modified.
		37	For section 2.9 "Debug Interface", the figure is modified.
		38	For section 2.10.1 "eMMC Memory", the figure is modified.
1.30	Nov. 27, 2025	49	Section 4 Appendix, added
		50, 51	Section 5 Certifications, added
1.40	Dec. 26, 2025	1	For section 1.1 “Overview”, the description is updated.
		9	For section 1.3 “Features”, table 1.1 “Features of RTK9744C22C01000BE” is updated.
		46	For section 3.2.1 “Functions of Switches and Mode Terminals”, table 3.4 “Functions of System Setting DIP Switches (SW1)” is modified.
2.00	May 27, 2026	All	Restructured the sections of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.
		13	Section 2 “Box Contents”, added
		14	Section 3 “Ordering Information”, added
		38	For section 4.8.2 “microSD Card”, the specification restriction and countermeasure for eSD boot were added.

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