User's Manual

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RZ/A2M SUB Board

RTK79210XXB00000BE

User's Manual

Renesas Microprocessor
RZ Family / RZ/A Series

Renesas Electronics
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The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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How to use this manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the functions and operating specifications of this SUB board. This manual is intended for all users of this SUB board. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product, functional specifications, and operating specifications.

Before using this SUB board, thoroughly understand the notes provided in the text of each section in this manual.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following document applies to the RZ/A2M SUB board RTK79210XXB00000BE.

Document Type	Description	Document Title	Document No.
User manual	Description of functional specifications (mounted devices, memory map, electrical characteristics, etc.) and operating specifications (connectors, switches, etc.)	RZ/A2M SUB Board RTK79210XXB00000BE User's Manual	This user's manual

The following documents apply to the RZ/A2M group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

document Type	Description	Document Title	Document No.
Application note	Application examples, reference programs, etc.	Available from Renesas Electronics Web site.	
RENESAS TECHNICAL UPDATE	Prompt reports on product specifications, documents, etc.		

2. Abbreviations

Abbreviation	Full Form
ACIA	Asynchronous Communications Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connect
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SFR	Special Function Register
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

CONTENTS

1. Overview

1.1 Overview

The RTK79210XXB00000BE is a SUB board for use with the RZ/A2M CPU board. In combination with the RZ/A2M CPU board RTK7921053C00000BE, RZ/A2M functionality and performance can be evaluated, and application software can be developed and evaluated in advance. The RTK79210XXB00000BE has the following features.

- The following external memory is included.
  - SDRAM: 64 MBytes ×1 (16-bit bus connection)
  - EEPROM: 16KBytes × 1
- Includes 50-Pin ML connector for evaluating input/output of digital image signal.
- Includes 1.25 mm pitch connector for evaluating LVDS image output (20-pin x 1, 6-pin x1)
- Includes 26-Pin MIL connector for CMOS camera connection.
- Audio CODEC included for advanced development of audio systems.
- LAN connector included to allow for development and evaluation of Ethernet-compatible software.
- RZ/A2M peripheral feature interface, SD card slot, serial port (USB Micro-B) connector, and USB connector included as standard components.
- USB connector, series A receptacle, and Mini-B receptacle included (cannot be used simultaneously).
- DRP testing 40-pin MIL connector included.

1.2 Configuration

Figure 1.1 shows an example of system configuration using RTK79210XXB00000BE.

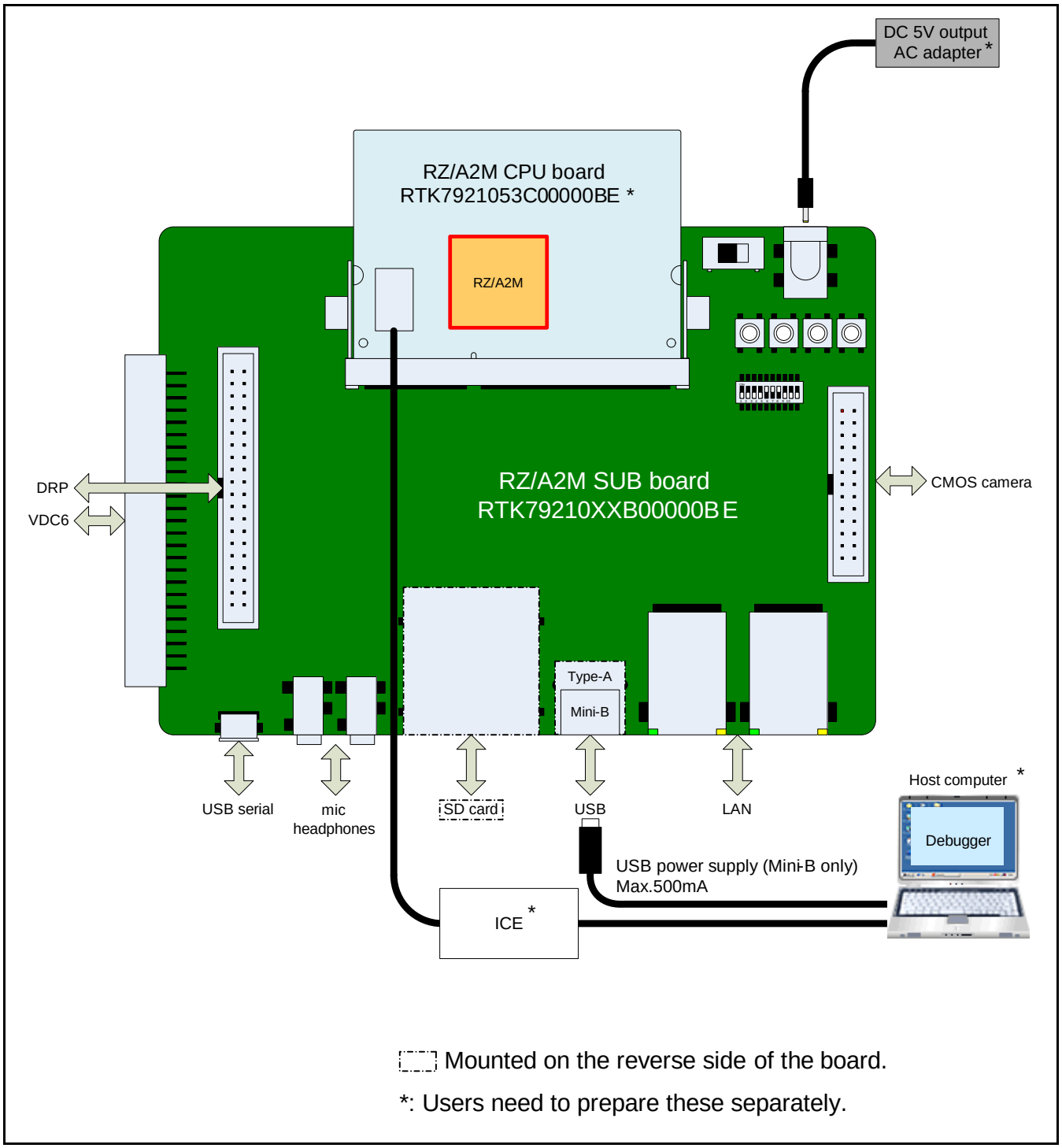

Figure 1.1 RTK79210XXB00000BE System Configuration Example

1.3 Features

Table 1.1 shows an overview of RTK79210XXB00000BE specifications.

Table 1.1 Features of RTK79210XXB00000BE

No.	item	details
1	Memory	● SDRAM: 64 MBytes ×1 - ISSI S42S16320F-7TL ● EEPROM: 16 KBytes ×1 - Renesas R1EX24128ASAS0A ● NAND flash memory: 128 MBytes ×1 is possible to mount on the board pattern. - Cypress S34ML01G100TFI000
2	Connector	● CPU board connector (204-pin): 1 ● DRP connector (40-pin): 1 ● Audio input/output mini jack (3,5 ϕ): 2 ● Serial port connector (USB Micro-B): 1 ● LAN connector (RJ-45): 2 ● SD card slot: 1 ● USB Series A receptacle: 1 ● USB Mini-B receptacle: 1 ● CMOS camera connector: 1 ● RZ/A2M VDC6 digital image signal input/output MIL connector (50-pin): 1 ● RZ/A2M LVDS digital image signal output connector (20-pin): 1 ● RZ/A2M LVDS back light connector (6-pin): 1 ● DC power jack: 1
3	Switch	● Power switch: 1 ● User switch: 2 (NMI, IRQ0) ● Key input switch: 2 ● DIP switch: 1 (I/F settings)
4	Outer dimensions/layered configuration	● Dimensions: 105 x 148mm ● Implementation: 4 level dual surface, board thickness: 1.6mm ● Circuit board configuration: Single board

1.4 Outside View

Figure 1.2 shows the outside view of RTK79210XXB00000BE.

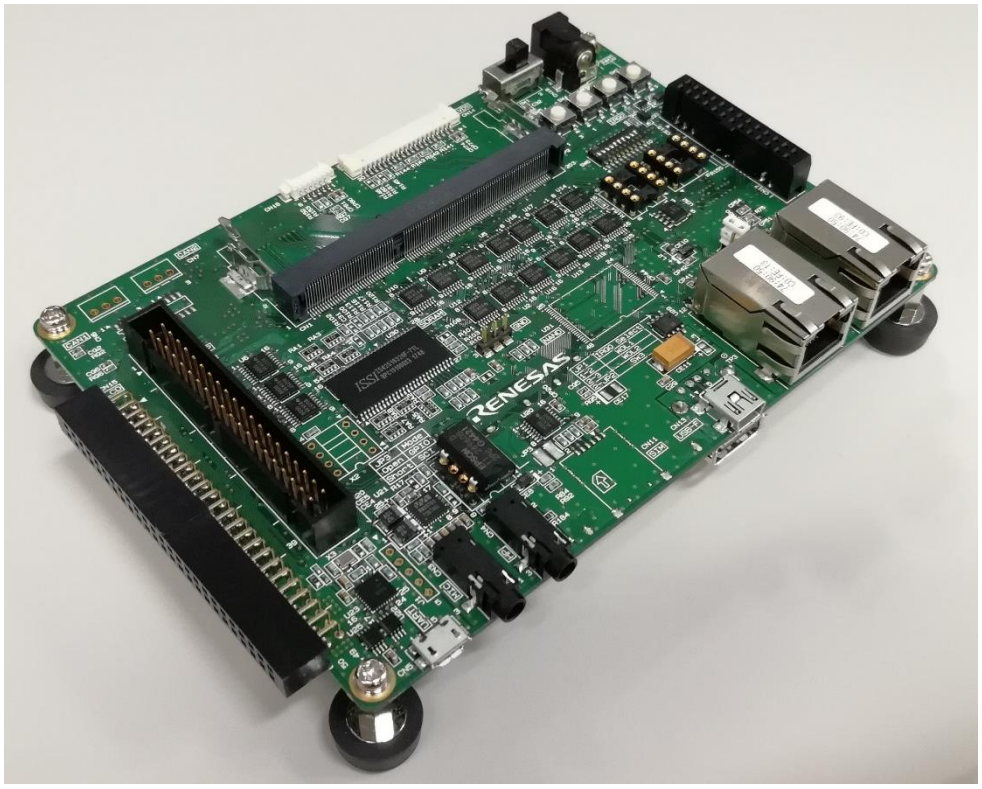

Figure 1.2 RTK79210XXB00000BE Outside View

1.5 Block Diagram

Figure 1.3 RTK79210XXB00000BE block diagram.

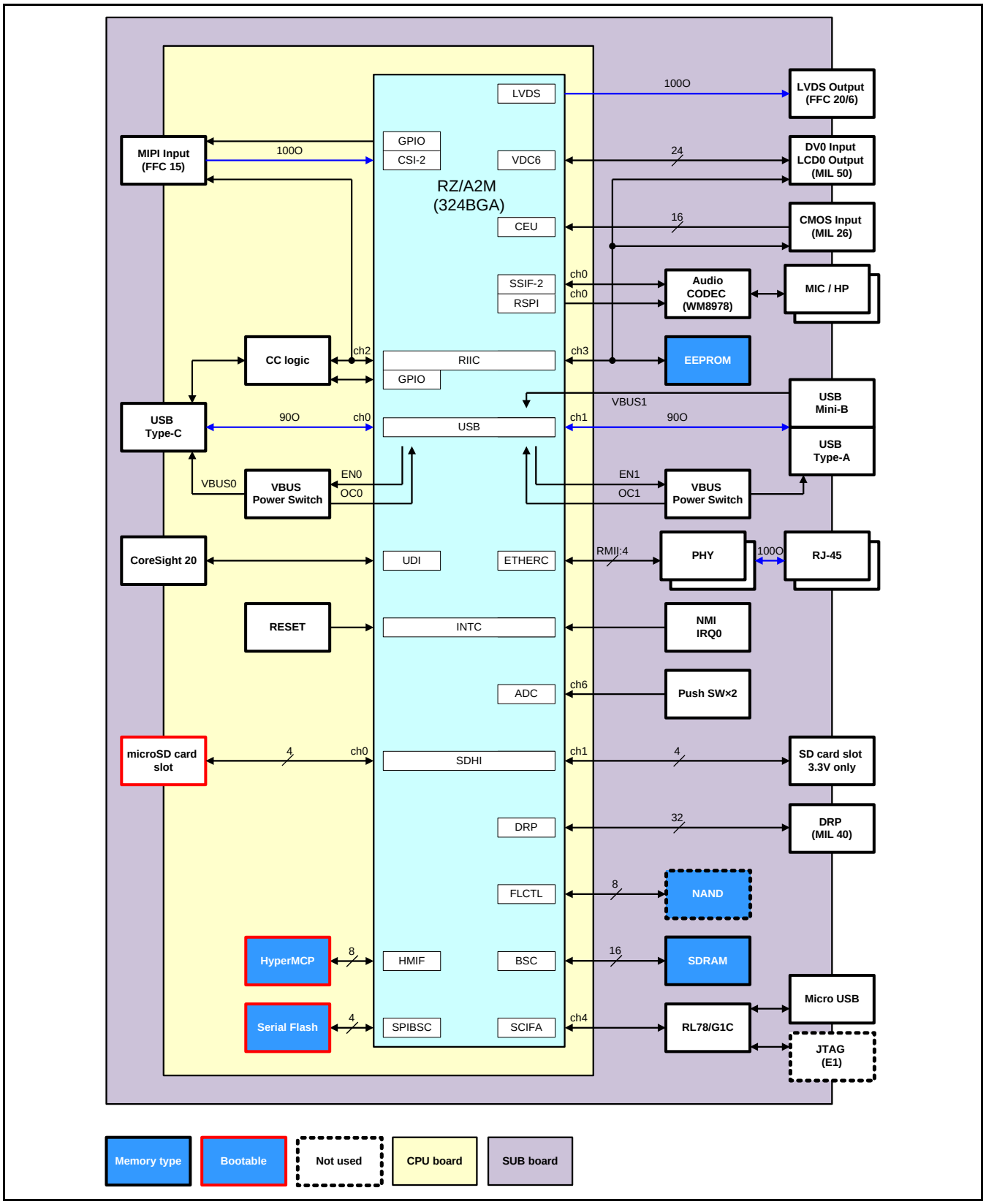

Figure 1.3 Block Diagram of RTK79210XXB00000BE

1.6 Layout of Components

Figure 1.4 - Figure 1.5 show the layout of RTK79210XXB00000BE main components.

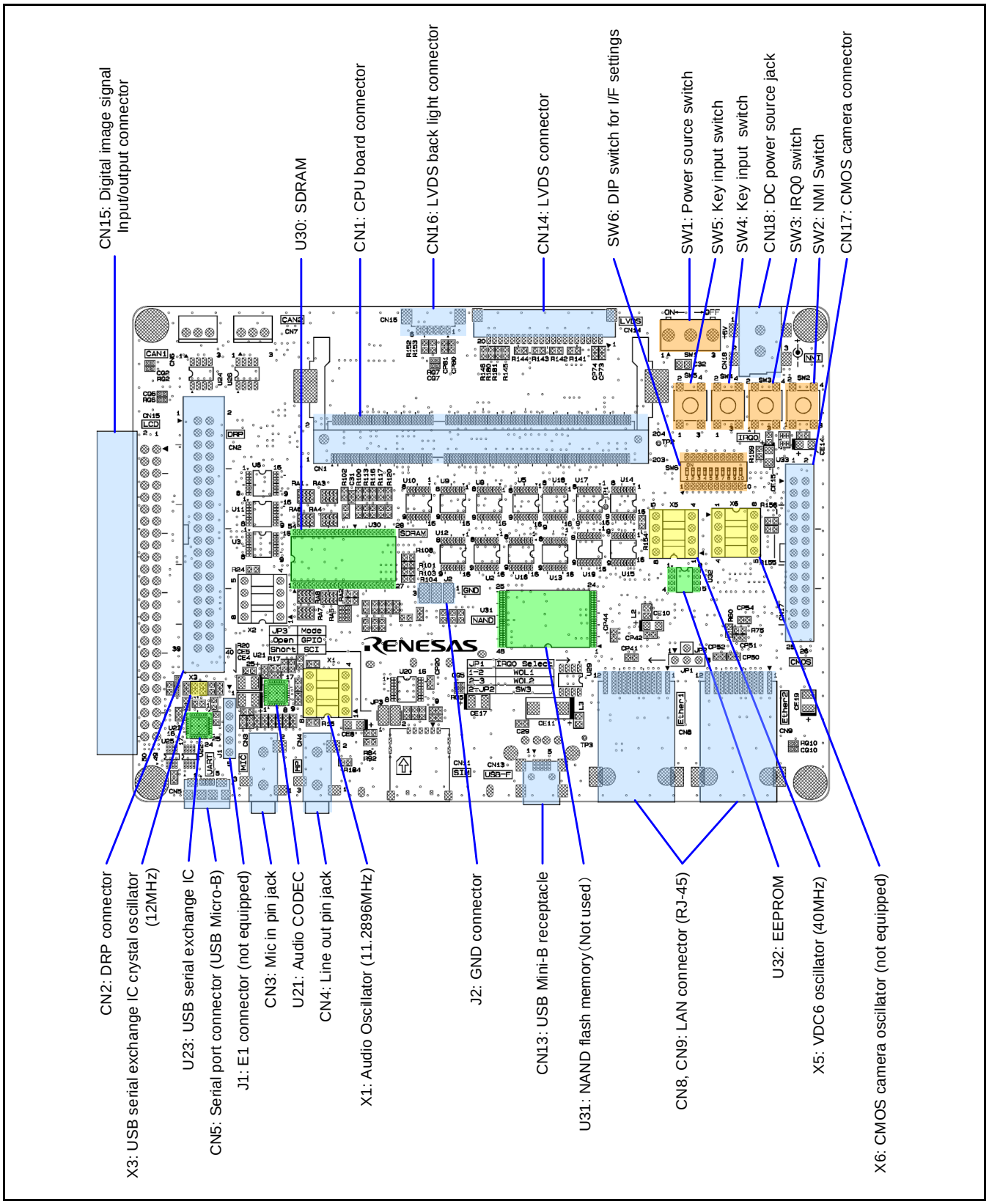

Figure 1.4 RTK79210XXB00000BE Layout of Components (C Side Top View)

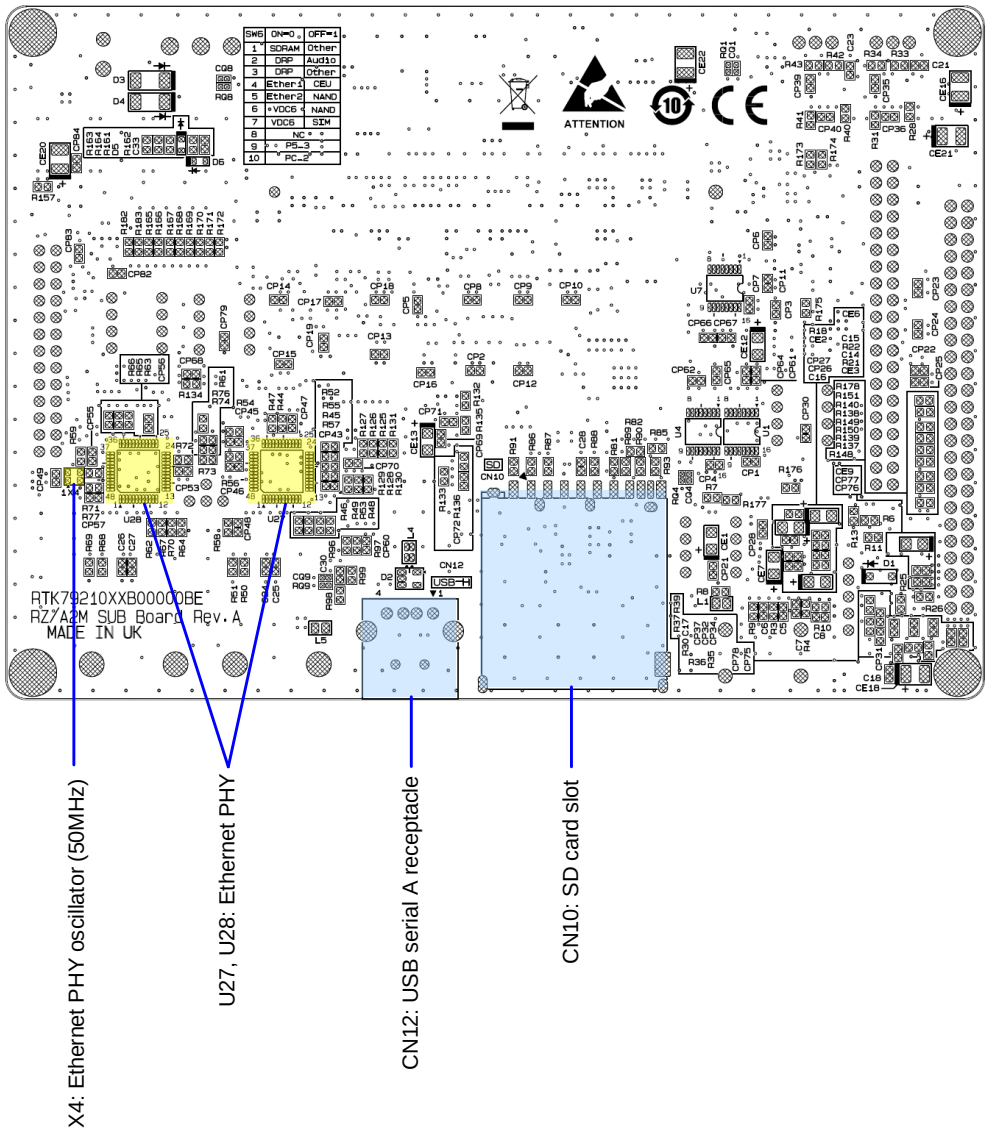

Figure 1.5 RTK79210XXB00000BE Layout of Components (S Side Top View)

Table 1.2 - Table 1.3 list the main components mounted on the RTK79210XXB00000BE.

Table 1.2 Main Components on RTK79210XXB00000BE (1) IC

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Components
U21	Audio CODEC	WM8978CGEFL/V (Cirrus)	
U23	USB serial converter IC	R5F10JBCANA#U0 (Renesas)	
U27, U28	Ethernet PHY	RTL8201FL-VB-CG (Realtek)	
U30	SDRAM	IS42S16320F-7TL (ISSI)	
U31	NAND flash memory	Not used	S34ML01G100TFI000 (Cypress)
U32	EEPROM	R1EX24128ASAS0A (Renesas)	
X1	Audio oscillator	SG-8002DC_11.2896MHz_PCB (EPSON)	11.2896MHz
X3	USB serial converter IC crystal oscillator	CX2520DB12000D0PPSC1 (Kyocera)	12MHz
X4	Ethernet PHY oscillator	KC2016K50.0000C1GE00 (Kyocera)	50MHz
X5	VDC6 oscillator	SG-8002DC_40MHz_PCB (EPSON)	40MHz
X6	CMOS camera oscillator	Not used	SG-8002DC (EPSON)

Table 1.3 Main Components mounted on RTK79210XXB00000BE (2) Connector

Component Number	Component Name	Type (Manufacturer)	Recommended Optional Components
CN1	CPU board connector (SODIMM 204-pin)	2013297-1 (TE)	
CN2	DRP connector	HIF3FC-40PA-2.54DSA (71) (HRS)	
CN3	Mic in pin jack	STX-3500-3NTR (Kycon)	
CN4	Line out pin jack	STX-3500-3NTR (Kycon)	
CN5	Serial port connector	ZX62-B-5PA (33) (HRS)	USB Micro-B
CN8, CN9	LAN connector (RJ-45)	J3011G21DNL (Pulse)	
CN10	SD card slot	DM1B-DSF-PEJ (82) (HRS)	
CN12	USB serial A receptacle	UBA-R4R-D14-4D (LF) (SN) (JST)	
CN13	USB Mini-B receptacle	KMBX-SMT-5S-S-30TR (Kycon)	
CN14	LVDS connector	DF14A-20P-1.25H (25) (HRS)	
CN15	Digital image input/output signal connector (50-pin)	SFH11-PBPC-D25-RA-BK (SULLINS)	
CN16	LVDS back light connector	53261-0671 (Molex)	
CN17	CMOS camera connector (26-pin)	HIF3FB-26DA-2.54DSA (71) (HRS)	
CN18	DC power source jack	KLDX-SMT2-0202-ATR (Kycon)	
J1	E1 connector	Not used	WM-6-5P (MAC8)
J2	GND connector	HWP-3P-G (MAC8)	

1.7 Memory Mapping

Figure 1.6 shows the RZ/A2M memory mapping of RTK79210XXB00000BE.

Logic address	RZ/A2M logic space	RTK79210XXB00000BE Memory mapping
H'0000 0000	CS0 space: 64 MBybes	-
H'0400 0000	CS1 space: 64 MBytes	-
H'0800 0000	CS2 space: 64 MBytes	-
H'0C00 0000	CS3 space: 64 MBytes	SDRAM (64 MBytes)
H'1000 0000	CS4 space: 64 MBytes	-
H'1400 0000	CS5 space: 64 MBytes	-
H'1800 0000	Other: 128 MBytes	Other: 128 MBytes
H'2000 0000	SPI multi I/O bus space: 256 MBytes	Serial flash memory (64 MBytes)
H’2400 0000		-
H'3000 0000	HyperFlash space: 256 MBytes	HyperFlash (64 MBytes)
H’3400 0000		-
H'4000 0000	HyperRAM space: 256 MBytes	HyperRAM (8 MBytes)
H’4080 0000		-
H'5000 0000	OctaFlash space: 256 MBytes	-
H'6000 0000	OctaRAM space: 256 MBytes	-
H'7000 0000	Reserved (cannot be used)	Reserve(cannot be used)
H'8000 0000	Large-capacity internal RAM: 4 MBytes	Large-capacity internal RAM: 4 MBytes
H'8040 0000	Other: 2044 MBytes	Other: 2044 MBytes
H'FFFF FFFF		

Figure 1.6 RZ/A2M Memory Mapping

1.8 Absolute Maximum Ratings

Table 1.4 lists absolute maximum ratings for RTK79210XXB00000BE.

Table 1.4 RTK79210XXB00000BE Absolute Maximum Ratings

Symbol	Item	Rating value	Note
D5V	5V power voltage	-0.3V to 6.25V	Vss is the reference.
D3.3V *1	3.3V power voltage	-0.3V to 4.2V	Vss is the reference.
AVcc *1	Analog 3.3V main power voltage	-0.3V to 4.2V	AVss is the reference.
T_{opr}	Operational temperature range*2	0℃ to 50℃	No condensation formation, corrosive gas environments not permitted
T_{stg}	Storage temperature *2	-10℃ to 60℃	No condensation formation, corrosive gas environments not permitted

[Note] *1 Supplied from the connected RZ/A2M CPU board.

*2 Ambient temperature is the air temperature at a position as close as possible to the board.

1.9 Operating Conditions

Table 1.5 - lists operating conditions of RTK79210XXB00000BE.

Table 1.5 RTK79210XXB00000BE - Operational Conditions

Symbol	Item	Rated Value	Note
D5V	5V power voltage	4.75V to 5.25V	Vss standard
D3.3V *1	3.3V power voltage	3.0V to 3.6V	Vss standard
AVcc *1	Analog 3.3V main power voltage	3.0V to 3.6V	AVss standard
―	Maximum consumed current	2A	Includes continuous RZ/A2M CPU board current consumption.
T_{opr}	Operational temperature range*2	0℃ to 40℃	Do not expose to condensation or corrosive gases

[Note] *1 Supplied from the connected RZ/A2M CPU board.

*2 Ambient temperature is the air temperature at a position as close as possible to the board.

2. Functional Specifications

2.1 Overview of Functions

Table 2.1.1 lists function modules of RTK79210XXB00000BE.

Table 2.1.1 Function Modules of RTK79210XXB00000BE

Section	Function	Description
2.2	CPU	● RZ/A2M pin functions used in the RTK79210XXB00000BE.
2.3	Memory	● SDRAM: 64 Mbytes x 1 - ISSI S42S16320F-7TL ● EEPROM: 16 KBytes x 1 - Renesas R1EX24128ASAS0A ● NAND flash memory: 128 MBytes x 1 is possible to mount on the board pattern. - Cypress S34ML01G100TFI000
2.4	USB interface	Connection for the RZ/A2M USB2.0 host/function module and USB connector
2.5	Serial interface	Connection for the RZ/A2M FIFO internal serial communication interface (SCIFA) and RL78-intermediate USB Micro-B connector
2.6	Interrupt switch	Connection for the RZ/A2M NMI pin, IRQ0 pin, and push switch
2.7	Clock configuration	System clock configuration
2.8	Reset control	Reset control for the RZ/A2M CPU board and devices installed on the RTK79210XXB00000BE
2.9	Power voltage configuration	System power supply configuration for the RZ/A2M CPU board and RTK79210XXB00000BE
2.10	Audio interface	Connection for the RZ/A2M Audio CODEC (WM8978)
2.11	CMOS camera interface	Connection for the RZ/A2M Capture engine unit (CEU) and the CMOS camera connector
2.12	SD card interface	Connection for the RZ/A2M SD host interface (SDHI) channel 1 and SD card slot
2.13	LAN interface	Connection for the RZ/A2M Ethernet controller (ETHERC) and LAN connector via Ethernet PHY
2.14	Key input switch	Connection for the RZ/A2M A/D converter (ADC) and push switches
2.15	VDC6 interface	Connection for the RZ/A2M Video display controller 6 (VDC6) and digital image input/output connector
2.16	LVDS interface	Connection for the RZ/A2M LVDS interface and LVDS connector
2.17	DRP interface	Connection for the RZ/A2M DRP interface and DRP connector
—	Operation specifications	Refer to Chapter 3 for details on connectors and interfaces

2.2 CPU

2.2.1 Overview of RZ/A2M

RTK79210XXB00000BE is used by connecting to an RZ/A2M CPU board RTK7921053C00000BE equipped with RZ/A2M.

RZ/A2M is a 32 bit RISC microprocessor which operates at a maximum clock speed of 528 MHz.

2.2.2 List of RZ/A2M Pin Functions Used on RTK79210XXB00000BE

Table 2.2.1 to Table 2.2.16 lists RZ/A2M Pin Functions used on RTK79210XXB00000BE

Table 2.2.1 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (1)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
A1	Vcc				
A2	QSPI1_IO3		Connects to serial flash memory (U2 on the CPU board)	—	
A3	QSPI1_SPCLK		Connects to serial flash memory (U2 on the CPU board)	—	
A4	RPC_WP#		Open	—	
A5	QSPI0_IO3		Connects to serial flash memory (U2 on the CPU board)	—	
A6	PVcc_SPI				3.3V
A7	Vss				
A8	PVcc				
A9	PF_4 / RxD2 / DV0_DATA19 / LCD0_DATA4 / MTIOC6A / SSIBCK0 / IRQ1	DV0_DATA19 LCD0_DATA4	Connects to digital image input/output connector (CN15)	113	
A10	PE_6 / ET0_MDIO / VIO_D2 / SSIRxD0 / MTIOC0D / CC2_RD1	ET0_MDIO	Connects to Ethernet PHY1 (U27)	107	SW6-4 : ON
		VIO_D2	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
A11	PL_2 / MD_BOOT2 / IRQ6	MD_BOOT2	Connects to DIP switch (SW1 on the CPU board)	—	PD_0 : High SW1-3
		IRQ6	Connects to USB CC logic controller (U7 on CPU the board)		PD_0 : Low
A12	PE_5 / ET0_MDC / VIO_D3 / SSITxD0 / MTIOC0C / CC1_RD1	ET0_MDC	Connects to Ethernet PHY1 (U27)	103	SW6-4 : ON
		VIO_D3	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
A13	P8_4 / A4 / DRP20 / DV0_DATA13 / SSL00 / SSIRxD3	A4	Connects to SDRAM (U3)	101	SW6-1 : ON
		DRP20	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-2 : ON
		SSL00	Connects to Audio CODEC (U21)		SW6-1 : OFF SW6-2 : OFF
A14	P8_6 / A6 / DRP18 / DV0_DATA11 / MOSI0 / SSIFS3	A6	Connects to SDRAM (U3)	95	SW6-1 : ON
		DRP18	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-2 : ON
		MOSI0	Connects to Audio CODEC (U21)		SW6-1 : OFF SW6-2 : OFF

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

Red text CPU board setting display.

Table 2.2.2 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (2)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
A15	PE_4 / ET0_CRS/RMII0_CRSDV / VIO_D4 / SSIFS0 / MTIOC0B	ET0_CRS/RMII0_CRSDV	Connects to Ethernet PHY1 (U27)	91	SW6-4 : ON
		VIO_D4	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
A16	P9_1 / A9 / DRP15 / DV0_DATA8 / RxD4 / SSIFS2	A9	Connects to SDRAM (U3) connection	83	SW6-1 : ON
		DRP15	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-3 : ON
		RxD4	Connects to USB Micro-B port (CN5) via USB serial converter IC (U23)		SW6-1 : OFF SW6-3 : OFF
A17	PVcc				
A18	Vss				
A19	PE_1 / ET0_RXD0/RMII0_RXD0 / VIO_D7 / RxD2 / POE8 / VBUSIN1 / IRQ1	ET0_RXD0/RMII0_RXD0	Connects to Ethernet PHY1 (U27)	73	SW6-4 : ON
		VIO_D7	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
A20	PA_4 / A20 / DV0_DATA9 / LCD0_DATA14 / SCI_TXD0 / MTIOC0C	DV0_DATA9	Connects to digital image input/output connector (CN15)	69	SW6-7 : ON
		LCD0_DATA14			
A21	CKIO		Connects to SDRAM (U3)	54	
A22	Vss				
B1	PK_1 / ET1_TXD0/RMII1_TXD0 / NAF4 / CC1_RA0 / CAN_CLK / SSIDATA2	ET1_TXD0/RMII1_TXD0	Connects to Ethernet PHY2 (U28)	137	SW6-5 : ON
		NAF4	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
B2	Vcc				
B3	QSPI1_IO1		Connects to serial flash memory (U2 on the CPU board)	—	
B4	QSPI1_IO0		Connects to serial flash memory (U2 on the CPU board)	—	
B5	RPC_RESET#		Connects to serial flash memory (U2 on the CPU board)	—	
B6	QSPI0_IO1		Connects to serial flash memory (U2 on the CPU board)	—	
B7	QSPI0_SPCLK		Connects to serial flash memory (U2 on the CPU board)	—	
B8	PF_5 / TxD2 / DV0_DATA20 / LCD0_DATA3 / MTIOC6B / SSIFS0	DV0_DATA20	Connects to digital image input/output connector (CN15)	115	
		LCD0_DATA3			
B9	P6_3 / ET0_TXD1/RMII0_TXD1 / VIO_HD / TxD3 / POE0	ET0_TXD1/RMII0_TXD1	Connects to Ethernet PHY1 (U27)	111	SW6-4 : ON
		VIO_HD	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
B10	PH_0 / AUDIO_CLK / VIO_D1 / GTIOC4A / MTIOC1A / CC1_RD0 / IRQ3	VIO_D1	Connects to CMOS camera connector (CN17)	105	
B11	PL_3 / MD_BOOT1 / IRQ7	MD_BOOT1	Connects to DIP switch (SW1 on the CPU board)	—	PD_0 : High SW1-4
		IRQ7	Connects to USB CC logic controller (U7 on the CPU board)		PD_0 : Low

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.3 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (3)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
B12	PL_1 / MD_CLK / IRQ5	MD_CLK	Connects to DIP switch (SW1 on the CPU board)	48	PD_0 : High SW1-2
		IRQ5	Connects to Ethernet PHY2 (U28)		PD_0 : Low SW6-5 : ON
B13	P8_3 / A3 / DRP21 / DV0_DATA14 / MTIOC6A / GTIOC3A	A3	Connects to SDRAM (U3)	97	SW6-1 : ON
		DRP21	Connects to DRP connector (CN2)		SW6-1 : OFF
B14	PF_2 / TxD3 / DV0_DATA17 / LCD0_DATA6 / MTIOC7C / MISO1	DV0_DATA17 LCD0_DATA6	Connects to digital image input/output connector (CN15)	93	
B15	P8_7 / A7 / DRP17 / DV0_DATA10 / RSPCK0 / SSIBCK3	A7	Connects to SDRAM (U3)	87	SW6-1 : ON
		DRP17	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-2 : ON
		RSPCK0	Connects to Audio CODEC (U21)		SW6-1 : OFF SW6-2 : OFF
B16	PE_3 / ET0_RXER/RMII0_RXER / VIO_D5 / SSIBCK0 / MTIOC0A	ET0_RXER/RMII0_RXER	Connects to Ethernet PHY1 (U27)	79	SW6-4 : ON
		VIO_D5	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
B17	PA_0 / A16 / DV0_DATA13 / LCD0_DATA10 / SCI_TXD1 / MTIOC8C	DV0_DATA13 LCD0_DATA10	Connects to digital image input/output connector (CN15)	77	
B18	PA_3 / A19 / DV0_DATA10 / LCD0_DATA13 / SCI_CTS0/RTS0 / MTIOC0D	DV0_DATA10 LCD0_DATA13	Connects to digital image input/output connector (CN15)	68	
B19	PA_5 / A21 / DV0_DATA8 / LCD0_DATA15 / SCI_RXD0 / MTIOC0B / IRQ5	DV0_DATA8 LCD0_DATA15	Connects to digital image input/output connector (CN15)	71	SW6-7 : ON
B20	PA_6 / A22 / DV0_DATA7 / LCD0_DATA16 / SCI_SCK0 / MTIOC0A	DV0_DATA7 LCD0_DATA16	Connects to digital image input/output connector (CN15)	67	SW6-7 : ON
B21	Vss		Connects to DIP switch (CPU board SW1)	—	SW1-8: ON
B22	PVcc				
C1	PH_2 / CTS2 / DV0_DATA22 / LCD0_DATA1 / MTIOC6D / SSIRxD0	DV0_DATA22 LCD0_DATA1	Connects to digital image input/output connector (CN15)	143	
C2	P8_2 / A2 / DRP22 / DV0_DATA15 / GTIOC5A / IRQ2	A2	Connects to SDRAM (U3)	141	SW6-1 : ON
		DRP22	DRP connector (CN2)		SW6-1 : OFF
C3	Vcc				
C4	QSPI1_SSL		Connects to serial flash memory (U2 on the CPU board)	—	
C5	RPC_INT#		Connects to serial flash memory (U2 on the CPU board)	—	
C6	QSPI0_SSL		Connects to serial flash memory (U2 on the CPU board)	—	
C7	QSPI0_IO0		Connects to serial flash memory (U2 on the CPU board)	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.4 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (4)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
C8	P6_1 / ET0_TXEN/RMII0_TXDEN / VIO_CLK / SCK3 / MTIOC2A	ET0_TXEN/RMII0_TXDEN	Connects to Ethernet PHY1 (U27)	119	SW6-4 : ON
		VIO_CLK	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
C9	P6_2 / ET0_TXD0/RMII0_TXD0 / VIO_VD / RxD3 / MTIOC2B / OTG_EXICEN1 / IRQ0	ET0_TXD0/RMII0_TXD0	Connects to Ethernet PHY1 (U27)	106	SW6-4 : ON
		VIO_VD	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
C10	PH_1 / AUDIO_XOUT / VIO_D0 / GTIOC4B / MTIOC1B / CC2_RD0 / IRQ2	VIO_D0	Connects to CMOS camera connector (CN17)	126	
C11	PL_4 / MD_BOOT0 / IRQ0	MD_BOOT0	D Connects to IP switch (SW1 on the CPU board)	—	SW1-5
C12	PL_0 / MD_CLKS / IRQ4	IRQ4	Connects to Ethernet PHY1 (U27)	50	PD_0 : Low SW6-4 : ON
		MD_CLKS	Connects to DIP switch (SW1 on the CPU board)	—	PD_0 : High SW1-1
C13	P8_5 / A5 / DRP19 / DV0_DATA12 / MISO0 / SSITxD3	A5	Connects to SDRAM (U3)	92	SW6-1 : ON
		DRP19	Connects to DRP connector (CN2)		SW6-1 : OFF
C14	PF_1 / RxD3 / DV0_DATA16 / LCD0_DATA7 / MTIOC7B / MOSI1 / IRQ4	DV0_DATA16	Connects to digital image input/output connector (CN15)	88	
		LCD0_DATA7			
C15	P9_0 / A8 / DRP16 / DV0_DATA9 / TxD4 / SSIDATA2	A8	Connects to SDRAM (U3)	84	SW6-1 : ON
		DRP16	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-3 : ON
		TxD4	Connects to USB Micro-B port (CN5) via USB serial converter IC (U23)		SW6-1 : OFF SW6-3 : OFF
C16	PE_2 / ET0_RXD1/RMII0_RXD1 / VIO_D6 / TxD2 / POE10	ET0_RXD1/RMII0_RXD1	Connects to Ethernet PHY1 (U27)	78	SW6-4 : ON
		VIO_D6	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
C17	PA_2 / A18 / DV0_DATA11 / LCD0_DATA12 / SCI_SCK1 / MTIOC8A	DV0_DATA11	Connects to digital image input/output connector (CN15)	74	
		LCD0_DATA12			
C18	PG_0 / ET0_TXCLK / VIO_D8 / RSPCK0 / MTIOC3A / HM_RSTO#	VIO_D8	Connects to CMOS camera connector (CN17)	72	
C19	PB_0 / A24 / DV0_DATA5 / LCD0_DATA18 / SSITxD1 / POE8	DV0_DATA5	Connects to digital image input/output connector (CN15)	64	
		LCD0_DATA18			
C20	Vss		Connects to DIP switch (CPU board SW1)	—	SW1-7: ON
C21	PD_7 / RIIC3SDA / IRQ7	RIIC3SDA	Connects to CMOS camera connector (CN17)	58	
			Connects to EEPROM (U32)		
			Connects to digital image input/output connector (CN15)		

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.5 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (5)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
C22	PD_3 / RIIC1SDA / IRQ3 / MTCLKD / GTETRGD	PD_3	Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
D1	PVcc				
D2	BSCANP		Connects to DIP switch (SW1 on the CPU board)	—	SW1-6
D3	P8_1 / A1 / DRP23 / DV0_DATA16 / GTIOC5B / IRQ3	A1	Connects to SDRAM (U3)	128	SW6-1 : ON
		DRP23	Connects to DRP connector (CN2)		SW6-1 : OFF
D4	Vcc				
D5	QSPI1_IO2		Connects to Serial flash memory (U2 on the CPU board)	—	
D6	Vss				
D7	QSPI0_IO2		Connects to Serial flash memory (U2 on the CPU board)	—	
D8	PK_0 / ET1_TXEN/RMII1_TXDEN / NAF3 / CC1_RD0 / MTIOC1B / SSIBCK2	ET1_TXEN/RMII1_TXDEN	Connects to Ethernet PHY2 (U28)	110	SW6-5 : ON
		NAF3	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
D9	PF_6 / RTS2 / DV0_DATA21 / LCD0_DATA2 / MTIOC6C / SSITxD0	DV0_DATA21	Connects to digital image input/output connector (CN15)	108	
		LCD0_DATA2			
D10	PE_0 / ET0_RXCLK/REF50CK0 / VIO_FLD / SCK2 / POE4	ET0_RXCLK/REF50CK0	Connects to Ethernet PHY1 (U27)	102	SW6-4 : ON
		VIO_FLD	Connects to CMOS camera connector (CN17)		SW6-4 : OFF
D11	PF_3 / SCK2 / DV0_DATA18 / LCD0_DATA5 / MTIOC7D / SSL10	DV0_DATA18	Connects to digital image input/output connector (CN15)	124	
		LCD0_DATA5			
D12	PVcc				
D13	Vss				
D14	PF_0 / SCK3 / DV0_DATA15 / LCD0_DATA8 / MTIOC7A / RSPCK1	DV0_DATA15	Connects to digital image input/output connector (CN15)	90	
		LCD_DATA8			
D15	P8_0 / A0 / DV0_DATA14 / LCD0_DATA9 / SCI_CTS1/RTS1 / MTIOC8D	DV0_DATA14	Connects to digital image input/output connector (CN15)	86	
		LCD0_DATA9			
D16	PA_1 / A17 / DV0_DATA12 / LCD0_DATA11 / SCI_RXD1 / MTIOC8B / IRQ6	DV0_DATA12	Connects to digital image input/output connector (CN15)	80	
		LCD0_DATA11			
D17	PA_7 / A23 / DV0_DATA6 / LCD0_DATA17 / SSIRxD1 / POE10	DV0_DATA6	Connects to digital image input/output connector (CN15)	76	SW6-7 : ON
		LCD0_DATA17			
D18	PVcc				
D19	Vss				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.6 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (6)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
D20	PD_6 / RIIC3SCL / IRQ6	RIIC3SCL	Connects to CMOS camera connector (CN17) Connects to EEPROM (U32) Connects to digital image input/output connector (CN15)	60	
D21	PD_4 / RIIC2SCL / IRQ4	RIIC2SCL	Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board) Connects to USB CC logic controller (U7 on the CPU board)	—	
D22	PD_1 / RIIC0SDA / IRQ1 / MTCLKB / GTETRGB	PD_1	Controls voltage supplied to PVcc_SD0	—	0 : 1.8V 1 : 3.3V
E1	Vss				
E2	PH_3 / HM_RSTO# / RTS2 / GTIOC6A / MTIOC2A / SD0_CD / IRQ3	HM_RSTO#	Connects to HyperMCP (U3 on the CPU board)	—	
E3	PK_3 / ET1_RXCLK/REF50CK1 / NAF6 / CC2_RD0 / CAN0RX_DATARATE_EN / MOSI0	ET1_RXCLK/REF50CK1 NAF6	Connects to Ethernet PHY2 (U28) Connects to NAND flash memory (U31)	132	SW6-5 : ON Not used SW6-5 : OFF
E4	PK_2 / ET1_TXD1/RMII1_TXD1 / NAF5 / VBUSEN1 / CAN0RX / RSPCK0 / IRQ5	ET1_TXD1/RMII1_TXD1 NAF5	Connects to Ethernet PHY2 (U28) Connects to NAND flash memory (U31)	133	SW6-5 : ON Not used SW6-5 : OFF
E19	PD_5 / RIIC2SDA / IRQ5	RIIC2SDA	Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board) Connects to USB CC logic controller (U7 on the CPU board)	—	
E20	PD_2 / RIIC1SCL / IRQ2 / MTCLKC / GTETRGC	PD_2	Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
E21	JP0_3 / TCK	TCK	Connects to UDI connector (CN5 on the CPU board)	—	
E22	JP0_0 / TDI	TDI	Connects to UDI connector (CN5 on the CPU board)	—	
F1	PVcc_HO				1.8V
F2	HM_CS0#/OM_CS0#	HM_CS0#	Connects to HyperMCP (U3 on the CPU board)	—	
F3	HM_CK/OM_SCLK	HM_CK	Connects to HyperMCP (U3 on the CPU board)	—	
F4	PF_7 / GTETRGD / DV0_DATA23 / LCD0_DATA0 / MTCLKD / IRQ1	DV0_DATA23 LCD0_DATA0	Connects to digital image input/output connector (CN15)	136	
F19	PD_0 / RIIC0SCL / IRQ0 / MTCLKA / GTETRGA	PD_0	Connection control for PL_[3:0]	—	0 : IRQ input 1 : SW1
F20	JP0_4 / TRST#	TRST#	Connects to UDI connector (CN5 on the CPU board)	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.7 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (7)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
F21	JP_2 / TMS	TMS	Connects to UDI connector (CN5 on the CPU board)	—	
F22	PB_1 / A25 / DV0_DATA4 / LCD0_DATA19 / SSIFS1 / POE4	DV0_DATA4 LCD0_DATA19	Connects to digital image input/output connector (CN15)	63	
G1	HM_DQ1/OM_SIO1	HM_DQ1	Connects to HyperMCP (U3 on the CPU board)	—	
G2	HM_RWDS/OM_DQS	HM_RWDS	Connects to HyperMCP (U3 on the CPU board)	—	
G3	HM_CS1#/OM_CS1#	HM_CS1#	Connects to HyperMCP (U3 on the CPU board)	—	
G4	HM_CK#		Connects to HyperMCP (U3 on the CPU board)	—	
G19	JP0_1 / TDO	TDO	Connects to UDI connector (CN5 on the CPU board)	—	
G20	PB_2 / BS / DV0_DATA3 / LCD0_DATA20 / SSIBCK1 / POE0	DV0_DATA3 LCD0_DATA19	Connects to digital image input/output connector (CN15)	66	
G21	PB_3 / CS0 / DV0_DATA2 / LCD0_DATA21 / SSIDATA2 / CTS0	DV0_DATA2 LCD0_DATA21	Connects to digital image input/output connector (CN15)	61	
G22	P9_2 / A10 / DRP14 / DV0_DATA7 / SCK4 / SSIBCK2	A10 DRP14	Connects to SDRAM (U3) Connects to DRP connector (CN2)	59	SW6-1 : ON SW6-1 : OFF
H1	HM_DQ4/OM_SIO4	HM_DQ4	Connects to HyperMCP (U3 on the CPU board)	—	
H2	HM_DQ2/OM_SIO2	HM_DQ2	Connects to HyperMCP (U3 on the CPU board)	—	
H3	HM_DQ3/OM_SIO3	HM_DQ3	Connects to HyperMCP (U3 on the CPU board)	—	
H4	HM_DQ0/OM_SIO0	HM_DQ0	Connects to HyperMCP (U3 on the CPU board)	—	
H19	PB_4 / CS1 / DV0_DATA1 / LCD0_DATA22 / SSIFS2 / RTS0	DV0_DATA1 LCD0_DATA22	Connects to digital image input/output connector (CN15)	40	
H20	P9_3 / A11 / DRP13 / DV0_DATA6 / SSIRxD0	A11 DRP13 SSIRxD0	Connects to SDRAM (U3) Connects to DRP connector (CN2) Connects to Audio CODEC (U21)	42	SW6-1 : ON SW6-1 : OFF SW6-2 : ON SW6-1 : OFF SW6-2 : OFF
H21	PB_5 / WAIT / DV0_DATA0 / LCD0_DATA23 / SSIBCK2 / TxD0	DV0_DATA0 LCD0_DATA23	Connects to digital image input/output connector (CN15)	57	
H22	P9_5 / A13 / DRP11 / DV0_DATA4 / SSIFS0	A13 DRP11 SSIFS0	Connects to SDRAM (U3) Connects to DRP connector (CN2) Connects to Audio CODEC (U21)	55	SW6-1 : ON SW6-1 : OFF SW6-2 : ON SW6-1 : OFF SW6-2 : OFF
J1	HM_RESET#/OM_RESET#	HM_RESET#	Connects to HyperMCP (U3 on the CPU board)	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.8 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (8)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
J2	HM_DQ6/OM_SIO6	HM_DQ6	Connects to HyperMCP (U3 on the CPU board)	—	
J3	HM_DQ7/OM_SIO7	HM_DQ7	Connects to HyperMCP (U3 on the CPU board)	—	
J4	HM_DQ5/OM_SIO5	HM_DQ5	Connects to HyperMCP (U3 on the CPU board)	—	
J9	Vcc				
J10	Vss				
J11	Vss				
J12	Vss				
J13	Vss				
J14	Vcc				
J19	P9_4 / A12 / DRP12 / DV0_DATA5 / SSITxD0	A12	Connects to SDRAM (U3)	112	SW6-1 : ON
		DRP12	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-2 : ON
		SSITxD0	Connects to Audio CODEC (U21)		SW6-1 : OFF SW6-2 : OFF
J20	P7_7 / RD / DV0_HSYNC / LCD0_TCON0 / GTIOC3B / RxD0	DV0_HSYNC	Connects to digital image input/output connector (CN15)	44	
		LCD0_TCON			
J21	P7_6 / AH / DV0_VSYNC / LCD0_TCON1 / GTIOC3A / SCK0	GTIOC3A	Connects to digital image input/output connector (CN15)	53	
		DV0_VSYNC			
J22	P9_6 / A14 / DRP10 / DV0_DATA3 / SSIBCK0	A14	Connects to SDRAM (U3)	49	SW6-1 : ON
		DRP10	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-2 : ON
		SSIBCK0	Connects to Audio CODEC (U21)		SW6-1 : OFF SW6-2 : OFF
K1	Vss				
K2	PJ_6 / GTETRGC / FCE / LCD0_CLK / MTCLKC / IRQ0	LCD0_CLK	Connects to digital image input/output connector (CN15)	147	SW6-6 : ON
		FCE	Connects to NAND flash memory (U31)		Not used SW6-6 : OFF
K3	PH_4 / HM_INT# / CTS2 / GTIOC6B / MTIOC2B / SD0_WP / IRQ2	HM_INT#	Connects to HyperMCP (U3 on the CPU board)	—	
K4	PJ_0 / TRACECLK / SPDIF_OUT / VRAMMON0 / SCK1 / SSIRxD3	TRACECLK	Connects to UDI connector (CN5 on the CPU board)	—	
K9	Vcc				
K10	Vss				
K11	Vss				
K12	Vss				
K13	Vss				
K14	Vcc				
K19	P9_7 / A15 / DRP09 / DV0_DATA2 / SD1_WP	A15	Connects to SDRAM (U3)	118	SW6-1 : ON
		DRP09	Connects to DRP connector (CN2)		SW6-1 : OFF

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.9 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (9)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
K20	PG_1 / ET0_TXD2 / VIO_D9 / MOSI0 / MTIOC3C / HM_INT#	VIO_D9	Connects to CMOS camera connector (CN17)	116	
K21	P7_5 / CKE / DRP08 / DV0_DATA1 / CTS1 / OVRCUR1	CKE	Connects to SDRAM (U3)	45	SW6-1 : ON
		DRP08	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-3 : ON
		CTS1			
		OVRCUR1	Connects to VBUS power supply control C (U29)		SW6-1 : OFF SW6-3 : OFF
K22	PG_2 / ET0_TXD3 / VIO_D10 / MISO0 / MTIOC3B / GTIOC0A / IRQ4	VIO_D10	Connects to CMOS camera connector (CN17)	43	
L1	PVcc				
L2	P0_1 / D1 / DRP25 / DV0_DATA18 / MTIOC6C / GTIOC4A	D1	Connects to SDRAM (U3)	151	SW6-1 : ON
		DRP25	Connects to DRP connector (CN2)		SW6-1 : OFF
L3	P0_0 / D0 / DRP24 / DV0_DATA17 / MTIOC6B / GTIOC3B	D0	Connects to SDRAM (U3)	144	SW6-1 : ON
		DRP24	Connects to DRP connector (CN2)		SW6-1 : OFF
L4	PJ_7 / GTETRGB / NAF0 / LCD0_EXTCLK / MTCLKB	LCD0_EXTCLK	Connects to VDC6 oscillator (X5)	140	40MHz SW6-6 : ON
		NAF0	Connects to NAND flash memory (U31)		Not used SW6-6 : OFF
L9	Vcc				
L10	Vss				
L11	Vss				
L12	Vss				
L13	Vss				
L14	Vcc				
L19	P7_1 / RD/WR / DRP05 / DV0_VSYNC / RxD1 / CC1_RA1	RD/WR	Connects to SDRAM (U3)	123	SW6-1 : ON
		DRP05	Connects to DRP connector (CN2)		SW6-1 : OFF
		RxD1			
L20	P7_4 / CAS / DRP07 / DV0_DATA0 / RTS1 / CC2_RA1	CAS	Connects to SDRAM (U3)	120	SW6-1 : ON
		DRP07	Connects to DRP connector (CN2)		SW6-1 : OFF
		RTS1			
L21	P7_3 / RAS / DRP06 / DV0_HSYNC / TxD1 / CC2_RD1	RAS	Connects to SDRAM (U3)	41	SW6-1 : ON
		DRP06	Connects to DRP connector (CN2)		SW6-1 : OFF
		TxD1			
L22	P7_2 / CS4 / DV0_CLK / LCD0_TCON2 / TEND0 / CC2_RA0	DV0_CLK	Connects to Connects digital image input/output connector (CN15)	37	
M1	P0_2 / D2 / DRP26 / DV0_DATA19 / MTIOC6D / GTIOC4B	D2	Connects to SDRAM (U3)	155	SW6-1 : ON
		DRP26	Connects to DRP connector (CN2)		SW6-1 : OFF
M2	P0_5 / D5 / DRP29 / DV0_DATA22 / MTIOC7C / GTIOC7A	D5	Connects to SDRAM (U3)	153	SW6-1 : ON
		DRP29	Connects to DRP connector (CN2)		SW6-1 : OFF
M3	P0_4 / D4 / DRP28 / DV0_DATA21 / MTIOC7B / GTIOC6B	D4	Connects to SDRAM (U3)	146	SW6-1 : ON
		DRP28	Connects to DRP connector (CN2)		SW6-1 : OFF

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.10 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (10)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
M4	P0_3 / D3 / DRP27 / DV0_DATA20 / MTIOC7A / GTIOC6A	D3	Connects to SDRAM (U3)	148	SW6-1 : ON
		DRP27	Connects to DRP connector (CN2)		SW6-1 : OFF
M9	Vcc				
M10	Vss				
M11	Vss				
M12	Vss				
M13	Vss				
M14	Vcc				
M19	P6_6 / CS2 / DRP02 / LCD0_TCON4 / DREQ0 / CC1_RA0	DRP02	Connects to DRP connector (CN2)	127	
M20	P6_0 / ADTRG0	P6_0	Connects to LED1 (red) on the CPU board	125	1 : Light on
M21	P7_0 / WE1/DQMU / DRP04 / DV0_CLK / SCK1 / CC1_RD1	WE1/DQML	Connects to SDRAM (U3)	25	SW6-1 : ON
		DRP04	Connects to DRP connector (CN2)		SW6-1 : OFF
		SCK1			
M22	PVcc				
N1	PJ_3 / TRACEDATA1 / NAF0 / VRAMMON3 / RTS1 / SSIFS3	TRACEDATA1	Connects to UDI connector (CN5 on the CPU board)	—	
N2	PJ_1 / TRACECTL / SPDIF_IN / VRAMMON1 / RxD1 / VBUSIN0 / IRQ0	IRQ0	Connects to IRQ0 switch (SW3)	159	JP1 : 2-JP2
			Connects to Ethernet PHY1 (U27)		JP1 : 1-2
			Connects to Ethernet PHY2 (U28)		JP1 : 2-3
N3	P0_6 / D6 / DRP30 / DV0_DATA23 / MTIOC7D / GTIOC7B	D6	Connects to SDRAM (U3)	150	SW6-1 : ON
		DRP30	Connects to DRP connector (CN2)		SW6-1 : OFF
N4	PJ_2 / TRACEDATA0 / FCE / VRAMMON2 / TxD1 / SSITxD3	TRACEDATA0	Connects to UDI connector (CN5 on the CPU board)	—	
N9	Vcc				
N10	Vss				
N11	Vss				
N12	Vss				
N13	Vss				
N14	Vcc				
N19	P6_5 / CS3 / DRP01 / LCD0_TCON5 / AUDIO_XOUT / CC1_RD0	CS3	Connects to SDRAM (U3)	135	SW6-1 : ON
		DRP01	Connects to DRP connector (CN2)		SW6-1 : OFF
N20	PG_3 / ET0_COL / VIO_D11 / SSL00 / MTIOC3D / GTIOC0B	VIO_D11	Connects to CMOS camera connector (CN17)	129	
N21	P6_4 / CS5 / DRP00 / LCD0_TCON6 / AUDIO_CLK / SD1_CD	DRP00	Connects to DRP connector (CN2)	36	SW6-2 : ON
		AUDIO_CLK	Connects to Audio oscillator (X1)		11.2896MHz SW6-2 : OFF
N22	Vss				
P1	PH_6 / HM_INT# / NAF3 / ET1_WOL / MTIC5V / IRQ4	ET1_WOL	Connects to Ethernet PHY2 (U28)	163	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.11 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (11)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
P2	PH_5 / HM_RSTO# / NAF2 / ET1_EXOUT / MTIC5U / IRQ5	ET1_EXOUT	Connects to Ethernet PHY2 (U28)	161	SW6-5 : ON
		NAF2	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
P3	PK_5 / GTETRGA / NAF1 / WDTOVF/PERROUT / MTCLKA	NAF1	Connects to NAND flash memory (U31)	167	Not used
P4	PVcc				
P9	Vcc				
P10	Vss				
P11	Vss				
P12	Vss				
P13	Vss				
P14	Vcc				
P19	SD0_DAT7		Connects to SDVcc through a resistor	—	
P20	SD0_RST#		Connects to the test point (TP1 on the CPU board)	—	
P21	P6_7 / WE0/DQML / DRP03 / LCD0_TCON3 / DACK0 / CC2_RD0	WE0/DQML	Connects to SDRAM (U3)	23	SW6-1 : ON
		DRP03	Connects to DRP connector (CN2)		SW6-1 : OFF
P22	PVcc_SD0				
R1	PVcc				
R2	PJ_4 / TRACEDATA2 / NAF1 / VRAMMON4 / CTS1 / SSIBCK3	TRACEDATA2	Connects to UDI connector (CN5 on the CPU board)	—	
R3	PJ_5 / TRACEDATA3 / NAF2 / OVRCUR0 / MTIOC1A / SSIFS2 / IRQ4	TRACEDATA3	Connects to UDI connector (CN5 on the CPU board)	—	
R4	Vss				
R19	SD0_DAT2		Connects to microSD card slot (CN1 on the CPU board)	—	
R20	SD0_DAT5		Connects to SDVcc through a resistor	—	
R21	SD0_DAT4		Connects to SDVcc through a resistor	—	
R22	SD0_DAT6		Connects to SDVcc through a resistor	—	
T1	AUDIO_X1		Connects to GND through a resistor	—	
T2	AUDIO_X2		Open	—	
T3	P3_5 / ET1_RXD1/RMII1_RXD1 / FCLE / CC2_RA0 / CAN0TX_DATARATE_EN / SSL00	ET1_RXD1/RMII1_RXD1	Connects to Ethernet PHY2 (U28)	156	SW6-5 : ON
		FCLE	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
T4	P3_2 / ET1_CRS/RMII1_CRSDV / FRE / CC1_RA1 / CAN1RX_DATARATE_EN / MOSI2	ET1_CRS/RMII1_CRSDV	Connects to Ethernet PHY2 (U28)	154	SW6-5 : ON
		FRE	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
T19	SD0_DAT0		Connects to microSD card slot (CN1 on the CPU board)	—	
T20	SD0_DAT1		Connects to microSD card slot (CN1 on the CPU board)	—	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.12 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (12)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
T21	SD0_DAT3		Connects to microSD card slot (CN1 on the CPU board) connection	—	
T22	Vss				
U1	Vss				
U2	PK_4 / ET1_RXD0/RMII1_RXD0 / NAF7 / OVRCUR1 / CAN0TX / MISO0 / IRQ6	ET1_RXD0/RMII1_RXD0	Connects to Ethernet PHY2 (U28)	164	SW6-5 : ON
		NAF7	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
U3	P3_1 / ET1_RXER/RMII1_RXER / FALE / VBUSEN0 / CAN1RX / RSPCK2 / IRQ6	ET1_RXER/RMII1_RXER	Connects to Ethernet PHY2 (U28)	166	SW6-5 : ON
		FALE	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
U4	MIPIAVcc18_1				
U19	SD1_DAT0		Connects to SD card slot (CN10)	33	
U20	SD1_DAT2		Connects to SD card slot (CN10)	31	
U21	SD0_CMD		Connects to microSD card slot (CN1 on the CPU board)	—	
U22	SD0_CLK		Connects to microSD card slot (CN1 on the CPU board)	—	
V1	CSI_CLKP		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
V2	CSI_CLKN		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
V3	PG_4 / ET0_TXER / VIO_D15 / RSPCK1 / MTIOC4A / GTIOC1A	VIO_D15	Connects to CMOS camera connector (CN17)	169	
V4	Vss				
V19	P5_4 / AN004 / IRQ0 / SD1_CD	SD1_CD	Connects to SD card slot (CN10)	18	
V20	SD1_DAT1		Connects to SD card slot (CN10)	29	
V21	SD1_DAT3		Connects to SD card slot (CN10)	32	
V22	PVcc_SD1				3.3V
W1	CSI_DATA0P		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
W2	CSI_DATA0N		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
W3	Vss				
W4	PG_6 / ET0_RXD2 / VIO_D13 / MISO1 / MTIOC4C / GTIOC2A / IRQ5	VIO_D13	Connects to CMOS camera connector (CN17)	171	
W5	P1_0 / D7 / DRP31 / IRQ0 / CAN_CLK / VBUSEN0	D7	Connects to SDRAM (U3)	160	SW6-1 : ON
		DRP31	Connects to DRP connector (CN2)		SW6-1 : OFF SW6-3 : ON
W6	P1_2 / D9 / MTIOC8B / IRQ2 / CAN0RX_DATARATE_EN / VBUSEN1	D9	Connects to SDRAM (U3)	196	

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.13 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (13)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
W7	P2_0 / D12 / GTIOC6A / IRQ5 / CAN1RX / OTG_EXICEN0	D12	Connects to SDRAM (U3)	200	SW6-1 : ON
W8	PC_2 / OTG_EXICEN0 / NAF7 / ET1_TXD3 / MISO2 / LCD0_TCON5	PC_2	Connects to DIP switch (SW6)	202	SW6-10
W9	P4_3 / RTS0 / TXOUT1M / SCI_CTS1/RTS1 / SSIFS1 / MTIOC8D / IRQ3	TXOUT1M	Connects to LVDS connector (CN14)	184	
W10	LVDSAPVcc				
W11	Vss				
W12	LVDSPLLVcc				
W13	USBDPVcc0				
W14	USBVss				
W15	Vss				
W16	PVcc				
W17	Vss				
W18	PLLVcc				
W19	P5_2 / AN002 / IRQ6 / VBUSIN0	VBUSIN0	Connects to USB connector (CN3 on the CPU board)	—	JP3
W20	P5_6 / AN006 / IRQ2	AN006	Connects to the key input switch (SW4 and SW5)	14	SW4, SW5
W21	SD1_CMD		Connects to SD card slot (CN10)	28	
W22	Vss				
Y1	CSI_DATA1P		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
Y2	CSI_DATA1N		Connects to MIPI CSI-2 connector (CN2 and J1 on the CPU board)	—	
Y3	Vss				
Y4	P3_3 / ET1_MDC / FWE / OTG_EXICEN0 / CAN1TX / MISO2 / IRQ7	ET1_MDC	Connects to Ethernet PHY2 (U28)	177	SW6-5 : ON
		FWE	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
Y5	P1_4 / D11 / MTIOC8D / IRQ4 / CAN0TX_DATARATE_EN / VBUSIN0	D11	Connects to SDRAM (U3)	173	
Y6	PC_0 / VBUSIN1 / NAF5 / ET1_TXCLK / RSPCK2 / IRQ2	VBUSIN1	Connects to USB Mini-B port (CN13)	194	
Y7	P2_2 / D14 / GTIOC7A / IRQ7 / CAN1TX / VBUSIN1	D14	Connects to SDRAM (U3)	198	SW6-1 : ON
Y8	P4_2 / TxD0 / TXOUT1P / SCI_TXD1 / SSITxD1 / MTIOC8C / IRQ2	TXOUT1P	Connects to LVDS connector (CN14)	182	
Y9	P4_6 / ET0_EXOUT / TXCLKOUTP / SCI_TXD0 / TxD4 / DACK0	TXCLKOUTP	Connects to LVDS connector (CN14) connection	188	
Y10	NMI		Connects to NMI switch (SW2)	203	
Y11	Vss				
Y12	USBVss				
Y13	USBVss				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.14 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (14)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
Y14	USBVss				
Y15	USBVss				
Y16	USBDPVcc1				
Y17	PC_7 / OVRCUR0 / FRB / ET1_RXD3 / SD1_WP / LCD0_TCON0 / IRQ6	OVRCUR0	Connects to USB VBUS power supply control IC (U5 on the CPU board)	—	
Y18	PC_6 / VBUSEN0 / FWE / ET1_RXD2 / SD1_CD / LCD0_TCON1 / IRQ7	VBUSEN0	Connects to USB VBUS power supply control IC (U5 on the CPU board)	—	
Y19	P5_0 / AN000 / IRQ4 / SD0_CD / SD1_CD	SD0_CD	Connects to microSD card slot (CN1 on the CPU board)	—	
Y20	P5_1 / AN001 / IRQ5 / SD0_WP / SD1_WP	SD0_WP	Connects to D 3.3V and GND through resistors	—	
Y21	P5_7 / AN007 / IRQ3	IRQ3	Connects to digital image input/output connector (CN15)	19	
Y22	SD1_CLK		Connects to SD card slot (CN10)	24	
AA1	MIPIAVcc18_2				
AA2	Vss				
AA3	P1_1 / D8 / MTIOC8A / IRQ1 / CAN0RX / OVRCUR0	D8	Connects to SDRAM (U3)	179	SW6-1 : ON
AA4	P3_4 / ET1_MDIO / FRB / CC2_RA1 / CAN1TX_DATARATE_EN / SSL20	ET1_MDIO	Connects to Ethernet PHY2 (U28)	187	SW6-5 : ON
		FRB	Connects to NAND flash memory (U31)		Not used SW6-5 : OFF
AA5	P3_0 / OTG_EXICEN1 / NAF4 / ET1_LINKSTA / MTIC5W / IRQ3	ET1_LINKSTA	Connects to Ethernet PHY2 (U28)	191	
AA6	PC_1 / VBUSIN0 / NAF6 / ET1_TXD2 / MOSI2 / LCD0_TCON6	PC_1	Connects to LED1 (green) on the CPU board	197	1 : Light on
AA7	P4_0 / SCK0 / TXOUT0P / SCI_SCK1 / SSIBCK1 / MTIOC8A / IRQ0	TXOUT0P	Connects to LVDS connector (CN14)	170	
AA8	P4_4 / CTS0 / TXOUT2P / SCI_CTS0/RTS0 / WDTOVF/PERROUT / OTG_EXICEN0	TXOUT2P	Connects to LVDS connector (CN14)	176	
AA9	P4_7 / ET0_WOL / TXCLKOUTM / SCI_SCK0 / SCK4 / TEND0	TXCLKOUTM	Connects to LVDS connector (CN14)	190	
AA10	USB_X2		Connects to USB oscillator (X2 on the CPU board)	—	48MHz
AA11	DP0		Connects to USB connector (CN3 on the CPU board)	—	
AA12	USBAPVcc0				
AA13	RREF0		Connects to GND through a resistor	—	2.2kΩ±1%
AA14	USBVss				
AA15	DP1		Connects to USB Type-A port (CN12) and USB Mini-B port (CN13)	96	
AA16	PVcc				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.15 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (15)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
AA17	PC_5 / VBUSEN1 / FRE / ET1_RXDV / SPDIF_OUT / LCD0_TCON2 / IRQ0	VBUSEN1	Connects to USB Mini-B port (CN13)	8	
AA18	XTAL		Connects to system clock oscillator (X1 on the CPU board)	—	24MHz
AA19	PC_4 / OTG_ID1 / FALE / ET1_TXER / SPDIF_IN / LCD0_TCON3 / IRQ1	LCD0_TCON3	Connects to digital image input/output connector (CN15)	20	
AA20	RTC_X2		Connects to RTC oscillator (X3 on the CPU board)	—	32.768kHz
AA21	P5_3 / AN003 / IRQ7 / OTG_ID0	P5_3	Connects to DIP switch (SW6)	15	SW6-9
AA22	P5_5 / AN005 / IRQ1 / SD1_WP	SD1_WP	Connects to SD card slot (CN10)	17	
AB1	Vss				
AB2	PG_5 / ET0_RXDV / VIO_D14 / MOSI1 / MTIOC4B / GTIOC1B	VIO_D14	Connects to CMOS camera connector (CN17)	183	
AB3	PG_7 / ET0_RXD3 / VIO_D12 / SSL10 / MTIOC4D / GTIOC2B	VIO_D12	Connects to CMOS camera connector (CN17)	181	
AB4	P1_3 / D10 / MTIOC8C / IRQ3 / CAN0TX / OTG_ID1	D10	Connects to SDRAM (U3)	189	SW6-1：ON
AB5	P2_1 / D13 / GTIOC6B / IRQ6 / CAN1RX_DATARATE_EN / OTG_ID0	D13	Connects to SDRAM (U3)	193	
AB6	P2_3 / D15 / GTIOC7B / WDTOVF/PERROUT / CAN1TX_DATARATE_EN / OTG_EXICEN1	D15	Connects to SDRAM (U3)	199	
AB7	P4_1 / RxD0 / TXOUT0M / SCI_RXD1 / SSIRxD1 / MTIOC8B / IRQ1	TXOUT0M	Connects to LVDS connector (CN14)	172	
AB8	P4_5 / ET0_LINKSTA / TXOUT2M / SCI_RXD0 / RxD4 / DREQ0	TXOUT2M	Connects to LVDS connector (CN14)	178	
AB9	RES#		Connects to Reset input switch (SW2 on the CPU board)	7	
AB10	USB_X1		Connects to USB oscillator (X2 on the CPU board)	—	48MHz
AB11	DM0		Connects to USB connector (CN3 on the CPU board)	—	
AB12	USBAPVcc1				
AB13	RREF1		Connects to GND through a resistor	—	2.2kΩ±1%
AB14	USBVss				
AB15	DM1		Connects to USB Type-A port (CN12) and USB Mini-B port (CN13)	98	
AB16	PVcc				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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Table 2.2.16 List of RZ/A2M Pin Function Selections Used on the RTK79210XXB00000BE (16)

Pin	Pin Name	Pin Function	Description	CN1 Pin	Comments
AB17	PC_3 / OTG_ID0 / FCLE / ET1_COL / SSL20 / LCD0_TCON4	LCD0_TCON4	Connects to digital image input/output connector (CN15)	10	
AB18	EXTAL		Connects to system clock oscillator (X1 on the CPU board)	—	24MHz
AB19	Vss				
AB20	RTC_X1		Connects to RTC oscillator (X3 on the CPU board)	—	32.768kHz
AB21	AVcc				
AB22	AVcc				

[Note] : 3.3V power source, : 1.8V power source, : 1.2V power source, : 3.3V or 1.8V power source, : GND

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2.2.3 RTK79210XXB00000BE Interface Use Combination List

Table 2.2.17 shows the usage permission/denial list for each RTK79210XXB00000BE interface. The ○ marks indicate that combined use by both interfaces is possible, while the × marks indicate that combined use is not possible.

Table 2.2.17 RTK79210XXB00000BE Interface Usage Permission List

			RTK7921053C00000BE						RTK79210XXB0000BE																
	Part No.	Interface name	Serial flash memory	HyperMCP	microSD card slot	MIPI	USB1(Type-C)	CoreSight 20	Audio CODEC	Ethernet1	Ethernet2	SDRAM	NAND flash memory (not equipped)	EEPROM	DRP	UART	SD card slot	USB2(Type-A&Mini-B)	LVDS output	LCD output	DV input	CMOS camera	NMI switch	IRQ0switch (DSTBY release)
RTK7921053C00000BE	U2	Serial flash memory		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
	U3	HyperMCP	o		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
	CN1	microSD card slot	o	o		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
	CN2	MIPI	o	o	o		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
	CN3	USB1 (Type-C)	o	o	o	o		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
	CN5	CoreSight 20	o	o	o	o	o		o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
RTK79210XXB0000BE	U21	Audio CODEC	o	o	o	o	o	o		o	o	×	o	o	×	o	o	o	o	o	o	o	o	o
	U27	Ethernet1	o	o	o	o	o	o	o		*1	o	o	o	o	o	o	o	o	o	o	×	o	*1
	U28	Ethernet2	o	o	o	o	o	o	o	*1		o	×	o	o	o	o	o	o	o	o	o	o	*1
	U30	SDRAM	o	o	o	o	o	o	×	o	o		o	o	×	×	o	×	o	o	o	o	o	o
	U31	NAND flash memory (not equipped)	o	o	o	o	o	o	o	o	×	o		o	o	o	o	o	o	×	o	o	o	o
	U32	EEPROM	o	o	o	o	o	o	o	o	o	o	o		o	o	o	o	o	o	o	o	o	o
	CN2	DRP	o	o	o	o	o	o	×	o	o	×	o	o		×	o	×	o	o	o	o	o	o
	CN5	UART	o	o	o	o	o	o	o	o	o	×	o	o	×		o	o	o	o	o	o	o	o
	CN10	SD card slot	o	o	o	o	o	o	o	o	o	o	o	o	o	o		o	o	o	o	o	o	o
	CN12, CN13	USB2 (Type-A & Mini-B)	o	o	o	o	o	o	o	o	o	×	o	o	×	o	o		o	o	o	o	o	o
	CN14	LVDS output	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o		o	o	o	o	o
	CN15	LCD output	o	o	o	o	o	o	o	o	o	o	×	o	o	o	o	o	o		×	o	o	o
		DV input	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	×		o	o	o
	CN17	CMOS camera	o	o	o	o	o	o	o	×	o	o	o	o	o	o	o	o	o	o	o		o	o
	SW2	NMI switch	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o		o
	SW3	IRQ0switch (DSTBY release)	o	o	o	o	o	o	o	*1	*1	o	o	o	o	o	o	o	o	o	o	o	o	

[Note] *1 PJ_1 / IRQ0 (DSTBY release) is a shared pin. If the WOL function of the Ethernet PHY1 (U27) and Ethernet PHY2 (U28) is not used, it can be shared.

2.3 Memory

2.3.1 SDRAM

The RTK79210XXB00000BE is equipped with external SDRAM×1 shown in Table 2.3.1 as the standard configuration. SDRAM control is performed by the RZ/A2M on-chip bus state controller (BSC). There is a 16-bit connection to the SDRAM.

Figure 2.3.1 shows the SDRAM block diagram, and Table 2.3.2 shows the function settings of the DIP switch SW6-1 for system settings. Table 2.3.3 shows clock pulse oscillator settings, and Table 2.3.4 and Table 2.3.5 show the RZ/A2M bus state controller settings (read and write for SDRAM) when the bus clock is operating at 132MHz.

Table 2.3.1 SDRAM Overview

Specifications	Details
Model name	IS42S16320F-7TL
Configuration	64 MBytes (8 Mwords x 16 bits x 4 banks) x 1
Capacity	64 MBytes
Access time	5.4 ns
CAS latency	3 (when system clock is 132 MHz)
Refresh interval	8192 refresh cycle every 64 ms
Row address	A12 to A0
Column address	A9 to A0
Number of banks	4-bank operation controlled by BA0 and BA1

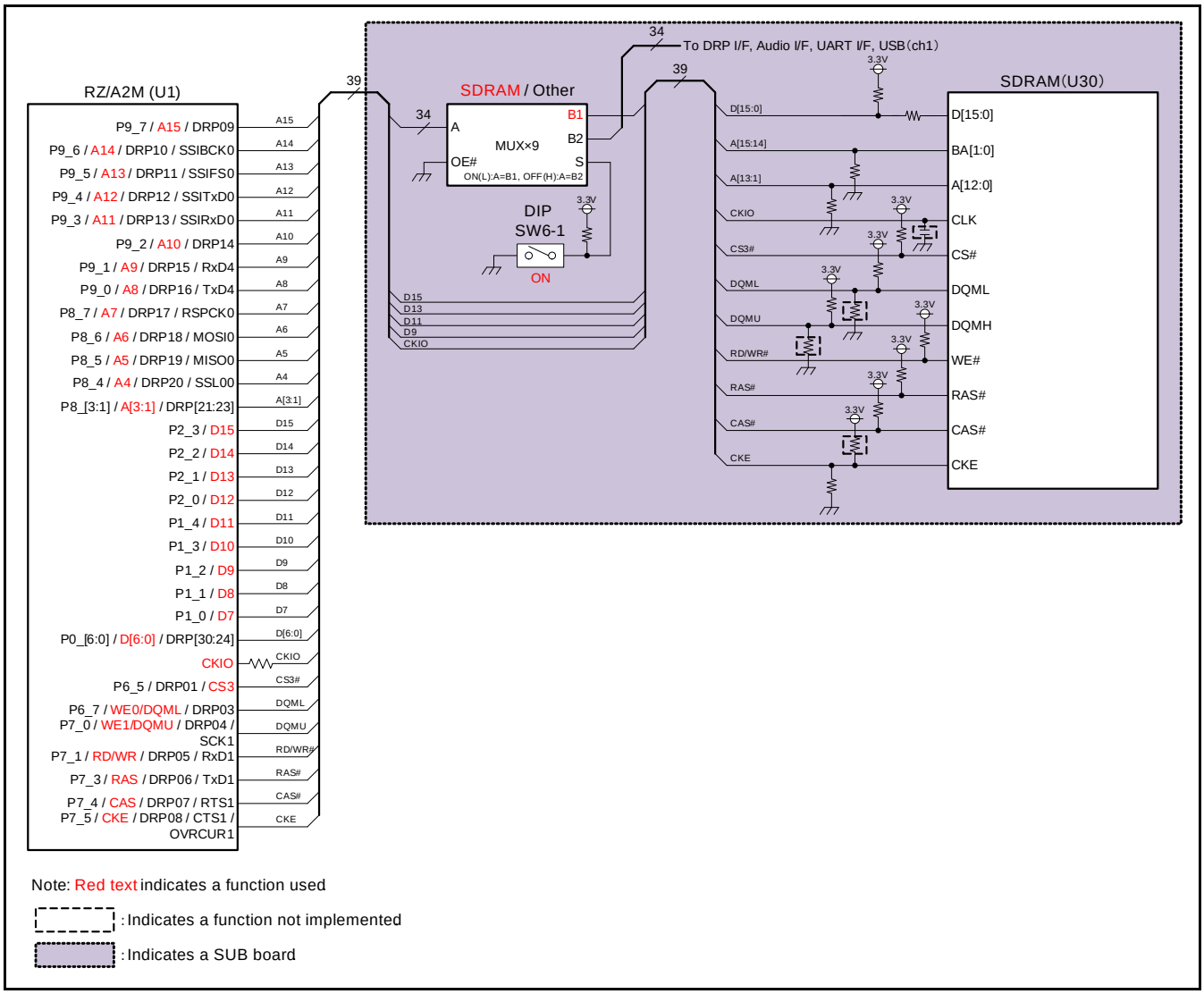


Figure 2.3.1 SDRAM Block Diagram

Table 2.3.2 Function Setting Table of DIP Switch SW6-1 for System Setting

DIP Switch	Function	
	ON	OFF
SW6-1	P9_[7 :0] and P8_[7 :1], P2_2, P2_0, P1_3, P1_[1 :0], P0_[6 :0], P6_7, P6_5, P7_[1 :0], P7[5 :3] are used as SDRAM control pins.	P9_[7 :0] and P8_[7 :1], P2_2, P2_0, P1_3, P1_[1 :0], P0_[6 :0], P6_7, P6_5, P7_[1 :0], P7[5 :3] are used as DRP, audio, UART and/or USB interface pins (default settings).

[Note] indicates setting functions.

Table 2.3.3 Clock Pulse Oscillator Settings

Target devices	Clock pulse oscillator settings
IS42S16320F-7TL	■ CKIO selection register (CKIOSEL) ・Initial value: H'0001 ・Recommended setting value: H'0000 -CKIO output clock selection: CKIOSEL[1:0] = B'00; Bφ clock output

Table 2.3.4 Bus State Controller Settings (SDRAM read/write) (1)

User region	Target device	Bus state controller settings
CS3	IS42S16320F-7TL	■ CS3 space bus control register (CS3BCR) ・Initial setting: H'36DB 0C00 ・Recommended setting: H'0000 4C00 - Memory specification: TYPE[2:0] = B'100; SDRAM - Data bus width specification: BSZ[1:0] = B'10; 16 bit bus width ■ CS3 space wait control register (CS3WCR) ・Initial setting：H'0000 0500 ・Recommended setting: H'0000 2D13 - Number of precharge completion wait cycles: WTRP[1:0] = B'01; 1 cycle - Number of ACTV command → READ (A) /WRIT (A) command interval wait cycles: WTRCD[1:0] = B'11; 3 cycle - Area 3CAS latency: A3CL[1:0] = B'10; 3 cycle - Number of precharge start wait cycles: TRWL[1:0] = B'10; 2 cycle - Number of REF command/ self refresh cancel →ACTV/REF/MRS command interval idle cycles: WTRC[1:0] = B'11; 8 cycle ■ SDRAM control register (SDCR) ・Initial setting: H'0000 0000 ・Recommended setting: H'0012 0812 - Refresh control: RFSH = 1; refresh - Refresh mode: RMODE = 0; carry out auto refresh - Bank active mode: BACTV = 0; Auto-precharge mode - Number of area 3 row address bits: A3ROW[1:0] = B'10; 13 bit - Number of area 3 column address bits: A3COL[1:0] = B'10; 10 bit ■ Refresh timer control/status register (RTCSR) ・Initial setting: H'0000 0000 ・Recommended setting: H'A55A 0010 - clock selection: CKS[2:0] = B'010; CKIO∅/16 - Number of refresh: RRC[2:0] = B'000; 1 time ■ Refresh time constant register (RTCOR) ・Initial setting: H'0000 0000 ・Recommended setting: H'A55A 0040 1 cycle＝121 nsec (132 MHz/16 = 8.25 MHz) Required refresh interval of this SDRAM: 7.8125 µsec / time 7.8125 µsec / 121 nsec = 64 (H'40) cycle/ number of refresh

Table 2.3.5 Bus State Controller Settings (SDRAM read/write) (2)

User region	Target device	Bus state controller settings
CS3	IS42S16320F-7TL	■ AC characteristics adjustment register (ACADJ) ・Initial setting: H'0000 0000 ・Recommended setting: H'0002 000F - Output characteristics adjustment bit: SDRODLY = B'0010; The SDRAM is to be connected. - Input characteristics adjustment bit: SDRIDLY = B'1111; The SDRAM is to be connected.

Table 2.3.6 GPIO Settings

Target devices	GPIO settings
IS42S16320F-7TL	■ CKIO pin driving ability control register (PCKIO) ・Initial setting: H'01 ・Recommended setting: H'02 - The driving ability of the CKIO pin: CKIO_DRV = B'10; 12mA

2.3.2 NAND Flash Memory Interface

RTK79210XXB00000BE is possible to mount NAND flash memory x 1 shown in Table 2.3.7 on the board pattern. NAND flash memory control is performed by the RZ/A2M on-chip NAND flash controller (FLCTL).

Figure 2.3.2 shows NAND flash memory interface block diagram, and Table 2.3.8 shows the function settings of the system setting DIP switches SW6-5 and SW6-6.

Table 2.3.7 NAND Flash Memory Overview

Model name	Bus size	Capacity	Access time
S34ML01G100TFI000	8 bit	128 MBytes (8 bit x 128 M word)	Random: 25 µs (max.) Sequential: 25 ns (min.)

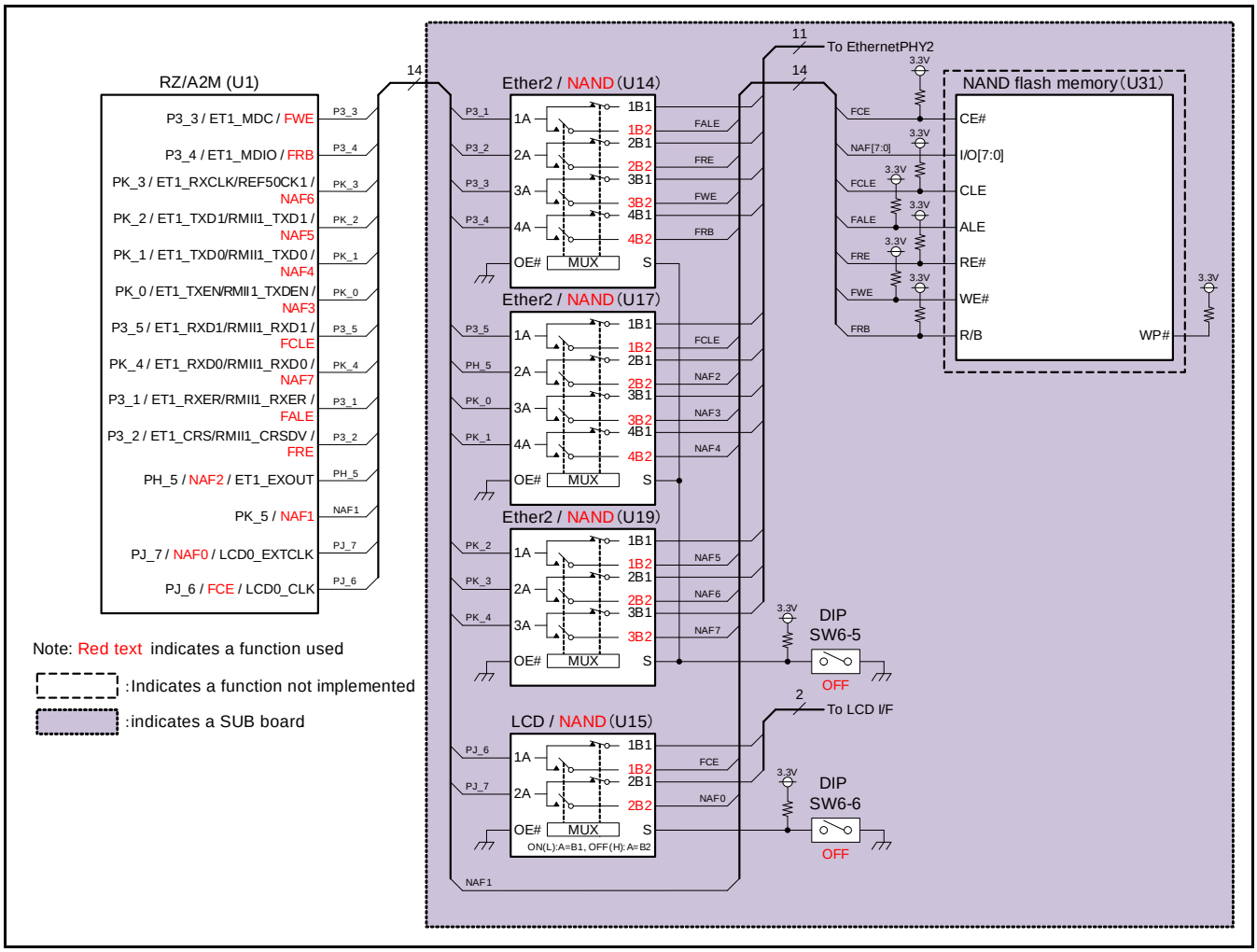


Figure 2.3.2 NAND Flash Memory Interface Block Diagram

Table 2.3.8 Function Setting Table of DIP Switches SW6-5 and SW6-6 for System Setting

DIP Switch	Function	
	ON	OFF
SW6-5	P3_[5 :1] and PH_5, PK_[4 :0] are used as Ethernet PHY2 control pins (default setting).	P3_[5 :1] and PH_5, PK_[4 :0] are used as FLCTL pins.
SW6-6	PJ_[7 :6] are used as VDC6 pins (default setting).	PJ_[7 :6] are used as FLCTL pins.

[Note] indicates setting function.

2.3.3 EEPROM Interface

RTK79210XXB00000BE is equipped with EEPROM x 1 shown in Table 2.3.9 as the standard configuration. EEPROM control is performed by the RZ/A2M on-chip 12C bus interface (RIIC) on channel 3.

Figure 2.3.3 shows EEPROM interface block diagram.

Table 2.3.9 EEPROM Overview

Model name	Interface	Capacity	Package
R1EX24128ASAS0A	2-line serial (RIIC)	16 KB (16 Kwords x 8 bits)	8 pin SOP

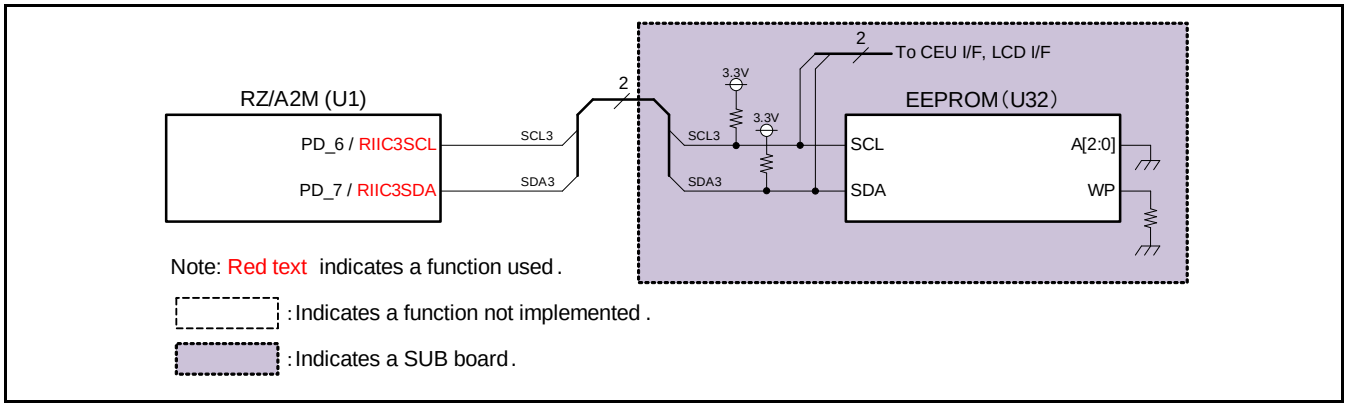


Figure 2.3.3 EEPROM Interface Block Diagram

2.4 USB Interface

RTK79210XXB00000BE is equipped with a USB series A port x 1 and USB Mini-B port x 1 as the standard configuration of USB connectors.

However, USB interface pins are shared by the Series A port pins and Mini-B port pins, therefore Series A port and Mini-B port cannot be used at the same time.

Figure 2.4.1 shows USB interface block diagram, and Table 2.4.1 shows the functions setting tables of DIP switches SW6-1 and SW6-3 for system setting.

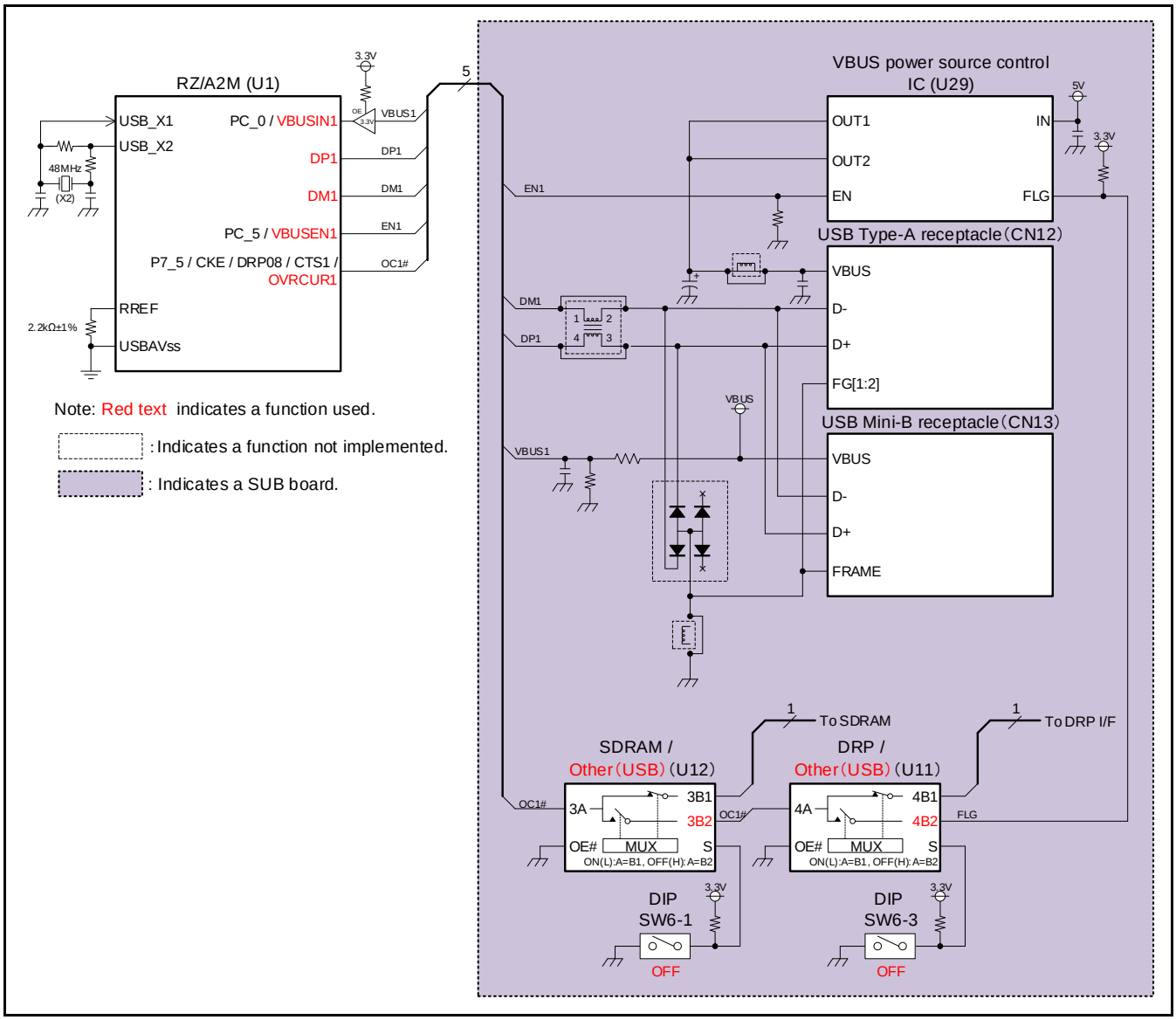


Figure 2.4.1 USB Interface Block Diagram

Table 2.4.1 Function Setting Table of DIP Switches SW6-1 and SW6-3 for System Setting

DIP switch	Function	
	ON	OFF
SW6-1	P7_5 is used as CKE pin.	P7_5 is used as OVRCUR1 pin (default setting).
SW6-3	P7_5 is used as DRP08 and CTS1 pin.	P7_5 is used as OVRCUR1 pin (default setting).

[Note] indicates setting functions.

2.5 Serial Interface

On the RTK79210XXB00000BE, channel 4 of serial communications interface built into the RZ/A2M on-chip FIFO (SCIFA) is connected to the serial port connector (USB Micro-B) (CN5) via the USB serial converter IC (RL78/G1C).

When equipping and connecting E1 connector (J1), be sure of the direction of the number 1 pin.

Figure 2.5.1 shows the serial interface block diagram, and Table 2.5.1 shows the function setting table of DIP switches SW6-1 and SW6-3 for system setting.

For performing serial communication between the USB connector of the host computer and the serial port connector (CN5) of RTK79210XXB00000BE, the driver of USB serial converter IC must be installed to the host computer.

Download and install the inf file onto the host computer from the following URL.

URL:TBD

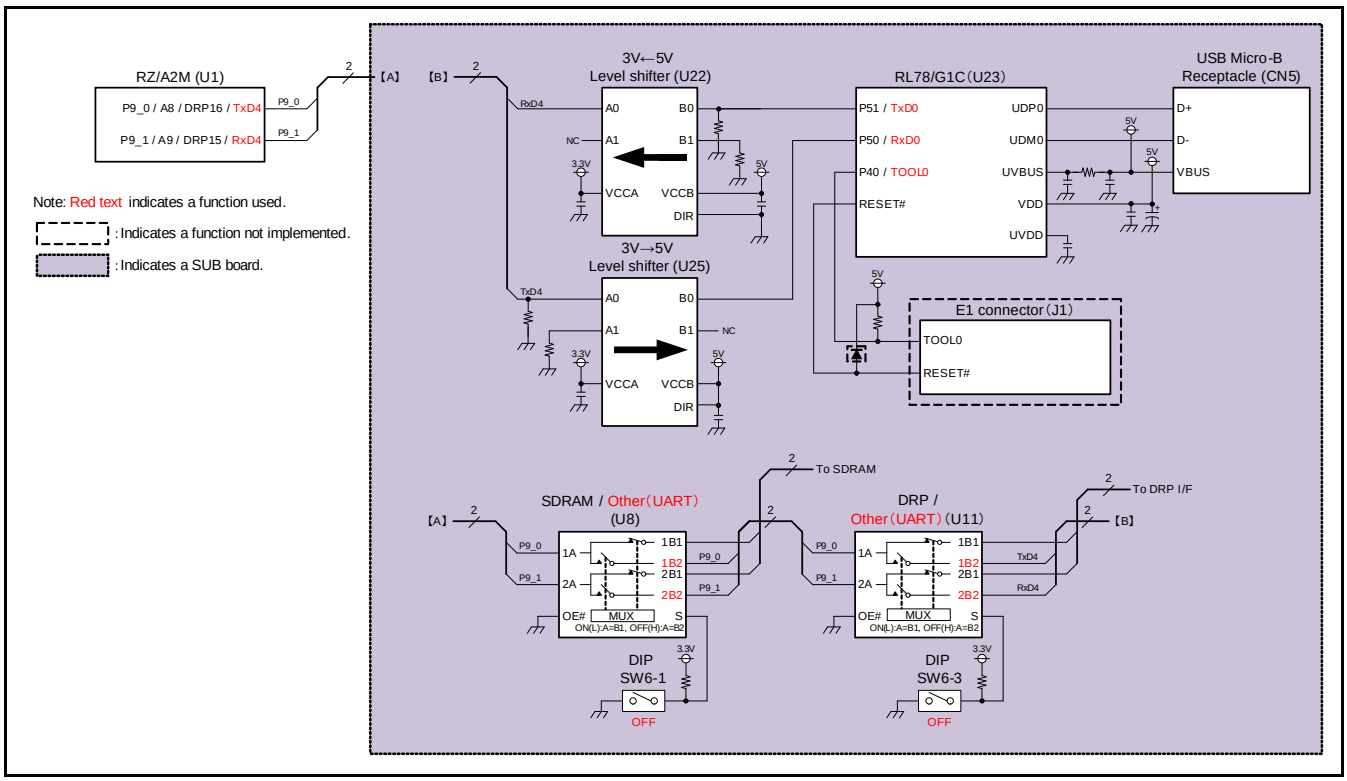


Figure 2.5.1 Serial Interface Block Diagram

Table 2.5.1 Function Setting Table of DIP Switches SW6-1 and SW6-3 for System Setting

DIP Switch	Function	
	ON	OFF
SW6-1	P9_[1 :0] is used as SDRAM control pin.	P9_[1 :0] is used as SCIFA pin (default setting).
SW6-3	P9_[1 :0] is used as DRP pin.	P9_[1 :0] is used as SCIFA pin (default setting).

[Note] indicates setting functions.

2.6 Interrupt Switches

RTK79210XXB00000BE is equipped with an RZ/A2M NMI and IRQ0 interrupt signal input push switches (NMI switch and IRQ0 switch).

The interrupt signal from IRQ0 RZ/A2M can be used to cancel the RZ/A2M deep standby mode. However, because the IRQ0pin is shared with the Ethernet PHY1 and Ethernet PHY2, when using the IRQ0 switch, the user must connect JP2 with the 2-pin of JP1.

Figure 2.6.1 shows an interrupt switch block diagram, and Table 2.6.1 shows a jumper JP1 function setting table.

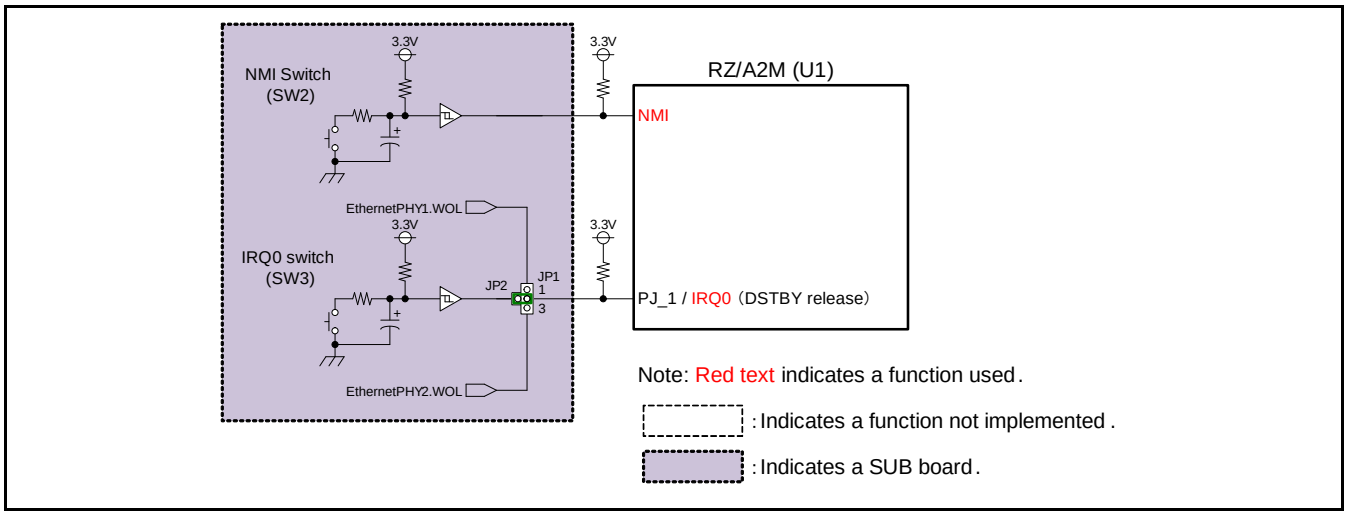


Figure 2.6.1 Interrupt Switch Block Diagram

Table 2.6.1 Function Settings for Jumper JP1

Jumper	1-2	2-3	2-JP2
JP1	PJ_1 is used as Ethernet PHY1 WOL signal interrupt pin.	PJ_1 is used as Ethernet PHY2 WOL signal interrupt pin.	PJ_1 used as IRQ0 switch (SW3) interrupt pin (default setting)

[Note] indicates setting functions.

2.7 Clock Configuration

RZ/A2M receives the following three types of clock inputs from the RZ/A2M CPU board.

- RZ/A2M input clock : 24 MHz
- RZ/A2M USB clock : 48 MHz
- RZ/A2M RTC clock : 32.768 kHz

RZ/A2M receives the following two clock inputs from RTK79210XXB00000BE.

- RZ/A2M audio clock : 11.2896MHz
- RZ/A2M VDC6 clock : 40MHz

Figure 2.7.1 shows clock configuration diagram, and Table 2.7.1 shows the function setting table of DIP switches SW6-4 and SW6-6 for system setting.

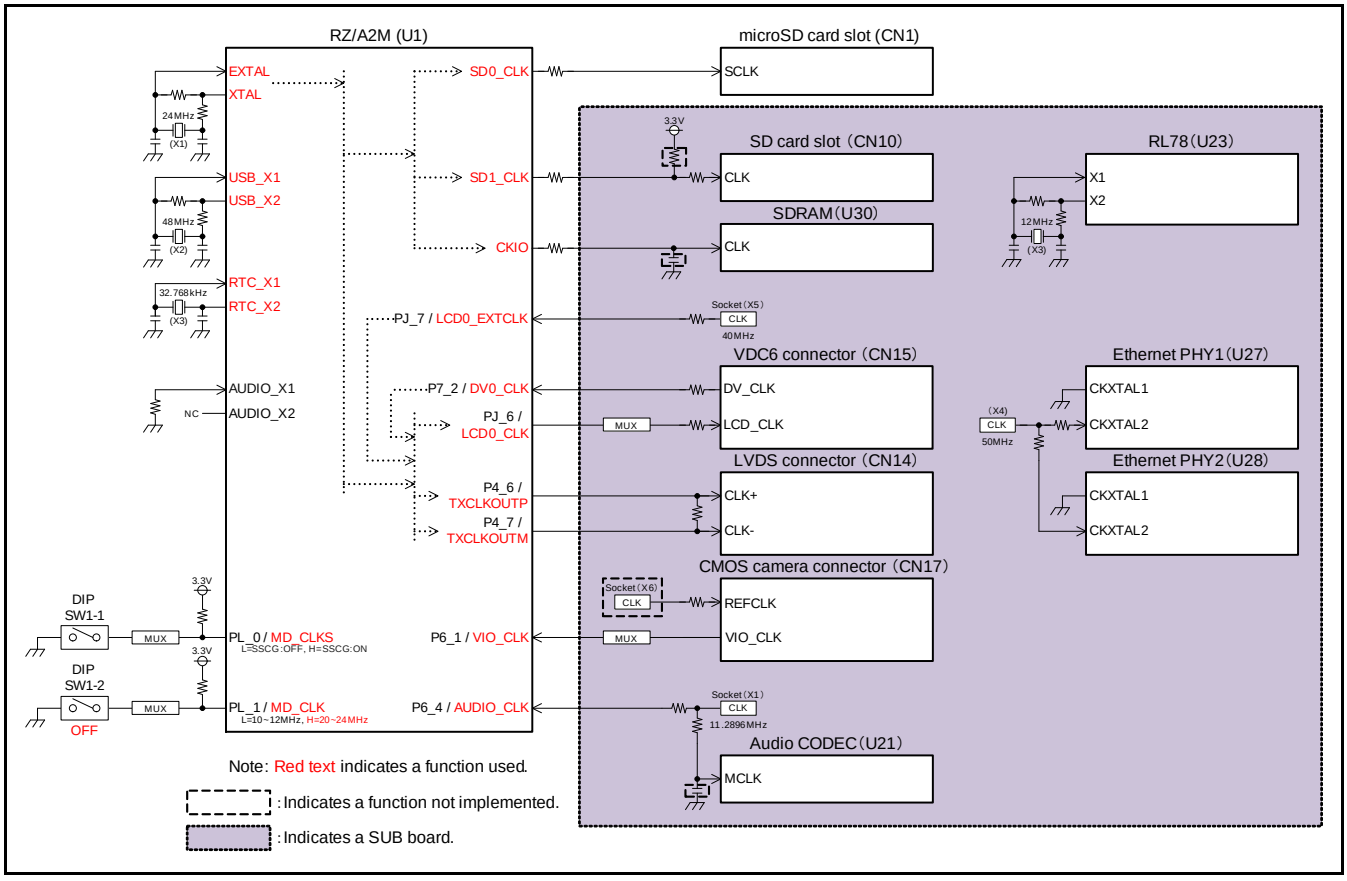


Figure 2.7.1 Clock Configuration Diagram

Table 2.7.1 Function Setting Table of DIP Switches SW6-4 and SW6-6 for System Setting

DIP Switch	Function	
	ON	OFF
SW6-4	P6_1 is used as RMII_TXDEN pin.	P6_1 is used as VIO_CLK input pin.*1 (default setting)
SW6-6	PJ_6 is used as LCD0_CLK output pin. PJ_7 is used as LCD0_EXTCLK input pin. (default setting)	PJ_6 is used as FCE pin. PJ_7 is used as NAF0 pin.

[Note] indicates setting functions.

*1 When using P6_1 as VIO_CLK input pin, an oscillator must be equipped to X6.

There is no reverse insertion guard on the oscillator socket, so be careful to insert in the direction of pin 1 when connecting.

2.8 Reset Control

On RTK79210XXB00000BE, a reset signal from the reset IC on the RZ/A2M CPU board is input to the Ethernet PHY1 (U27), Ethernet PHY2 (U28), and digital image input/output connector (CN15).

There are two types of system reset: power-on reset and switch-based reset.

Figure 2.8.1 shows a reset control block diagram.

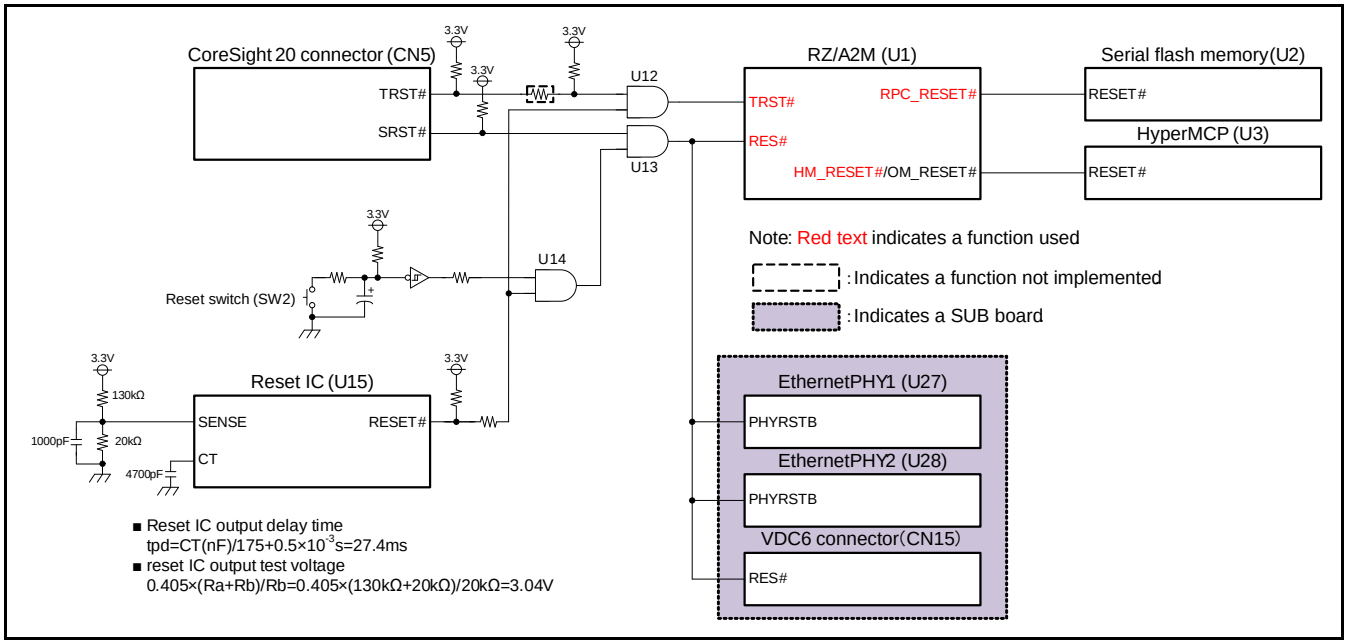


Figure 2.8.1 Reset Control Block Diagram

2.9 Power Voltage Configuration

RTK79210XXB00000BE uses 5V power supply, and the regulator on the RZ/A2M CPU board generates 3.3V power supply. 5V power supply can also be supplied from the RZ/A2M CPU board.

USB serial converter IC (U23) is operated by the VBUS power supply provided from USB Micro-B connector (CN5).

Figure 2.9.1 shows a power configuration diagram.

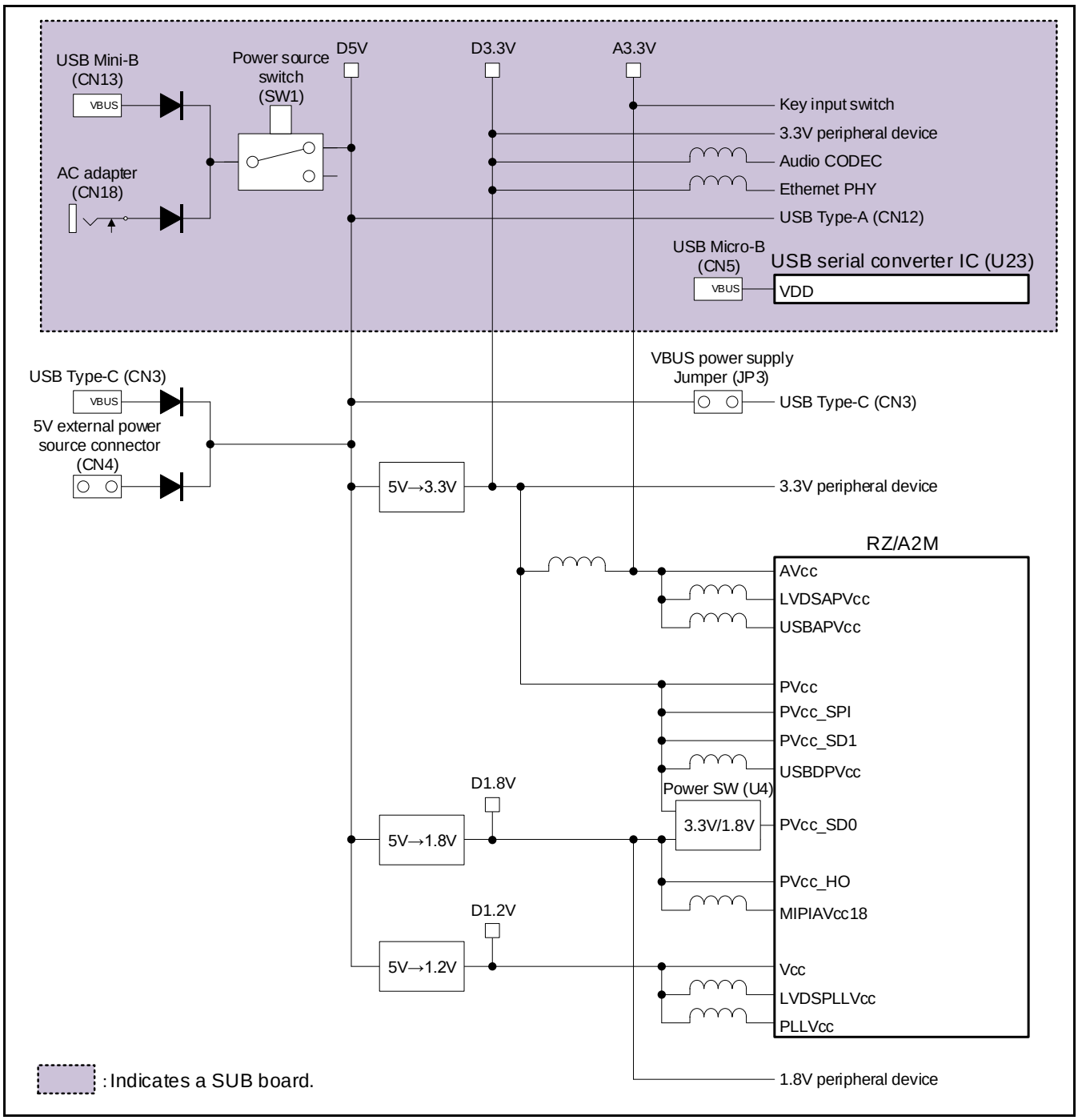


Figure 2.9.1 Power Configuration Diagram

2.10 Audio Interface

RTK79210XXB00000BE is equipped with a Cirrus audio CODEC WM8978 × 1 for audio interface. The WM8978 register control is performed on the channel 0 of the RZ/A2M on-chip Renesas serial peripheral interface (RSPI), and the input/output control for audio data is performed on the channel 0 of the RZ/A2M on-chip serial sound interface (SSIF-2).

Figure 2.10.1 shows the audio interface block diagram, and Table 2.10.1 shows the function setting table of DIP switches SW6-1 and SW6-2 for system setting.

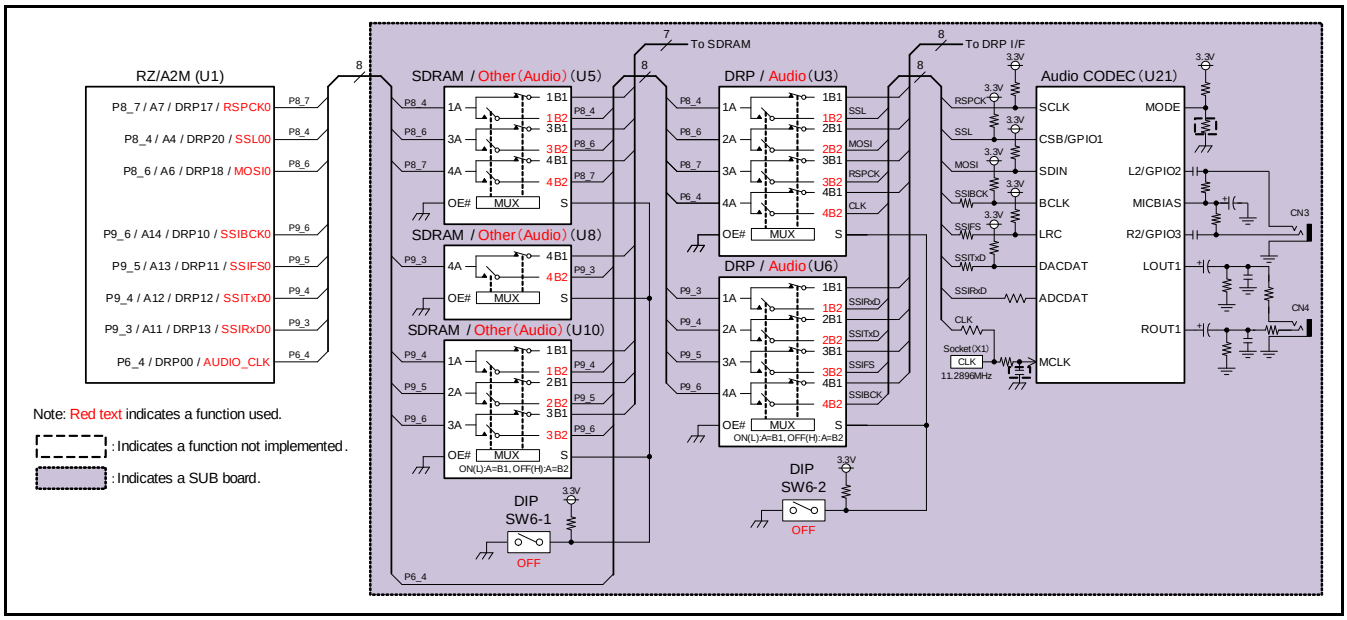


Figure 2.10.1 Audio Interface Block Diagram

Table 2.10.1 Function Setting Table of DIP Switches SW6-1 and SW6-2 for System Setting

DIP switch	Function	
	ON	OFF
SW6-1	P8_4 and P8_[7 :6], P9_[6 :3] are used as SDRAM control pins.	P8_4 and P8_[7 :6], P9_[6 :3] are used as audio interface pins (default settings).
SW6-2	P8_4 and P8_[7 :6], P6_4, P9_[6 :3] are used as DRP pins.	P8_4 and P8_[7 :6], P6_4, P9_[6 :3] used as audio interface pins (default settings).

[Note] indicates setting functions.

2.11 CMOS Camera Interface

RZ/A2M is equipped with an on-chip capture engine unit (CEU) that captures digital image data externally input, and transfers the data to memory. On RTK79210XXB00000BE, CEU pins of RZ/A2M connect with 26 pin MIL pitch connector to enable connection with various CMOS cameras.

X6 can be connected to an oscillator to input a sampling clock externally for the CMOS camera.

A pull-up resistor for I2C-bus is already mounted on RTK79210XXB00000BE, therefore it is not needed for the CMOS camera side.

Figure 2.11.1 shows CMOS camera interface block diagram, and Table 2.11.1 shows a function setting table of DIP switch SW6-4 for system setting.

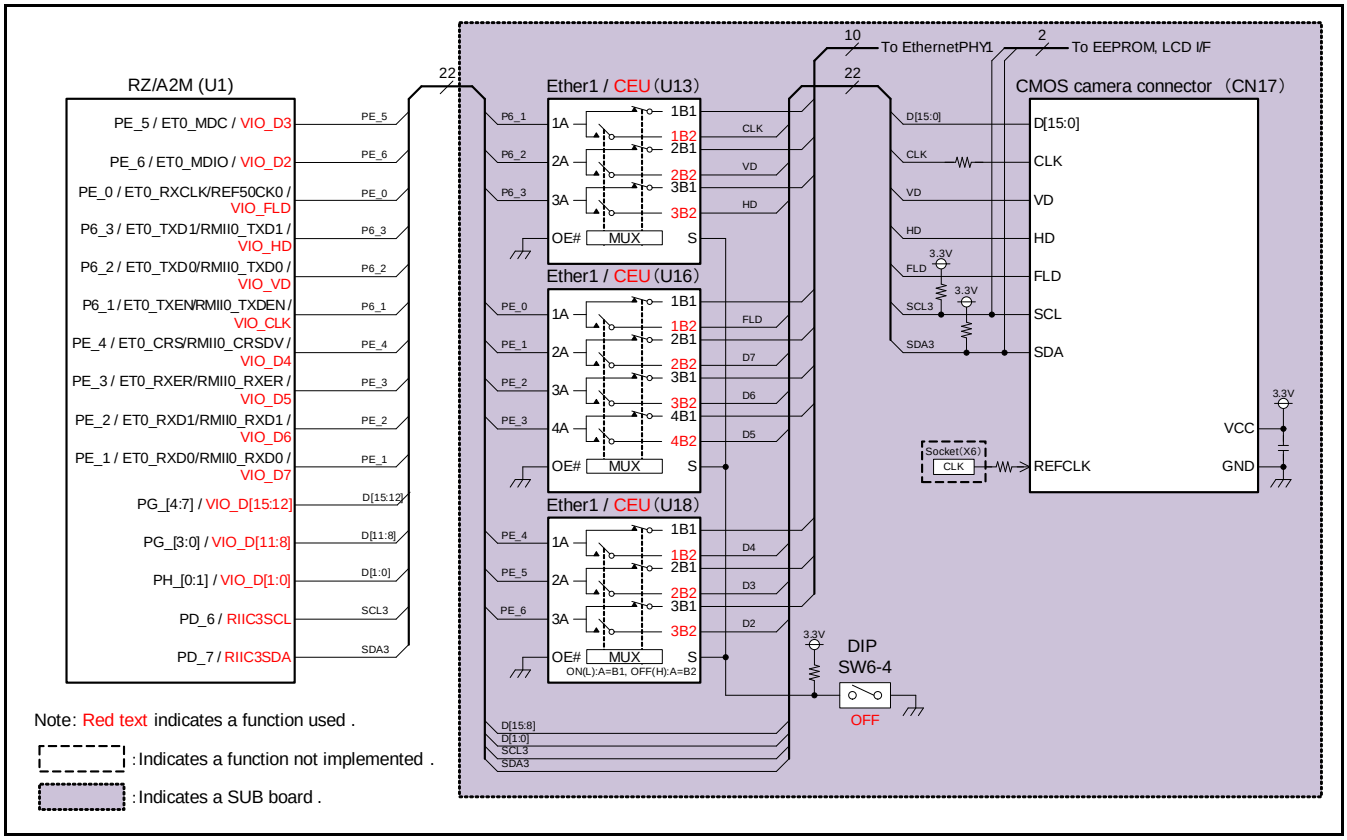


Figure 2.11.1 CMOS Camera Interface Block Diagram

Table 2.11.1 Function Setting Table of DIP Switch SW6-4 for System Setting

DIP switch	Function	
	ON	OFF
SW6-4	P6_[3 :1] and PE_[6 :0] are used as Ethernet PHY1 control pins.	P6_[3 :1] and PE_[6 :0] are used as CEU pins. (default setting)

[Note] indicates setting functions.

2.12 SD Card Interface

RTK79210XXB00000BE is equipped with 4-bit SD card slot, and it connects to the channel 1 of the RZ/A2M on-chip SD/MMC host interface (SDHI).

Figure 2.12.1 shows the SD card interface block diagram.

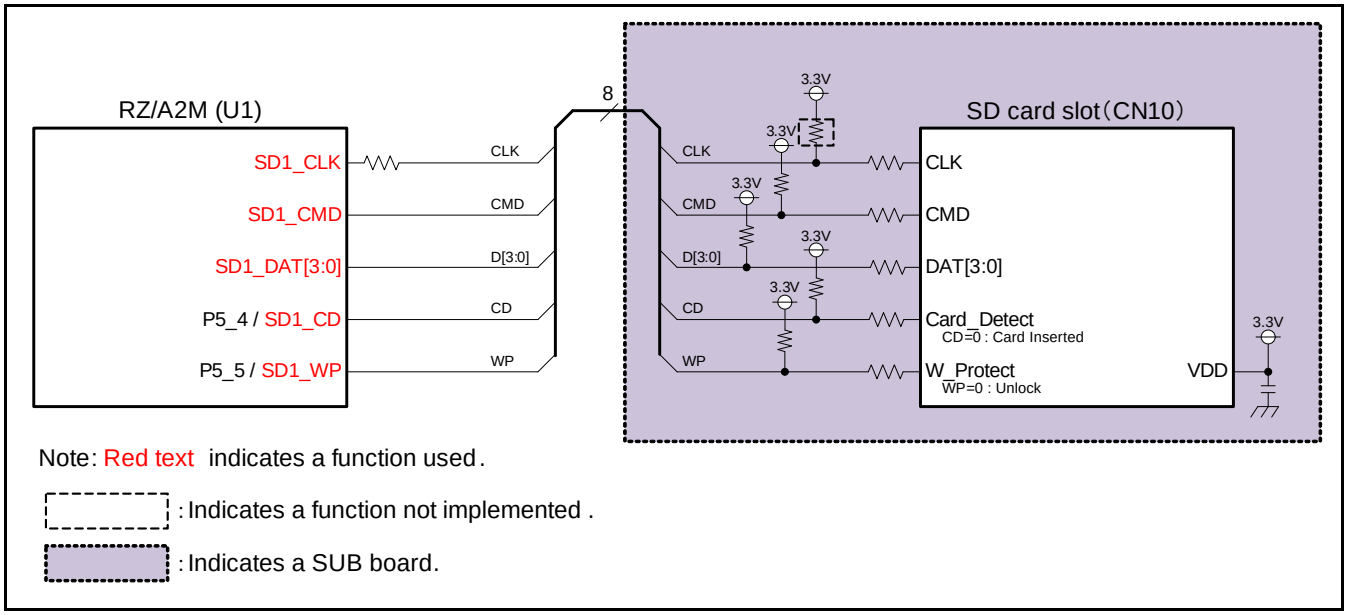


Figure 2.12.1 SD Card Interface Block Diagram

2.13 LAN Interface

RTK79210XXB00000BE is equipped with Realtek Ethernet PHY RTL8201FL-VB-CG × 2, which can communicate with the channel 0 and channel 1 of the RZ/A2M on-chip ethernet controller (ETHERC).

The Ethernet PHY incorporates the Wake-On-Lan (WOL) functionality, and outputs a WOL signal when a Magic Packet has been detected, allowing the deep standby mode of RZ/A2M to be canceled.

Figure 2.13.1 shows the LAN interface (channel 0) block diagram, Figure 2.13.2 shows the LAN interface (channel 1) block diagram, Table 2.13.1 shows the RZ/A2M CPU board port L function switching table, Table 2.13.2 shows the function setting table of DIP switch SW6-4 for system setting, Table 2.13.3 and Table 2.13.5 show the function setting table of jumper JP1, and Table 2.13.4 shows the function setting table of DIP switch SW6-5 for system setting.

Table 2.13.1 RZ/A2M CPU Board Port L Function Switching Table

Pin	Function	
	High	Low
PD_0	PL_[3 :0] is used as system setting pin.	Use PL_[3 :0] is used as RQ input pin.

[Note] indicates setting functions.

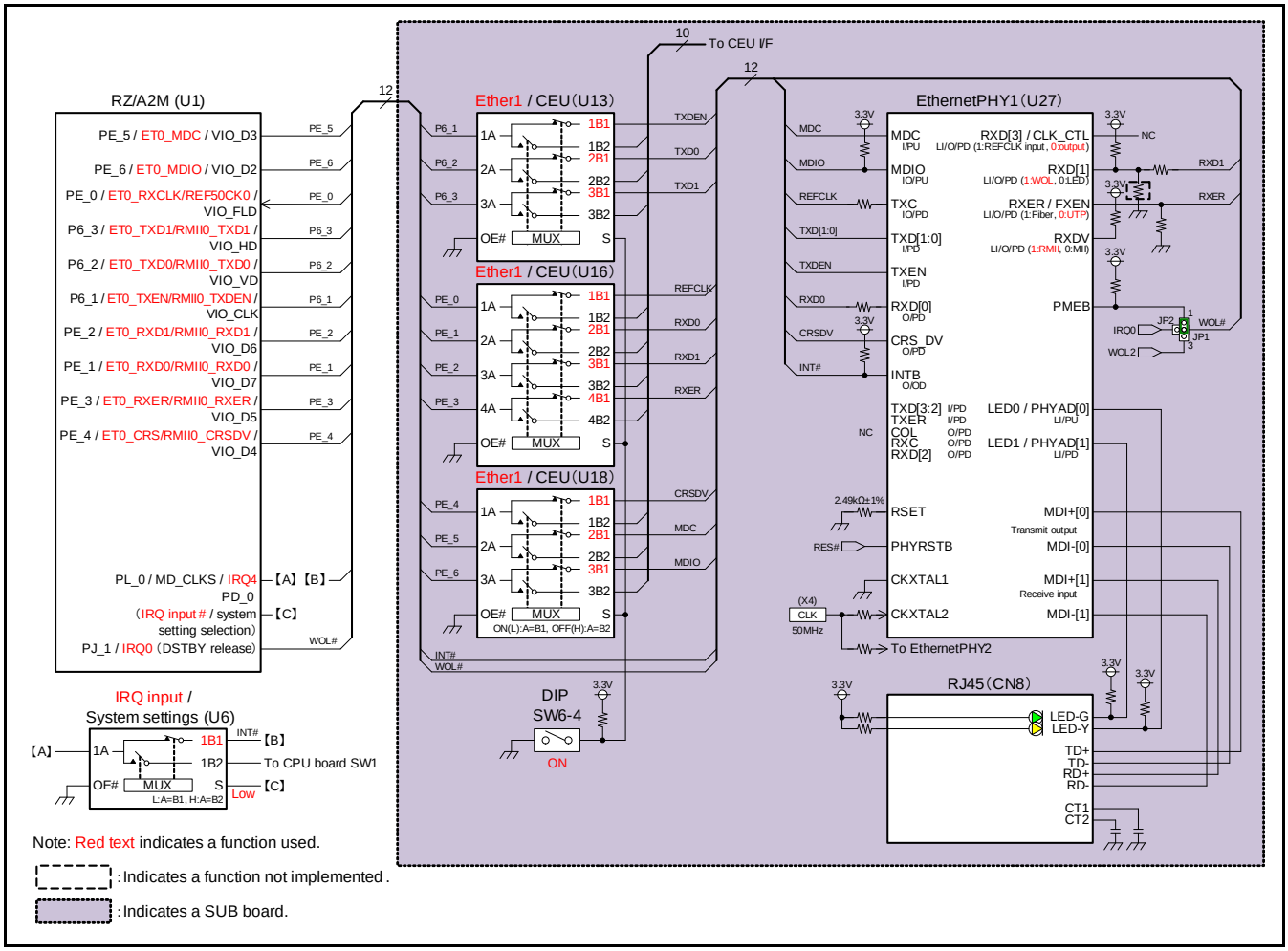


Figure 2.13.1 LAN Interface (Channel 0) Block Diagram

Table 2.13.2 Function Setting Table of DIP Switch SW6-4 for System Setting

DIP switch	Function	
	ON	OFF
SW6-4	P6_[3 :0] and PE_[6 :0] are used as Ethernet PHY1 control pins.	P6_[3 :0] and PE_[6 :0] are used as CEU pins. (default setting)

[Note] indicates setting functions.

Table 2.13.3 Function Setting Table of Jumper JP1

Jumper	1-2	2-3	2-JP2
JP1	PJ_1 is used as Ethernet PHY1 signal interrupt pin.	PJ_1 is used as Ethernet PHY2 signal interrupt pin.	PJ_1 is used as IRQ0 switch (SW3) interrupt pin. (default setting)

[Note] indicates setting functions.

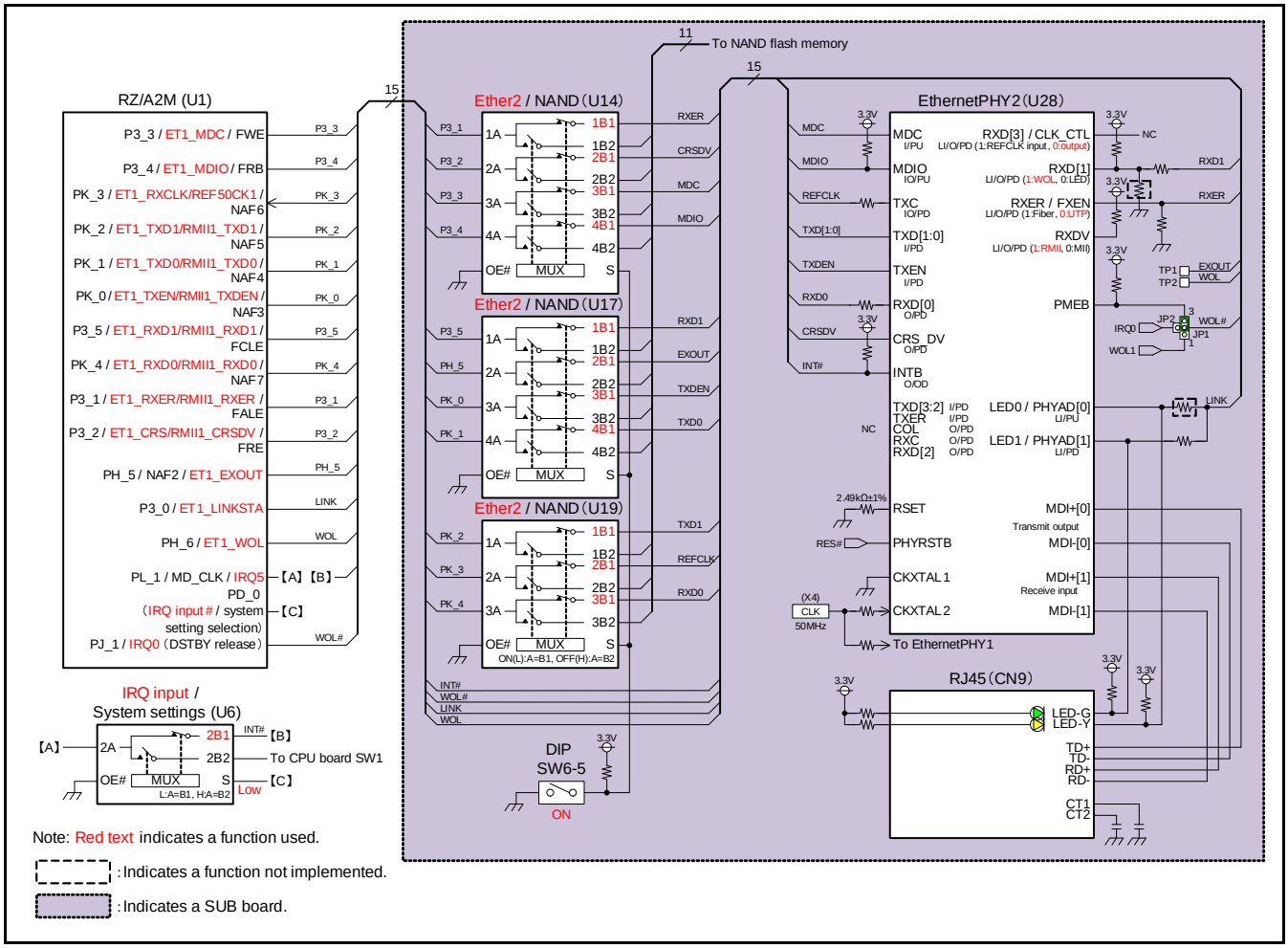


Figure 2.13.2 LAN Interface (channel 1) Block Diagram

Table 2.13.4 Function Setting Table of DIP Switch SW6-5 for System Setting

DIP switch	Function	
	ON	OFF
SW6-5	P3_[5 :1] and PH_5, PK_[4 :0] are used as Ethernet PHY2 control pins (default settings).	P3_[5 :1] and PH_5, PK_[4 :0] are used as FLCTL pins.

[Note] indicates setting functions.

Table 2.13.5 Function Setting Table of Jumper JP1

Jumper	1-2	2-3	2-JP2
JP1	PJ_1 is used as Ethernet PHY1 signal interrupt pin.	PJ_1 is used as Ethernet PHY2 signal interrupt pin.	PJ_1 is used as IRQ0 switch (SW3) interrupt pin (default setting).

[Note] indicates setting functions.

2.14 Key Input Switches

Port P5_6 is set as an analog input pin (AN006), and can be used as a key input switch through an A/D converter (ADC)

Figure 2.14.1 shows the key input switch block diagram, and Table 2.14.1 shows the AD input pin voltage and AD value when each switch is pressed.

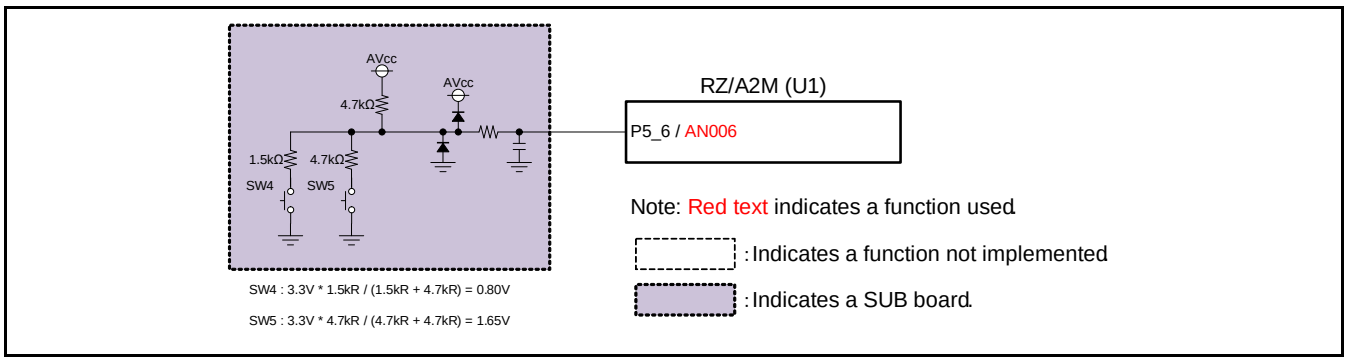


Figure 2.14.1 Key Input Switch Block Diagram

Table 2.14.1 AD Input Pin Voltage and AD Values When Switch Is Pressed

Switch	Pin voltage (V)	8 bit AD value	10 bit AD value	12 bit AD value
SW4	0.80	62	248	991
SW5	1.65	128	512	2048

[Note] Calculated at AVcc=3.3V, and AVss= 0V. Errors of resistor and voltage are not included.

2.15 VDC6 Interface

RZ/A2M has a digital image signal input pin (DV pin) which supports YCbCr422, YCbCr444, RGB888, RGB666, and RGB565 images. In addition, there is a digital image signal output pin (LCD pin) which supports a maximum image size of 1999 pixels (horizontal) by 2035 lines (vertical). On the RTK79210XXB00000BE, there is a 50 pin MIL connector to connect the DV pins and LCD pins of RZ/A2M.

Figure 2.15.1 shows the VDC6 interface block diagram, and Table 2.15.1 shows the function setting table of DIP switches SW6-6 and SW6-7 for system setting.

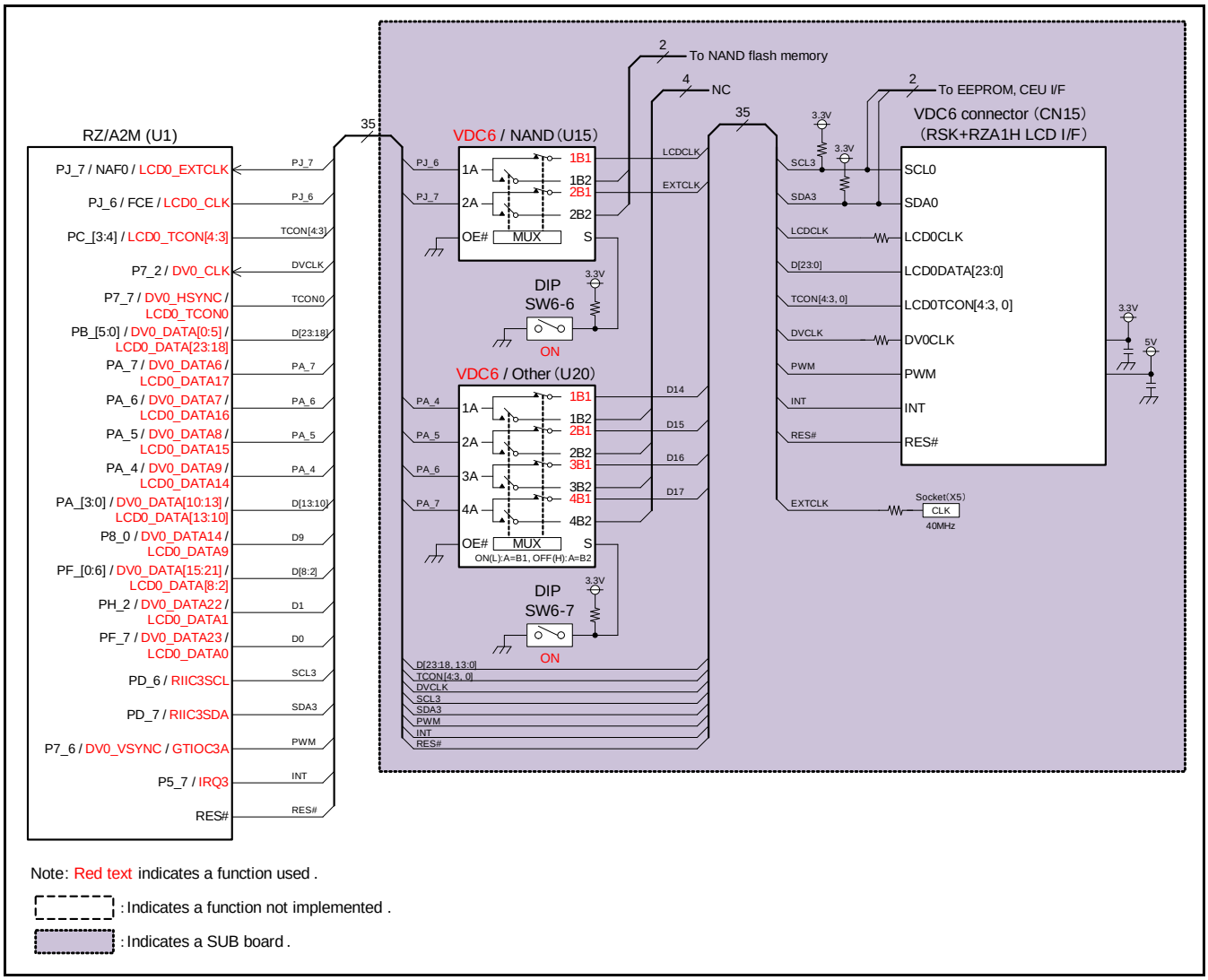


Figure 2.15.1 VDC6 Interface Block Diagram

Table 2.15.1 Function Setting Table of DIP Switches SW6-6 and SW6-7 for System Setting

DIP switch	Function	
	ON	OFF
SW6-6	PJ_[7 :6] is used as VDC6 pin (default setting).	PJ_[7 :6] is used as FLCTL pin.
SW6-7	PA_[7 :4] is used as VDC6 pin (default setting).	NC

[Note] indicates setting functions.

2.16 LVDS Interface

RTK79210XXB00000BE is equipped with a 1.25mm pitch 20 pin connector, which allows connection with the RZ/A2M LVDS interface. There is also a connector for the LVDS backlight.

Figure 2.16.1 shows the LVDS interface block diagram.

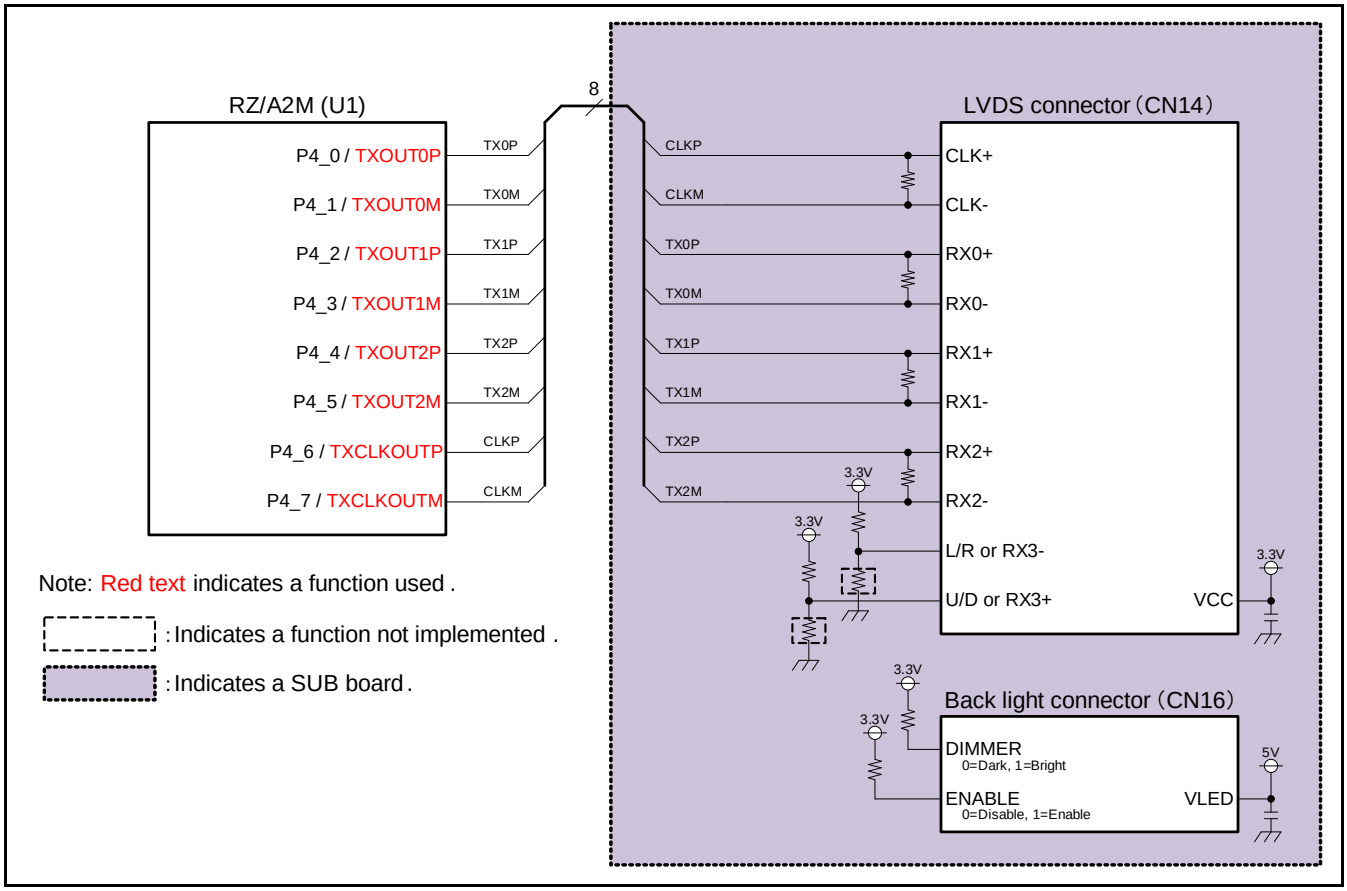


Figure 2.16.1 LVDS Interface Block Diagram

2.17 DRP Interface

RTK79210XXB00000BE is equipped with a 40 pin MIL connector, which allows interface with the RZ/A2M DRP interface.

Figure 2.17.1 shows the DRP interface block diagram, and Table 2.17.1 shows the function setting table of DIP switches SW6-1, SW6-2, and SW6-3 for system setting.

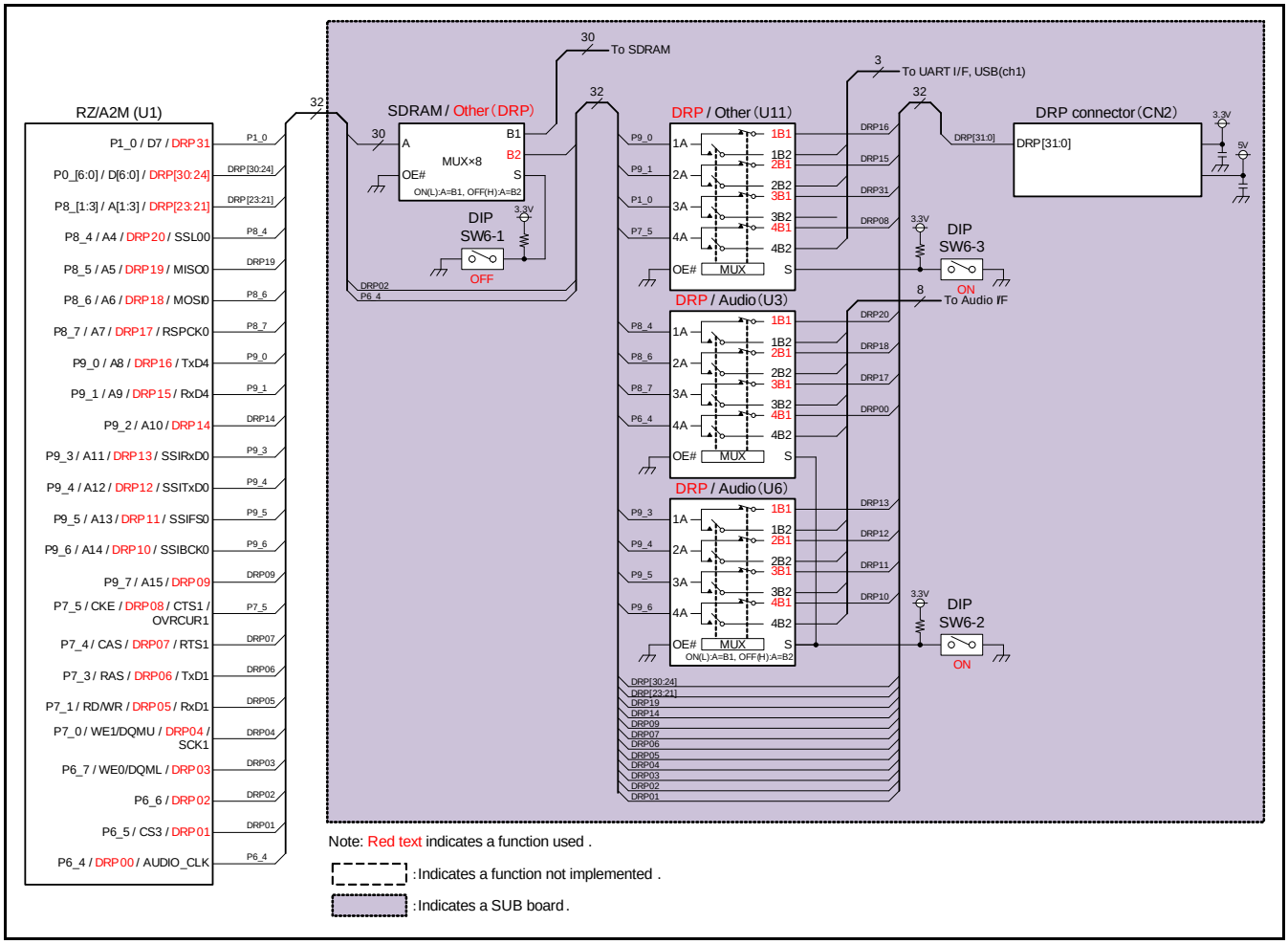


Figure 2.17.1 DRP Interface Block Diagram

Table 2.17.1 Function Setting Table of DIP Switches SW6-1, SW6-2, and SW6-3 for System Setting

DIP switch	Function	
	ON	OFF
SW6-1	P1_0 and P0_[6 :0], P8_[7 :1], P9_[7 :0], P7_[5 :3], P7_[1 :0], P6_7, P6_5 are used as SDRAM control pins.	P1_0 and P0_[6 :0], P8_[7 :1], P9_[7 :0], P7_[5 :3], P7_[1 :0], P6_7, P6_5 are used as DRP pins (default setting).
SW6-2	P8_4 and P8_[7 :6], P6_4, P9_[6 :3] are used as DRP pins.	P8_4 and P8_[7 :6], P6_4, P9_[6 :3] are used as audio interface pins (default settings).
SW6-3	P9_[1 :0] and P1_0, P7_5 are used as DRP pins.	P9_[1 :0] and P7_5 are used as UART or USB interface pins (default settings).

[Note] indicates setting functions.

3. Operating specifications

3.1 Overview of Connector

Figure 3.1.1 and Figure 3.1.2 show connector layout diagrams for RTK79210XXB00000BE.

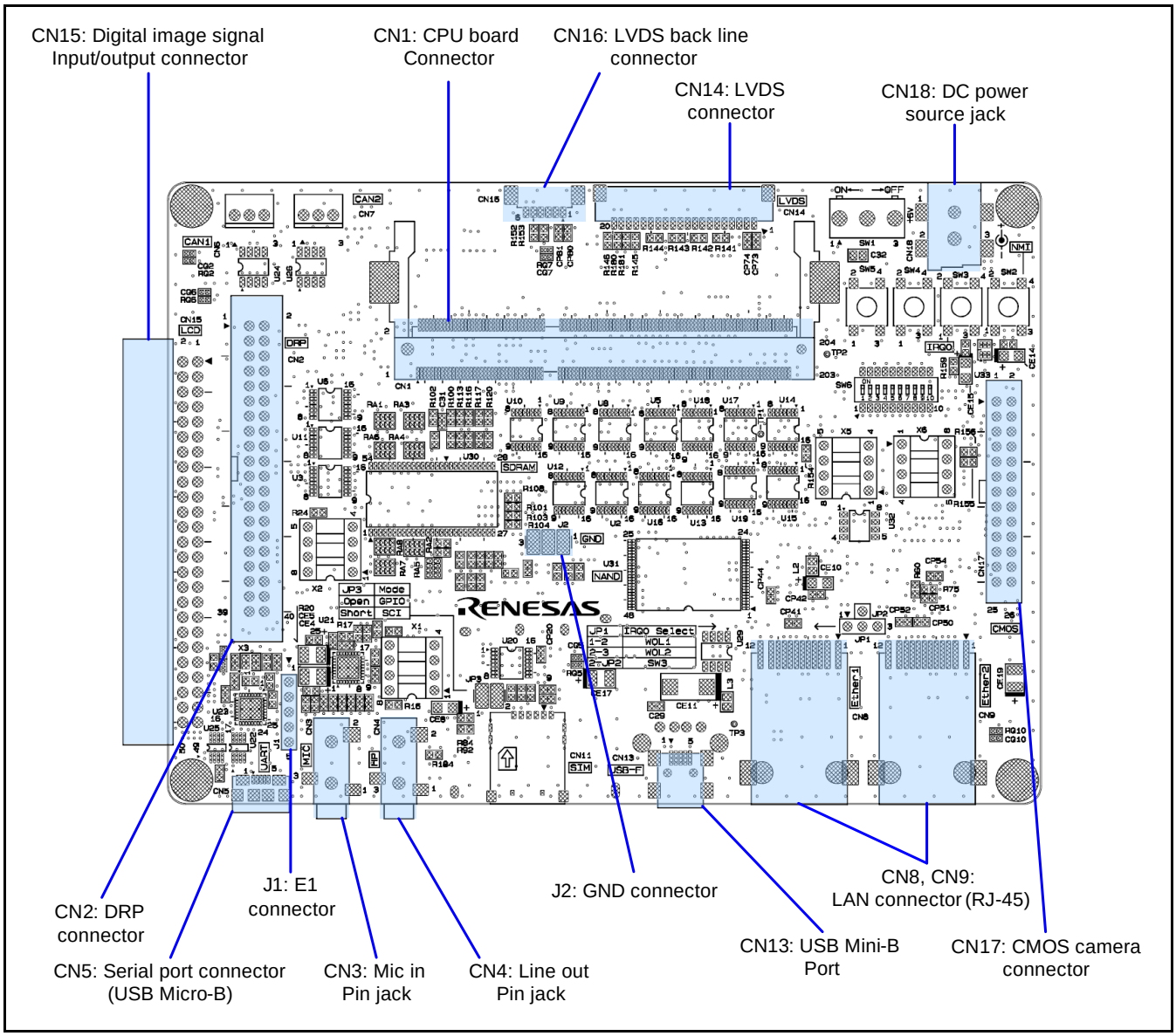


Figure 3.1.1 RTK79210XXB00000BE Connector Layout Diagram (C Side Top View)

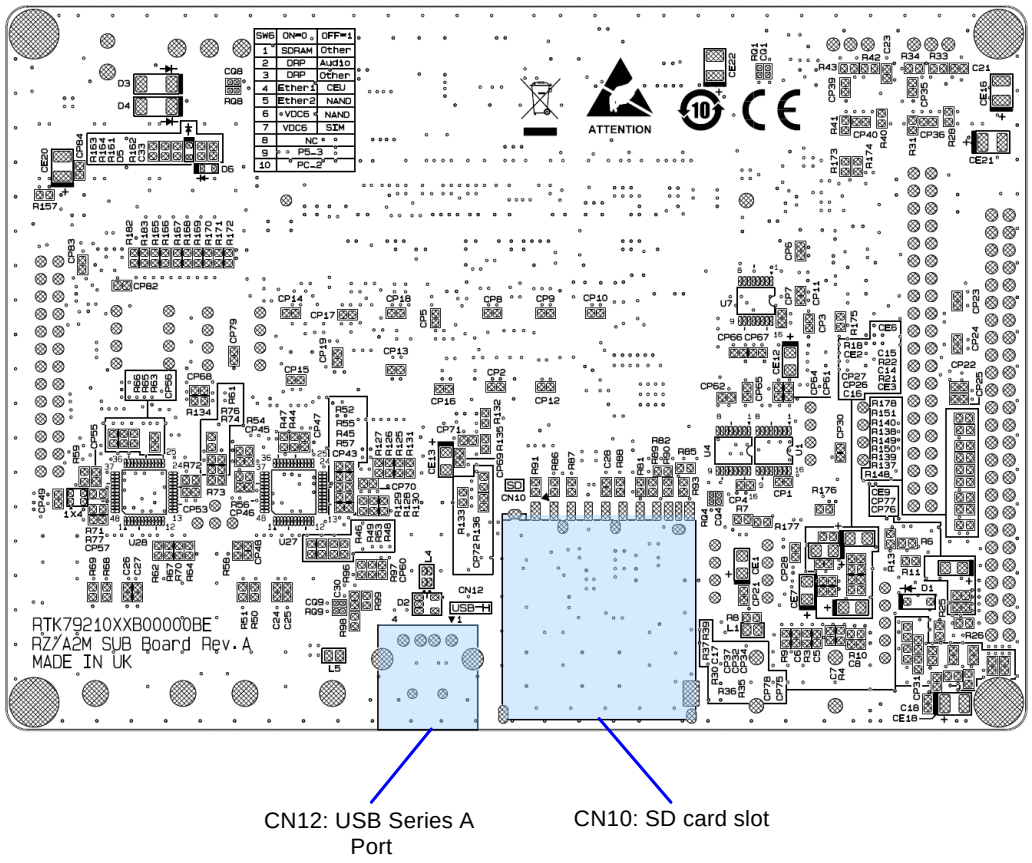


Figure 3.1.2 RTK79210XXB00000BE Connector Layout Diagram (S Side Top View)

3.1.1 CPU Board Connector (CN1)

The RTK79210XXB00000BE can be connected to the RZ/A2M CPU board RTK7921053C00000BE via the CPU board connector (CN1).

Figure 3.1.3 shows the CPU board connection pin layout diagram, and Table 3.1.1 to Table 3.1.3 show CPU board connector pin layout table.

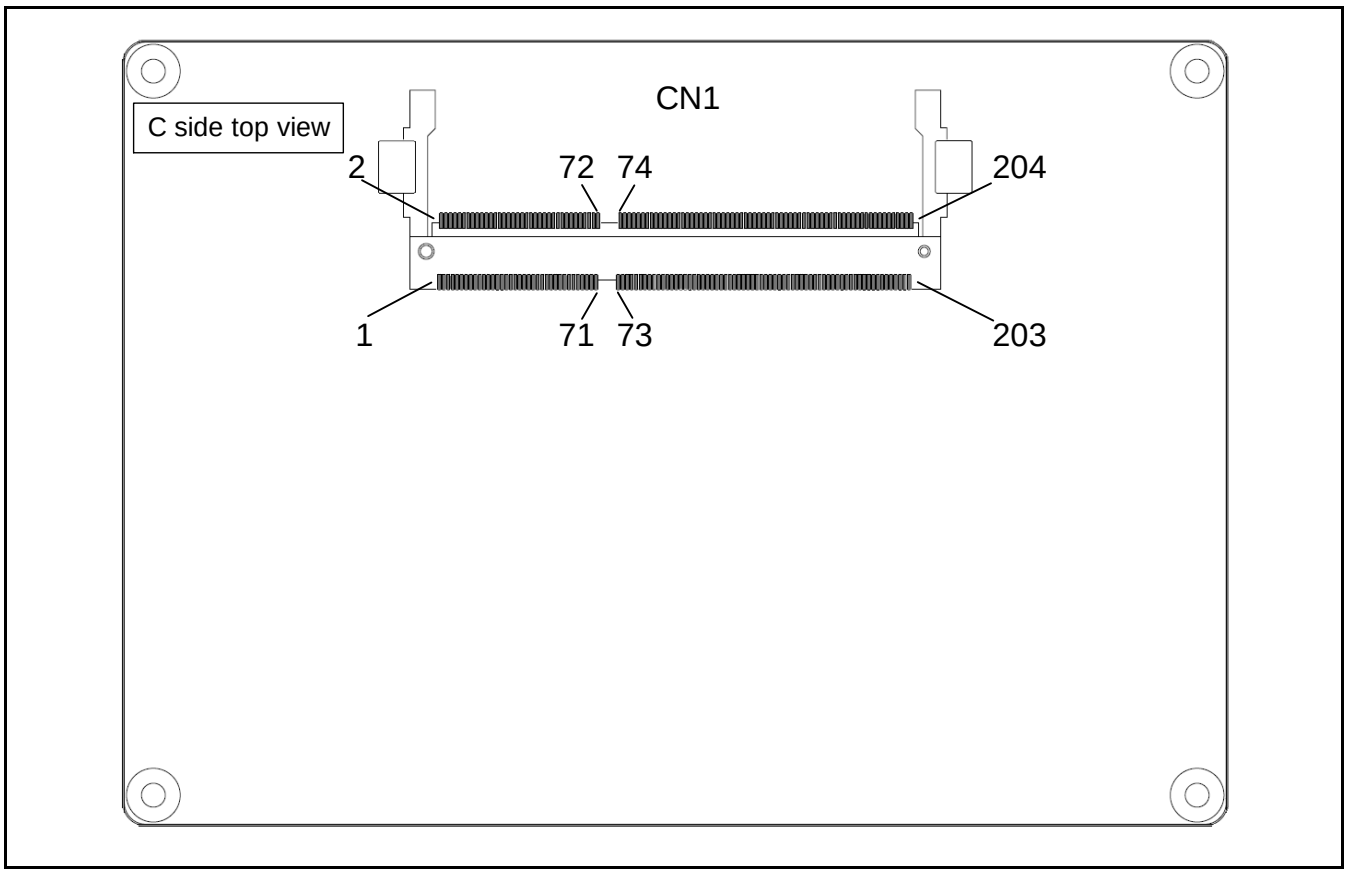


Figure 3.1.3 CPU Board Connector (CN1) Pin Layout Diagram

Table 3.1.1 CPU Board Connector (CN1) Pin Layout Table (1)

Pin	Signal name	Pin	Signal name
1	D5V	2	D5V
3	D5V	4	D5V
5	D5V	6	D5V
7	RES#	8	PC_5 / VBUSEN1
9	D3.3V	10	PC_3 / LCD0_TCON4
11	D3.3V	12	AVcc
13	D3.3V	14	P5_6 / AN006
15	P5_3	16	AVss
17	P5_5 / SD1_WP	18	P5_4 / SD1_CD
19	P5_7 / IRQ3	20	PC_4 / LCD0_TCON3
21	D3.3V	22	Vss
23	P6_7 / WE0/DQML / DRP03	24	SD1_CLK
25	P7_0 / WE1/DQMU / DRP04 / SCK1	26	Vss
27	D3.3V	28	SD1_CMD
29	SD1_DAT1	30	Vss
31	SD1_DAT2	32	SD1_DAT3
33	SD1_DAT0	34	Vss
35	Vss	36	P6_4 / DRP00 / AUDIO_CLK
37	P7_2 / DV0_CLK	38	Vss
39	Vss	40	PB_4 / DV0_DATA1 / LCD0_DATA22
41	P7_3 / RAS / DRP06 / TxD1	42	P9_3 / A11 / DRP13 / SSIRxD0
43	PG_2 / VIO_D10	44	P7_7 / DV0_HSYNC / LCD0_TCON0
45	P7_5 / CKE / DRP08 / CTS1 / OVRCUR1	46	Vss
47	Vss	48	PL_1 / MD_CLK / IRQ5
49	P9_6 / A14 / DRP10 / SSIBCK0	50	PL_0 / MD_CLKS / IRQ4
51	Vss	52	Vss
53	P7_6 / DV0_VSYNC / GTIOC3A	54	CKIO
55	P9_5 / A13 / DRP11 / SSIFS0	56	Vss
57	PB_5 / DV0_DATA0 / LCD0_DATA23	58	PD_7 / RIIC3SDA
59	P9_2 / A10 / DRP14	60	PD_6 / RIIC3SCL
61	PB_3 / DV0_DATA2 / LCD0_DATA21	62	Vss
63	PB_1 / DV0_DATA4 / LCD0_DATA19	64	PB_0 / DV0_DATA5 / LCD0_DATA18
65	Vss	66	PB_2 / DV0_DATA3 / LCD0_DATA20
67	PA_6 / DV0_DATA7 / LCD0_DATA16	68	PA_3 / DV0_DATA10 / LCD0_DATA13
69	PA_4 / DV0_DATA9 / LCD0_DATA14	70	Vss
71	PA_5 / DV0_DATA8 / LCD0_DATA15	72	PG_0 / VIO_D8

[Note] : 5V power source, : 3.3V power source, : GND

Table 3.1.2 CPU Board Connector (CN1) Pin Layout Table (2)

Pin	Signal name	Pin	Signal name
73	PE_1 / ET0_RXD0/RMII0_RXD0 / VIO_D7	74	PA_2 / DV0_DATA11 / LCD0_DATA12
75	Vss	76	PA_7 / DV0_DATA6 / LCD0_DATA17
77	PA_0 / DV0_DATA13 / LCD0_DATA10	78	PE_2 / ET0_RXD1/RMII0_RXD1 / VIO_D6
79	PE_3 / ET0_RXER/RMII0_RXER / VIO_D5	80	PA_1 / DV0_DATA12 / LCD0_DATA11
81	Vss	82	Vss
83	P9_1 / A9 / DRP15 / RxD4	84	P9_0 / A8 / DRP16 / TxD4
85	Vss	86	P8_0 / DV0_DATA14 / LCD0_DATA9
87	P8_7 / A7 / DRP17 / RSPCK0	88	PF_1 / DV0_DATA16 / LCD0_DATA7
89	Vss	90	PF_0 / DV0_DATA15 / LCD0_DATA8
91	PE_4 / ET0_CRS/RMII0_CRSDV / VIO_D4	92	P8_5 / A5 / DRP19 / MISO0
93	PF_2 / DV0_DATA17 / LCD0_DATA6	94	Vss
95	P8_6 / A6 / DRP18 / MOSI0	96	DP1
97	P8_3 / A3 / DRP21	98	DM1
99	Vss	100	Vss
101	P8_4 / A4 / DRP20 / SSL00	102	PE_0 / ET0_RXCLK/REF50CK0 / VIO_FLD
103	PE_5 / ET0_MDC / VIO_D3	104	Vss
105	PH_0 / VIO_D1	106	P6_2 / ET0_TXD0/RMII0_TXD0 / VIO_VD
107	PE_6 / ET0_MDIO / VIO_D2	108	PF_6 / DV0_DATA21 / LCD0_DATA2
109	Vss	110	PK_0 / ET1_TXEN/RMII1_TXDEN / NAF3
111	P6_3 / ET0_TXD1/RMII0_TXD1 / VIO_HD	112	P9_4 / A12 / DRP12 / SSITxD0
113	PF_4 / DV0_DATA19 / LCD0_DATA4	114	Vss
115	PF_5 / DV0_DATA20 / LCD0_DATA3	116	PG_1 / VIO_D9
117	Vss	118	P9_7 / A15 / DRP09
119	P6_1 / ET0_TXEN/RMII0_TXDEN / VIO_CLK	120	P7_4 / CAS / DRP07 / RTS1
121	Vss	122	Vss
123	P7_1 / RD/WR / DRP05 / RxD1	124	PF_3 / DV0_DATA18 / LCD0_DATA5
125	P6_0	126	PH_1 / VIO_D0
127	P6_6 / DRP02	128	P8_1 / A1 / DRP23
129	PG_3 / VIO_D11	130	Vss
131	Vss	132	PK_3 / ET1_RXCLK/REF50CK1 / NAF6
133	PK_2 / ET1_TXD1/RMII1_TXD1 / NAF5	134	Vss
135	P6_5 / CS3 / DRP01	136	PF_7 / DV0_DATA23 / LCD0_DATA0
137	PK_1 / ET1_TXD0/RMII1_TXD0 / NAF4	138	Vss
139	Vss	140	PJ_7 / NAF0 / LCD0_EXTCLK
141	P8_2 / A2 / DRP22	142	Vss
143	PH_2 / DV0_DATA22 / LCD0_DATA1	144	P0_0 / D0 / DRP24
145	Vss	146	P0_4 / D4 / DRP28
147	PJ_6 / FCE / LCD0_CLK	148	P0_3 / D3 / DRP27
149	Vss	150	P0_6 / D6 / DRP30
151	P0_1 / D1 / DRP25	152	Vss
153	P0_5 / D5 / DRP29	154	P3_2 / ET1_CRS/RMII1_CRSDV / FRE
155	P0_2 / D2 / DRP26	156	P3_5 / ET1_RXD1/RMII1_RXD1 / FCLE

[Note] : 5V power source, : 3.3V power source, : GND

Table 3.1.3 CPU Board Connector (CN1) Pin Layout Table (3)

Pin	Signal name	Pin	Signal name
157	Vss	158	Vss
159	PJ_1 / IRQ0	160	P1_0 / D7 / DRP31
161	PH_5 / NAF2 / ET1_EXOUT	162	Vss
163	PH_6 / ET1_WOL	164	PK_4 / ET1_RXD0/RMII1_RXD0 / NAF7
165	Vss	166	P3_1 / ET1_RXER/RMII1_RXER / FALE
167	PK_5 / NAF1	168	Vss
169	PG_4 / VIO_D15	170	P4_0 / TXOUT0P
171	PG_6 / VIO_D13	172	P4_1 / TXOUT0M
173	P1_4 / D11	174	Vss
175	Vss	176	P4_4 / TXOUT2P
177	P3_3 / ET1_MDC / FWE	178	P4_5 / TXOUT2M
179	P1_1 / D8	180	Vss
181	PG_7 / VIO_D12	182	P4_2 / TXOUT1P
183	PG_5 / VIO_D14	184	P4_3 / TXOUT1M
185	Vss	186	Vss
187	P3_4 / ET1_MDIO / FRB	188	P4_6 / TXCLKOUTP
189	P1_3 / D10	190	P4_7 / TXCLKOUTM
191	P3_0 / ET1_LINKSTA	192	Vss
193	P2_1 / D13	194	PC_0 / VBUSIN1
195	Vss	196	P1_2 / D9
197	PC_1	198	P2_2 / D14
199	P2_3 / D15	200	P2_0 / D12
201	Vss	202	PC_2
203	NMI	204	Vss

[Note] : 5V power source, : 3.3V power source, : GND

3.1.2 DRP Connector (CN2)

RTK79210XXB00000BE is equipped with a DRP connector (CN2).

Figure 3.1.4 shows the DRP connector pin layout diagram, and Table 3.1.4 shows the DRP connector pin layout table.

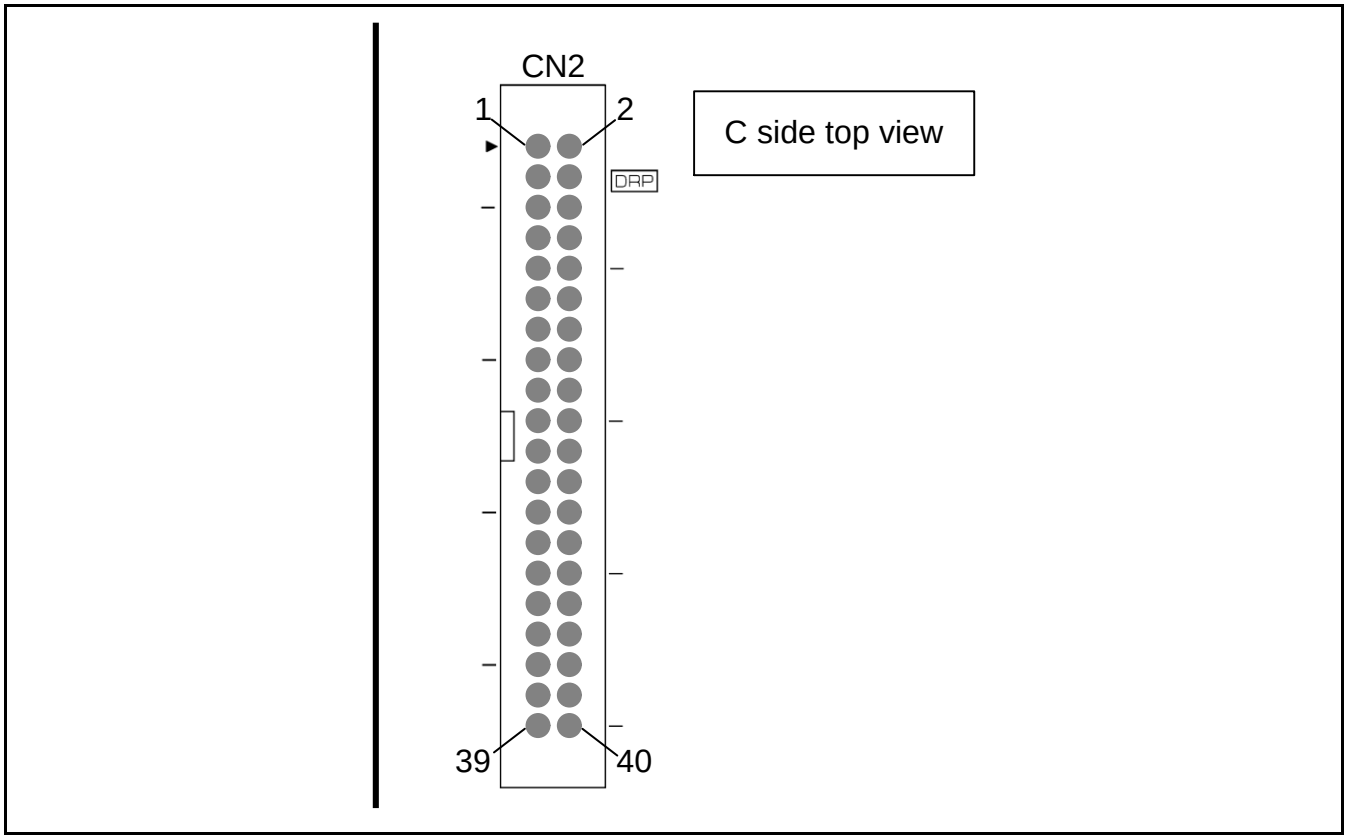


Figure 3.1.4 DRP Connector (CN2) Pin Layout Diagram

Table 3.1.4 DRP Connector (CN2) Pin Layout Table

Pin	Signal name	Pin	Signal name
1	P6_4 / AUDIO_CLK / DRP00	2	P6_5 / CS3 / DRP01
3	P6_6 / DRP02	4	P6_7 / WE0/DQML / DRP03
5	Vss	6	P7_0 / WE1/DQMU / DRP04 / SCK1
7	P7_1 / RD/WR / DRP05 / RxD1	8	P7_3 / RAS / DRP06 / TxD1
9	P7_4 / CAS / DRP07 / RTS1	10	Vss
11	P7_5 / CKE / DRP08 / CTS1 / OVRCUR1	12	P9_7 / A15 / DRP09
13	P9_6 / A14 / DRP10 / SSIBCK0	14	P9_5 / A13 / DRP11 / SSIFS0
15	+3.3V	16	P9_4 / A12 / DRP12 / SSITxD0
17	P9_3 / A11 / DRP13 / SSIRxD0	18	P9_2 / A10 / DRP14
19	P9_1 / A9 / DRP15 / RxD4	20	+3.3V
21	P9_0 / A8 / DRP16 / TxD4	22	P8_7 / A7 / DRP17 / RSPCK0
23	P8_6 / A6 / DRP18 / MOSI0	24	P8_5 / A5 / DRP19 / MISO0
25	+5V	26	P8_4 / A4 / DRP20 / SSL00
27	P8_3 / A3 / DRP21	28	P8_2 / A2 / DRP22
29	P8_1 / A1 / DRP23	30	+5V
31	P0_0 / D0 / DRP24	32	P0_1 / D1 / DRP25
33	P0_2 / D2 / DRP26	34	P0_3 / D3 / DRP27
35	Vss	36	P0_4 / D4 / DRP28
37	P0_5 / D5 / DRP29	38	P0_6 / D6 / DRP30
39	P1_0 / D7 / DRP31	40	Vss

[Note] Red characters indicate functions in use.

3.1.3 Mic-in Pin Jack (CN3)

RTK79210XXB00000BE is equipped with the mic-in pin jack (CN3).

Figure 3.1.5 shows the mic pin jack layout diagram, and Table 3.1.5 shows the mic-in pin jack layout table.

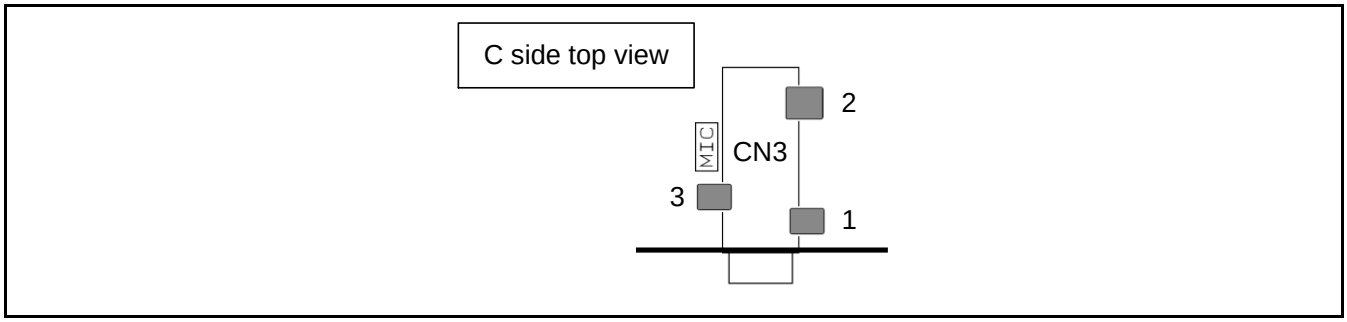


Figure 3.1.5 Mic-in Pin Jack (CN3) Layout Diagram

Table 3.1.5 Mic-in Pin Jack (CN3) Layout Table

Pin	Signal name
1	GND (AVss)
2	L2 (audio CODEC Lch analog input pin)
3	R2 (audio CODEC Rch analog input pin)

3.1.4 Line out Pin Jack (CN4)

RTK79210XXB00000BE is equipped with the line out pin jack (CN4).

Figure 3.1.6 shows the line out pin jack layout diagram, and Table 3.1.6 shows the line out pin jack layout table.

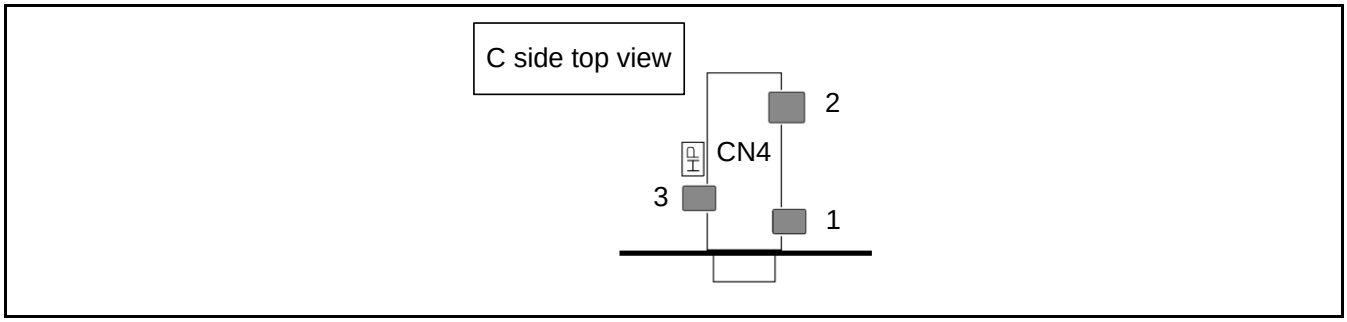


Figure 3.1.6 Line Out Pin Jack (CN4) Layout Diagram

Table 3.1.6 Line Out Pin Jack Layout Table

Pin	Signal name
1	GND (AVss)
2	LOUT1 (audio CODEC Lch analog output pin)
3	ROUT1 (audio CODEC Rch analog output pin)

3.1.5 Serial Board Connector (CN5)

RTK79210XXB00000BE is equipped with a serial board (USB Micro-B) connector (CN5).

Figure 3.1.7 shows the serial board connector pin layout diagram, and Table 3.1.7 shows the serial board connector pin layout table.

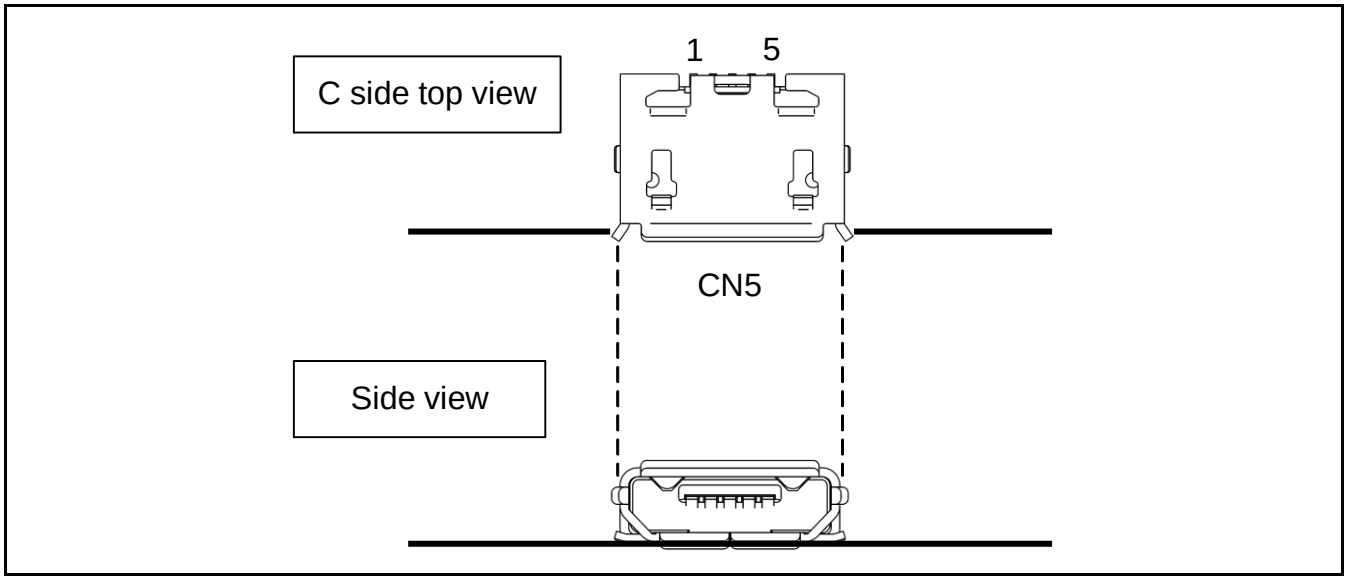


Figure 3.1.7 Serial Board Connector (CN5) Pin Layout Diagram

Table 3.1.7 Serial Board Connector (CN5) Pin Layout Table

Pin	Signal name
1	VBus (UVBUS)
2	D- (UDM0)
3	D+ (UDP0)
4	ID (NC)
5	GND (Vss)

3.1.6 LAN Connector (CN8, CN9)

RTK79210XXB00000BE is equipped with the LAN connectors (CN8, CN9).

Figure 3.1.8 shows the LAN connector pin layout diagram, and Table 3.1.8 shows the LAN connector pin layout table.

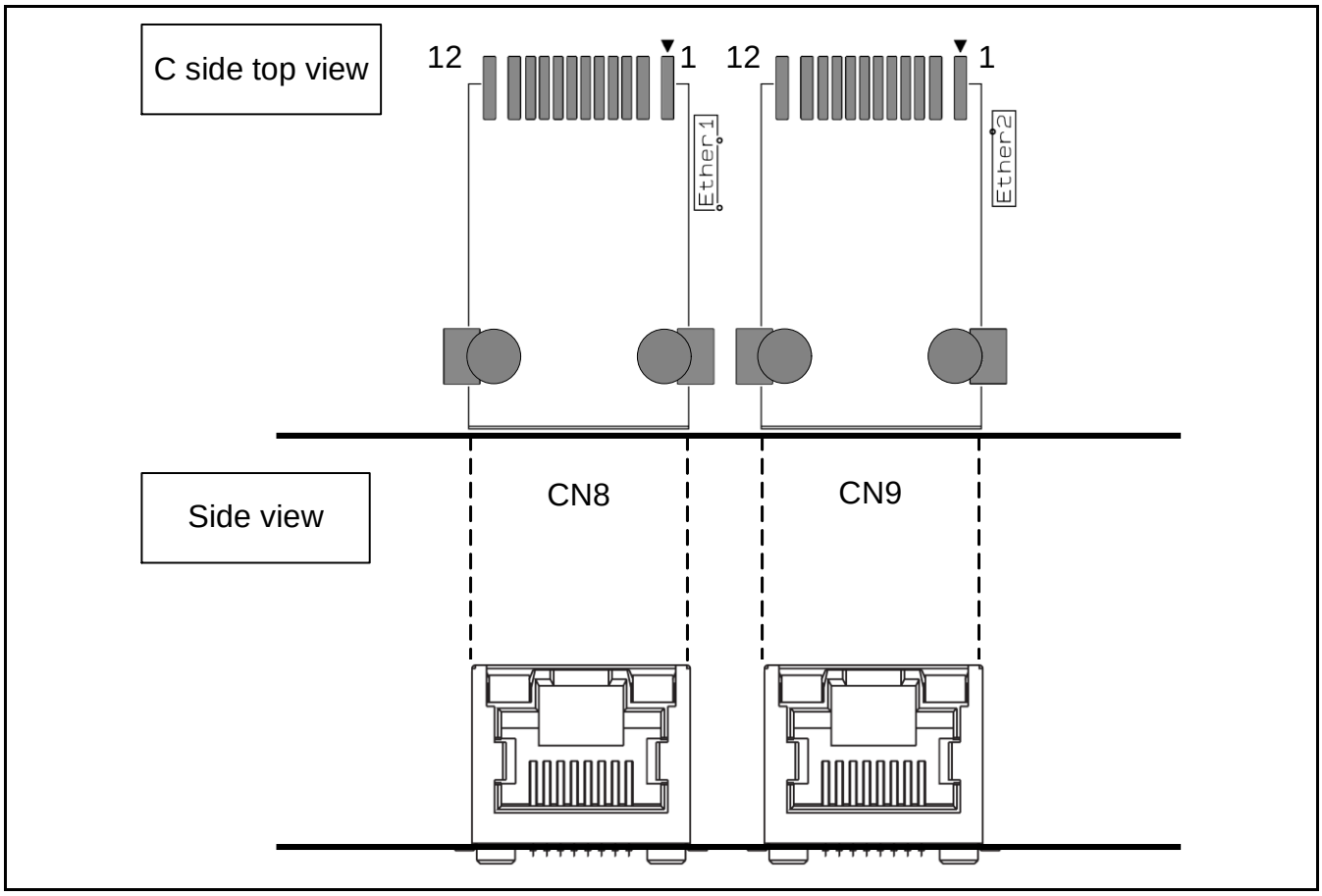


Figure 3.1.8 LAN Connector (CN8, CN9) Pin Layout Figure

Table 3.1.8 LAN Connector (CN8, CN9) Pin Layout Table

Pin	Signal name	
	CN8	CN9
1	LED-A (Y) (+3.3V)	LED-A (Y) (+3.3V)
2	LED-K (Y) (LED0/PHYAD[0])	LED-K (Y) (LED0/PHYAD[0])
3	TD+ (MDI+[0])	TD+ (MDI+[0])
4	TD- (MDI-[0])	TD- (MDI-[0])
5	CT1	CT1
6	CT2	CT2
7	RD+ (MDI+[1])	RD+ (MDI+[1])
8	RD- (MDI-[1])	RD- (MDI-[1])
9	NC	NC
10	CAP	CAP
11	LED-K (G) (LED1/PHYAD[1])	LED-K (G) (LED1/PHYAD[1] and P3_0 / ET1_LINKSTA)
12	LED-A (G) (+3.3V)	LED-A (G) (+3.3V)

[Note] Red characters indicate functions in use.

3.1.7 SD Card Slot (CN10)

RTK79210XXB00000BE is equipped with the SD card slot (CN10).

Figure 3.1.9 shows the SD card slot pin layout diagram, and Table 3.1.9 shows the SD card slot pin layout table.

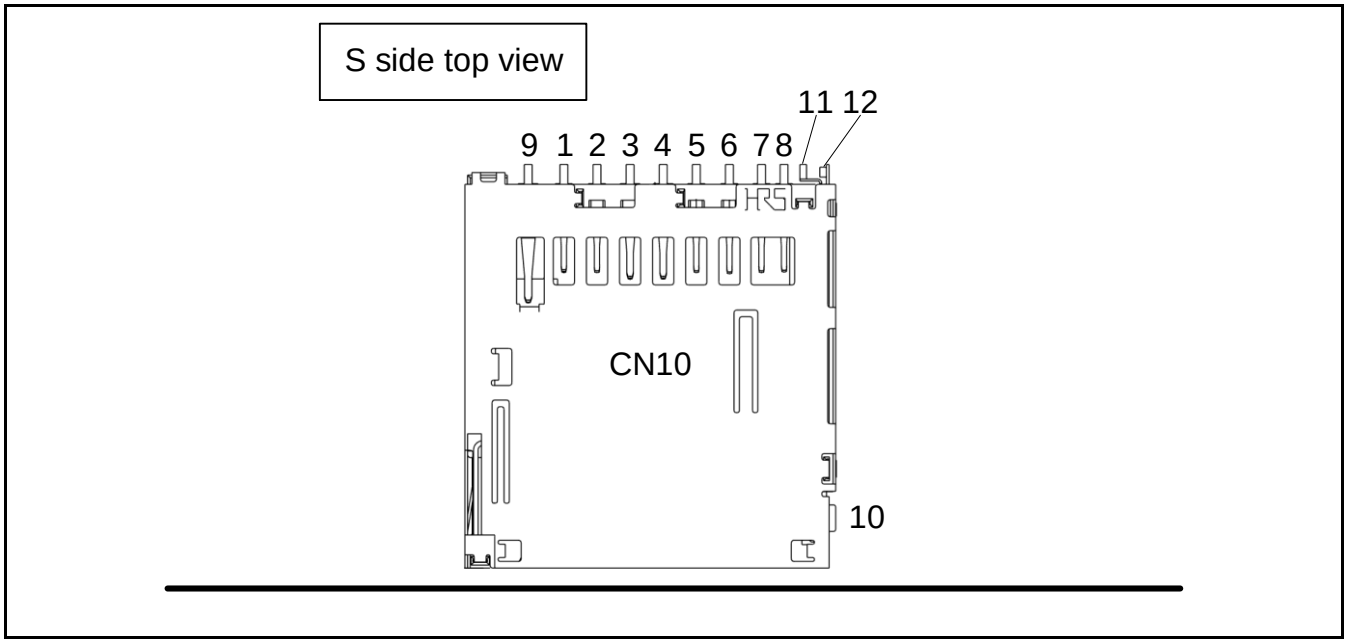


Figure 3.1.9 SD Card Slot (CN10) Pin Layout Diagram

Table 3.1.9 SD Card Slot (CN10) Pin Layout Table

Pin	Signal name
1	CD/DAT3 (SD1_DAT3)
2	CMD (SD1_CMD)
3	VSS1 (Vss)
4	VDD (+3.3V)
5	CLK (SD1_CLK)
6	VSS2 (Vss)
7	DAT0 (SD1_DAT0)
8	DAT1 (SD1_DAT1)
9	DAT2 (SD1_DAT2)
10	Write_Protect (P5_5 / SD1_WP)
11	Card_Detect (P5_4 / SD1_CD)
12	COMMON (Vss)

[Note] Red characters indicate functions in use.

3.1.8 USB Connector (CN12, CN13)

RTK79210XXB00000BE is equipped with the series A port (CN12) and Mini-B port (CN13).

Figure 3.1.10 shows the series A port pin layout diagram, and Figure 3.1.11 shows the Mini-B port pin layout diagram. Table 3.1.10 shows the series A port pin layout table, and Table 3.1.11 shows the Mini-B port pin layout table.

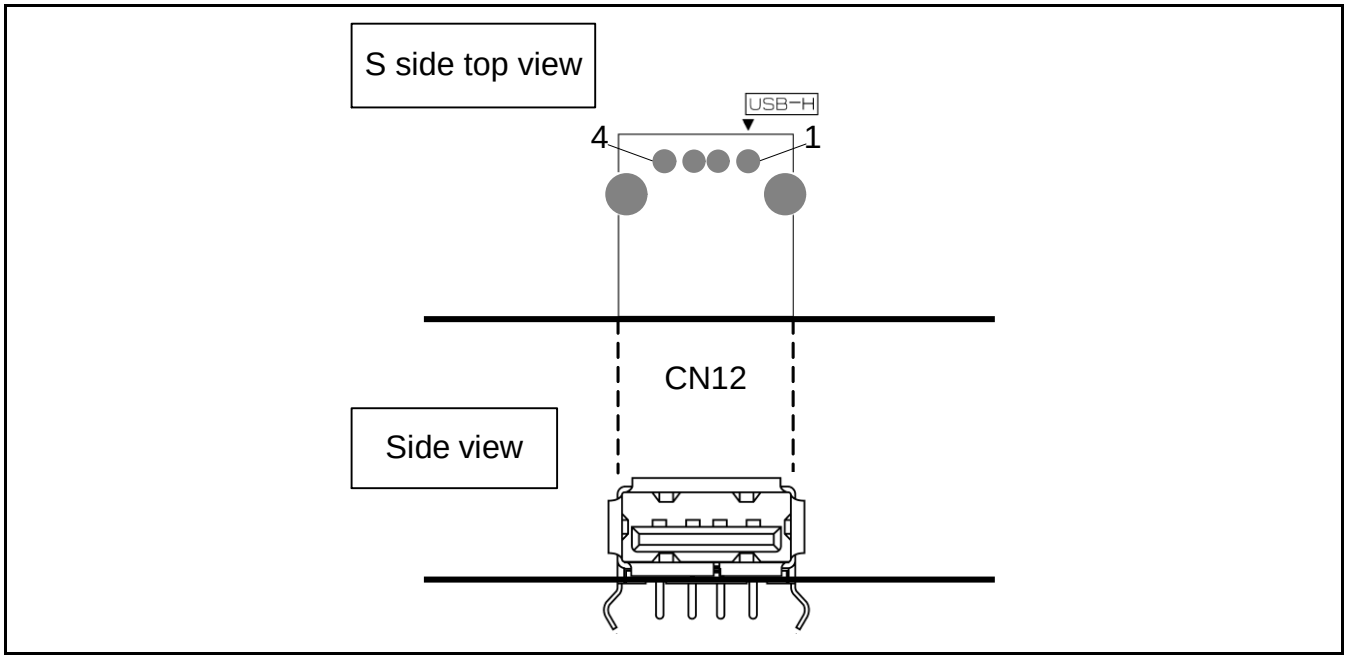


Figure 3.1.10 Series A Port (CN12) Pin Layout Diagram

Table 3.1.10 Series Port (CN12) Pin Layout Table

Pin	Signal name
1	VBus
2	D- (DM1)
3	D+ (DP1)
4	GND (Vss)

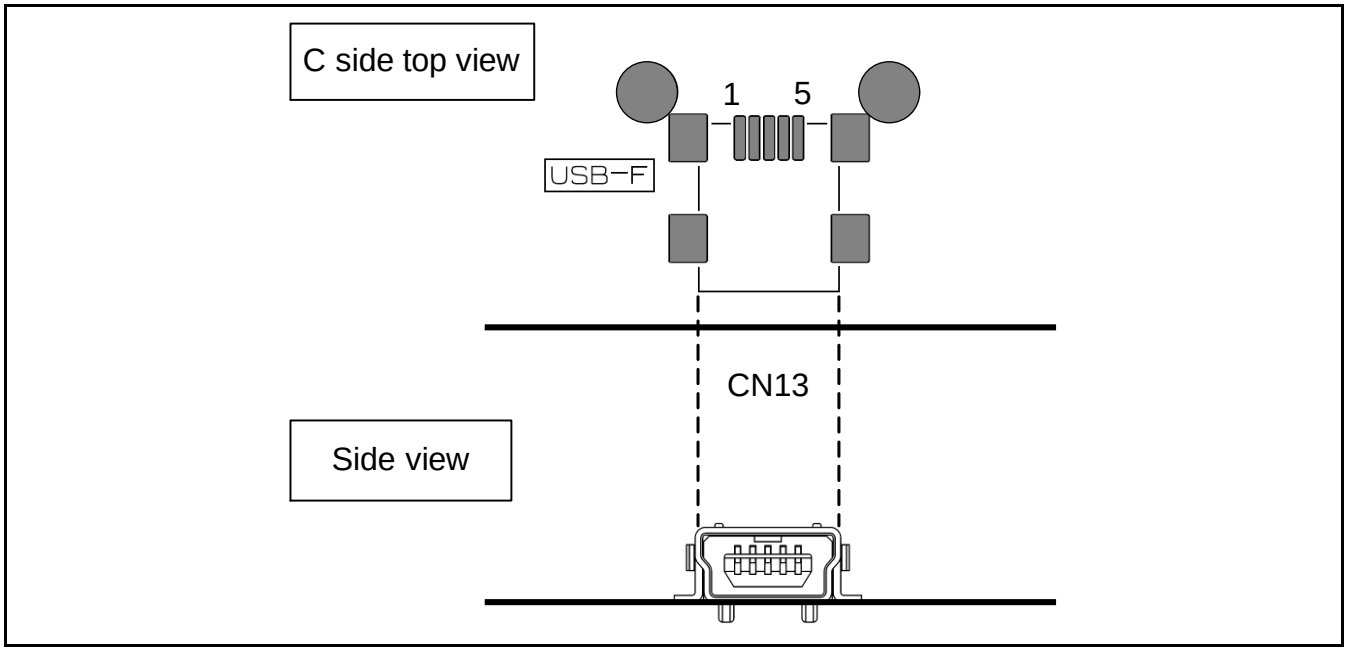


Figure 3.1.11 Mini-B Port (CN13) Pin Layout Diagram

Table 3.1.11 Mini-B Port (CN13) Pin Layout Table

Pin	Signal name
1	VBus (PC_0 / VBUSIN1)
2	D- (DM1)
3	D+ (DP1)
4	IC (connects to test pin TP3)
5	GND (Vss)

[Note] Red characters indicate functions in use.

3.1.9 LVDS Connector (CN14, CN16)

RTK79210XXB00000BE is equipped with the LVDS connector (CN14) and the back light connector (CN16) for power supply.

Figure 3.1.12 shows the LVDS connector and LVDS backlight connector pin layout diagram, Table 3.1.12 shows the LVDS connector pin layout table, and Table 3.1.13 shows the LVDS back light connector pin layout table.

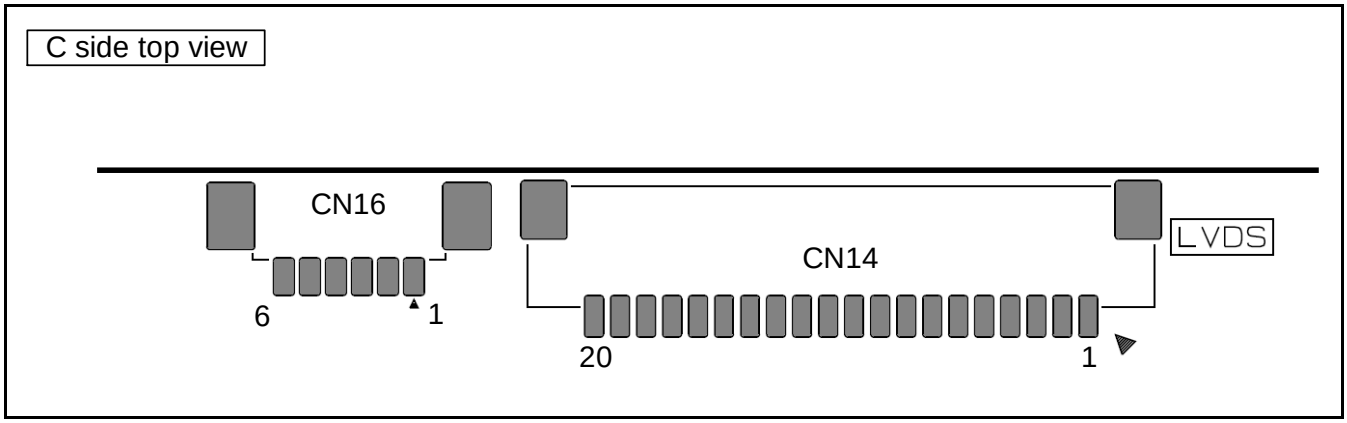


Figure 3.1.12 LVDS Connector (CN14, CN15) Pin Layout Diagram

Table 3.1.12 LVDS Connector (CN14) Pin Layout Table

Pin	Signal name
1	Vcc (+3.3V)
2	Vcc (+3.3V)
3	GND (Vss)
4	GND (Vss)
5	RX0- (P4_1 / TXOUT0M)
6	RX0+ (P4_0 / TXOUT0P)
7	GND (Vss)
8	RX1- (P4_3 / TXOUT1M)
9	RX1+ (P4_2 / TXOUT1P)
10	GND (Vss)
11	RX2- (P4_5 / TXOUT2M)
12	RX2+ (P4_4 / TXOUT2P)
13	GND (Vss)
14	CLK- (P4_7 / TXCLKOUTM)
15	CLK+ (P4_6 / TXCLKOUTP)
16	GND (Vss)
17	L/R or RX3- (connects to +3.3V via 680Ω resistor)
18	U/D or RX3+ (connects to +3.3V via 680Ω resistor)
19	GND (Vss)
20	GND (Vss)

[Note] Red characters indicate functions in use.

Table 3.1.13 LVDS Back Light Connector (CN16) Pin Layout Table

Pin	Signal name
1	VLED (5V) (+5V)
2	VLED (5V) (+5V)
3	DIMMER (Brightness Adjust) (connects to +3.3V via 10kΩ resistor)
4	ENABLE (connects to +3.3V via 10kΩ resistor)
5	GND (Vss)
6	GND (Vss)

3.1.10 Digital Image Input/output Connector (CN15)

RTK79210XXB00000BE is equipped with the digital image input/output connector (CN15).

Figure 3.1.13 shows the digital image input/output connector pin layout diagram, and Table 3.1.14 shows the digital image input/output connector pin layout.

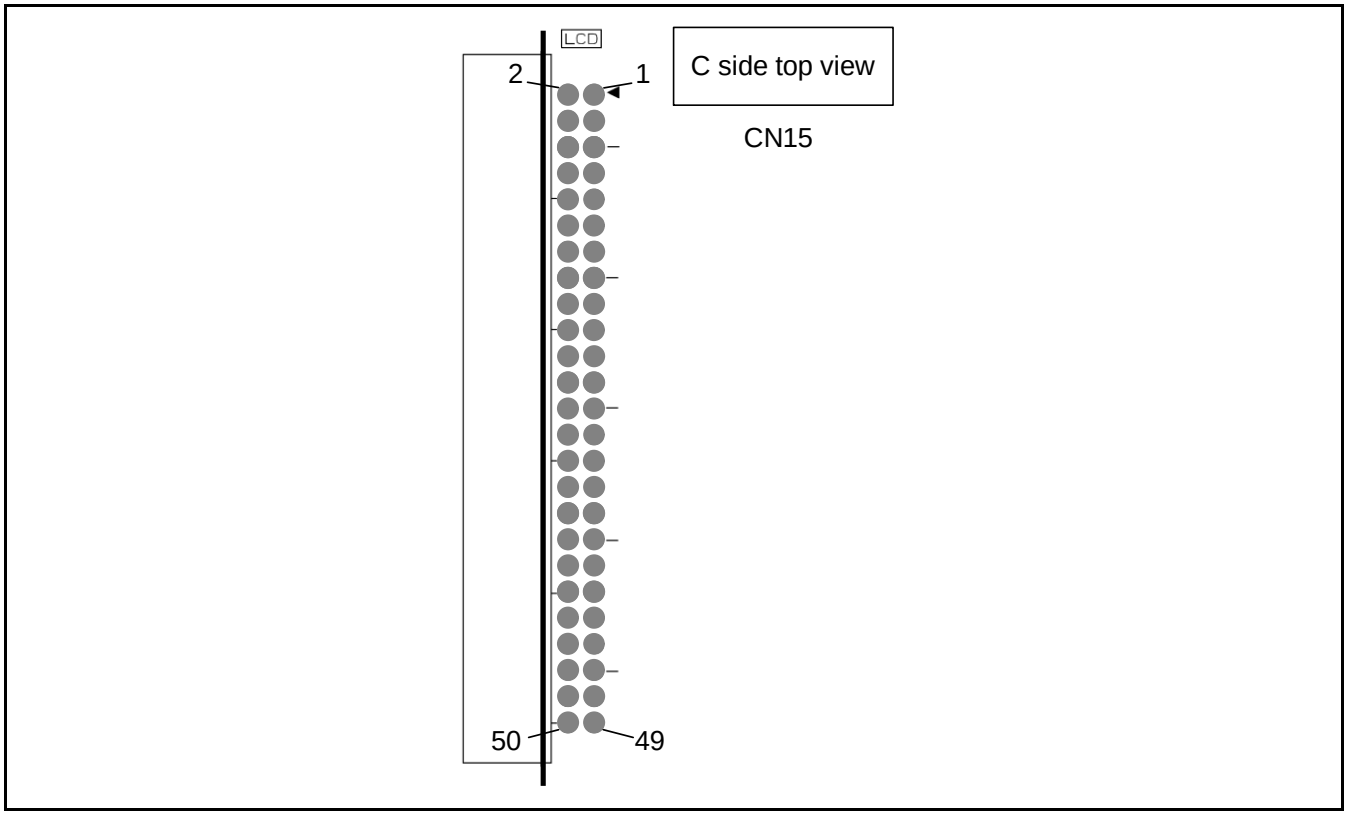


Figure 3.1.13 Digital Image Input/output Connector (Cn15) Pin Layout Diagram

Table 3.1.14 Digital Image Input/output Connector (CN15) Pin Layout Table

Pin	Signal name	Pin	Signal name
1	DATA0 (PF_7 / DV0_DATA23 / LCD0_DATA0)	2	DATA1 (PH_2 / DV0_DATA22 / LCD0_DATA1)
3	DATA2 (PF_6 / DV0_DATA21 / LCD0_DATA2)	4	DATA3 (PF_5 / DV0_DATA20 / LCD0_DATA3)
5	DATA4 (PF_4 / DV0_DATA19 / LCD0_DATA4)	6	DATA5 (PF_3 / DV0_DATA18 / LCD0_DATA5)
7	DATA6 (PF_2 / DV0_DATA17 / LCD0_DATA6)	8	DATA7 (PF_1 / DV0_DATA16 / LCD0_DATA7)
9	DATA8 (PF_0 / DV0_DATA15 / LCD0_DATA8)	10	DATA9 (P8_0 / DV0_DATA14 / LCD0_DATA9)
11	DATA10 (PA_0 / DV0_DATA13 / LCD0_DATA10)	12	DATA11 (PA_1 / DV0_DATA12 / LCD0_DATA11)
13	DATA12 (PA_2 / DV0_DATA11 / LCD0_DATA12)	14	DATA13 (PA_3 / DV0_DATA10 / LCD0_DATA13)
15	DATA14 (PA_4 / DV0_DATA9 / LCD0_DATA14)	16	DATA15 (PA_5 / DV0_DATA8 / LCD0_DATA15)
17	DATA16 (PA_6 / DV0_DATA7 / LCD0_DATA16)	18	DATA17 (PA_7 / DV0_DATA6 / LCD0_DATA17)
19	DATA18 (PB_0 / DV0_DATA5 / LCD0_DATA18)	20	DATA19 (PB_1 / DV0_DATA4 / LCD0_DATA19)
21	DATA20 (PB_2 / DV0_DATA3 / LCD0_DATA20)	22	DATA21 (PB_3 / DV0_DATA2 / LCD0_DATA21)
23	DATA22 (PB_4 / DV0_DATA1 / LCD0_DATA22)	24	DATA23 (PB_5 / DV0_DATA0 / LCD0_DATA23)
25	RESET (RES#)	26	LCD_CLK (PJ_6 / FCE / LCD0_CLK)
27	TCON1 (PC_3 / LCD0_TCON4)	28	TCON2 (PC_4 / LCD0_TCON3)
29	TCON3 (P7_7 / DV0_HSYNC / LCD0_TCON0)	30	Hi (DITHB) (connects to +3.3V via 10kΩ resistor)
	DV_HSYNC (P7_7 / DV0_HSYNC / LCD0_TCON0)		
31	Hi (MODE) (connects to +3.3V via 10kΩ resistor)	32	Hi (L/R) (connects to +3.3V via 10kΩ resistor)
33	Low (U/D) (connects to Vss via 10kΩ resistor)	34	PWM (P7_6 / DV0_VSYNC / GTIOC3A)
			DV_VSYNC (P7_6 / DV0_VSYNC / GTIOC3A)
35	NC	36	NC
37	SDA (PD_7 / RIIC3SDA)	38	SCL (PD_6 / RIIC3SCL)
39	TP_INT (P5_7 / IRQ3)	40	NC
41	NC	42	NC
43	NC	44	DV_CLK (P7_2 / DV0_CLK)
45	Vcc (+3.3V)	46	Vcc (+3.3V)
47	GND (Vss)	48	GND (Vss)
49	5V (+5V)	50	5V (+5V)

[Note] Red characters indicate functions in use.

3.1.11 CMOS Camera Connector (CN17)

RTK79210XXB00000BE is equipped with a CMOS camera connector (CN17).

Figure 3.1.14 shows the CMOS camera connector pin layout diagram, and Table 3.1.15 shows the CMOS camera connector pin layout.

CMOS camera connector (CN17) does not have a reverse insertion prevention guide, so be sure to insert in the direction of the #1 pin during connection. Moreover, confirm that the camera device signal pin is compatible with the circuit board.

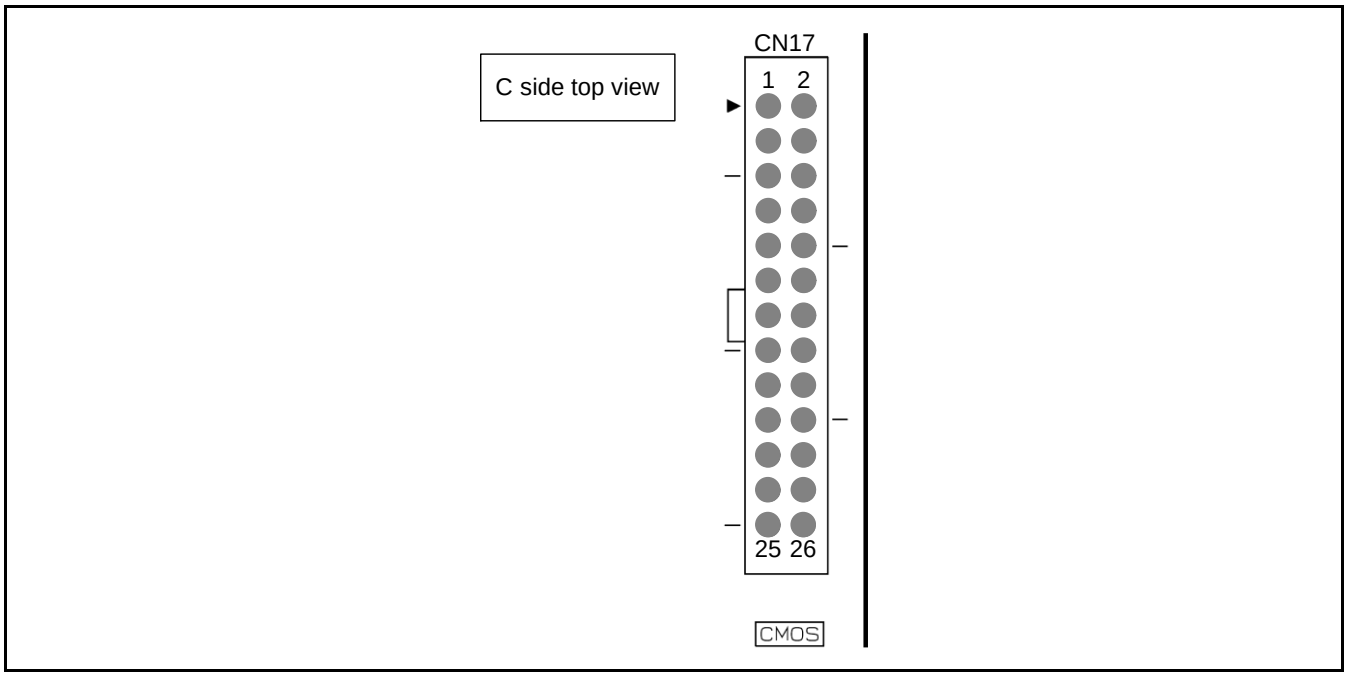


Figure 3.1.14 CMOS Camera Connector (CN17) Pin Layout Diagram

Table 3.1.15 CMOS Camera Connector (CN17) Pin Layout Table

Pin	Signal name	Pin	Signal name
1	Vcc (+3.3V)	2	GND (Vss)
3	SCL (PD_6 / RIIC3SCL)	4	SDA (PD_7 / RIIC3SDA)
5	VSYNC (P6_2 / ET0_TXD0/RMII0_TXD0 / VIO_VD)	6	HSYNC (P6_3 / ET0_TXD1/RMII0_TXD1 / VIO_HD)
7	PCLK (P6_1 / ET0_TXEN/RMII0_TXDEN / VIO_CLK)	8	XCLK
9	D7 (PE_1 / ET0_RXD0/RMII0_RXD0 / VIO_D7)	10	D6 (PE_2 / ET0_RXD1/RMII0_RXD1 / VIO_D6)
11	D5 (PE_3 / ET0_RXER/RMII0_RXER / VIO_D5)	12	D4 (PE_4 / ET0_CRS/RMII0_CRSDV / VIO_D4)
13	D3 (PE_5 / ET0_MDC / VIO_D3)	14	D2 (PE_6 / ET0_MDIO / VIO_D2)
15	D1 (PH_0 / VIO_D1)	16	D0 (PH_1 / VIO_D0)
17	GND (Vss)	18	I/O (PE_0 / ET0_RXCLK/REF50CK0 / VIO_FLD)
19	I/O (PG_4 / VIO_D15)	20	I/O (PG_5 / VIO_D14)
	D15 (PG_4 / VIO_D15)		D14 (PG_5 / VIO_D14)
21	D13 (PG_6 / VIO_D13)	22	D12 (PG_7 / VIO_D12)
23	D11 (PG_3 / VIO_D11)	24	D10 (PG_2 / VIO_D10)
25	D7 (PG_1 / VIO_D9)	26	D8 (PG_0 / VIO_D8)

[Note] Red characters indicate functions in use.

3.1.12 DC Power Supply Jack (CN18)

RTK79210XXB00000BE is equipped with the DC power supply jack (CN18) for providing power to the system.

Figure 3.1.15 shows the power supply connector pin layout diagram, and Table 3.1.16 shows the power supply connector pin layout table.

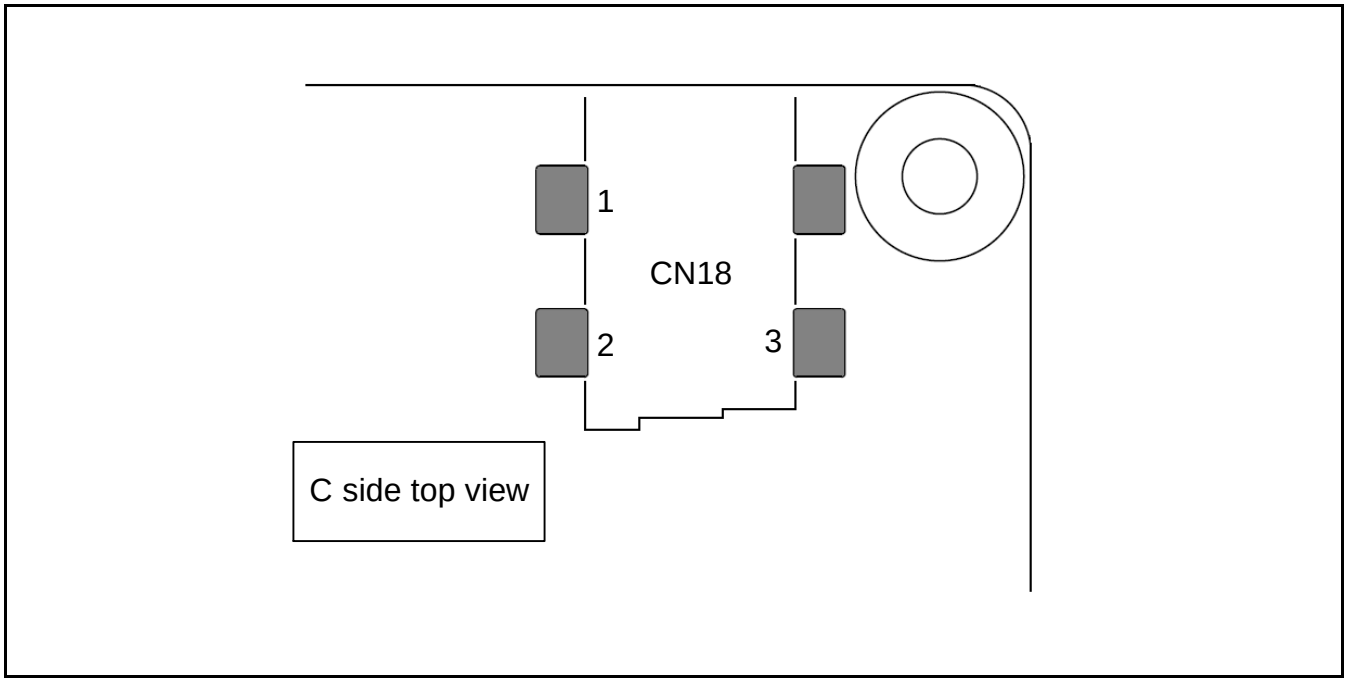


Figure 3.1.15 Power Supply Connector (CN18) Pin Layout Figure

Table 3.1.16 Power Voltage Connector (CN18) Pin Layout Table

Pin	Signal name
1	GND (Vss)
2	GND (Vss)
3	+5V

3.2 Operational Component Layout

Figure 3.2.1 shows the RTK79210XXB00000BE operational component layout diagram.

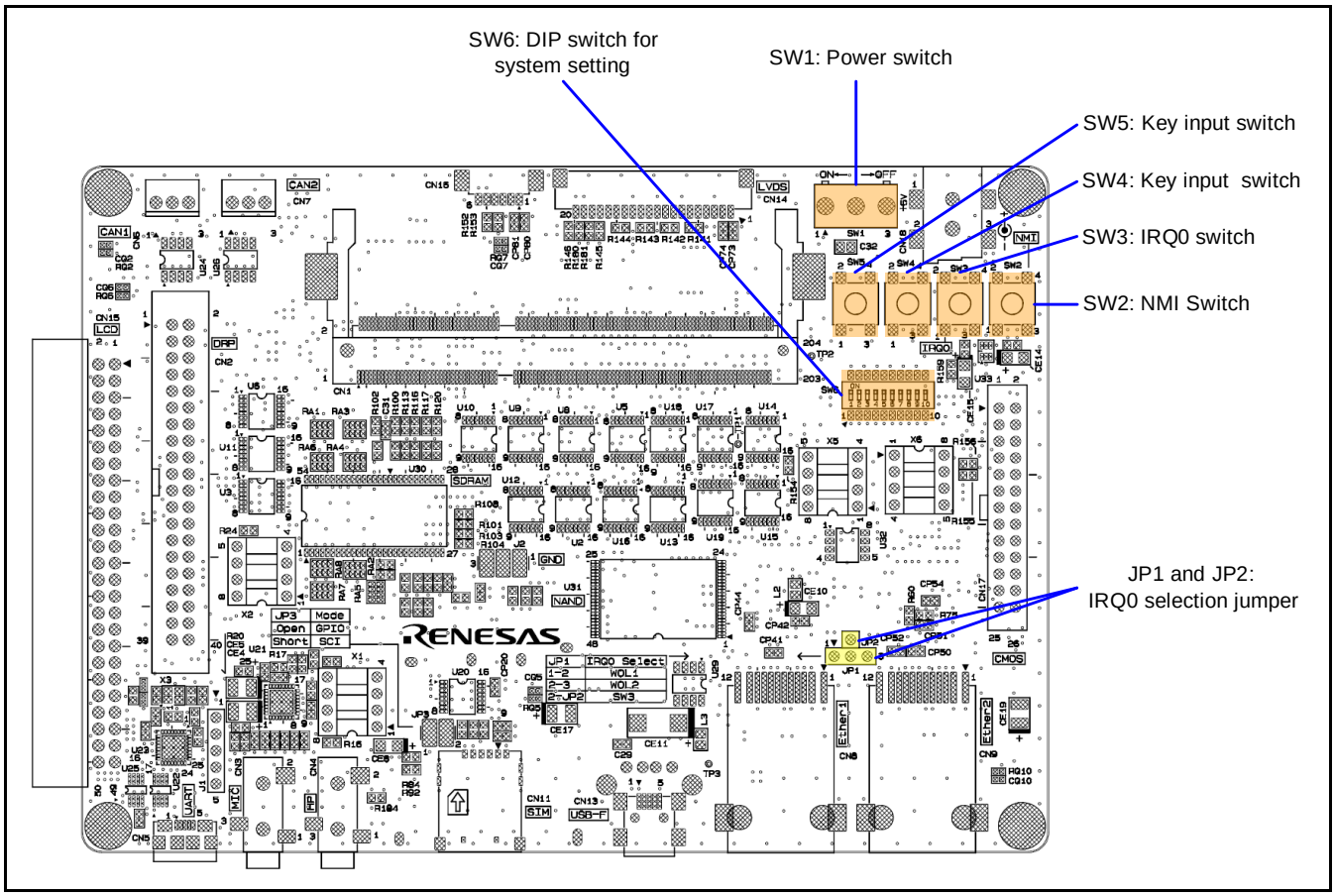


Figure 3.2.1 RTK79210XXB00000BE Operational Component Layout Diagram (C Side Top View)

3.2.1 Jumpers (JP1 and JP2)

RTK79210XXB00000BE is equipped with two system setting jumpers.
Figure 3.2.2 shows the jumper layout diagram, and Table 3.2.1 shows the jumper setting table.

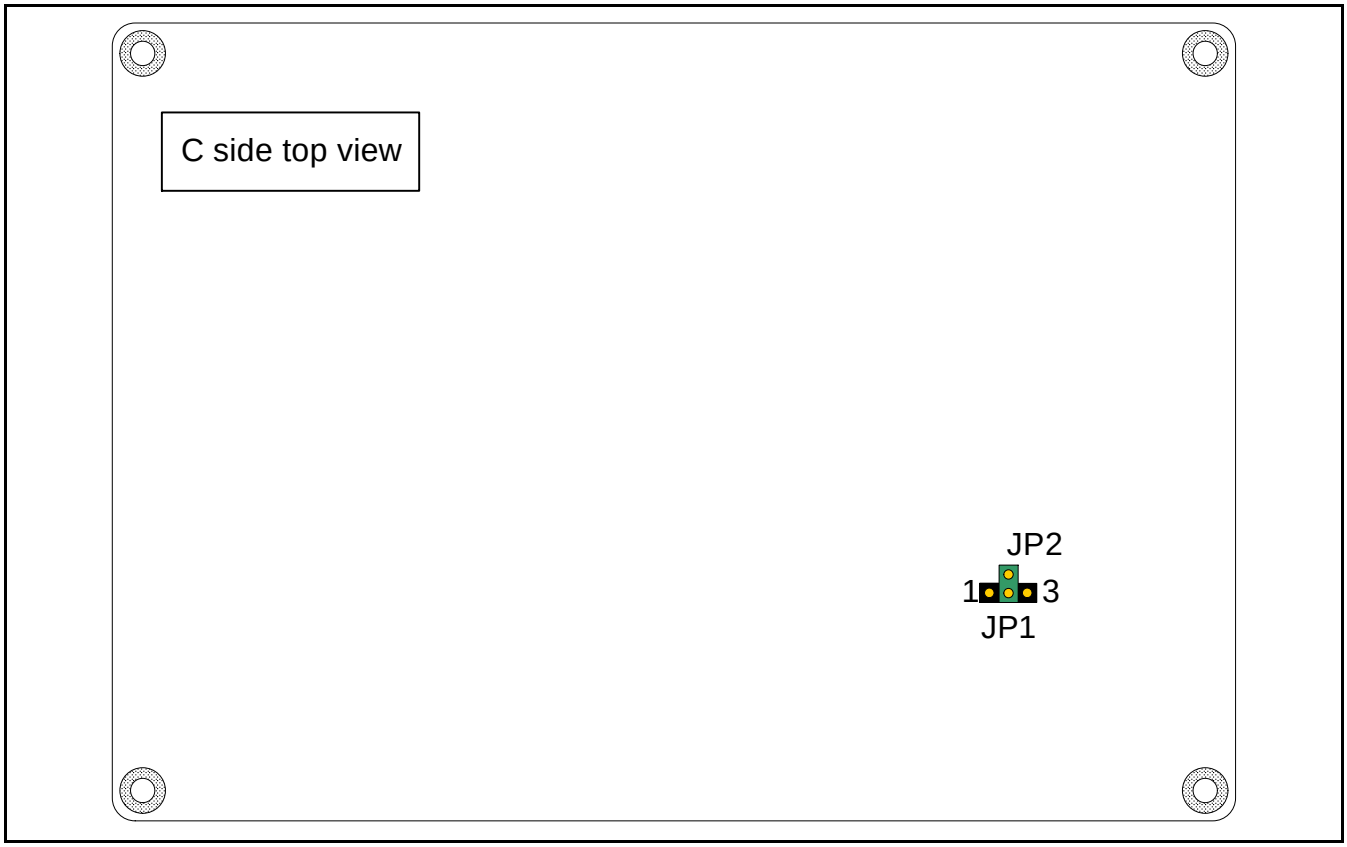


Figure 3.2.2 RTK79210XXB00000BE Jumper Layout Diagram

Table 3.2.1 Jumper Setting Table (JP1 and JP2)

Jumper	Settings	Function
JP1 IRQ0 input selection	1-2	Ethernet PHY1 (U27) WOL pin
	2-3	Ethernet PHY2 (U28) WOL pin
	2-JP2	IRQ0 switch (SW3)

[Note] displayed during initial settings.

Be sure to turn off the power before altering the jumper settings.

3.2.2 Switch Functions

RTK79210XXB00000BE is equipped with six switches.

Figure 3.2.3 shows the mounted switch layout diagram, Table 3.2.2 lists the mounted switches, and Table 3.2.3 provides the explanation of DIP switch functions.

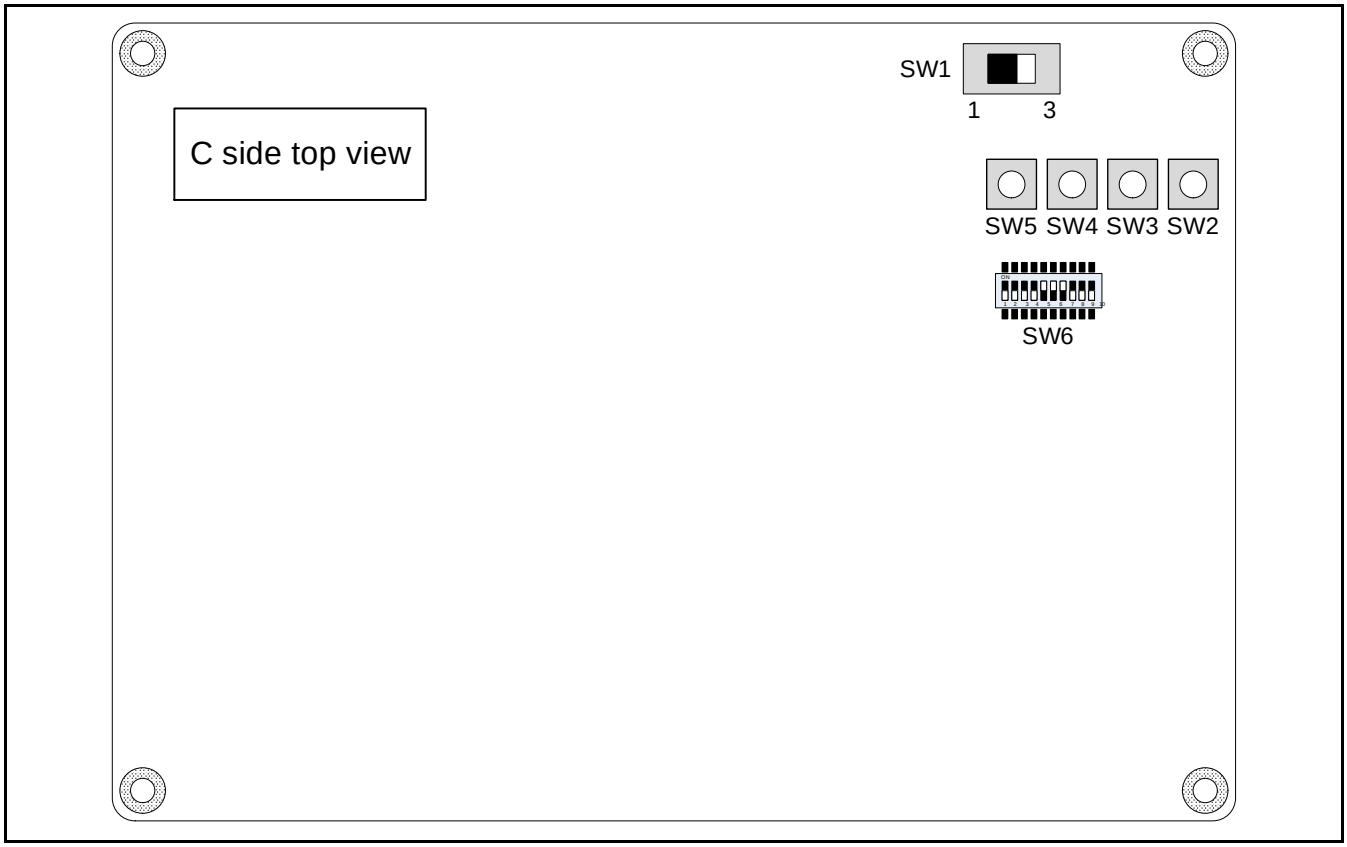


Figure 3.2.3 RTK79210XXB00000BE Mounted Switch Layout Diagram

Table 3.2.2 Mounted RTK79210XXB00000BE Switch Overview

Numbers	Function	Note
SW1	Power supply switch	
SW2	NMI switch	Refer to section 2.6 for details.
SW3	IRQ0 switch	
SW4	Key input switch	Refer to section 2.14 for details.
SW5	Key input switch	
SW6	DIP switch for system settings	Refer to Table 3.2.3 for further details

Table 3.2.3 Explanation of DIP Switch Functions (SW6)

Numbers	Settings		Function
SW6-1 P9_[7 :0]、P8_[7 :1]、P2_2、P2_0、P1_3、P1_[1 :0]、P0_[6 :0]、P6_7、P6_5、P7_[1 :0]、P7[5 :3] connection address selection	OFF	SDRAM#/Other = “H”	Used as DRP, audio, UART, and USB interface pins
	ON	SDRAM#/Other = “L”	Used as SDRAM control pin
SW6-2 P8_4、P8_[7:6]、P6_4、P9_[6:3] connection address selection	OFF	DRP#/Audio = “H”	Used as audio interface pin
	ON	DRP#/Audio = “L”	Used as DRP pin
SW6-3 P9_[1 :0]、P1_0、P7_5 connection address selection	OFF	DRP#/Other = “H”	Used as UART and USB interface pins
	ON	DRP#/Other = “L”	Used as DRP pin
SW6-4 P6_[3:1]、PE_[6:0] connection address selection	OFF	Ether1#/CEU = “H”	Used as CEU pin
	ON	Ether1#/CEU = “L”	Used as Ethernet PHY1 control pin
SW6-5 P3_[5:1]、PH_5、PK_[4:0] connection address selection	OFF	Ether2#/NAND = “H”	Used as FLCTL pin
	ON	Ether2#/NAND = “L”	Used as Ethernet PHY2 control pin
SW6-6 PJ_[7:6] connection address selection	OFF	VDC6#/NAND = “H”	Used as FLCTL pin
	ON	VDC6#/NAND = “L”	Used as VDC6 pin
SW6-7 P7_[7:4] connection address selection	OFF	VDC6#/Other = “H”	NC
	ON	VDC6#/Other = “L”	Used as VDC6 pin
SW6-8	OFF	NC	
	ON	NC	
SW6-9 P5_3	OFF	P5_3 = “H”	Generic input port P5_3 = “H”
	ON	P5_3 = “L”	Generic input board P5_3 = “L”
SW6-10 PC_2	OFF	PC_2 = “H”	Generic input port PC_2 = “H”
	ON	PC_2 = “L”	Generic input port PC_2 = “L”

[Note] indicates default setting.

Be sure to turn the board power to off before altering the DIP switch setting.

3.3 External Dimensions

Figure 3.3.1 shows the external dimensions of the RTK79210XXB00000BE C side top view.

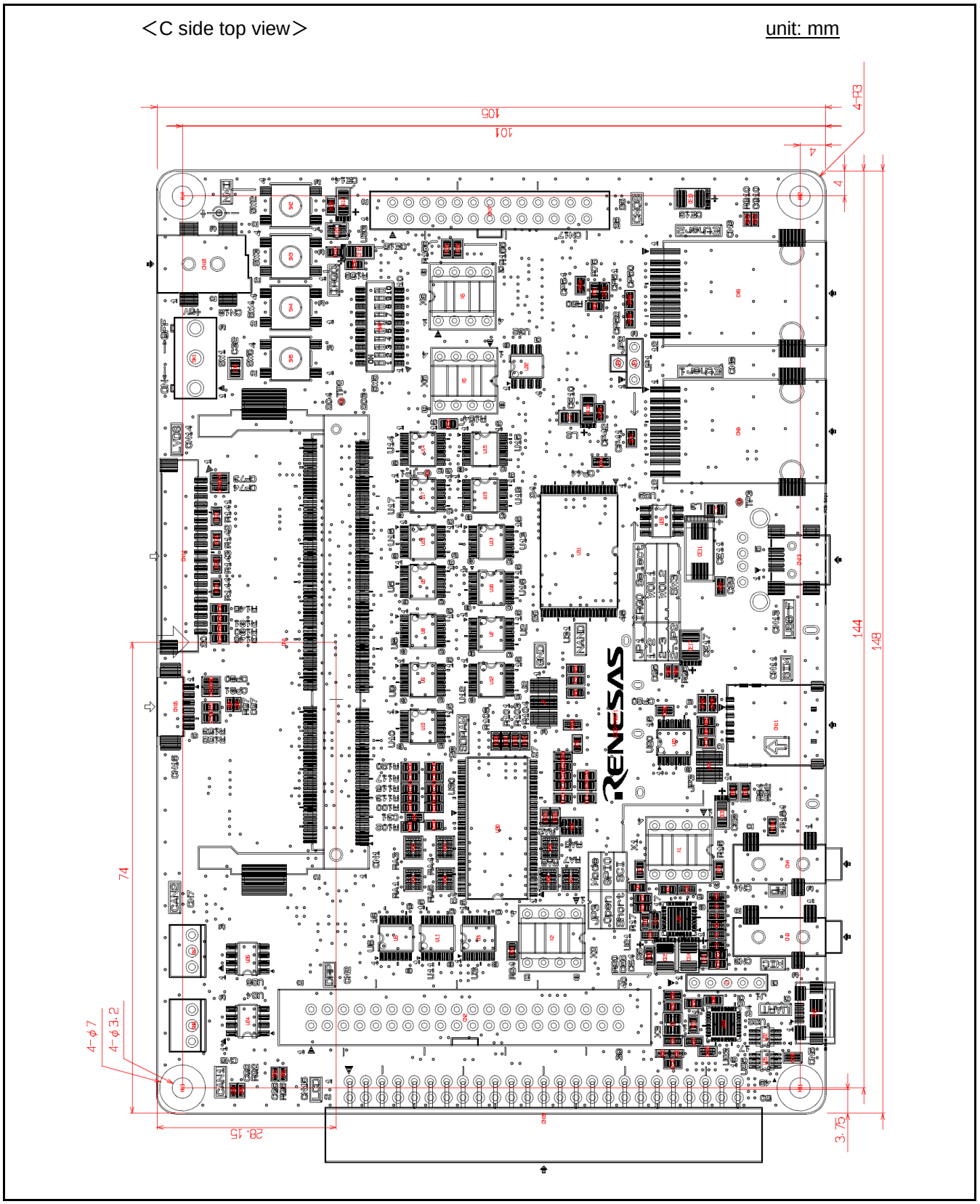


Figure 3.3.1 RTK79210XXB00000BE External Dimensions Diagram

Appendix 1 RTK79210XXB00000BE Connection Diagram

RZ/A2M SUB board RTK79210XXB00000BE SCHEMATICS

Note:


Digital GND (GND)

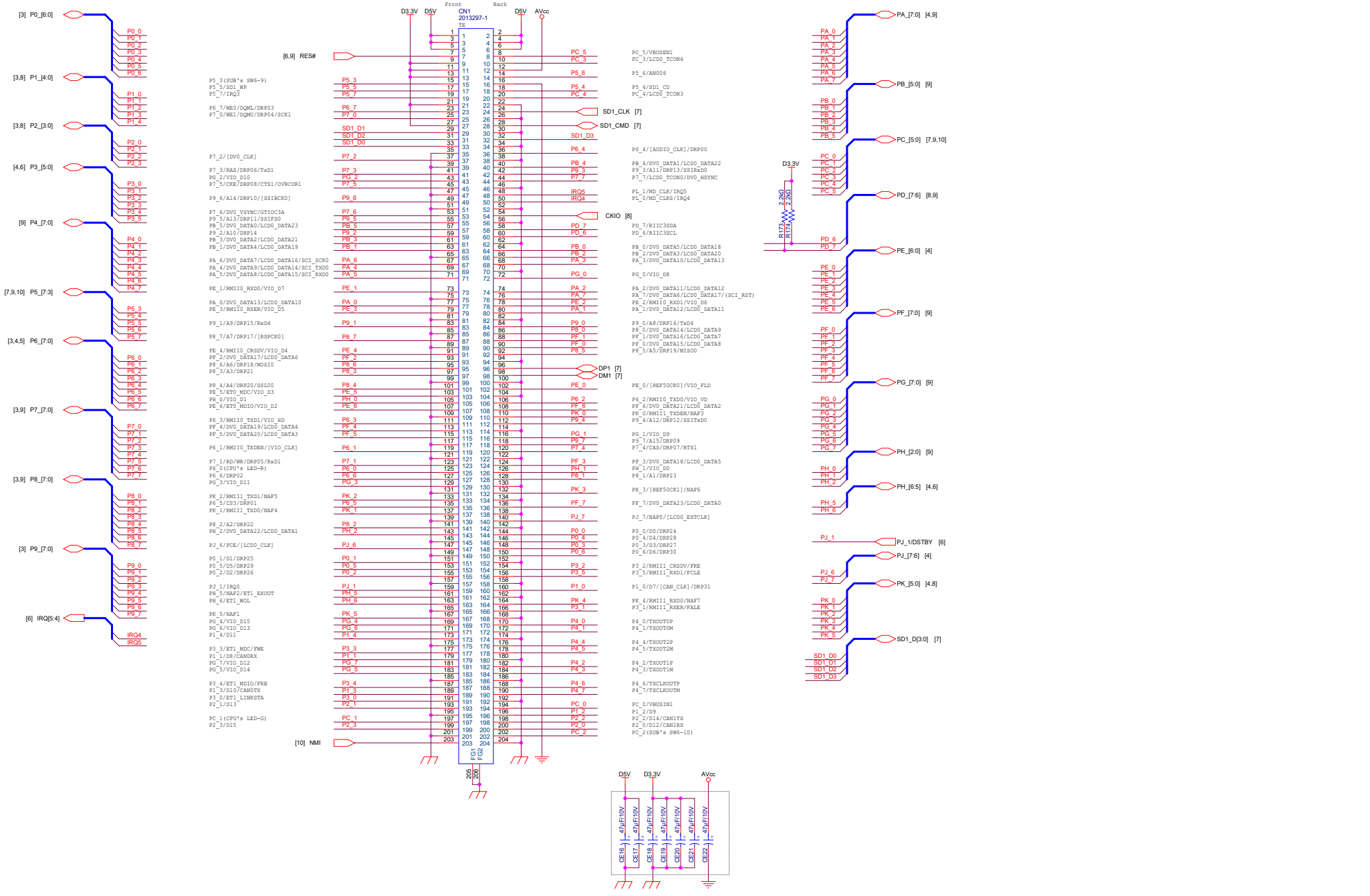

Analog GND (AVss)


Not mounted

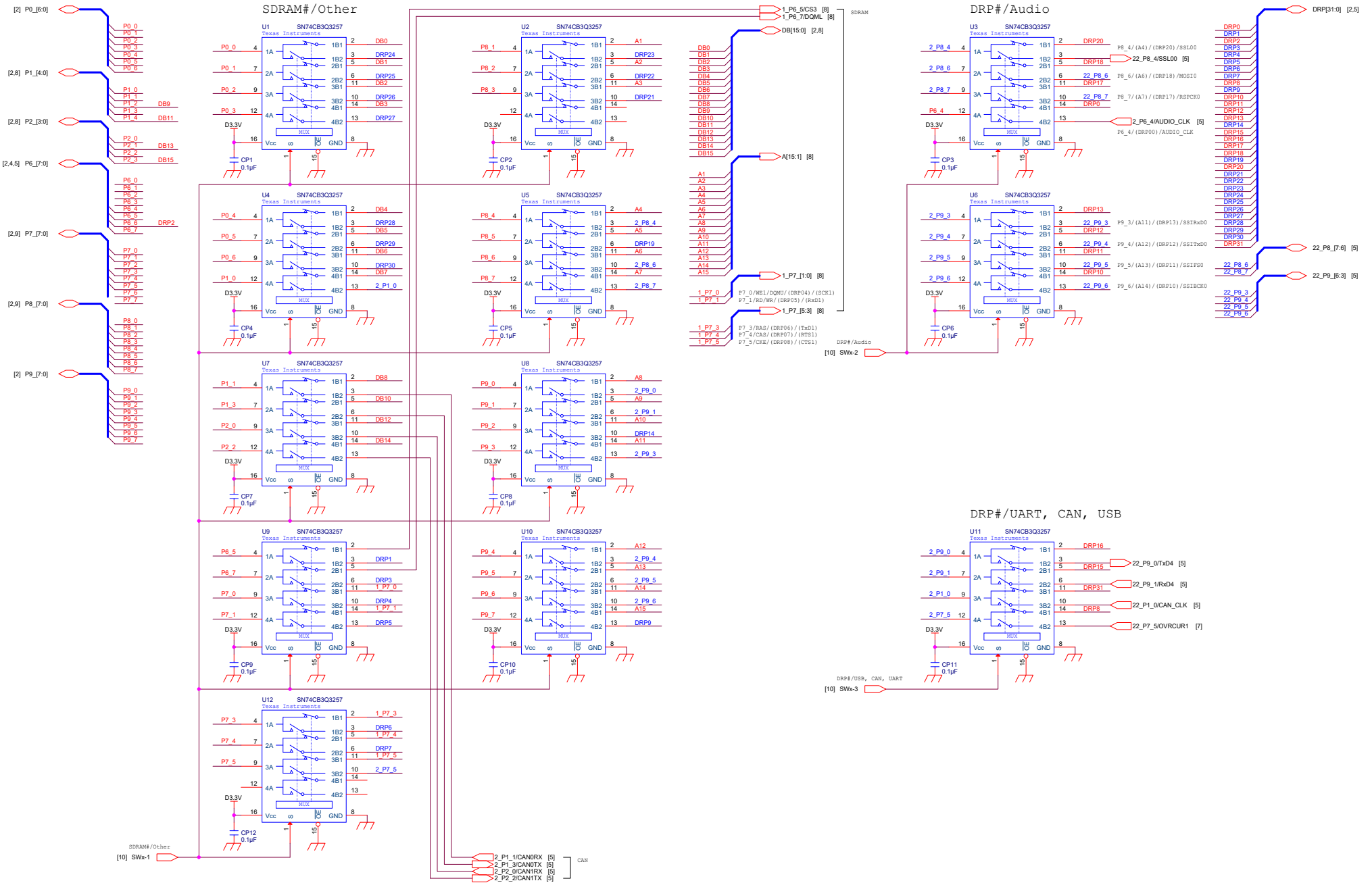
D5V = Digital 5V (System Power)
D3.3V = Digital 3.3V
AVcc = Analog 3.3V for RZ/A2M
A3.3V = Analog 3.3V for Audio CODEC
EA3.3V = Analog 3.3V for Ethernet PHY

R = Fixed Resistors
RA = Resistor Array
C = Ceramic Caps
CE = Tantalum Electrolytic Caps
CP = Decoupling Caps

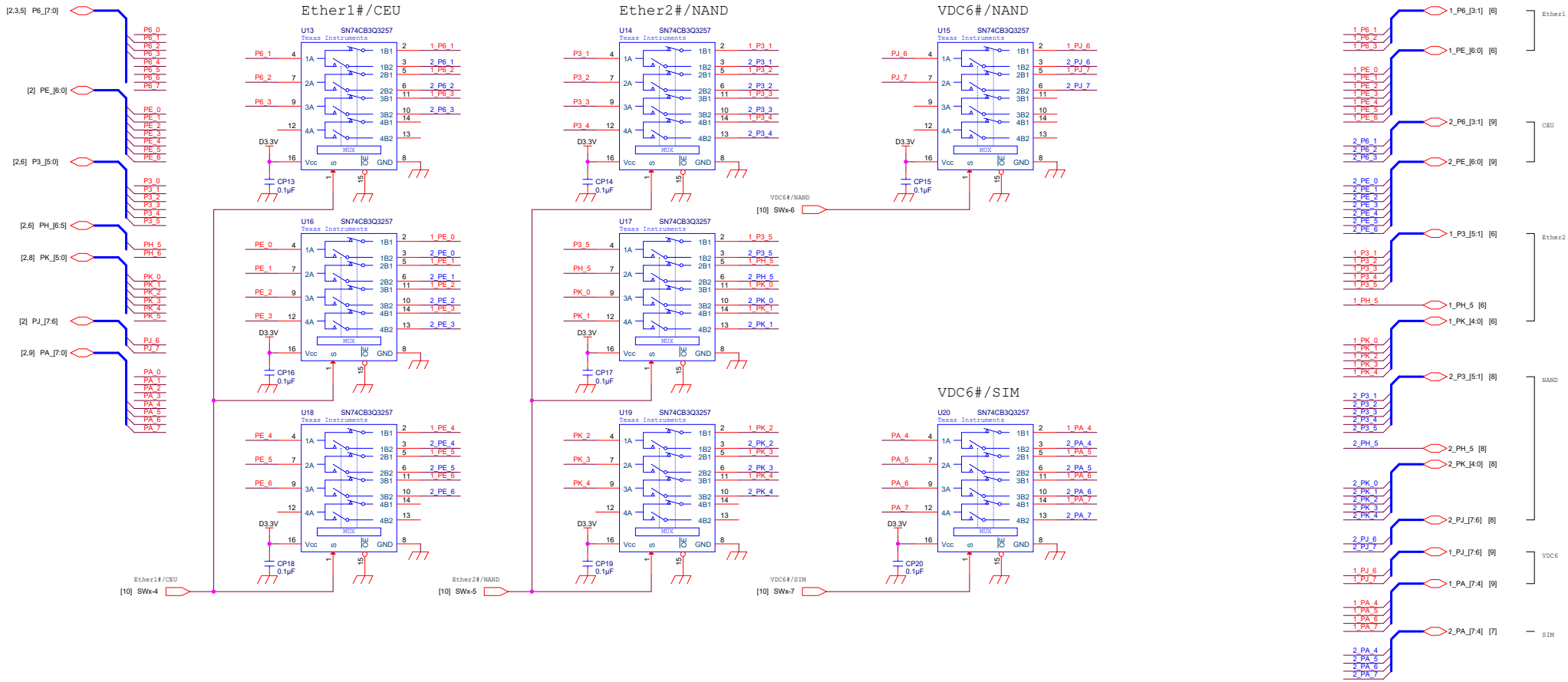
CHANGE		SCALE		Renesas Electronics Corporation.				RZ/A2M SUB board
				DRAWN	CHECKED	DESIGNED	APPROVED	INDEX
		DATE	18-10-09					R20UT4395EJ0100
								(1 / 10)



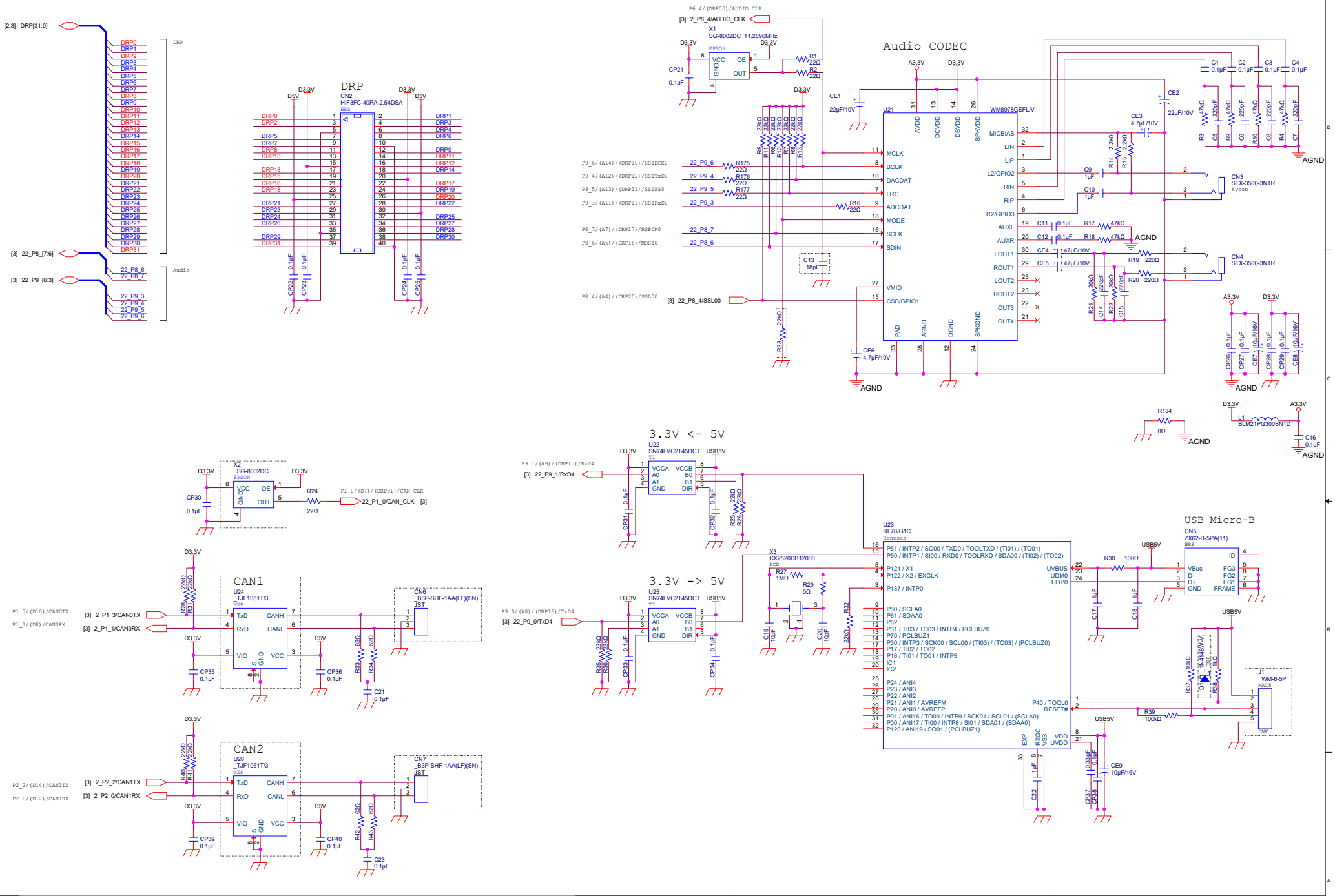
CHANGE		SCALE		DATE 18-10-09	Renesas Electronics Corporation.				RZ/A2M SUB board
					DRAWN	CHECKED	DESIGNED	APPROVED	SODIMM Connector
									R20UT4395EJ0100
									(2 / 10)



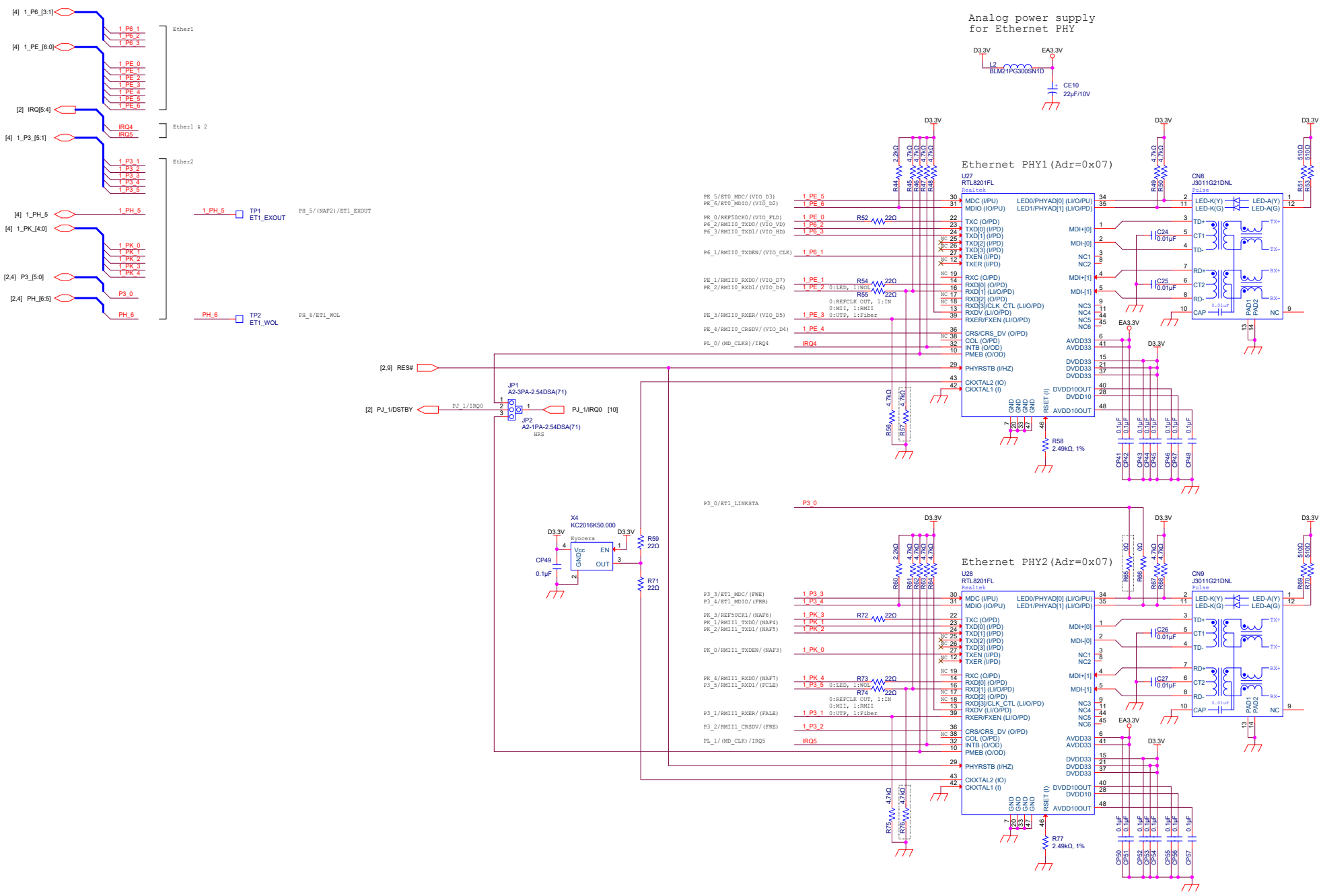
CHANGE			Renesas Electronics Corporation.			RZ/A2M SUB board
			DRAWN	CHECKED	DESIGNED	APPROVED	MUX1 (SDRAM#/Other)
	SCALE						R20UT4395EJ0100
	DATE	18-10-09					(3 / 10)



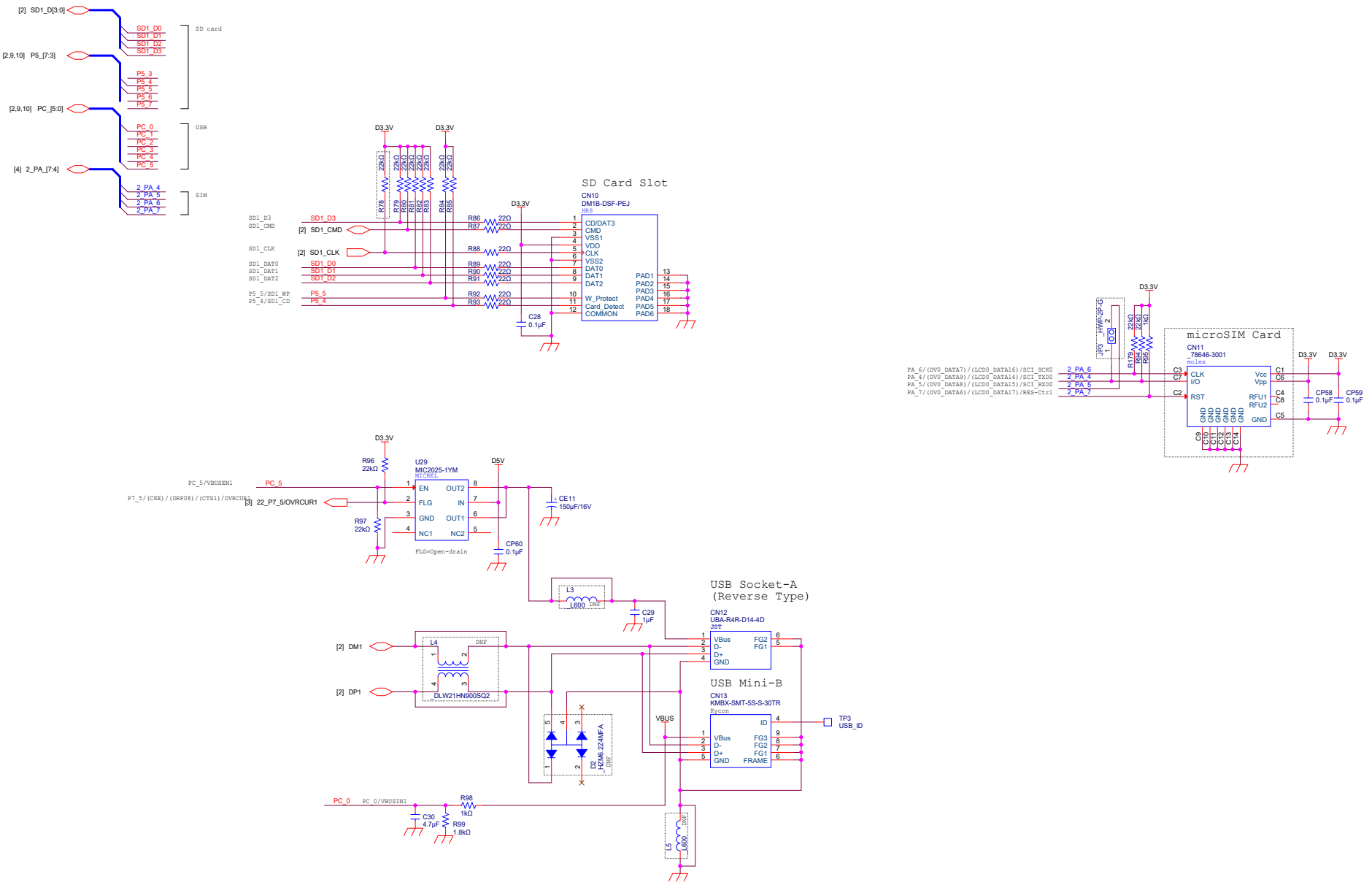
CHANGE			Renesas Electronics Corporation.				RZ/A2M SUB board
			DRAWN	CHECKED	DESIGNED	APPROVED	MUX2(Ether#, VDC6#/CEU, NAND, SIM)
		SCALE					R20UT4395EJ0100
		DATE	18-10-09				(4 / 10)



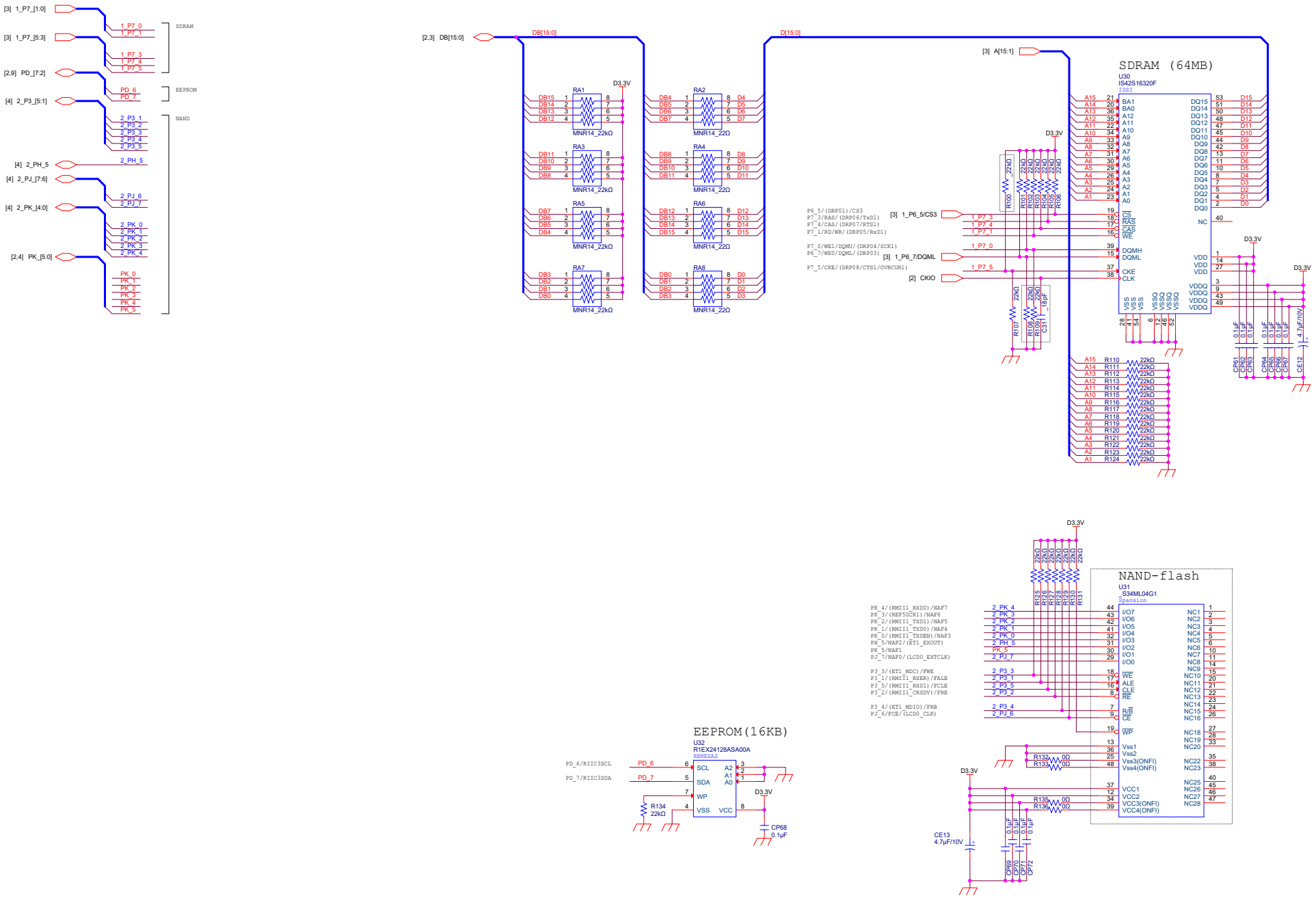
CHANGE			Renesas Electronics Corporation.		RZ/A2M SUB board
			DRAWN	CHECKED / DESIGNED / APPROVED	DRP, Audio, CAN, UART
	SCALE				R20UT4395EJ0100
	DATE	18-10-09			(5 / 10)



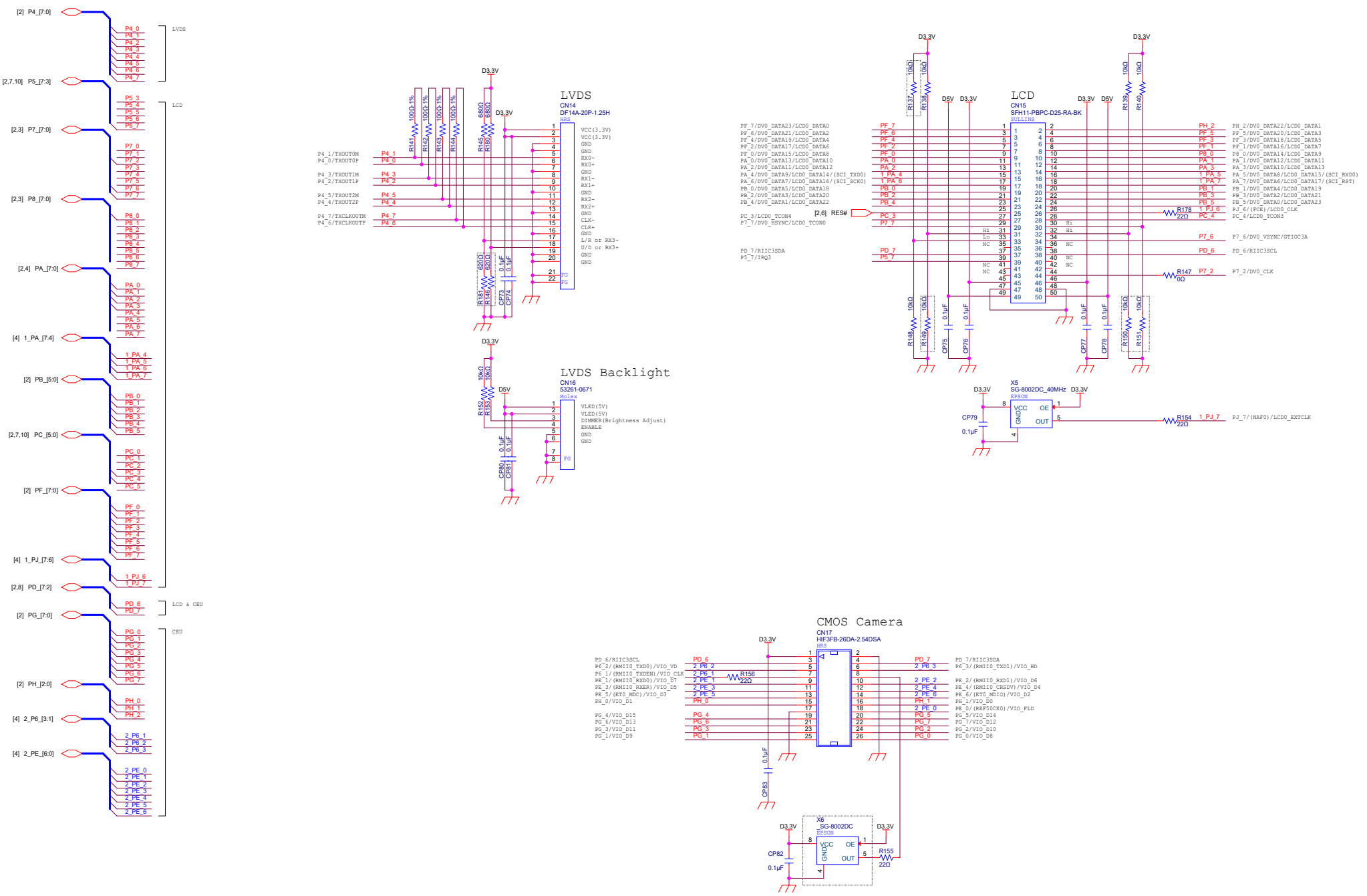
CHANGE			Renesas Electronics Corporation.		RZ/A2M SUB board
			DRAWN	CHECKED / DESIGNED / APPROVED	Etrhernet
	SCALE				R20UT4395EJ0100
	DATE	18-10-09			(6 / 10)



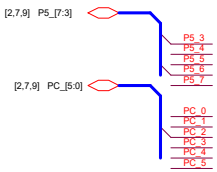
CHANGE			Renesas Electronics Corporation.		RZ/A2M SUB board
			DRAWN	CHECKED / DESIGNED / APPROVED	SD, SIM, USB
	SCALE				R20UT4395EJ0100
	DATE	18-10-09			(7 / 10)

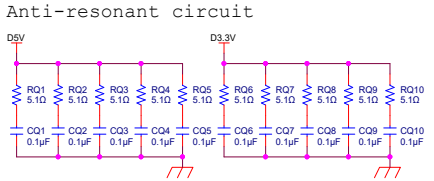


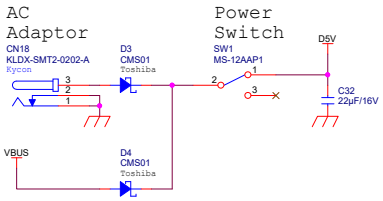
CHANGE			Renesas Electronics Corporation.		RZ/A2M SUB board
			DRAWN	CHECKED / DESIGNED / APPROVED	Memory(EEPROM, NAND, SDRAM)
	SCALE				R20UT4395EJ0100
	DATE	18-10-09			(8 / 10)

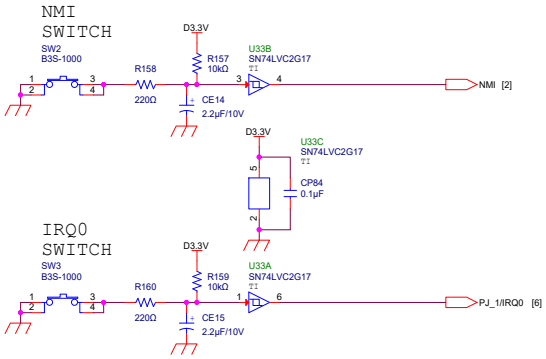


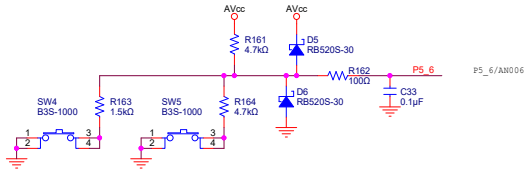
CHANGE			Renesas Electronics Corporation.		RZ/A2M SUB board
			DRAWN	CHECKED / DESIGNED / APPROVED	CMOS, LCD, LVDS
	SCALE				R20UT4395EJ0100
	DATE	18-10-09			(9 / 10)

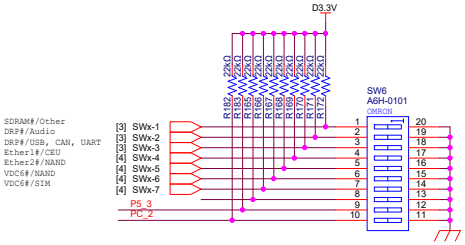


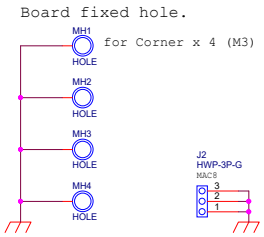






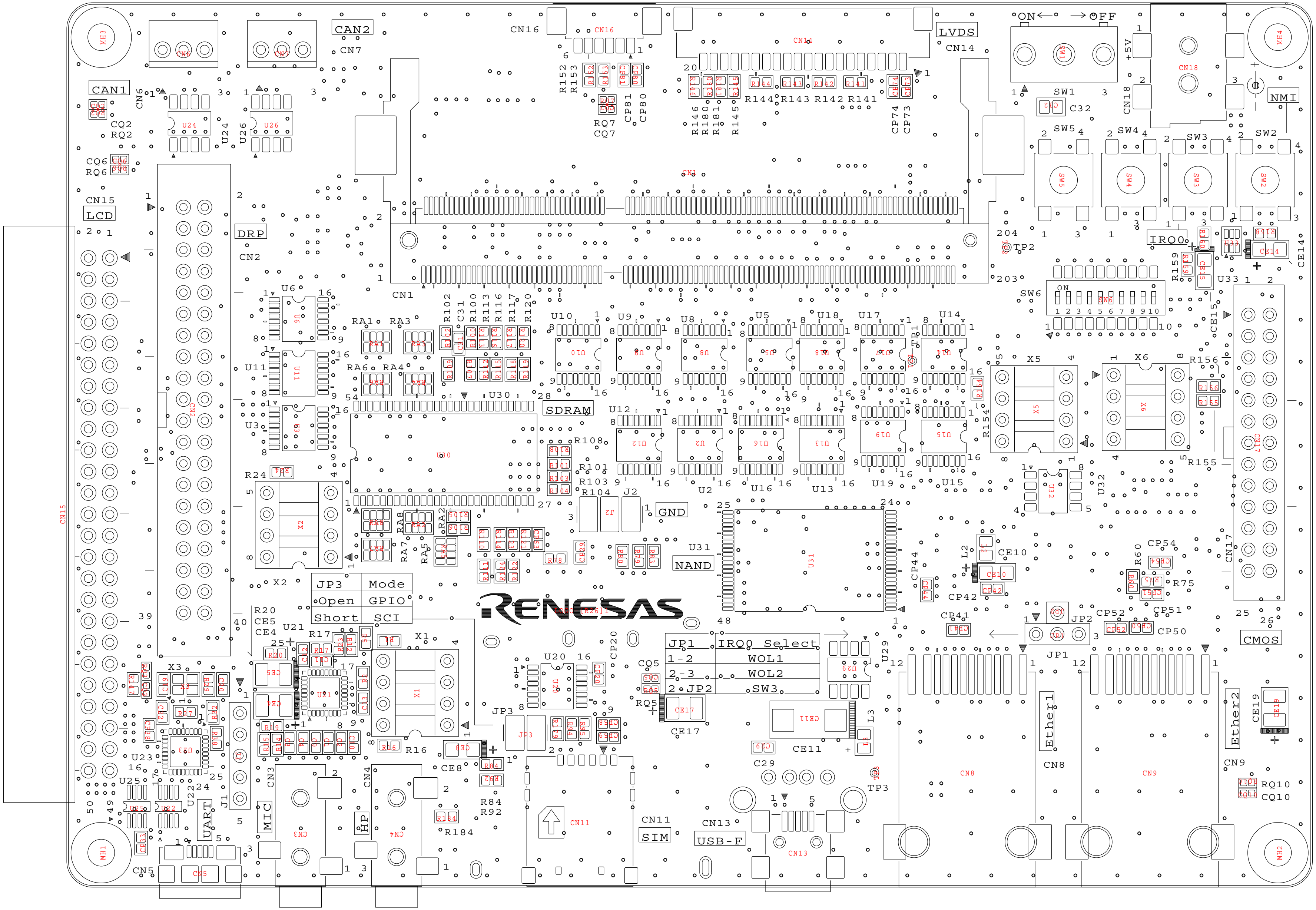




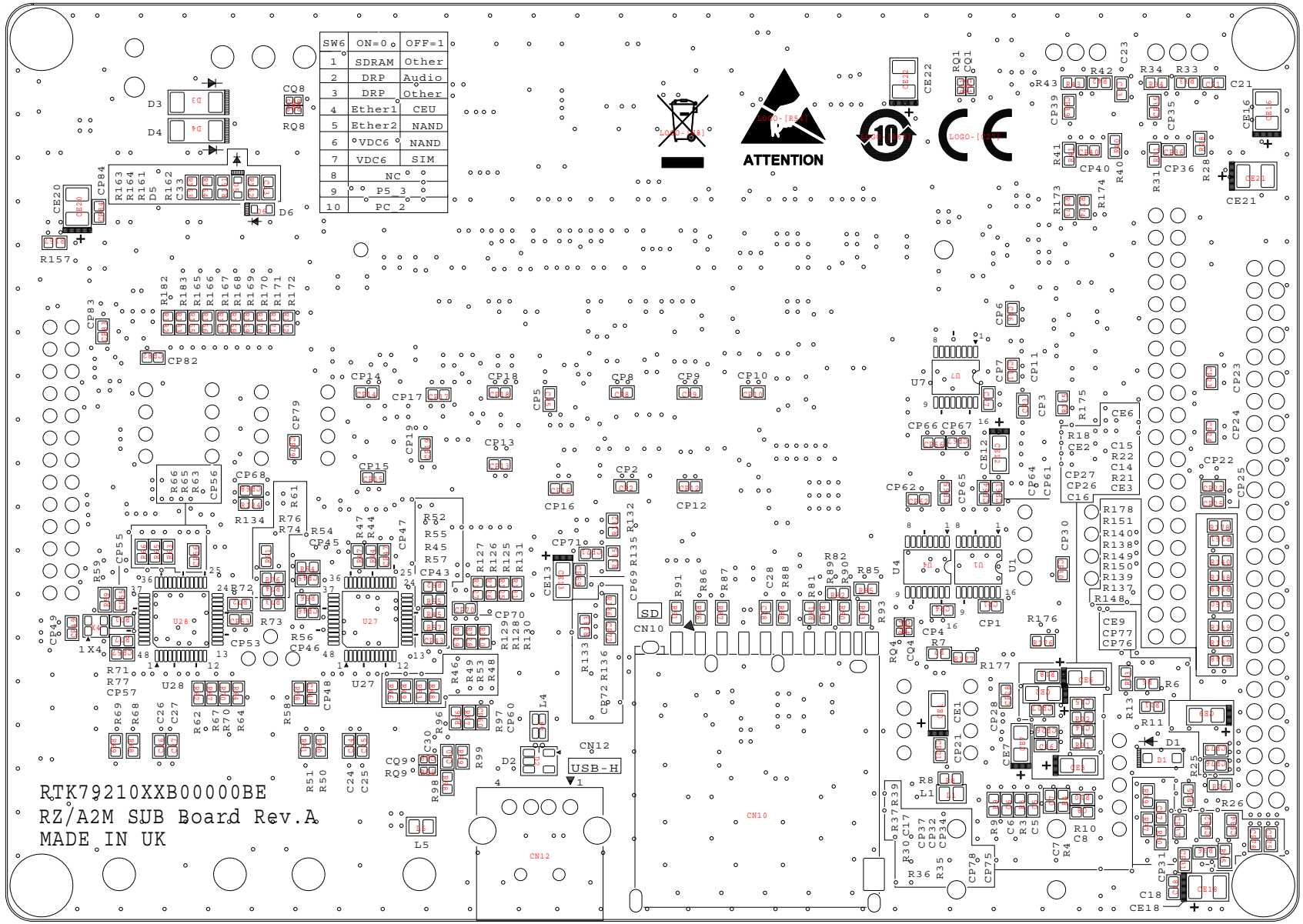


CHANGE				Renesas Electronics Corporation.				RZ/A2M SUB board
				DRAWN	CHECKED	DESIGNED	APPROVED	Power, SW
		SCALE						R20UT4395EJ0100
		DATE	18-10-09					(10 / 10)

Appendix 2 RTK79210XXB00000BE Component Installation Diagram



CAN1
CAN2
CN7
CN6
CN16
LVDS
CN14
ON
OFF
SW1
C32
+5V
CN18
NMI
SW5
SW4
SW3
SW2
CQ2
RQ2
CQ6
RQ6
U24
U26
CN15
LCD
DRP
CN2
CN1
TP2
IRQ0
U33
SW6
R152
R153
RQ7
CQ7
CP81
CP80
R144
R143
R142
R141
R146
R180
R181
R145
CP74
CP73
U6
U11
U3
RA1
RA3
RA6
RA4
R102
C31
R100
R113
R116
R117
R120
U30
SDRAM
U10
U9
U8
U5
U18
U17
U14
X5
X6
R156
R155
R154
U12
U2
U16
U13
U19
U15
U32
R108
R101
R103
R104
J2
GND
R24
X2
RA8
RA7
RA5
RA2
U31
NAND
CE10
CP44
CP42
CP41
CP54
R60
R75
CP52
CP51
CP50
CN17
CMOS
JP2
JP1
CE15
R159
CE14
JP3 | Mode
Open | GPIO
Short | SCI
RENESAS
JP1 | IRQ0 Select
1-2 | WOL1
2-3 | WOL2
2 • JP2 | SW3
R20
CE5
CE4
U21
R17
X1
X3
U20
CP20
CQ5
RQ5
CE17
CE11
L3
U29
Ether1
CN8
Ether2
CN9
CE19
RQ10
CQ10
U23
U25
U22
UART
J1
MIC
CN3
HP
CN4
R16
CE8
R84
R92
R184
JP3
CN11
SIM
CN13
USB-F
C29
TP3
CN5


SW6 ON=0 OFF=1
1 SDRAM Other
2 DRP Audio
3 DRP Other
4 Ether1 CEU
5 Ether2 NAND
6 VDC6 NAND
7 VDC6 SIM
8 NC
9 P5_3
10 PC_2
ATTENTION
RTK79210XXB00000BE
RZ/A2M SUB Board Rev.A
MADE IN UK

Revision History	RZ/A2M SUB Board RTK79210XXB00000BE User's Manual

Rev.	Date of issue	Revised content	
		Page	Point
1.00	2018.10.11	—	Issue of first version
1.10	2018.12.21	2-22	Table 2.3.5: Recommended setting of AC characteristics adjustment register (ACADJ) corrected
		2-22	Table 2.3.6: GPIO Settings added
1.20	2019.07.17	—	Added notes on USB power supply
		1-2	- 1.2 Configuration
		2-32	- 2.9 Power Voltage Configuration
		—	Unused HM_INT# and HM_RSTO# pins
		2-7	- Table 2.2.6, E2 pin
		2-9	- Table 2.2.8, K3 pin
		—	Correction of mistakes
2.00	2019.12.06	Overall	Updated silk screen
		1-2	1.2: Deleted notes on USB power supply
		2-2	Table 2.2.1: Corrected comments of A6 pin
		2-7	Table 2.2.6: Corrected pin function and description of E2 pin
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