User's Manual

RZ SMARC Series Carrier Board II

User's Manual: Hardware

Renesas Microprocessor
RZ Family / RZ/G Series

Renesas Electronics
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Precautions

This Evaluation Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area, or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

• Ensure attached cables do not lie across the equipment.

• Reorient the receiving antenna.

• Increase the distance between the equipment and the receiver.

• Connect the equipment into an outlet on a circuit different from that which the receiver is connected.

• Power down the equipment when not in use.

• Consult the dealer or an experienced radio/TV technician for help.

Note: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken:

• The user is advised that mobile phones should not be used within 10 m of the product when in use.

• The user is advised to take ESD precautions when handling the equipment.

The Evaluation Kit does not represent an ideal reference design for an end product and does not fulfill the regulatory standards for an end product.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. Introduction

The RZ SMARC Series Carrier Board II (hereinafter referred to as "RZ SMARC Carrier II") is an 8-layer 190x130mm PCB, a platform designed according to the SMARC 2.1.1 Specification providing a carrier for Renesas RZ SMARC Module boards.

Basically, the RZ SMARC Carrier II is connected to the Renesas RZ/G3S SMARC Module board (hereinafter referred to as "G3S SMARC Module") and used as the RZ/G3S SMARC Evaluation Board (hereinafter referred to as "G3S SMARC EVK").

This guide is based on a combination of the RZ SMARC Carrier II and the G3S SMARC Module.

This guide includes system setup and configuration. This guide also provides detailed information on the overall design and use of the RZ SMARC Carrier II from a hardware system perspective.

Details of the RZ/G3S SMARC Module board are to be found in the **RZ/G3S SMARC Module Board Kit User's Manual**.

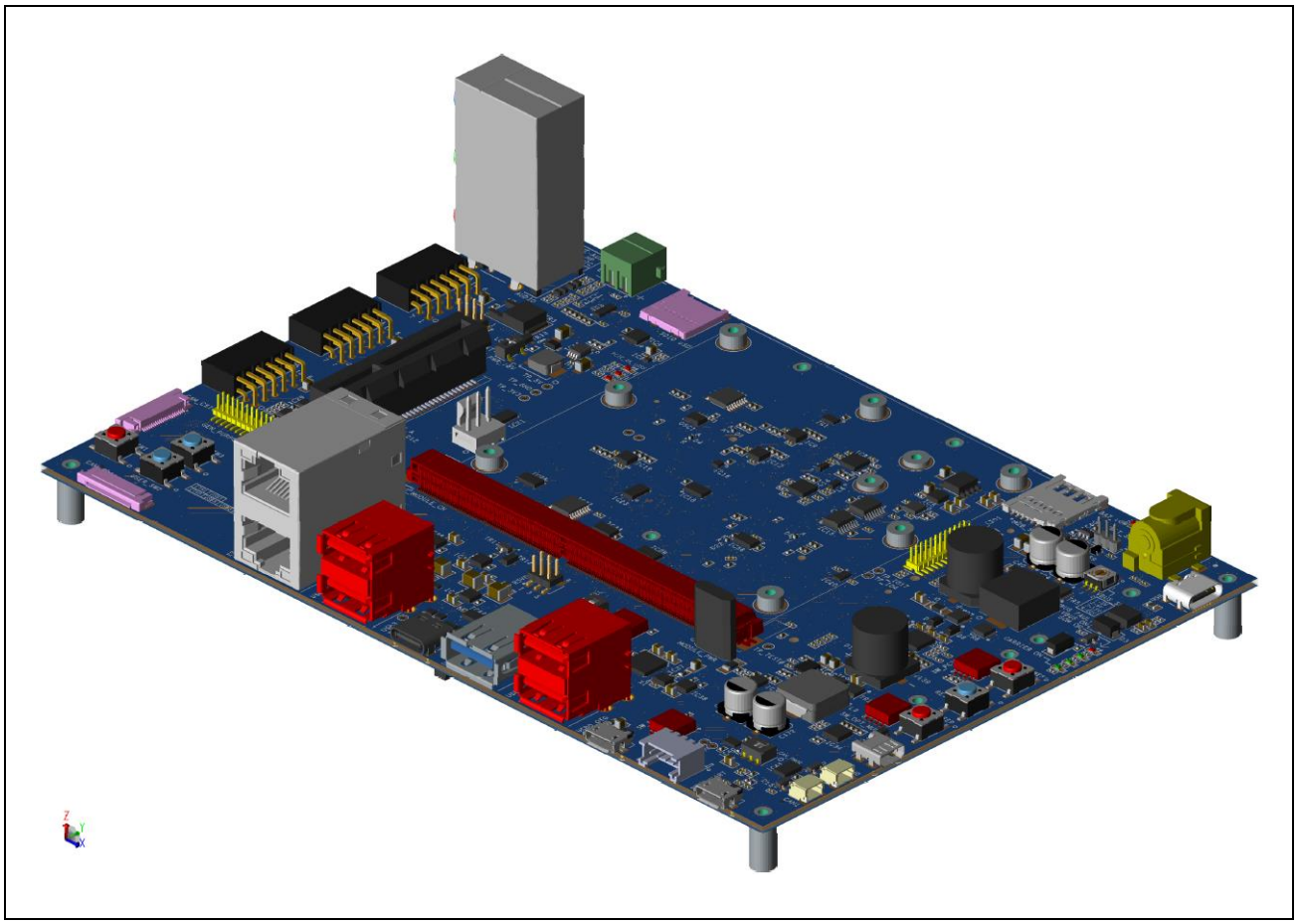

Figure 1.1 RZ SMARC Series Carrier Board II

The key features of the RZ SMARC Carrier II are as follows.

Board Features	Details
Power supply	USB Type-C with USB-PD support (input range: 5V2A to 20V4A)
Memory	Micro SD card slot with default, high-speed, UHS-I/SDRR50, SDR104 transfer modes support
Supported interface and peripherals	4x USB2.0 Host interface, Type A
	1x USB2.0 OTG interface, Type microAB
	1x USB3.2 Host interface, Type A
	1x USB3.2 OTG interface, Type C
	Speaker, Headphone, Microphone, Auxiliary
	2x Gigabit Ethernet interface supporting 10/100/1000 Mbps data rate on the RJ45 connector
	PCIe 4-lane slot
	M.2 Key E interface
	M.2 Key B interface and SIM card interface
	2x CAN interface
	2x UART interface for debugging (1 is micro-USB)
	2x LVDS/MIPI-DSI display connector (Support MIPI-DSI to HDMI in channel 0)
	HDMI interface
	2x MIPI CSI-2 camera connector
	3x PMOD connectors (Type-2A SPI, Type-3A UART and Type-6A I2C)
Expansion connectors/headers	Coin cell battery holder
	GPIO pin header
	GPIO pin header for M.2 Key B
	ISL28022FRZ current monitor for the module power supply
Board dimensions	190mm(W) * 130mm(L), 8-layer

1.1 Kit Contents

The following components are included in the RZ SMARC Series Carrier Board II Kit (P/N: RTK9SMCBB2B01000BE).

- RZ SMARC Series Carrier Board II
  - Fitted with RZ SMARC Series MIPI-DSI to HDMI conversion adaptor board (P/N: RTK9SMCABDB00000BE) to DISP0
    (hereinafter referred to as "SMARC MIPI-DSI to HDMI Adaptor")
- USB Type-A to USB Micro B cable for serial debug
- Accessories bag:
  - 7off M2.5 x4mm pan-head machine screws (for securing SMARC Module)
  - 2off M2.5 x6mm pan-head machine screws (for securing M.2 cards)
  - 1off 2.5mm spacer (for securing M.2 key B cards)

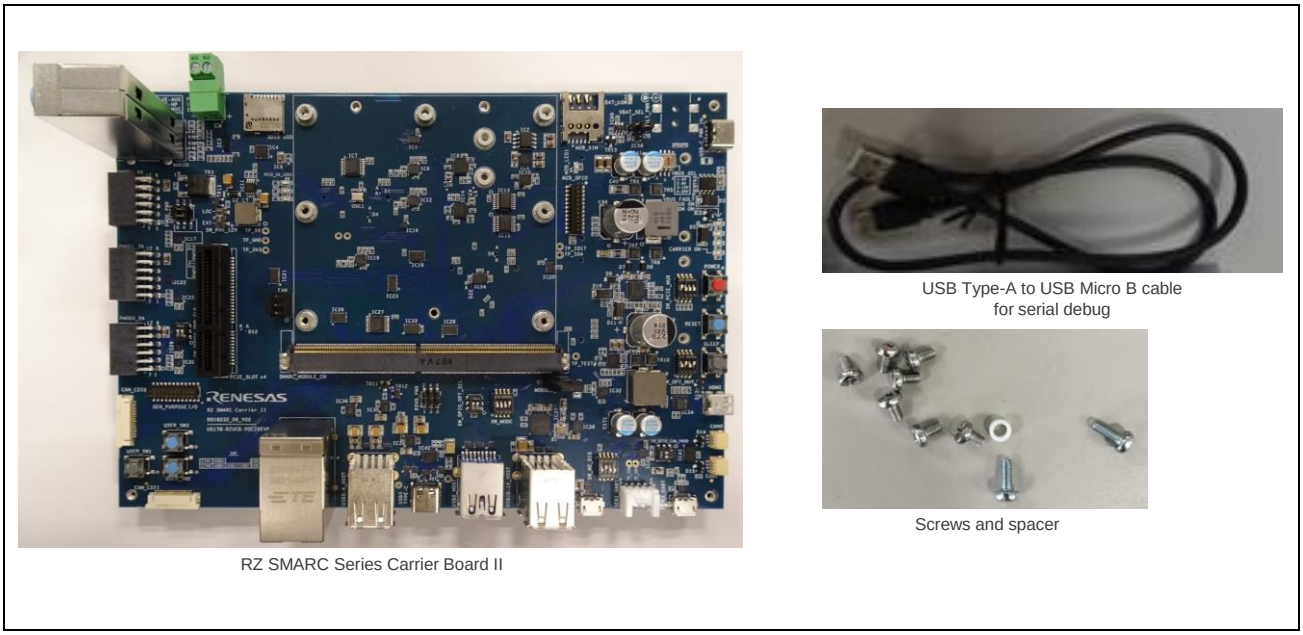

Figure 1.2 RZ SMARC Series Carrier Board II Kit Contents

If you have purchased the RZ/G3S SMARC Evaluation Board Kit, your contents will include:

- RZ/G3S SMARC Carrier Board II Kit (P/N: RTK9SMCB02000BE)
  - RZ SMARC Series Carrier Board II
  - USB Type-A to USB Micro B cable for serial debug
  - Accessories bag:
    - 2off M2.5 x6mm pan-head machine screws (for securing M.2 cards)
    - 1off 2.5mm spacer (for securing M.2 key B cards)

- RZ/G3S SMARC Module Board Kit (P/N: RTK9843S33C01000BE)
  - RZ/G3S SMARC Module board
  - RZ SMARC Series JTAG adaptor cable (P/N: RTK9SMCABJB00000BE)

NOTE

The Module will have been fitted to the Carrier using the 7off M2.5 x4mm pan-head machine screws.

1.2 Assembly

The RZ SMARC Carrier II can only be used when fitted with a SMARC compliant Module board.

Secure the Module using 7off M2.5 x4mm pan-head machine screws (provided).

2. System Description

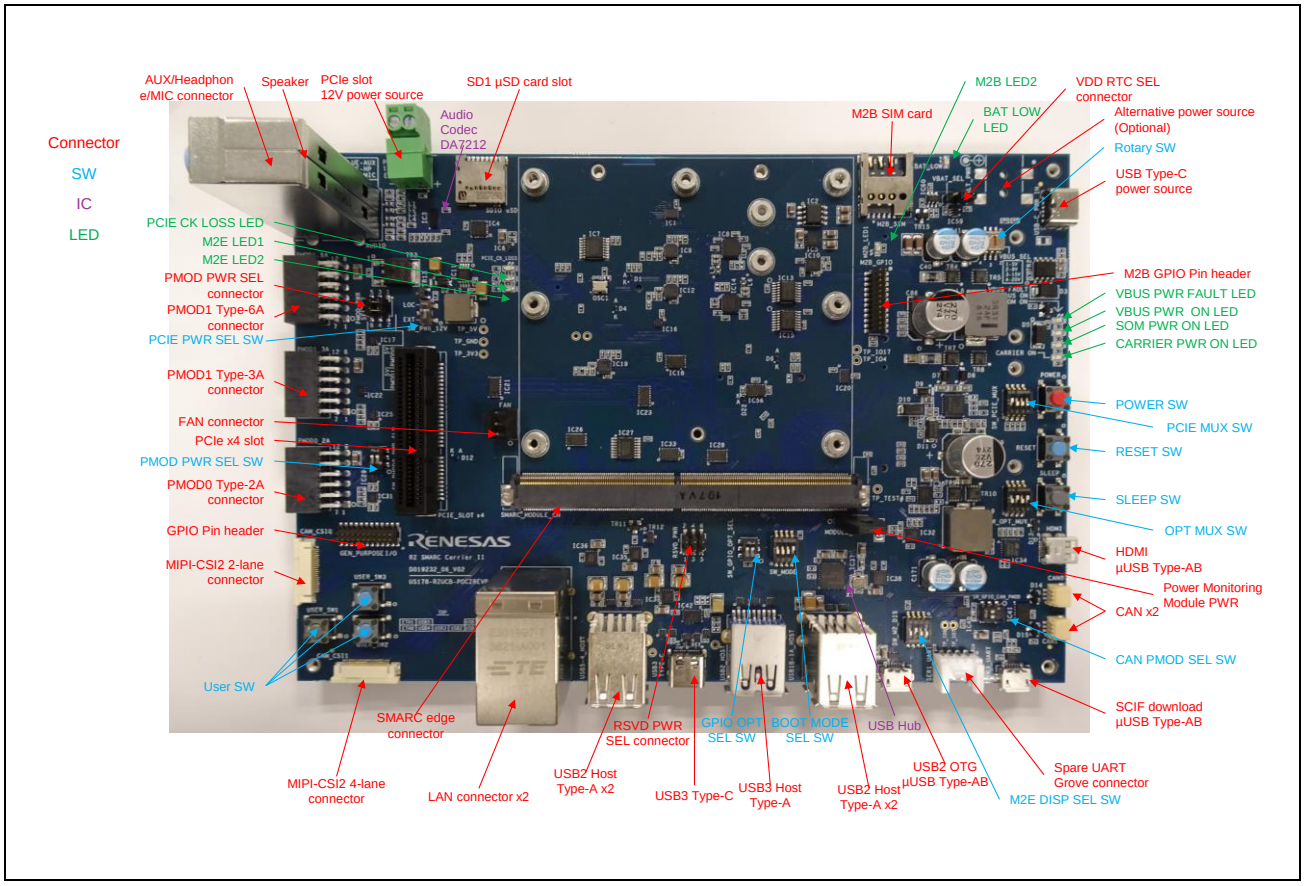

Figure 2.1 RZ SMARC Series Carrier Board II Top View

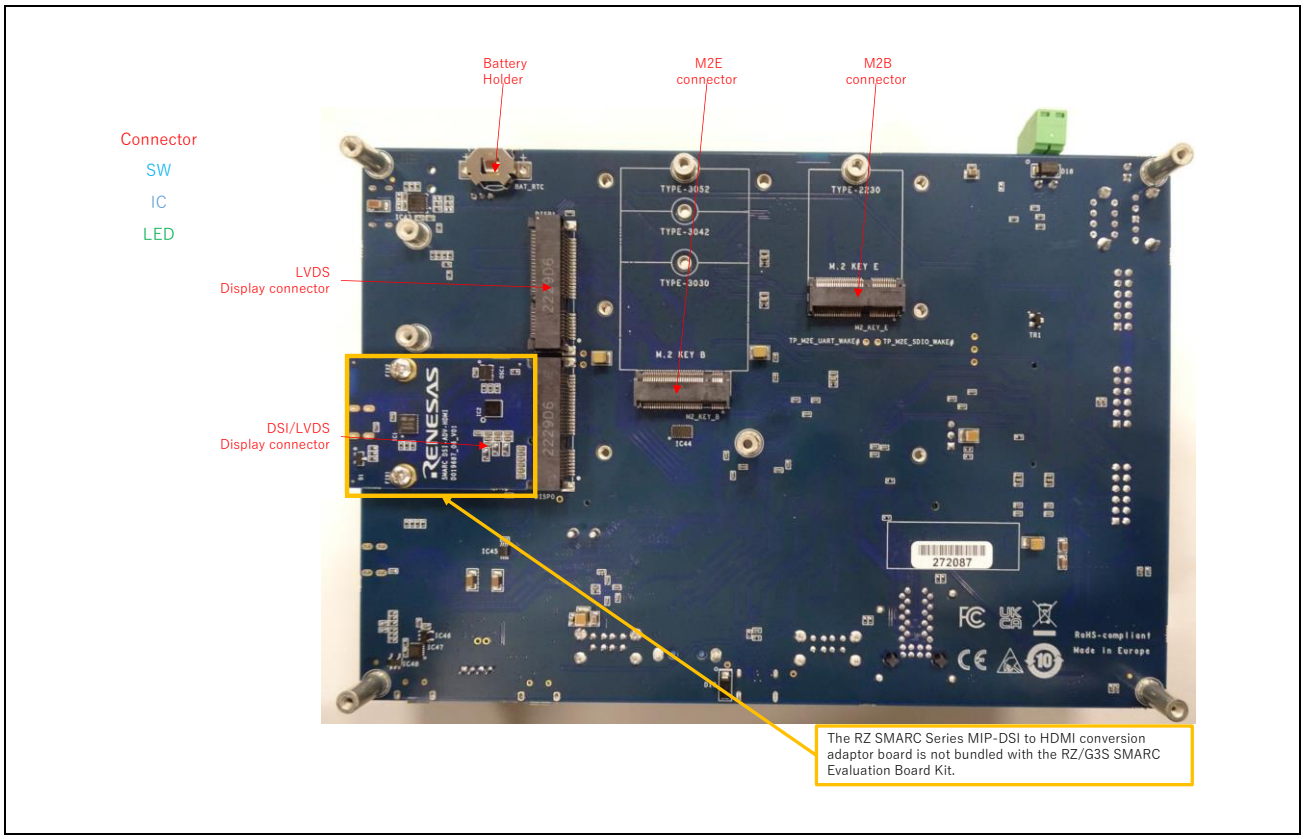

Figure 2.2 RZ SMARC Series Carrier Board II Bottom View

2.1 G3S SMARC EVK Functional Block

Figure 2.3 shows the functional block diagram of the G3S SMARC EVK. ICs, connectors and switches surrounded by red frame indicate functions used on the RZ SMARC Carrier II.

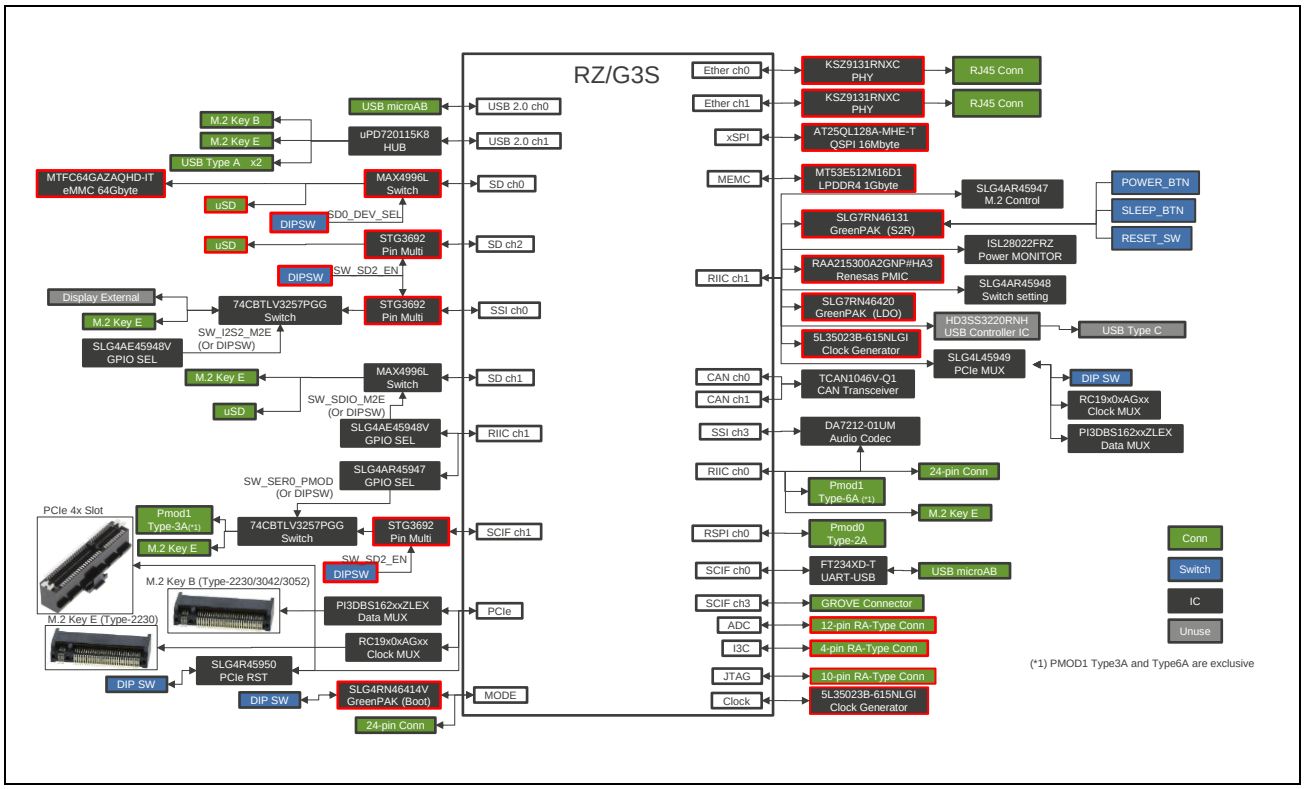

Figure 2.3 G3S SMARC EVK Block Diagram

2.2 G3S SMARC EVK Interface Mapping

Renesas parts are highlighted.

Table 2.1 Interface Mapping (1/2)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description
USB0	USB2.0 ch0	629105150921	USB Type-microB receptacle
USB1	USB2.0 ch1	uPD720115K8-711-BAK-A	USB Hub IC
		72309-8014BLF	USB Type-A receptacle
CAN0	CAN ch0	TCAN1046VDMTRQ1	CAN transceiver
		SM03B-SRSS-TB(LF)(SN)	3-pin connector
CAN1	CAN ch1	SM03B-SRSS-TB(LF)(SN)	3-pin connector
I2S0	SSI ch3	DA7212-01UM	Audio Codec
		STX-4335-5BGP-S1	Stereo Headphone, Stereo Mic, Aux for connector
		M20-9990246	Speaker for pin header
I2S2	SSI ch0	MDT420B01001	M.2 Key E for I2S interface
SPI1	RSPI ch0	SSW-106-02-T-D-RA	PMOD Type-2A connector
SER0	SCIF ch1	SSW-106-02-T-D-RA	PMOD Type-3A connector
SER1	SCIF ch3	110990037	Grove connector
SER3	SCIF ch0	FT234XD-T	USB to UART conversion IC
		629105150921	UART Debug for USB Type-microB receptacle
PCIE_A	PCIe Gen2	10061913-111PLF	PCIe 4x Slot
		MDT420B01001	M. 2 Key B
		MDT420E01001	M. 2 Key E
		78646-3001	SIM card for M. 2 Key B
		MDT420B01001	M. 2 Key B
GBE0	Ether ch0	KSZ9131RNXC	Ethernet PHY
		2301997-7	Stacked RJ45 connector
GBE1	Ether ch1	KSZ9131RNXC	Ethernet PHY
I2C_GP	RIIC ch0	GRPB122VWQS-RC	GPIO pin header
		MDT420B01001	M. 2 Key E for I2C interface
		DA7212-01UM	Audio Codec for I2C interface
		SSW-106-02-T-D-RA	PMOD Type-6A connector
I2C_PM	RIIC ch1	ISL28022FRZ	Current monitor for measuring SMARC module
		SLG4L45949	GreenPAK (PCIe Data Multiplexing Control, PCIe Slot Enable, M.2 Key E Enable, M.2 Key B Enable)
		SLG4R45950	yGreenPAK (PCIe Slot Reset, M.2 Key E Reset, M.2 Key B Reset)
		SLG4AE45947	GreenPAK (GPIO and SER0 Multiplexing Control, M.2 Key B Reset/Power off, M.2 Key E Disable)
		SLG4AE45948	GreenPAK (M.2 Key B Configuration Decoding, USB2, I2S2 and SDIO Multiplexing Control, USB1 Hub Enable)
		RAA215300A2GNP#HA3	PMIC
		SLG7RN46420	GreenPAK (Power Regulator)
		SLG7RN46131	GreenPAK (Power/Reset control)
		ISL28025FRZ	Current monitor for measuring five power rails on SMARC module

Table 2.1 Interface Mapping (2/2)

SMARC Interface Name	RZ/G3S I/F	Device Part Number	Description
—	SD/MMC ch0	1040310811	USB Type-microB receptacle
		MTFC64GASAQHD-IT	64GB eMMC memory
SDIO	SD/MMC ch1	1040310811	USB Type-microB receptacle
—	SD/MMC ch2	1040310811	USB Type-microB receptacle
—	MEMC	MT53E512M16D1FW-046WT	1GB LPDDR4 SDRAM
—	xSPI	AT25QL128A-MHE	128Mbit Quad SPI flash memory
—	ADC	SM12B-SRSS-TB(LF)(SN)	12-pin connector
—	I3C	SM04B-SRSS-TB(LF)(SN)	4-pin connector
—	JTAG	10051922-1010EHLF	10-pin connector
—	CPG	5L35023B-615NLGI	Clock generator
		830208214909	AUDIO_CLK2 for oscillator
—	Power	ISL28025FRZ	Current monitor for measuring five power rails on the SMARC module
		FT232HQ-REEL	USB to I2C conversion IC
		629105150921	USB Type-microB receptacle

2.3 Board Configuration and Status

The RZ SMARC Carrier II has many switched configuration options and on-board interfaces. These are described in detail in the following sections.

Default settings are highlighted.

2.3.1 VBUS_SEL – Main Power

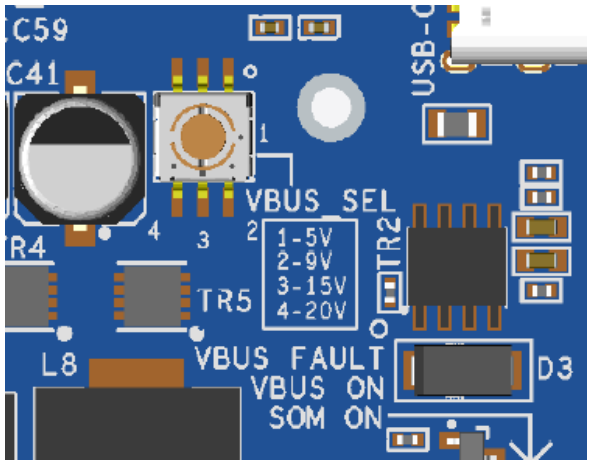

Figure 2.4 The Location and the Default Setting of the VBUS_SEL

The primary power input for the RZ SMARC Carrier II is from the USB Type-C connected to a power delivery device (not provided).

The specification for the USB Type-C power adaptor is dependent on the requirements for the SMARC Module and peripheral boards connected.

Ensure the following switch settings match the minimum power requirements and USB Type-C power adaptor capabilities.

Table 2.2 Power Requirements for Each Switch Setting

SW_MODE[4]	VBUS_SEL	Min. Voltage	Min. Current	Min. Power
ON	1	5 V	2 A	10 W
ON	2	9 V	2 A	18 W
ON	3	15 V	2 A	30 W
ON	4	20 V	2 A	40 W
OFF	1	5 V	4 A	20 W
OFF	2	9 V	4 A	36 W
OFF	3	15 V	4 A	60 W
OFF	4	20 V	4 A	80 W

2.3.2 VBAT_SEL – VDD_RTC Power

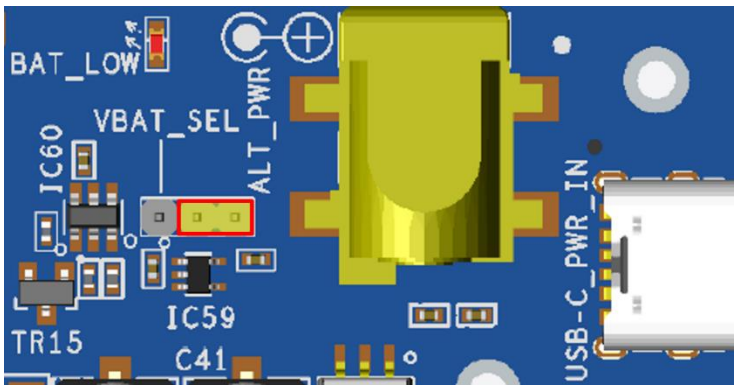

Figure 2.5 The Location and the Default Setting of the VBAT_SEL

The power to the SMARC Module required for VDD_RTC may be provided by a regulator or coin cell battery (not provided).

The power source selection is made with a 2mm header fitted to VBAT_SEL header.

Table 2.3 Jumper Pin “VBAT_SEL” Settings

VBAT_SEL Header Link	VDD_RTC Source
Pin 1 – Pin 2	A coin cell battery must be fitted to BAT_RTC
Pin 2 – Pin 3	An on-board regulator provides 2.8 V *Note*: Power is removed when the main power is disconnected.

2.3.3 SW_PWR_12V – PCIe Slot Power

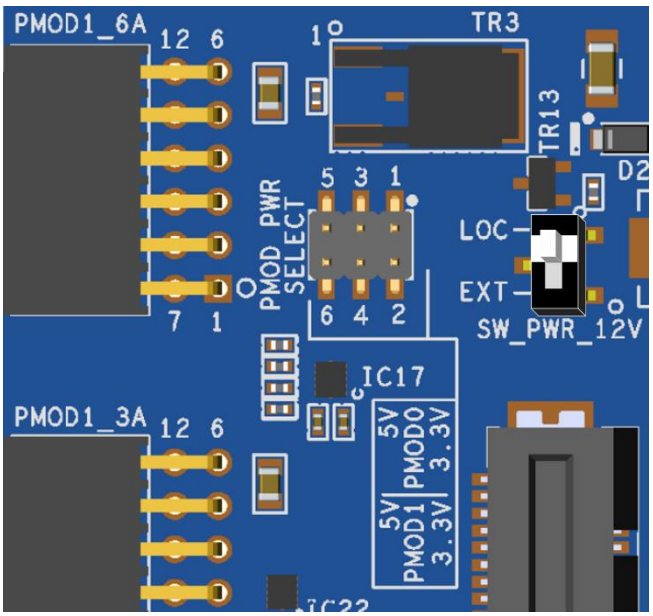

Figure 2.6 The Location and the Default Setting of the SW_PWR_12V

The 12V power supply to the PCIe Slot may be provided by a regulator or external supply.

The power source is selected with SW_PWR_12V.

Table 2.4 Jumper Pin “SW_PWR_12V” Settings

SW_PWR_12V	PCIe Slot 12V Source
ON	An externally 12V supply must be connected to PWR_12V_EXT Required for PCIe cards >10W
OFF	An on-board regulator provides 12V @0.5A *Note*: PCIe plug-in card is limited to 10W.

2.3.4 RSVD_PWR – Module Power

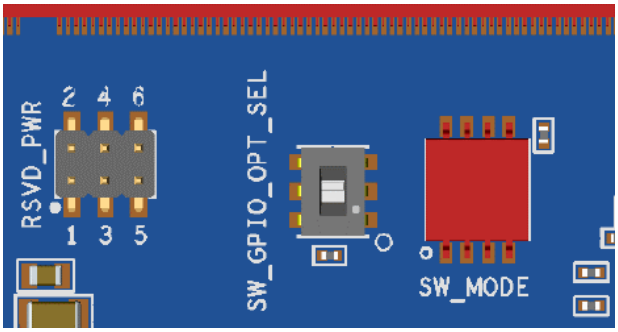

Figure 2.7 The Location and the Default Setting of the RSVD_PWR

The SMARC specification restricts the module power to 25W (5.0V, 10 pins @0.5A). However, the RZ SMARC Carrier II can make use of the Module RSVD pins and increase this value.

Table 2.5 Jumper Pin “RSVD_PWR” Settings

RSVD_PWR Header Link	Max. SMARC Module Power
Pin 1 – Pin 2	32.5 W
Pin 3 – Pin 4	*Note*: For use with compatible SMARC Modules only.
Pin 5 – Pin 6	
No headers fitted	25 W

2.3.5 PMOD_PWR_SEL – PMOD Power

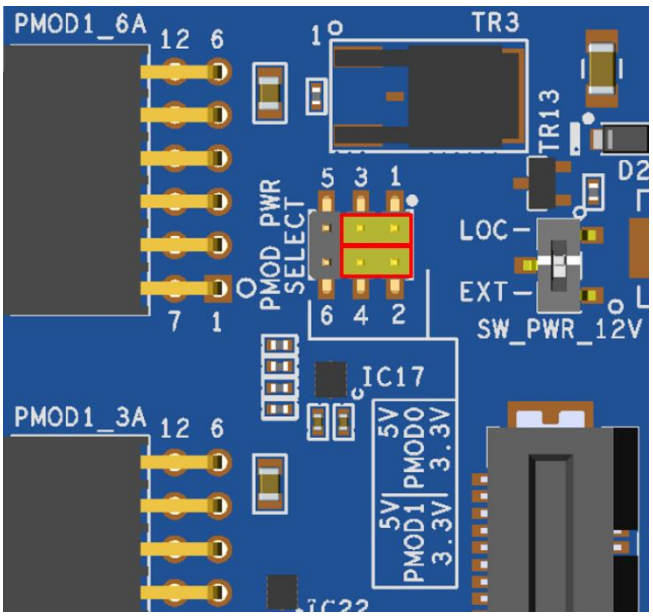

Figure 2.8 The Location and the Default Setting of the PMOD_PWR_SEL

PMOD interfaces support either 3.3 V or 5.0 V.

A 2mm header is used to select the power level for PMOD0 (Type-2A) and another 2mm header is used to select the power level for PMOD1 (Type-3A and Type 6A).

Table 2.6 Jumper Pin “PMOD_PWR_SEL” Settings (1/2)

PMOD_PWR_SEL Header Link	PMOD0 Power Level
Pin 1 – Pin 3	3.3 V
Pin 3 – Pin 5	5.0 V

Table 2.6 Jumper Pin “PMOD_PWR_SEL” Settings (2/2)

PMOD_PWR_SEL Header Link	PMOD1 Power Level
Pin 2 – Pin 4	3.3 V
Pin 4 – Pin 6	5.0 V

2.3.6 SW_PMOD0_PWR_SLP – PMOD Power/Sleep Control

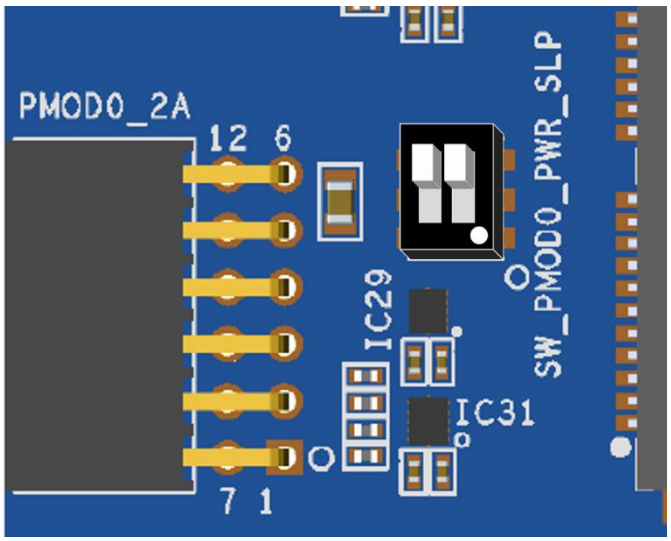

Figure 2.9 The Location and the Default Setting of the SW_PMOD0_PWR_SLP

PMOD0 has the capability to drive the POWER_BTN# and SLEEP# signals of the RZ SMARC Carrier II by configuring SW_PMOD0_PWR_SLP.

Table 2.7 DIP Switch “SW_PMOD0_PWR_SLP” Setting (1/2)

SW_PMOD0_PWR_SLP-1	PMOD0_GPIO/CS2 (Pin 9)
1 – 2	Connected to POWER_BTN#
2 – 3	Connected to GPIO6

Table 2.7 DIP Switch “SW_PMOD0_PWR_SLP” Setting (2/2)

SW_PMOD0_PWR_SLP-2	PMOD0_GPIO/CS3 (Pin 10)
4 – 5	Connected to SLEEP#
5 – 6	Connected to GPIO7

2.3.7 SW_GPIO_OPT_SEL – GPIO Options

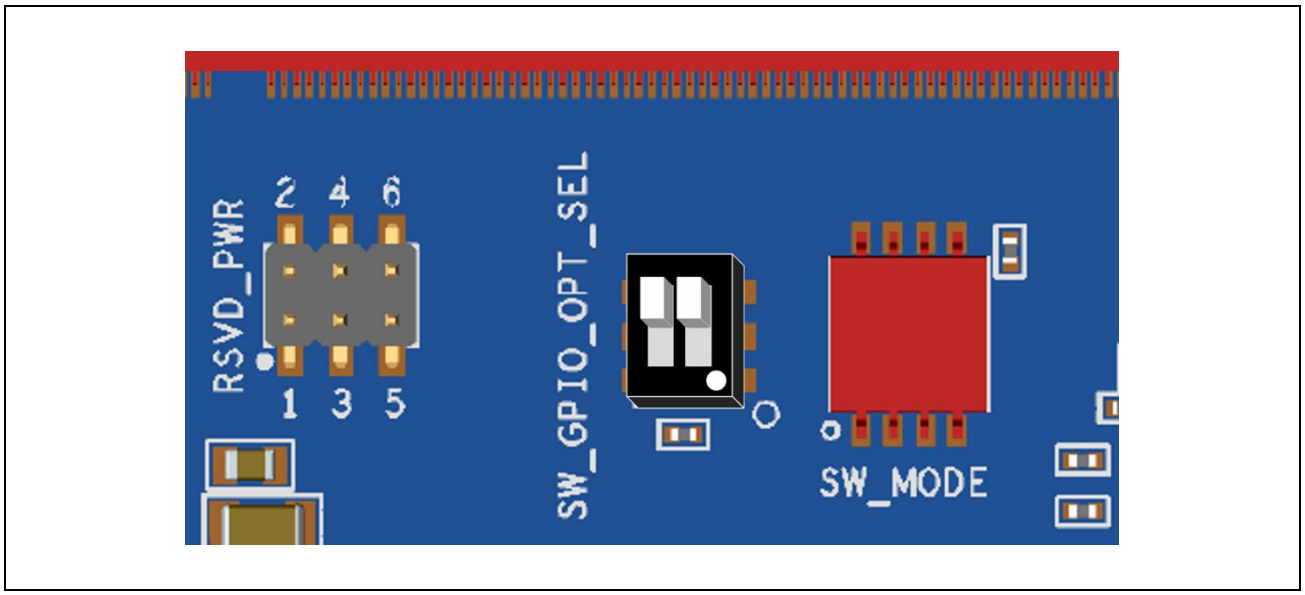

Figure 2.10 The Location and the Default Setting of the SW_GPIO_OPT_SEL

GPIO10 may be used for DISP_INT# or PMOD1. GPIO2 may be used for CAM0_RST# or DISP_INT#.

Table 2.8 DIP Switch “SW_GPIO_OPT_SEL” Setting (1/2)

SW_GPIO_OPT_SEL-1	GPIO10
1 – 2	Connected to DISP_INT#
2 – 3	Connected to PMOD1

Table 2.8 DIP Switch “SW_GPIO_OPT_SEL” Setting (2/2)

SW_GPIO_OPT_SEL-2	GPIO2
4 – 5	Connected to CAM_RST#
5 – 6	Connected to DISP_INT# *Note*: CAM_RST# is pulled high.

2.3.8 SW_GPIO_CAN_PMOD – CAN Standby

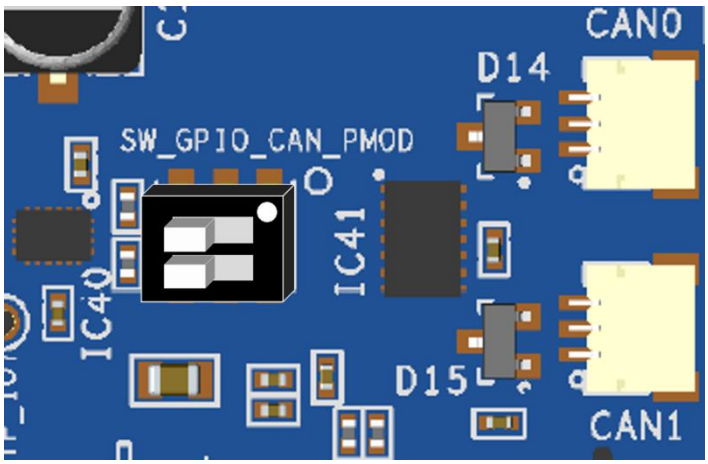

Figure 2.11 The Location and the Default Setting of the SW_GPIO_CAN_PMOD

GPIO8 and GPIO9 may be used for CAN standby or PMOD1 GPIO.

Table 2.9 DIP Switch “SW_GPIO_CAN_PMOD” Setting (1/2)

SW_GPIO_CAN_PMOD-1	GPIO8
1 – 2	Connected to CAN0_STB
2 – 3	Connected to PMOD1 *Note*: CAN0_STB is pulled low.

Table 2.9 DIP Switch “SW_GPIO_CAN_PMOD” Setting (2/2)

SW_GPIO_CAN_PMOD-2	GPIO9
4 – 5	Connected to CAN1_STB
5 – 6	Connected to PMOD1 *Note*: CAN1_STB is pulled low.

2.3.9 SW_MODE – Boot Mode (and Power)

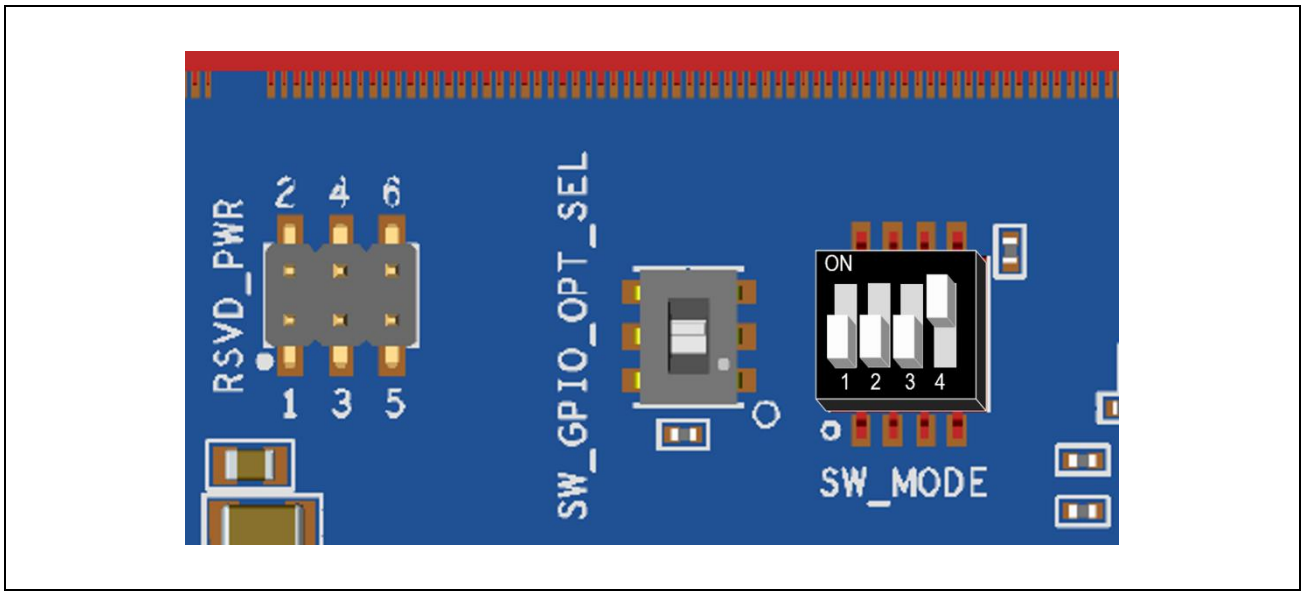

Figure 2.12 The Location and the Default Setting of SW_GPIO_OPT_SEL

As described in the SMARC specification, the Module boot mode can be configured as follows.

Table 2.10 DIP Switch “SW_MODE” Settings

Boot Mode #	SW_MODE[1] (BOOT_SEL0#)	SW_MODE[2] (BOOT_SEL1#)	SW_MODE[3] (BOOT_SEL2#)	Boot Source
0	ON	ON	ON	Carrier SATA *Note*: SATA signals are routed to the GEN_PURPOSE_IO connector.
1	OFF	ON	ON	Carrier SD card (SDIO)
2	ON	OFF	ON	Carrier eSPI (CS0#) *Note*: eSPI signals are routed to PMOD0 - Type-2A.
3	OFF	OFF	ON	Carrier SPI (CS0#) *Note*: SPI0 signals are routed to the GEN_PURPOSE_IO connector.
4	ON	ON	OFF	Module device (NAND, NOR) vendor specific E.g. Module uSD card
5	OFF	ON	OFF	Remote boot (GBE, serial) – vendor specific E.g. SCIF download using SER3_UART
6	ON	OFF	OFF	Module eMMC flash E.g. eMMC
7	OFF	OFF	OFF	Module SPI E.g. QSPI

SW_MODE[4] is not used for mode selection. It is used for selecting minimum current required from the USB-C power input. Refer to VBUS_SEL for details.

2.3.10 SW_M2_DIS – M.2 Card Control Signals

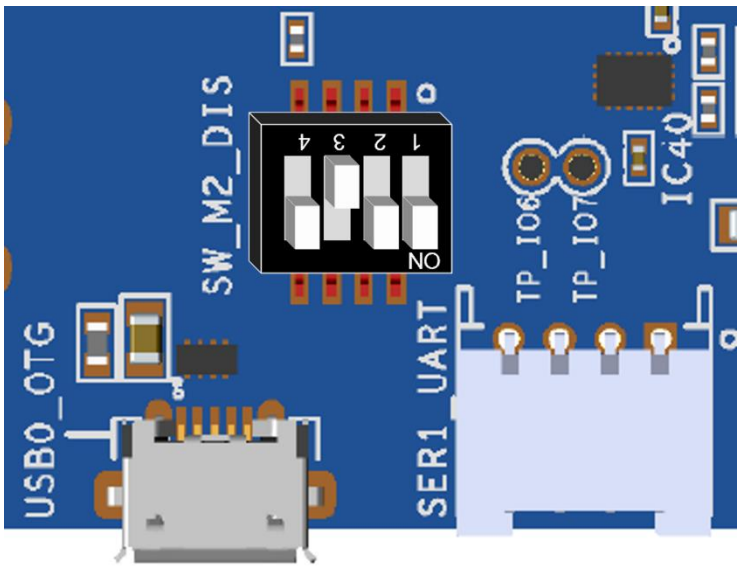

Figure 2.13 The Location and the Default Setting of the SW_M2_DIS

The M.2 cards may require control signals that are not in scope of the SMARC specification.

The RZ SMARC Carrier-II provides options for

- M.2 Key E: W_DISABLE1#, W_DISABLE2#
- M.2 key B: RESET#, FULL_CARD_POWER_OFF

These signals may be left open (usually pulled up on the M.2 card) or, for legacy modules, GPIO signals may be used, and for newer modules, these may be controlled using I2C_PM.

Table 2.11 DIP Switch “SW_OPT_MUX” Settings (1/4)

SW_M2_DIS[1]	SW_M2_DIS[4]	M.2 Key E: W_DISABLE1#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 7 (toggle)
ON	OFF	Inverted GPIO12
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.11 DIP Switch “SW_OPT_MUX” Settings (2/4)

SW_M2_DIS[2]	SW_M2_DIS[4]	M.2 Key E: W_DISABLE2#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 6 (toggle)
ON	OFF	Inverted GPIO13
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.11 DIP Switch “SW_OPT_MUX” Settings (3/4)

SW_M2_DIS[3]	SW_M2_DIS[4]	M.2 Key B: RESET#
ON	ON	Controlled by I2C_PM Byte 0x7A bit 5 (toggle)
ON	OFF	Inverted GPIO8
OFF	X	Open. Pull-up is expected on the M.2 card.

Table 2.11 DIP Switch “SW_OPT_MUX” Settings (4/4)

SW_M2_DIS[4]	M.2 Key B: FULL_CARD_POWER_OFF
ON	Controlled by I2C_PM Byte 0x7A bit 4 (toggle)
OFF	Inverted GPIO9

2.3.11 SW_OPT_MUX

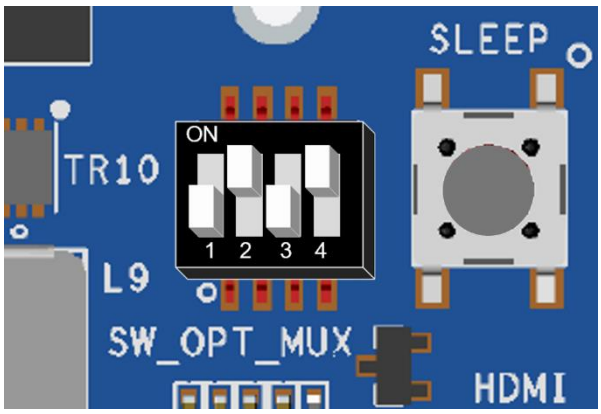

Figure 2.14 The Location and the Default Setting of the SW_OPT_MUX

To support legacy modules and provide greater flexibility, the RZ SMARC Carrier II provides multiplexing options for SDIO, I2S and SER0.

Table 2.12 DIP Switch “SW_PCIE_MUX” Settings (1/4)

SW_OPT_MUX[1]	SDIO
ON	The SMARC SDIO signals are routed to the M.2 Key E interface. *Note*: The uSD interface on the Carrier cannot be used.
OFF	The SMARC SDIO signals are routed to the uSD on the Carrier. *Note*: The M.2 Key E interface cannot use SDIO.

Table 2.12 DIP Switch “SW_PCIE_MUX” Settings (2/4)

SW_OPT_MUX[2]	I2S
ON	The SMARC I2S signals are routed to the M.2 Key E interface. *Note*: External display interface DISP0 has no I2S connection
OFF	The SMARC I2S signals are routed to the external display interface DISP0. *Note*: The M.2 Key E interface has no I2S connection.

Table 2.12 DIP Switch “SW_PCIE_MUX” Settings (3/4)

SW_OPT_MUX[3]	SPARE
X	No function

Table 2.12 DIP Switch “SW_PCIE_MUX” Settings (4/4)

SW_OPT_MUX[4]	SER0
ON	The SMARC SER0 signals are routed to PMOD1. *Note*: M.2 Key E has no UART connection.
OFF	The SMARC SER0 signals are routed to M.2 Key E UART. *Note*: PMOD1 has no UART connection.

2.3.12 SW_PCIE_MUX

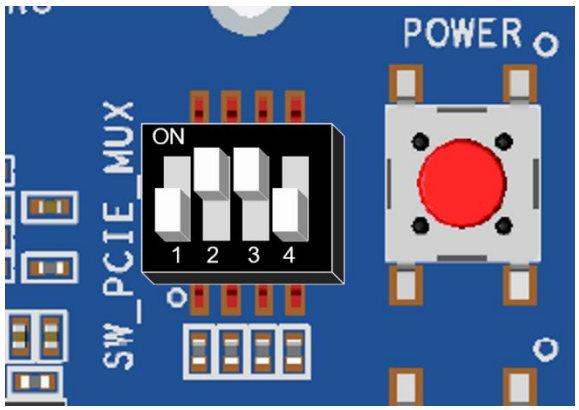

Figure 2.15 The Location and the Default Setting of the SW_PCIE_MUX

The RZ SMARC Carrier II supports SMARC Modules with the following PCIe configurations.

- 1x Channel, 1-Lane
- 2x Channel, 1-Lane
- 1x Channel, 2-Lane
- 2x Channel, 2-Lane
- 1x Channel, 4-Lane

The PCIe signals are multiplexed on the RZ SMARC Carrier II so that they can be connected to a combination of PCIE Slot, M.2 Key E and M.2 Key B interfaces.

The SMARC PCIe links are designated PCIE_A, PCIE_B, PCIE_C and PCIE_D.

Table 2.13 DIP Switch “SW_PCIE_MUX” Settings (1/4)

SW_PCIE_MUX[1]	PCIE MUX1 Refer to **Table 2.14, Usable PCIe Configurations** for details
ON	High
OFF	Low

Table 2.13 DIP Switch “SW_PCIE_MUX” Settings (2/4)

SW_PCIE_MUX[2]	PCIE MUX2 Refer to **Table 2.14, Usable PCIe Configurations** for details
ON	High
OFF	Low

Table 2.13 DIP Switch “SW_PCIE_MUX” Settings (3/4)

SW_PCIE_MUX[3]	PCIE MUX3 Refer to **Table 2.14, Usable PCIe Configurations** for details
ON	High
OFF	Low

Table 2.13 DIP Switch “SW_PCIE_MUX” Settings (4/4)

SW_PCIE_MUX[4]	USB2/M.2 Key B
ON	The SMARC USB2 signals are routed to the M.2 Key B interface. *Note*: The USB3.2 Type-A interface on the Carrier cannot be used.
OFF	The SMARC USB2 signals are routed to the USB3.2 Type-A interface. *Note*: The M.2 Key B interface on the Carrier cannot be used.

In case of the RZ/G3S, this processor supports 1lane for PCIe Interface. Only hatched "SW_PCIE_MUX" DIP switch settings are supported on the G3S SMARC EVK.

Table 2.14 Usable PCIe Configurations

					SW_PCIE_MUX			PCIe Slot					M.2 Key E				M.2 Key B		
Link Configuration	A	B	C	D	0	1	2	REFCK	Lane0	Lane1	Lane2	Lane3	REFCK0	Lane0	REFCK1	Lane1	REFCK	Lane0	Lane1
1x PCIe 1-lane	1x				1	0	0	A	A											
					0	1	1						A	A					
					1	0	1									A	A		
2x PCIe 1-lane	1x	1x			0	1	0	A	A				B	B					
					0	0	1	A	A								B	B	
					0	1	1	B					A	A	B	B			
					1	1	1						A	A			B	B	
1x PCIe 2-lane	2x				1	0	0	A	A	B										
					0	1	1						A	A		B			
					1	0	1										A	A	B
2x PCIe 2-lane	2x		2x		0	1	1	B	C	D			A	A	B	B			
					1	0	1	B	C	D							A	A	B
1x PCIe 4-lane	4x				1	0	0	A	A	B	C	D							
					0	1	1						A	A		B			
					1	0	1										A	A	B

2.4 User IO

2.4.1 Push Buttons

2.4.1.1 POWER, RESET, SLEEP

These push buttons are used to connect SMARC Module signals to ground. The SMARC Module inputs are open-drain.

The operation of each push button is dependent on the connected module.

Table 2.15 Features of Each Push Button

Label	Color	SMARC Signal	Description
POWER	Red	POWER_BTN#	Power-button output to the SMARC Module
RESET	Blue	RESET_IN#	Reset output to the SMARC Module
SLEEP	Grey	SLEEP#	Sleep indicator to the SMARC Module

2.4.1.2 USER_SW1, USER_SW2, USER_SW3

These push buttons are used to connect SMARC Module GPIO signals to ground. Care must be taken to avoid signal conflicts if other peripherals are using the same GPIO signals.

Table 2.16 Features of Each Push Button

Label	Color	SMARC Signal
USER_SW1	Grey	GPIO4
USER_SW1	Blue	GPIO6
USER_SW2	Blue	GPIO7

2.4.2 LED Indicators

2.4.2.1 Power

Four LED indicators are used to provide the user with power status.

Table 2.17 Features of Each Indicator for Power Status

Label	Color	Status (when lit)
VBUS_FAULT	RED	The connected USB-C power supply is not capable of providing the minimum current and/or minimum voltage as set by VBUS_SEL and SW_MODE[4].
VBUS_ON	GREEN	USB-C power supply is ON
SOM_ON	GREEN	SMARC Module (5 V) power is ON
CARRIER_ON	GREEN	Carrier power is ON
BAT_LOW	RED	VDD_RTC is below 2.0 V. Coin cell battery voltage is low or VBAT_SEL jumper is not fitted correctly.

2.4.2.2 PCI Express

Table 2.18 Feature of Indicator for PCI Express

Label	Color	Status (when lit)
PCIE_CK_LOSS	RED	PCIE_A_REFCK is not stable

2.4.2.3 M.2

Table 2.19 Features of Each Indicator for M.2

Label	Color	Status (when lit)
M.2E_LED1	RED	Refer to datasheet of connected M.2 Key E card
M.2E_LED2	RED	Refer to datasheet of connected M.2 Key E card
M.B_LED1	RED	Refer to datasheet of connected M.2 Key B card

2.4.2.4 Ethernet

The stacked Ethernet ports have integrated LEDs.

Table 2.20 Features of Each Indicator for Ethernet

Label	Color	Status (when lit)
ETHERNET1-0	GREEN	Link is up
ETHERNET1-0	YELLOW	Activity

2.5 Recommended Operating Condition

Table 2.21 lists operating conditions of the RZ SMARC Carrier II.

Table 2.21 Operating Conditions of RZ SMARC Carrier II

Symbol	Item	Rated Value	Note
USBC_PWR_IN	Power voltage	15 V	Reference: VSS
—	Maximum consumed current	4 A	Includes continuous G3S SMARC Module current consumption
Topr	Operating ambient temperature*1	0°C to 40°C	Do not expose to condensation or corrosive gases

Note 1. The ambient temperature is the air temperature at a point as close to the board as possible.

3. Functional Specifications

This section provides details of the RZ SMARC Carrier II interfaces.

3.1 Power

Figure 3.1 shows a block diagram of power system of the G3S SMARC EVK.

This board has one USB Type-C receptacle for power input with USB Power Delivery. The input voltage of VBUS can be selected among 5 V, 9 V, 15 V, and 20 V.

The 5 V power supply is supplied to the PMIC (RAA215300A2GNP#HA3) installed in the G3S SMARC Module, and the PMIC generates the power supply voltage for each interface.

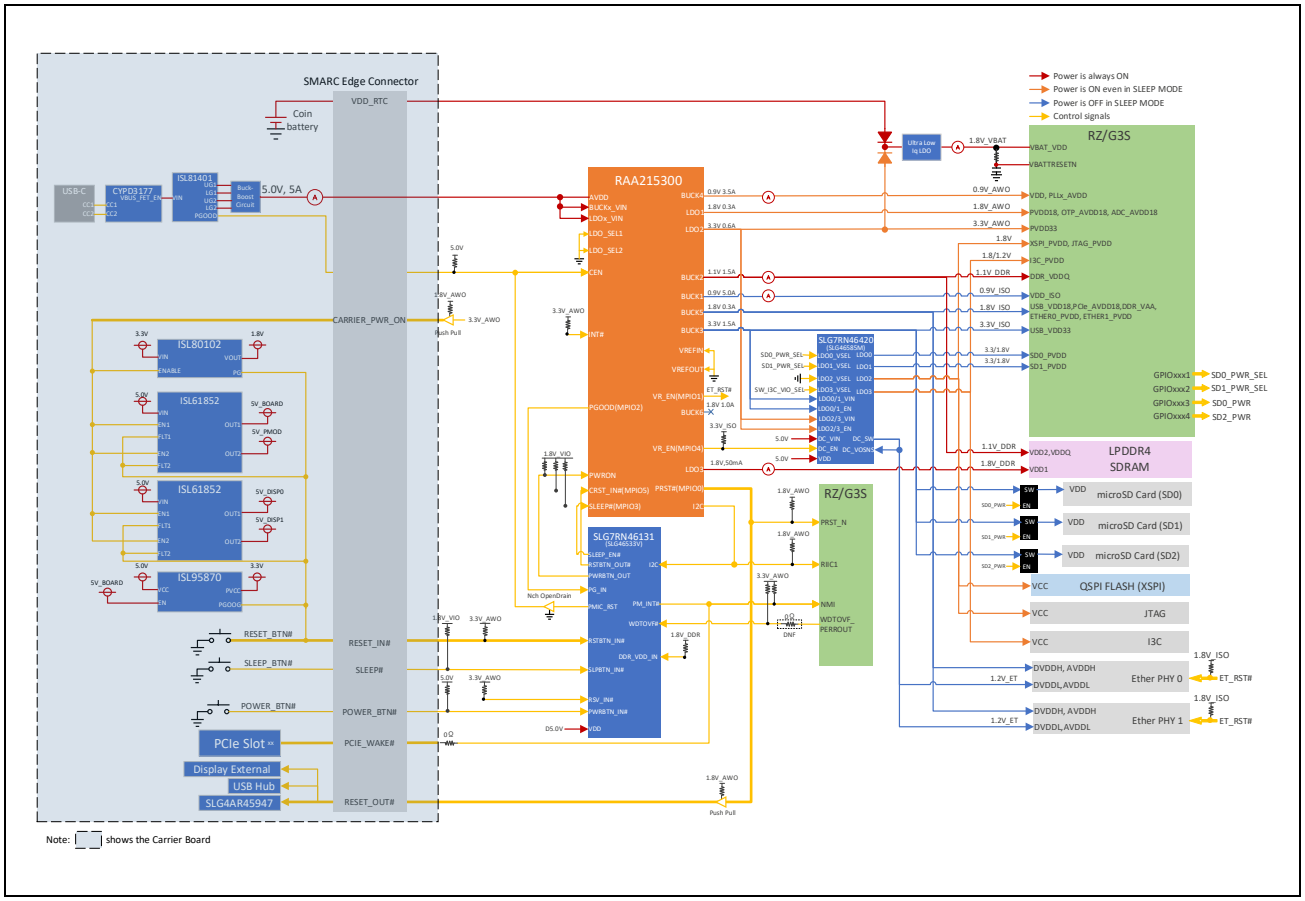

Figure 3.1 Power System Circuitry of G3S SMARC EVK

3.1.1 USB-C – Main Power

The RZ SMARC Carrier- II primary power input is from the USB -Type-C connected to a power delivery device (not provided).

3.1.2 BAT_RTC – VDD_RTC Power

A 3.0V coin cell battery may be fitted to provide VDD_RTC power as an alternative to the on-board regulator.

The advantage of using a coin cell is that power is maintained when USB-C main power is removed.

Compatible battery sizes are CR927and CR1025.

3.1.3 PWR 12V EXT – PCIe Slot Power

To support PCIe cards that are greater than 10W, an external 12V supply is required.

The interface on the RZ SMARC Carrier II for this is from Wurth Electronik, part number 691305140002.

The mating part, to which power cables can be attached, is provided (Wurth Electronik, part number 691361100002) – picture below. Ensure correct polarity.

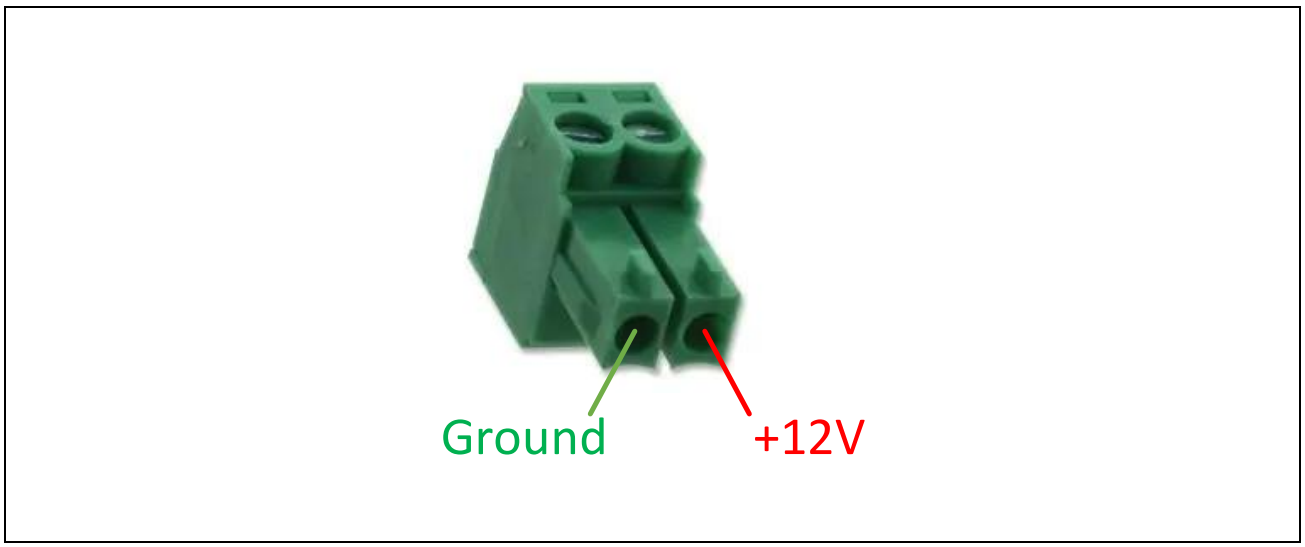

Figure 3.2 PWR_12V_EXT

3.2 Clock

Clock inputs required for peripherals such as FT232HQ, USB Hub, M.2 Key E Card Module, HDMI Transmitter are generated locally using separate crystals or oscillators. The crystals or oscillators used to provide the reference clocks for the G3S SMARC EVK peripherals are shown in the table below.

Table 3.1 Clock Table

Peripheral	Device Part Number	Frequency
FT232HQ Bridge *1	FL2400022	24.000 MHz
USB Hub	FL2400022	24.000 MHz
M.2 Key E	7XZ-32.768KBE	32.768 kHz
HDMI Transmitter *2	SIT1602AI-23-18E-12.000000D	12.000 MHz

Note 1. G3S SMARC Module

Note 2. SMARC MIPI-DSI to HDMI Adaptor. However, the SMARC MIPI-DSI to HDMI adaptor is not bundled with the RZ/G3S SMARC EVK.

3.3 Serial UART

3.3.1 SER1_UART

A 4-pin connector (Seeed Technology, part number 110990037) provides connection to SER1.

Table 3.2 SER1 Pin Assignment

Pin Number	Signal
1	SER1_RX
2	SER1_TX
3	1.8 V
4	Ground

Note: TX and RX signals are at 1.8 V levels.

3.3.2 SER3_UART

Connection to SER3 is via a micro-USB interface. This is generally used for connection to the console/terminal.

3.4 USB

The RZ SMARC Carrier II provides interfaces for the following.

Table 3.3 Supported Interfaces of Each USB

SMARC IO	Connector Type	
USB0	USB2.0 micro USB OTG	
USB1	USB2.0 Stacked Type-A	Connected from a 4-channel USB hub IC
USB2	USB3.0 Type-A	
USB3	USB-C	
USB4	USB2.0 Stacked Type-A	
USB5	USB2.0 Stacked Type-A	

3.5 Ethernet

A stacked RJ45 connector provides 2 ports, each capable of Gbit speeds.

3.6 Camera

The SMARC specification defines two MIPI CSI serial camera interfaces. The defined CSI0 interface supports up to two differential data lanes (CSI0_D[0:1]+/- signals). CSI1 may be implemented with up to four differential data lanes (CSI1_D[0:3]+/- signals) to support higher resolution cameras.

Both camera interfaces use a 22 pin FPC connector (TYCOELECTRONICS part number 2-1734592-2) following the SMARC specification pinout.

Table 3.4 CSI0 and CSI1 Pin Assignment

Pin Number	CAM_CS0	CAM_CS1
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	Ground	Ground
4	CSI0_RX0+	CSI1_RX0+
5	CSI0_RX0-	CSI1_RX0-
6	Ground	Ground
7	CSI0_RX1+	CSI1_RX1+
8	CSI0_RX1-	CSI1_RX1-
9	Ground	Ground
10	Not connected	CSI1_RX2+
11	Not connected	CSI1_RX2-
12	CAM0_RST#/GPIO2 (refer to SW_GPIO_OPT_SEL)	CAM1_RST#/GPIO3
13	Not connected	CSI1_RX3+
14	Not connected	CSI1_RX3-
15	Ground	Ground
16	CSI0_CK+	CSI1_CK+
17	CSI0_CK-	CSI1_CK-
18	Ground	Ground
19	I2C_CAM0_CK	I2C_CAM1_CK
20	I2C_CAM0_DAT	I2C_CAM1_DAT
21	CAM0_PWR#/GPIO0	CAM1_PWR#/GPIO1
22	CAM_MCK	CAM_MCK

3.7 PMOD

The RZ SMARC Carrier II provides 3 PMOD interfaces, although there is some signal overlap, so care must be taken if both PMOD1 types are required simultaneously.

SER0 and some GPIOs are multiplexed, so refer to the relevant configuration settings to ensure the signals are available.

Table 3.5 PMOD Pin Assignment

Pin Number	PMOD0_2A (SPI)	PMOD1_3A (UART)	PMOD1_6A (I2C)
1	SPI1_CS0#	SER0_CTS# *1	GPIO10 (INT)
2	SPI1_DO	SER0_TX *1	GPIO11 (RESET)
3	SPI1_DIN	SER0_RX *1	I2C_GP_CK
4	SPI1_CK	SER0_RTS# *1	I2C_GP_DAT
5	Ground	Ground	Ground
6	PWR_PMOD0	PWR_PMOD1	PWR_PMOD1
7	GPIO4 (INT)	GPIO10 (INT)	GPIO8 *2 (refer to SW_GPIO_CAN_PMOD)
8	GPIO5 (RESET)	GPIO11 (RESET)	GPIO9 *2 (refer to SW_GPIO_CAN_PMOD)
9	GPIO6 / POWR_BTN# (refer to SW_PMOD0_PWR_SLP)	GPIO12 *2	GPIO12 *2
10	GPIO7 / SLEEP# (refer to SW_PMOD0_PWR_SLP)	GPIO13 *2	GPIO13 *2
11	Ground	Ground	Ground
12	PWR_PMOD0	PWR_PMOD1	PWR_PMOD1

Note 1. Refer to SW_OPT_MUX[4]

Note 2. Refer to SW_M2_DIS[4]

3.8 Audio

The mono SPEAKER connection is provided by a 2-pin header, 2.54mm pitch.

All other audio connections are made using stereo connections to the 3.5mm colored jack sockets. Signal lines support stereo.

Table 3.6 Functions of Each Jack

Color	Function	Direction
Blue	Auxiliary	In
Lime	Headphone	Out
Pink	Microphone	In

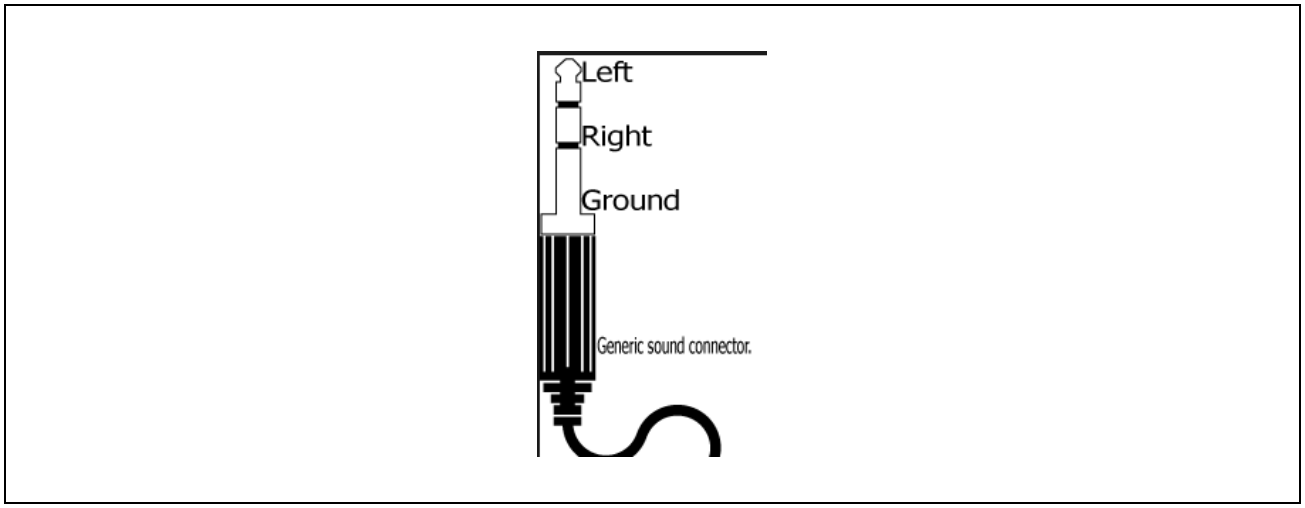

Figure 3.3 Stereo Jack

3.9 CAN

The RZ SMARC Carrier II provides 2 CAN channels, each connected through a 3-pin connector (JST, part number SM03B_SRRS-TB).

Table 3.7 CAN0 and CAN1 Pin Assignment

Pin Number	CAN0	CAN1
1	CAN0_H	CAN1_H
2	CAN0_L	CAN1_L
3	Ground	Ground
Transceiver STANDBY	GPIO8 *1	GPIO9 *1

Note 1. The on-board CAN transceiver has Standby functions that may be controlled using GPIO. Refer to SW_GPIO_CAN_PMOD for configuration.

3.10 uSD1 Card Interface

A uSD Card interface provides connection the SMARC SDIO signals, however, these signals are multiplexed. Refer to SW_OPT_MUX[1] for configuration.

3.11 M.2

Both Key E and Key B interfaces are provided for the RZ SMARC Carrier II.

3.11.1 M.2 Key E

A threaded spacer for Type-2230 is already inserted into the RZ SMARC Carrier II for mounting a plug-in M.2 Key E card. A M2.5x5mm machine screw is provided in the kit.

Table 3.8 Supported Interface for M.2 Key E

Communication Interface	SMARC Signal
USB2.0	USB1 via the 4-channel HUB
PCIe 2x Channels, 1-lane OR 1x Channel 2-lanes	PCIE_A, PCIE_B multiplexed
SDIO	SDIO multiplexed with the uSD card
I2S	I2S2 multiplexed with Display port 0
UART	SER0 (multiplexed with PMOD) or SER2
I2C	I2C_GP

Table 3.9 M.2 Key E Pin Assignment (1/2)

Pin	Signal	Signal	Pin
74	3.3 V	Ground	75
72	3.3 V	PCIE_M2E_REFCK1-	73
70	PCIE_WAKE#	PCIE_M2E_REFCK1+	71
68	PCIE_M2E_CKREQ1#	Ground	69
66	PCIE_M2E_RST1#	PCIE_M2E_RX1-	67
64	Not connected	PCIE_M2E_RX1+	65
62	Not connected	Ground	63
60	I2C_GP_CK	PCIE_M2E_TX1-	61
58	I2C_GP_DAT	PCIE_M2E_TX1+	59
56	M2E_W_DISABLE1#	Ground	57
54	M2E_W_DISABLE2#	PCIE_WAKE#	55
52	PCIE_M2E_RST0#	PCIE_M2E_CKREQ0#	53
50	M2E_SUSCLK (32.768 kHz)	Ground	51
48	Not connected	PCIE_M2E_REFCK0-	49
46	Not connected	PCIE_M2E_REFCK0+	47
44	Not connected	Ground	45
42	Not connected	PCIE_M2E_RX0-	43
40	Not connected	PCIE_M2E_RX0+	41
38	Not connected	Ground	39
36	SER0_RTS#/SER2_RTS#	PCIE_M2E_TX0-	37
34	SER0_CTS#/SER2_CTS#	PCIE_M2E_TX0+	35
32	SER0_TX/SER2_TX	Ground	33
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	
	CONNECTOR KEY E	CONNECTOR KEY E	

Table 3.9 M.2 Key E Pin Assignment (2/2)

Pin	Signal	Signal	Pin
22	SER0_RX/SER2_RX	SDIO_RESET#	23
20	TP_M2E_UART_WAKE#	TP_M2E_SDIO_WAKE#	21
18	Not connected	SDIO_D3	19
16	M2E_LED2 (Red)	SDIO_D2	17
14	I2S2_SDOUT	SDIO_D1	15
12	I2S2_SDIN	SDIO_D0	13
10	I2S2_LRCK	SDIO_CMD	11
8	I2S2_CK	SDIO_CK	9
6	M2E_LED1 (Red)	Ground	7
4	3.3 V	USB1_M2E-	5
2	3.3 V	USB1_M2E+	3
		Ground	1

3.11.2 M.2 Key B

A threaded spacer for Type-3052 is already inserted into the RZ SMARC Carrier II for mounting a plug-in M.2 Key B card. A M2.5x5mm machine screw is provided in the kit.

Type-xx42 or Type-xx30 plug-in M.2 Key B card can also be mounted using the threaded inserts and 2.5mm spacer provided.

Table 3.10 Supported Interface for M.2 Key B

Communication Interface	SMARC Signal
USB2.0	USB1 via the 4-channel HUB
PCIe 1x Channel, 1-lane or 2-lanes	PCIE_A, PCIE_B multiplexed
USB3.0	USB2 multiplexed with USB-C
SIM card	N/A

Table 3.11 M.2 Key B Pin Assignment (1/2)

Pin	Signal	Signal	Pin
74	3.3 V	M2B_CONFIG2	75
72	3.3 V	Ground	73
70	3.3 V	Ground	71
68	M2B_SUSCLK *1	M2B_CONFIG1	69
66	Not connected	M2B_RESET#	67
64	M2B_COEX_RXD *1	M2B_ANTCTL3 *1	65
62	M2B_COEX_TXD *1	M2B_ANTCTL2 *1	63
60	M2B_COEX3 *1	M2B_ANTCTL1 *1	61
58	M2B_RFFE_DATA *1	M2B_ANTCTL0 *1	59
56	M2B_RFFE_CLK *1	Ground	57
54	PCIE_WAKE#	PCIE_M2B_REFCK+	55
52	PCIE_M2B_CKREQ#	PCIE_M2B_REFCK-	53
50	PCIE_M2B_RST#	Ground	51
48	M2B_GPIO_4 *1	PCIE_M2B_TX0+	49

Table 3.11 M.2 Key B Pin Assignment (2/2)

Pin	Signal	Signal	Pin
46	M2B_GPIO_3 *1	PCIE_M2B_TX0-	47
44	M2B_GPIO_2 *1	Ground	45
42	M2B_GPIO_1 *1	PCIE_M2B_RX0+	43
40	M2B_GPIO_0 *1	PCIE_M2B_RX0-	41
38	M2B_DEVSLP *1	Ground	39
36	SIM_PWR	PCIE_M2B_TX1+/USB2_SSTX_M2B+	37
34	SIM_DATA	PCIE_M2B_TX1-/USB2_SSTX_M2B-	35
32	SIM_CLK	Ground	33
30	SIM_RESET	PCIE_M2B_RX1+/USB2_SSRX_M2B+	31
28	M2B_GPIO_8 *1	PCIE_M2B_RX1-/USB2_SSRX_M2B-	29
26	Pull-up 10k (W_DISABLE2#)	Ground	27
24	M2B_GPIO_7 *1	M2B_DPR *1	25
22	M2B_GPIO_6 *1	PCIE_WAKE#	23
20	M2B_GPIO_5 *1	M2B_CONFIG0	21
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
	CONNECTOR KEY B	CONNECTOR KEY B	
10	M2B_LED1#	Ground	11
8	Pull-up 10k (W_DISABLE1#)	USB1_M2B-	9
6	M2B_FULL_CARD_POWER_OFF#	USB1_M2B+	7
4	3.3 V	Ground	5
2	3.3 V	Ground	3
		M2B_CONFIG3	1

Note 1. Connected to the M2B_GPIO header.

3.12 Display

The RZ SMARC Carrier II provides a micro-HDMI port for direct connection to the SMARC HDMI display interface and two further interfaces (DISP0 and DISP1) for LVDS/MIPI-DSI channels 0 and 1.

By default, the RZ SMARC Carrier II is fitted with the SMARC MIPI-DSI to HDMI adaptor in DISP0.

NOTE

The SMARC MIPI-DSI to HDMI adaptor is not bundled with the RZ/G3S SMARC EVK.

3.12.1 HDMI

A Micro-HDMI is provided for direct connection the SMARC Module HDMI signals.

3.12.2 DISP0 and DISP1

Two mini-PCIe connectors (not to be used for mini-PCIe cards) are provided for interfacing to SMARC LVDS/DSI signals.

DISP0 only has I2S connection for audio and is fitted with the SMARC MIPI-DSI to HDMI adaptor by default. However, the SMARC MIPI-DSI to HDMI adaptor is not bundled with the RZ/G3S SMARC EVK.

Table 3.12 DISP0 Pin Assignment (1/2)

Pin Number	DISP0 Signal	DISP0 Signal	Pin Number
1	5V_DISPL0	3.3 V	2
3	5V_DISPL0	3.3 V	4
5	5V_DISPL0	3.3 V	6
7	5V_DISPL0	3.3 V	8
9	Not connected	1.8 V	10
11	Not connected	1.8 V	12
13	Not connected	1.8 V	14
15	Not connected	1.8 V	16
	KEY	KEY	
17	Ground	Ground	18
19	LVDS0_CK+/DSI0_CLK+	I2S2_DISP0_CK	20
21	LVDS0_CK-/DSI0_CLK-	I2S2_DISP0_LRCK	22
23	Ground	I2S2_DISP0_SDIN	24
25	LVDS0_0+/DSI0_D0+	I2S2_DISP0_SDOUT	26
27	LVDS0_0-/DSI0_D0-	I2C_LCD_CK	28
29	Ground	I2C_LCD_DAT	30
31	LVDS0_1+/DSI0_D1+	Ground	32
33	LVDS0_1-/DSI0_D1-	LCD0_BKLT_PWM	34
35	Ground	Ground	36
37	LVDS0_2+/DSI0_D2+	DSI0_TE	38
39	LVDS0_2-/DSI0_D2-	LCD0_VDD_EN	40

Table 3.12 DISP0 Pin Assignment (2/2)

Pin Number	DISP0 Signal	DISP0 Signal	Pin Number
41	Ground	LCD0_BKLT_EN	42
43	LVDS0_3+/DSI0_D3+	RESET_OUT#	44
45	LVDS0_3-/DSI0_D3-	DISP_INT#	46
47	Ground	Ground	48
49	Not connected	Not connected	50
51	Not connected	Not connected (DISP_ID)	52

Table 3.13 DISP1 Pin Assignment

Pin Number	DISP1 Signal	DISP1 Signal	Pin Number
1	5V_DISPL1	3.3 V	2
3	5V_DISPL1	3.3 V	4
5	5V_DISPL1	3.3 V	6
7	5V_DISPL1	3.3 V	8
9	Not connected	1.8 V	10
11	Not connected	1.8 V	12
13	Not connected	1.8 V	14
15	Not connected	1.8 V	16
	KEY	KEY	
17	Ground	Ground	18
19	LVDS1_CK+/DSI1_CLK+	Not connected	20
21	LVDS1_CK-/DSI1_CLK-	Not connected	22
23	Ground	Not connected	24
25	LVDS1_0+/DSI1_D0+	Not connected	26
27	LVDS1_0-/DSI1_D0-	I2C_LCD_CK	28
29	Ground	I2C_LCD_DAT	30
31	LVDS1_1+/DSI1_D1+	Ground	32
33	LVDS1_1-/DSI1_D1-	LCD1_BKLT_PWM	34
35	Ground	Ground	36
37	LVDS1_2+/DSI1_D2+	DSI1_TE	38
39	LVDS1_2-/DSI1_D2-	LCD1_VDD_EN	40
41	Ground	LCD1_BKLT_EN	42
43	LVDS1_3+/DSI1_D3+	RESET_OUT#	44
45	LVDS1_3-/DSI1_D3-	DISP_INT#	46
47	Ground	Ground	48
49	Not connected	Not connected	50
51	Not connected	Ground (DISP_ID)	52

3.13 I2C

There are six I2C interfaces connected to the SMARC Module.

Table 3.14 Supported Interface for I2C

I2C Bus	Signal Names
Power management	I2C_PM_CK, I2C_PM_DAT
General purpose	I2C_GP_CK, I2C_GP_DAT
Camera interface 0	I2C_CAM0_CK, I2C_CAM0_DAT
Camera interface 1	I2C_CAM1_CK, I2C_CAM1_DAT
LCD display ID	I2C_LCD_CK, I2C_LCD_DAT
HDMI interface	HDMI_CTRL_CK, HDMI_CTRL_DAT

3.13.1 I2C_PM

This I2C bus is designed to support power management and system configuration management.

Table 3.15 Address Mapping for I2C_PM

I2C_PM Device	7-bit Address
Renesas ISL28022FRZ (current monitor)	0x44
Renesas GreenPAK SLG4AR45947 (logic)	0x08
Renesas GreenPAK SLG4AE45948 (logic)	0x10
Renesas GreenPAK SLG4L45949 (PCIe mixing)	0x18
HD3SS3220RNH (USB-C port controller)	0x47

3.13.2 I2C_GP

This I2C bus is intended for general purpose use.

Table 3.16 Address Mapping for I2C_GP

I2C_GP Device	7-bit Address
Renesas DA7212-01UM (audio codec)	0x1A
PMOD1 – Type-6A	
M.2 Key E	
GEN_PURPOSE IO	

3.13.2.1 Current Monitoring

The SMARC Module current can be measured by using I2C_PM to read the Renesas ISL28022FRZ.

3.13.2.2 Board Configuration

Using the I2C_PM bus, it is possible to read back the board configuration from many of the switches and M2B_CONFIG.

Table 3.17 Board Configuration

Switch Configuration Read	Linux Command	Bit
SW_GPIO_PMOD	i2cget -y 1 0x8 0x74	2
SW_SER0_PMOD	i2cget -y 1 0x8 0x74	6
SW_SDIO_M2E	i2cget -y 1 0x10 0xF0	7
SW_I2S2_M2E	i2cget -y 1 0x10 0xF0	6
SW_SPARE	i2cget -y 1 0x10 0xF0	4
SW_USB2_M2B	i2cget -y 1 0x10 0xF0	3
M2B_CONFIG3	i2cget -y 1 0x10 0xF6	4
M2B_CONFIG2	i2cget -y 1 0x10 0xF6	3
M2B_CONFIG1	i2cget -y 1 0x10 0xF6	1
M2B_CONFIG0	i2cget -y 1 0x10 0xF6	0
SW_PCIE_MUX0	i2cget -y 1 0x18 0xF0	6
SW_PCIE_MUX1	i2cget -y 1 0x18 0xF0	4
SW_PCIE_MUX2	i2cget -y 1 0x18 0xF0	2
PCIE_SLOT_PRSNT#	i2cget -y 1 0x18 0xF0	1

3.13.2.3 M.2 Key E Controls

W_DISABLE1# and W_DISABLE2# control signals may be activated using the I2C_PM providing SW_M2_DIS[1], SW_M2_DIS[2] and SW_M2_DIS[4] are all ON.

After power on or reset, both W_DISABLE1# and W_DISABLE2# control signals are driven low. Setting the relevant bit to '1' and then to '0' toggles the state of the control signal.

Table 3.18 M.2 Key E Controls

M.2 Key E Control Signal	Linux Command	Bit
W_DISABLE1#	i2cset -y 1 0x08 0x7a	7
W_DISABLE2#	i2cset -y 1 0x08 0x7a	6

3.13.2.4 M.2 Key B Controls

M2B_RESET# control signal may be activated using the I2C_PM providing SW_M2_DIS[3] and SW_M2_DIS[4] are both ON.

M2B_FULL_CARD_POWER_OFF control signal may also be activated using the I2C_PM.

After power on or reset, both M2B_RESET# and M2B_FULL_CARD_POWER_OFF control signals are driven low. Setting the relevant bit to '1' and then to '0' toggles the state of the control signal.

Table 3.19 M.2 Key B Controls

M.2 Key B Control Signal	Linux Command	Bit
M2B_RESET#	i2cset -y 1 0x08 0x7a	5
M2B_FULL_CARD_POWER_OFF	i2cset -y 1 0x08 0x7a	4

3.13.3 I2C_CAM0, I2C_CAM1

This I2C bus is intended for camera support.

3.13.4 I2C_LCD

This I2C bus is intended for LCD display support and connects the SMARC Module directly to DISP0 and DISP1.

3.13.5 HDMI_CTRL

This I2C bus is intended for HDMI control and connects the SMARC Module to the micro-HDMI connector with level shifting and protection.

3.14 Miscellaneous

3.14.1 FAN

A 3-pin header is provided for connection to a standard fan IO.

Table 3.20 FAN Pin Assignment

Pin Number	CAN0
1	Not connected (Sense)
2	Power (12 V*1)
3	Ground

Note 1. If 5V is required, resistor fitting options are available.

3.14.2 GEN_PURPOSE I/O

A 24-pin, 0.27mm pitch header from Sullins, part number GRPB122VWQS-RC, provides access to general purpose IO.

NOTE

Take care connecting to some pins that are already used on the RZ SMARC Carrier II.

Table 3.21 GEN_PURPOSE I/O Pin Assignment

Pin Number	Signal	Signal	Pin Number
2	5.0 V	1.8 V	1
4	POWER_BTN#	BOOT_SEL0#	3
6	RESET_IN#	BOOT_SEL1#	5
8	SLEEP#	BOOT_SEL2#	7
10	5.0 V	Ground	9
12	Ground	SPI0_CS0#	11
14	SATA_TX+	SPI0_CK	13
16	SATA_TX-	SPI0_DIN	15
18	Ground	SPI0_DO	17
20	SATA_RX+	I2C_GP_CK	19
22	SATA_RX-	I2C_GP_DAT	21
24	Ground	Ground	23

3.14.3 M2B_GPIO

A 24-pin, 0.27mm pitch header from Sullins, part number GRPB122VWQS-RC, provides access to general purpose IO for M.2 Key B.

Table 3.22 M2B_GPIO Pin Assignment

Pin Number	Signal	Signal	Pin Number
2	M2B_REFE_CLK	1.8 V	1
4	M2B_REFE_DATA	M2B_DEVSLP	3
6	CLK_32K	M2B_SUSCLK	5
8	M2B_GPIO_8	M2B_GPIO_0	7
10	M2B_ANTCTL0	M2B_GPIO_1	9
12	M2B_ANTCTL1	M2B_GPIO_2	11
14	M2B_ANTCTL2	M2B_GPIO_3	13
16	M2B_ANTCTL3	M2B_GPIO_4	15
18	M2B_COEX_RXD	M2B_GPIO_5	17
20	M2B_COEX_TXD	M2B_GPIO_6	19
22	M2B_COEX3	M2B_GPIO_7	21
24	M2B_DPR	Ground	23

3.14.4 M2B SIM

A push-pull type, 1.27mm pitch connector from Molex, part number 78646-3001, provides access to SIM card for M.2 Key B.

Table 3.23 M2B_SIM Pin Assignment

Pin Number	Signal
1	SIM_PWR
2	SIM_RESET
3	SIM_CLK
5	Ground
6	SIM_PWR
7	SIM_DATA

3.15 SMARC Module Connector

The 314 pin, 0.5mm pitch, R/A memory socket style connector is used to interface the SMARC Module.

3.15.1 Display Interfaces

The RZ SMARC Carrier II provides two interfaces that may be used for LVDS, MIPI-DSI or eDP and a secondary HDMI.

These signals are routed to DISP0:

Table 3.24 DISP0 Signals

LVDS Signal Name	MIPI DSI Signal Name	eDP Signal Name	Pin #	RZ Port Pin	Signal
LVDS0_0+	DSI0_D0+	eDP0_TX0+	S125	N/A	
LVDS0_0-	DSI0_D0-	eDP0_TX0-	S126		
LVDS0_1+	DSI0_D1+	eDP0_TX1+	S128		
LVDS0_1-	DSI0_D1-	eDP0_TX1-	S129		
LVDS0_2+	DSI0_D2+	eDP0_TX2+	S131		
LVDS0_2-	DSI0_D2-	eDP0_TX2-	S132		
LVDS0_3+	DSI0_D3+	eDP0_TX3+	S137		
LVDS0_3-	DSI0_D3-	eDP0_TX3-	S138		
LVDS0_CK+	DSI0_CLK+	eDP0_AUX+	S134	N/A	
LVDS0_CK-	DSI0_CLK-	eDP0_AUX-	S135		
LCD0_VDD_EN	LCD0_VDD_EN	LCD0_VDD_EN	S133	N/A	
LCD0_BKLT_EN	LCD0_BKLT_EN	LCD0_BKLT_EN	S127	N/A	
LCD0_BKLT_PWM	LCD0_BKLT_PWM	LCD0_BKLT_PWM	S141	N/A	
—	DSI0_TE	eDP0_HPD	S144	N/A	
I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT	S140	N/A	
I2C_LCD_CK	I2C_LCD_CK	I2C_LCD_CK	S139	N/A	

These signals are routed to DISP1.

Table 3.25 DISP1 Signals

LVDS Signal Name	MIPI DSI Signal Name	eDP Signal Name	Pin #	RZ Port Pin	Signal
LVDS1_0+	DSI1_D0+	eDP1_TX0+	S111	N/A	
LVDS1_0-	DSI1_D0-	eDP1_TX0-	S112		
LVDS1_1+	DSI1_D1+	eDP1_TX1+	S114		
LVDS1_1-	DSI1_D1-	eDP1_TX1-	S115		
LVDS1_2+	DSI1_D2+	eDP1_TX2+	S117		
LVDS1_2-	DSI1_D2-	eDP1_TX2-	S118		
LVDS1_3+	DSI1_D3+	eDP1_TX3+	S120		
LVDS1_3-	DSI1_D3-	eDP1_TX3-	S121		
LVDS1_CK+	DSI1_CLK+	eDP1_AUX+	S108	N/A	
LVDS1_CK-	DSI1_CLK-	eDP1_AUX-	S109		
LCD1_VDD_EN	LCD1_VDD_EN	LCD1_VDD_EN	S116	N/A	
LCD1_BKLT_EN	LCD1_BKLT_EN	LCD1_BKLT_EN	S107	N/A	
LCD1_BKLT_PWM	LCD1_BKLT_PWM	LCD1_BKLT_PWM	S122	N/A	
—	DSI1_TE	eDP1_HPD	S113	N/A	
I2C_LCD_DAT	I2C_LCD_DAT	I2C_LCD_DAT	S140	N/A	
I2C_LCD_CK	I2C_LCD_CK	I2C_LCD_CK	S139	N/A	

These signals are routed to the HDMI connector.

Table 3.26 HDMI Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
HDMI_D2+ HDMI_D2- HDMI_D1+HDMI_D1- HDMI_D0+ HDMI_D0-	P92 P93 P95 P96 P98 P99	N/A	
HDMI_CK+ HDMI_CK-	P101 P102	N/A	
HDMI_CTRL_CK	P105	N/A	
HDMI_CTRL_DAT	P106	N/A	
HDMI_HPD	P104	N/A	

3.15.2 Camera Interfaces

The RZ SMARC Carrier II provides two interfaces that may be used for MIPI-CSI.

The CSI0 and CSI1 signals are not connected to the G3S SMARC Module.

Table 3.27 CAM0 and CAM1 Signals

SMARC Signal Name	Pin #	Description	RZ Port Pin	Signal
CSI0_RX0+ CSI0_RX0- CSI0_RX1+ CSI0_RX1-	S11 S12 S14 S15	CSI0 differential input	N/A	
CSI0_CK+ CSI0_CK-	S8 S9	CSI0 differential clock input (point to point)	N/A	
I2C_CAM0_DAT/CSI0_TX-	S7	I2C data for serial camera data support link or differential data lane	N/A	
I2C_CAM0_CK/CSI0_TX+	S5	I2C clock for serial camera data support link or differential data lane	N/A	
CAM0_PWR#	P108	Camera 0 Power Enable, active low output.	N/A	
CAM0_RST#	P110	Camera 0 reset, active low output	N/A	
CSI1_RX0+ CSI1_RX0- CSI1_RX1+ CSI1_RX1- CSI1_RX2+ CSI1_RX2- CSI1_RX3+ CSI1_RX3-	P7 P8 P10 P11 P13 P14 P16 P17	CSI1 differential input (point to point)	N/A	
CSI1_CK+ CSI1_CK-	P3 P4	CSI1 differential clock input (point to point)	N/A	
I2C_CAM1_DAT / CSI1_TX-	S2	I2C data for serial camera data support link or differential data lane	N/A	
I2C_CAM1_CK / CSI1_TX+	S1	I2C clock for serial camera data support link or differential data lane	N/A	
CAM1_PWR#	P109	Camera 1 Power Enable, active low output	N/A	
CAM1_RST#	P111	Camera 1 reset, active low output	N/A	
CAM_MCK	S6	Master clock output	N/A	

3.15.3 SDIO Card (4 bit) Interface

The SDIO signal is routed to the USB card slot.

Table 3.28 SDIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SDIO_D0	P39	SD1_DATA0	RZ_SD1_D0
SDIO_D1	P40	SD1_DATA1	RZ_SD1_D1
SDIO_D2	P41	SD1_DATA2	RZ_SD1_D2
SDIO_D3	P42	SD1_DATA3	RZ_SD1_D3
SDIO_WP	P33	—	Not connected
SDIO_CMD	P34	SD1_CMD	RZ_SD1_CMD
SDIO_CD#	P35	P0_2	RZ_SD1_CD#
SDIO_CK	P36	SD1_CLK	RZ_SD1_CLK
SDIO_PWR_EN	P37	P2_3	RZ_SDIO_PWR_EN

3.15.4 SPI Interfaces

The SPI1 signal is routed to the PMOD Type-2A connector.

The SPI0 signal is not connected to the G3S SMARC Module.

Table 3.29 SPI0 and SPI1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SPI0_CS0#	P43	N/A	
SPI0_CS1#	P31	N/A	
SPI0_CK	P44	N/A	
SPI0_DIN	P45	N/A	
SPI0_DO	P46	N/A	
SPI1_CS0#	P54	P15_3	RZ_RSPI0_SSL
SPI1_CS1#	P55	—	Not connected
SPI1_CK	P56	P15_0	RZ_RSPI0_CK
SPI1_DIN	P57	P15_2	RZ_RSPI_MISO
SPI1_DO	P58	P15_1	RZ_RSPI0_MOSI

3.15.5 Audio

These signals are routed to the Audio Codec and M.2 Key E.

Table 3.30 I2S0 and I2S2 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2S0_LRCK	S39	P18_3	RZ_SSI3_RCK
I2S0_SDOUT *1	S40	P18_4	RZ_SSI3_TXD
I2S0_SDIN *1	S41	P18_5	RZ_SSI3_RXD
I2S0_CK	S42	P18_2	RZ_SSI3_BCK
AUDIO_MCK	S38	N/A	AUDIO_MCK (clock generator)
I2S2_LRCK	S50	P11_1	RZ_SSI0_RCK
		—	Not connected
I2S2_SDOUT	S51	P11_2	RZ_SSI0_TXD
		—	Not connected
I2S2_SDIN	S52	P11_3	RZ_SSI0_RXD
		—	Not connected
I2S2_CK	S53	P11_0	RZ_SSI0_BCK
		—	Not connected

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.15.6 I2C Interfaces

The I2C_GP signals are routed to the GPIO pin header, M.2 Key E, Audio Codec and PMOD1 Type6A connecter.

The I2C_PM signals are routed to the ISL28022FRZ, SLG4L45949, SLG4R45950, SLG4AE45947 and SLG4AE45948.

The I2C_CAM0, I2C_CAM1, and I2C_LCD signals is not connected to the G3S SMARC Module.

Table 3.31 I2C_GP and I2C_PM Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
I2C_GP_CK	S48	RIIC0_SCL	RZ_RIIC0_SCL
I2C_GP_DAT	S49	RIIC0_SDA	RZ_RIIC0_SDA
I2C_PM_CK	P121	RIIC1_SCL	RZ_RIIC1_SCL
I2C_PM_DAT	P122	RIIC1_SDA	RZ_RIIC1_SDA

Note: RZ_RIIC1 bus is also used on the Module itself for:
- Power/Reset Control: SLG7RN46131
- PMIC: RAA215300A2GNP#HA3
- Power Regulator: SLG7RN46420
- Clock Generator: 5L35023B-615NLGI

3.15.7 Asynchronous Serial Ports

The RZ SMARC Carrier II provides four interfaces that may be used for asynchronous serial ports.

These signals are routed to the PMOD1 Type-3A connector, GROVE connector, M.2 Key E and DEBUG UART.

SER2 is not connected to the G3S SMARC Module.

Table 3.32 SER0, SER2, and SER3 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
SER0_TX	P129	P14_0	RZ_SCIF1_TXD
SER0_RX	P130	P14_1	RZ_SCIF1_RXD
		—	Not connected
SER0_RTS#	P131	P16_1	RZ_SCIF1_RTS#
SER0_CTS#	P132	P16_0	RZ_SCIF1_CTS#
SER1_TX	P134	P17_3	RZ_SCIF3_TXD
SER1_RX *1	P135	P17_2	RZ_SCIF3_RXD
SER2_TX	P136	N/A	
SER2_RX	P137	N/A	
SER2_RTS#	P138	N/A	
SER2_CTS#	P139	N/A	
SER3_TX	P140	P6_4	RZ_SCIF0_TXD
SER3_RX	P141	P6_3	RZ_SCIF0_RXD

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.15.8 CAN Bus

These signals are routed to the CAN connectors:

Table 3.33 CAN0 and CAN1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
CAN0_TX	P143	P6_1	RZ_CAN0_TX
CAN0_RX	P144	P6_2	RZ_CAN0_RX
CAN1_TX	P145	P17_0	RZ_CAN1_TX
CAN1_RX	P146	P17_1	RZ_CAN1_RX

3.15.9 USB Interfaces

These signals are routed to the USB Type micro-AB and USB hub IC.

The USB channels 2, 3, 4, and 5 signals are not connected to the G3S SMARC Module.

Table 3.34 USB0 and USB1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
USB0+	P60	USB0_DP	RZ_USB0_DP
USB0-	P61	USB0_DM	RZ_USB0_DM
USB0_EN_OC# *1	P62	P5_0	RZ_USB0_VBUSEN
		P5_2	RZ_USB0_OVRCUR#
USB0_VBUS_DET	P63	USB0_VBUSIN	RZ_USB0_VBUSIN
USB0_OTG_ID	P64	P5_3	RZ_USB0_OTG_ID
USB1+	P65	USB1_DP	RZ_USB1_DP
USB1-	P66	USB1_DM	RZ_USB1_DM
USB1_EN_OC# *1	P67	P6_0	RZ_USB1_VBUSEN
		P5_4	RZ_USB1_OVRCUR#

Note 1. Logic circuitry is used to provide independent enable and overcurrent IO.

3.15.10 PCI Express

The PCIE_A signal is routed to the PCIe slot, M.2 Key E and M.2 Key B.

The PCIE_B, PCIE_C, and PCIE_D signals are not connected to the G3S SMARC Module.

Table 3.35 PCIE_A Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
PCIE_A_TX+	P89	PCIE_TX_DP	PCIE_A_TX+
PCIE_A_TX-	P90	PCIE_TX_DM	PCIE_A_TX-
PCIE_A_RX+	P86	PCIE_RX_DP	PCIE_A_RX+
PCIE_A_RX-	P87	PCIE_RX_DM	PCIE_A_RX-
PCIE_A_REFCK+	P83	PCIE_REFCLKP0	RZ_PCIE_REFCLK+
PCIE_A_REFCK-	P84	PCIE_REFCLKN0	RZ_PCIE_REFCLK-
PCIE_A_RST#	P75	P13_2	PCIE_A_RST#
PCIE_A_CKREQ#	P78	P13_3	PCIE_A_CKREQ#

3.15.11 SATA

The RZG3S does not support SATA interfaces. None of the SATA signals are connected.

3.15.12 Ethernet

These signals are routed to the RJ45 connectors.

Table 3.36 GBE0 and GBE1 Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GBE0_MDI0+ GBE0_MDI0- GBE0_MDI1+ GBE0_MDI1- GBE0_MDI2+ GBE0_MDI2- GBE0_MDI3+ GBE0_MDI3-	P30 P29 P27 P26 P24 P23 P20 P19	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET0_xxx
GBE0_LINK100#	P21	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK1000#	P22	N/A	ET0_LED2 (ET0 PHY)
GBE0_LINK_ACT#	P25	N/A	ET0_LED1 (ET0 PHY)
GBE0_CTREF	P28	—	Not connected
GBE0_SDP	P6	—	Not connected
Ethernet PHY0 Interrupt *1	N/A	P12_0	ET0_INT# (RZ_IRQ0)
		—	Not connected
GBE1_MDI0+ GBE1_MDI0- GBE1_MDI1+ GBE1_MDI1- GBE1_MDI2+ GBE1_MDI2- GBE1_MDI3+ GBE1_MDI3-	S17 S18 S20 S21 S23 S24 S26 S27	—	These signals are provided by the Ethernet PHY controlled by the RZ RGMII signals ET1_xxx
GBE1_LINK100#	S19	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK1000#	S22	N/A	ET1_LED2 (ET1 PHY)
GBE1_LINK_ACT#	S31	N/A	ET1_LED1 (ET1 PHY)
GBE1_CTREF	S28	—	Not connected
GBE1_SDP	P5	—	Not connected
Ethernet PHY1 Interrupt *1	N/A	P12_1	ET1_INT# (RZ_IRQ1)
		—	Not connected

Note 1. SW_CONFIG[3] switch option on the G3S SMARC Module

3.15.13 GPIO

Table 3.37 GPIO Signals

SMARC Signal Name	Pin #	RZ Port Pin	Signal
GPIO0	P108	N/A	Not connected
GPIO1	P109	N/A	Not connected
GPIO2	P110	N/A	Not connected
GPIO3	P111	N/A	Not connected
GPIO4 *1	P112	P18_0	RZ_IRQ2_GPIO4
		TAMPIN	RZ_TAMPIN
GPIO5	P113	P13_4	RZ_P13_4_GPIO5
GPIO6	P114	P0_1	RZ_P0_1_GPIO6
GPIO7	P115	P0_3	RZ_P0_3_GPIO7
GPIO8	P116	P13_0	RZ_P13_0_GPIO8
GPIO9	P117	P13_1	RZ_P13_1_GPIO9
GPIO10	P118	P18_1	RZ_IRQ3_GPIO10
GPIO11	P119	P14_2	RZ_P14_2_GPIO11
GPIO12	S142	P8_2	RZ_P8_2_GPIO12
GPIO13	S123	P8_3	RZ_P8_3_GPIO13

Note 1. GPIO4_SEL switch option on the G3S SMARC Module

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