RTKA271005DE0000BU

Automotive Power Management IC Evaluation Board

Description

The RTKA271005DE0000BU evaluation board provides a quick and comprehensive method for evaluating the RAA271005. The RAA271005 is a versatile automotive power management IC (PMIC) that is designed for a range of applications, including vehicle computers, communication gateways, and domain servers. It integrates five high-efficiency DC/DC switching regulators and six LDO (low-dropout) regulators.

The RAA271005 is optimized for safety-critical automotive environments, supporting up to ASIL D functional safety. It includes various safety and monitoring features, such as dual internal temperature sensors, a 12-bit ADC to monitor voltages and temperatures, and a challenge-response watchdog timer. The device also includes programmable power sequencing and supports low-power modes like Suspend-to-RAM and DDR backup.

Additionally, it is designed to work seamlessly with R-Car SoCs, making it ideal for advanced driver-assistance systems (ADAS) and automotive infotainment systems. The PMIC is configurable using I²C and SPI interfaces, and it can be used in conjunction with external MCUs to monitor and manage power sequencing for various subsystems.

Features

- Five high-efficiency switching regulators (Buck) and six low-dropout (LDO) regulators for flexible power delivery.
- Programmable power sequencing to control the startup and shutdown of various power domains, suitable for complex SoCs (like Renesas' R-Car).
- Dual internal temperature sensors, voltage monitoring with a 12-bit ADC, and a challenge-response watchdog timer to ensure robust system operation.
- Supports low power modes such as Suspend-to-RAM (S2R) and DDR backup, allowing for efficient energy use in standby scenarios.
- Operates over a broad input voltage range (from 2.7V to 5.5V), suitable for automotive environments.
- Supports both I²C and SPI interfaces for configuration, monitoring, and control, allowing integration with external microcontrollers.
- Integrated overvoltage, undervoltage, overcurrent, and thermal protection mechanisms.
- Specifically designed for automotive applications like vehicle gateways, domain controllers, and infotainment systems, ensuring reliable operation under automotive condition

Specifications

This board is optimized for the following operating conditions:

- Supply Voltage (AVIN1/2 to GND) = 2.7V to 5.5V
- Supply Voltage (PVINx to GND) = 2.7V to 5.5V
- Supply Voltage (LDOIN1 to GND) = 2.7V to 5.5V
- Supply Voltage (LDOIN2 to GND) = 1.8V(LDO3 OFF) / 2.7V(LDO3 ON) to 5.5V
- Supply Voltage (LDOIN3 to GND) = 1.8V to 5.5V
- Supply Voltage (VIN_SENSE to GND) = 2.7V to 5.5V
- VIO Voltage = 1.7V to AVIN2
- Ambient Temperature = -40°C to +125°C
- Buck 1 Operating Current = 12A
- Buck[2-5] Operating Current = 2.5A
- LDO[1-4] Operating Current = 75mA
- LDO[5-6] Operating Current = 500mA

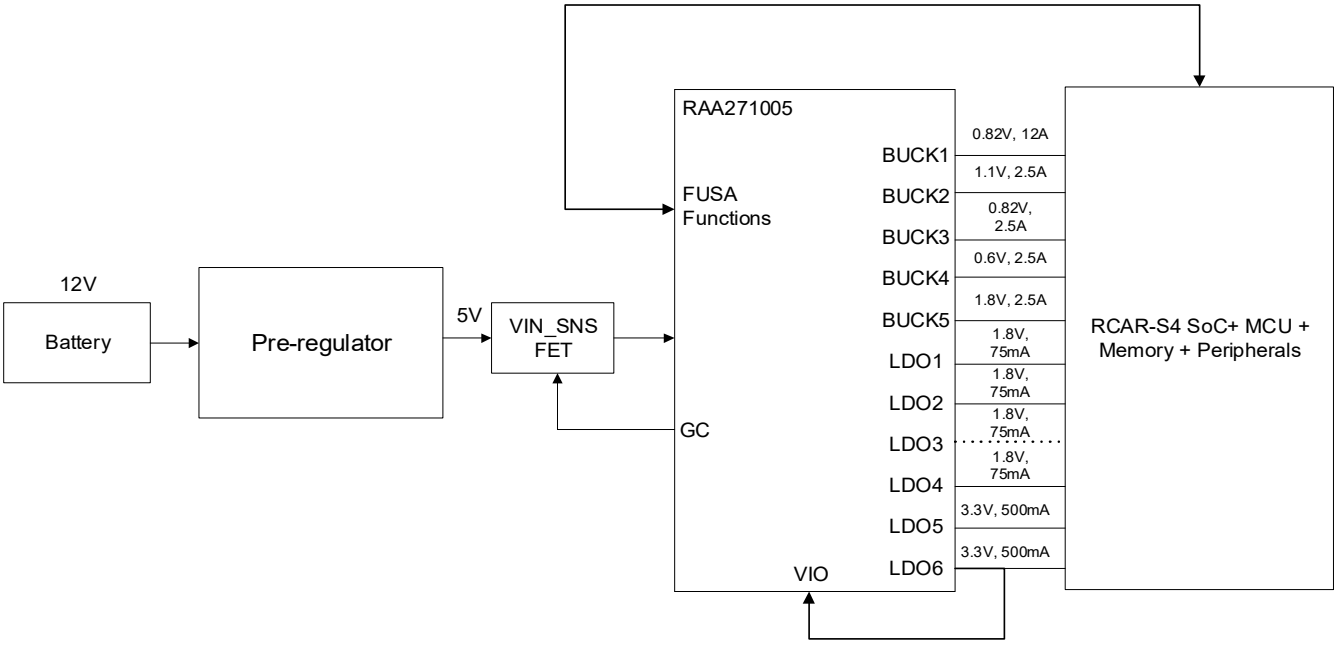

Figure 1. RAA271005 Block Diagram

Contents

1. Functional Description

The RTKA271005DE0000BU offers a comprehensive and flexible platform, enabling users to evaluate the PMIC's functionality and prototype their applications. The board allows users to test startup and shutdown sequences, apply different loads, and assess efficiency under varying temperatures. It also provides the capability to monitor I/Os, regulators, ADCs, and various signal functionalities, as well as observing the phase switching for each buck converter. Additionally, the evaluation board supports SoC activation testing with an MCU. Communication with the board can be facilitated through I^2C or SPI protocol.

1.1 Recommended Equipment

- Two 2.7V to 5.5V power supply with at least 2A source current capability
- Minimum 10-channel oscilloscope to verify all regulators, PRESET-IO8, INTb-IO14, and PGOOD_GLB signals
- Load such as DC motor, or electronic load (optional)

1.2 Quick Start Guide

Connect the following headers with a jumper:

- I^2C communication is used:
  - J26, J28
- SPI communication is used:
  - J25 (IO1 SCLK), J27 (IO2 NSS2), J29, J31, J33, J157 (IO9 NSS2), J159 (IO6 SCLK)
- I^2C ISLUSB dongle is used:
  - J60 3-pin header: J69 + middle pin
  - J61 3-pin header: J69 + middle pin
  - Connect dongle to J69 on the top-right of the board.
- SPI Cheetah Adapter is used:
  - J62 3-pin header: J68 + middle pin
  - J63 3-pin header: J68 + middle pin
  - J64 3-pin header: J68 + middle pin
  - J65 3-pin header: J68 + middle pin
  - J143 3-pin header: Use a female to female wire and connect J68 to J28 (left-side of the 2-pin header)
  - Connect adapter to J68 on the top-right of the board.
- VIO Input: J55 (3.3V) or J56 (1.8V)
- VIN is used as LDOIN:
  - VIN to LDOIN
  - J96, J100, J126
- IO17 to IO13:
  - MTE Mode and SoC Activation not enable: J151
  - SoC Activation enable: No jumper required
- If VIO is External:
  - 6V0 to 3V3 LDO: J66
  - 6V0 to 1V8 LDO: J67
- VIN_SENSE to VCC_6V: J144

After the jumpers are connected, follow these procedures based on SoC activation.

- For OTP in MTE mode and SoC activation not enable:

1. For V4M and V4H Target SoC, tie both of the PWRCTRL (IO17 and IO18) to GND. For all other Target SoC, tie both of the PWRCTRL (IO17 and IO18) to 3.3V or 5V.
2. If the EN does not come from an external MCU, connect one power supply to the EN pin. Turn on supply to 5V.
3. Connect the other power supply to VIN terminals. Turn on supply to 5V.
4. Verify all the regulators. The Preset and PGOOD_GLB signals are high. IO14 remains high or low (based on whether IO14 is set to invert). If invert is set to False, IO14 remains high when there is no fault, and if invert is set to True, IO14 remains low when there is no fault.

- For OTP with SoC activation enable:

1. If PWRCTRL1 (IO17) and PWRCTRL2 (IO18) is not controlled using software, (for V4M and V4H Target SoC) tie both of the PWRCTRL (IO17 and IO18) to GND and (for all other Target SoC) tie both of the PWRCTRL (IO17 and IO18) to 3.3V or 5V. If PWRCTRL1 (IO17) and PWRCTRL2 (IO18) is controlled using software, both of the PWRCTRL (IO17 and IO18) is not required to be tied to anything.
2. If the EN does not come from an external MCU, connect one power supply to the EN pin. Turn on supply to 5V.
3. Connect the other power supply to VIN terminals. Turn on supply to 5V.
4. Verify all the regulators. The Preset and PGOOD_GLB signals are high. IO14 remains high or low (based on whether IO14 is set to invert). If invert is set to False, IO14 remains high when there is no fault, and if invert is set to True, IO14 remains low when there is no fault.

2. Board Design

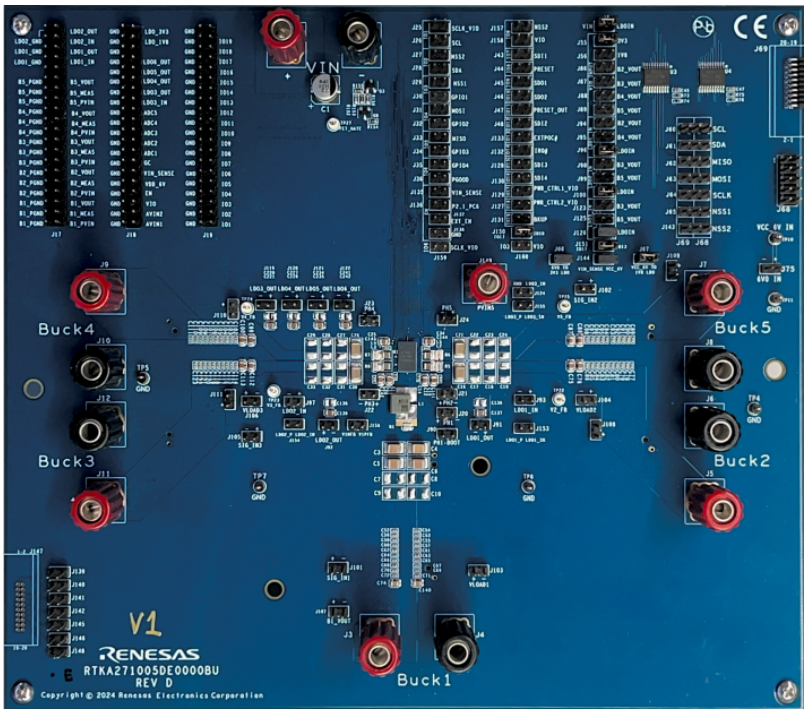

Figure 2. RTKA271005DE0000BU Evaluation Board (Top)

2.1 PCB Layout Guidelines

The following is for the layout of Buck[1-5].

1. Place the input capacitors as close as possible to the Buck PVIN and PGND pins with the least impedance routing.
2. Connect all PGND pins together through GND copper plane and use multiple vias connecting the inner and other GND layers.
3. Connect the Buck-1 PH1 pins together through a PH1 copper plane on the PMIC component layer.
4. Place inductors as close as possible to the PMIC.
5. Place the output bulk capacitor COUT1 close to the inductor L1 output terminal.
   a. Minimize the GND distance of the input capacitor CIN1 and the output capacitor COUT1. If CIN1 GND plane and CIN2 GND plane cannot be connected directly with copper, use enough vias connecting them to the inner or other GND plane respectively so that the two GND planes can be connected through the other GND layers with minimized resistance.
   b. Solid ground plane is helpful for a good EMI performance, current conduction, and thermal dissipation.
6. If possible, use two or multiple layer or wide enough PCB copper trace for the output voltage VOUT1 to minimize the conduction loss because Buck-1 output carries high current.

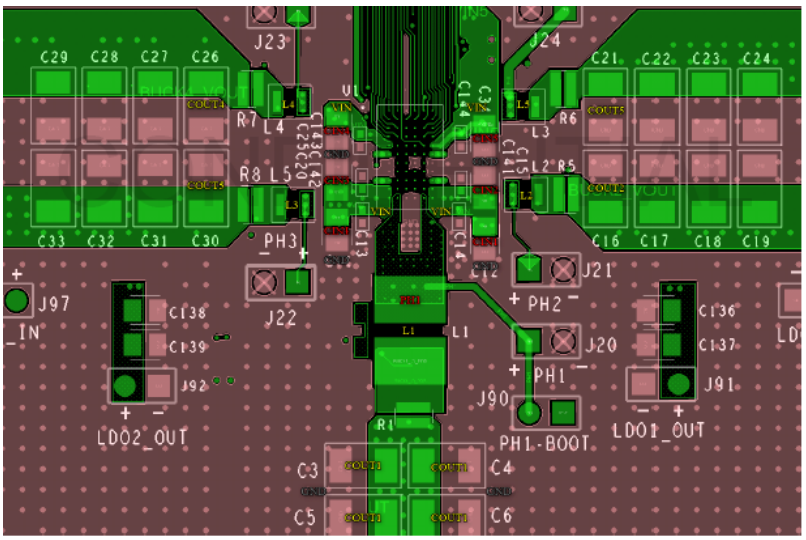

Figure 3. Top Layer

7. For the Buck-1 bootstrap cap CBOOT (recommended 47nF), place it on the PCB bottom component layer.
   a. Use a via connecting BOOT pin to the bottom layer and use a via connecting PH1 net to the bottom layer.
   b. Minimize the loop and the PCB trace of Boot pin → Boot trace → Cboot → PH1 trace.
   c. Use at least a 10 mil width trace for the Boot trace and PH1 trace to conduct the Buck-1 high-side FET driver current.
   d. Keep all other smaller signals away from BOOT and PH1 via/trace/copper.

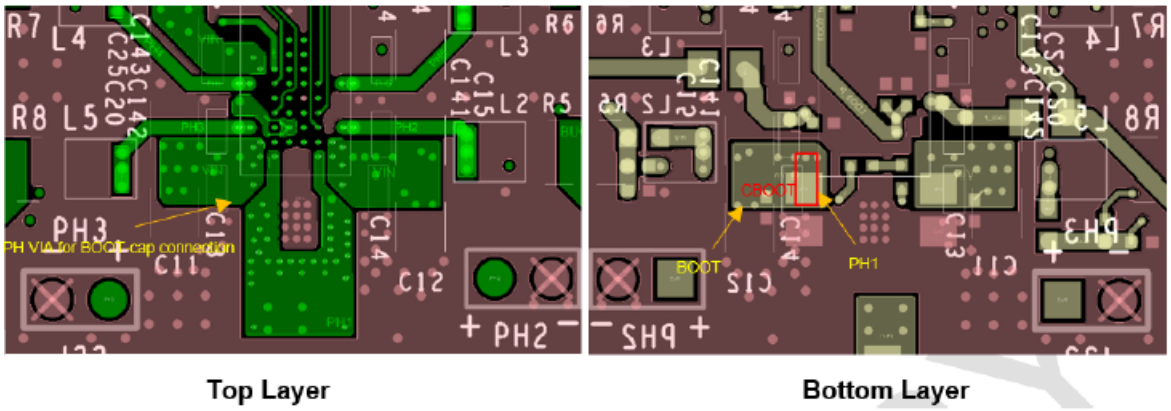

Figure 4. Top and Bottom Layer

8. Run the VOUT1 and RTN1 output voltage feedback differential trace in parallel, staying away from the PH1, PH2, PH3, PH4, PH5, and BOOT nets noisy signal via/trace/copper, and away from any high-speed digital signals. Shield the VOUT1 and RTN1 differential parallel traces with GND copper.

   Important: Limit the impedance for the VOUT1 and RTN1 traces to less than 100mΩ. This is because the discharge resistor and discharge detect circuit inside the PMIC staying within the electrical specifications for these functions.

9. Connect the VOUT1 and RTN1 differential sensing point to the VOUT1 output high-frequency ceramic cap bank to minimize the feedback ripple and noise.

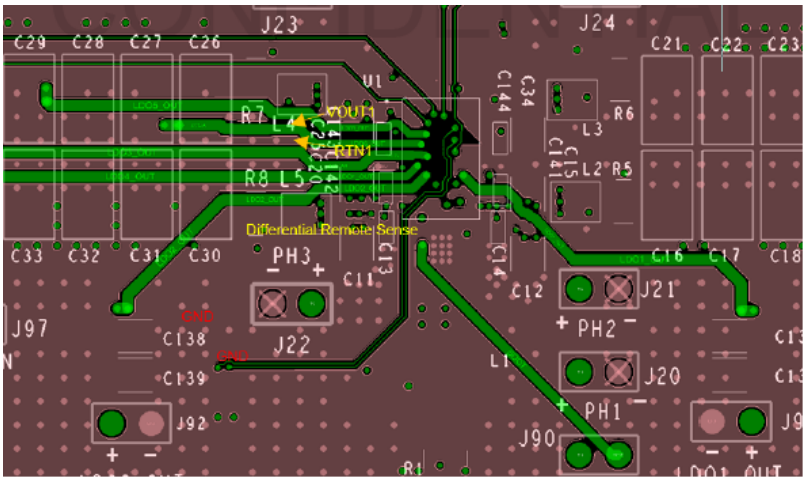

Figure 5. Differential Remote Sense

10. Use the inner layer or bottom layer to run the PH traces, connect to the PH pin and inductor pad through multiple vias.
    a. The PH trace should be wide enough to carry the output current.
    b. Avoid any sensitive signal close to the PH trace and via.

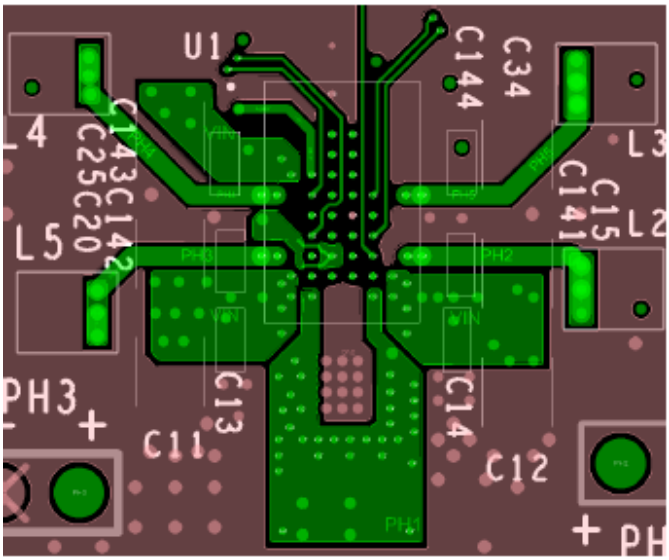

Figure 6. PH Trace

2.1.1 Placement of All Other Components and PCB Routing

1. Place the LDOIN1, LDOIN2, and LDOIN3 input capacitors as close as possible to the pins.
2. Place the LDO1-6 output capacitors as close as possible to the LDO1-6 output pins, respectively.
3. Place the AVIN1 pin and AVIN2 pin R-C filter capacitor as close as possible to the AVIN1 and AVIN2 pins, respectively. Always reference the decoupling capacitor GND pad to a quiet GND plane.
4. Run the ADCs and GPIOs digital traces away from the PH1/2/3/4/5 and BOOT noisy signal via/trace/copper.

2.1.2 PCB Thermal Considerations

The indicated thermal impedances θ_{JA} and θ_{JC} are determined using JEDEC standard testing as noted in the Thermal Information section in the *RAA271005 Datasheet*, but additional improvements can be made using either or both of the listed recommendations. *Note:* Consider these recommendations if the RAA271005 is being used to supply a large amount of power from its combined outputs and the junction temperature of the device is too high:

- Providing more PCB copper (larger shapes and/or adding layers) to dissipate more heat from the bottom of the device.
- Provide airflow over the top of the device and/or add a heatsink attached to the top of the package. The thermal resistance of the package molding material is sufficient enough to allow a heatsink to be used this manner.

2.2 Schematic Diagrams

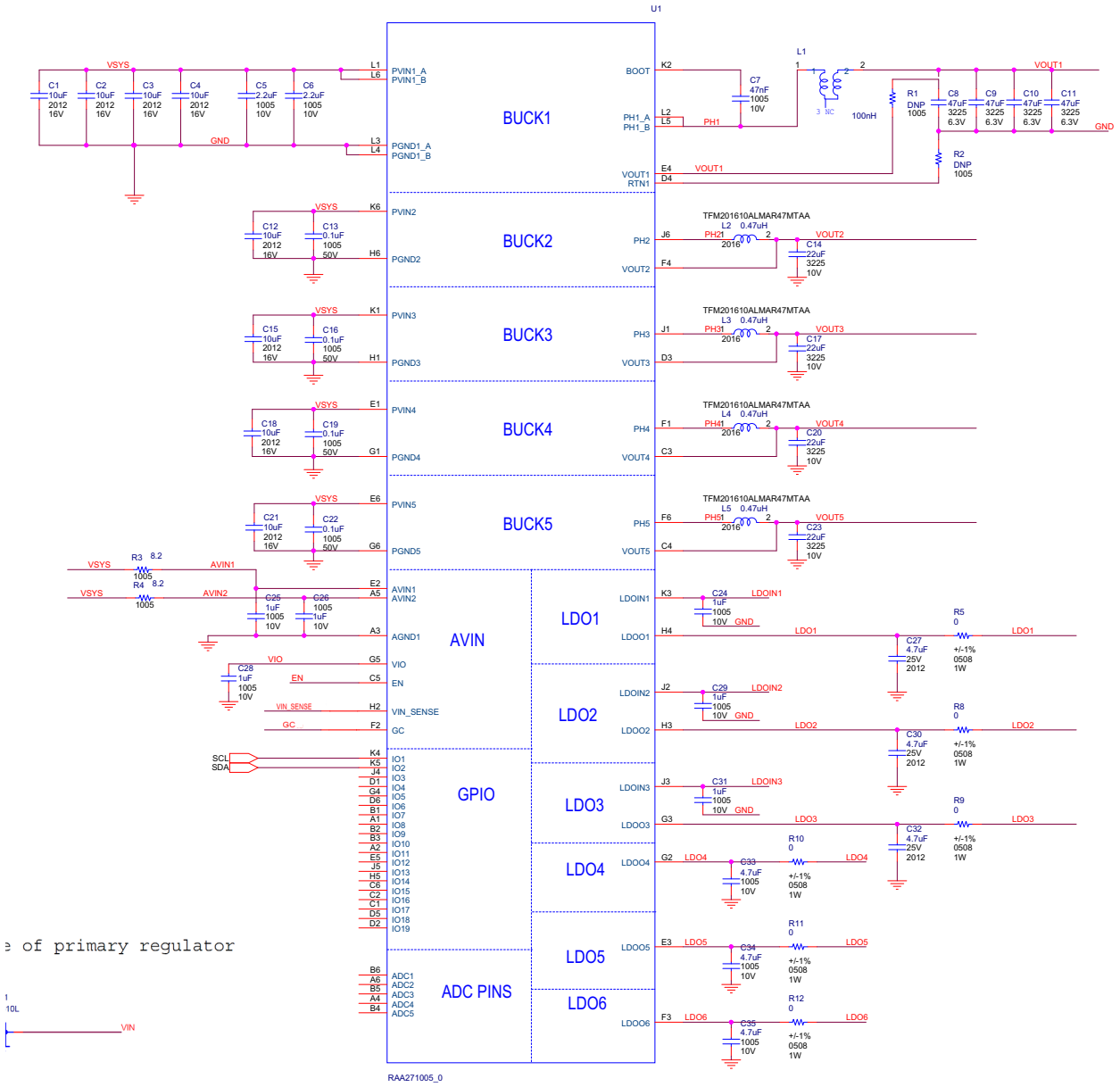

Figure 7. Schematic (1 of 2)

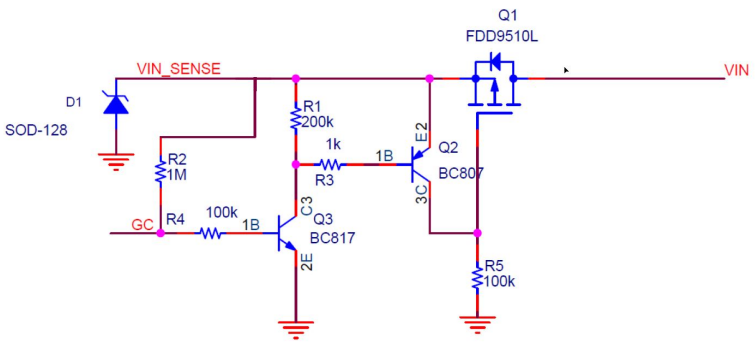

Figure 8. Schematic (2 of 2)

2.3 Bill of Materials

Based on the operating option, the buck regulators can be used with a different minimum amount of output capacitance to maintain their load transient specifications. Table 1 shows the recommended BOM to achieve the best transient performance on each rail.

Table 1. Recommended BOM

Quantity	Regulator	Component	Value	Manufacturer	Manufacturer Part Number
4	Buck1	CIN	10µF	Murata	GCM21BC71C106KE36
2			2.2µF	Murata	GRT155C71A225KE13D
2			0.1µF	Murata	GCM155R71H104KE02D
1		L	0.1µH	TDK	HPL505028FR10MRD3P
4		COUT	47µF	Murata	GCM32ER70J476KE19
1		CBOOT	47nF	Murata	GCM155R71H473ME02D
1	Buck2	CIN	10µF	Murata	GCM21BC71C106KE36
1			0.1µF	Murata	GCM155R71H104KE02D
1		L	0.47µH	TDK	TFM201610ALMAR47MTAA
1		COUT	22µF	Murata	GCM32ER71A226KE12L
1	Buck3	CIN	10µF	Murata	GCM21BC71C106KE36
1			0.1µF	Murata	GCM155R71H104KE02D
1		L	0.47µH	TDK	TFM201610ALMAR47MTAA
1		COUT	22µF	Murata	GCM32ER71A226KE12L
1	Buck4	CIN	10µF	Murata	GCM21BC71C106KE36
1			0.1µF	Murata	GCM155R71H104KE02D
1		L	0.47µH	TDK	TFM201610ALMAR47MTAA
1		COUT	22µF	Murata	GCM32ER71A226KE12L
1	Buck5	CIN	10µF	Murata	GCM21BC71C106KE36
1			0.1µF	Murata	GCM155R71H104KE02D
1		L	0.47µH	TDK	TFM201610ALMAR47MTAA
1		COUT	22µF	Murata	GCM32ER71A226KE12L
1	LDOIN1	CIN	1µF	Murata	GCM155C71A105KE38
1			0.1µF	Murata	GCM155R71H104KE02D
1	LDOIN2	CIN	2.2µF	Murata	GRT155C71A225KE13D
1			0.1µF	Murata	GCM155R71H104KE02D
1	LDOIN3	CIN	2.2µF	Murata	GRT155C71A225KE13D
1			0.1µF	Murata	GCM155R71H104KE02D
-	LDO1	COUT	4.7µF	Murata	GCM21BC71E475KE36
-	LDO2	COUT	4.7µF	Murata	GCM21BC71E475KE36
-	LDO3	COUT	4.7µF	Murata	GCM21BC71E475KE36
-	LDO4	COUT	4.7µF	Murata	GCM21BC71E475KE36
-	LDO5	COUT	4.7µF	Murata	GCM21BC71E475KE36
-	LDO6	COUT	4.7µF	Murata	GCM21BC71E475KE36

Table 1. Recommended BOM

1	GC	Diode	-	-	SOD-128
1		NPN	-	STMicroelectronics	BC817
1		PNP	-	onsemi	BC807
1		MOSFET	-	onsemi	FDD9510L
1		R	1MΩ	YAGEO	RC0603FR-071ML
2		R	100kΩ	YAGEO	RC0603FR-07100KL
1		R	200kΩ	YAGEO	RC0603JR-07200KL
1		R	1kΩ	YAGEO	RC0603FR-071KL

Other recommended values for miscellaneous RCs are shown on the reference schematic (see Schematic Diagrams).

Note: ADC3-5 pins are changed to become outputs and these outputs are low during CVM test in SoC activation. If any external device output is connected directly to ADC3-5 and not through an external mux, the output of the external device has a low impedance path to ground during this time. If the output of the device cannot withstand this, Renesas recommends placing a 10k resistor before the ADC3-5 input pin.

Note: For proper usage of the SDO pins, external pull-ups or pull-downs are required to avoid floating conditions on these signals. Refer to the *Safety Application Note*.

2.4 Board Layout

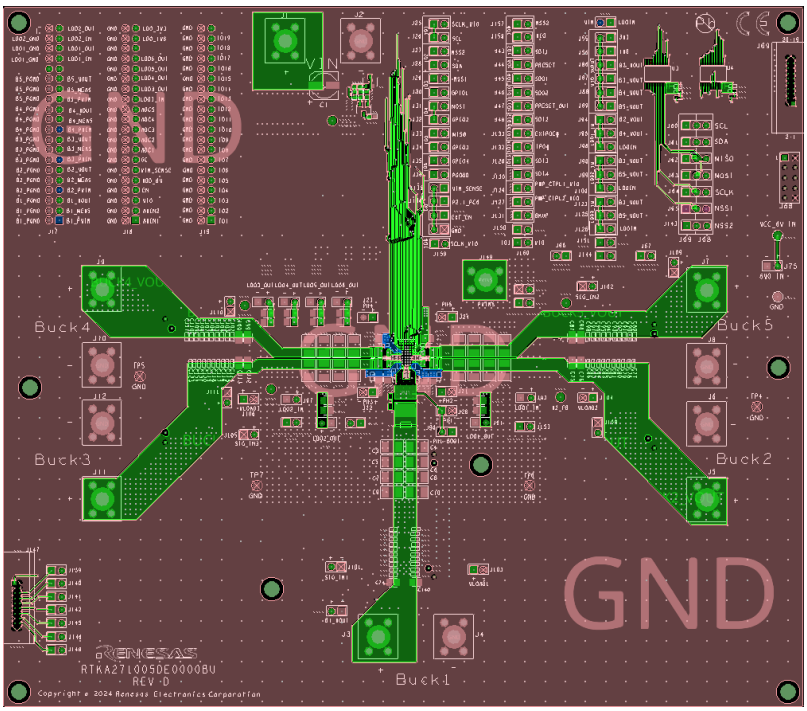

Figure 9. Top Layer

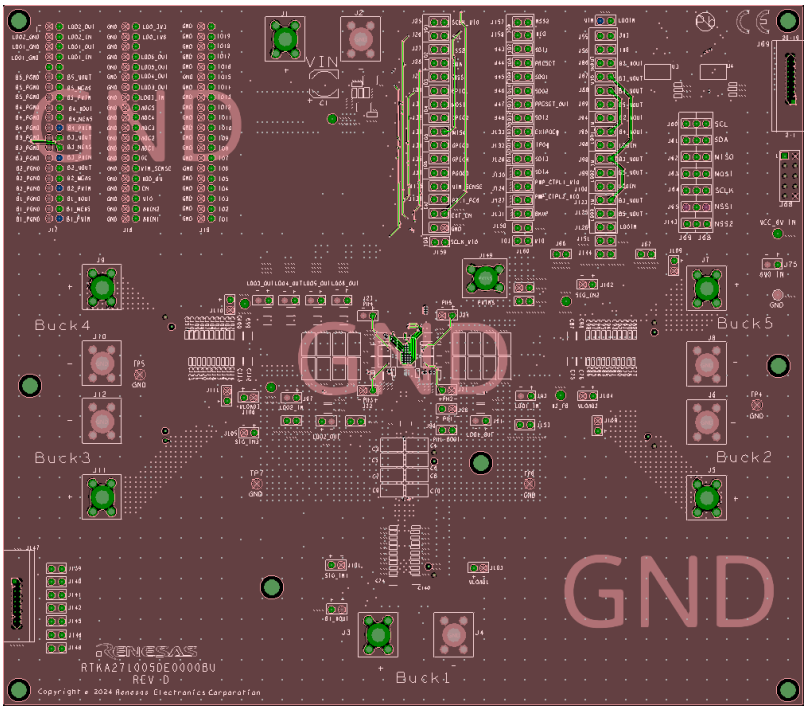

Figure 10. Layer 2

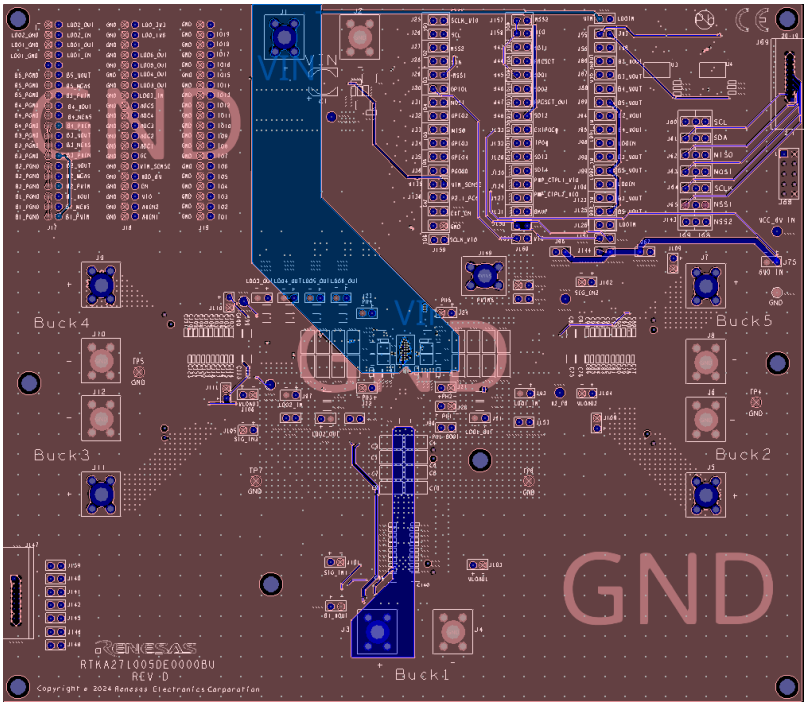

Figure 11. Layer 3

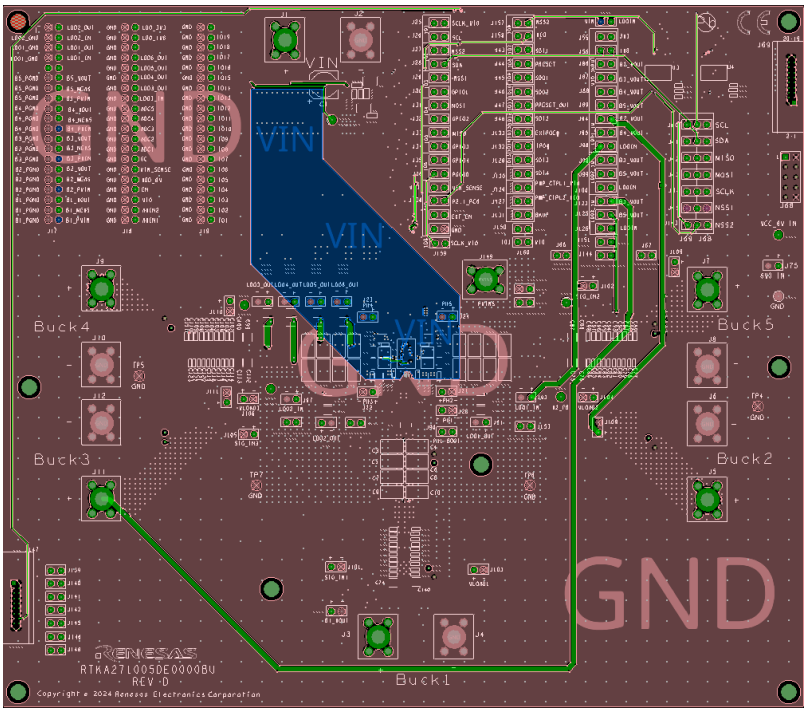

Figure 12. Layer 4

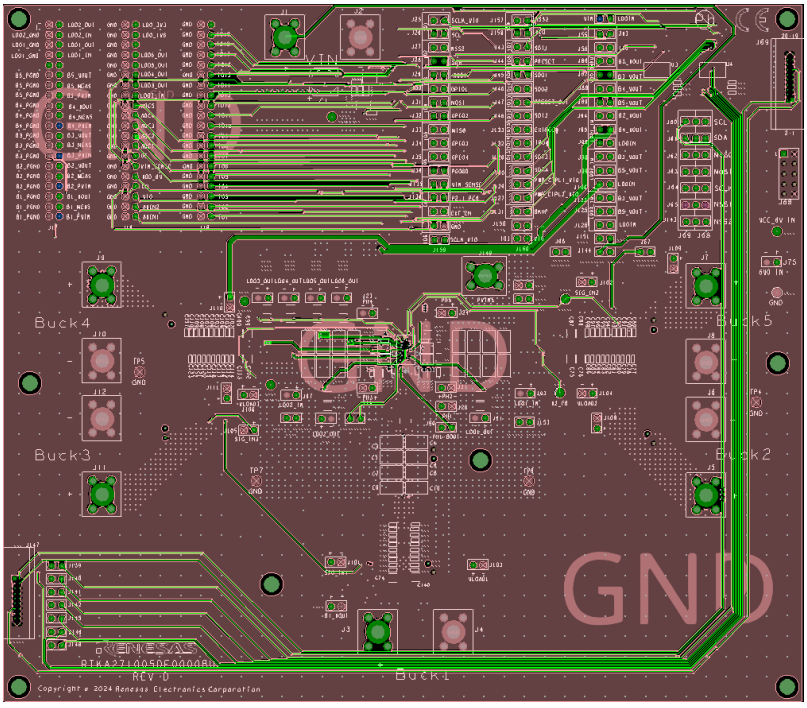

Figure 13. Layer 5

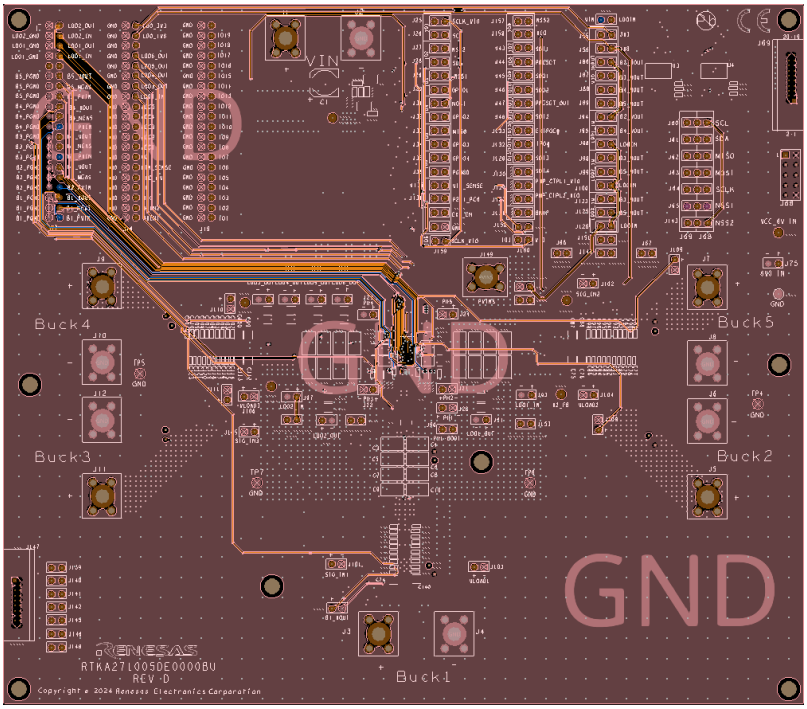

Figure 14. Layer 6

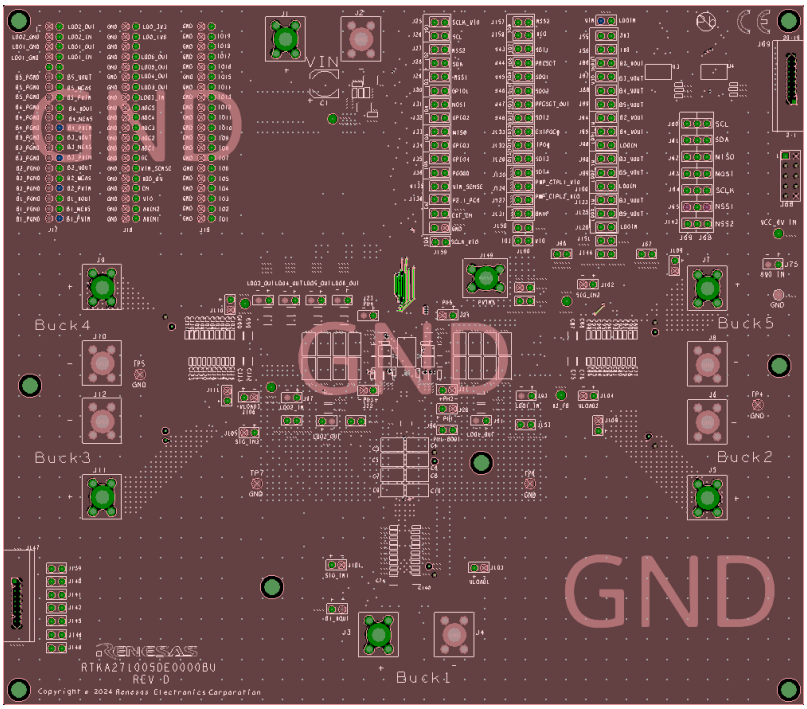

Figure 15. Layer 7

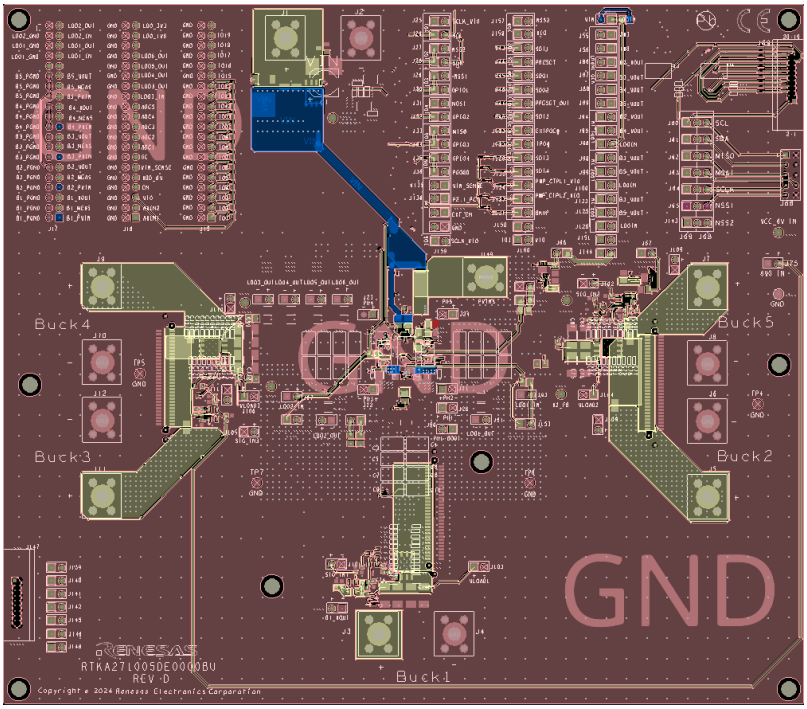

Figure 16. Layer 8

3. Typical Performance Graphs

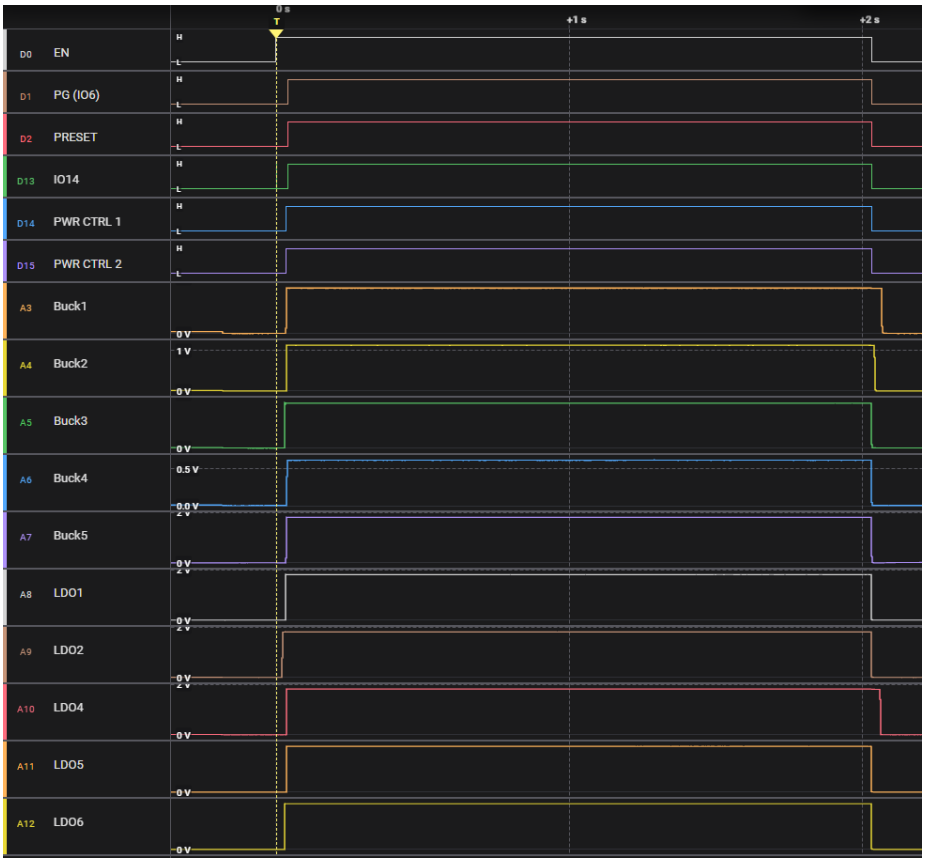

Figure 17. Startup and Shutdown Sequence (V_{IN} = 5V, EN = 5V, VIO = 3.3V)

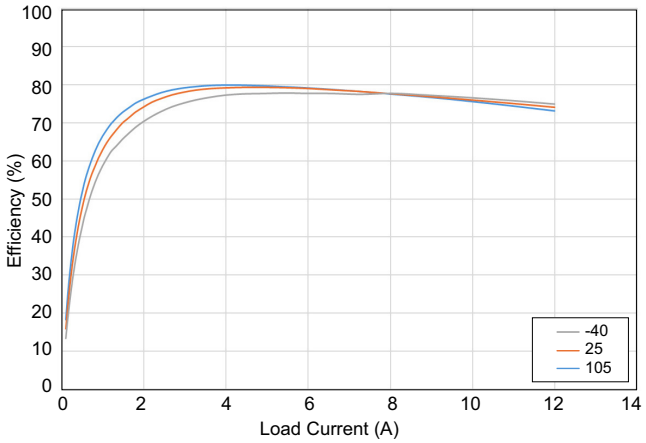

Figure 18. Buck1 Efficiency at V_{IN} = 5V, V_{OUT} = 0.82V, f_{SW} = 2.3MHz

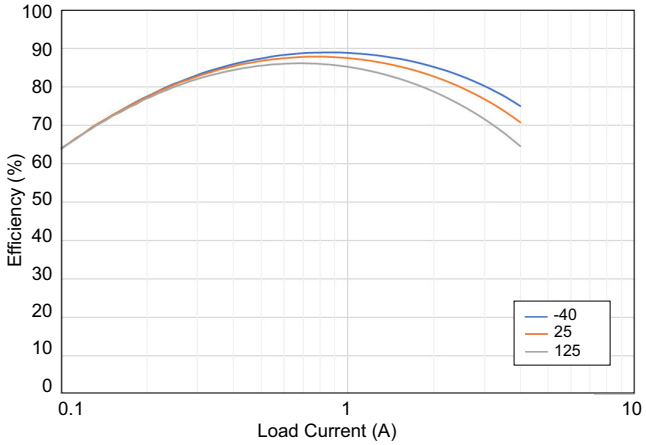

Figure 19. Buck2 Efficiency at V_{IN} = 5V, V_{OUT} = 1.05V, f_{SW} = 2.3MHz

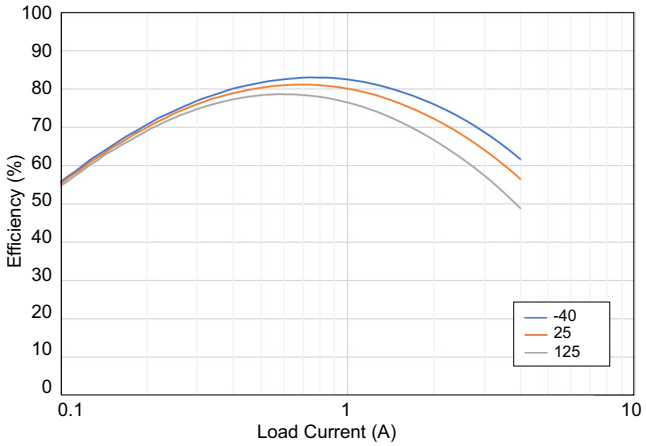

Figure 20. Buck3 Efficiency at V_{IN} = 5V, V_{OUT} = 0.60V, f_{SW} = 2.3MHz

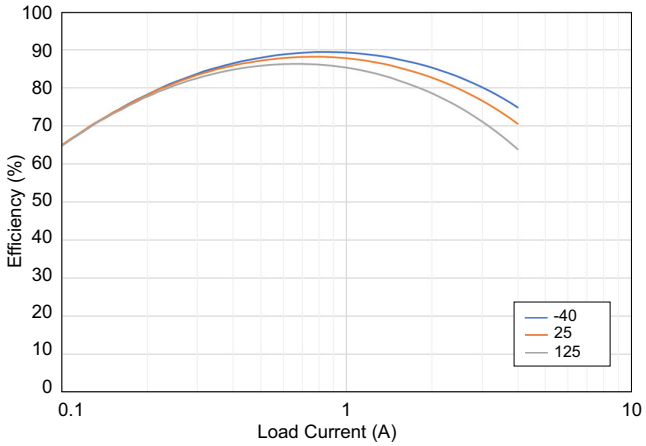

Figure 21. Buck4 Efficiency at V_{IN} = 5V, V_{OUT} = 1.1V, f_{SW} = 2.3MHz

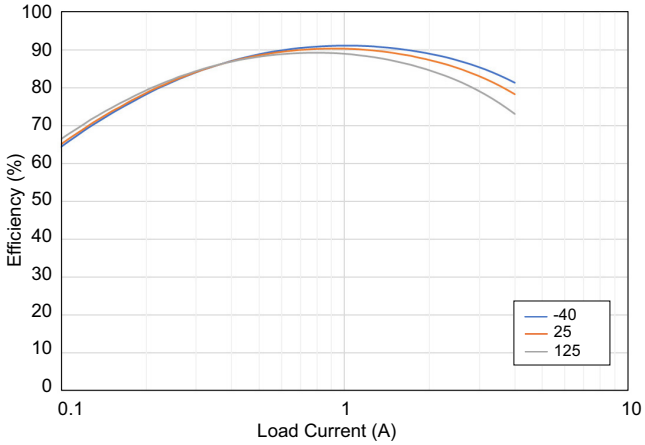

Figure 22. Buck5 Efficiency at V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 2.3MHz

4. Ordering Information

Part Number	Description
RTKA271005DE0000BU	RAA271005 Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Nov 22, 2024	Initial release.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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