RTDTTP4200W066A

4.2kW Digital Bridgeless Totem-Pole PFC

Description

This user guide describes the RTDTTP4200W066A 4.2kW bridgeless totem-pole power factor correction (PFC) evaluation board. Very high efficiency single-phase AC-DC conversion is achieved with Renesas' latest Gen IV (SuperGaN™) TP65H030G4PWS, a diode-free Gallium Nitride (GaN) FET bridge with low reverse-recovery charge. Using Renesas GaN FETs in the fast-switching leg of the circuit and low-resistance MOSFETs in the slow-switching leg of the circuit results in improved performance and efficiency. For more information and complete design files, visit RTDTTP4200W066A-KIT. The RTDTTP4200W066A-KIT is for evaluation purposes only.

Specifications

- Input voltage: 85VAC to 270VAC, 47Hz to 63Hz
- Input current maximum: 19A (rms): (2000W at 115VAC, 4200W at 230VAC)
- 10% overload short time: 20.9A (rms) (2200W at 115VAC, 4400W at 230VAC)
- Ambient temperature: < 100°C
- Output Voltage: 387VDC ±5VDC
- PWM frequency: 66kHz
- Auxiliary supply: 12VDC for bias voltage
- Power dissipation in the GaN FET is limited by the maximum junction temperature (refer to the TP65H030G4PWS Datasheet)

Board Contents

RTDTTP4200W066A PFC Evaluation Board

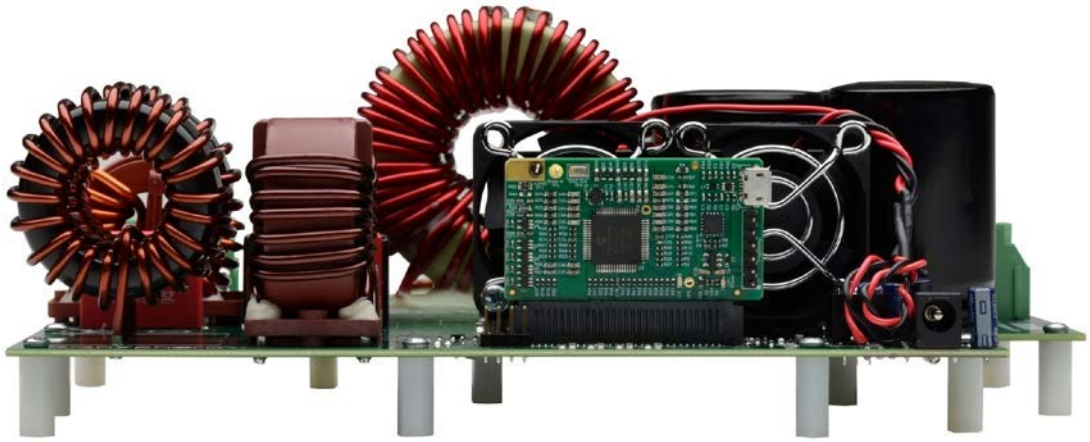


Figure 1. RTDTTP4200W066A-KIT 4.2kW Totem-Pole PFC Evaluation Board

Caution: This evaluation board is intended to validate Renesas's SuperGaN FET technology and is for demonstration purposes only. No guarantees are made for standards compliance. There are areas of this evaluation board that have exposed access to hazardous high-voltage levels. Also note that the evaluation board may retain high-voltage temporarily after input power has been removed. Exercise caution when handling to avoid contact with those voltages. When testing converters on an evaluation board, ensure adequate cooling is used. Apply cooling air with a fan blowing across the converter or across the heat sink attached to the converter. Monitor the converter temperature to ensure it does not exceed the maximum rated per the datasheet specification.

Contents

Figures

1. Input and Output Cable Connections

Figure 2 shows the input and output connections. To reduce EMI noise, adding a ferrite core at the input and output cable is recommended.

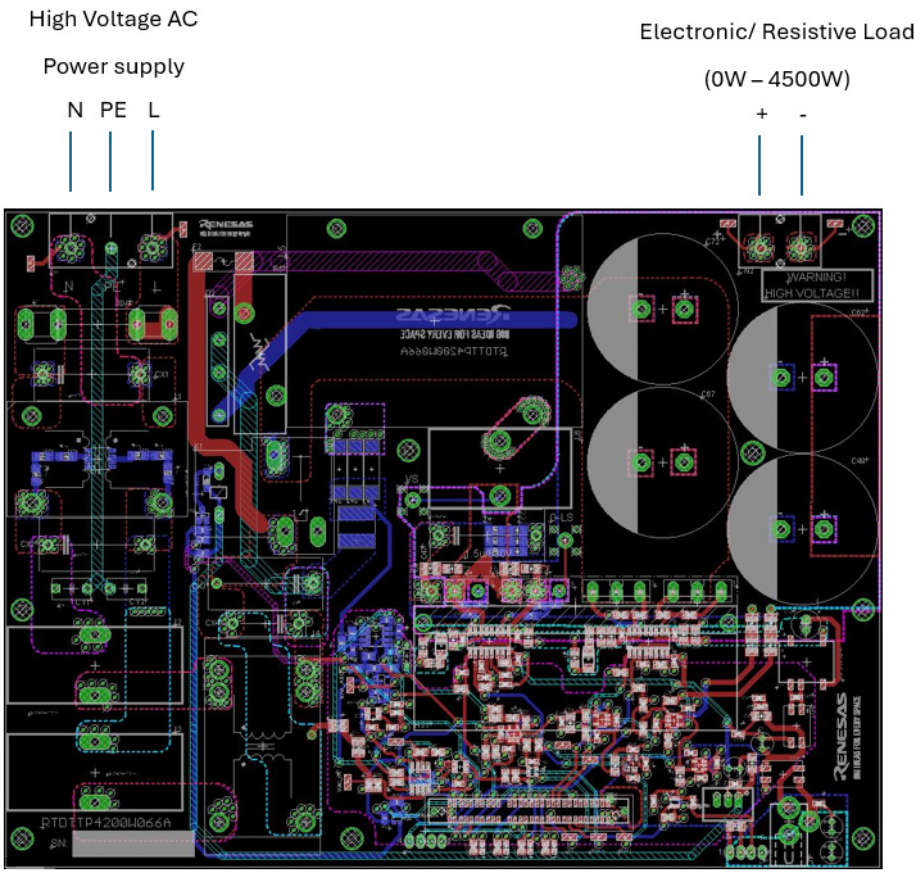


Figure 2. Input and Output Cable Connections

2. Circuit Description for Bridgeless Totem-Pole PFC based on GaN FET

The Bridgeless totem-pole topology is shown in Figure 3. As shown in Fig 3(a), two GaN FETs and two diodes are used for the line rectification, while in Fig 3(b), the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs for line rectification, replacing diodes with IV drops to improve efficiency. For more information on the performance and the characteristics of Bridgeless PFC circuit, see References item [1].

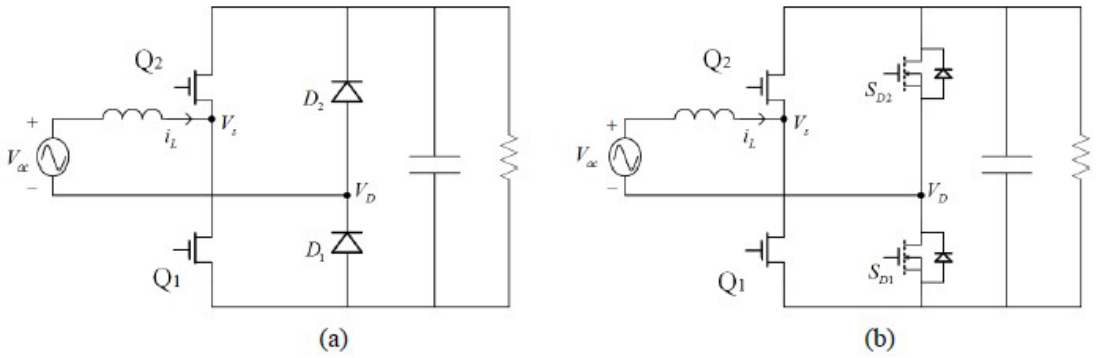


Figure 3. Totem-Pole Bridgeless PFC Boost Converter based on GaN FET

The large recovery charge (Qrr) of existing silicon MOSFETs makes continuous conduction mode (CCM) operation of a silicon bridgeless totem-pole PFC impractical and reduces the total efficiency.

Figure 4(a) is a simplified schematic of a totem-pole PFC in CCM mode, focused on minimizing conduction losses. It is comprised of two fast-switching GaN FETs (Q1 and Q2) operating at a high pulse-width-modulation (PWM) frequency and two very low-resistance MOSFETs (S1 and S2) operating at a much slower line frequency (50Hz/60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S1 and S2 is that of a synchronized rectifier as illustrated in Figures 4(b) and 4(c). During the positive AC cycle (b), S1 is on and S2 is off, forcing the AC neutral line tied to the negative terminal to the DC output. The opposite applies for the negative cycle (c).

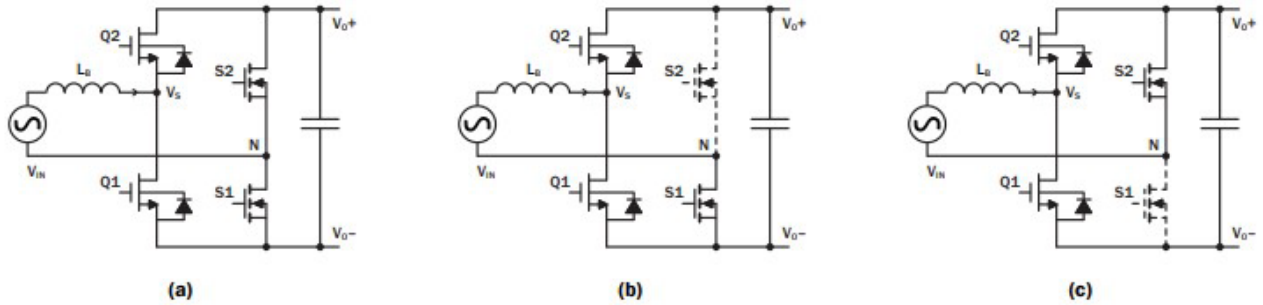
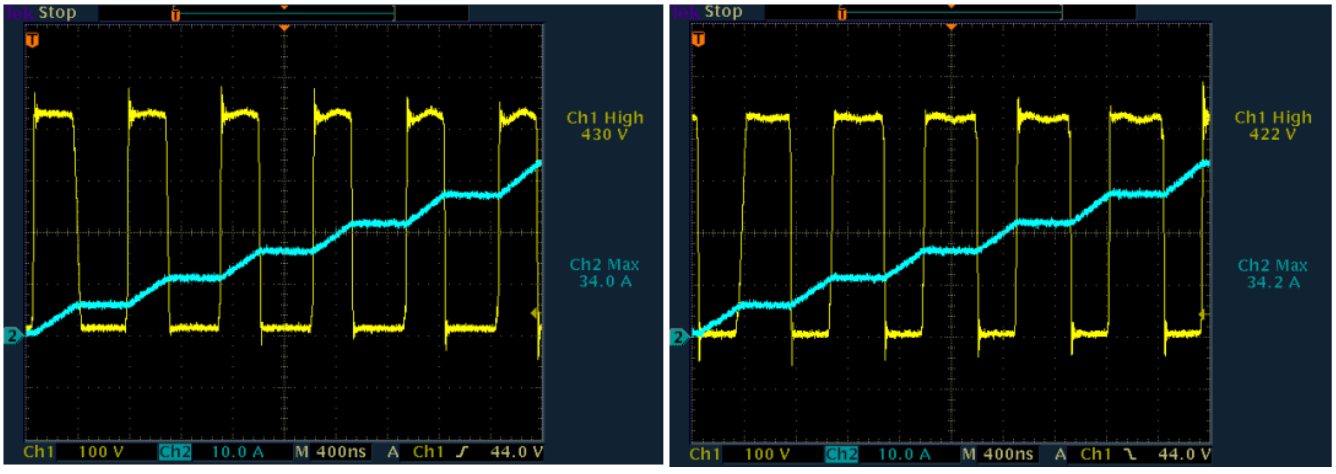


Figure 4. Totem-Pole PFC Schematics with GaN FETs

In either AC polarity, the two GaN FETs form a synchronized boost converter with one transistor acting as a master (controller) switch to allow energy intake by the boost inductor (LB), and the other transistor as a slave (target) switch to release energy to the DC output. The roles of the two GaN devices interchange when the polarity of the AC input changes, thus each transistor must be able to perform both master and slave functions. To avoid shoot-through, a dead time is built in between two switching events during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave (target) transistor must function as a flyback diode for the inductor current to flow during dead time. However, the diode current must quickly reduce to zero and transition to the reverse blocking state once the master (controller) switch turns on. This is the critical process for a totem-pole PFC, which with the high-Qrr of the body diode of high-voltage Si MOSFETs results in abnormal spikes, instability, and associated high switching losses. The low-Qrr of the GaN switches allows designers to overcome this barrier.

In Figure 5, inductive tests at 430V shows clean voltage waveforms up to inductor current exceeding 35A using either a high-side (Figure 5(a)) or low-side (Figure 5(b)) GaN transistor as a master switch. With a design goal of 4kW output power in CCM mode with a 230VAC input, the required inductor current is 20A. This test confirms a successful totem-pole power block with enough current overhead.



(a) (b)

Figure 5. Hard-Switched Waveforms of a Pair of GaN FET Switches

One issue inherent in the bridgeless totem-pole PFC is the operation mode transition at AC voltage zero-crossing. For example, when the circuit operation mode changes from positive half-line to negative half-line at the zero-crossing, the duty ratio of the high-side GaN switch changes abruptly from almost 100% to 0%, and the duty ratio of low-side GaN switch changes from 0% to 100%. Due to the slow reverse recovery of diodes (or body diode of a MOSFET), the voltage VDC cannot jump from ground to VDC instantly and a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio (a soft-start time of a few switching cycles is enough). The RTDTTP4200W066A evaluation board is designed to run in CCM and the larger inductance alleviates the current spike issue at zero-crossing.

3. Dead-Time Control

The required form of the gate-drive signals is shown in Figure 6. The times marked A are the dead times when neither transistor is driven on. The dead-time must be greater than zero to avoid shoot-through currents. The Si8230 gate drive chip ensures a minimum dead-time based on the value of resistor R24, connected to the DT input. The dead-time in **ns** is equal to the resistance in kΩ × 10, so the default value of 12k corresponds to 120ns. This will add to any dead-time already present in the input signals. The on-board pulse generator circuit; for example, creates dead times of about 60ns (see Figure 6). The resulting dead-time at the gate pins of Q1 and Q2 is about 120ns. Shorting or removing R7 reduces the dead-time to 60ns.

Note: The dead-time control can also be set on the firmware. See the Firmware Guide for more information.

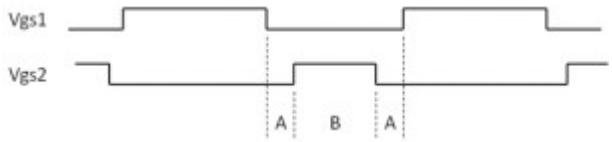


Figure 6. Non-Overlapping Gate Pulses

While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the TP65H030G4PWS GaN FET will switch at dV/dt of 100V/ns or higher to achieve the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown in Figure 9, the recommended layout keeps a minimum gate drive loop and keeps the traces between the switching nodes very short--with the shortest practical return trace to the power bus and ground. The power ground plane provides a large cross-sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the FET to avoid any possible ground loop. Note that the Renesas GaN FETs in TO-247 packages have a pinout configuration of G-S-D, versus the traditional G-D-S of a Si MOSFET. The G-S-D configuration is designed with thorough consideration to minimize the gate source driving loop, reducing parasitic inductance while separating the driving loop (gate source) and power loop (drain source) to minimize noise. All PCB layers of the RTDTTP4200W066A design are shown Figure 9(a-c) and available in the design files.

4. Functional Description

4.1 Setup and Configuration

The board can be used for the evaluation of Renesas TP65H030G4PWS (30mΩ) GaN FETs in a bridgeless totem-pole PFC circuit. It is not a complete circuit, but rather a building block.

4.1.1 Turn-On Sequence

1. Connect an electronic/resistive load to the corresponding marking (CN2).
   a. The requirement for the resistive load:
      i. At 115VAC input: 0W and ≤ 2200W.
      ii. At 230VAC input: 0W and ≤ 4400W.
2. Connect Microchip PIM (MA330048) onto CONN1.
3. Connect the 12VDC auxiliary supply to the demo-board (included in the demo-kit package).
   a. Verify auxiliary LD1 on Microchip PIM is illuminated and LD2 is flashing.
   b. Verify both FANS attached to the heatsink are running
4. With HV power off, connect the high-voltage AC power input to the corresponding marking (CN1) on the PCB.
   a. -N and L (PE: potential ground)
5. Turn on the AC power input (85 to 270 VAC; 50Hz – 60Hz)
   a. Minimum power load for turn-on sequence is 350W.
      i. Monitor CN2 output voltage with VDC meter to verify 385V ±5V is generated.

4.1.2 Turn-Off Sequence

1. Switch off the high-voltage AC power input.
2. Power-off DC bias.
3. Verify input and output voltage = 0.

4.1.3 Operating Structure

1. When VAC is first switched on, VOUT will increase to 390VDC.
   a. Note that all LEDs (LED1 – LED4) on RTDTTP4200W066A board are OFF.
2. After startup is completed, LED1 illuminates continuously to indicate normal operation.
   a. Electronic/resistive load can be increased while AC supply is ON and board is functional.
   b. Loads can be increased by 500W per step, up to the rated power for operation.
3. If OCP is triggered, LED3 and LED4 will blink rapidly and continuously. A complete reset will need to be completed.
   a. Complete reset instructions:
      i. Switch off VAC.
      ii. Remove 12V aux connector and reconnect 12V aux connector to EV board.
      iii. Perform turn-on sequence procedure explained in section 4.1.1.
4. At burst mode, load < 80W, output voltage will reach 410VDC.

4.1.4 Operational Waveforms

Figure 7 and Figure 8 show the converter start-up procedures. For the start-up, there are three phases to charge the DC bus to a reference voltage. In the beginning, the relay K1 is open, and DC bus capacitors are charged by input voltage through NTC and diode bridge. When the VDC is over 100V, the relay K1 is closed to bypass the NTC and the VDC increases to the peak of the input voltage. After 100ms, the GaN FET leg is engaged in voltage closed-loop control, in which the DC bus voltage reference slowly increases to the rated voltage 385VDC. The NTC and diode bridge are applied in this circuit to avoid high inrush current flow through the GaN FETs.

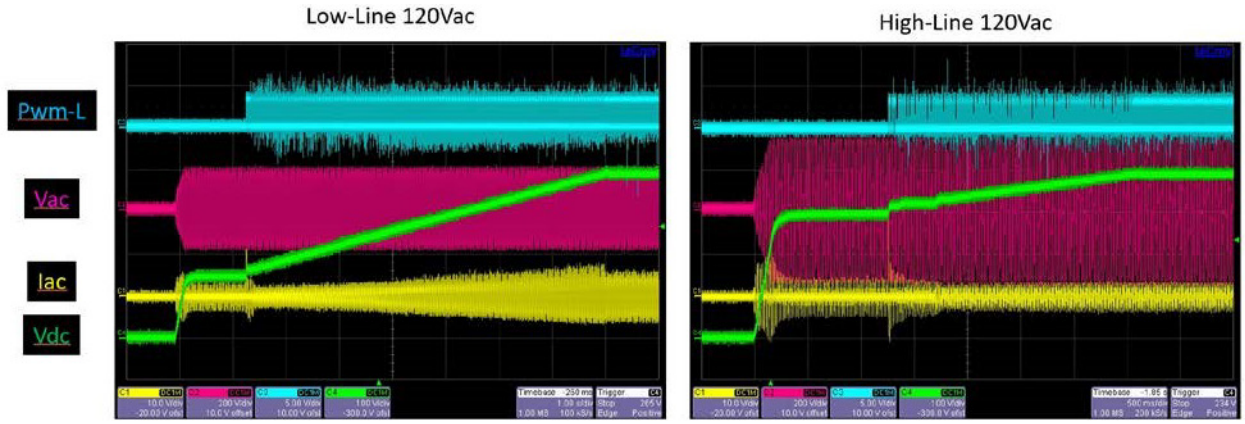


Figure 7. Start-Up of the Bridgeless Totem-Pole PFC Low-Line and High-Line with 380W Load

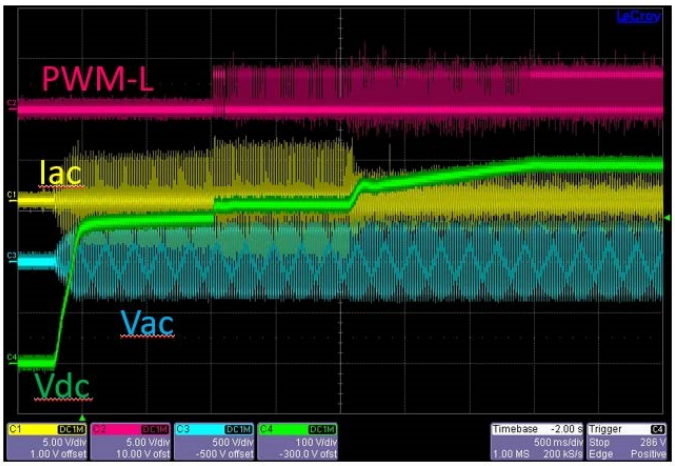


Figure 8. Start-Up of the Bridgeless Totem-Pole PFC High-Line with 1.2kW Load

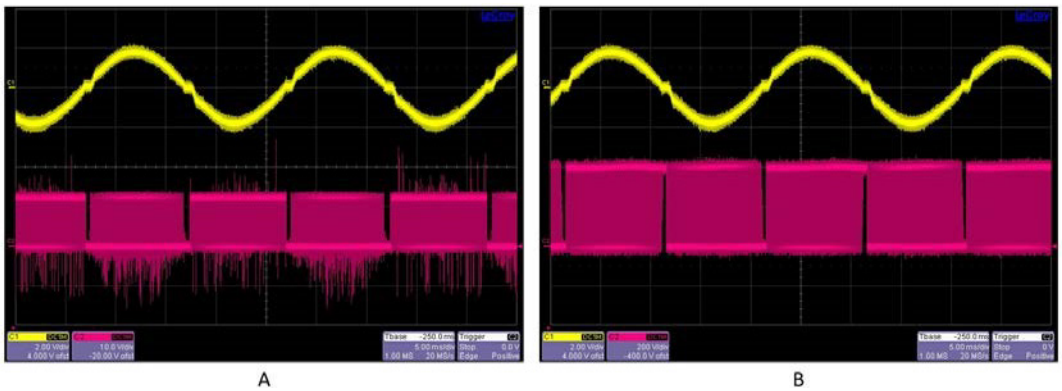
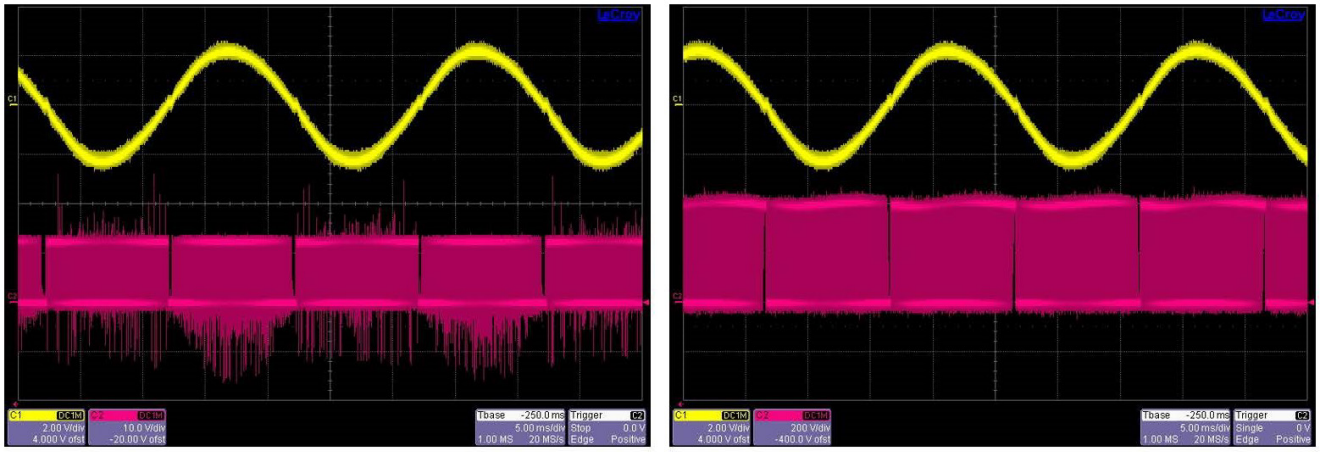


Figure 9. Waveform of Active Switch Version of the Bridgeless Totem-Pole PFC at Low-Line, 1.5kW at Low-Line

CH1: input current Iin (2A/div); CH2: (A) Vgs of Q2 (10V/div), (B) Vds of Q2 (200V/div)



A B

Figure 10. Waveform of Active Switch Version of the Bridgeless Totem-Pole PFC at High-Line, 3.5kW at High-Line

CH1: input current Iin (2A/div); CH2: (A) Vgs of Q2 (10V/div), (B) Vds of Q2 (200V/div)

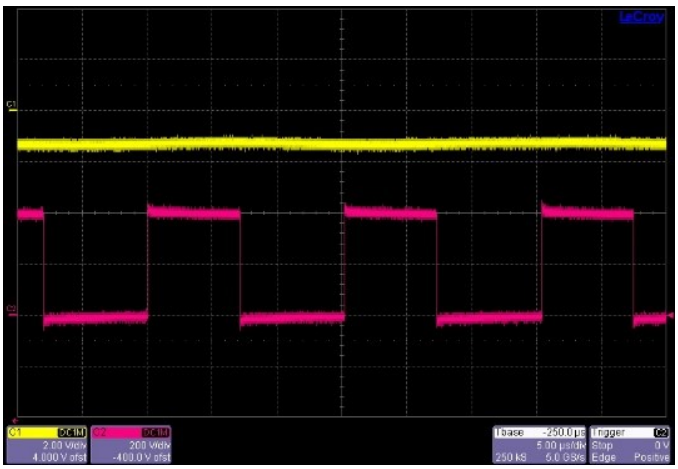


Figure 11. Waveforms of VDS of Q3 at IAC = 16A

CH1: input current Iin (2A/div); CH2: VDS (200V/div)

4.2 Probing

In the demo board, there are two probing sockets for customers measuring VGS and VDS of low-side Gan FET. By removing the jumpers and using a short wire to clamp the current probe, the PFC inductor can also be measured (see Figure 12).

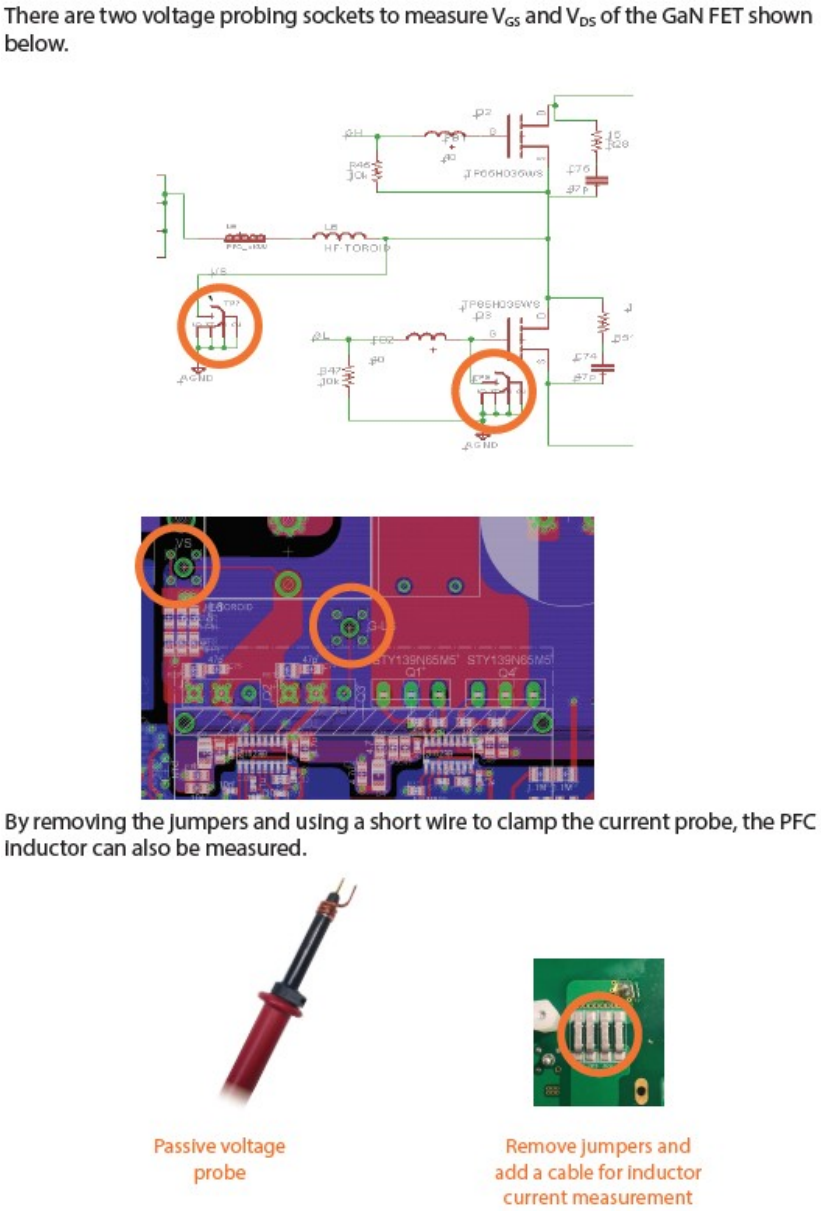


Figure 12. VGS and VDS of Low Side GaN FET Measurement Socket Tips and PFC Inductor Current Measuring Position

4.3 Efficiency Sweep and EMI

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at 120VAC or 230VAC input and 400VDC output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this Totem-Pole PFC board are shown in Figure 13. The extremely high efficiency of 99% at 230VAC input, and > 98% at 120V AC input is the highest among PFC designs with similar PWM frequency. This high efficiency enables customers to reach peak system efficiency to meet and exceed Titanium standards.

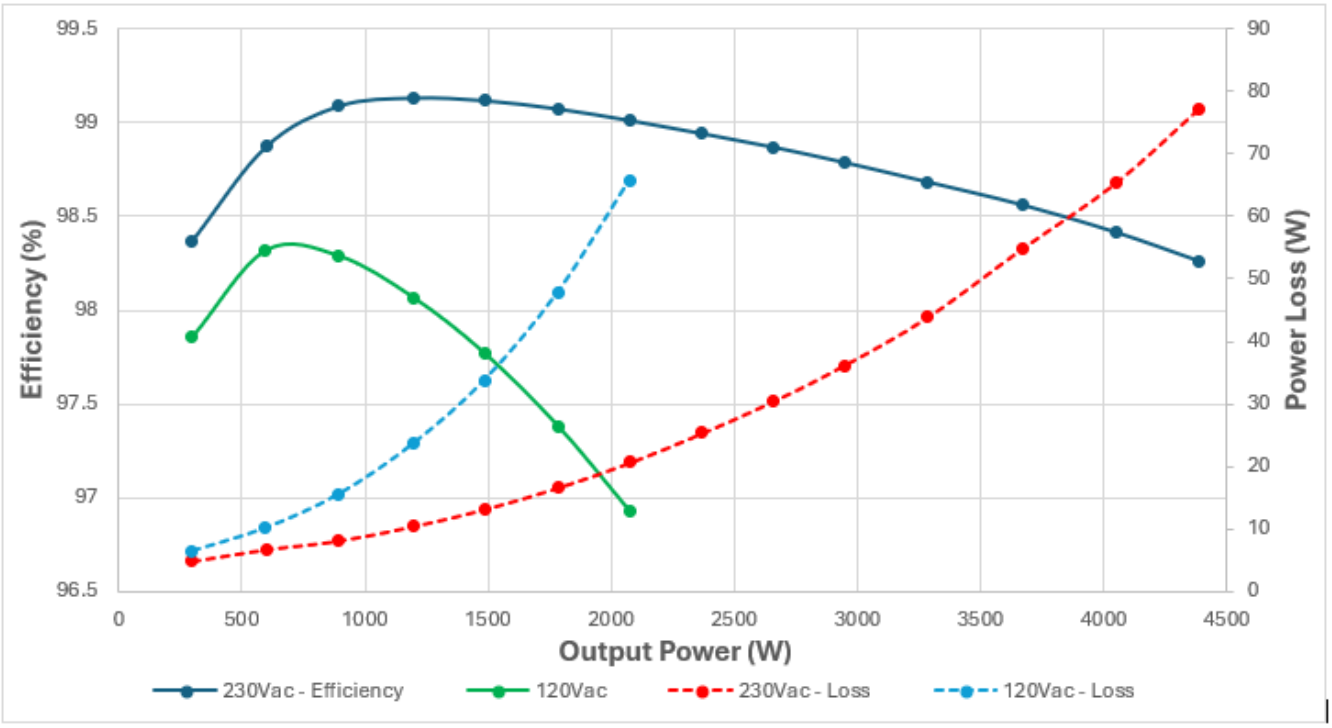


Figure 13. Efficiency Results for Bridgeless Totem-Pole PFC Evaluation Board

Conducted emissions have also been measured for this board using an LIN-115A LISN by Com-Power. The results compared to EN55022A limits are shown in Figure 14. Note that the EMI test was performed by using the lab-use power supply for auxiliary 12V source. Do not use a wall AC-DC adaptor for EMI testing.

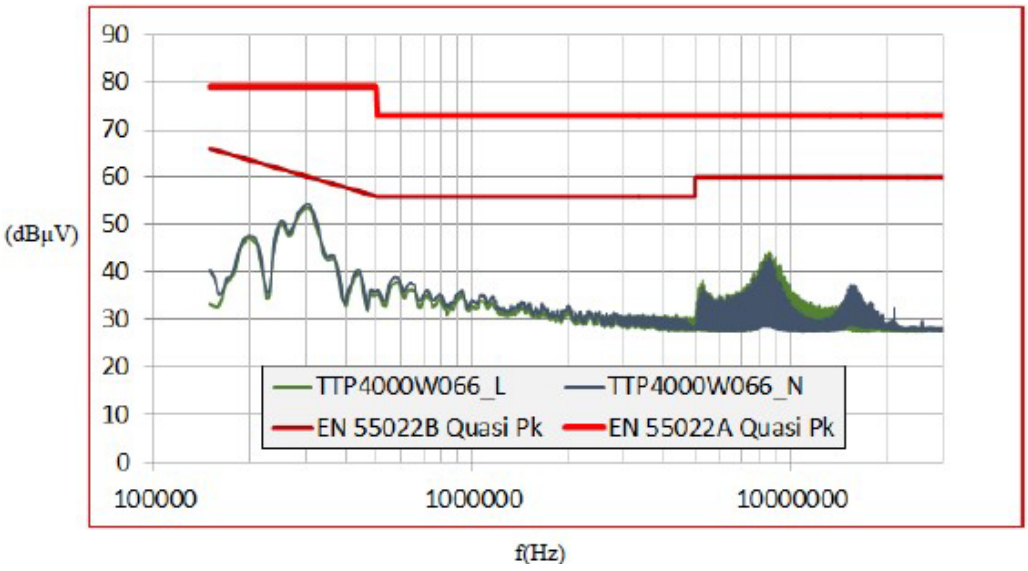


Figure 14. Conducted Emissions at 115V, 1150W

The THDi is measured using WT1800 at the condition of input THDv 3.8% and meets the standards of IEC61000-3-12 (see Figure 15).

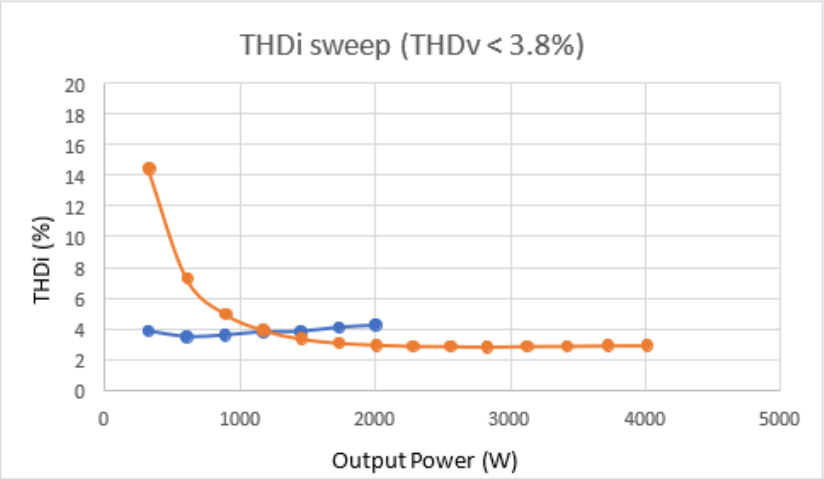


Figure 15. THDi Meets IEC61000-3-12 (> 16A)

4.4 Maximum Load Limit

The RTDTTP4200W066A Bridgeless totem-pole PFC evaluation board is allowed to run overload in a short time. The rated input current for 230VAC input is 19A and the 10% overload current can be 20.9A. The input OCP will be triggered when the current is over 21A.

4.4.1 Load Limit Warnings

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Thus, the following warnings and cautionary measures should be observed:

1. An isolated AC source should be used as input. An isolated lab bench grade power supply or the included AUX DC supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.
2. Use a resistive load only. The Totem-pole PFC kit can work at zero load with burst mode. The output voltage will be swinging between 375V and 385V during burst mode.
3. The demo board is not fully tested at large load steps. DO NOT apply a very large step in the load (>2000W) when it is running.
4. DO NOT manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.
5. The auxiliary VDC supply must be 12V. The demo board will not work under, for example, 10V or over 15V VDC.
6. DO NOT touch any part of the demo board when it is running.
7. When plugging the control cards into the socket, ensure the control cards are fully pushed down with a clicking sound.
8. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.
9. DO NOT use a passive probe to measure control circuit signals and power circuit signals at the same time. GND1 and AGND are not the same ground.
10. To get clean VGS of low side GaN FET, it is recommended not to measure the VDS at the same time.
11. Using passive voltage probe for VDS and VGS measurements and using differential voltage probe for VIN measure measurement at the same time is NOT recommended unless the differential probe has very good dv/dt immunity.

5. Board Design

5.1 Schematic Diagrams

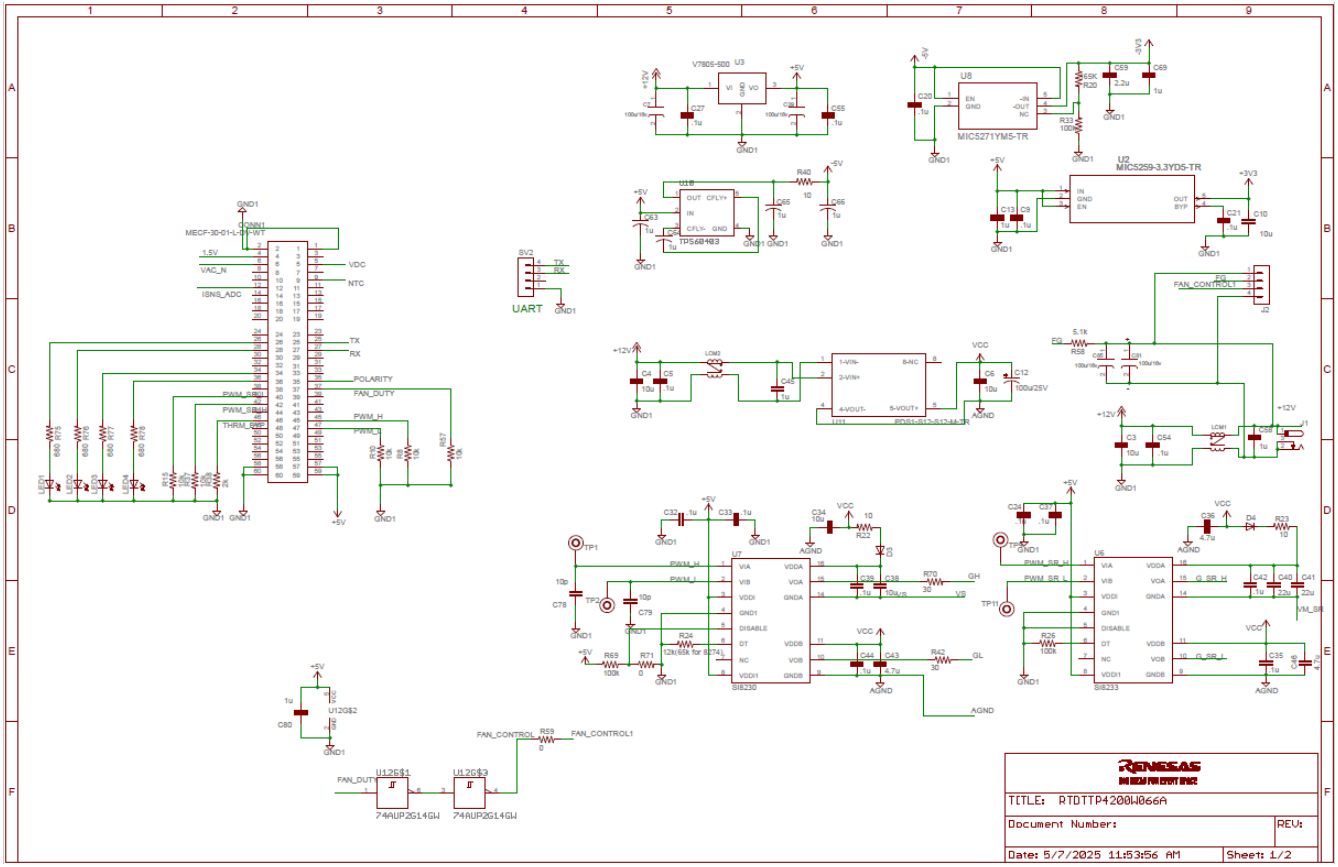


Figure 16. RTDTTP4200W066A Schematic – Page 1

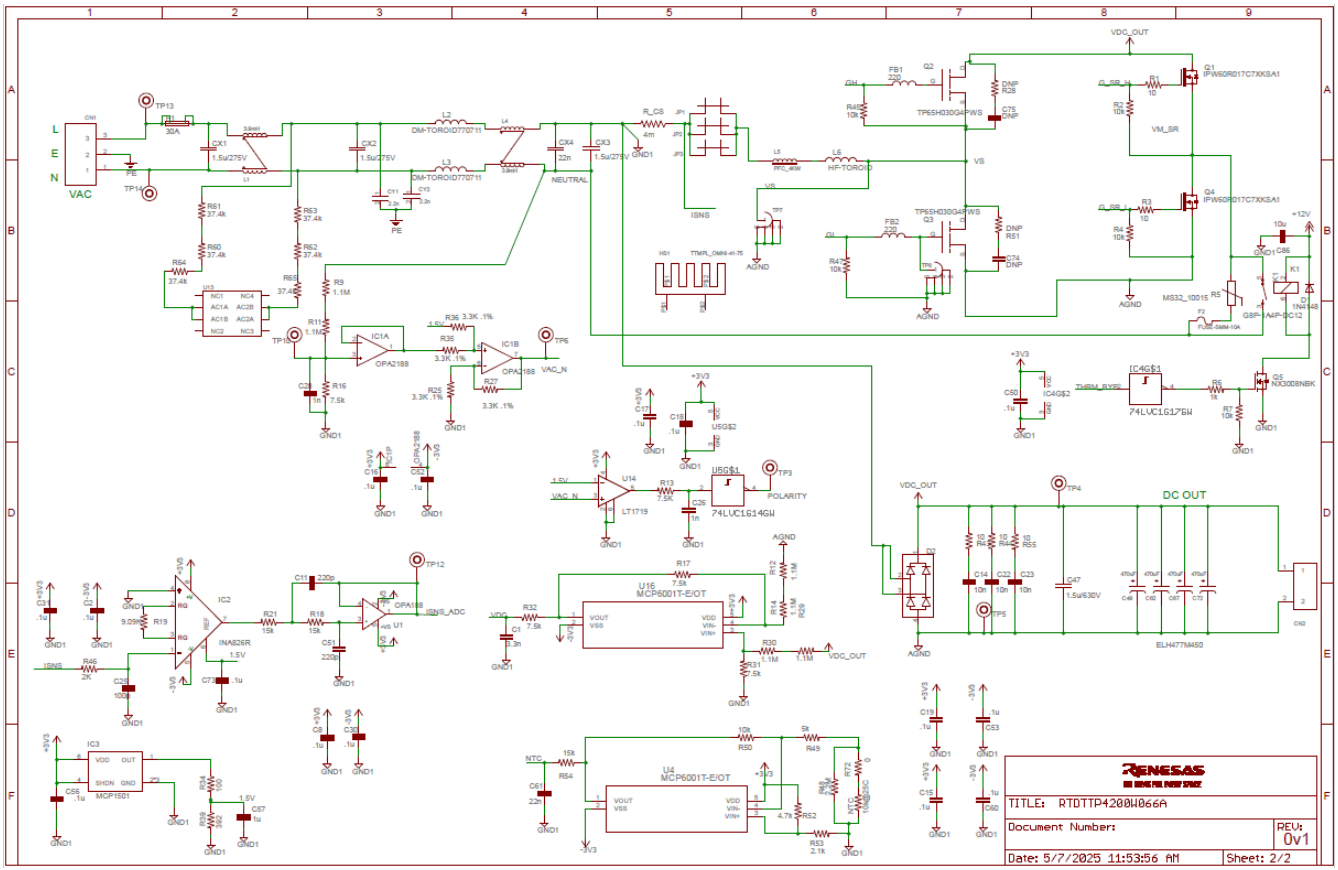


Figure 17. RTDTTP4200W066A Schematic – Page 2

5.2 Board Layers

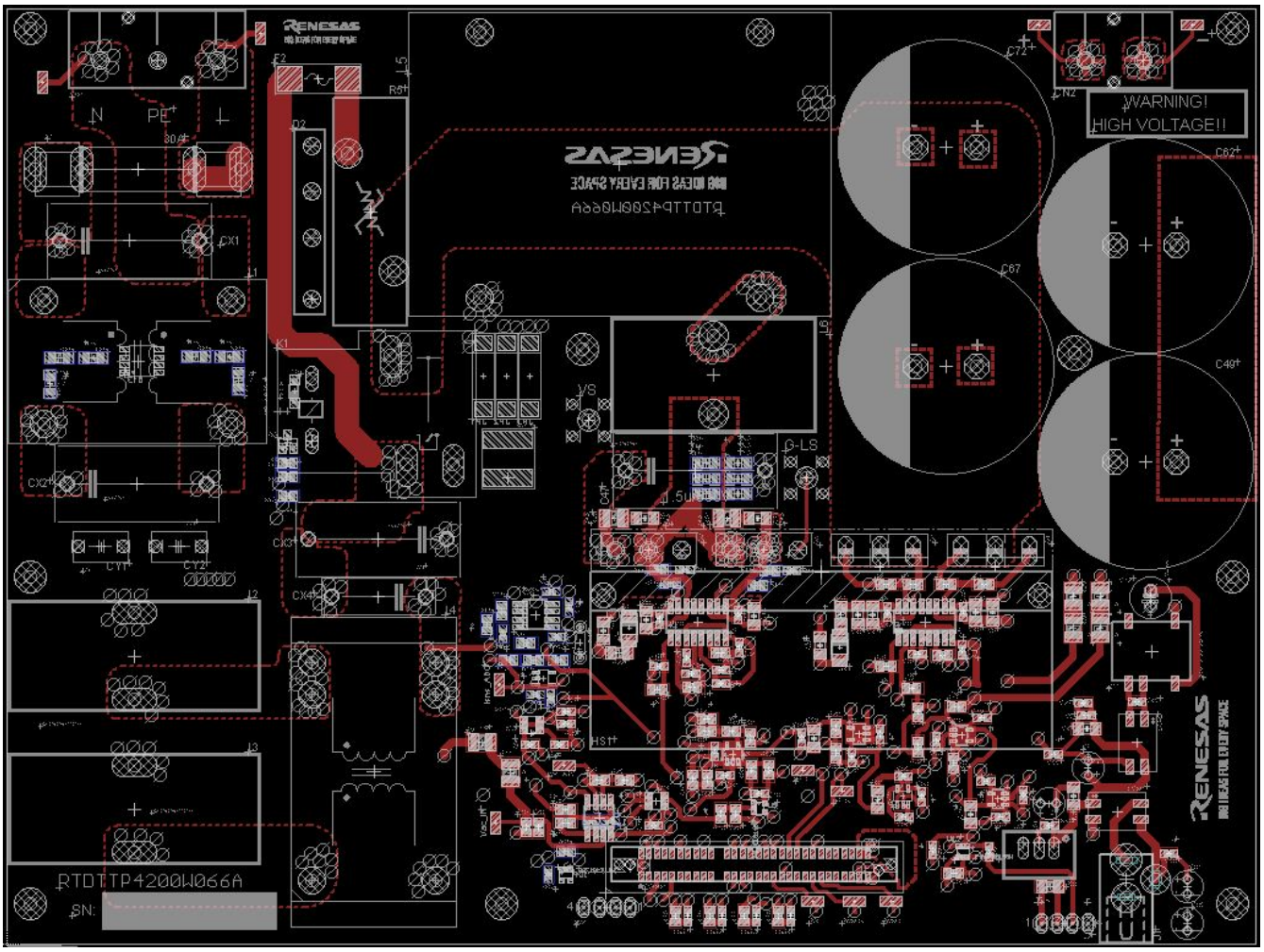


Figure 18. RTDTTP4200W066A Board – Top Layer

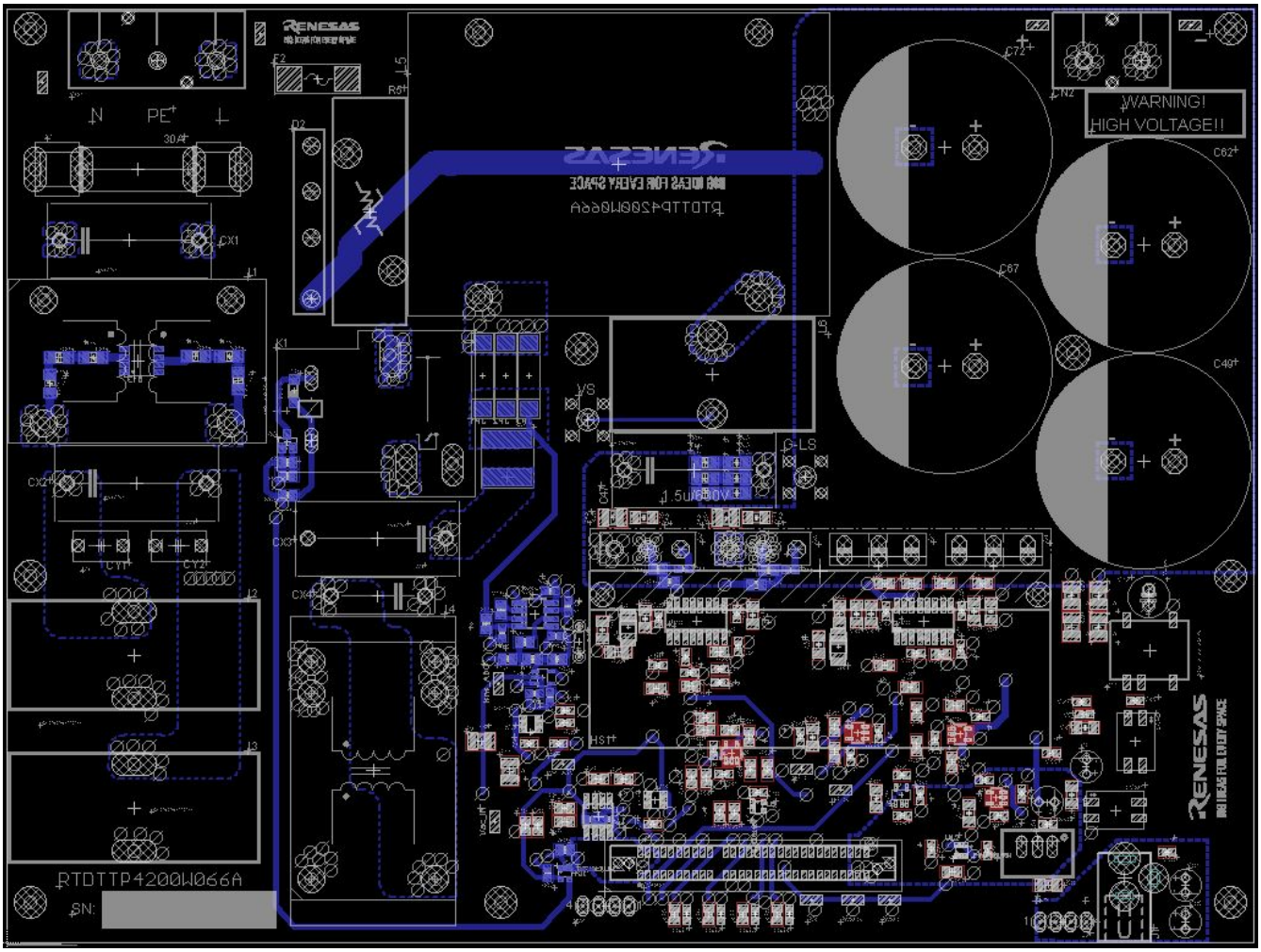


Figure 19. RTDTTP4200W066A Board – Bottom Layer

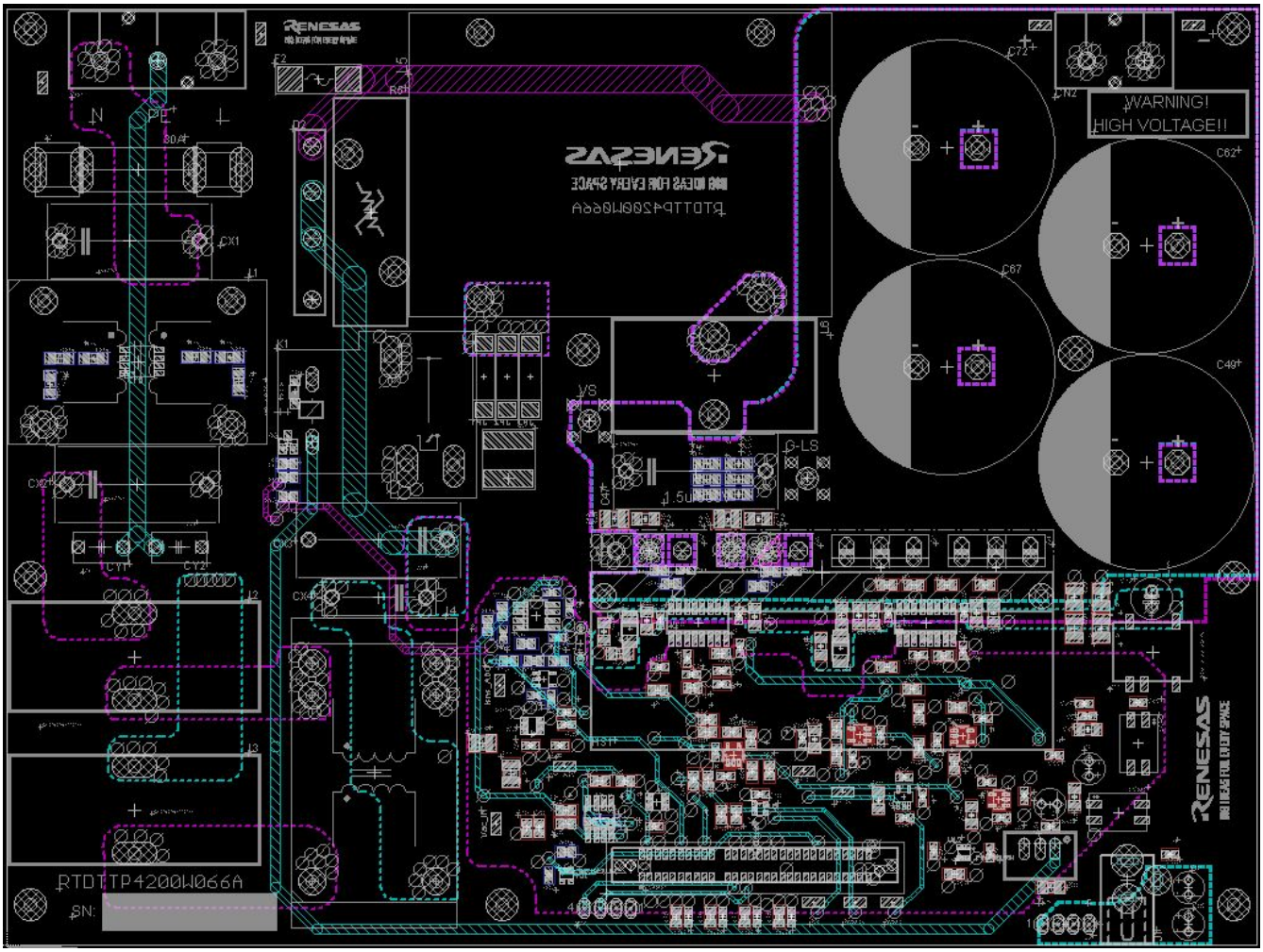


Figure 20. RTDTTP4200W066A Board – Inner Layer 2 (ground plane) + Inner Layer 3 (power plane)

5.3 Bill of Materials

Qty	Reference Designator	Description/Value	Manufacturer Part Number
2	D3, D4	DIODE-DO-214AC	ES1J
4	LED1, LED2, LED3, LED4	LEDCHIP-LED0805	SML-211UTT86
12	TP1, TP2, TP3, TP4, TP5, TP6, TP9, TP10, TP11, TP12, TP13, TP14	TESTPOINT-KEYSTONE5015	5015
30	C2, C5, C8, C9, C15, C16, C17, C18, C19, C20, C21, C24, C27, C30, C31, C32, C33, C35, C37, C39, C42, C44, C50, C52, C53, C54, C55, C56, C60, C73	C-EUC0603, 0.1µF	C0603C104J3RACTU
2	R59, R71	R-US_R0603, 0 ohm	RCS06030000Z0EA
1	R72	R-US_R0805, 0 ohm	RC0805JR-070RL
6	R9, R11, R12, R14, R29, R30	R-US_R1210, 1.1M	KTR25JZPF1104
1	D1	DIODE-SOD123, 1N4148	1N4148W-E3-18
1	R6	R-US_R0805, 1k	ERJ-6ENF1001V

Qty	Reference Designator	Description/Value	Manufacturer Part Number
2	C26, C28	C-EUC0805, 1n	CC0805KRX7R9BB102
6	C13, C45, C57, C58, C69, C80	C-EUC0603, 1µF	TMK107B7105KA-T
4	C63, C64, C65, C66	C-USC0603, 1µF	TMK107B7105KA-T
1	R34	R-US_R0603, 100 ohm	RC0603FR-07100RL
1	R53	R-US_R0805, 2.1k ohm	RC0805FR-072K1L
1	R48	R-US_R0805, 2.2M	RMCF0805JT2M20
1	C59	C-EUC1206, 2.2µF	CL31B225KAHNNNE
1	R46	R-US_R0805, 2K	ERJ-6ENF2001V
1	R38	R-US_R0805, 2k	ERJ-6ENF2001V
4	R25, R27, R35, R36	R-US_R0805, 3.3K .1%	ERA-6AEB332V
1	C1	C-EUC0805, 3.3n	C0805C332K5RACTU
1	R52	R-US_R0805, 4.7k	RC0805FR-074K7L
3	C36, C43, C46	C-EUC1206, 4.7µF	CL31B475KBHNNNE
1	R_CS	RES_CSSH2728, 4m	CSSH2728FT4L00
1	R58	R-US_R1206, 5.1k	RC1206FR-075K1L
1	R49	R-US_R0805, 5k	RC0805FR-075K1L
1	R13	R-US_R0805, 7.5K	ERJ-6ENF7501V
4	R16, R17, R31, R32	R-US_R0805, 7.5k	RN73C2A7K5BTDF
1	R19	R-US_R0805, 9.09k	RC0805FR-079K09L
2	R1, R3	R-US_R0805, 10	ERJ-6GEYJ100V
6	R22, R23, R40, R43, R44, R55	R-US_R1206, 10	ERJ-8ENF10R0V
1	R39	R-US_R0603, 392	RC0603FR-07392RL
3	C14, C22, C23	C-EUC1206, 10n	SMK316B7103KF-T
11	R2, R4, R7, R8, R10, R15, R37, R45, R47, R50, R57	R-US_R0805, 10k	ERJ-6ENF1002V
2	C78, C79	C-EUC0603, 10p	C0603C100K3GACTU
1	C86	C-EUC0805, 10µF	GRM21BR61E106KA73L
6	C3, C4, C6, C10, C34, C38	C-EUC1206, 10µF	12063D106KAT2A
1	R24	R-US_R0805, 12k (65k for 8274)	RC0805FR-0712KL
2	R28, R51	R-US_R1210, 15	RMCF1210FT15R0
3	R18, R21, R54	R-US_R0805, 15kohm	RC0805FR-0715KL
2	R42, R70	R-US_R0805, 30	ERJ-6GEYJ300V
1	C61	C-EUC0805, 22n	C2012C0G1V223J060AC
2	C40, C41	C-EUC1206, 22µF	CL31X226KAHN3NE
6	R60, R61, R62, R63, R64, R65	R-US_R1206, 37.4k	RC1206FR-0737K4L
2	FB1, FB2	FB0603, 220	MMZ1608B221
2	C74, C75	C-EUC1206, 47p	CC1206JKNPOZBN470

Qty	Reference Designator	Description/Value	Manufacturer Part Number
1	U12	74AUP2G14GW	NC7WZ14P6X
1	U5	74LVC1G14GW	NC7SZ14M5X
1	IC4	74LVC1G17GW	SN74LVC1G17DBVR
2	R26, R33	R-US_R0805, 100kohm	ERJ-6ENF1003V
1	C25	C-EUC0603, 100p	06035A101FAT2A
1	R20	R-US_R0805, 165K	ERJ-6ENF1653V
2	C11, C51	C-EUC0805, 220p	CC0805KRX7R9BB221
4	R75, R76, R77, R78	R-US_R0805, 680	RC0805FR-07680RL
2	LCM1, LCM2	CMC_WURTH_744229	744229
1	F2	FUSE-SMM	0463015.ER
1	IC2	INA826R	INA826AID
3	JP1, JP2, JP3	JUMPER_S1621-46R	S1621-46R
1	U14	LT1719	LT1719CS6#TRMPBF
1	IC3	MCP1501T-18E/CHY	MCP1501T-18E/CHY
2	U4, U16	MCP6001T-E/OT	MCP6001T-E/OT
1	CONN1	MECF-30-01-L-DV-WT	MECF-30-01-L-DV-WT
1	U2	MIC5259-3.3YD5-TR	MIC5259-3.3YD5-TR
1	U8	MIC5271YM5-TR	MIC5271YM5-TR
1	U13	CAP200DG	CAP200DG
1	Q5	NX3008NBK	NX3008NBK,215
1	U1	OPA188	OPA188AIDBVT
1	IC1	OPA2188	OPA2188AIDR
1	U11	PDS1-S12-S12-M-TR	PDS1-S12-S12-M-TR
1	U7	SI8230	SI8230BB-D-IS1
1	U6	SI8230	SI8233BB-D-IS1
1	U10	TPS60403	TPS60403DBVR
1	U3	V7805-500, 5V DC-DC converter	TR05S05
1		DSPIC33CK256MP506 DIGITAL POWER	MA330048
9	standoff (nylon 1/2)	standoff (nylon 1/2)	1902C
9	machine screw (ss 1/2)	machine screw (ss 1/2)	9902
4	Thermal pad for Q2, Q3, Q1, Q4	Thermal pad for Q2, Q3, Q1, Q4	4169G
1	D2	GBJ2506	GBJ2506-BP
2	screws for FETs to HS (Q2, Q3)	screws for FETs to HS (Q2, Q3)	6/32
2	SV2, J2	MA04-1	961104-6404-AR
1	J1	PJ-002AH	PJ-002AH
2	TP7, TP8	TEKTRONIX-PCB	131-4353-00

Qty	Reference Designator	Description/Value	Manufacturer Part Number
3	CX1, CX2, CX3	155MKP275KG, 1.5μ/310Vac	890334026030cs
1	CN2	2PIN_9.53MM	20020705-M021B01LF
1	L1	CMC_42X27MM_SM, 3.9mH	T60405-R6128-X225
1	CN1	3PIN_9.53MM	T70343500000G
2	CY1, CY2	VY2_CAP_SAFETY, 4.7n	B32021A3472M
1	L4	CMC_42X27MM, 7.2mH	T60405-R6128-X230
1	NTC	R-US_0204/5, 10k@25C	B57703M103G40
1	C47	FILM-CAP-C4ATGB_5100, 10uH	890334026030cs
1	CX4	ECQ-U2A474ML22N, 22n	PME271M522MR30
1	F1	SH32, 30A	01020078H
1	R69	R-US_R0603, 100kohm	DNI
4	C7, C29, C81, C85	ELE_CAP_D5MM_P2MM, 100μ/16v	UKL1C101KPDANA
1	C12	CPOL-USE2.5-7, 100μ/25V	ESK107M025AC3AA
4	C49, C62, C67, C72	ELE_CAP_D35MM_P10MM, 470μF	ELXS451VSN471MA45S
2	L2, L3	DM-TOROID770711	CWS-1SN-12606
1	K1	G8P-1A4P-DC12	JTN1AS-PA-F-DC12V
1	L6	HF-TOROID	CWS-1SN-12554
1	HS1	HS-OMNI-41-75	OMNI-UNI-41-75
1	R5	MS35_10015	MS32 10015-B
1	L5	019-8598-00R	019-8598-00R
2	Q1, Q4	IPW60R017C7XKSA1	IPW60R017C7XKSA1
2	Q2, Q3	TP65H030G4PWS	TP65H030G4PWS
1	Power adaptor	Power adaptor	SMI6B-12-4-P5R

6. References

[1]. Liang Zhou, Yi-Feng Wu and Umesh Mishra, “True Bridgeless Totem-pole PFC based on GaN FETs”, PCIM Europe 2013, 1416 May 2013, pp.1017-1022.

[2]. L. Huber, Y. Jang, and M. M. Jovanovic, “Performance evaluation of Bridgeless PFC boost rectifiers,” IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp. 1381-1390, May 2008.

7. Ordering Information

Part Number	Description
RTDTTP4200W066A	RTDTTP4200W066A Evaluation Board

8. Revision History

Revision	Date	Description
1.00	Jul 2, 2025	Initial release.

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