User's Manual

32

RH850 Evaluation Platform

RH850/U2C 404pin

User's Manual: Piggyback Board

Y-RH850-U2C-404PIN-PB-T1-V1

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Rev.2.00 Jan 2026

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2C 404pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2C 404pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document active low signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g. the reset pin is named RESETZ or RESET#.
3. In this document the following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2C-404PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2C-404PIN-PB-T1-V1 package contains all these items. *Table 1.1 Package Components for Y-RH850-U2C-404PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2C-404PIN-PB-T1-V1 package.

Table 1.1 Package Components for Y-RH850-U2C-404PIN-PB-T1-V1

Item	Description	Quantity
D019726	RH850/U2C 404pin piggyback board	1
D020252	Documentation CD	1
D010818-24	WEEE+CE document	1
D020251-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	40 (board version D019726_06_V01) 42 (board version D019726_06_V02) 45 (board version D019726_06_V03 and later)
Red Hirschmann 4 mm power lab socket	In the bag	1
Resonator, HC49, 8 / 16 / 24 MHz	In the bag	3

Note

Please keep the Y-RH850-U2C-404PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2C-404PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

Note

It is not possible to use all functions of the piggyback board with each main board.
For the best feature match the main board “Y-COMMON-MB-T1-V1” should be used.

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with power supply from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.09 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - Support JTAG/LPD/RHSIFD
  - 46-pin Aurora Debug Connector (e.g. for using Renesas IE850A emulator)
  - 14-pin connector for E2 emulator
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 8 / 16 / 20 / 24 MHz Crystal Resonator
- Eight general purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Jumpers to configure CAN XL connection to main board
- Jumpers to configure Ethernet connections to main board
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the piggyback board are available:

Table 1.2 Y-RH850-U2C-404PIN-PB-T1-V1 board versions

Board Version	Schematic Version
D019726_06_V01	D019726_04_V0110
D019726_06_V02	D019726_04_V0200
D019726_06_V03	D019726_04_V0310

Table 1.3 lists all modifications that have been implemented in board versions D019726_06_V01, D019726_06_V02 and D019726_06_V03.

Table 1.3 Differences between board versions V01, V02 and V03

Item	Modified Function	Detailed Description of Changes	D019726_06_V01	D019726_06_V02	D019726_06_V03
1	Pull-down resistor on RESET# signal input to IC4	A pull-down resistor has been added to the RESET# signal input.	The pull-down resistor has been connected manually.	The pull-down resistor is part of the board design.	
2	TRST_TOOL# signal	Changed connections of TRST_TOOL# signal.	Connected to connector CN10 for Aurora I/F only.	Connected to connector CN10 for Aurora I/F and to connector CN9 for E2 debug I/F.	
3	Reset signal inputs	Reset Adapter was removed and signalling for RESET#_in was changed.	Connectors CN19 – CN21 could be used to input external signals for Reset sources.	Connectors CN19 – CN21 have been removed.	
4	Ethernet signals	Make signal connection for ETH1MDIO and ETH1MDC more flexible	Signal connections fixed: ETH1MDIO = P21_0 ETH1MDC = P20_11	Signal connection flexible: ETH1MDIO = P21_0 or P04_9 ETH1MDC = P20_11 or P04_8	
5	Ethernet 1 signal port connection on connector CN3	Changed pins on CN3	ETH1_SG_RXD_N – CN3[108] ETH1_SG_RXD_P – CN3[106] ETH1_SG_TXD_N – CN3[102] ETH1_SG_TXD_P – CN3[100]	ETH1_SG_RXD_N – CN3[120] ETH1_SG_RXD_P – CN3[118] ETH1_SG_TXD_N – CN3[114] ETH1_SG_TXD_P – CN3[112]	
6	Ports connected to main board as DIGIO_13, DIGIO_14 and	Changed ports used on RH850/U2C for	DIGIO_13 = CN1[98] = P00_5	DIGIO_13 = CN1[98] = P06_2	

Item	Modified Function	Detailed Description of Changes	D019726_06_V01	D019726_06_V02	D019726_06_V03
	DIGIO_15	DIGIO ports	DIGIO_14 = CN1[99] = P00_6 DIGIO_15 = CN1[100] = P00_7	DIGIO_14 = CN1[99] = P06_3 DIGIO_15 = CN1[100] = P06_4	
7	Jumper for signalling LED	Renamed jumper	Jumper is named CN11	Jumper is named JP20	
8	Production test	Added circuit for production tests.	---	JP19 and some circuitries were added.	
9	Pull-up / pull- down jumper	On board version D019726_06_V02 only the pull-down resistor R60 is connected to GND, R61-R67 are not connected to GND.	Function is correct.	Added manually a bridge from R60 to R61-R67 so all pull-down resistors have a GND connection.	
10	GreenPAK IC (IC4)	Updated version of GreenPAK IC to improve functionality.	SLG46855-AP		SLG7RN47274-AP_r004
11	Ethernet T1S connection	Added jumper to switch functionality of port P20_3 between MII and T1S interface.	---	---	Added jumper JP21.
12	Termination resistors	Removed termination resistors R8 – R11	Termination resistors R8 -R11 with value of 33 Ohm assembled.		Replaced termination resistors by switches IC8 – IC11 and jumpers JP22 and JP23.
13	CAN XL connections	Switch functionality of port P17_2, P17_3, P24_7 and P24_8 to improve signal quality for CAN XL interfaces.	---	---	Added jumpers JP22 and JP23.
14	Aurora interface circuit	Reduced values of pull-up resistors R26, R27 and R28 to improve functionality	R26 = R27 = R28 = 4.7kOhm		R26 = R27 = 470 Ohm R28 = 1kOhm

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

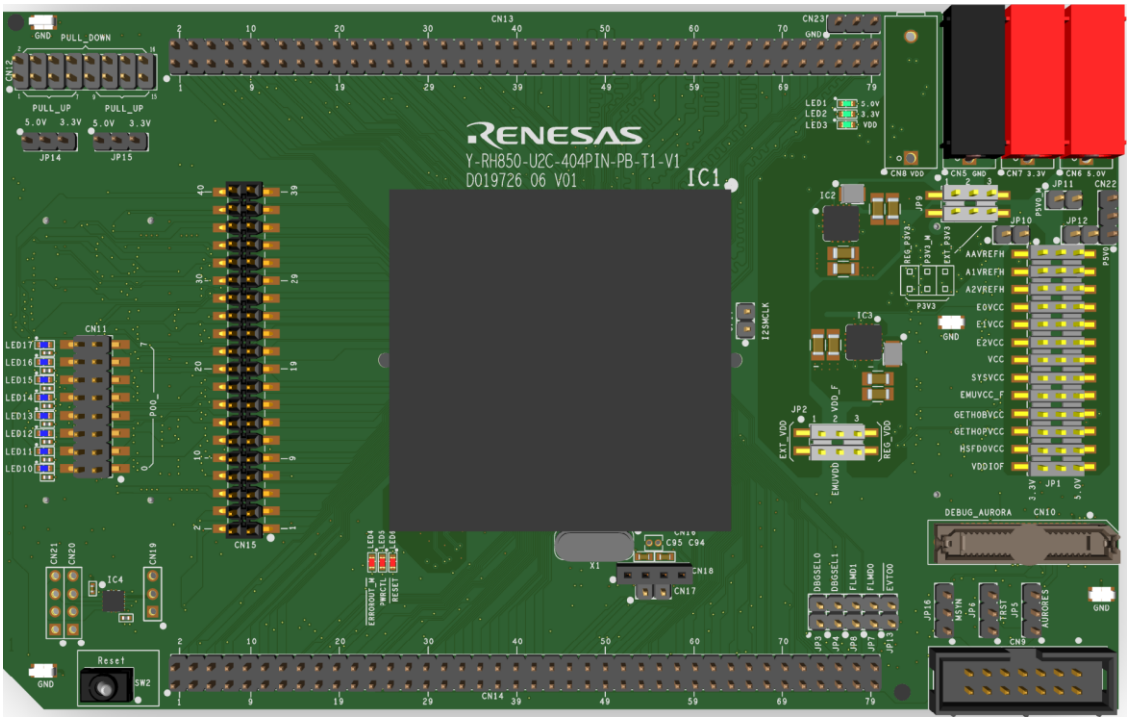


Figure 1.1 Piggyback board top view of board version D019726_06_V01

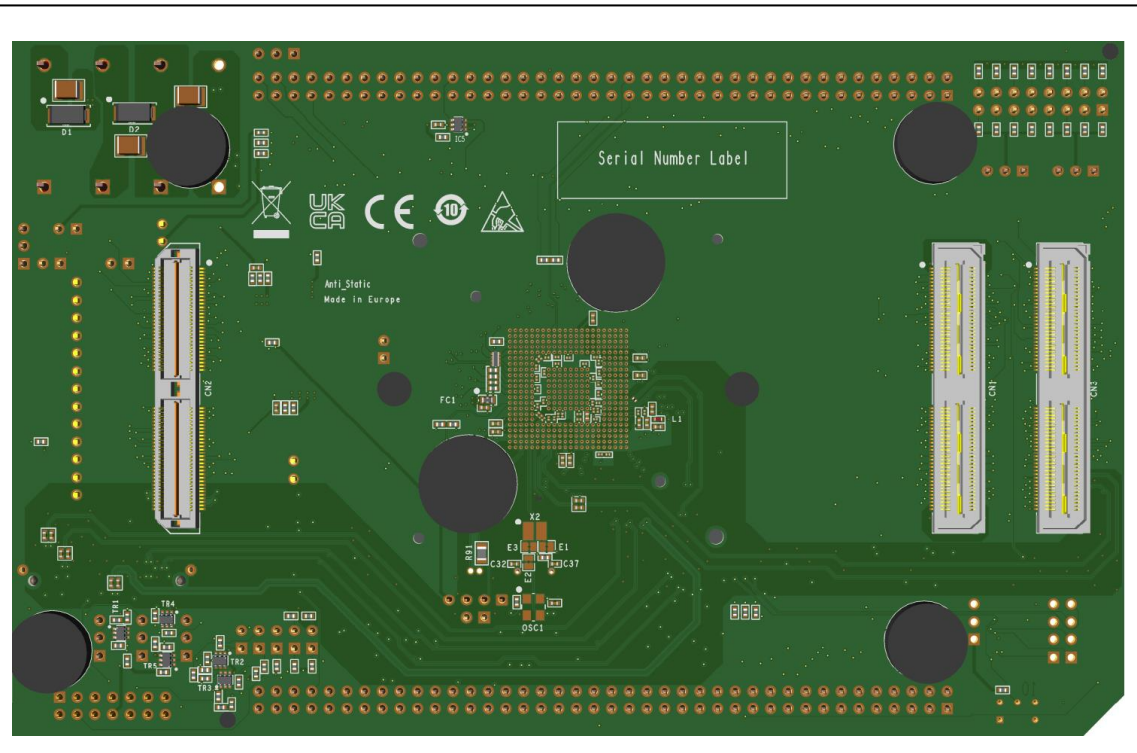


Figure 1.2 Piggyback board bottom view of board version D019726_06_V01

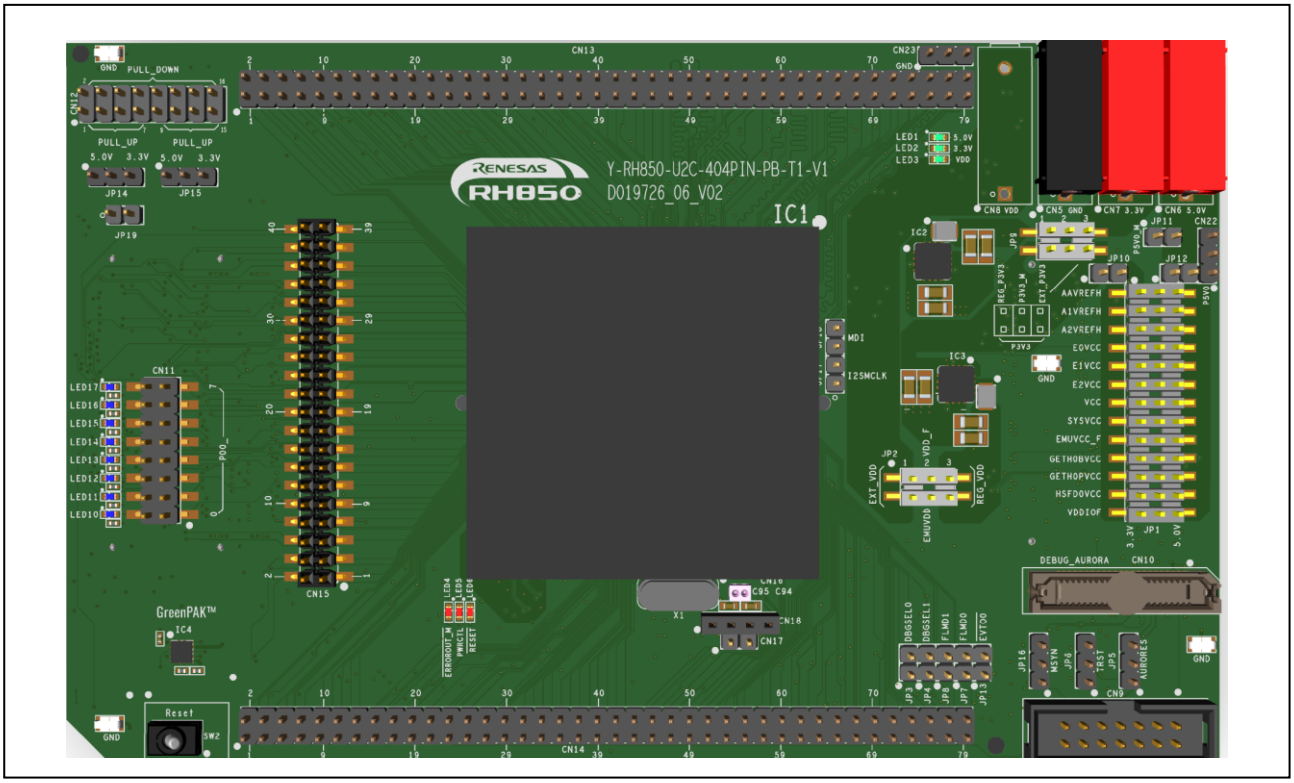


Figure 1.3 Piggyback board top view of board version D019726_06_V02

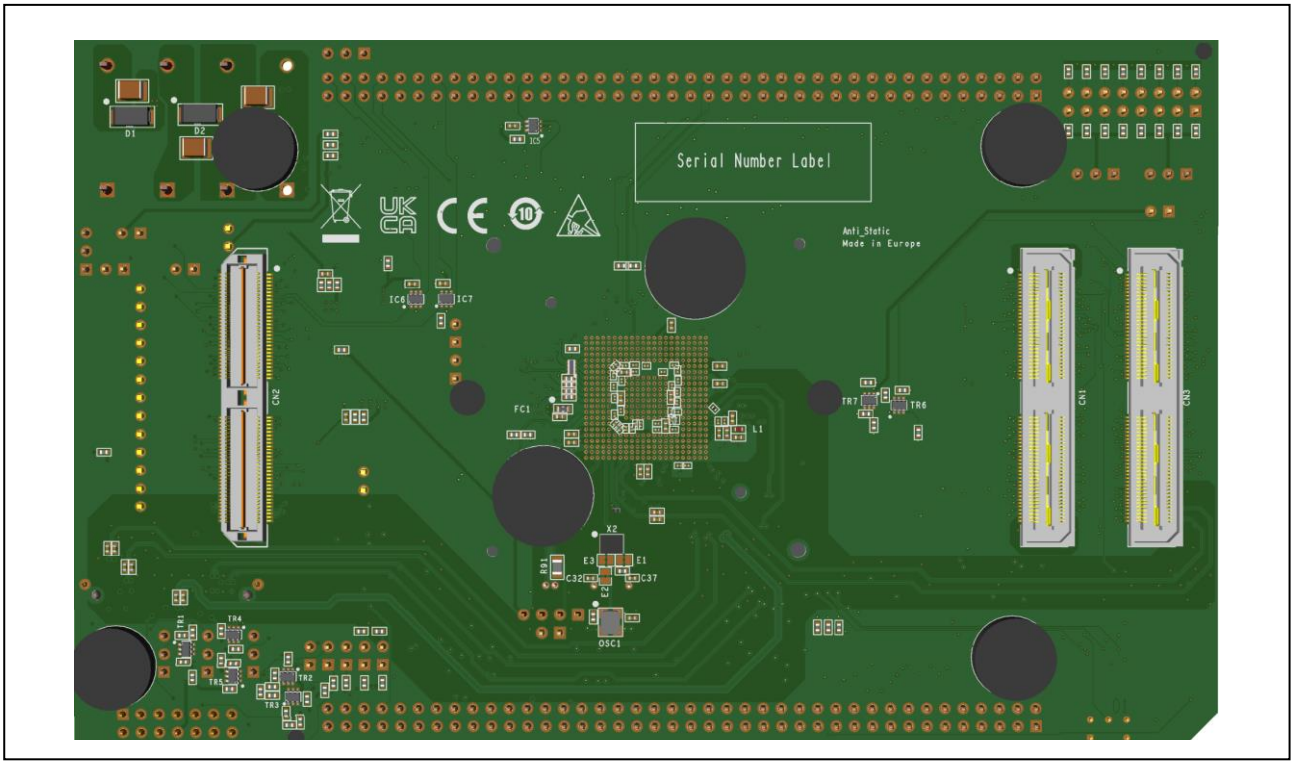


Figure 1.4 Piggyback board bottom view of board version D019726_06_V02

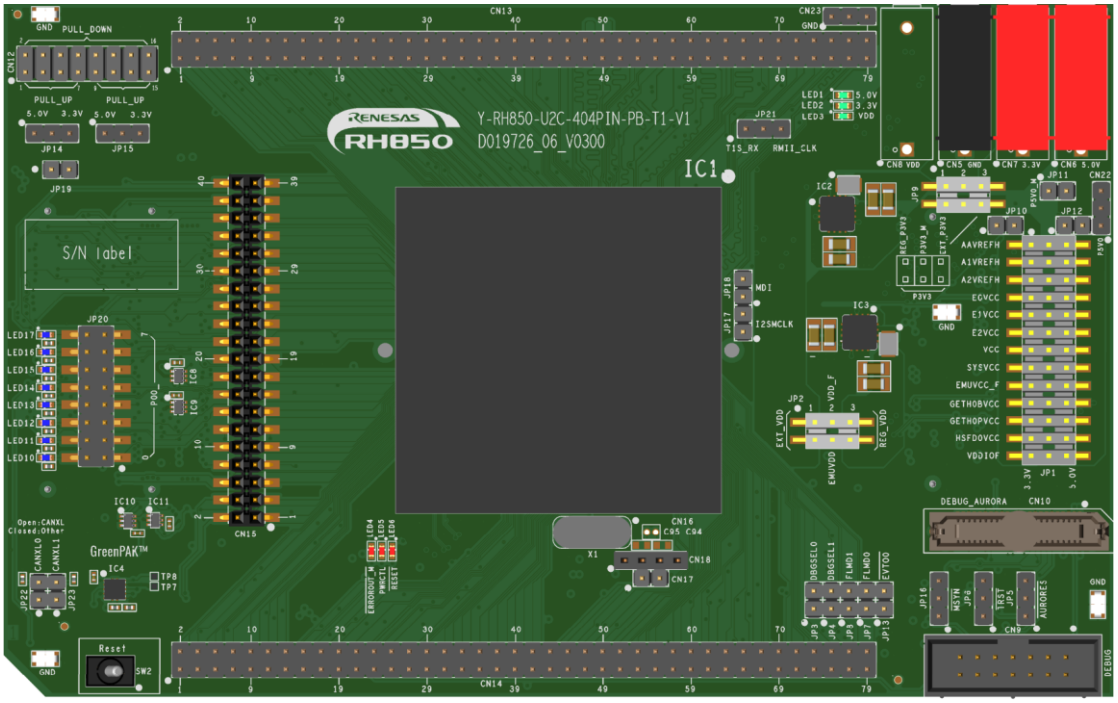


Figure 1.5 Piggyback board top view of board version D019726_06_V03

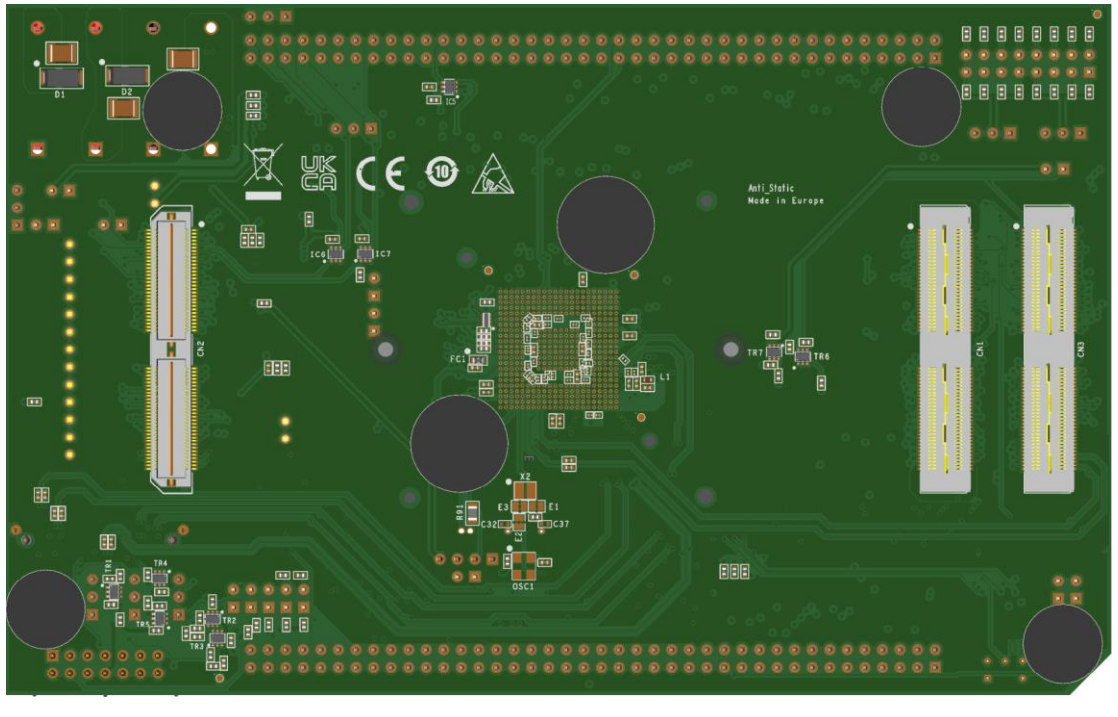


Figure 1.6 Piggyback board bottom view of board version D019726_06_V03

Following figures provide the drawing of top and bottom views of the piggyback board.

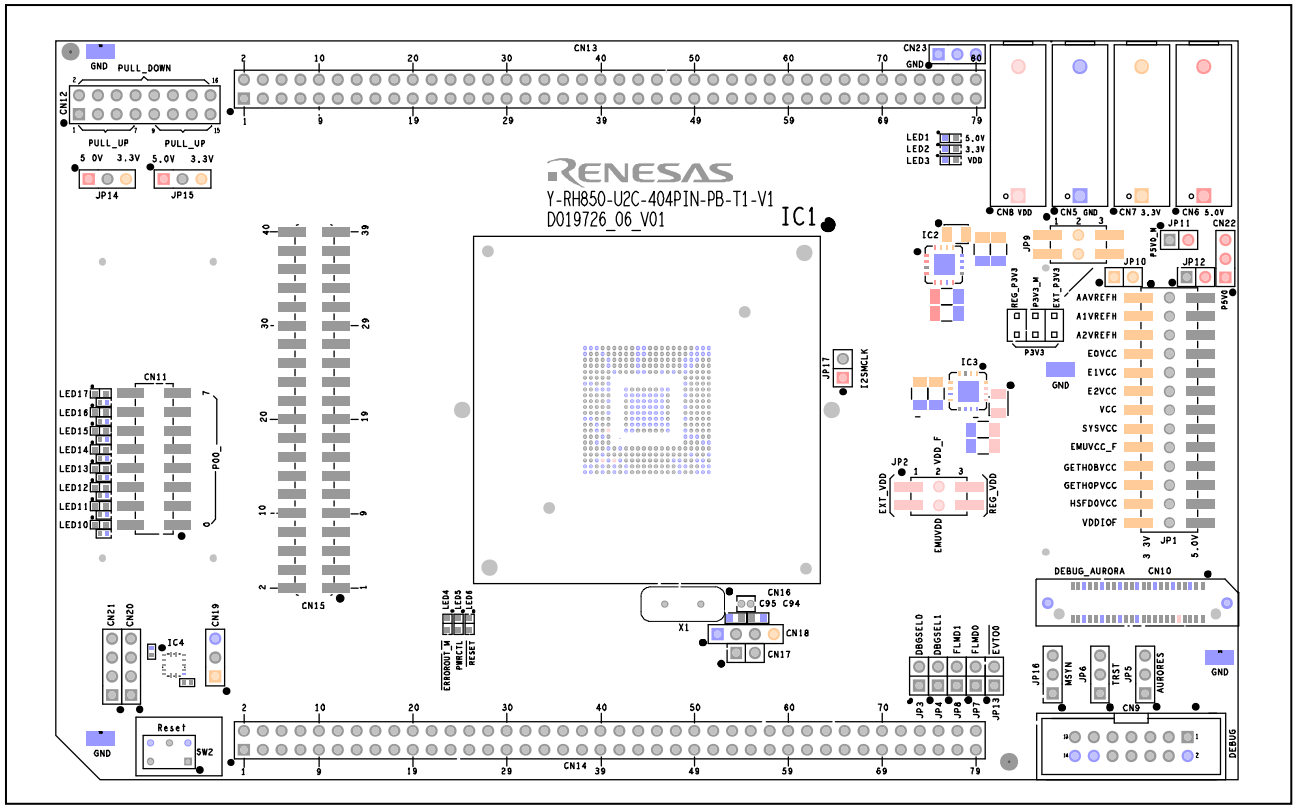


Figure 1.7 Piggyback board top view of board version D019726_06_V01

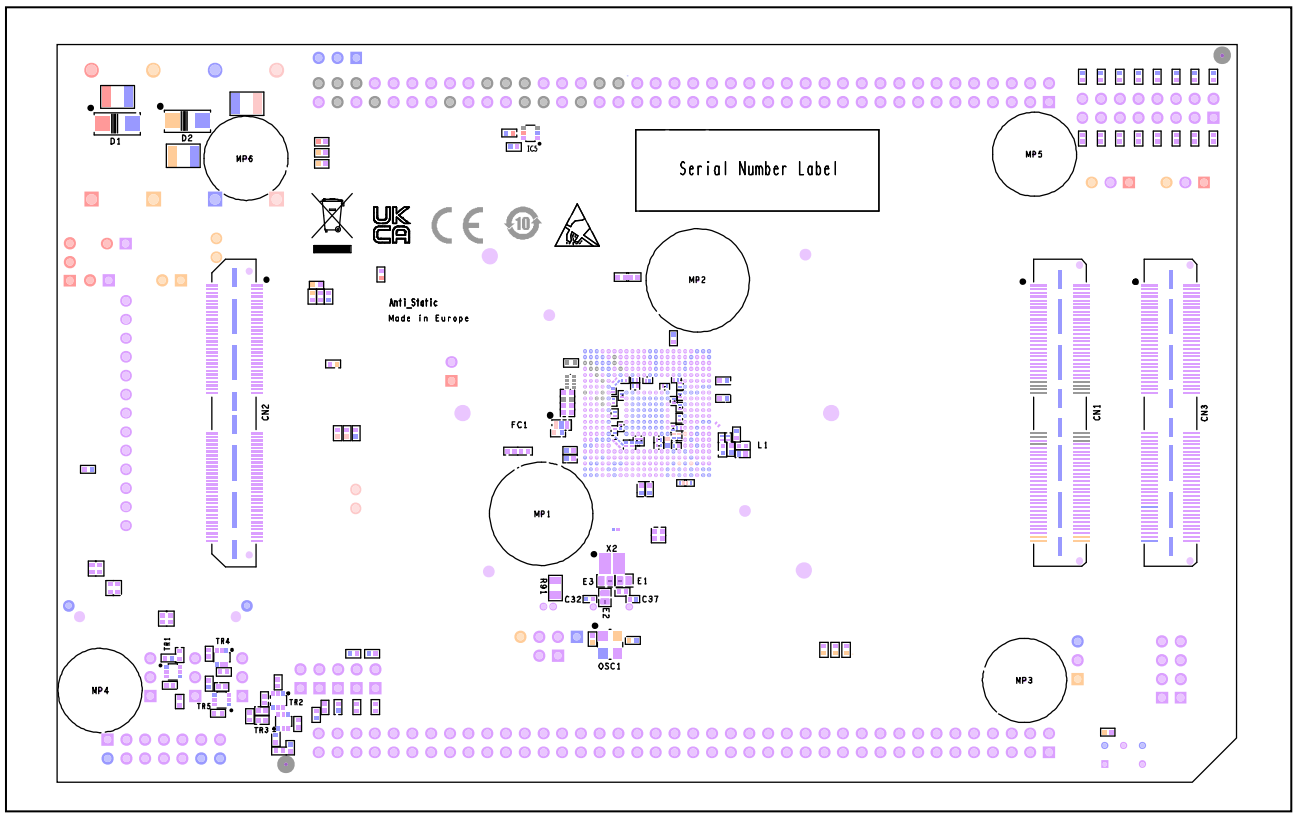


Figure 1.8 Piggyback board bottom view of board version D019726_06_V01

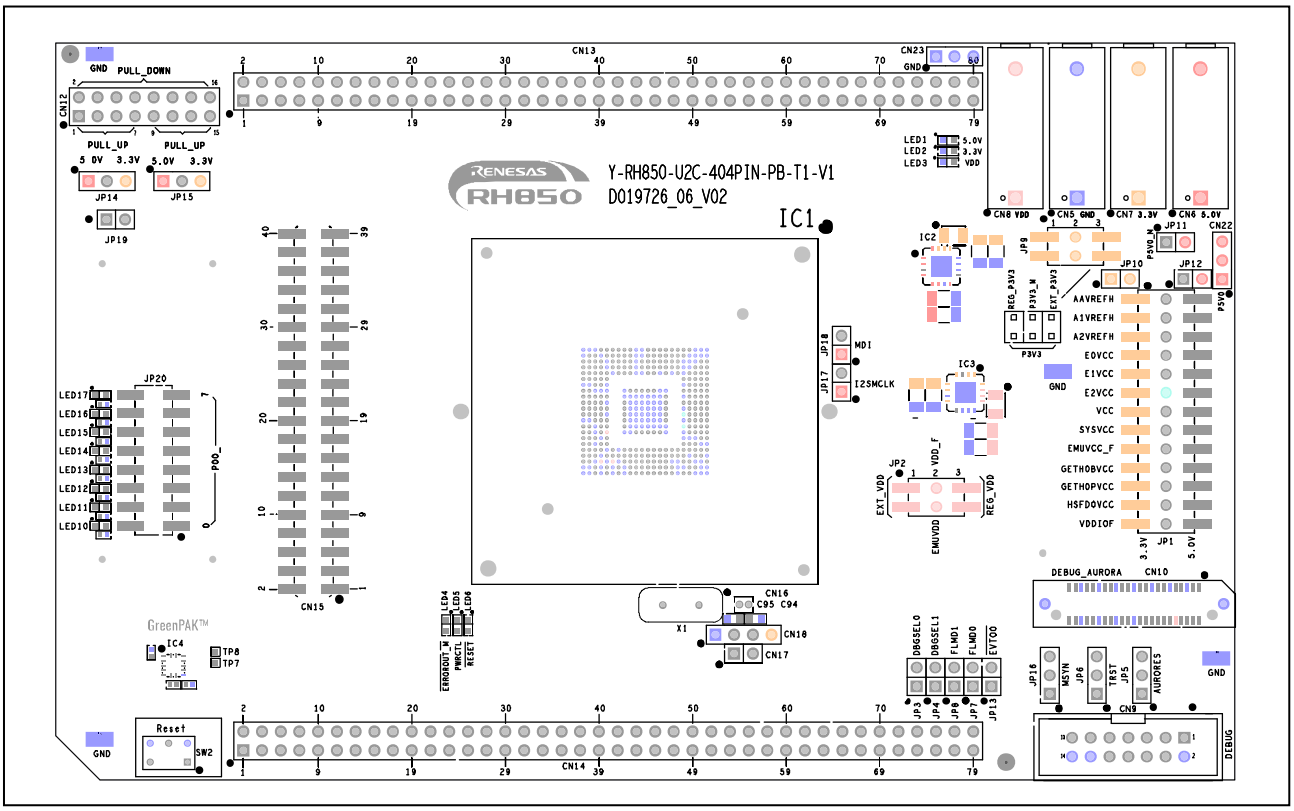


Figure 1.9 Piggyback board top view of board version D019726_06_V02

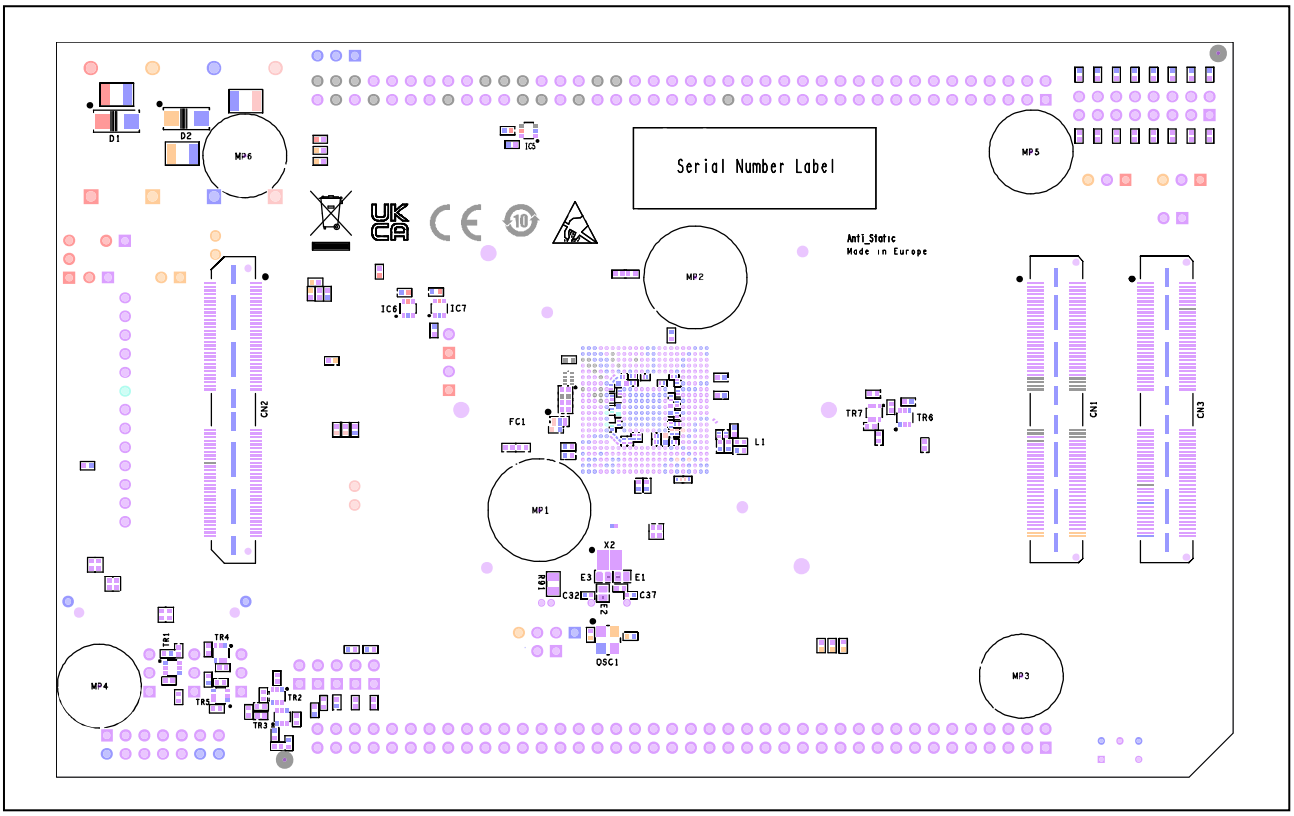


Figure 1.10 Piggyback board bottom view of board version D019726_06_V02

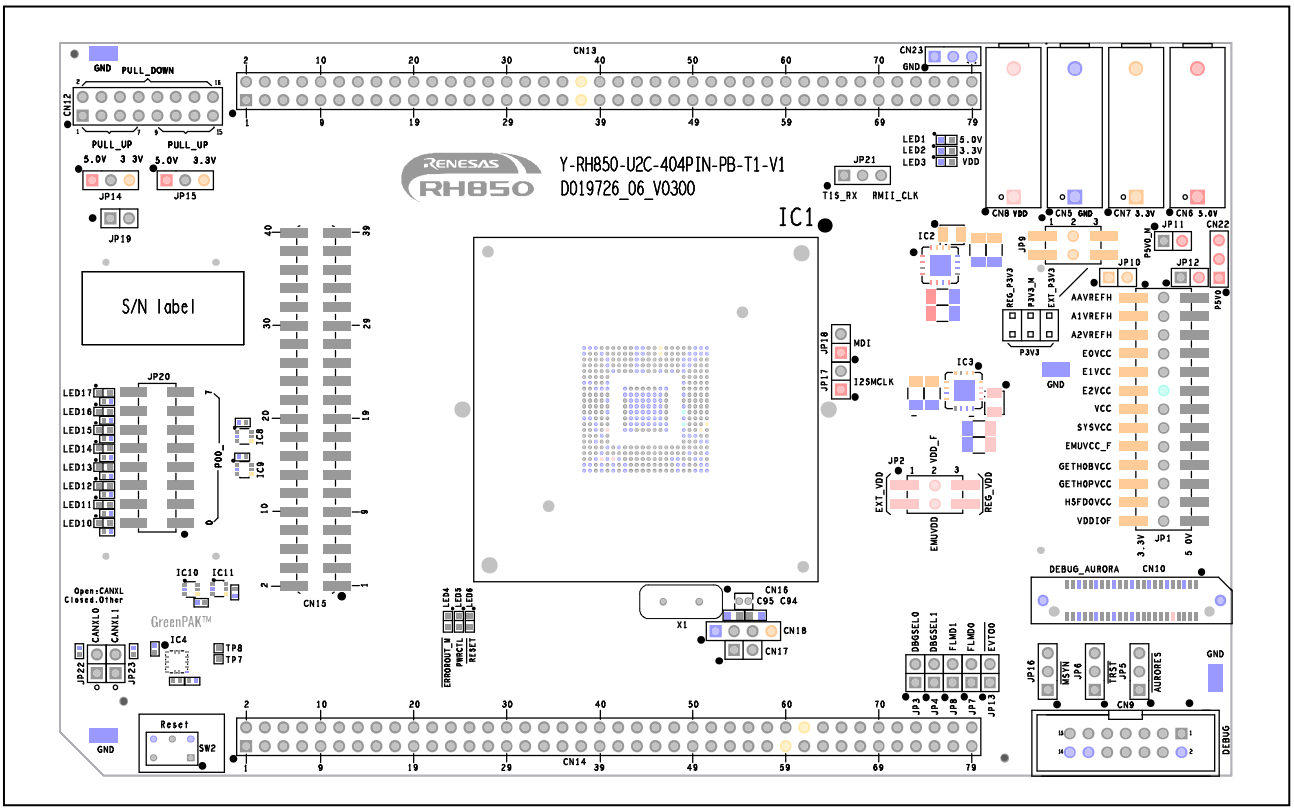


Figure 1.11 Piggyback board top view of board version D019726_06_V03

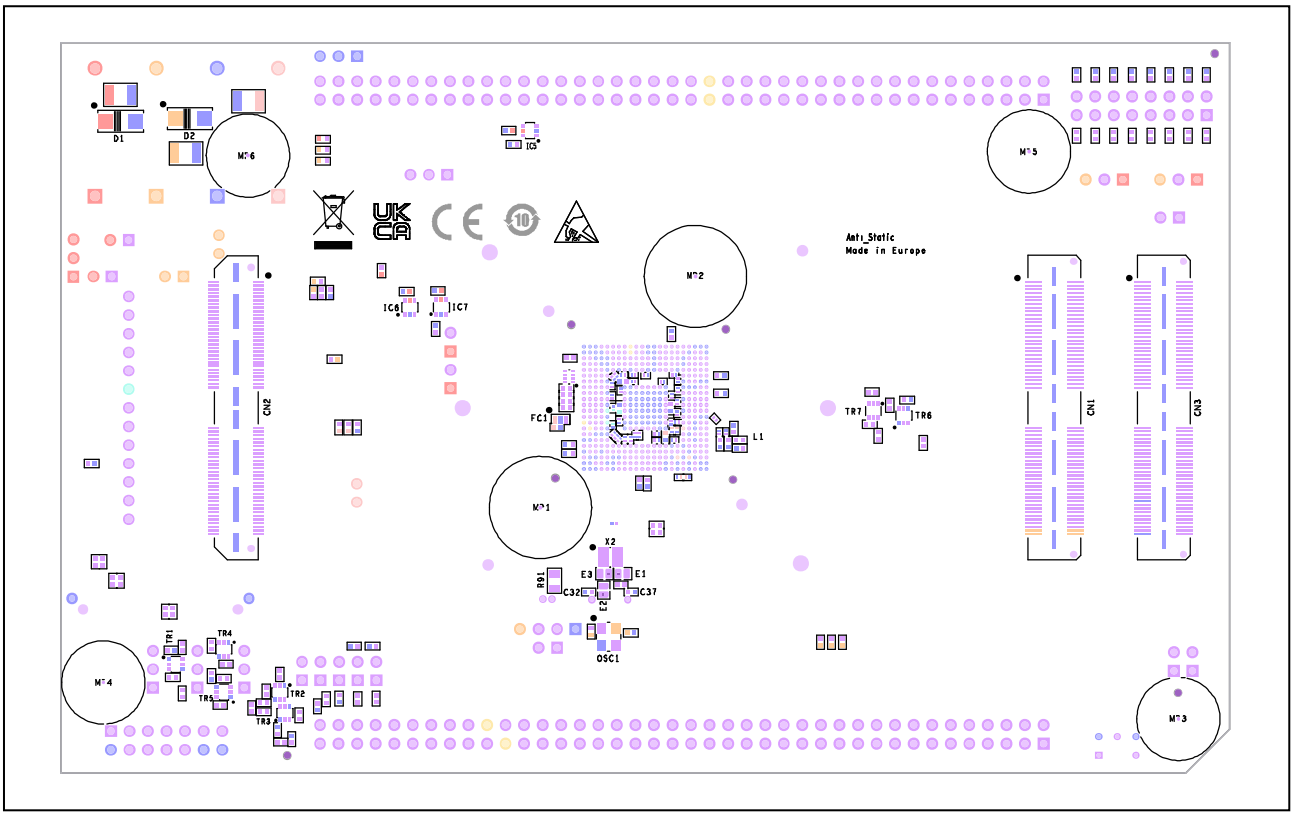


Figure 1.12 Piggyback board bottom view of board version D019726_06_V03

1.6 Mounting of the Device

The board is designed for use with the following devices.

Table 1.4 Type names for suitable devices

	FCC device	Comments
RH850/U2C8-EVA	R7F702Z32AFDBF-C	Evaluation chip for development purpose

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking of the socket.
In below picture the A1 pin of the socket is marked with a circle. Please see the white point in *Figure 1.13 Yamaichi NP351-404-483 socket*.
On the device the index area is available on the corner near the A1 pin.

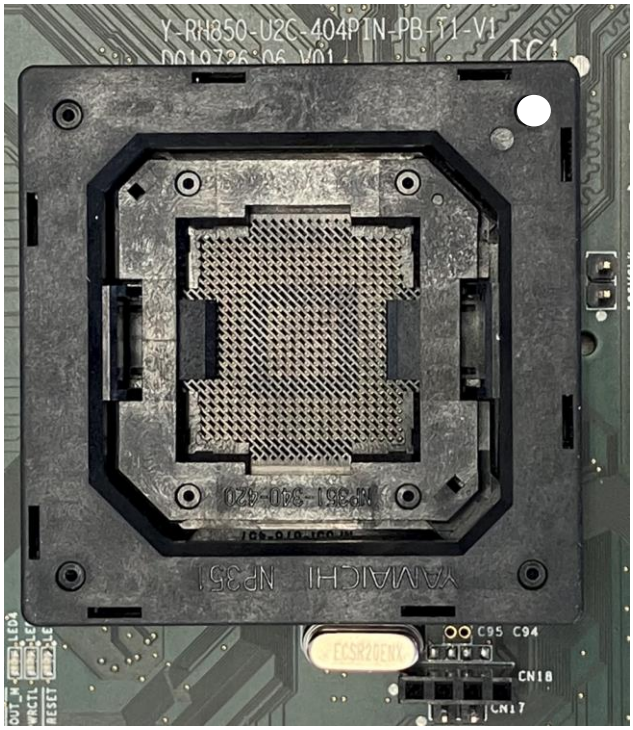


Figure 1.13 Yamaichi NP351-404-483 socket

CAUTION

Be careful with the device placement in the socket to avoid damage to the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figures below.

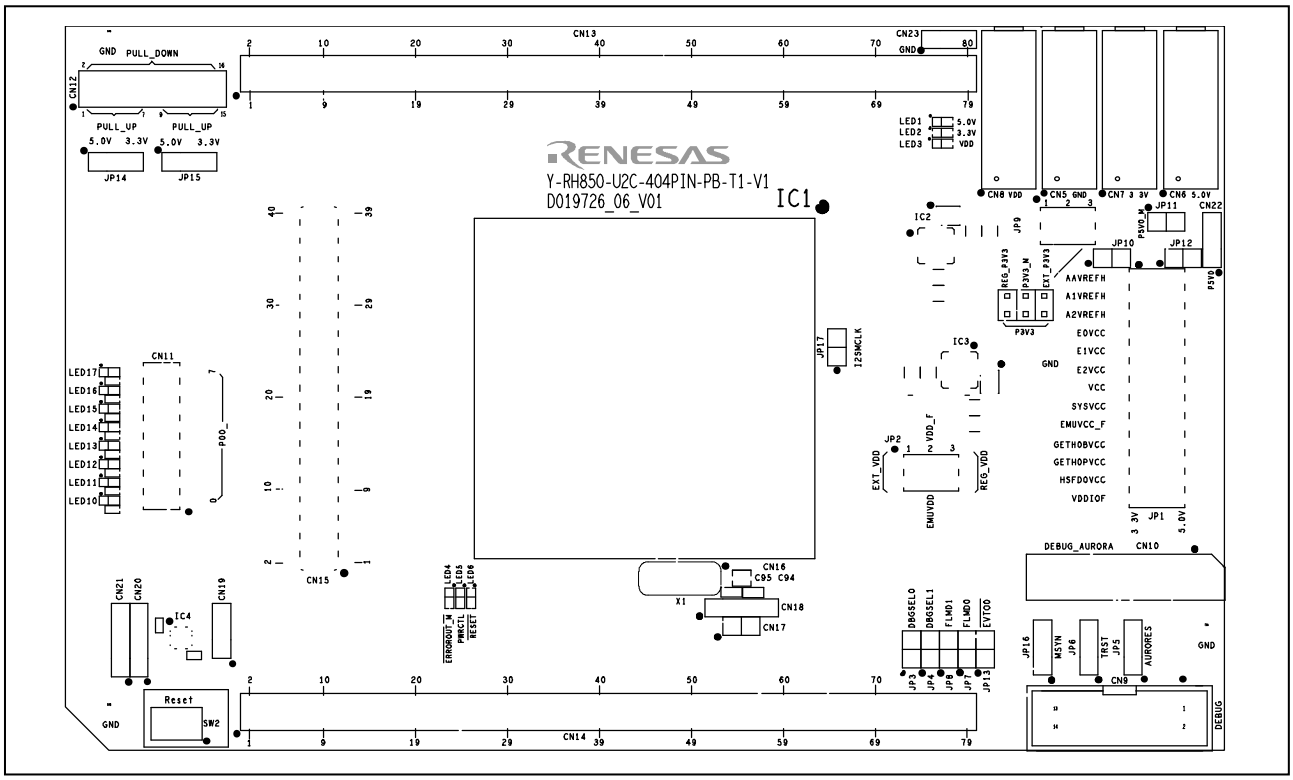


Figure 2.2 Placement of jumpers, connectors and LEDs on top side of board version D019726_06_V01

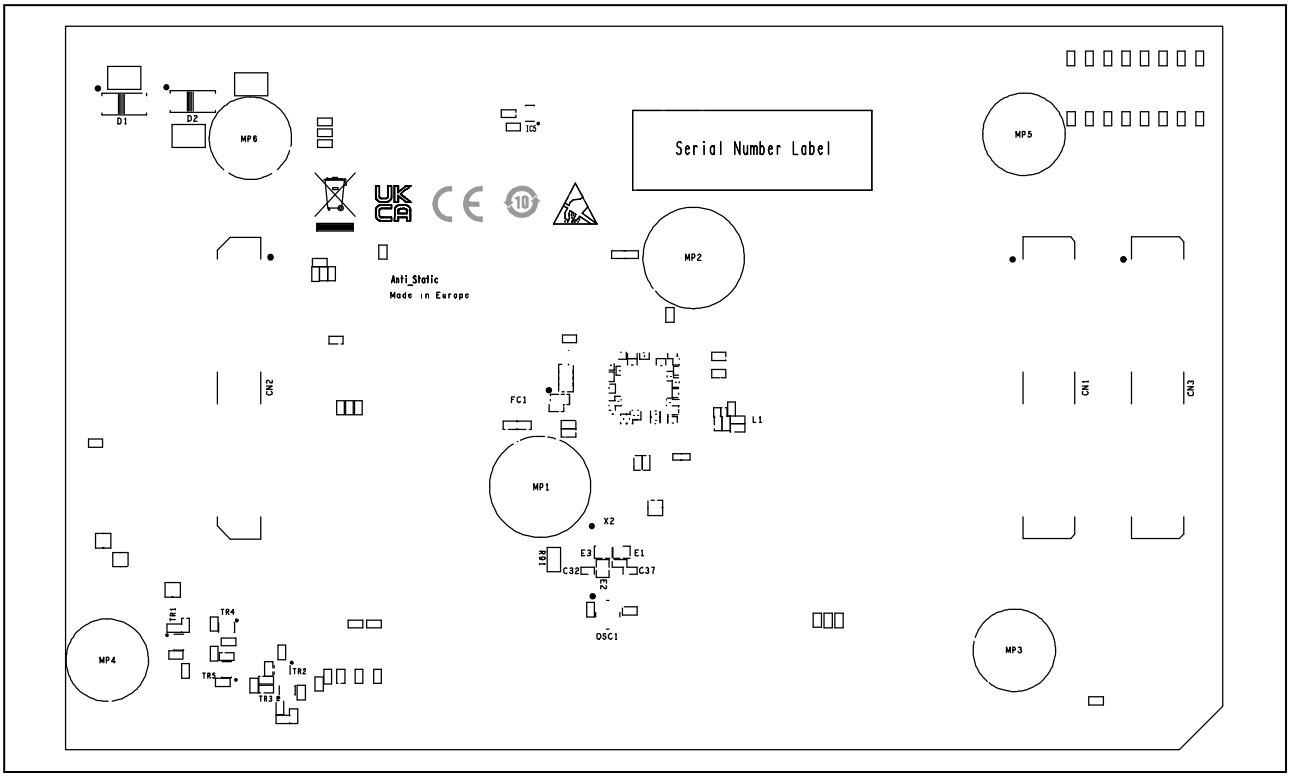


Figure 2.1 Placement of connectors on bottom side of board version D019726_06_V01

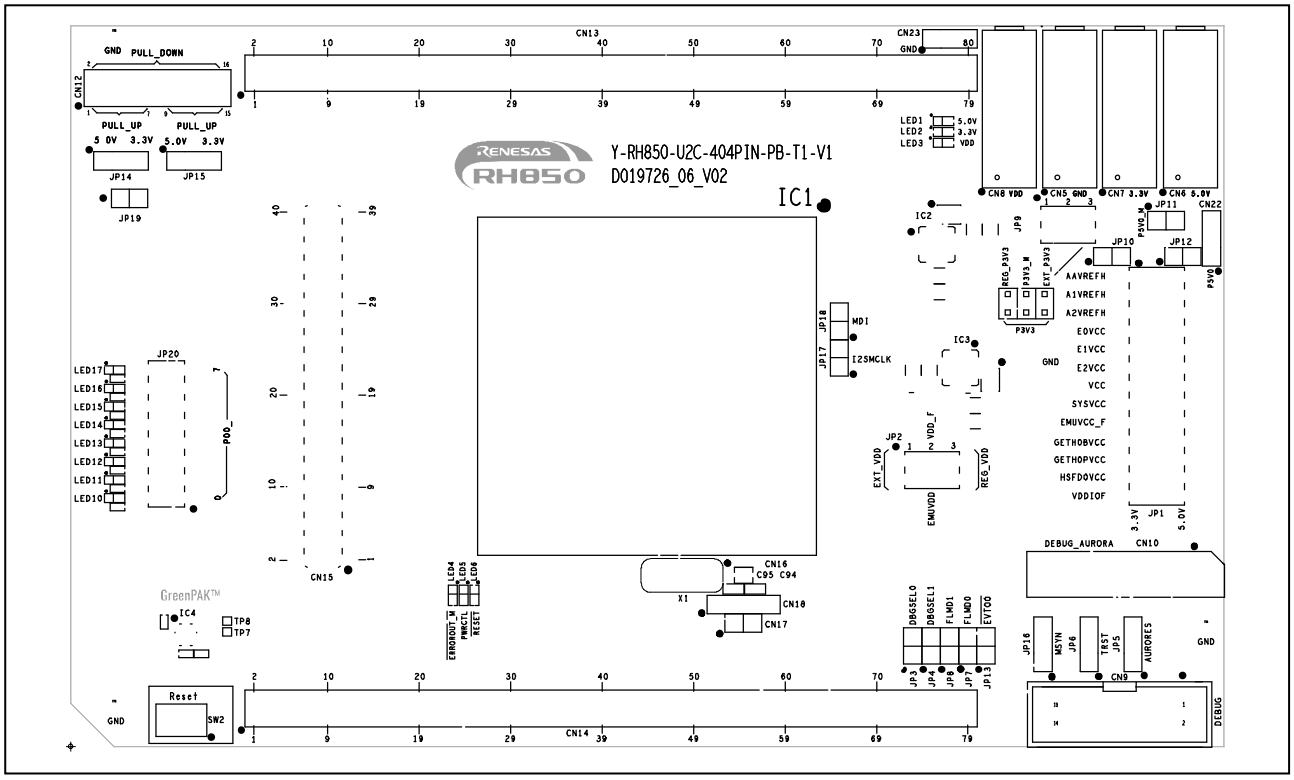


Figure 2.3 Placement of jumpers, connectors and LEDs on top side of board version D019726_06_V02

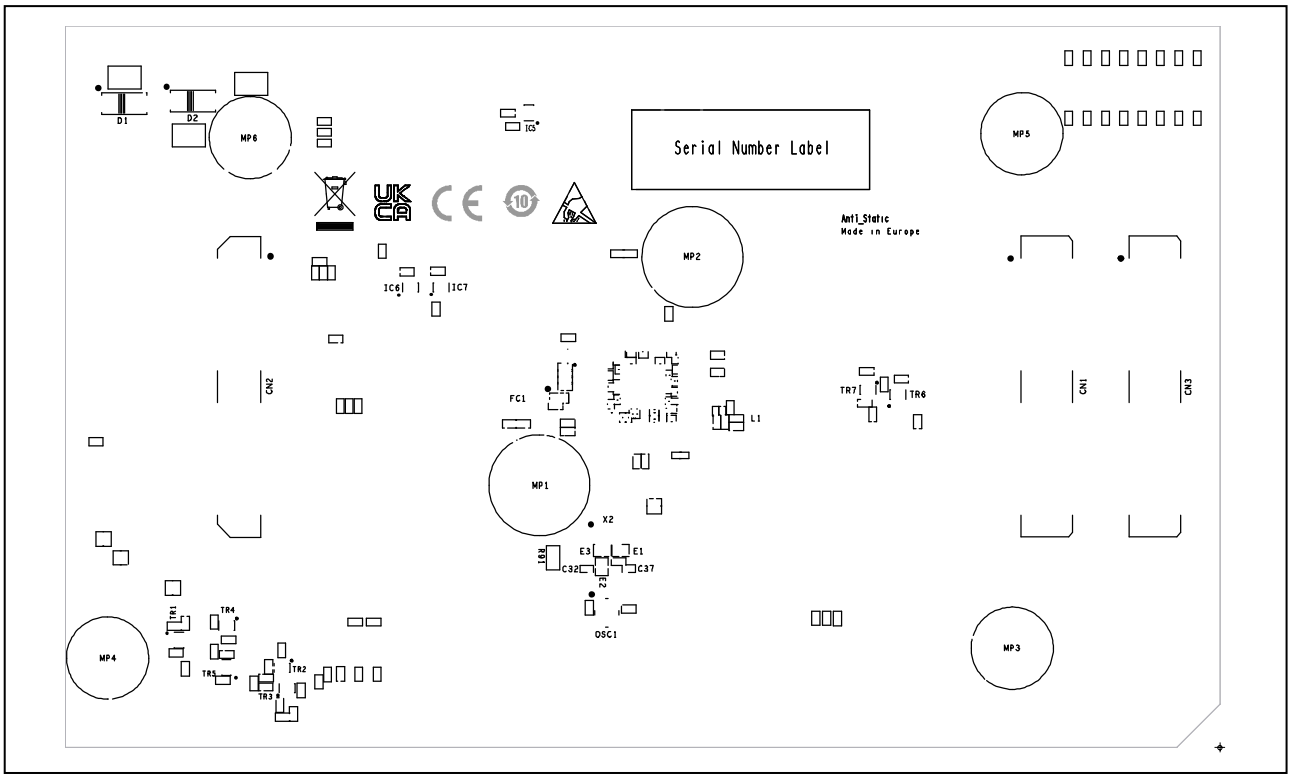


Figure 2.4 Placement of connectors on bottom side of board version D019726_06_V02

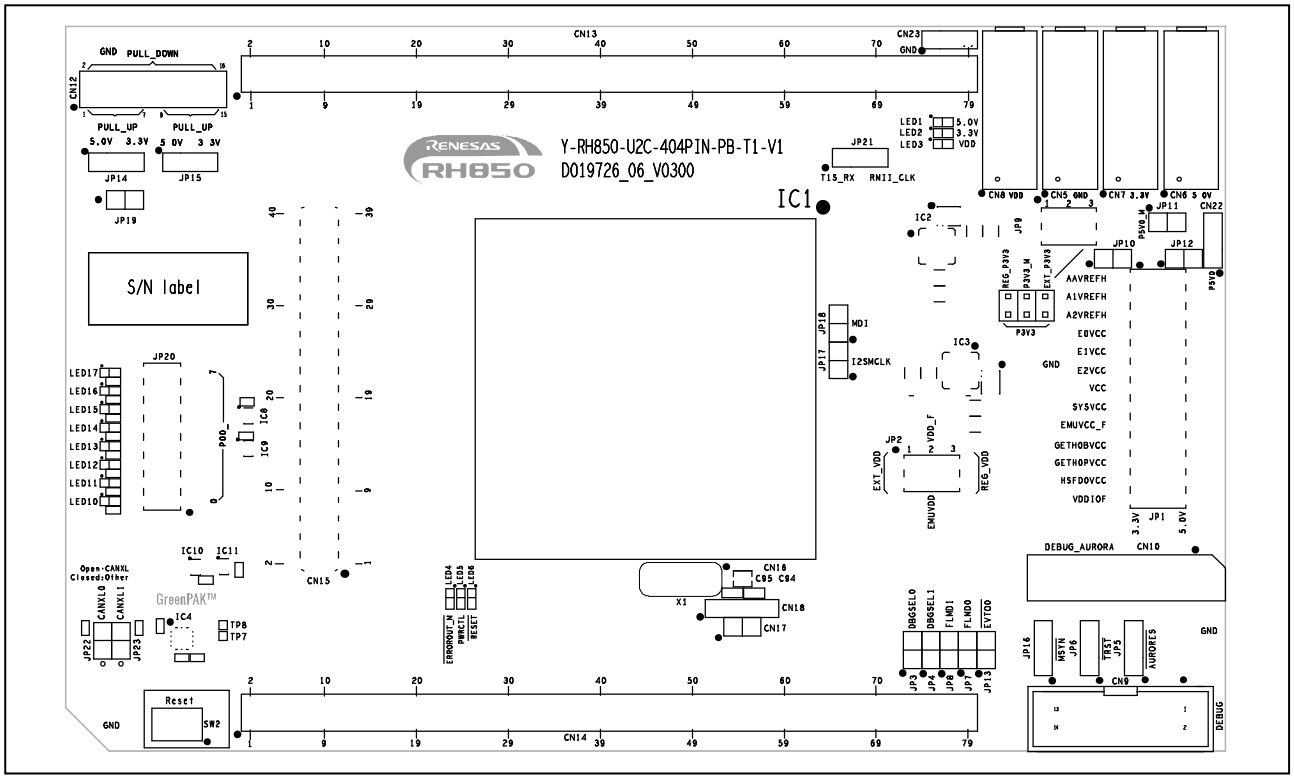


Figure 2.5 Placement of jumpers, connectors and LEDs on top side of board version D019726_06_V03

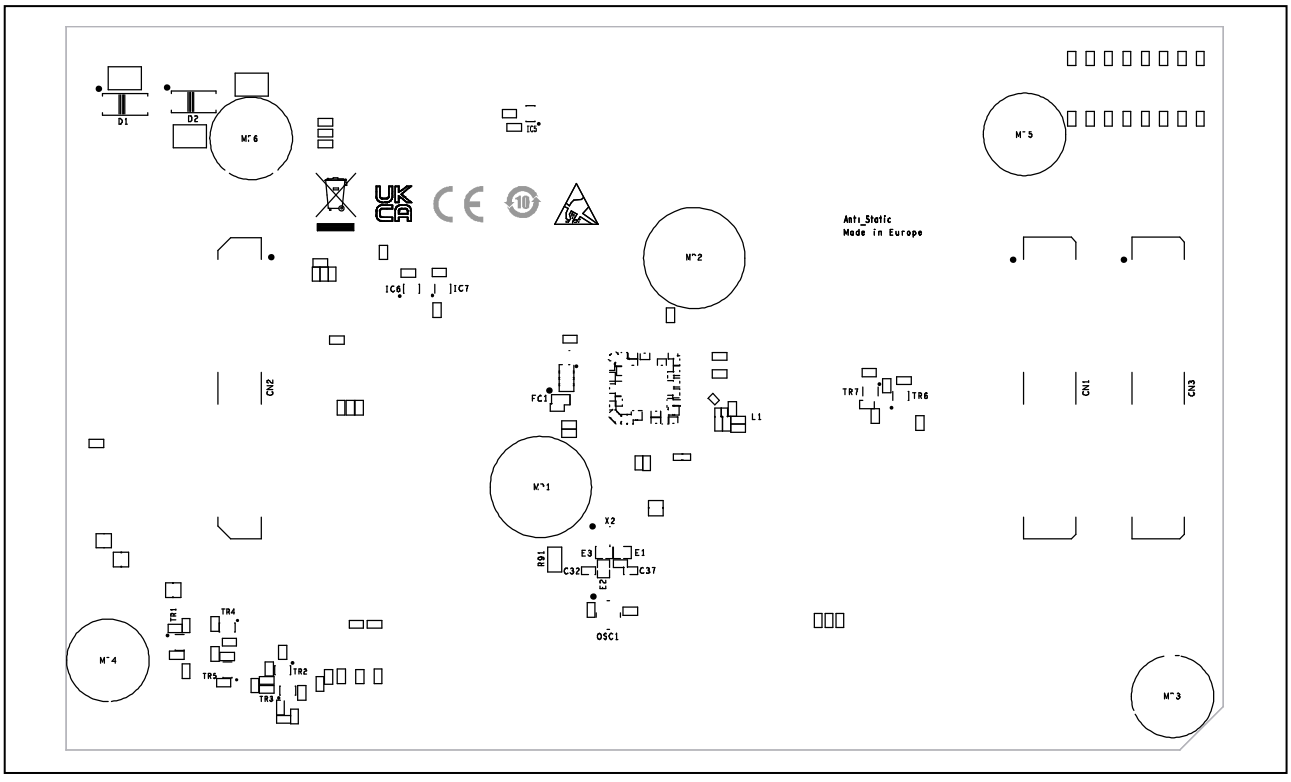


Figure 2.6 Placement of connectors on bottom side of board version D019726_06_V03

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select +3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
JP2	Core voltage selection	refer to *3.3 Device Core Voltage (VDD) Selection*
JP3	Apply “H” level to JP3 for DBGSEL0 signal	
JP4	Apply “H” level to JP4 for DBGSEL1 signal	
JP5	Select signal source for AURORES# input on RH850/U2C ▪ JP5[2-1]: TRST# signal selected by jumper JP6 ▪ JP5[2-3]: AURORES_VCC# signal from Aurora debug I/F connector (pin 8 on connector CN10) or from E2 debug connector (pin 3 on connector CN9).	Refer to *5 Debug and Flash Programming Interfaces*
JP6	Select signal source for TRST# signal ▪ JP6[1-2]: Fix TRST# signal to E0VCC ▪ JP6[2-3]: TRST# signal is TRST_TOOL# signal from Aurora debug I/F connector (pin 12 on connector CN10). From board version D019726_06_V02 onwards TRST_TOOL# is also connected to E2 debug I/F (pin 3 on connector CN9).	
JP7	Change FLMD0 signal to “H”.	refer to *6.1 Operation Mode Selection*
JP8	Change FLMD1 signal to “GND”.	
JP9	Select +3.3 V power supply source ▪ JP9[1-4]: Get +3.3 V from onboard voltage regulator ▪ JP9[2-5]: Get +3.3 V from main board ▪ JP9[3-6]: Get +3.3 V from external +3.3 V supply on CN7	refer to *3.2 Voltage Distribution*
JP10	Current measurement bridge +3.3 V	refer to *3.4 Current Measurement Bridges*
JP11	Enable +5.0 V supply from main board	refer to *3.1 Board Power Connection*
JP12	Current measurement bridge +5.0 V	refer to *3.4 Current Measurement Bridges*
JP13	Debug port connection EVTO0	refer to *5 Debug and Flash Programming Interfaces*
JP14 JP15	Select pull-up voltage for Pull-Up Pull-Down connector CN12 ▪ JP14[1-2]: 5.0 V pull-up on pins 1 / 3 / 5 / 7 ▪ JP14[2-3]: 3.3 V pull-up on pins 1 / 3 / 5 / 7 ▪ JP15[1-2]: 5.0 V pull-up on pins 9 / 11 / 13 / 15 ▪ JP15[2-3]: 3.3 V pull-up on pins 9 / 11 / 13 / 15	refer to *6.9 Pull-Up/Pull-Down Pin Header*
JP16	Select debug signal MSYN# connection	refer to *5 Debug and Flash Programming Interfaces*
JP17	Select Ethernet function to port P20_0 ▪ JP17[OPEN]: P20_0 = ETH0RXD0 ▪ JP17[CLOSED]: P20_0 = I2SMCLK	refer to *6.3 Ethernet / I2S Selection*
JP18	Select Ethernet 1 control ports on connector CN2 (from board version D019726_06_V02 onwards) ▪ JP18[OPEN]: ETH1_MDIO (CN2_99) = P21_0 ETH1_MDC (CN2_100) = P20_11 ▪ JP18[CLOSED]: ETH1_MDIO (CN2_99) = P04_9 ETH1_MDC (CN2_100) = P04_8	refer to *6.4 Ethernet 1 Control Ports MDIO / MDC*

Table 2.1 Jumper overview (cont'd)

Jumper	Function	Remark
JP19	Jumper for board production test	Must be left open
JP20 (CN11)	Enable LED outputs (CN11 for board version D019726_06_V01)	refer to *6.8 Signalling LEDs*
JP21	Select Ethernet function for port P20_3 ▪ JP21[1-2]: T1S_RX ▪ JP21[2-3]: RMII_TXCLK	refer to *6.5 Ethernet Control Port P20_3*
JP22	Select CAN XL function for port P17_2 and P17_3 (from board version D019726_06_V03 onwards) ▪ JP22[OPEN]: P17_2 = CANXL0RX; P17_3 = CANXL0TX ▪ JP22[CLOSED]: P17_2 and P17_3 are connected to other interfaces	refer to *6.6 CAN XL Ports*
JP23	Select CAN XL function for port P24_7 and P24_8 (from board version D019726_06_V03 onwards) ▪ JP23[OPEN]: P24_7 = CANXL1TX; P24_8 = CANXL1RX ▪ JP23[CLOSED]: P24_7 and P24_8 are connected to other interfaces	

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview

Connector	Function	Remark
CN1	Main board connectors	refer to *7.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN5	GND external power supply	refer to *3.1 Board Power Connection*
CN6	+5.0 V external power supply	
CN7	+3.3 V external power supply	
CN8	+1.09 V external power supply	
CN9	E2 emulator debug connector	refer to *5 Debug and Flash Programming Interfaces*
CN10	Aurora I/F debug connector	
CN11	Signaling LEDs pin header	only for board version D019726_06_V01, from board version D019726_06_V02 onwards named JP20 refer to *6.8 Signalling LEDs*
CN12	Pull up / pull down configuration	refer to *6.9 Pull-Up/Pull-Down Pin Header*
CN13	Device ports connector	refer to *7.4 Device Ports Connectors CN13, CN14 and CN15*
CN14		
CN15		
CN16	Socket for sub-oscillator	refer to *4.4 Sub Oscillator*
CN17	IP0_0 and IP0_1 connector	
CN18	IP0_0 and IP0_1 fixed inputs	

Table 2.2 Connector overview (cont'd)

Connector	Function	Remark
CN19	Connectors for external Reset signal module (only board version D019726_06_V01)	refer to *6.2 System* State and RESET
CN20		
CN21		
CN22	+5.0 V connector	refer to *3.1 Board Power Connection*
CN23	GND connector	

2.3 Switch Overview

The following table provides an overview of all switches.

Table 2.3 Switches overview

Connector	Function	Remark
SW2	RESET#	refer to *6.2 System* State and RESET

2.4 LED Overview

The following table provides an overview of all LEDs.

Table 2.4 LED overview

LED	Function	Color	Remark
LED1	5.0 V power supply P5V0	green	refer to *3.5 Power Supply LEDs*
LED2	3.3 V power supply P3V3	green	
LED3	LED_PG_VDD signal	green	
LED4	Device ERROROUT_M# signal	red	refer to *6.2 System* State and RESET
LED5	LED_PWRCTL signal	red	
LED6	LED_RESET# signal	red	
LED10	Signaling LED	blue	refer to *6.8 Signalling LEDs*
LED11	Signaling LED		
LED12	Signaling LED		
LED13	Signaling LED		
LED14	Signaling LED		
LED15	Signaling LED		
LED16	Signaling LED		
LED17	Signaling LED		

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage
- 1.09 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

Four 4 mm ‘banana-type’ connectors are used to connect external power supplies:

- black connector CN5 for GND (VSS)
- red connector CN6 for 5.0 V (P5V0)
- red connector CN7 for 3.3 V (Ext_P3V3)
- red connector CN8 for 1.09 V (Ext_P1V09)
  Connector CN8 is not assembled at delivery of the board, but separately supplied with the board package.
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

In case the piggyback board is mounted on a main board, all voltages except for 1.09 V (VDD) can be supplied by the main board. The jumpers JP11 (5.0 V) and JP9[2-5] (3.3 V) are used to enable power supply from main board.

The piggyback board has 2 pin headers with 3 pins each. The pin headers are named CN22 and CN23. They can be used for example as power supply for some additional hardware.

- CN22: connected to the 5.0 V supply (P5V0) on the piggyback board.
- CN23: GND connection

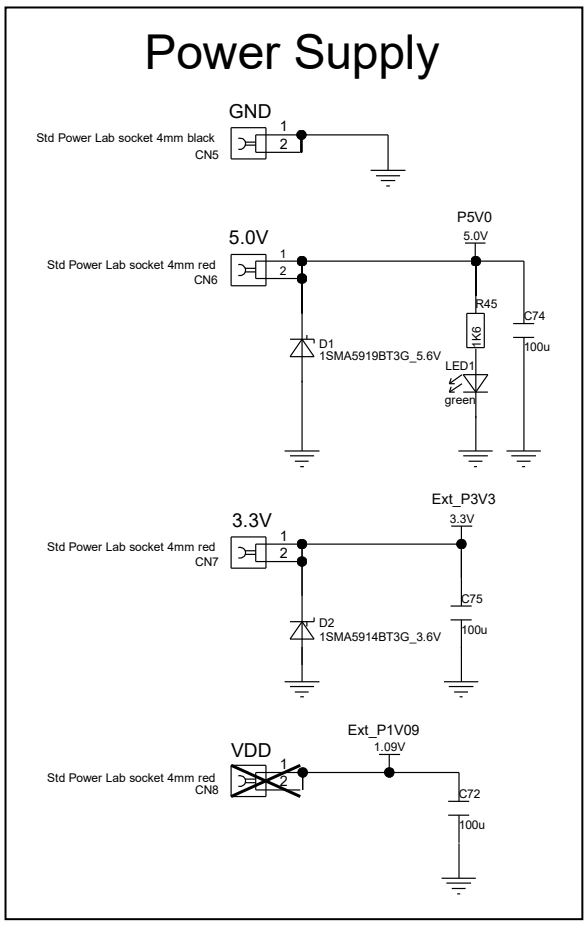


Figure 3.1 Power supply connectors

CAUTION

Do not supply the 5 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board if power supply from the main board is enabled.

Connecting external 1.09 V via CN8 (and GND via CN5) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

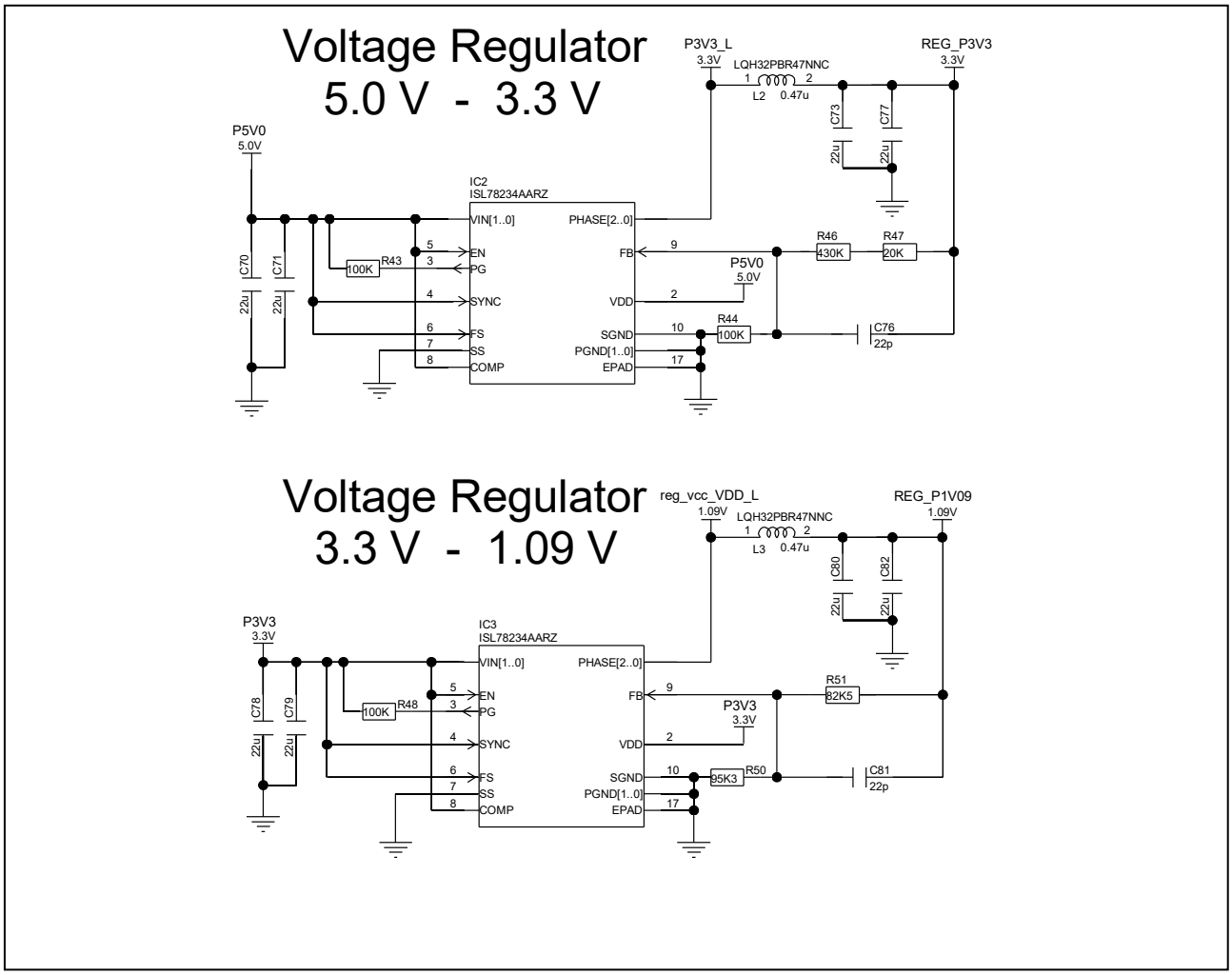


Figure 3.2 Voltage regulator circuit

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	Power supply for I/O ports
EMUVDD	1.09 V	Power supply for debug circuits, only available on FCC devices
EMUVCC_F	3.3 V	
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
AAVREFH, A1VREFH, A2VREFH	3.3 V, 5 V	A/D converter's power supplies and reference voltages
VDD_F	1.09 V	Core supply voltage Refer to *3.3 Device Core Voltage (VDD) Selection*
GETH0BVCC	3.3 V	Power supply for Ethernet
GETH0PVCC	3.3 V, 5 V	
HSFD0VCC	3.3 V, 5 V	Power supply for RHSIF debug interface

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V (P3V3) can be selected from external power supply (EXT_P3V3, CN7), main board power supply (P3V3_M) or from the onboard voltage regulator (REG_P3V3) using jumper JP9:

- JP9 [1-4]: 3.3 V supply P3V3 comes from the onboard voltage regulator REG_P3V3.
- JP9 [2-5]: 3.3 V supply P3V3 comes from the main board power supply P3V3_M.
- JP9 [3-6]: 3.3 V supply P3V3 comes from the external power supply CN7 EXT_P3V3.

The supply for 5.0 V (P5V0) can be selected from external power supply (P5V0, CN6) or from main board power supply (P5V0_M) using jumper JP11:

- JP11 [open]: 5.0 V supply P5V0 comes from external power supply CN6.
- JP11 [closed]: 5.0 V supply comes from main board supply P5V0_M

Table 3.2 Voltage Selection shows which jumpers to set to select the different device supply voltages, and *Figure 3.3 Voltage distribution* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
AAVREFH	JP1 [1-2]	JP1 [2-3]
A1VREFH	JP1 [4-5]	JP1 [5-6]
A2VREFH	JP1 [7-8]	JP1 [8-9]
E0VCC	JP1 [10-11]	JP1 [11-12]
E1VCC	JP1 [13-14]	JP1 [14-15]
E2VCC	JP1 [16-17]	JP1 [17-18]
VCC	JP1 [19-20]	JP1 [20-21]
SYSVCC	JP1 [22-23]	JP1 [23-24]
EMUVCC_F	JP1 [25-26]	---
GETH0BVCC	JP1 [28-29]	---
GETH0PVCC	JP1 [31-32]	JP1 [32-33]
HSFD0VCC	JP1 [34-35]	JP1 [35-36]
VDDIOF	JP1 [37-38]	JP1 [38-39]

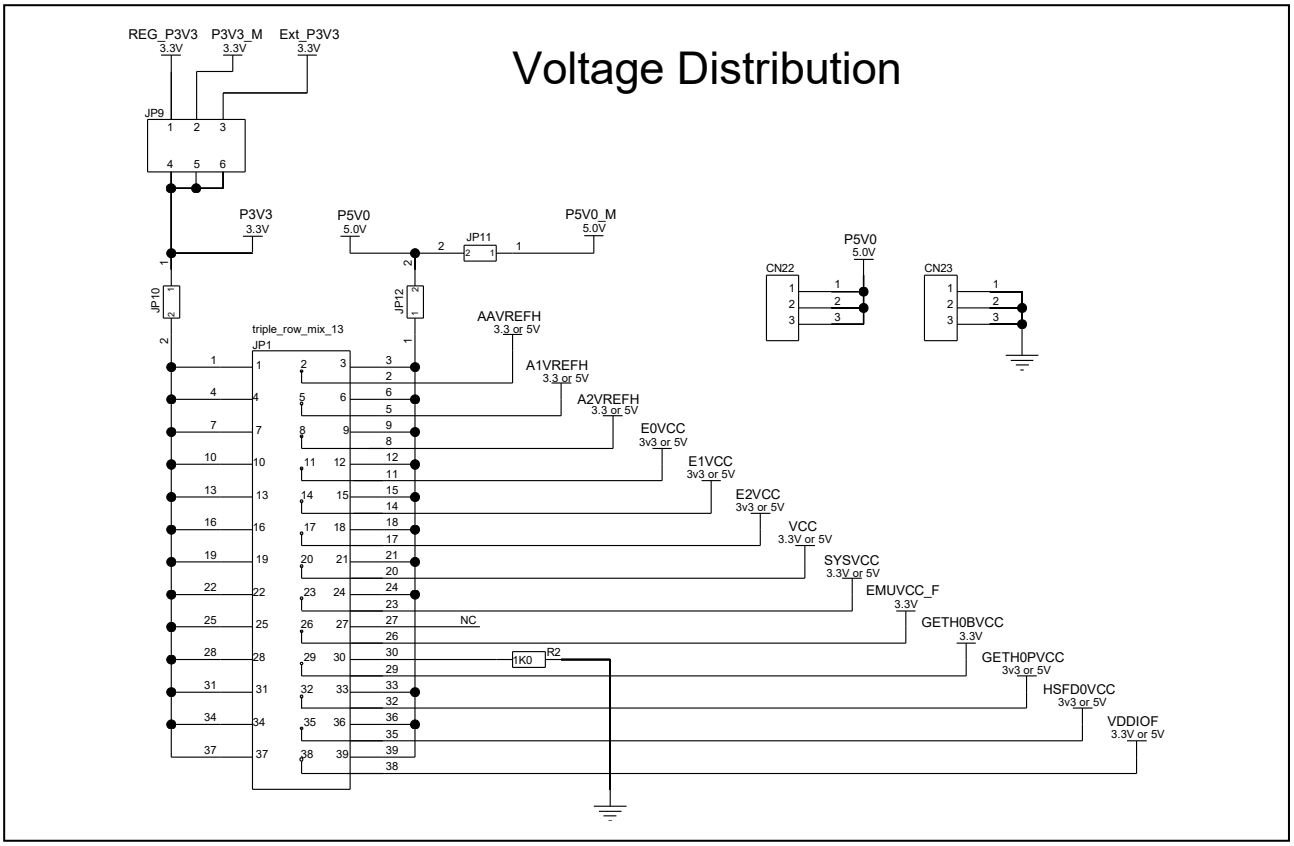


Figure 3.3 Voltage distribution

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.09 V) can be

- supplied from external via CN8 (voltage EXT_P1V09)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage REG_P1V09)

VDD source is selected by jumpers in JP2:

- JP2[1-2]: VDD_F = Ext_P1V09
- JP2[2-3]: VDD_F = REG_P1V09
- JP2[4-5]: EMUVDD = Ext_P1V09
- JP2[5-6]: EMUVDD = REG_P1V09

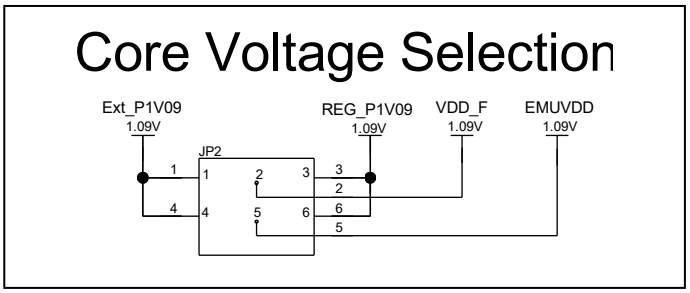


Figure 3.4 Device core voltage (VDD) selection

3.4 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP10 and JP12 with a current meter.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.3 Voltage distribution*.

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED1 for 5.0 V power rail P5V0
- LED2 for 3.3 V power rail P3V3
- LED3 for 1.09 V device core voltage VDD

4. Clock Supply

The device's operation clock can be generated by

- the on-chip main oscillator circuit in combination with an external resonator, connected to the X1, X2 terminals of RH850/U2C.
- an external oscillator circuit where the clock is fed into the X1 terminal.

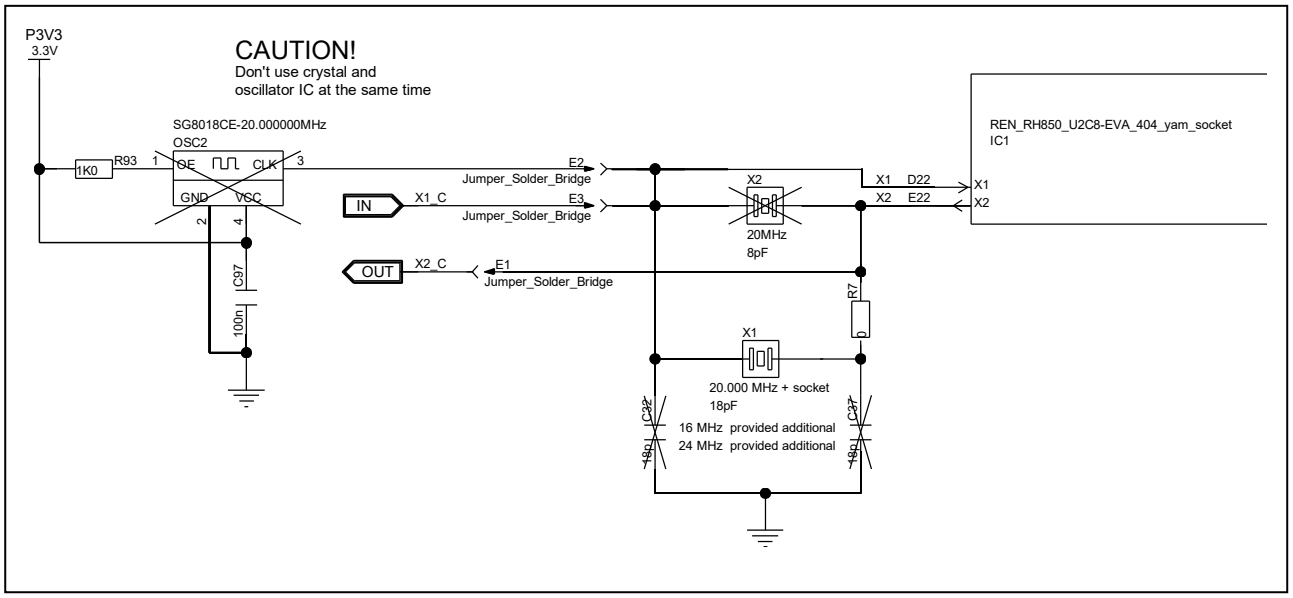


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides socket (X1) for a resonator.

Resonators for various main oscillator frequencies (8 MHz, 16 MHz, 20 MHz, 24 MHz) are included in the board package.

The 20MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*

CAUTION

Only one oscillator, either X1, X1_C, X2 or OSC1, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via solder bridge E2.

For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 Device Pins X1 and X2 on Connector CN14

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN14 via 0 Ω resistors:

- Device pin X1: Connect to pin 41 of CN14 via solder bridge E3 to supply an external clock to the device.
- Device pin X2: Connect to pin 42 of CN14 via solder bridge E1 for measurement purposes of the clock.

4.4 Sub Oscillator

The pins IP0_0 and IP0_1 can also be used as oscillator pins XT1 and XT2 to connect a real-time clock oscillator.

If no oscillator is connected the pins IP0_0 and IP0_1 can be used as input ports.

If an oscillator is connected this oscillator is started by programming the SOSCE (Sub OSC Enable) register.

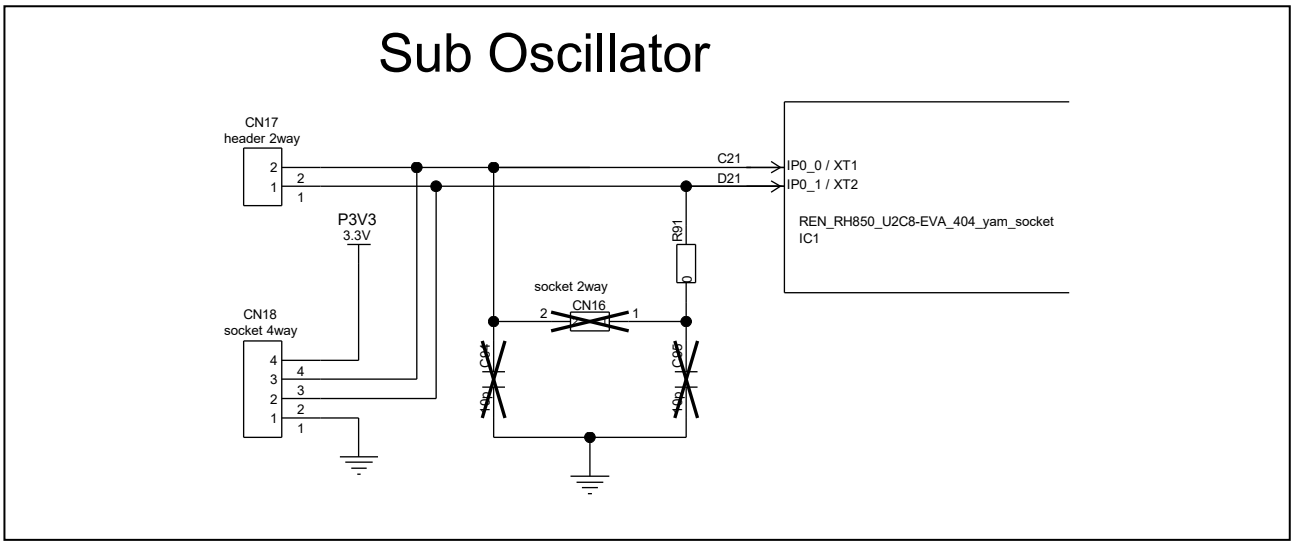


Figure 4.2 Sub Oscillator connnection

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to CN9 or CN10 connector.

The Renesas standard emulator for RH850/U2C is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

CN9 is the debug connector for Renesas E2 emulator.

CN10 is a connector for emulators that support AURORA standard. This is for example the Renesas IE850A emulator.

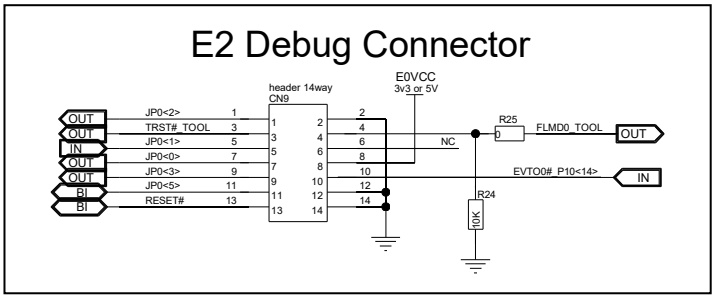


Figure 5.1 E2 debug connector CN9

Refer to *7.3 Debug Connector CN10* for details about the CN10 pin assignment and *7.2 Debug Connector CN9* for details about the CN9 pin assignment.

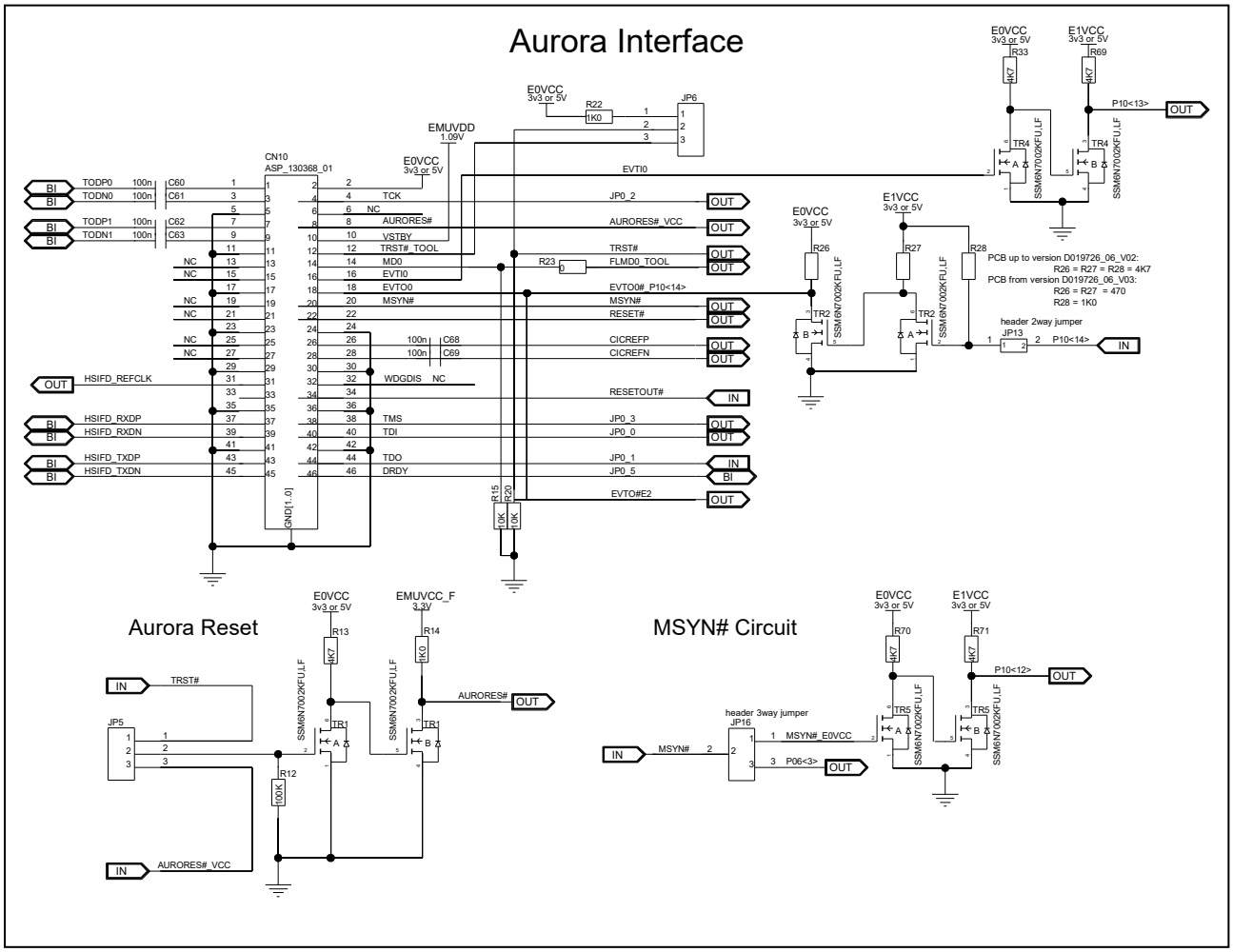


Figure 5.2 Aurora debug interface

RH850/U2C event trigger input and output to synchronize with the emulator. The event trigger output (EVTO0#) is shared with port P10_14, the event trigger input (EVTI0) is shared with port P10_13.

The event trigger input is always connected to RH850/U2C.

The event trigger output is connected to RH850/U2C by closing jumper JP13.

On board version D019726_06_V03 the resistors R26, R27 and R28 in the EVTO0# circuit have been modified.

Board version D019726_06_V01 and D019726_06_V02: R26 = R27 = R28 = 4.7 kOhm

Board version D019726_06_V03: R26 = R27 = 470 Ohm; R28 = 1.0 kOhm

5.1 Debug Formats

RH850/U2C8-EVA supports 3 different debugging formats: JTAG, LPD4 and RHSIFD.

JTAG and LPD4 use the same pins. The used format is selected using jumpers JP3 (signal DBGSEL0) and JP4 (signal DBGSEL1).

RHSIFD uses a separate set of pins and is always active when debug mode is selected.

Jumper JP4 activates the debug mode.

Jumper JP3 selects JTAG or LPD4 mode.

Table 5.1 Debug format selection jumpers

Debug Format	Jumper JP3	Jumper JP4
JTAG	Open	Closed
LPD4	Closed	Closed
RHSIFD	Open or closed	Closed

5.2 Connection of Emulators Supporting 34-pin Connector to Aurora Connector

Some emulators (e.g. Renesas IE850A) use a 34-pin connector for the target connection including trace function.

To be able to use such an emulator it is possible to use the adapter RTE0T0850AKCT00000J on the 46-pin AURORA connector.

Figure 5.3 shows the picture of this adapter.

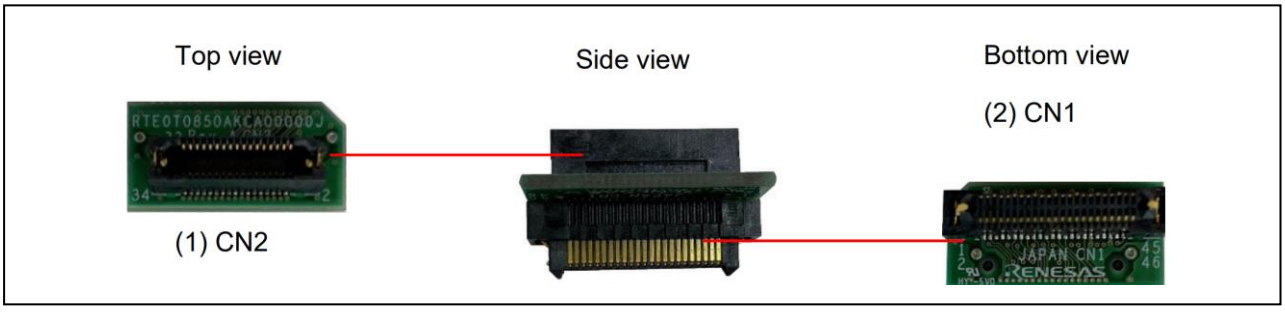


Figure 5.3 34-pin to 46-pin Adapter RTE0T0850AKCT00000J

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers for selection of the device operation mode.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP7	FLMD0 pin level ▪ JP7[CLOSED]: FLMD0 = H level ▪ JP7[OPEN]: FLMD0 • controlled by debugger or programming tool if a tool is connected via CN9 or CN10 • GND, if no tool connected
JP8	FLMD1 pin level ▪ JP8[CLOSED]: FLMD1 = GND • JP8 must be closed if Serial Programming Mode is used by a debugger flash programming tool, that is connected to the board. ▪ JP8[OPEN]: FLMD1 open • Port function of P06_7 can be used.

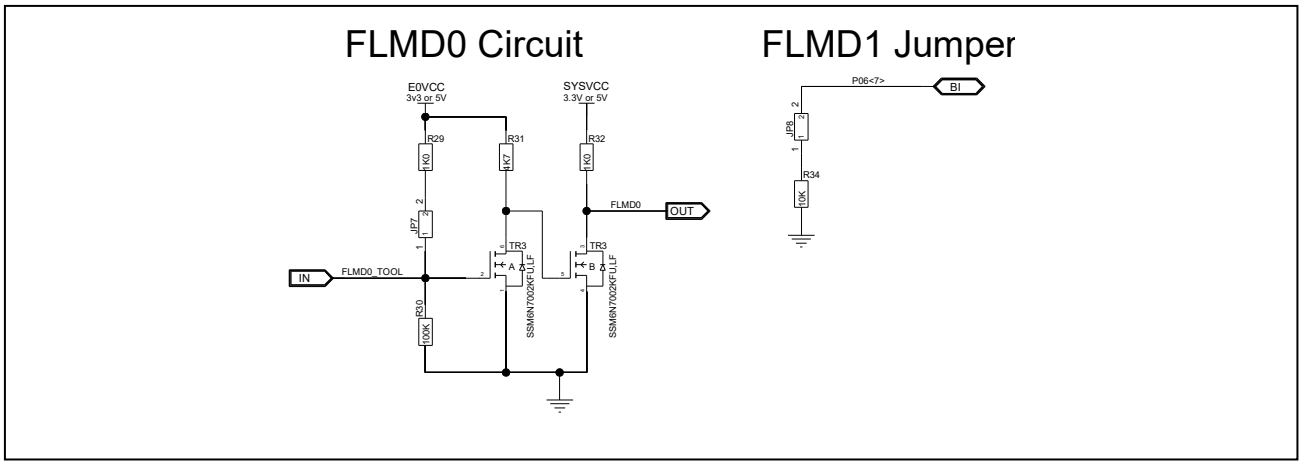


Figure 6.1 Operating mode selection jumpers

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP7.

All other jumpers related to the mode selection can be left open.

6.2 System State and RESET

This piggyback board has a special reset circuit using the Renesas GreenPAK IC.
On board version D019726_06_V01 and D019726_06_V02 this is the IC SLG46855.
On board version D019726_06_V03 and later this is the IC SLG7RN47274-AP_r004.

The basic function is the same on both GreenPAK ICs, but the internal circuit has been modified.

This GreenPAK IC is designed to receive various RH850 control signals and switch control LED accordingly. It also receives the signal from the RESET switch SW2 to generate the reset signal for the piggyback board and controls the reset LED.

The piggyback board has 3 LED to indicate control signals and reset status:

- LED4 for a control signal triggered by ERROROUT_M# or VMONOUT#.
- LED5 for a control signal triggered by PWRCTL.
- LED6 for a reset triggered by the reset switch SW2.

On board version D019726_06_V01 the piggyback board included the connectors CN19 – CN21. These could be used to input reset signals from external sources to the board. These connectors have been removed from board version D019726_06_V02 onwards.

Figure 6.2, Figure 6.3 and *Figure 6.4* show the circuit of the GreenPAK IC and the reset signal inputs.

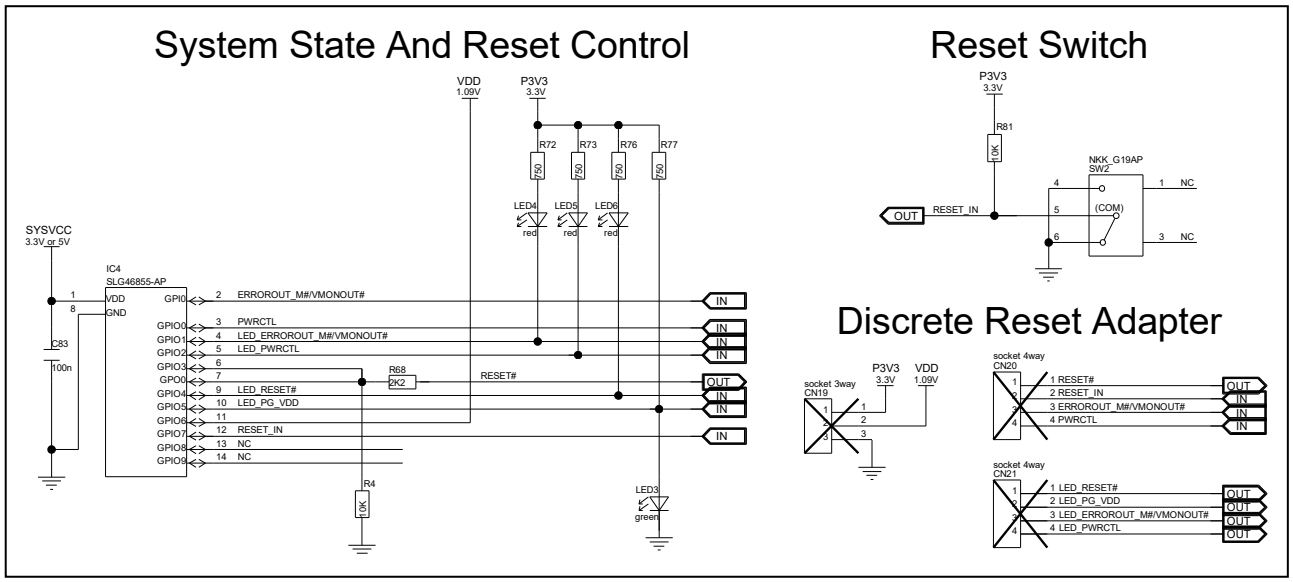


Figure 6.2 RESET circuit of board version D019726_06_V01

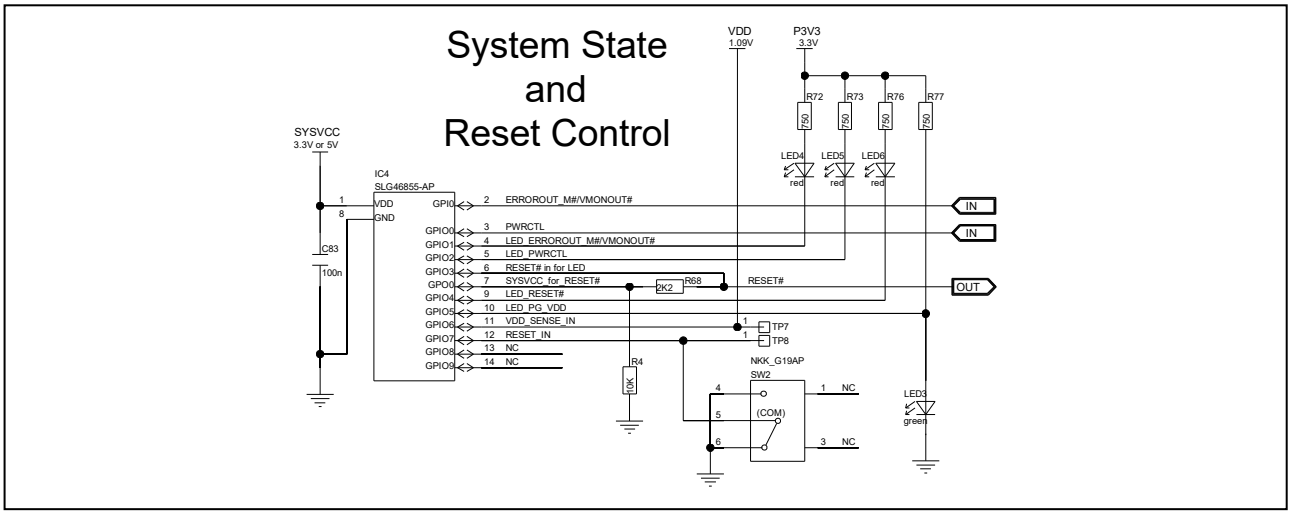


Figure 6.3 RESET circuit of board version D019726_06_V02

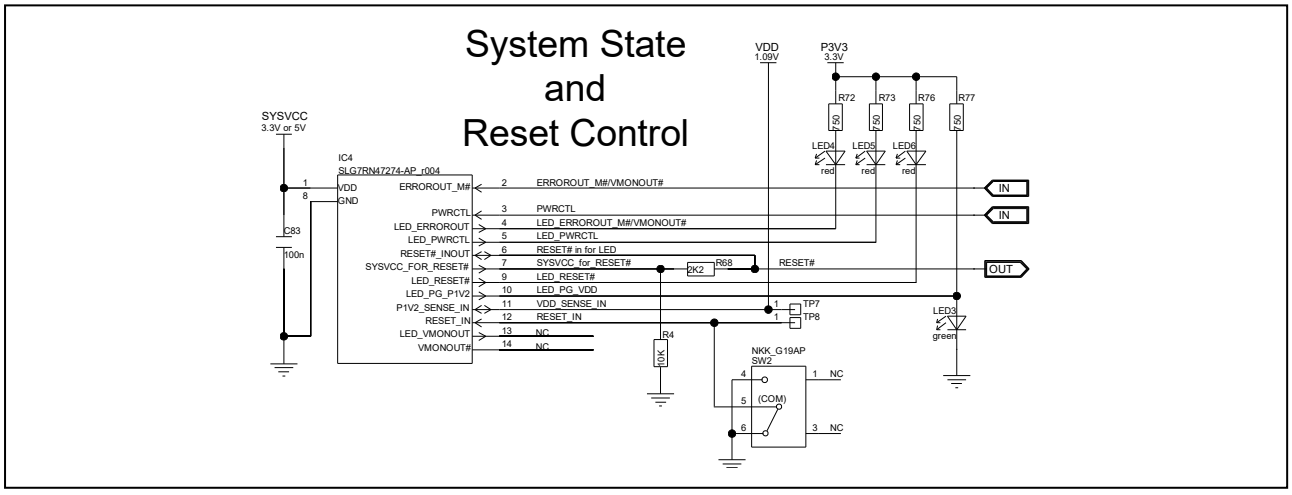


Figure 6.4 RESET circuit of board version D019726_06_V03

6.2.1 RESET Switch

Switch SW2 is used to issue a reset to the RH850/U2Cx.

The SW2 toggle switch allows to activate the reset in two different ways:

- SW2 in left '5-4' (left) position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW2 in right '5-6' (right) position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in *Figure 6.5*.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

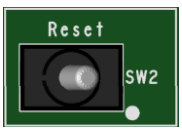


Figure 6.5 Operation of RESET switch

6.3 Ethernet / I2S Selection

Port P20_0 can be used to provide an I2SMCLK or ETH0RXD0 signal to an attached main board.

Jumper JP17 is used to select which signal is being used.

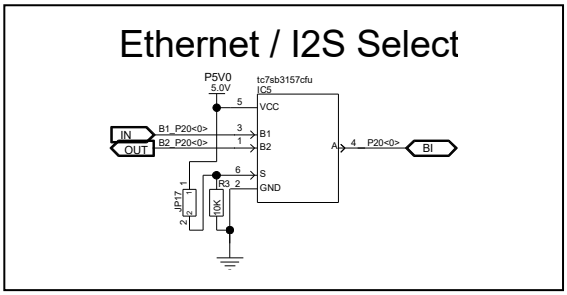


Figure 6.6 Circuit diagram for Ethernet and I2S signal selection

Table 6.2 Ethernet / I2S selection

Jumper	Function
JP17 [OPEN]	B1_P20_0 = ETH0RXD0
JP17 [CLOSED]	B2_P20_0 = I2SMCLK

6.4 Ethernet 1 Control Ports MDIO / MDC

The piggyback board Y-RH850-U2C-404PIN-PB-T1-V1 provides the Ethernet 1 control signals ETH1MDIO and ETH1MDC to a connected main board.

With board version D019726_06_V01 the Ethernet 1 control signals ETH1MDIO and ETH1MDC are fixed to the ports P21_0 (ETH1MDIO) and P20_11 (ETH1MDC).

On boards with version D019726_06_V02 and later the control ports can be used either with ports P21_0 (ETH1MDIO) / P20_11 (ETH1MDC) or with ports P04_9 (ETH1MDIO) / P04_8 (ETH1MDC). Jumper JP18 selects which ports are being used.

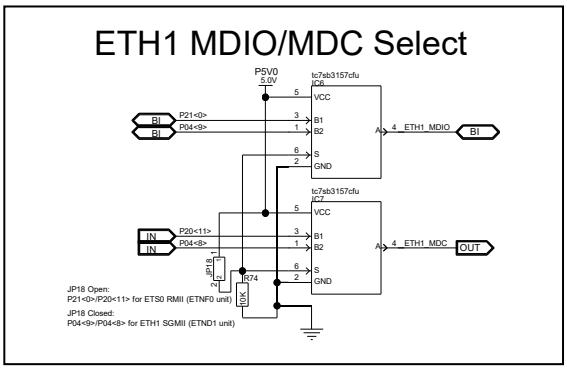


Figure 6.7 Circuit diagram for port selection for Ethernet control signals

Table 6.3 Ethernet 1 control port selection

Jumper	Function	Remark
JP18 [OPEN]	ETH1_MDIO = P21_0 ETH1_MDC = P20_11	Used for ETS0 RMII interface (ETNF0)
JP18 [CLOSED]	ETH1_MDIO = P04_9 ETH1_MDC = P04_8	Used for ETH1 SGMII interface (ETND1)

6.5 Ethernet Control Port P20_3

From board version D019726_06_V03 onwards the piggyback board Y-RH850-U2C-404PIN-PB-T1-V1 allows to use port P20_3 either as T1S_RX signal or as RMII_TXCLK signal.

The usage is selected by jumper JP21:

- JP21[1-2]: P20_3 used as T1S_RX
- JP21[2-3]: P20_3 used as RMII_TXCLK

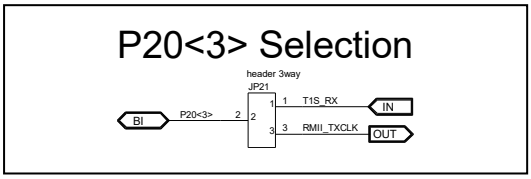


Figure 6.8 Circuit diagram for port P20_3 port selection

6.6 CAN XL Ports

RH850/U2C8 has 2 CAN XL interfaces, that can be used with CAN XL modules mounted on a connected main board (Y-COMMON-MB-T1-V1).

On board version D019726_06_V01 and D019726_06_V02 these ports are, only separated by termination resistors, connected to many other peripherals like

- Motor control circuits
- SFMA interface
- MMCA interface
- I2S interface
- FlexRay interface

These connections, including the necessary wiring on the pcb, may affect the CAN XL signals. To avoid such interferences the CAN XL signal are separated from the other peripheral circuits on board version D019726_06_V03 by multiplexers. The jumpers JP22 (CANXL0) and JP23 (CANXL1) control the multiplexers.

Figure 6.9 shows the switches that are used to separate the CAN XL signals from other peripheral circuits.

Table 6.4 lists the port connections for different jumper settings.

Table 6.4 Connections for ports P17_2, P17_3, P24_7 and P24_8

RH850 Port	Jumper Setting	Signal Name	Connector
P17_2	JP22[OPEN]	CANXL0RX	CN1_73
	JP22[CLOSED]	SFMA0IO1 / MOT0V_P / I2S1RXD	CN2_82 / CN3_87 / CN3_14
P17_3	JP22[OPEN]	CANXL0TX	CN1_71
	JP22[CLOSED]	SFMA0IO0 / MOT0V_N / I2S1TXD	CN2_81 / CN3_89 / CN3_12
P24_7	JP23[OPEN]	CANXL1TX	CN1_72
	JP23[CLOSED]	MMCA0DAT3 / FLX1TX	CN2_92 / CN1_45
P24_8	JP23[OPEN]	CANXL1RX	CN1_74
	JP23[CLOSED]	MMCA0CLK / FLX1RX	CN2_87 / CN1_47

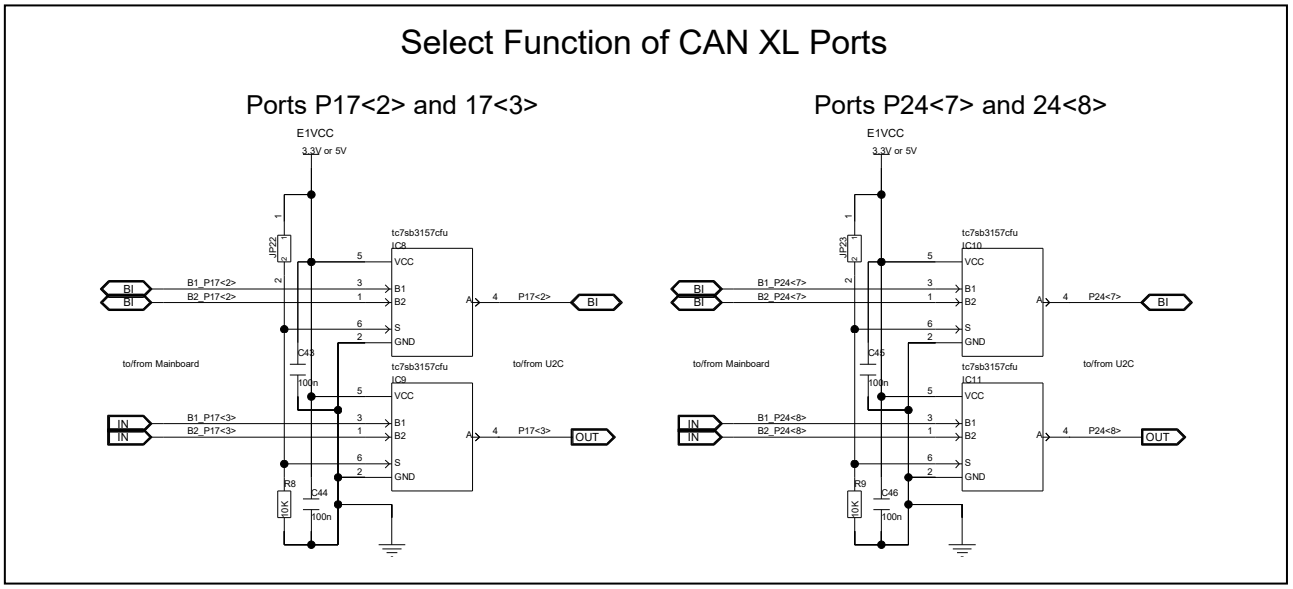


Figure 6.9 CAN XL port selection on board version D019726_06_V03

6.7 Series Termination Resistors

The piggyback board includes several series resistors, which can be used as termination resistors for high-speed communication channels. All signals are connected to the main board connectors CN1 – CN3.

On board version D019726_06_V03 the resistors R8 – R11 have been replaced by multiplexers (see chapter *6.6 CAN XL Ports*).

Table 6.5 lists all resistors and shows to which signal on the main board connector they are connected.

Figure 6.10 shows the circuit diagram for the series resistors.

Figure 6.11 shows the location of the resistors on the lower side of the piggyback board. These positions apply to all board versions, except that board version D019726_06_V03 does not have resistors R8 – R11.

Table 6.5 Series termination resistors

Resistor	RH850 Port	Signal Name	Connector
R8 *	P24_7	FLX1TX / MMCA0DAT3	CN1_45 / CN2_92
R9 *	P24_8	FLX1RX / MMCA0CLK	CN1_47 / CN2_87
R10 *	P17_2	I2S1RXD / MOT0V_P / SFMA0IO1	CN3_14 / CN3_87 / CN2_82
R11 *	P17_3	I2S1TXD / MOT0V_N / SFMA0IO0	CN3_12 / CN3_89 / CN2_81
MR1_1	P21_2	ETH0TXD0	CN1_54
MR1_2	P21_3	ETH0TXD1	CN1_56
MR1_3	P20_9	ETH0TXD2	CN1_58
MR1_4	P20_10	ETH0TXD3	CN1_60
R1	P20_6	ETH0TXER	CN1_64
R16	P22_0	ETH0MDC	CN1_52
R17	P21_10	ETH0RESET / MUX2	CN1_69 / CN1_105
R18	P20_5	ETH0TXEN	CN1_66
R19	P22_1	ETH0MDIO / FLXSTPWT	CN1_51 / CN1_44

* Only for board versions D019726_06_V01 and D019726_06_V02

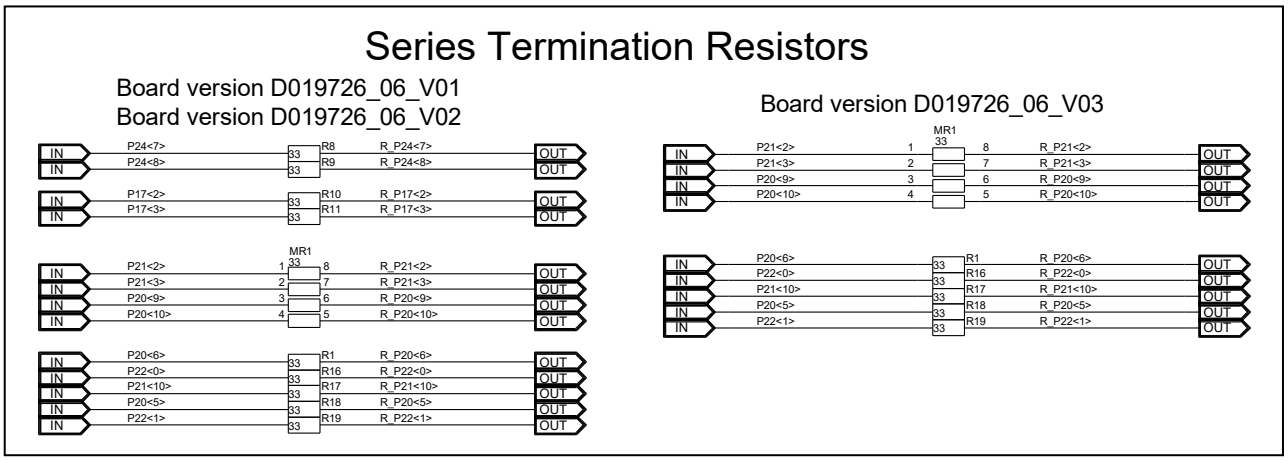


Figure 6.10 Series termination resistors

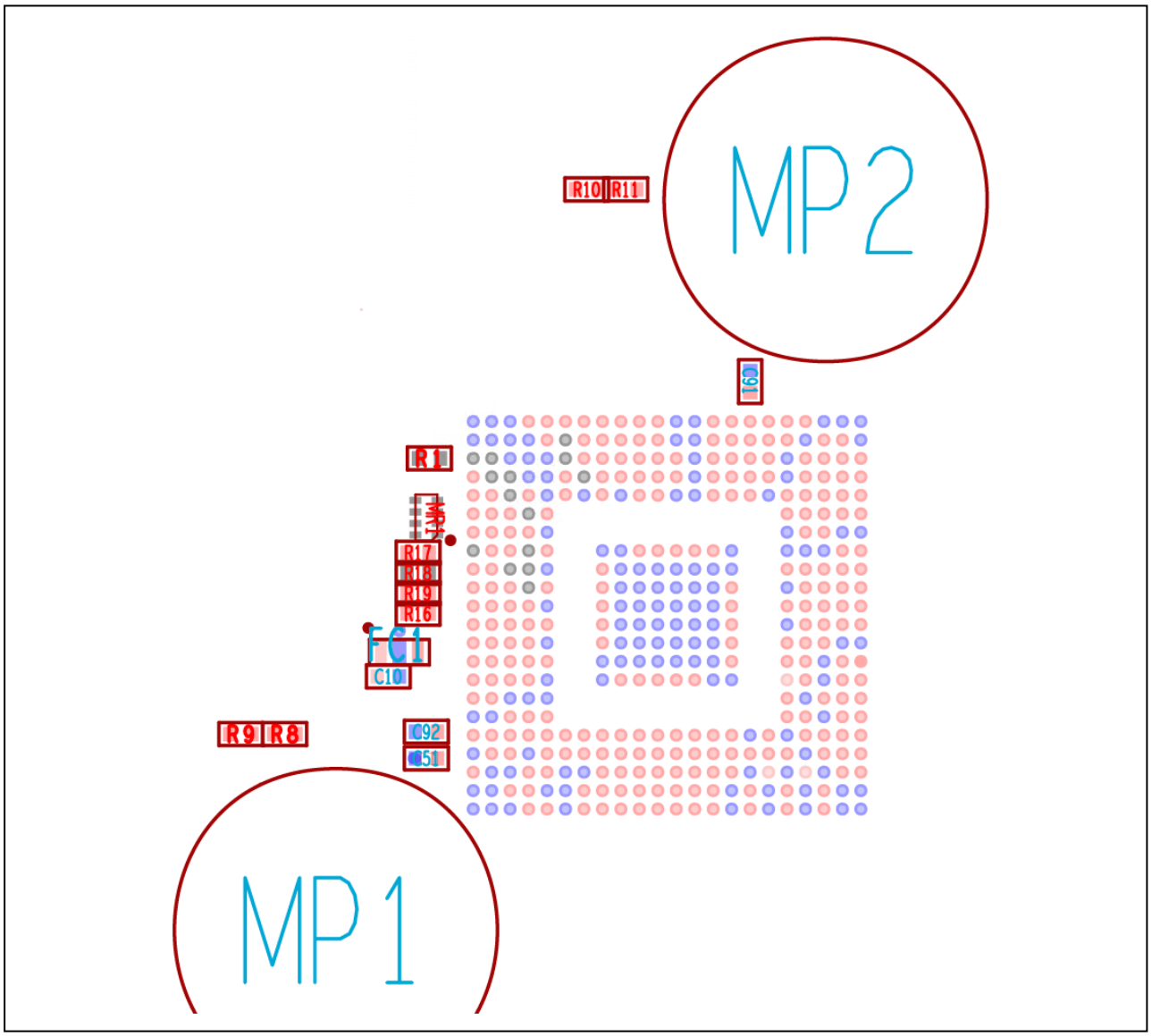


Figure 6.11 Location of series termination resistors

6.8 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

The device pins P00_0 to P00_7 are connected to the odd pins of the pin header JP20 (CN11 for board version D019726_06_V01).

The LEDs LED10 to LED17 are connected to the even JP20 (CN11) pins.

Thus, the LEDs can be either connected to

- the device port pins P00_0 to P00_7 by closing the connection on JP20 (CN11) using a jumper, or
- any device pin by connecting the pin (from the connectors CN13, CN14 or CN15) directly with the even JP20 (CN11) pins using a separate cable.

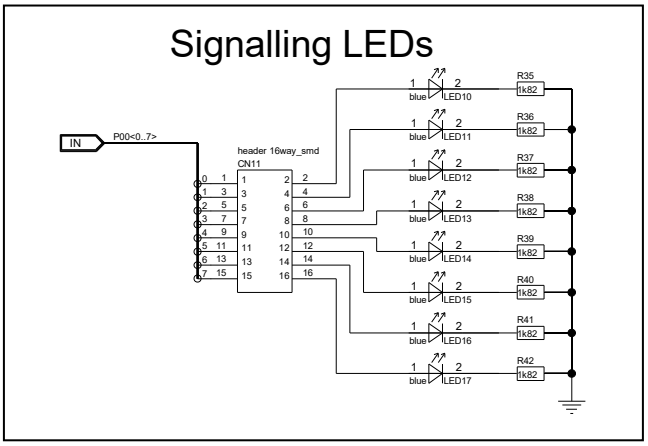


Figure 6.12 Circuit diagram for signalling LEDs of board version D019726_06_V01

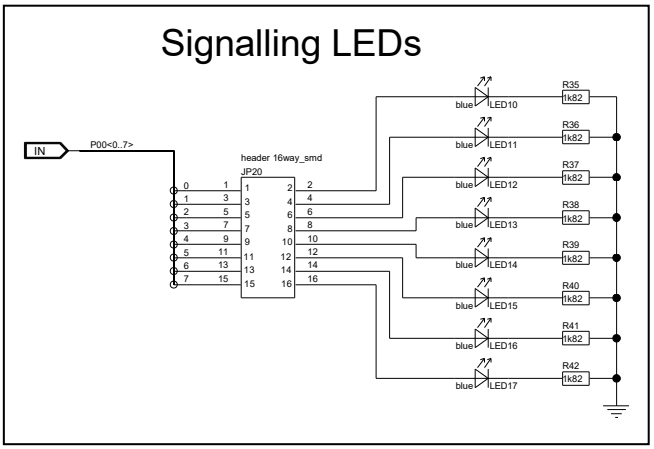


Figure 6.13 Circuit diagram for signalling LEDs from board version D019726_06_V02 onwards

6.9 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- All even numbered pins are connected to L level, i.e. to GND.
- Odd numbered pins 1, 3, 5 and 7 are connected jumper JP14 and can be pulled up to 3.3 V or 5.0 V.
- Odd numbered pins 9, 11, 13 and 15 are connected jumper JP15 and can be pulled up to 3.3 V or 5.0 V.

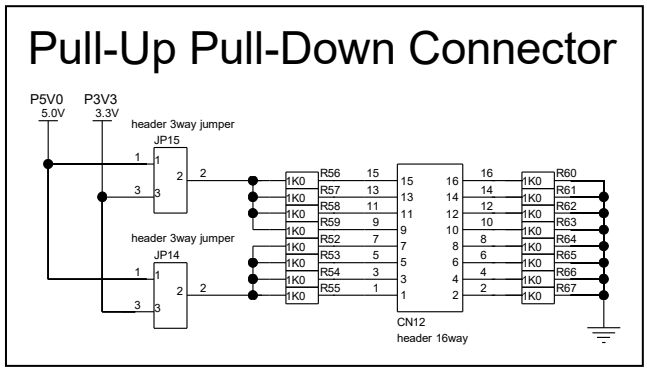


Figure 6.14 Circuit diagram for pull up / pull down signals

Refer to *7.5 Pull-Up/Pull-Down Pin Header CN12* for CN12 details.

Note

On board version D019726_06_V02 only the pull-down resistor R60 is connected to GND, R61-R67 are not connected to GND.

So we manually added a bridge from R60 to R61-R67 to make sure all pull-down resistors work as expected.

Other board versions are not affected.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.

Refer to *1.2 Supported Main Boards* for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Function on		Device port	Pin	Function on		Device port
	Main Board	Piggyback			Main Board	Piggyback	
1	VDDA	–	–	2	VDDA	–	–
3	VDDA	–	–	4	VDDA	–	–
5	RESET	RESET#	RESET#	6	NMI	NMI	P02_3
7	WAKE	IRQ39	P03_12	8	–	–	–
9	INT0	IRQ39	P03_12	10	INT1	IRQ34	P02_11
11	INT2	IRQ16	P06_13	12	INT3	IRQ20	P10_14
13	–	–	–	14	–	–	–
15	UART0TX	RLIN36TX	P04_15	16	UART1TX	RLIN318TX	P02_13
17	UART0RX	RLIN36RX	P04_14	18	UART1RX	RLIN318RX	P02_12
19	LIN0TX	RLIN30TX	P06_6	20	LIN1TX	RLIN31TX	P06_4
21	LIN0RX	RLIN30RX	P06_7	22	LIN1RX	RLIN31RX	P06_5
23	IIC0SCL	RI3C0SCL	P03_1	24	IIC1SCL	RI3C1SCL	P06_8
25	IIC0SDA	RI3C0SDA	P03_0	26	IIC1SDA	RI3C1SDA	P06_9
27	CAN0TX	CAN0TX	P02_2	28	CAN1TX	CAN1TX	P04_12
29	CAN0RX	CAN0RX	P02_0	30	CAN1RX	CAN1RX	P04_13
31	SENT0RX	RSENT2RX	P02_9	32	SENT1RX	RSENT5RX	P22_3
33	SENT0SPCO	RSENT2SPCO	P02_8	34	SENT1SPCO	RSENT5SPCO	P22_4
35	PSI5SRX0	–	–	36	PSI5RX0	–	–
37	PSI5STX0	–	–	38	PSI5TX0	–	–
39	PSI5SCLK0	–	–	40	–	–	–
41	FLX0TX	FLXA0TXDA	P24_12	42	FLX0EN	FLXA0TXENA	P24_10
43	FLX0RX	FLXA0RXDA	P24_11	44	FLXSTPWT	FLXA0STPWT	R_P22_1
45	FLX1TX	FLXA0TXDB	R_P24_7 [1) 2)] B2_P24_7 [4)]	46	FLX1EN	FLXA0TXENB	P24_9

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
47	FLX1RX	FLXA0RXDB	R_P24_8 [1) 2)] B2_P24_8 [4)]
49	–	–	–
51	ETH0MDIO	ETH0_MDIO	R_P22_1
53	ETH0RXD0	ETH0_MII_RXD0 ETH0_RMII_RXD0	B1_P20_0
55	ETH0RXD1	ETH0_MII_RXD1 ETH0_RMII_RXD1	P20_1
57	ETH0RXD2	ETH0_MII_RXD2	P10_1
59	ETH0RXD3	ETH0_MII_RXD3	P10_2
61	ETH0RXCLK	ETH0_MII_RX_CLK	P10_3
63	ETH0RXER	ETH0_MII_RX_ER ETH0_RMII_ER	P20_12
65	ETH0CRSDV	–	–
67	ETH0RXDV	ETH0_MII_RX_DV ETH0_RMII_RX_DV	P20_2
69	ETH0RESET	P21_10	R_P21_10
71	CANXL0TX	CANXL0TXD	P17_3 [1) 2)] B1_P17_3 [4)]
73	CANXL0RX	CANXL0RXD	P17_2 [1) 2)] B1_P17_2 [4)]
75	CANXL2TX	–	–
77	CANXL2RX	–	–
79	ETH0_T1S_TX	ETS0_TX	P20_4
81	ETH0_T1S_ RX_MDC	ETS0_RX_MDC	P20_3
83	ETH0_T1S_ RX_MDIO	ETS0_ED_MDIO	P20_13
85	DIGIO_0	P02_11	P02_11
87	DIGIO_2	P02_14	P02_14
89	DIGIO_4	P17_7	P17_7
91	DIGIO_6	P22_8	P22_8
93	DIGIO_8	P00_0	P00_0
95	DIGIO_10	P00_2	P00_2
97	DIGIO_12	P00_4	P00_4
99	DIGIO_14	P00_6 [1)] P06_3 [3)]	P00_6 [1)] P06_3 [3)]

Pin	Function on		Device port
	Main Board	Piggyback	
48	FLX1CLK	–	–
50	–	–	–
52	ETH0MDC	ETH0_MDC	R_P22_0
54	ETH0TXD0	ETH0_MII_TXD0 ETH0_RMII_TXD0	R_P21_2
56	ETH0TXD1	ETH0_MII_TXD1 ETH0_RMII_TXD1	R_P21_3
58	ETH0TXD2	ETH0_MII_TXD2	R_P20_9
60	ETH0TXD3	ETH0_MII_TXD3	R_P20_10
62	ETH0TXCLK	ETH0_MII_TX_CLK ETH0_RMII_CLK	P21_1
64	ETH0TXER	ETH0_MII_TX_ER	R_P20_6
66	ETH0TXEN	ETH0_MII_TX_EN ETH0_RMII_TX_EN	R_P20_5
68	ETH0COL	–	–
70	ETH0LINK	ETH0_LINKSTA	P22_2
72	CANXL1TX	CANXL1TXD	P24_7 [1) 2)] B1_P24_7 [4)]
74	CANXL1RX	CANXL1RXD	P24_8 [1) 2)] B1_P24_8 [4)]
76	CANXL3TX	–	–
78	CANXL3RX	–	–
80	ETH1_T1S_TX	–	–
82	ETH1_T1S_ RX_MDC	–	–
84	ETH1_T1S_ RX_MDIO	–	–
86	DIGIO_1	P19_4	P19_4
88	DIGIO_3	P19_5	P19_5
90	DIGIO_5	P22_7	P22_7
92	DIGIO_7	P22_9	P22_9
94	DIGIO_9	P00_1	P00_1
96	DIGIO_11	P00_3	P00_3
98	DIGIO_13	P00_5 [1)] P06_2 [3)]	P00_5 [1)] P06_2 [3)]
100	DIGIO_15	P00_7 [1)] P06_4 [3)]	P00_7 [1)] P06_4 [3)]

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
101	–	–	–
103	MUX0	ADCK2SEL0	P21_8
105	MUX2	ADCK2SEL2	R_P21_10
107	ADC0	ADCK2I0	AP4_0
109	ADC2	ADCK2I2	AP4_2
111	ADC4	ADCK2I4	AP4_4
113	ADC6	ADCK2I6	AP4_6
115	VDDIOF	–	–
117	VDDB	–	–
119	VDDB	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
102	–	–	–
104	MUX1	ADCK2SEL1	P21_9
106	–	–	–
108	ADC1	ADCK2I1	AP4_1
110	ADC3	ADCK2I3	AP4_3
112	ADC5	ADCK2I5	AP4_5
114	ADC7	ADCK2I7	AP4_7
116	VDDIOF	–	–
118	VDDB	–	–
120	VDDB	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

[1] Board version D019726_06_V01
[2] Board version D019726_06_V02
[3] Board version D019726_06_V02 and later
[4] Board version D019726_06_V03

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function on		Device port
	Main Board	Piggyback	
1	CAN2TX	CAN2TX	P06_0
3	CAN2RX	CAN2RX	P06_1
5	CAN4TX	CAN4TX	P06_11
7	CAN4RX	CAN4RX	P06_12
9	LIN2TX	RLIN32TX	P06_0
11	LIN2RX	RLIN32RX	P06_1
13	LIN4TX	RLIN34TX	P04_9
15	LIN4RX	RLIN34RX	P04_8
17	LIN6TX	RLIN36TX	P04_15
19	LIN6RX	RLIN36RX	P04_14
21	LIN8TX	RLIN38TX	P02_1
23	LIN8RX	RLIN38RX	P02_0
25	LIN10TX	RLIN310TX	P19_1

Pin	Function on		Device port
	Main Board	Piggyback	
2	CAN3TX	CAN3TX	P10_7
4	CAN3RX	CAN3RX	P10_6
6	CAN5TX	CAN5TX	P02_7
8	CAN5RX	CAN5RX	P02_8
10	LIN3TX	RLIN33TX	P06_3
12	LIN3RX	RLIN33RX	P06_2
14	LIN5TX	RLIN35TX	P19_3
16	LIN5RX	RLIN35RX	P19_2
18	LIN7TX	RLIN37TX	P04_12
20	LIN7RX	RLIN37RX	P04_13
22	LIN9TX	RLIN39TX	P02_6
24	LIN9RX	RLIN39RX	P02_5
26	LIN11TX	RLIN311TX	P10_12

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
27	LIN10RX	RLIN310RX	P19_0
29	LIN12TX	RLIN312TX	P04_6
31	LIN12RX	RLIN312RX	P04_5
33	LIN14TX	RLIN314TX	P22_6
35	LIN14RX	RLIN314RX	P22_5
37	–	–	–
39	CAN12TX	CAN12TX	P08_3
41	CAN12RX	CAN12RX	P08_2
43	CAN14TX	–	–
45	CAN14RX	–	–
47	CAN6TX	CAN6TX	P21_6
49	CAN6RX	CAN6RX	P21_5
51	CAN8TX	CAN8TX	P03_10
53	CAN8RX	CAN8RX	P03_11
55	CAN10TX	CAN10TX	P04_3
57	CAN10RX	CAN10RX	P04_2
59	–	–	–
61	LIN16TX	RLIN316TX	P17_11
63	LIN16RX	RLIN316RX	P17_10
65	LIN18TX	RLIN318TX	P02_13
67	LIN18RX	RLIN318RX	P02_12
69	LIN20TX	–	–
71	LIN20RX	–	–
73	LIN22TX	–	–
75	LIN22RX	–	–
77	–	–	–
79	SFMA0CLK	SFMA0CLK	P17_5
81	SFMA0IO0	SFMA0IO0	R_P17_3 [1) 2)] B2_P17_3 [4)]
83	SFMA0IO2	SFMA0IO2	P17_1
85	–	–	–
87	MMCA0CLK	MMCA0CLK	R_P24_8 [1) 2)] B2_P24_8 [4)]
89	MMCA0DAT0	MMCA0DAT0	P24_10

Pin	Function on		Device port
	Main Board	Piggyback	
28	LIN11RX	RLIN311RX	P10_11
30	LIN13TX	RLIN313TX	P02_4
32	LIN13RX	RLIN313RX	P02_3
34	LIN15TX	RLIN315TX	P17_13
36	LIN15RX	RLIN315RX	P17_12
38	–	–	–
40	CAN13TX	CAN13TX	P08_0
42	CAN13RX	CAN13RX	P08_1
44	CAN15TX	–	–
46	CAN15RX	–	–
48	CAN7TX	CAN7TX	P04_1
50	CAN7RX	CAN7RX	P04_0
52	CAN9TX	CAN9TX	P04_9
54	CAN9RX	CAN9RX	P04_8
56	CAN11TX	CAN11TX	P04_11
58	CAN11RX	CAN11RX	P04_10
60	–	–	–
62	LIN17TX	RLIN317TX	P17_9
64	LIN17RX	RLIN317RX	P17_8
66	LIN19TX	–	–
68	LIN19RX	–	–
70	LIN21TX	–	–
72	LIN21RX	–	–
74	LIN23TX	RLIN323TX	P06_9
76	LIN23RX	RLIN323RX	P06_8
78	–	–	–
80	SFMA0SSL	SFMA0SSL	P17_4
82	SFMA0IO1	SFMA0IO1	R_P17_2 [1) 2)] B2_P17_2 [4)]
84	SFMA0IO3	SFMA0IO3	P17_0
86	–	–	–
88	MMCA0CMD	MMCA0CMD	P24_9
90	MMCA0DAT1	MMCA0DAT1	P24_11

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
91	MMCA0DAT2	MMCA0DAT2	P24_12
93	MMCA0DAT4	MMCA0DAT4	P24_4
95	MMCA0DAT6	MMCA0DAT6	P24_6
97	–	–	–
99	ETH1MDIO	ETS0_MDIO	P21_0 [1)] ETH1_MDIO [3)]
101	ETH1RXD0	ETS0_RMII_RXD0	P10_4
103	ETH1RXD1	ETS0_RMII_RXD1	P10_5
105	ETH1RXD2	–	–
107	ETH1RXD3	–	–
109	ETH1RXCLK	–	–
111	ETH1RXER	–	–
113	ETH1CRSDV	ETS0_RMII_CRSDV	P10_10
115	ETH1RXDV	–	–
117	ETH1RESET	P10_9	P10_9
119	–	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
92	MMCA0DAT3	MMCA0DAT3	R_P24_7 [1) 2)] B2_P24_7 [4)]
94	MMCA0DAT5	MMCA0DAT5	P24_5
96	MMCA0DAT7	MMCA0DAT7	P24_13
98	–	–	–
100	ETH1MDC	ETS0_MDC	P20_11 [1)] ETH1_MDC [3)]
102	ETH1TXD0	ETS0_RMII_TXD0	P20_8
104	ETH1TXD1	ETS0_RMII_TXD1	P20_7
106	ETH1TXD2	–	–
108	ETH1TXD3	–	–
110	ETH1TXCLK	ETS0_RMII_REFCLK	P20_3
112	ETH1TXER	–	–
114	ETH1TXEN	ETS0_RMII_TXEN	P10_0
116	ETH1COL	–	–
118	ETH1LINK	–	–
120	–	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

[1)] Board version D019726_06_V01
[2)] Board version D019726_06_V02
[3)] Board version D019726_06_V02 and later
[4)] Board version D019726_06_V03

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function on		Device port
	Main Board	Piggyback	
1	CSI0CS0	MSPI0CSS0	P06_9
3	CSI0CS1	MSPI0CSS1	P06_8
5	CSI0CS2	MSPI0CSS6	P06_11
7	CSI0CS3	MSPI0CSS7	P06_10

Pin	Function on		Device port
	Main Board	Piggyback	
2	CSI0CLK	MSPI0SC	P06_6
4	CSI0SI	MSPI0SI	P06_5
6	CSI0SO	MSPI0SO	P06_7
8	–	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
9	–	–	–
11	I2S0TXD	–	–
13	I2S0RXD	–	–
15	I2S0BCLK	–	–
17	I2S0LRCLK	–	–
19	I2S0MCLK	SSIFACK	B2_P20_0
21	CSI1CS2	MSPI1CSS5	P04_5
23	–	–	–
25	–	–	–
27	–	–	–
29	CSI1SCLK	MSPI1SC	P02_3
31	–	–	–
33	MOT0ADU	ADCKAI0	AP0_0
35	MOT0ADV	ADCKAI1	AP0_1
37	MOT0ADW	ADCKAI2	AP0_2
39	MOT0RDCS1	ADCKAI3	AP0_3
41	MOT0RDCS3	ADCKAI4	AP0_4
43	MOT0RDCS2	ADCKAI5	AP0_5
45	MOT0RDCS4	ADCKAI6	AP0_6
47	MOT0RDCCOM	ADCKAI7	AP0_7
49	MOT0RDCRSO	ADCKAI8	AP0_8
51	–	–	–
53	–	–	–
55	AD1_0	ADCKAI9	AP0_9
57	AD1_2	ADCKAI11	AP0_11
59	AD1_4	ADCKAI13	AP0_13
61	AD1_6	ADCKAI15	AP0_15
63	PWM0	PWGC32O	P02_0
65	PWM2	PWGC41O	P02_2
67	PWM4	PWGC43O	P02_4
69	PWM6	PWGC45O	P02_6
71	DIGIO16	P02_10	P02_10

Pin	Function on		Device port
	Main Board	Piggyback	
10	CSI1CS1	MSPI1CSS2	P02_6
12	I2S1TXD	SSIF1TXD	R_P17_3 [1) 2)] B2_P17_3 [4)]
14	I2S1RXD	SSIF1RXD	R_P17_2 [1) 2)] B2_P17_2 [4)]
16	I2S1BCLK	SSIF1BCK	P17_4
18	I2S1LRCLK	SSIF1LRCK SSIF1FS	P17_5
20	–	–	–
22	CSI1CS3	MSPI1CSS6	P04_6
24	CSI1CS0	MSPI1CSS0	P02_2
26	DIGIO_24	P04_4	P04_4
28	CSI1SO	MSPI1SO	P02_5
30	CSI1SI	MSPI1SI	P02_4
32	–	–	–
34	MOT1ADU	ADCK1I0	AP2_0
36	MOT1ADV	ADCK1I1	AP2_1
38	MOT1ADW	ADCK1I2	AP2_2
40	MOT1RDCS1	ADCK1I3	AP2_3
42	MOT1RDCS3	ADCK1I4	AP2_4
44	MOT1RDCS2	ADCK1I5	AP2_5
46	MOT1RDCS4	ADCK1I6	AP2_6
48	MOT1RDCCOM	ADCK1I7	AP2_7
50	MOT1RDCRSO	ADCK1I8	AP2_8
52	–	–	–
54	–	–	–
56	AD1_1	ADCKAI10	AP0_10
58	AD1_3	ADCKAI12	AP0_12
60	AD1_5	ADCKAI14	AP0_14
62	AD1_7	ADCKAI16	AP1_0
64	PWM1	PWGC33O	P02_1
66	PWM3	PWGC42O	P02_3
68	PWM5	PWGC44O	P02_5
70	PWM7	PWGC50O	P02_7
72	DIGIO17	P22_2	P22_2

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
73	DIGIO18	P04_7	P04_7
75	DIGIO20	P10_14	P10_14
77	DIGIO22	P21_4	P21_4
79	ENC0	ENCA0E0	P02_9
81	MOT0ERR	–	–
83	MOT0U_P	TSG30O1	P17_0
85	MOT0U_N	TSG30O2	P17_1
87	MOT0V_P	TSG30O3	R_P17_2 [1) 2)] B2_P17_2 [4)]
89	MOT0V_N	TSG30O4	R_P17_3 [1) 2)] B2_P17_3 [4)]
91	MOT0W_P	TSG30O5	P17_4
93	MOT0W_N	TSG30O6	P17_5
95	–	–	–
97	–	–	–
99	–	–	–
101	GND	–	–
103	AD2_0	ADCK1I9	AP2_9
105	AD2_1	ADCK1I10	AP2_10
107	AD2_2	ADCK1I11	AP2_11
109	AD2_3	ADCK1I12	AP2_12
111	AD2_4	ADCK1I13	AP2_13
113	AD2_5	ADCK1I14	AP2_14
115	AD2_6	ADCK1I15	AP2_15
117	AD2_7	ADCK1I16	AP3_0

Pin	Function on		Device port
	Main Board	Piggyback	
74	DIGIO19	P10_8	P10_8
76	DIGIO21	P17_6	P17_6
78	DIGIO23	P21_7	P21_7
80	ENC1	ENCA0E1	P10_11
82	MOT1ERR	TAPA0ESO	P06_6
84	MOT1U_P	TAPA0UP	P06_1
86	MOT1U_N	TAPA0UN	P06_0
88	MOT1V_P	TAPA0VP	P06_5
90	MOT1V_N	TAPA0VN	P06_4
92	MOT1W_P	TAPA0WP	P06_3
94	MOT1W_N	TAPA0WN	P06_2
96	–	–	–
98	–	–	–
100	ETH0_SO_P	CN_ETH1_SG_TXD_P [1)] – [3)]	CN_ETH1_SG_TXD_P [1)] – [3)]
102	ETH0_SO_N	CN_ETH1_SG_TXD_N [1)] – [3)]	CN_ETH1_SG_TXD_N [1)] – [3)]
104	–	–	–
106	ETH0_SI_P	ETH1_SG_RXD_P [1)] – [3)]	ETH1_SG_RXD_P [1)] – [3)]
108	ETH0_SI_N	ETH1_SG_RXD_N [1)] – [3)]	ETH1_SG_RXD_N [1)] – [3)]
110	–	–	–
112	ETH1_SO_P	– [1)] CN_ETH1_SG_TXD_P [3)]	– [1)] CN_ETH1_SG_TXD_P [3)]
114	ETH1_SO_N	– [1)] CN_ETH1_SG_TXD_N [3)]	– [1)] CN_ETH1_SG_TXD_N [3)]
116	–	–	–
118	ETH1_SI_P	– [1)] ETH1_SG_RXD_P [3)]	– [1)] ETH1_SG_RXD_P [3)]

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
119	GND	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
120	ETH1_SI_N	– [1)] ETH1_SG_RXD_N [3)]	– [1)] ETH1_SG_RXD_N [3)]
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

[1)] Board version D019726_06_V01
[2)] Board version D019726_06_V02
[3)] Board version D019726_06_V02 and later
[4)] Board version D019726_06_V03

7.2 Debug Connector CN9

Table 7.4 On-chip debug connector CN9

Pin	Function	Device port
1	LPDCLK / FPCK	JP0_2
3	TRST	TRST#_TOOL
5	LPDO	JP0_1
7	LPDI / FPDR	JP0_0
9	–	JP0_3
11	LPDCLKO	JP0_5
13	RESET	RESET#

Pin	Function	Device port
2	GND	GND
4	FPMD0	FLMD0_TOOL
6	FPMD1	–
8	TVDD	E0VCC
10	EVTO	EVTO0#_P10_14
12	GND	GND
14	GND	GND

7.3 Debug Connector CN10

Table 7.5 On-chip debug connector CN10

Pin	Function	Device port
1		TODP0
3		TODN0
5	GND	
7	–	TODP1
9	–	TODN1
11	GND	
13	–	–
15	–	–
17	GND	
19	–	–
21	–	–
23	GND	
25	–	–
27	–	–
29	GND	
31	–	HSIFD_REFCLK
33	–	–
35	GND	
37	–	HSIFD_RXDP
39	–	HSIFD_RXDN
41	GND	
43	–	HSIFD_TXDP
45	–	HSIFD_TXDN

Pin	Function	Device port
2	VCC	E0VCC
4	TCK	JP0_2
6	–	–
8	AURORES#	AURORES#_VCC
10	VSTBY	EMUVDD
12	Controlled by JP6 JP6 [1-2]: E0VCC JP6 [2-3]: TRST#_TOOL	TRST#
14	MD0	FLMD0_TOOL
16	EVTI0	EVTI0
18	EVTO0	EVTO0#_P10_14
20	MSYN#	MSYN#
22		RESET#
24	GND	
26		CICREFP
28		CICREFN
30	GND	
32	WDGDIS	–
34		RESETOUT#
36	GND	
38	TMS	JP0_3
40	TDI / LPDIO / FPDR	JP0_0
42	GND	
44	TDO / LPDO / FPDT	JP0_1
46	DRDY	JP0_5

7.4 Device Ports Connectors CN13, CN14 and CN15

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.4.1 Device Ports Connector CN13

Table 7.6 Device ports connector CN13

Pin	Device port	Pin	Device port
1	AP0_13	2	AP1_3
3	AP1_1	4	AP0_1
5	AP1_0	6	AP1_2
7	AP2_4	8	AP2_0
9	AP2_8	10	AP2_2
11	AP2_6	12	AP2_3
13	AP2_12	14	AP2_1
15	AP2_10	16	AP2_7
17	AP3_0	18	AP2_5
19	AP2_14	20	AP2_11
21	AP3_2	22	AP2_9
23	AP3_3	24	AP3_1
25	AP2_15	26	AP2_13
27	P10_14	28	P10_13
29	P10_12	30	P10_11
31	P17_12	32	P17_13
33	P17_6	34	P17_5
35	P17_4	36	P17_11
37	P17_3	38	P17_2
39	P17_1	40	P10_10
41	P17_10	42	P10_9
43	P17_0	44	P10_8
45	P10_7	46	P10_6
47	P10_5	48	P10_3
49	P10_4	50	P10_2
51	P10_1	52	P10_0
53	P17_8	54	P17_9
55	P20_2	56	P17_7

Table 7.6 Device ports connector CN13 (cont'd)

Pin	Device port	Pin	Device port
57	R_P20_6	58	P20_0
59	P21_5	60	P20_1
61	P20_8	62	R_P20_10
63	P21_9	64	P20_7
65	R_P20_9	66	P21_6
67	P21_7	68	P20_11
69	P20_3	70	P20_4
71	P21_8	72	P20_13
73	P20_12	74	P21_0
75	P21_4	76	R_P21_3
77	P21_1	78	R_P21_2
79	R_P21_10	80	R_P20_5

7.4.2 Device Ports Connector CN14

Table 7.7 Device ports connector CN14

Pin	Device port	Pin	Device port
1	P08_3	2	P02_14
3	P02_12	4	P04_9
5	P03_10	6	P04_15
7	P04_10	8	P03_12
9	P02_13	10	P03_11
11	P02_11	12	P02_10
13	P04_4	14	P04_7
15	P04_6	16	P04_5
17	P02_9	18	P02_7
19	P02_4	20	P02_6
21	P02_5	22	P02_1
23	P02_8	24	RESETOUT#
25	P02_3	26	P00_6
27	P02_2	28	P00_7
29	P02_0	30	P00_5
31	P03_0	32	P03_1
33	P00_4	34	P00_3
35	P00_2	36	P00_1
37	TRST#	38	P00_0

Table 7.7 Device ports connector CN14 (cont'd)

Pin	Device port	Pin	Device port
39	PWRCTL	40	RESET#
41	X1_C	42	X2_C
43	FLMD0	44	AWOVCL
45	GETH0VCL	46	AP4_7
47	AP4_4	48	AP4_6
49	AP4_2	50	AP4_3
51	AP4_5	52	AP4_1
53	AP4_0	54	ERROROUT_M# / VMONOUT#
55	P24_12	56	P24_13
57	P24_9	58	P24_10
59	P24_7	60	P24_11
61	P24_6	62	P24_8
63	P24_4	64	P24_5
65	P19_5	66	P19_4
67	P22_6	68	R_P22_0
69	P19_2	70	P19_3
71	P22_9	72	P22_5
73	P19_0	74	P19_1
75	P22_8	76	R_P22_1
77	P22_7	78	P22_2
79	P22_4	80	P22_3

7.4.3 Device Ports Connector CN15

Table 7.8 Device ports connector CN15

Pin	Device port	Pin	Device port
1	P04_14	2	P04_11
3	P08_2	4	P04_8
5	P04_12	6	P04_13
7	P08_0	8	P08_1
9	P04_1	10	P04_2
11	P04_0	12	P04_3
13	P06_2	14	P06_3
15	P06_0	16	P06_1
17	P06_6	18	P06_7
19	P06_5	20	P06_4
21	P06_8	22	P06_9

Table 7.8 Device ports connector CN15 (cont'd)

Pin	Device port	Pin	Device port
23	P06_10	24	P06_12
25	P06_11	26	P06_13
27	AP0_11	28	AP0_8
29	AP0_10	30	AP0_9
31	AP0_7	32	AP0_4
33	AP0_6	34	AP0_5
35	AP0_15	36	AP0_14
37	AP0_2	38	AP0_0
39	AP0_12	40	AP0_3

7.5 Pull-Up/Pull-Down Pin Header CN12

Table 7.9 Pull-up and pull-down signal connector CN12

Pin	Function	Pin	Function
1	Level set by jumper JP14: JP14 [1-2]: 5.0 V (P5V0) JP14 [2-3]: 3.3 V (P3V3)	2	Fixed L level
3		4	
5		6	
7		8	
9	Level set by jumper JP15: JP15 [1-2]: 5.0 V (P5V0) JP15 [2-3]: 3.3 V (P3V3)	10	
11		12	
13		14	
15		16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Emulator

Basically, the piggyback board can solely be powered by a connected emulator. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings

All of the following board configurations are based on these conditions:

- Normal device operation mode (JP7[OPEN]: FLMD0 = L).
  - When Serial Programming Mode is used by a debugger or programming tool, that is connected to the board, make sure to set JP8 (JP8[CLOSED]: FLMD1 = GND).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN5 (GND), CN6 (+5.0 V) and CN7 (+3.3 V) are assembled on the board.
- If also the core supply voltage of 1.09 V will be supplied from an external power supply the connector CN8 (included in the package) has to be assembled on the pcb.

8.2.2 Jumper Indicators

The green jumper JP7 for FLMD0 must always be open for ‘normal’ (user mode and debug) operation of the device.

The red jumpers are related to the power supply configuration.
Following jumper symbols are used:

- : Jumper must not be set.
- 1 2 3: Jumper must be set in the indicated position
- 1 2 3: Jumper can be set to position [1-2] or position [2-3]
- 1 2 3: Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by
- a small circle near the jumper
- a square soldering pad.

8.2.3 Stand-Alone Operation with Single External Power Supply 3.3 V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is generated using the on-board voltage regulator IC3. All I/O ports can only use 3.3 V.

Table 8.1 Power supply connectors for single power supply 3.3 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Not connected	Jumpers in JP1 (VCC and VREF selection) are set to 3.3 V position
CN7	3.3 V	Connected, +3.3 V	
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT and JP2[5-6] = SHORT) Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

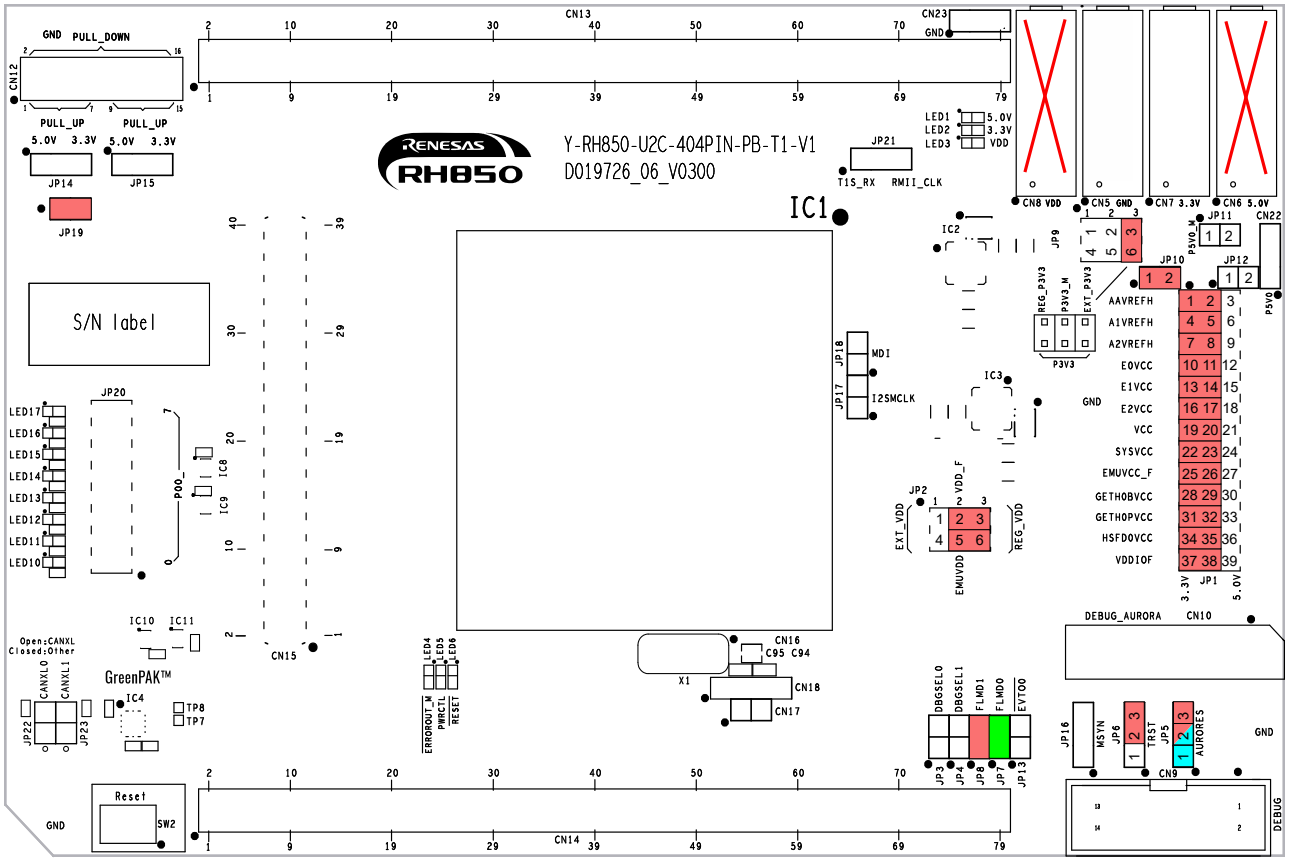


Figure 8.1 Stand-alone operation with 3.3 V external power supply

8.2.4 Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can only use 5.0 V.

Table 8.2 Power supply connectors for single power supply 5.0 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	
CN7	3.3 V	Not connected	3.3 V supply (P3V3) from on-board voltage regulator IC2 (JP9[1-4] = SHORT)
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT and JP2[5-6] = SHORT) Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

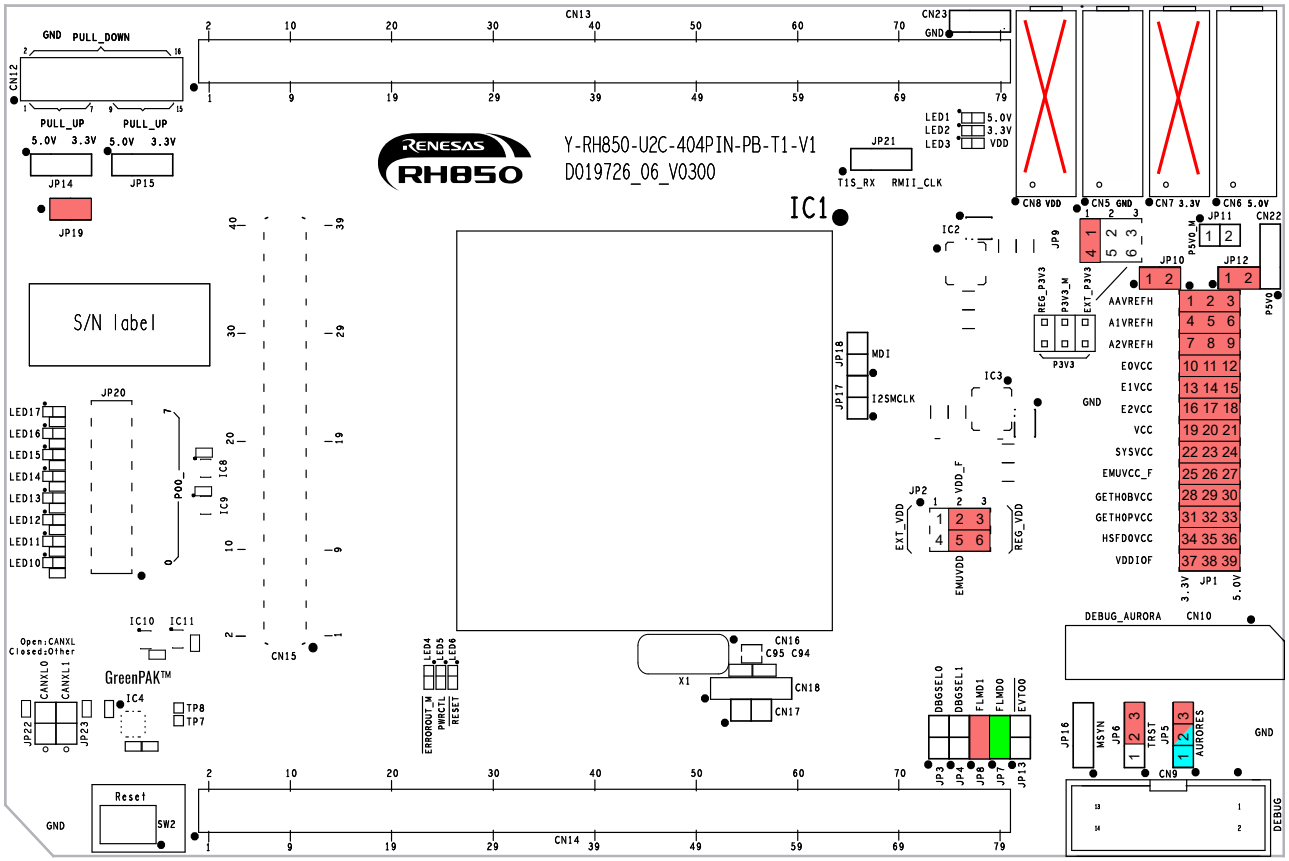


Figure 8.2 Stand-alone operation with 5.0 V external power supply

8.2.5 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.3 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. JP9[3-6] = SHORT: use Ext_P3V3 supply for 3.3 V supply. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	Connected, 1.09 V	JP2[1-2] = SHORT and JP2[4-5] = SHORT: use Ext_P1V09 for VDD voltage. Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

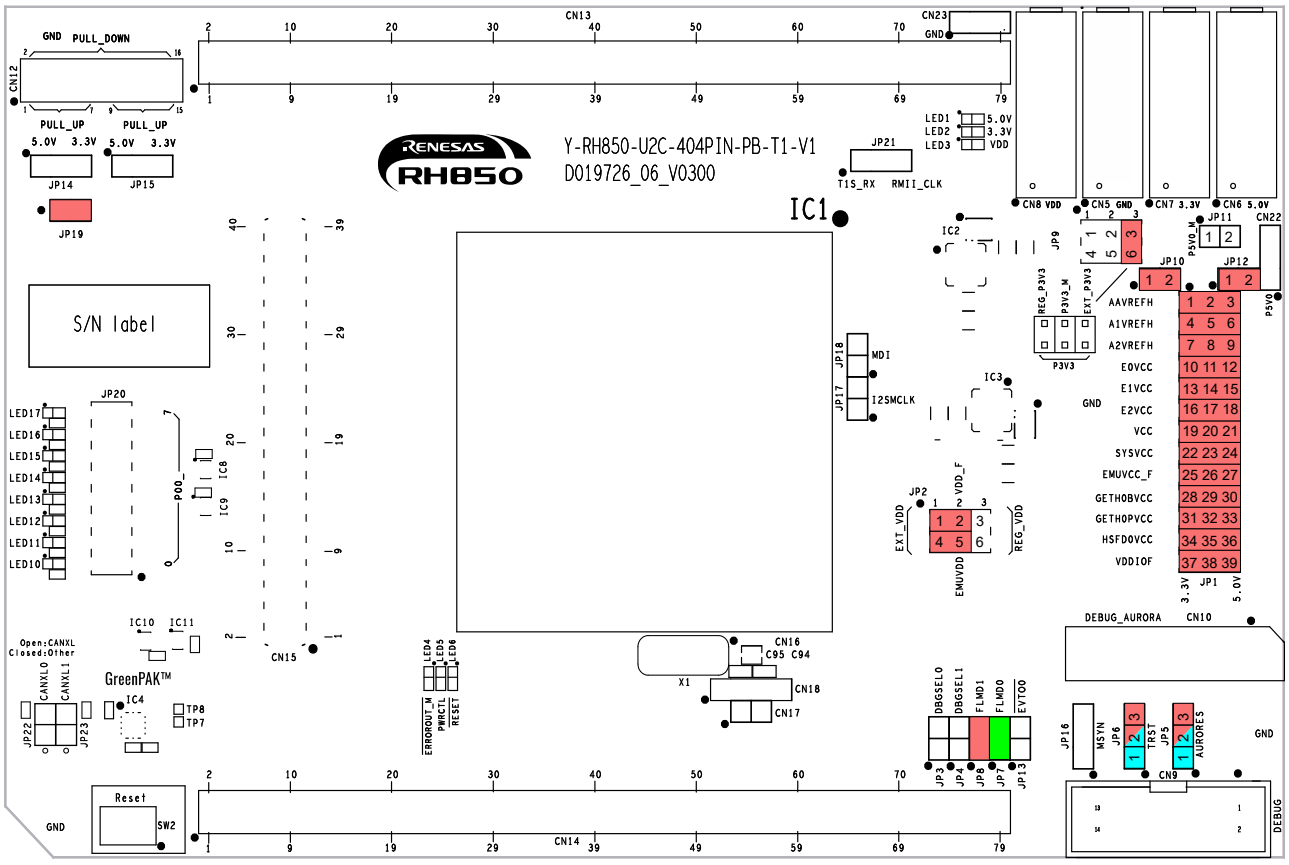


Figure 8.3 Stand-alone operation with all external power supplies

8.2.6 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

The jumpers JP11 (P5V0) and JP9 (P3V3) must be set to connect the main board supply voltages P5V0_M and P3V3_M to the piggyback board power supply rails P5V0 and P3V3.

Do not supply the 5.0 V (CN9) and 3.3 V (CN21) voltage directly to the piggyback board.

Table 8.4 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Not connected	
CN6	5.0 V	Not connected	Use jumper JP11[1-2] to connect the 5.0 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Not connected	Use jumper JP9[2-5] to connect the 3.3 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT and JP2[5-6] = SHORT). Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

This configuration still allows to utilize an external EXT_P1V09 voltage (connected to CN8) as the source for VDD voltage. In this case set JP2[1-2] and JP2[4-5].

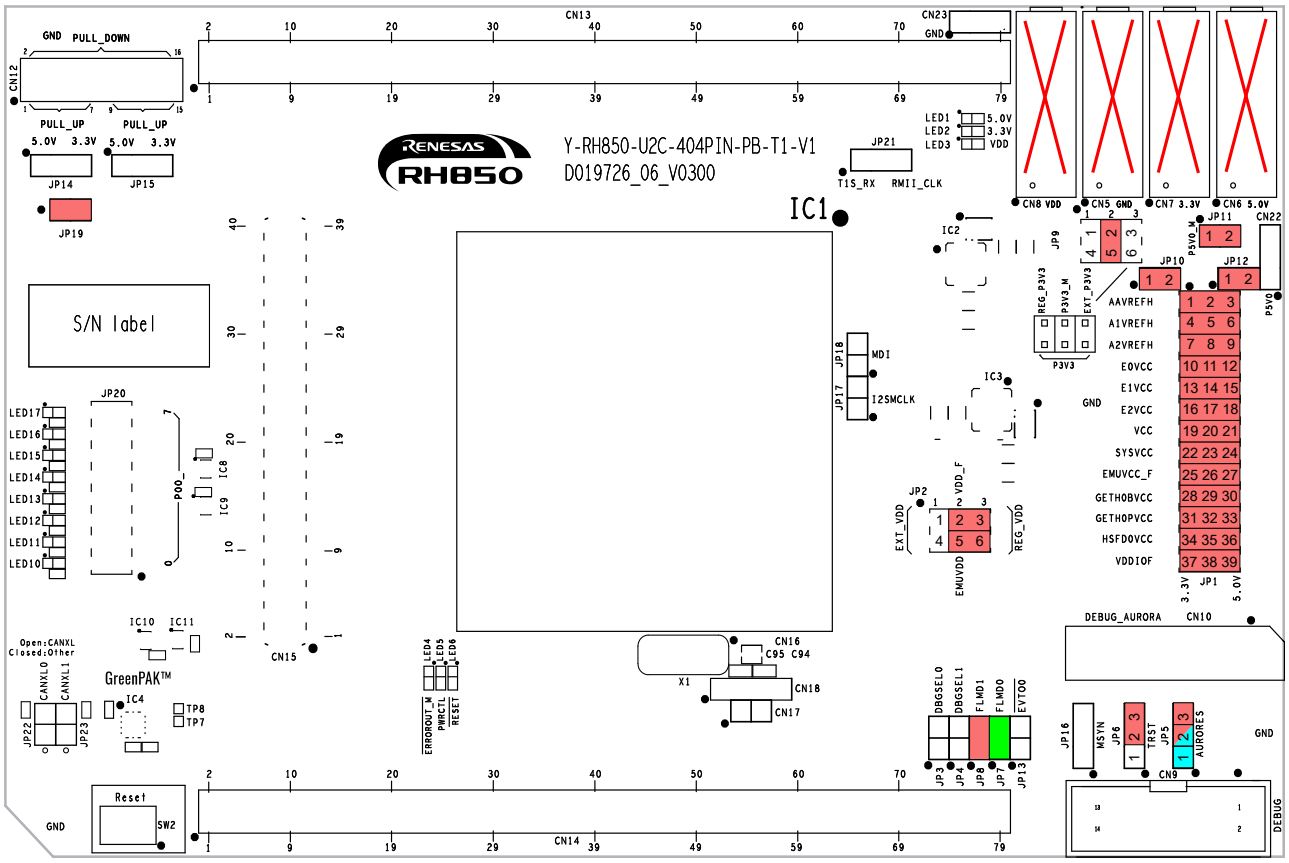


Figure 8.4 Main board operation without external power supply

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW2 into '5-6 ON' position, so that RESET is permanently asserted. Alternatively keep SW2 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW2 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 System State and RESET*

10. Mechanical Dimensions

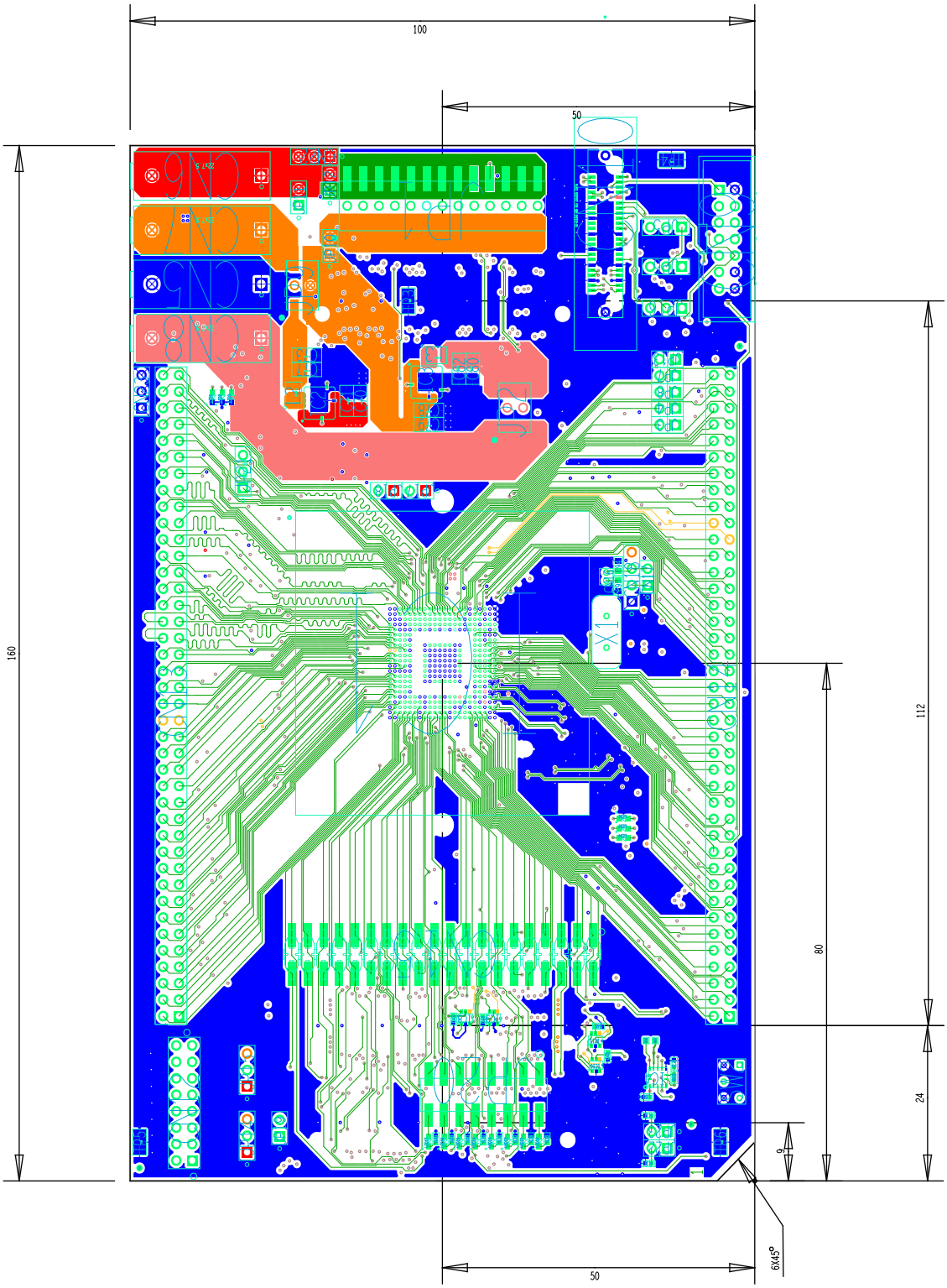


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is the sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C32, C37, C94, C95
- Connectors/sockets: CN16, CN19, CN20, CN21
- Oscillator: OSC1, X2

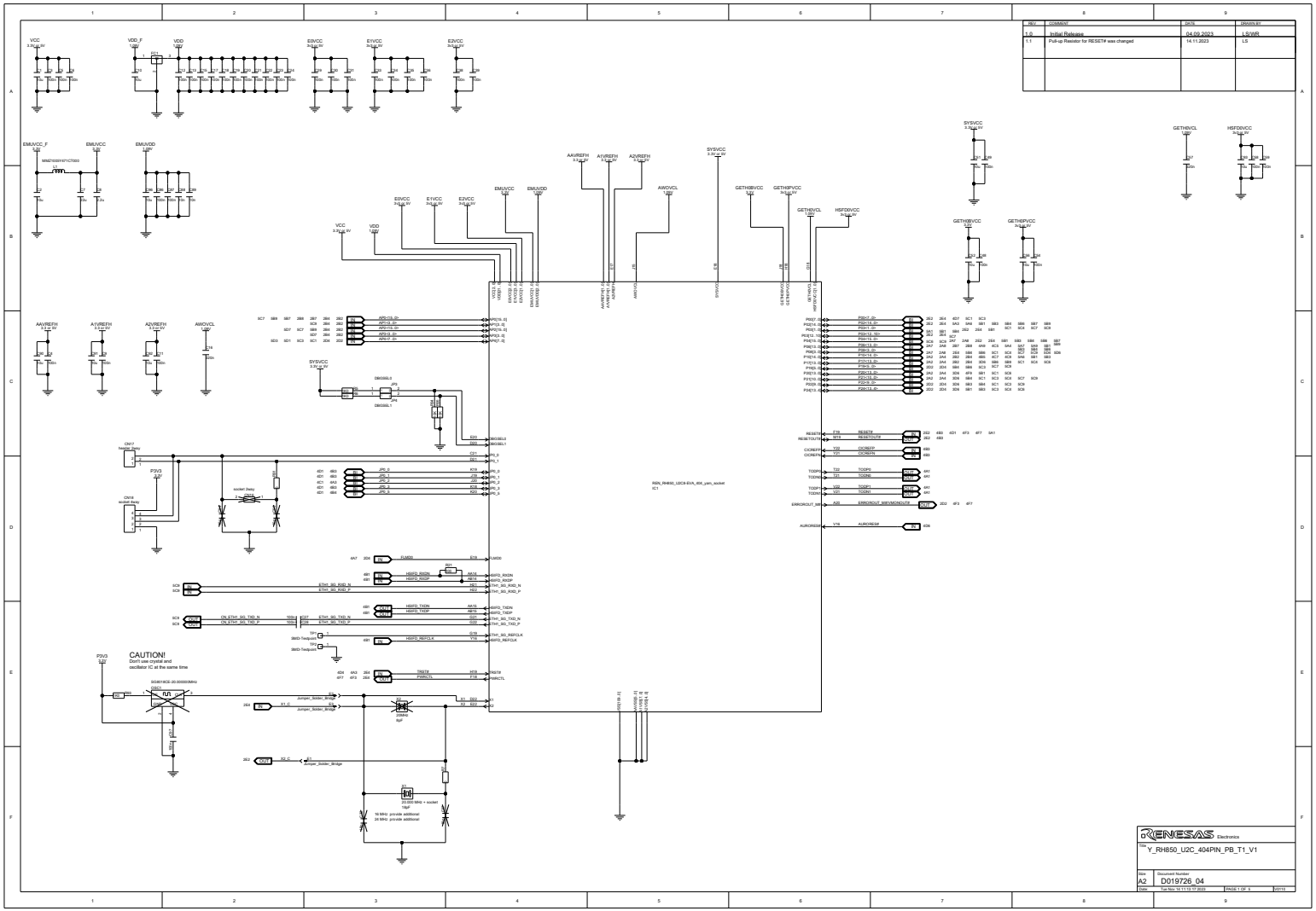
The above components are crossed out in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

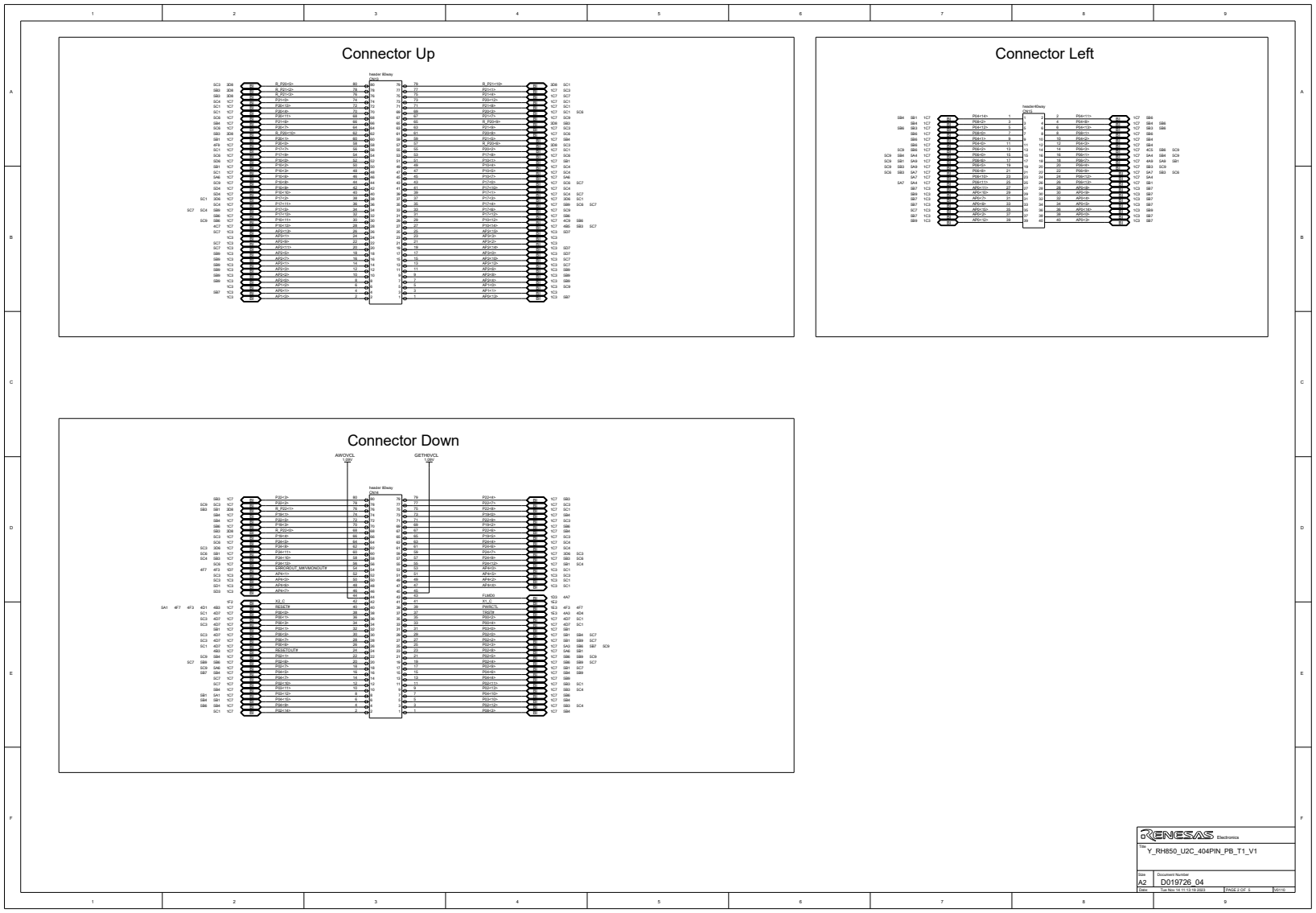
- 1 Hirschmann 4 mm power lab sockets, red for CN8
- Three resonators HC49 (8 / 16 / 24 MHz)
- 40 jumpers, 2.54 mm, black (board version D019726_06_V01)
  42 jumpers, 2.54 mm, black (board version D019726_06_V02)
  45 jumpers, 2.54 mm, black (board version D019726_06_V03 and later)

11.1 Board Version D019726_06_V01

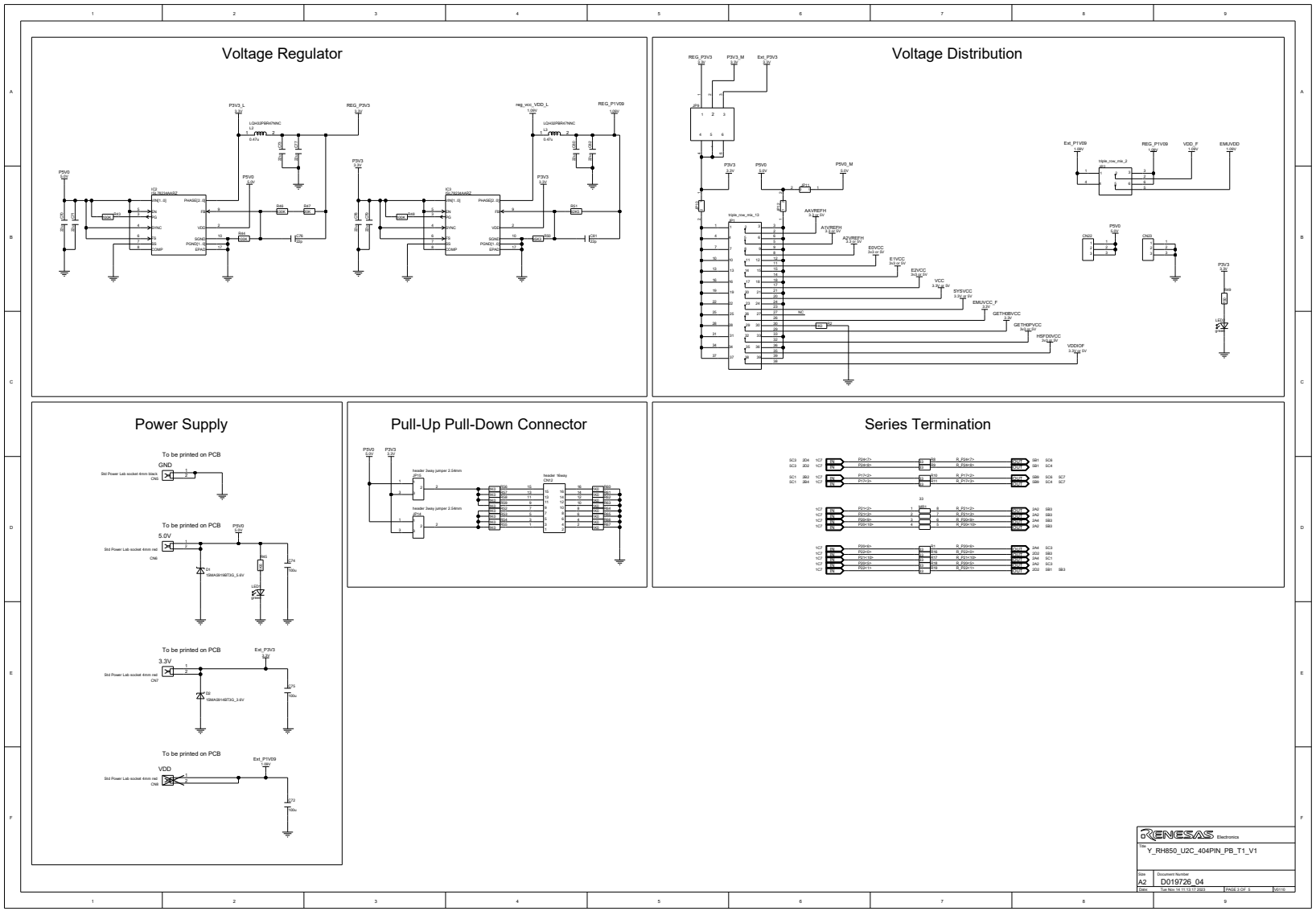
11.1.1 RH850/U2C



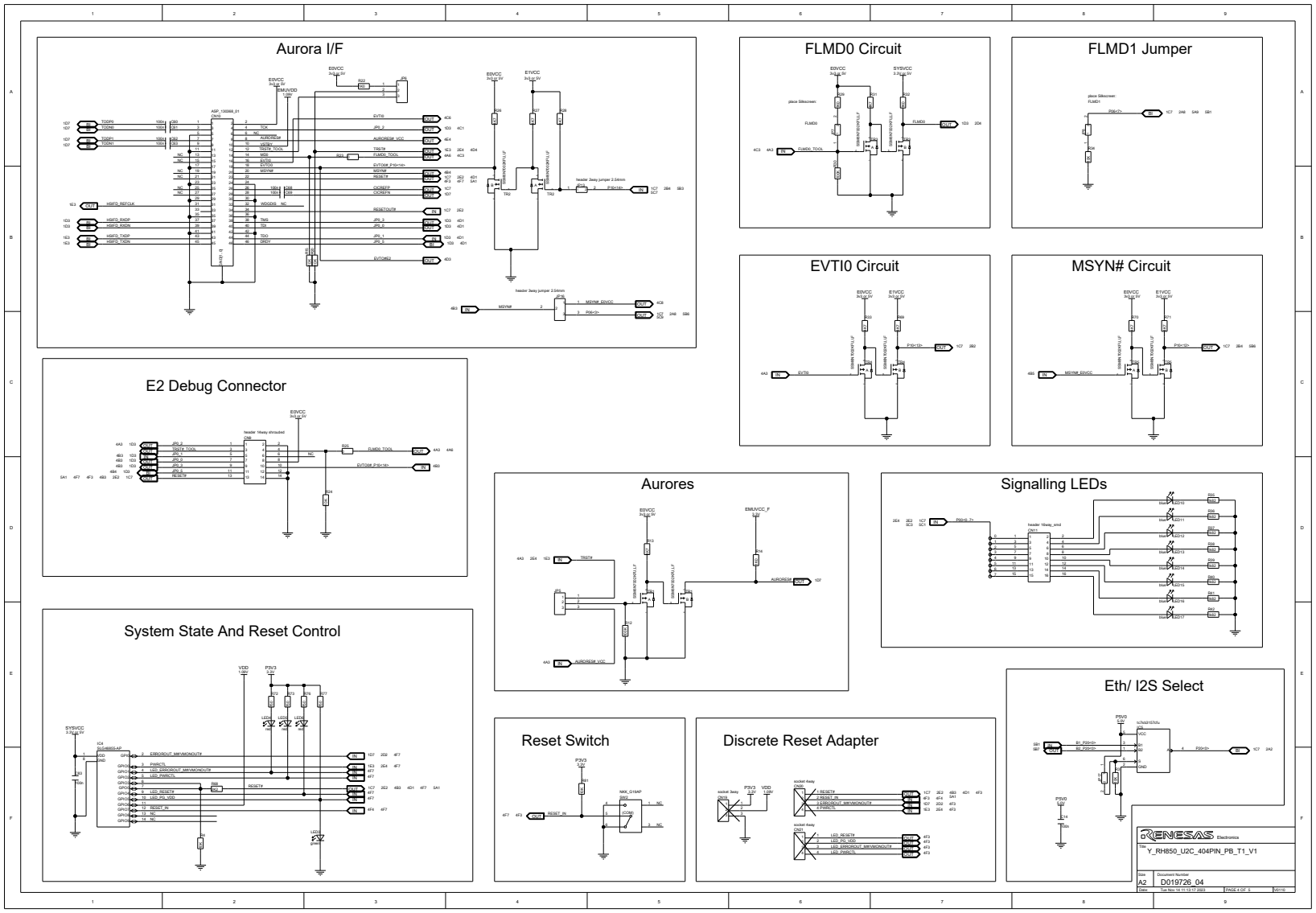
11.1.2 Breakout Connectors



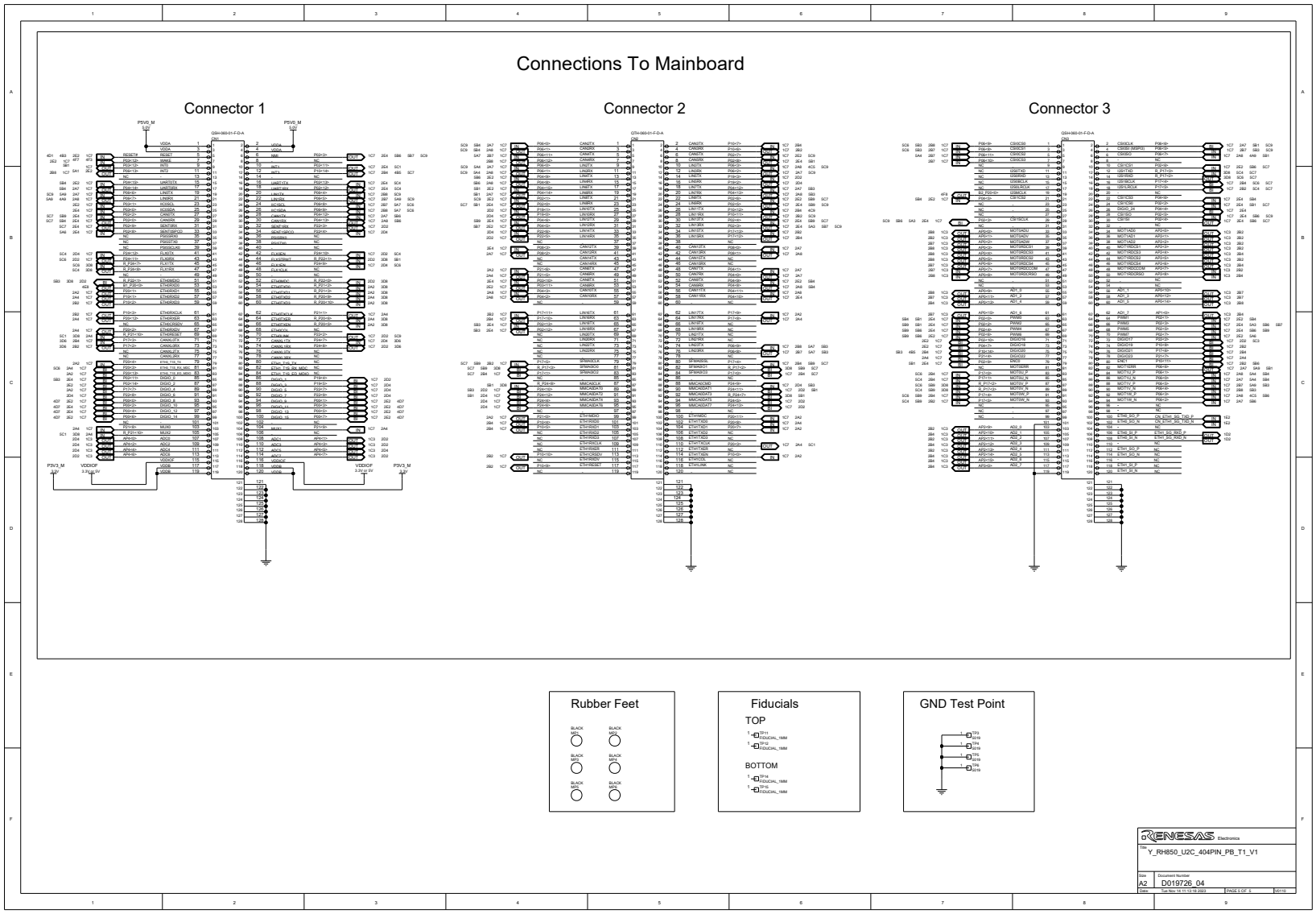
11.1.3 Power Supply



11.1.4 RH850 Configuration

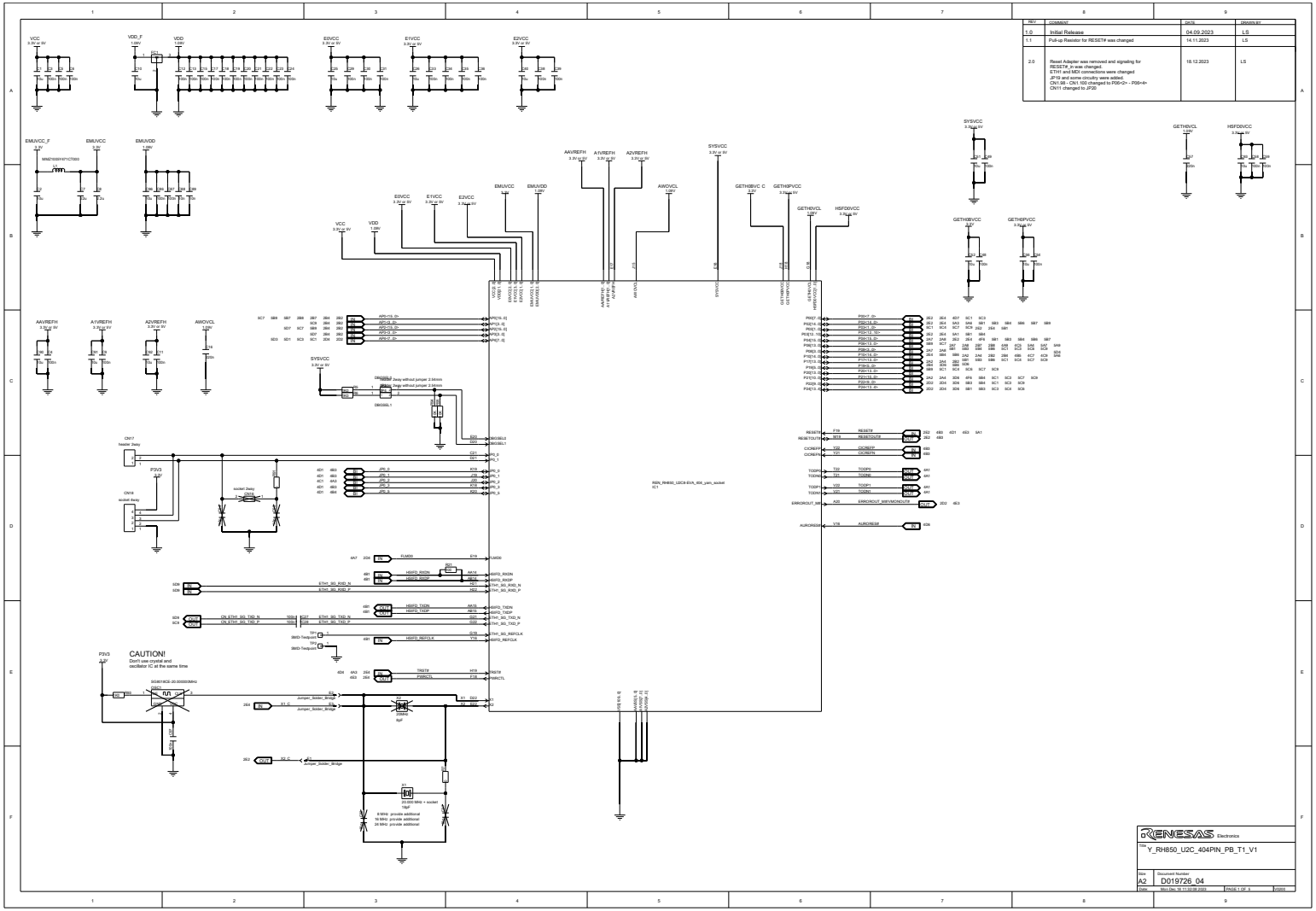


11.1.5 Main Board Connectors

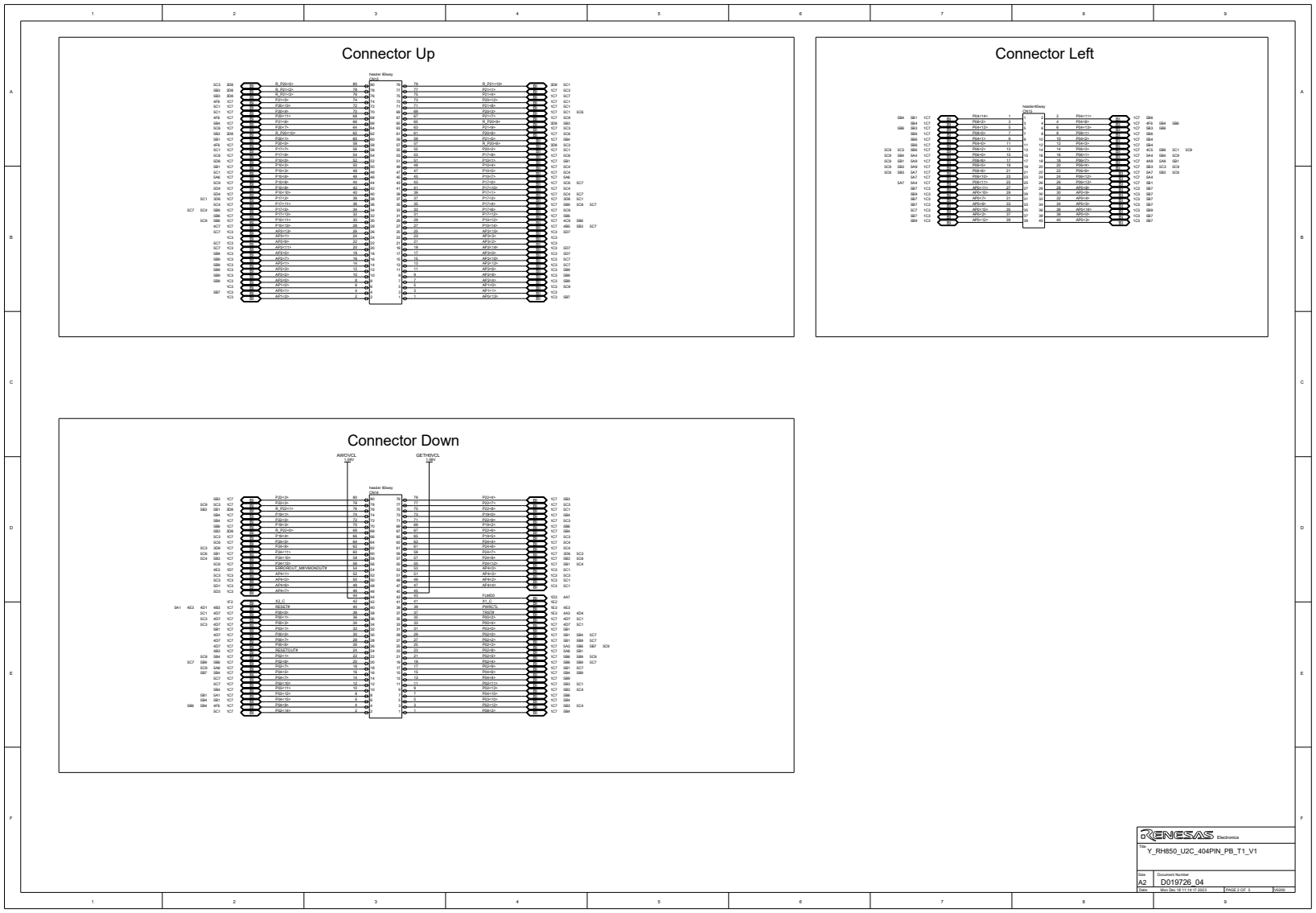


11.2 Board Version D019726_06_V02

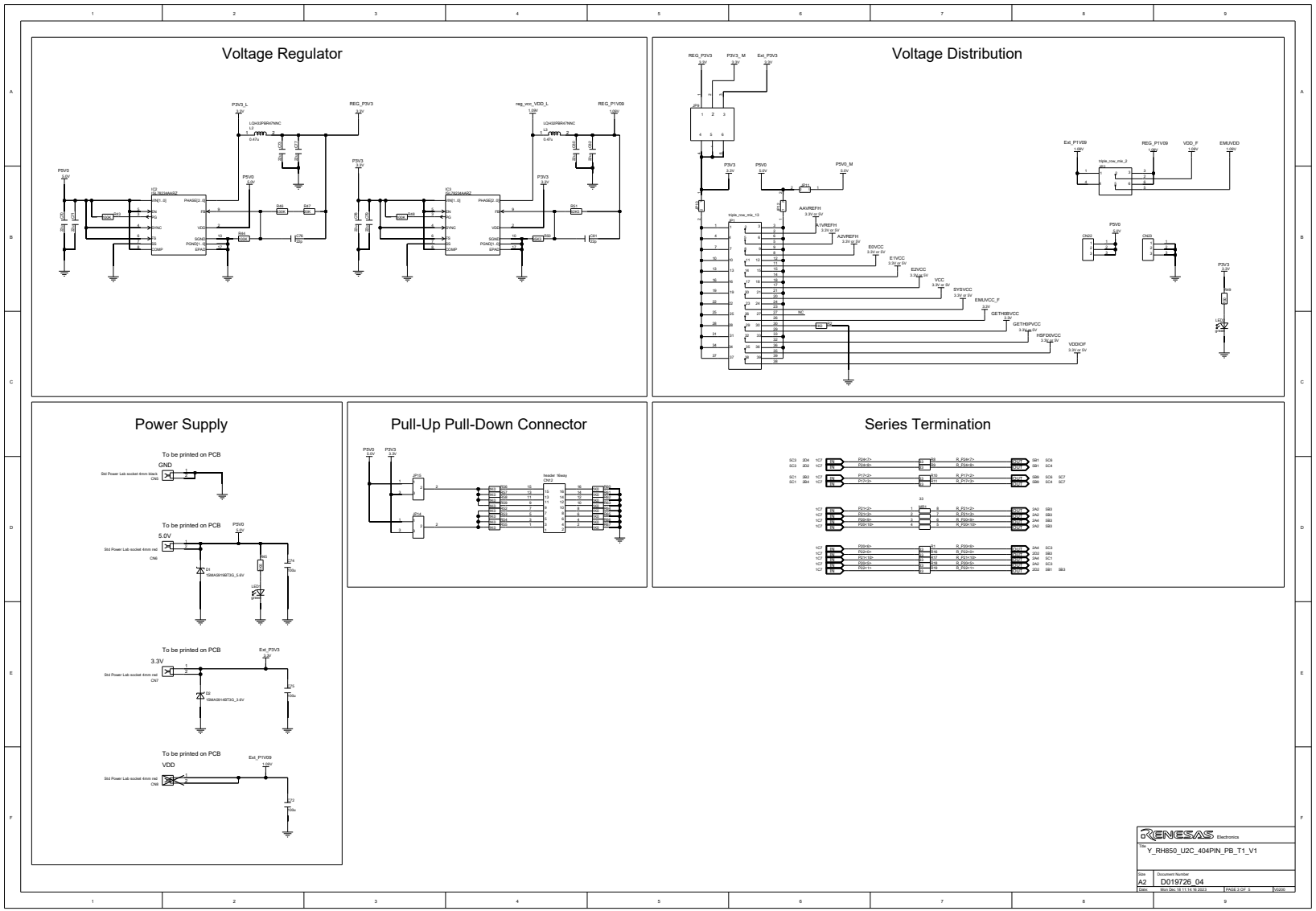
11.2.1 RH850/U2C



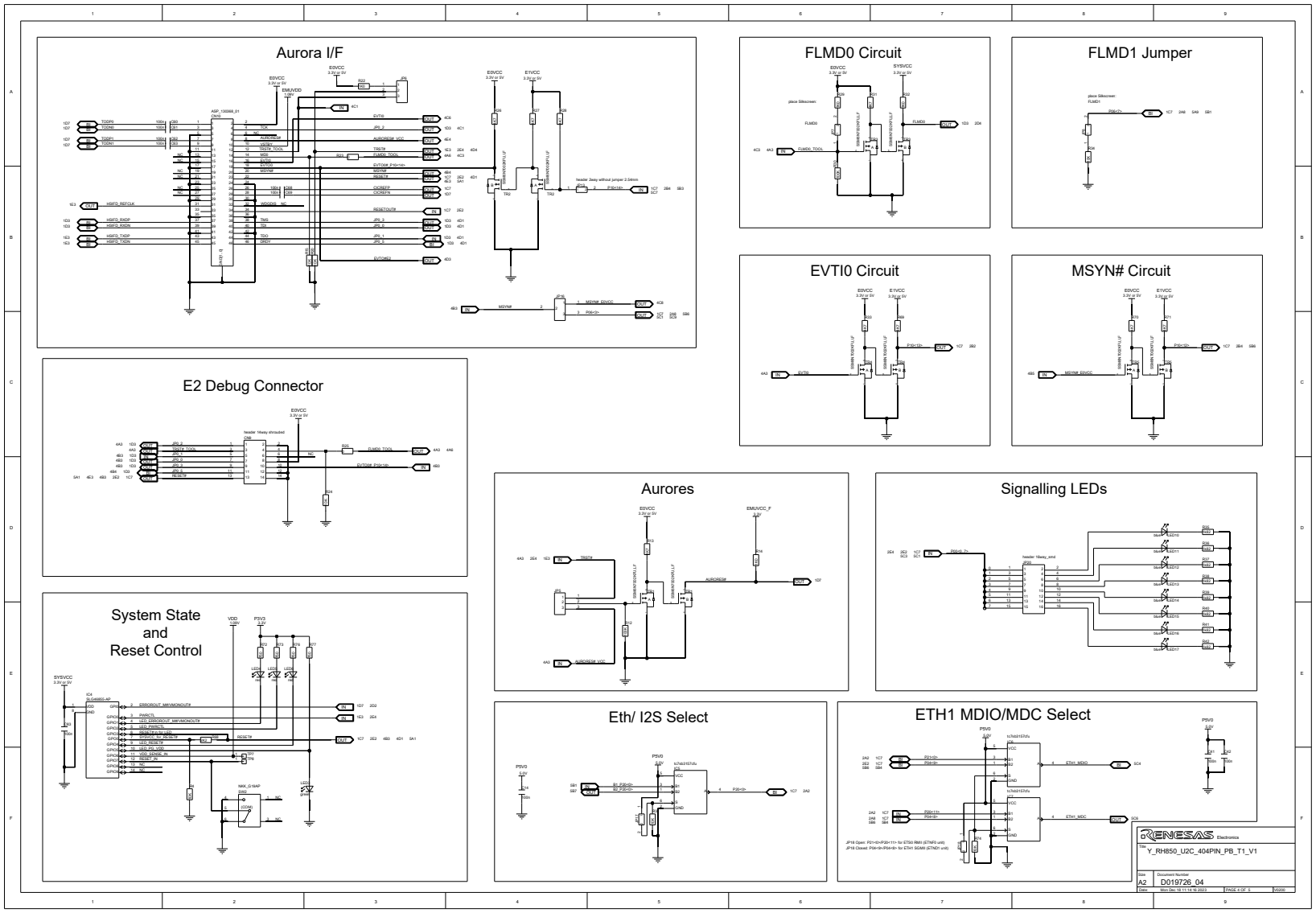
11.2.2 Breakout Connectors



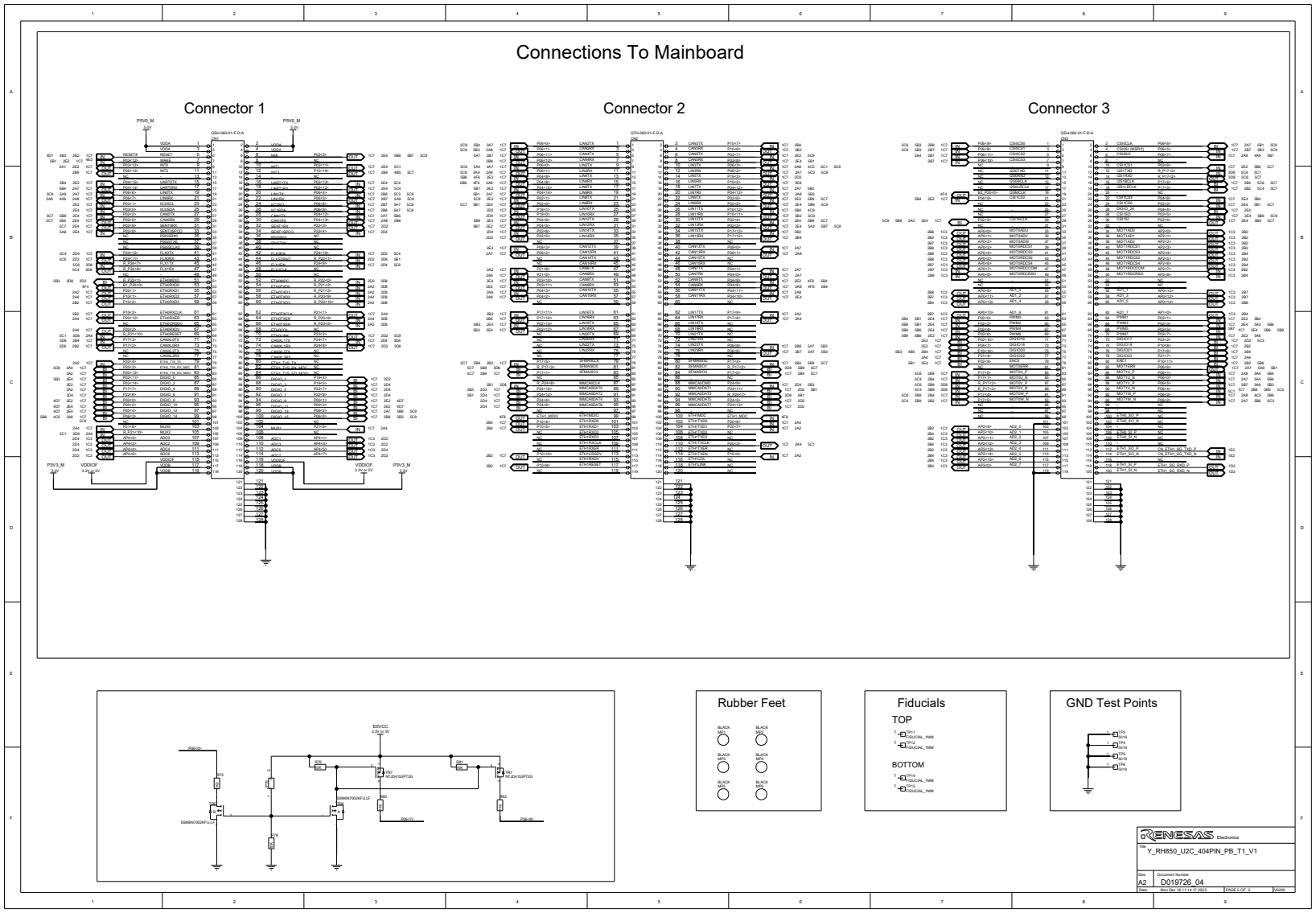
11.2.3 Power Supply



11.2.4 RH850 Configuration

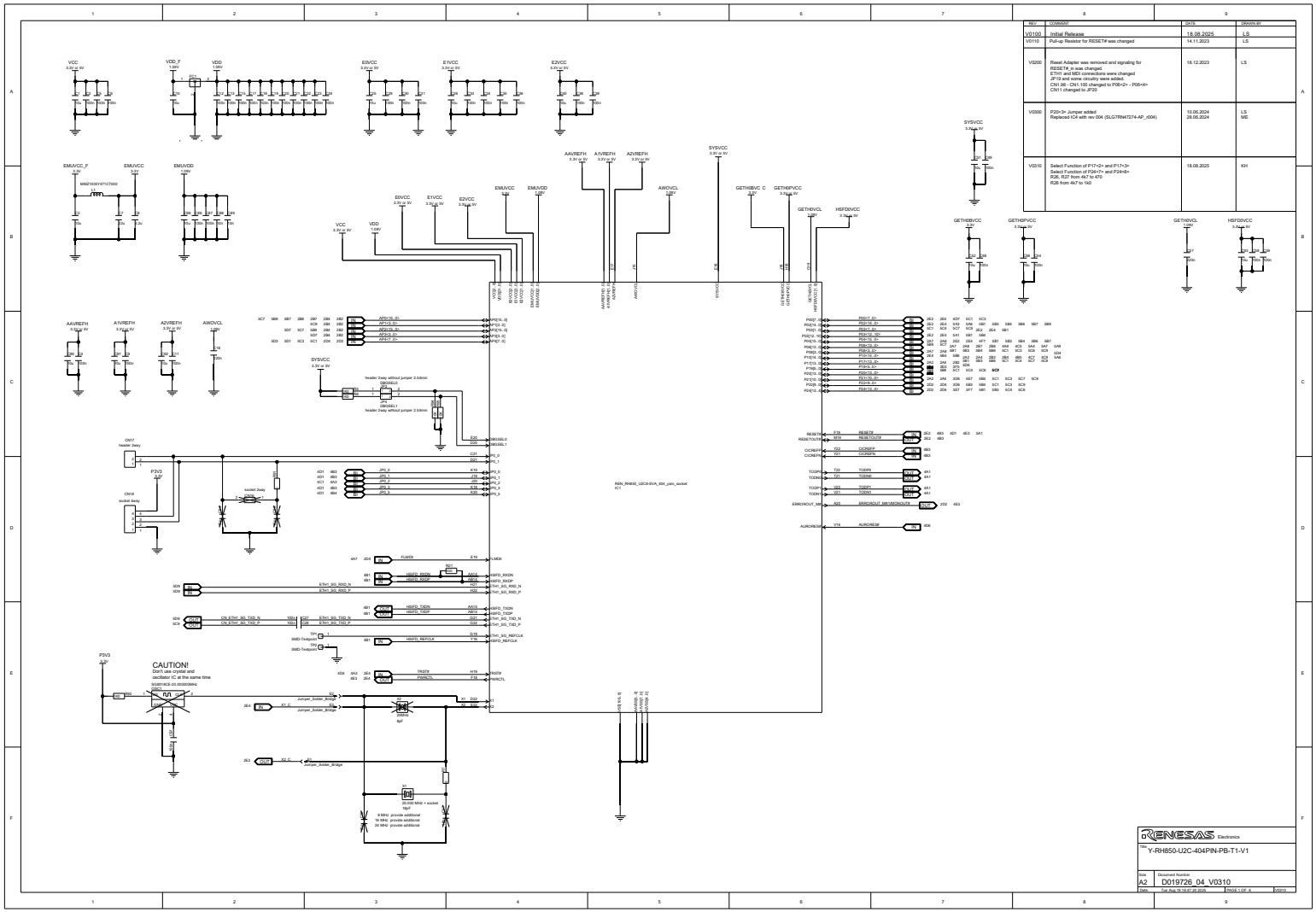


11.2.5 Main Board Connectors

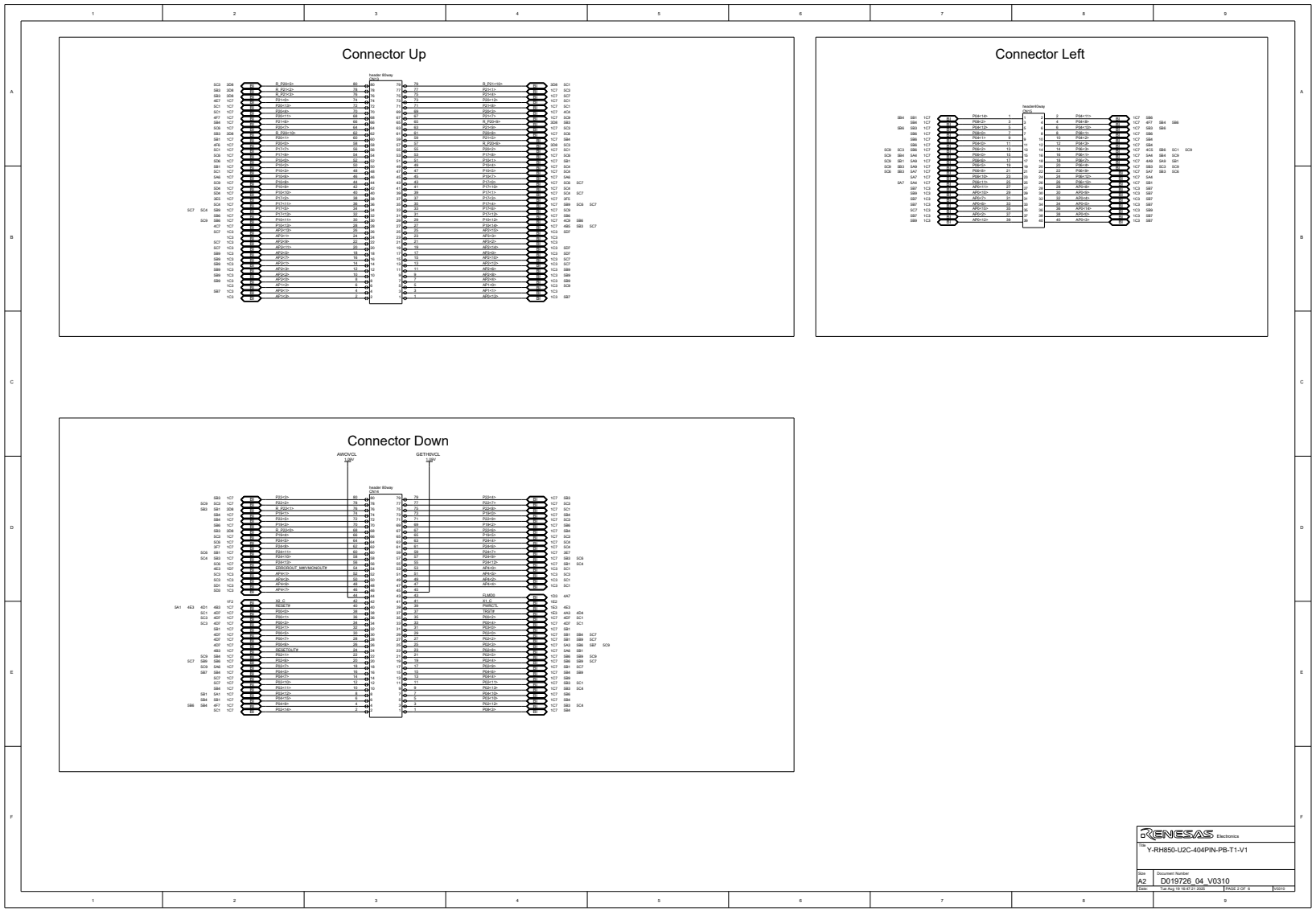


11.3 Board Version D019726_06_V03

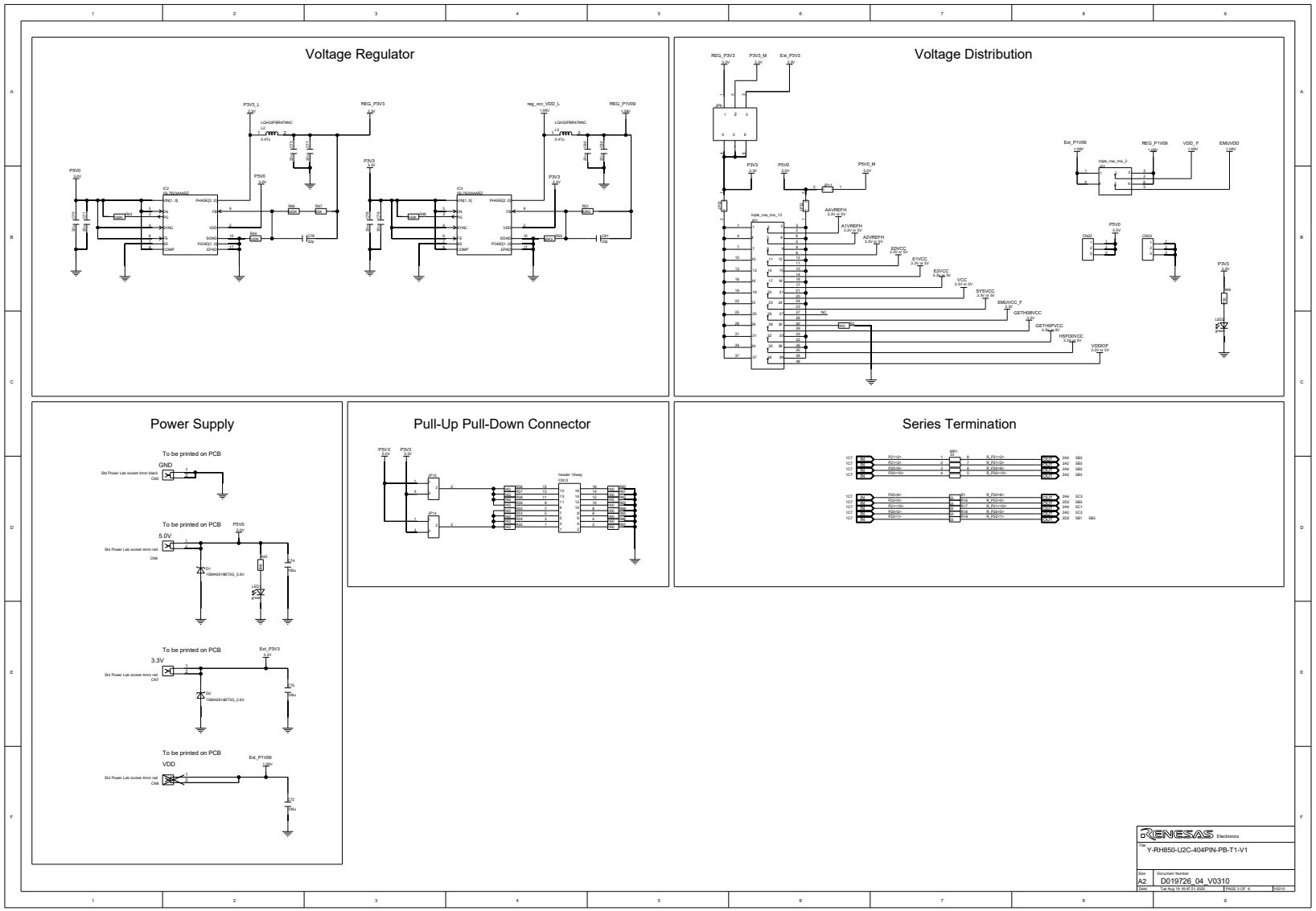
11.3.1 RH850/U2C



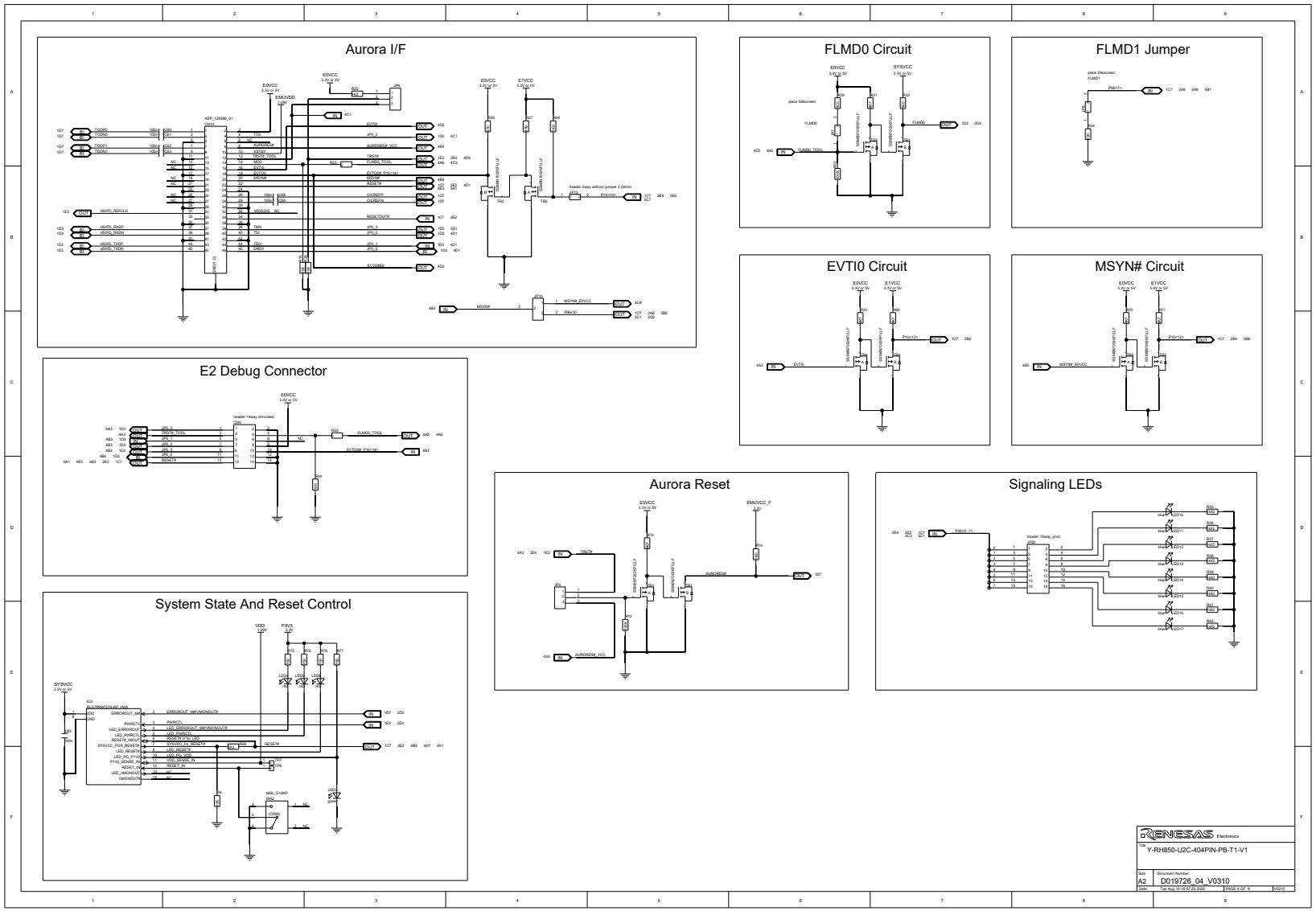
11.3.2 Breakout Connectors



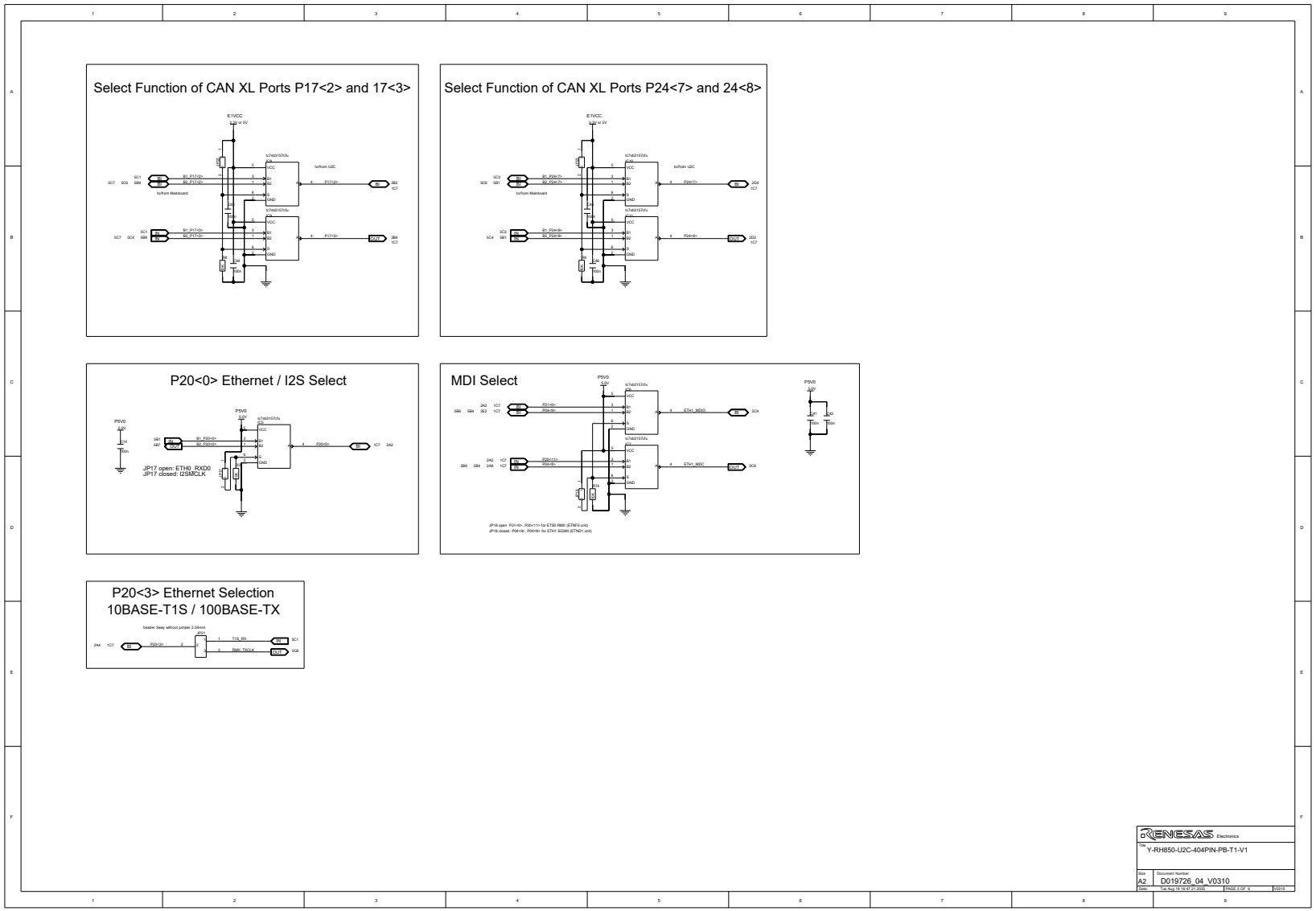
11.3.3 Power Supply



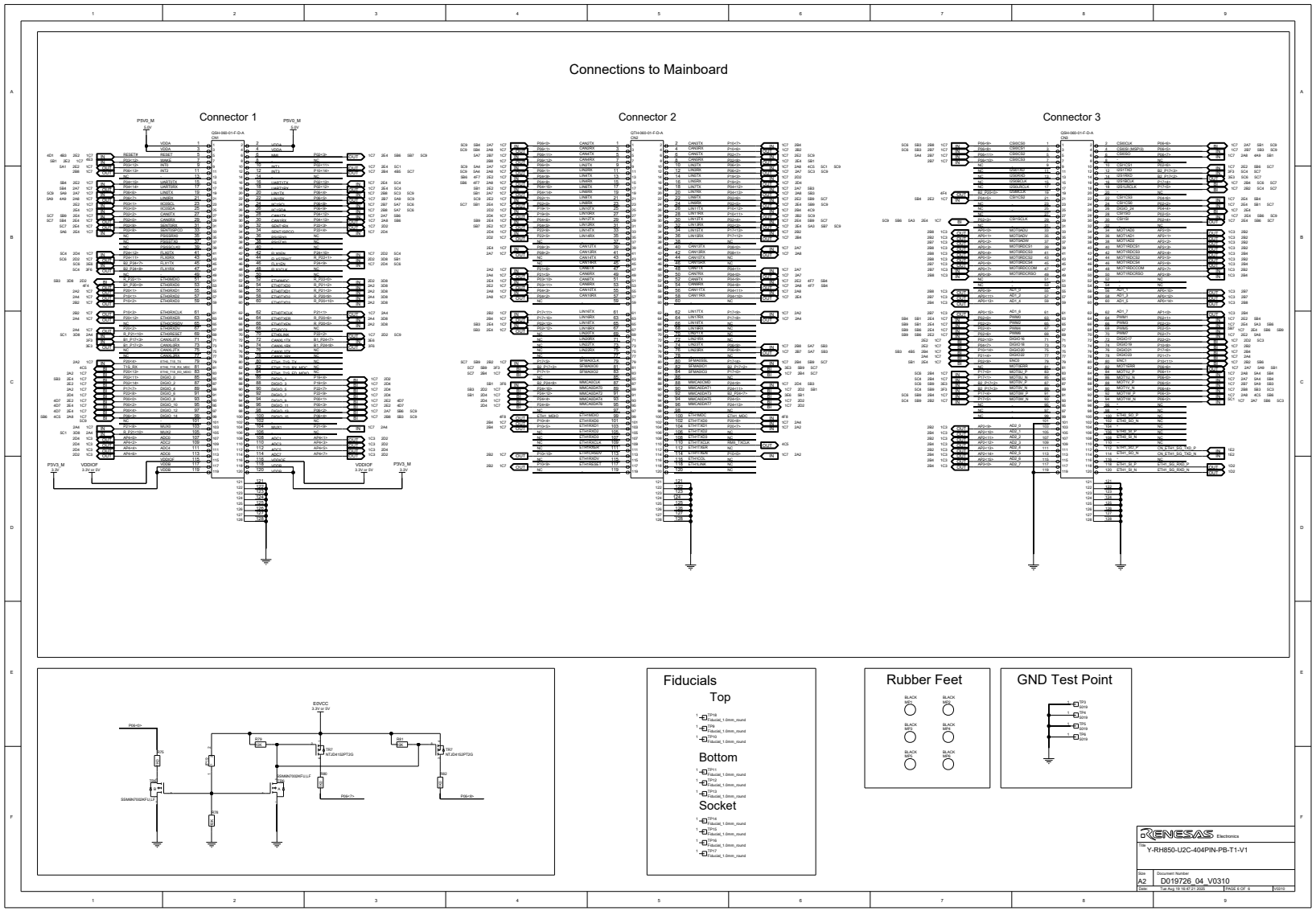
11.3.4 RH850 Configuration



11.3.5 CAN XL and Ethernet Configurations



11.3.6 Main Board Connectors



Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2023-11-15	–	Initial release
V1.01	2023-12-15	*33*	Added information about board modification near IC4 in chapter *6.2 System State and RESET.*
		55 - 58	Changed the recommended settings for jumper JP6 and JP8 in the jumper graphics in chapters *8.2.3 - 8.2.6.*
V1.02	2024-05-08	*8*	Added information about board versions in *1.4 Piggyback Board Versions.*
		19	Updated jumper descriptions in *2.1 Jumper Overview.*
		32, 54	Added explanation for FLMD1 setting in Serial Programming Mode in *6.1 Operation Mode Selection* and *8.2 Configuration Examples.*
V2.00	2026-01-23	***Error! Bookmark not defined.***	Corrected number of jumpers in *Table 1.1 Package Components for the Y-RH850-U2C-404PIN-PB-T1-V1*
			Updated device list in *Table 1.4 Type names for suitable devices.*
		16	Updated GreenPAK IC (IC4) to version V0400 in chapter *6.2 System State and RESET.*
		33	Added jumper JP21 for port P20_3 Ethernet function selection *6.5 Ethernet Control Port P20_3.*
		35	Added comment about Ethernet units being used with different JP18 jumper settings in chapter *6.4 Ethernet 1 Control Ports MDIO / MDC* and chapter *11.3.4 RH850 Configuration.*
		35, 76	

RH850/U2C 404pin Piggyback Board V1 User's Manual: Piggyback Board

Publication Date: Rev.2.00 January 23, 2026

Published by: Renesas Electronics Corporation

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