User's Manual

32

RH850 Evaluation Platform

RH850/U2C 292pin

User's Manual: Piggyback Board

Y-RH850-U2C-292PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2C 292pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2C 292pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document active low signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g. the reset pin is named RESETZ or RESET#.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2C-292PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2C-292PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2C-292PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2C-292PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2C-292PIN-PB-T1-V1

Item	Description	Quantity
D020145	RH850/U2C 292pin piggyback board	1
D020147	Documentation CD	1
D010816-24	China RoHS document	1
D010818-24	WEEE+CE document	1
D020145-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	31 (board version D020145_06_V01) 34 (board version D020145_06_V02.1) 37 (board version D020145_06_V03) 39 (board version D020145_06_V0400)
Red Hirschmann 4 mm power lab socket	In the bag	1
Resonator, HC49, 8 / 16 / 24 MHz	In the bag	3

Note

Please keep the Y-RH850-U2C-292PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2C-292PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with power supply from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.09 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage Selection*.
- 14-pin connector for E2 emulator
- Support JTAG/LPD debug interface
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 8/16/20/24 MHz Crystal Resonator
- Eight general purpose signalling LEDs
- Jumpers for device mode selection and other configuration options
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the piggyback board are available:

Table 1.2 Y-RH850-U2C-292PIN-PB-T1-V1 board versions

Board Version	Schematic Version
D020145_06_V01	D020145_04_V0121
D020145_06_V02.1	D020145_04_V0210
D020145_06_V03	D020145_04_V0302
D020145_06_V0400	D020145_04_V0400

Table 1.3 on the next page lists all modifications that have been implemented in different board revisions.

Table 1.3 Differences between board versions V01, V02.1, V03 and V0400

Item	Modified Function	Detailed Description of Changes	D020145_06_V01	D020145_06_V02.1	D020145_06_V03	D020145_06_V0400
1	Pull-down resistor on RESET# signal input to IC4	A pull-down resistor has been added to the RESET# signal input.	The pull-down resistor R5 has been connected manually.	The pull-down resistor R5 is part of the board design.		
2	Reset signal inputs	Reset Adapter was removed and signalling for RESET#_IN was changed.	Connectors CN19 – CN21 could be used to input external signals for Reset sources.	Connectors CN19 – CN21 have been removed.		
3	Core power supply selection for RH850/U2C4 and RH850/U2C8	RH850/U2C4 and RH850/U2C8 differ in some power supply pins. The different voltages can be selected using jumper JP3.	The circuit implemented in board revision D020145_06_V01 does not work correctly, so a small board has been added manually to fix this. The circuit diagram includes already the functions of this board.	The fixed circuit has been implemented in the board design.		
4	Ethernet signals	Make signal connection for ETH1MDIO and ETH1MDC more flexible	Signal connections fixed: ETH1MDIO = P21_0 ETH1MDC = P20_11	Signal connection flexible, selectable by jumper JP18: ETH1MDIO = P21_0 or P04_9 ETH1MDC = P20_11 or P04_8		
5	Ethernet 1 signal port connection on connector CN3	Changed pins on CN3 (will be implemented in next version)	CN_ETH1_SG_TXD_P – CN3[100] CN_ETH1_SG_TXD_N – CN3[102] ETH1_SG_RXD_P – CN3[106] ETH1_SG_RXD_N – CN3[108]	CN_ETH1_SG_TXD_P – CN3[112] CN_ETH1_SG_TXD_N – CN3[114] ETH1_SG_RXD_P – CN3[118] ETH1_SG_RXD_N – CN3[120]		
6	Jumper for signalling LED	Renamed jumper.	Jumper is named CN11.	Jumper is named JP20.		
7	Production test	Added circuit for production tests.	---	JP19 and some circuitries were added.		
8	Jumper to add support for Ethernet T1S	Switch functionality of port P20_3 to support MII and T1S interface.	---	---	Added jumper JP5.	
9	Updated revision of GreenPAK IC (IC4)	Improved functionality of GreenPAK IC .	SLG46855-AP	SLG7RN47274-APTR	SLG7RN47274-AP_r004	
10	CAN XL port selection	Added multiplexer to connect CAN XL ports to main board connector CN1.	Connected to CAN XL ports on CN1 in parallel to other functions like I2S, SFMA, motor control signals.			Added multiplexer to connect the CAN XL ports directly to connector CN1 without interference from other connections.

Table 1.3 Differences between board versions V01, V02.1, V03 and V0400 (cont'd)

Item	Modified Function	Detailed Description of Changes	D020145_06_V01	D020145_06_V02.1	D020145_06_V03	D020145_06_V0400
11	Core voltage power supply	RH850/U2C4 devices use eVR or DPS mode for core power supply. Added options to adjust the hardware to the use of the on-chip voltage regulators or an external core voltage supply.	VDD circuit designed for external core voltage supply (DPS).			PCB includes options so customers can rework the board easily to work with eVR devices or DPS devices. Refer to chapter *3.3.2* for details.

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

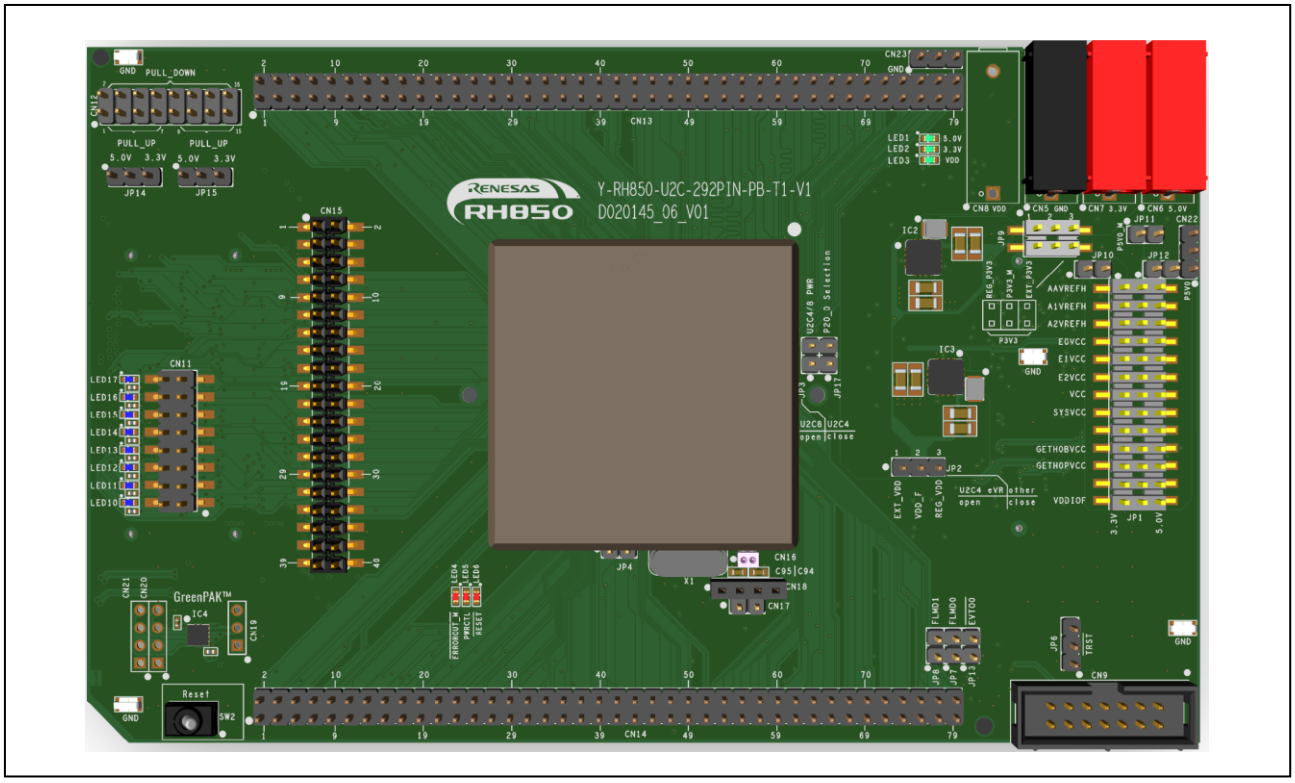


Figure 1.1 Piggyback board top view of board version D020145_06_V01

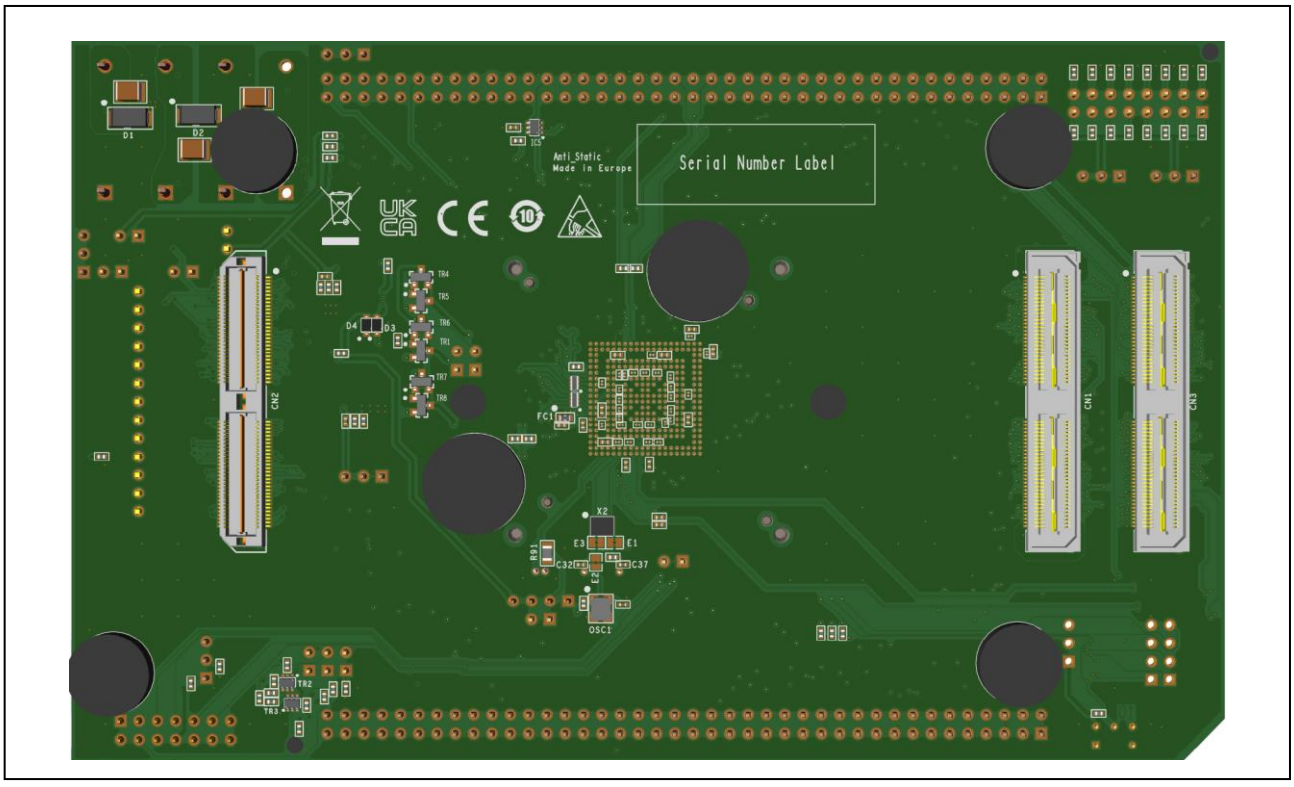


Figure 1.2 Piggyback board bottom view of board version D020145_06_V01

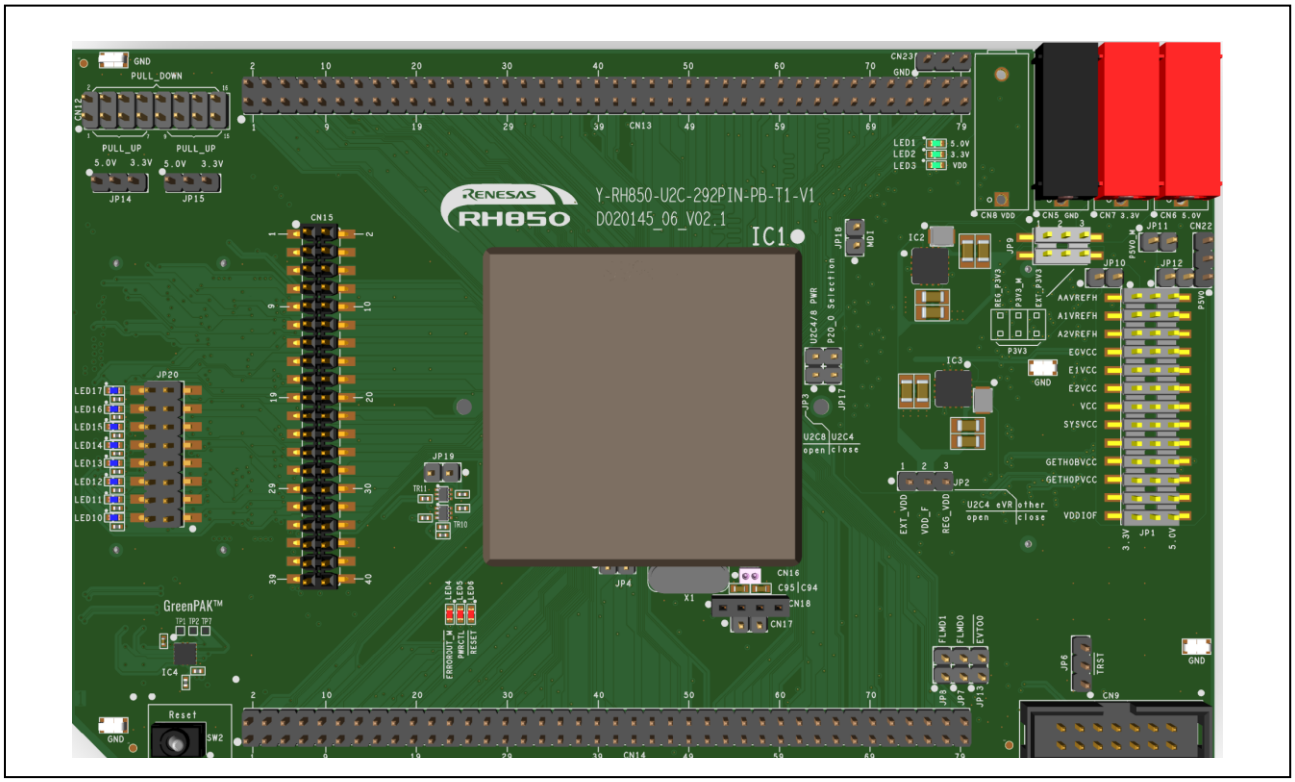


Figure 1.3 Piggyback board top view of board version D020145_06_V02.1

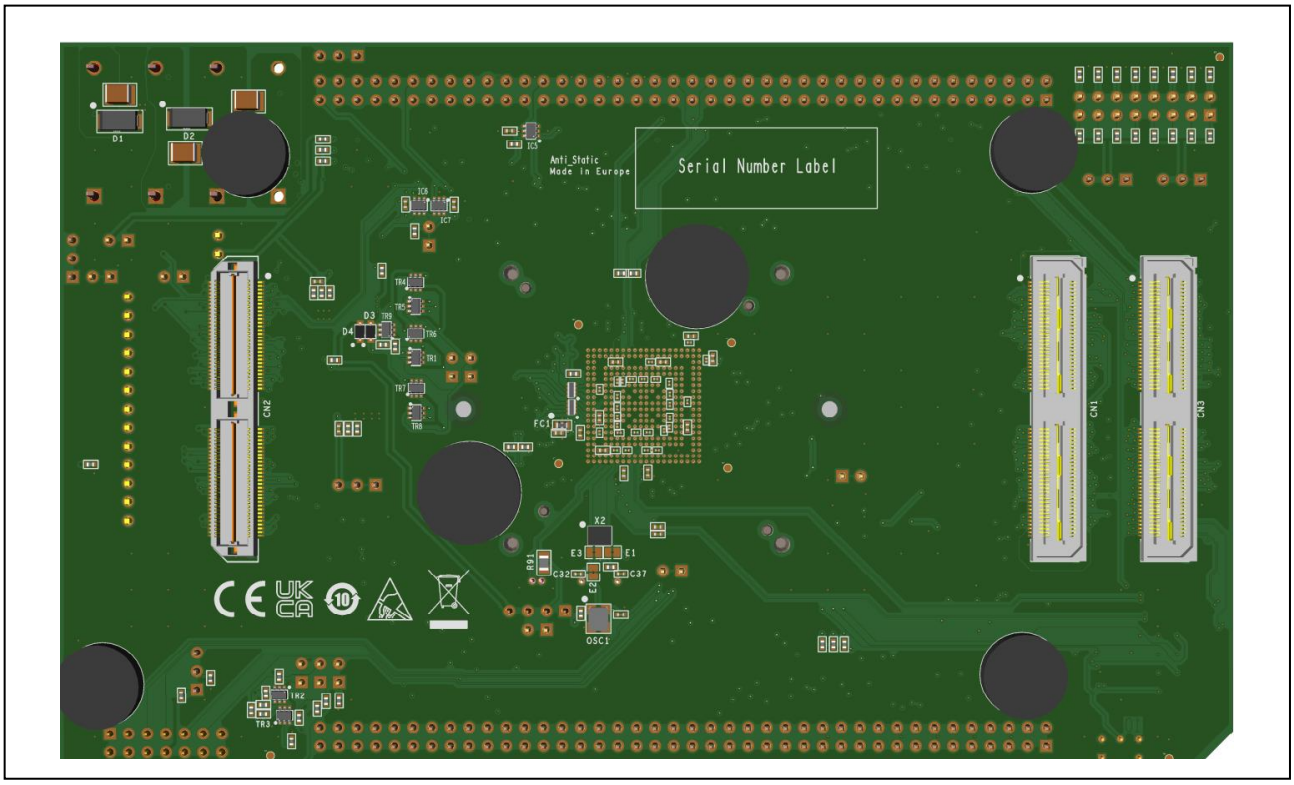


Figure 1.4 Piggyback board bottom view of board version D020145_06_V02.1

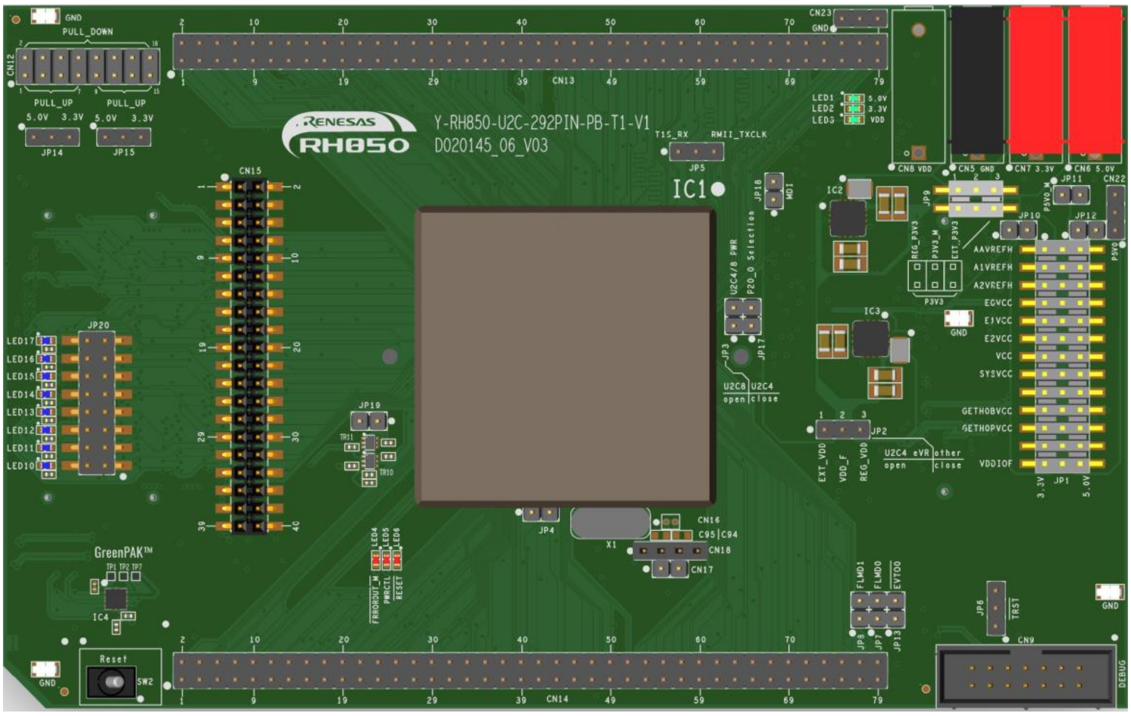


Figure 1.5 Piggyback board top view of board version D020145_06_V03

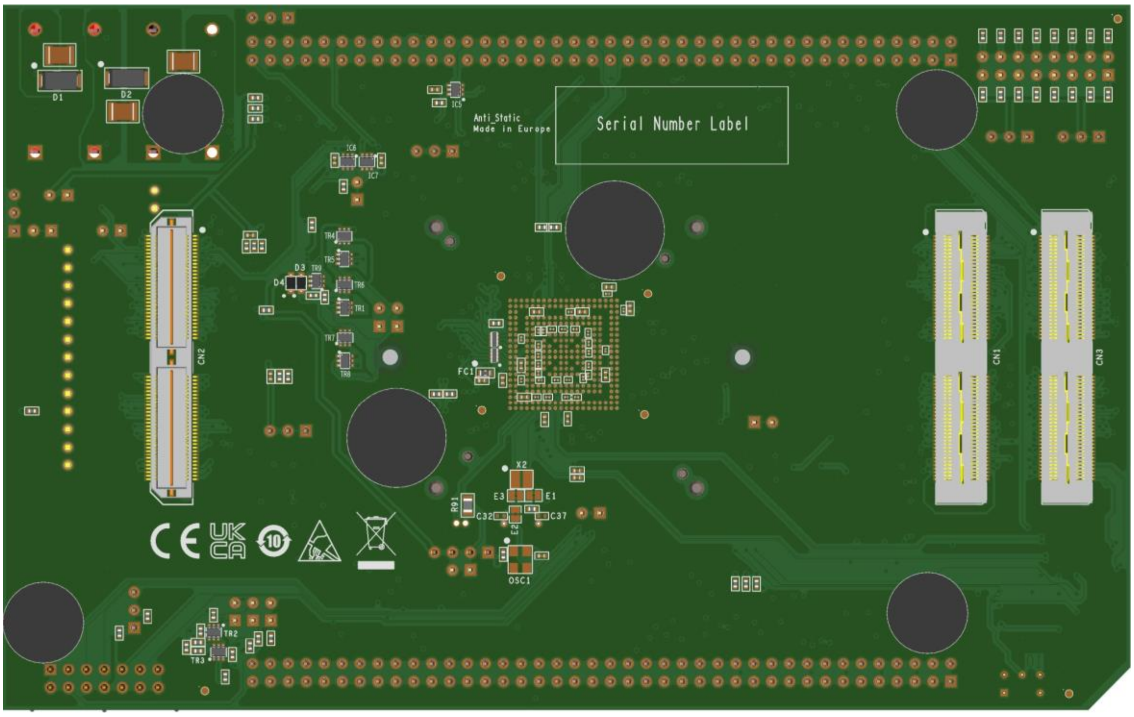


Figure 1.6 Piggyback board bottom view of board version D020145_06_V03

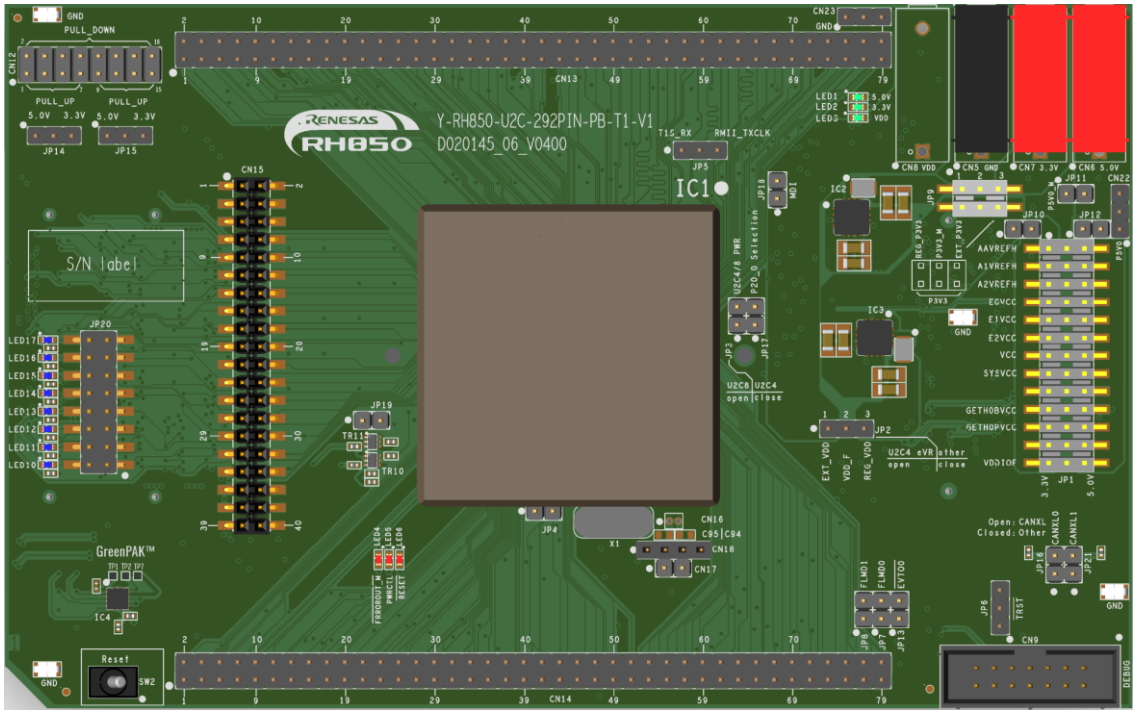


Figure 1.7 Piggyback board top view of board version D020145_06_V0400

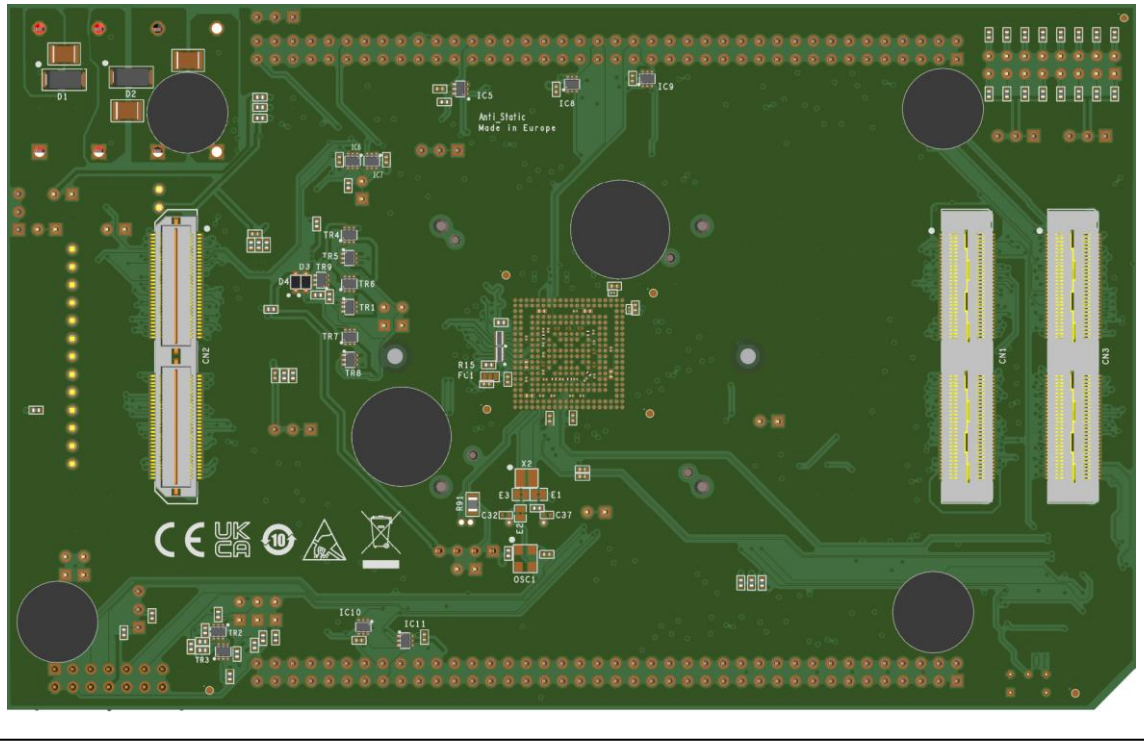


Figure 1.8 Piggyback board bottom view of board version D020145_06_V0400

Following figures provide the drawing of top and bottom views of the piggyback board.

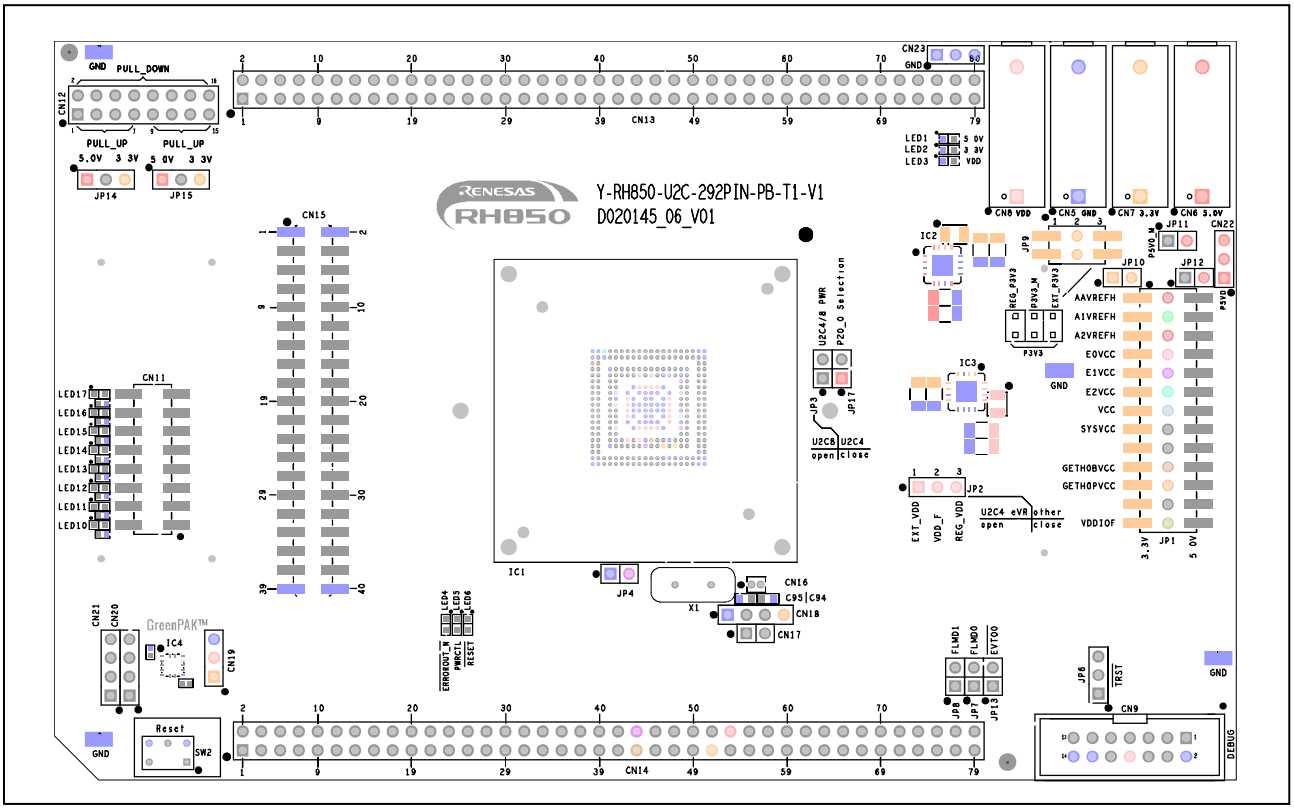


Figure 1.9 Piggyback board top view of board version D020145_06_V01

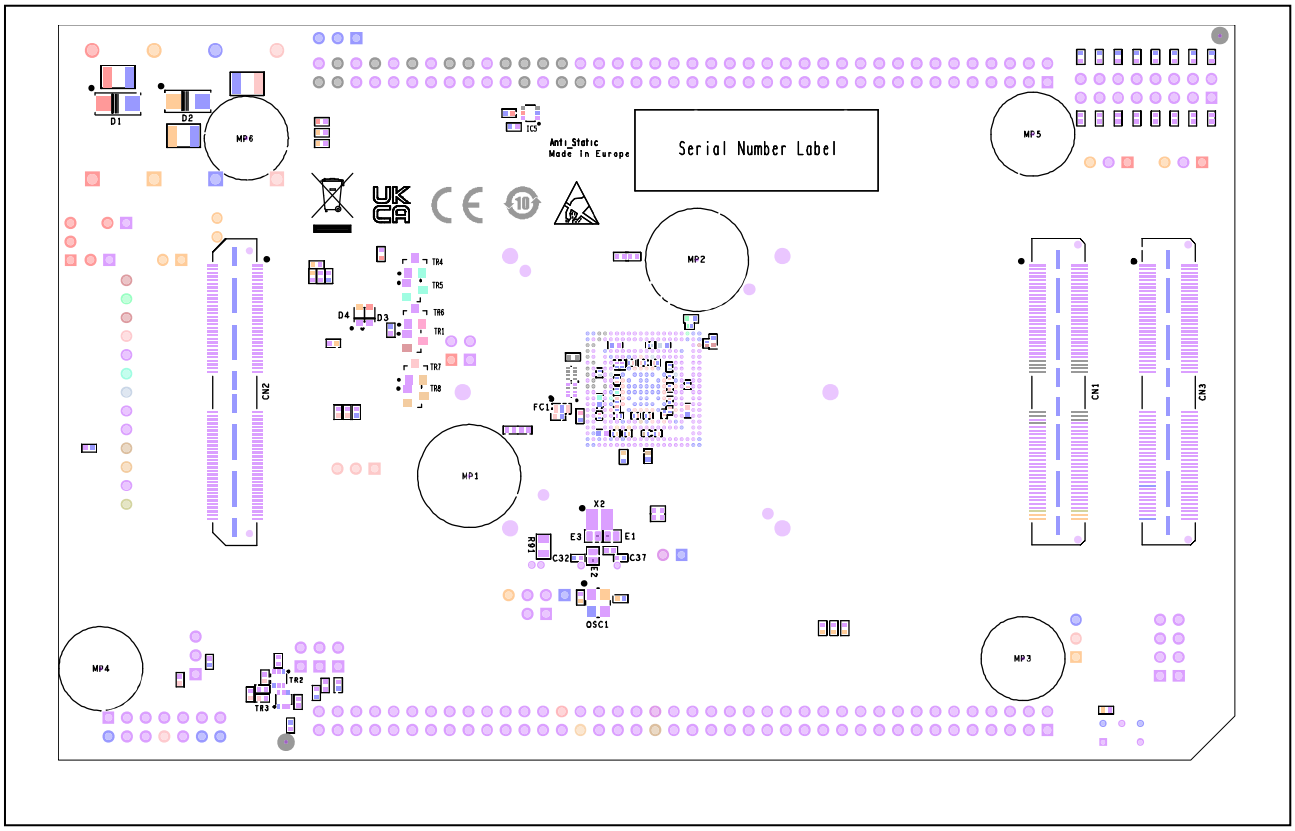


Figure 1.10 Piggyback board bottom view of board version D020145_06_V01

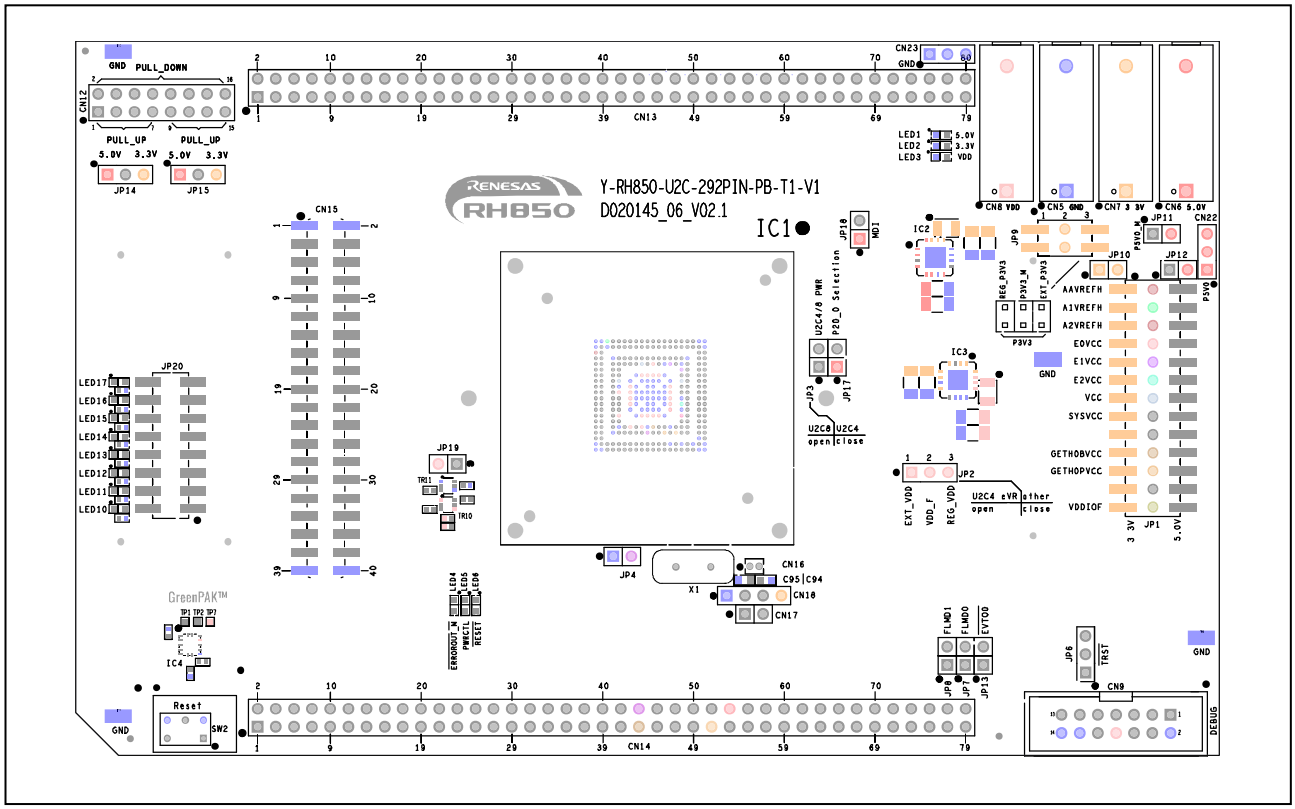


Figure 1.11 Piggyback board top view of board version D020145_06_V02.1

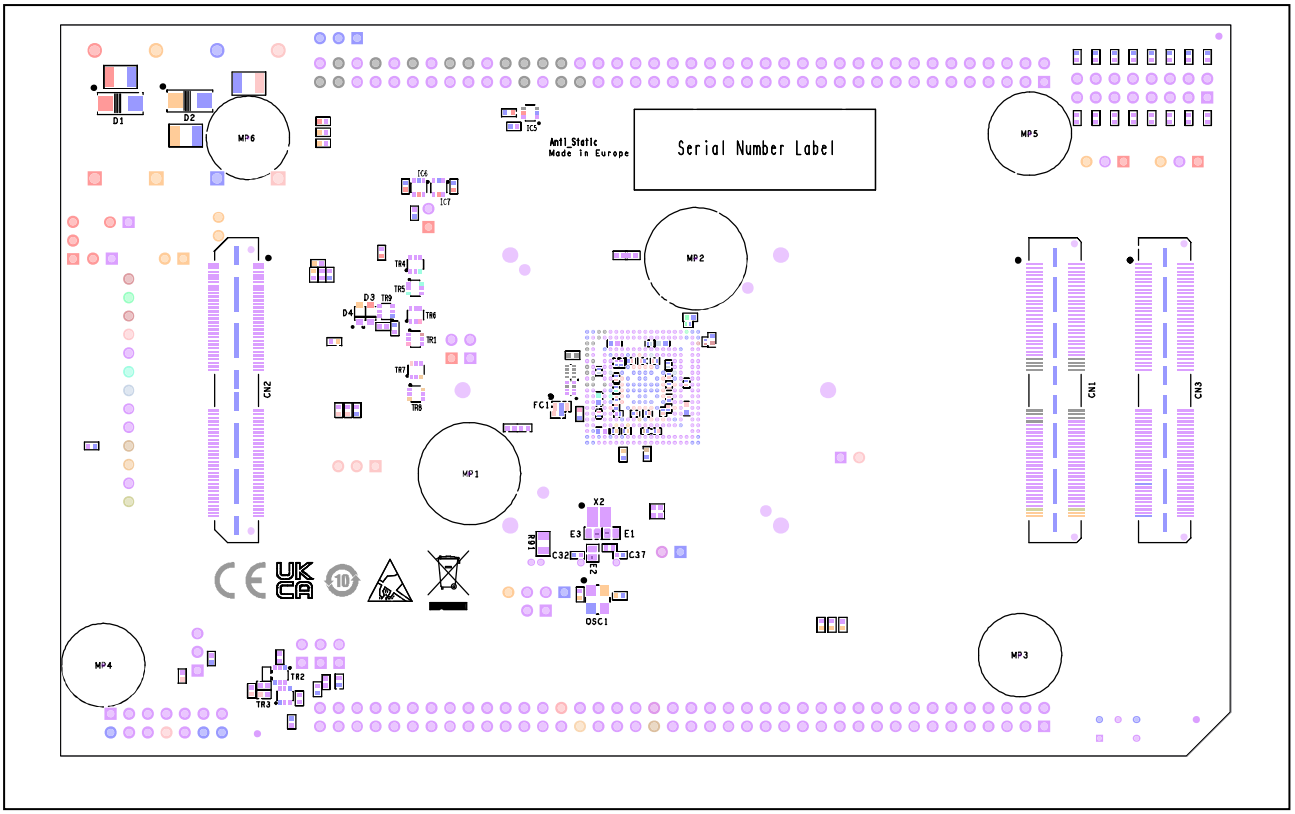


Figure 1.12 Piggyback board bottom view of board version D020145_06_V02.1

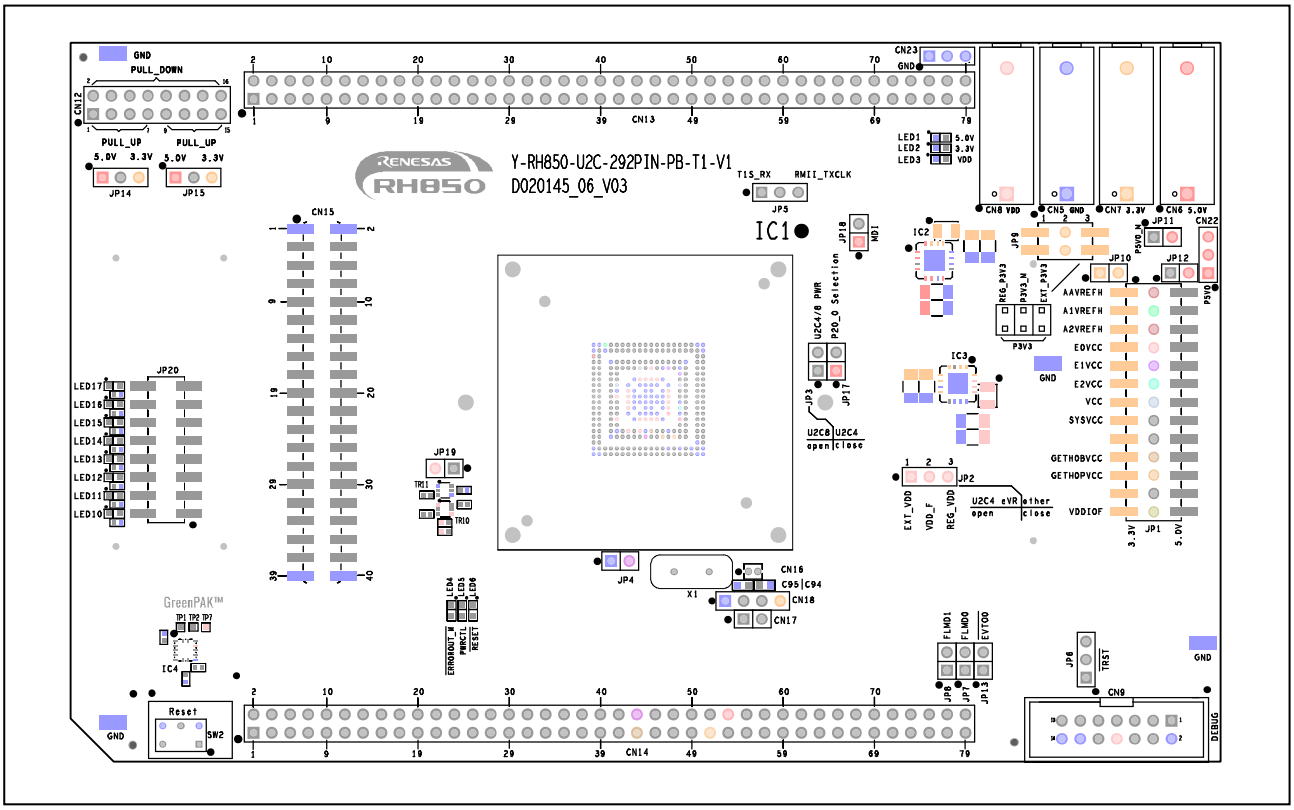


Figure 1.13 Piggyback board top view of board version D020145_06_V03

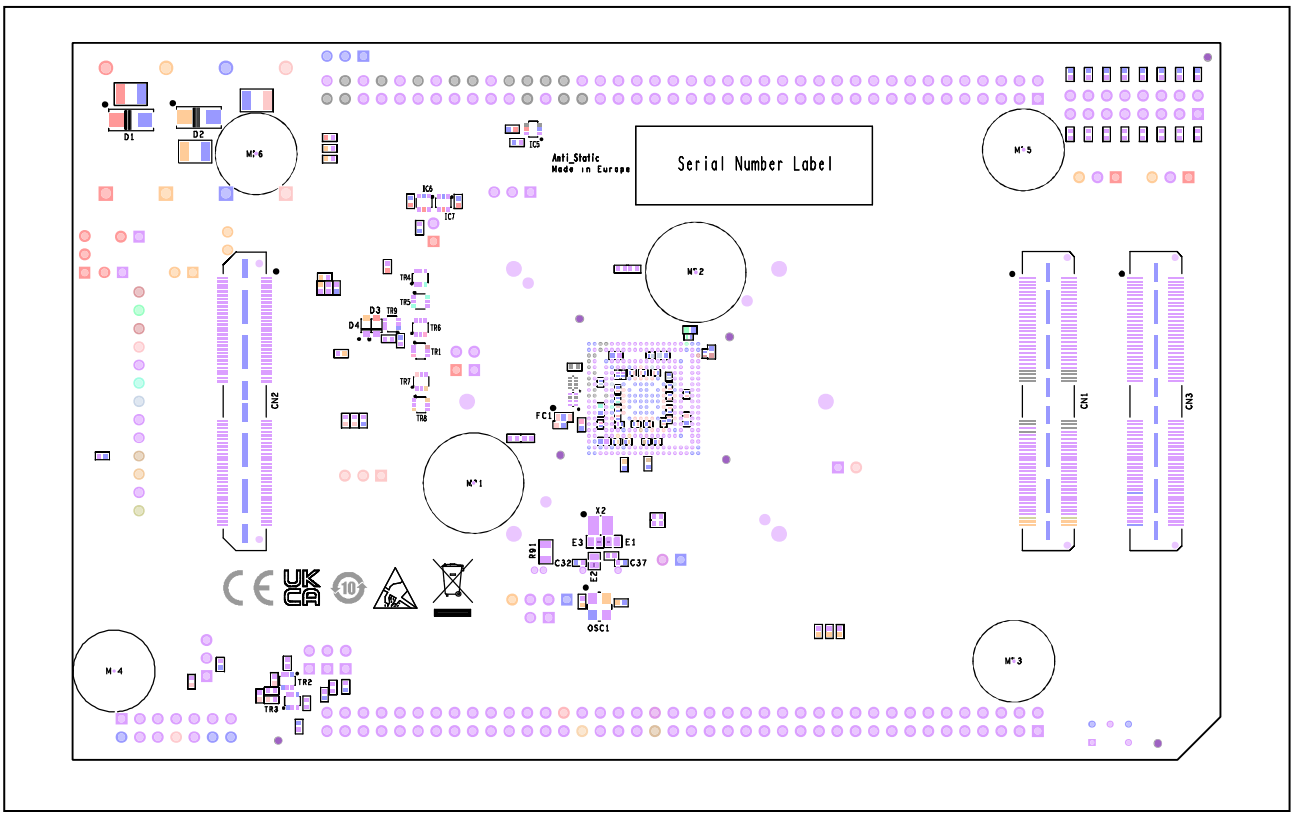


Figure 1.14 Piggyback board bottom view of board version D020145_06_V03

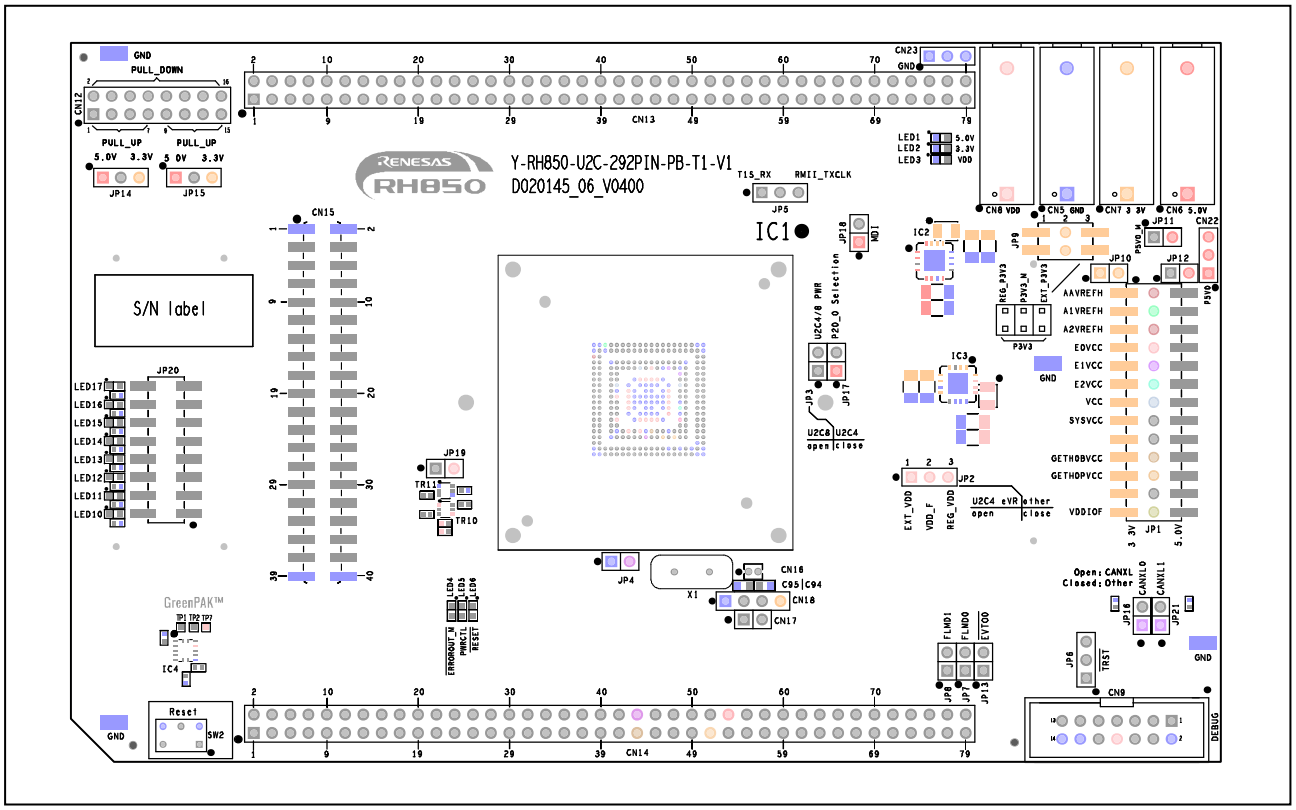


Figure 1.15 Piggyback board top view of board version D020145_06_V0400

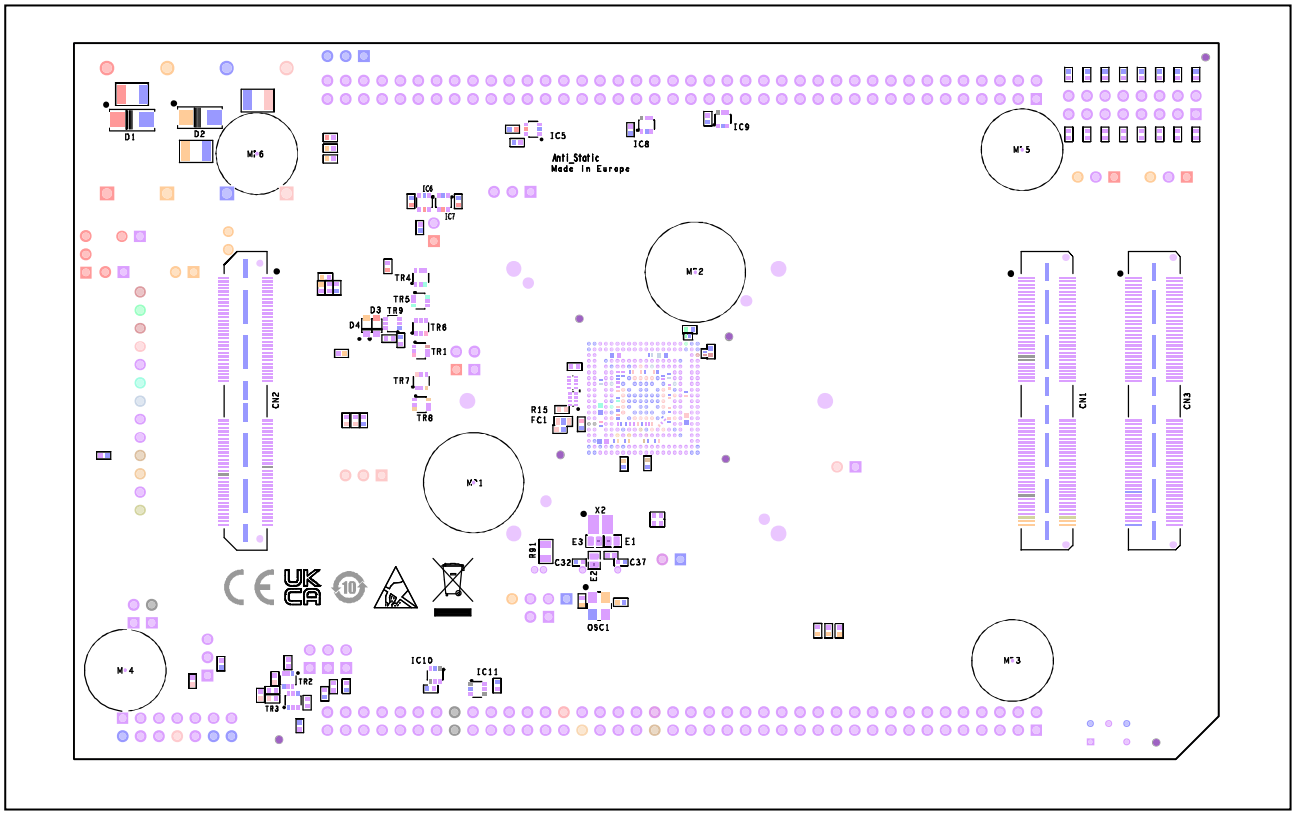


Figure 1.16 Piggyback board bottom view of board version D020145_06_V0400

1.6 Mounting of the Device

The board is designed for use with the following devices.

Table 1.4 Type names for suitable devices

	Device Name	Comments
RH850/U2C4	R7F702606FABB-C	Core power supply DPS *
	R7F702606AFABB-C	
	R7F702613FABB-C	Core power supply eVR * VCC = VPOC ~ 3.6 V
	R7F702613AFABB-C	
	R7F702616AFABB-C	Core power supply eVR * VCC = 4.5 V ~ 5.5 V
RH850/U2C8	R7F702600FABB-C	Core power supply DPS *
	R7F702600AFABB-C	

* The isolated area power domain is supplied by an external power supply (DPS) or internal regulator (eVR).

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking on the pcb. There the A1 pin of the socket is marked with a white dot. Please see *Figure 1.17 Yamaichi NP566-292-048 socket*.
On the device the index area is available on the corner near the A1 pin.

Figure 1.17 Yamaichi NP566-292-048 socket

CAUTION

Be careful with the device placement in the socket to avoid damaging the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors, and LEDs.

The placement of these components on the board is depicted in the figures below.

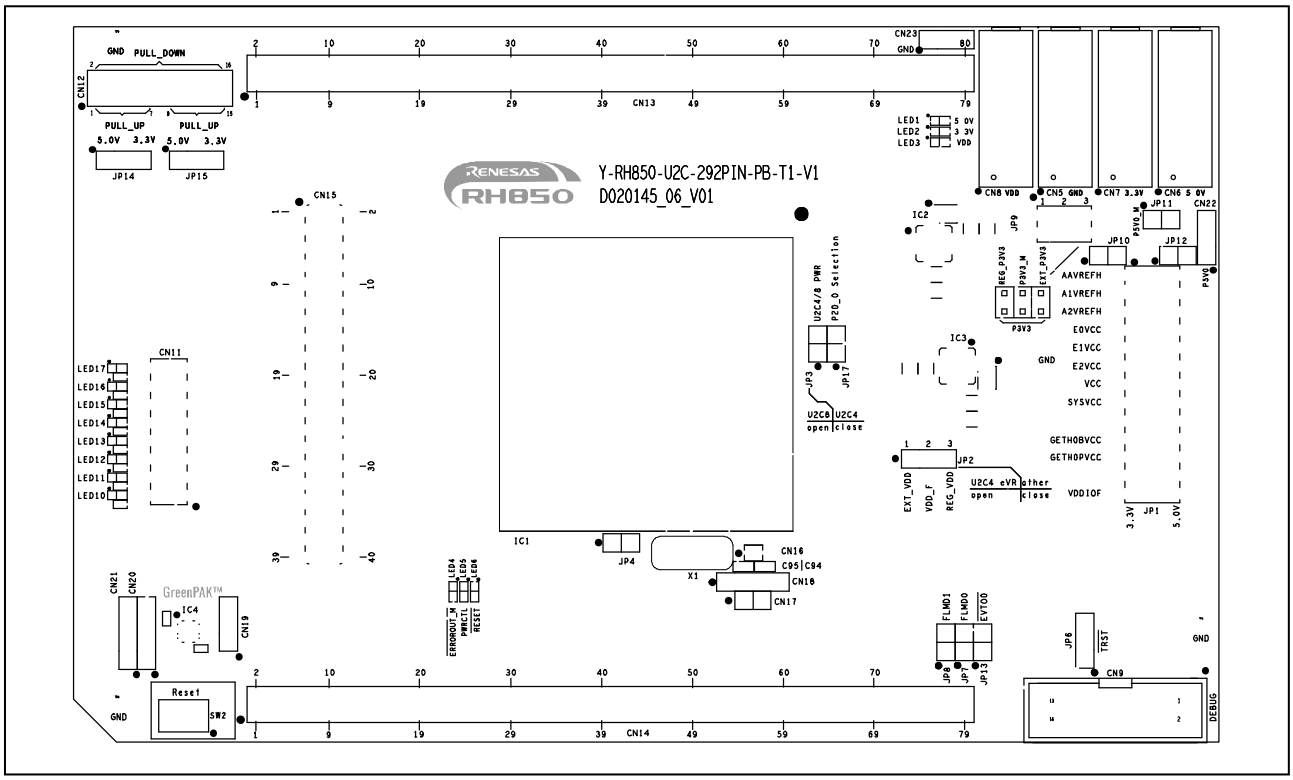


Figure 2.1 Placement of jumpers, connectors and LED on top side of board version D020145_06_V01

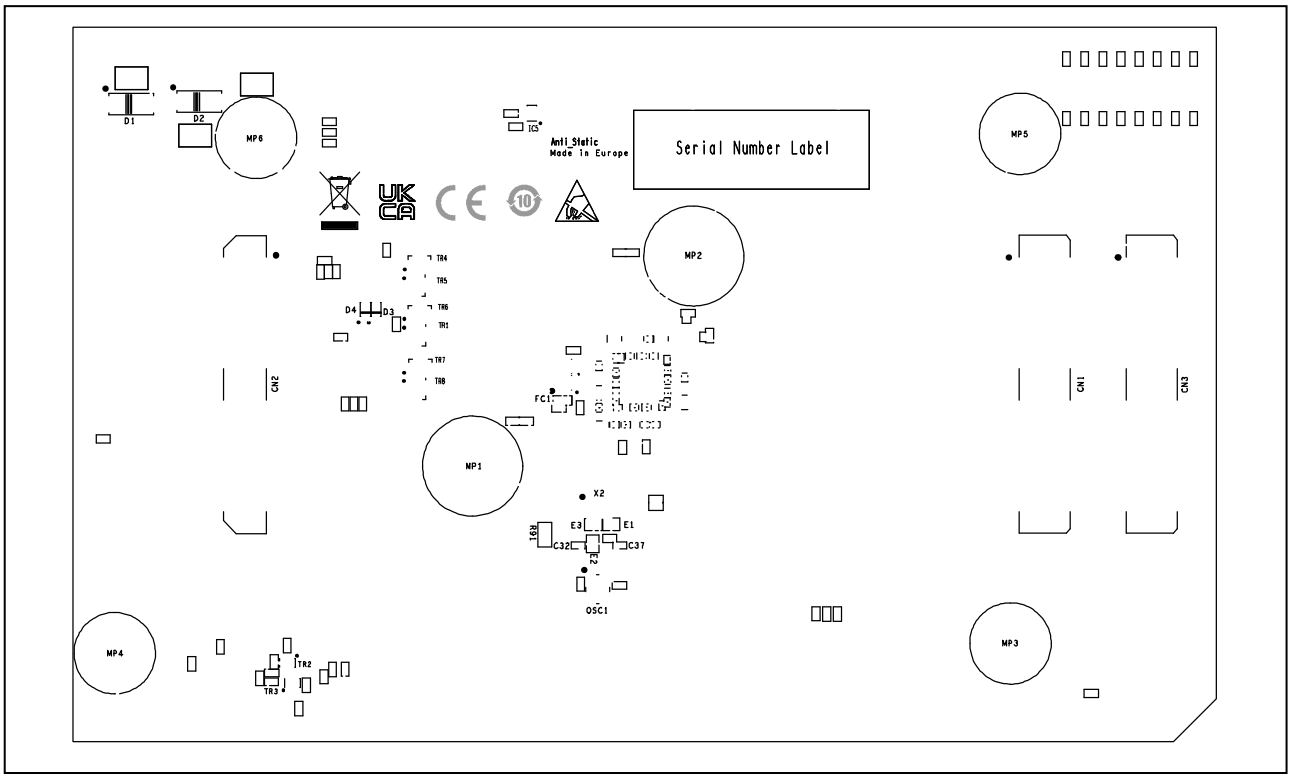


Figure 2.2 Placement of connectors on bottom side of board version D020145_06_V01

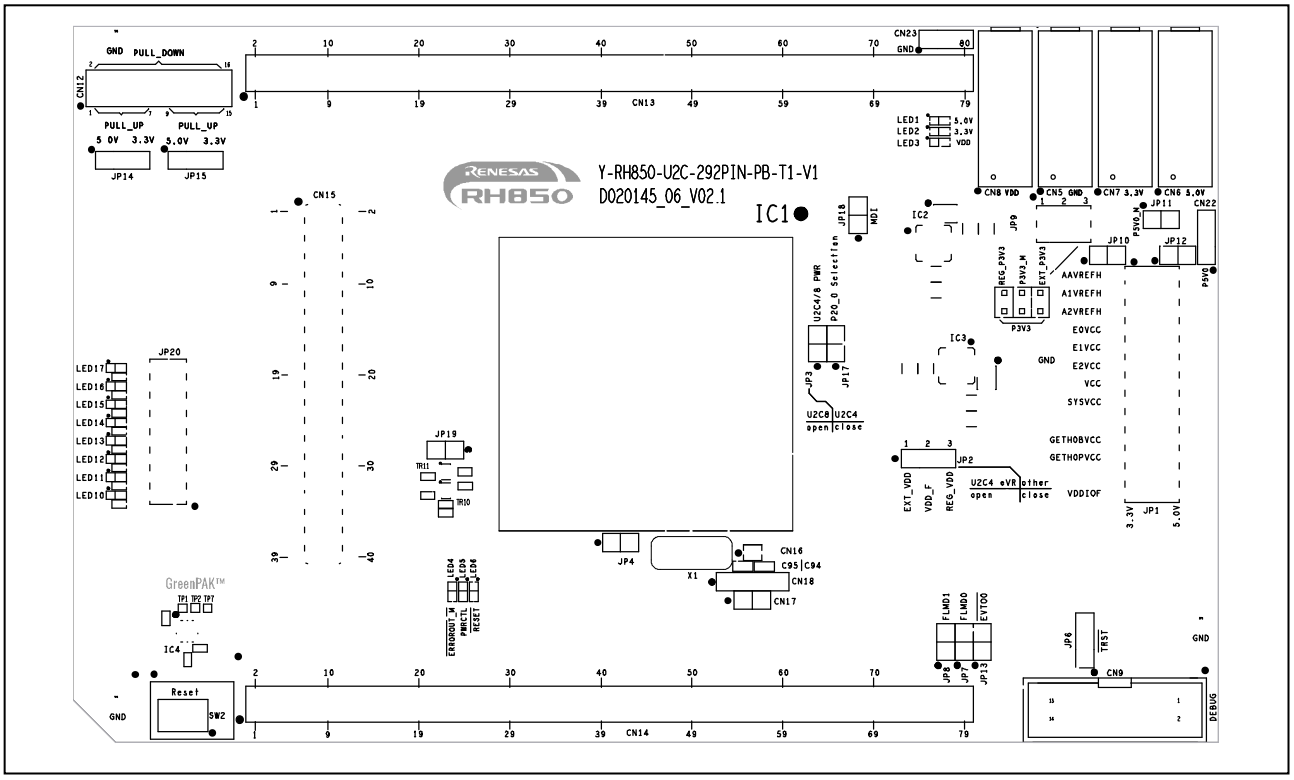


Figure 2.3 Placement of jumpers, connectors and LEDs on top side of board version D020145_06_V02.1

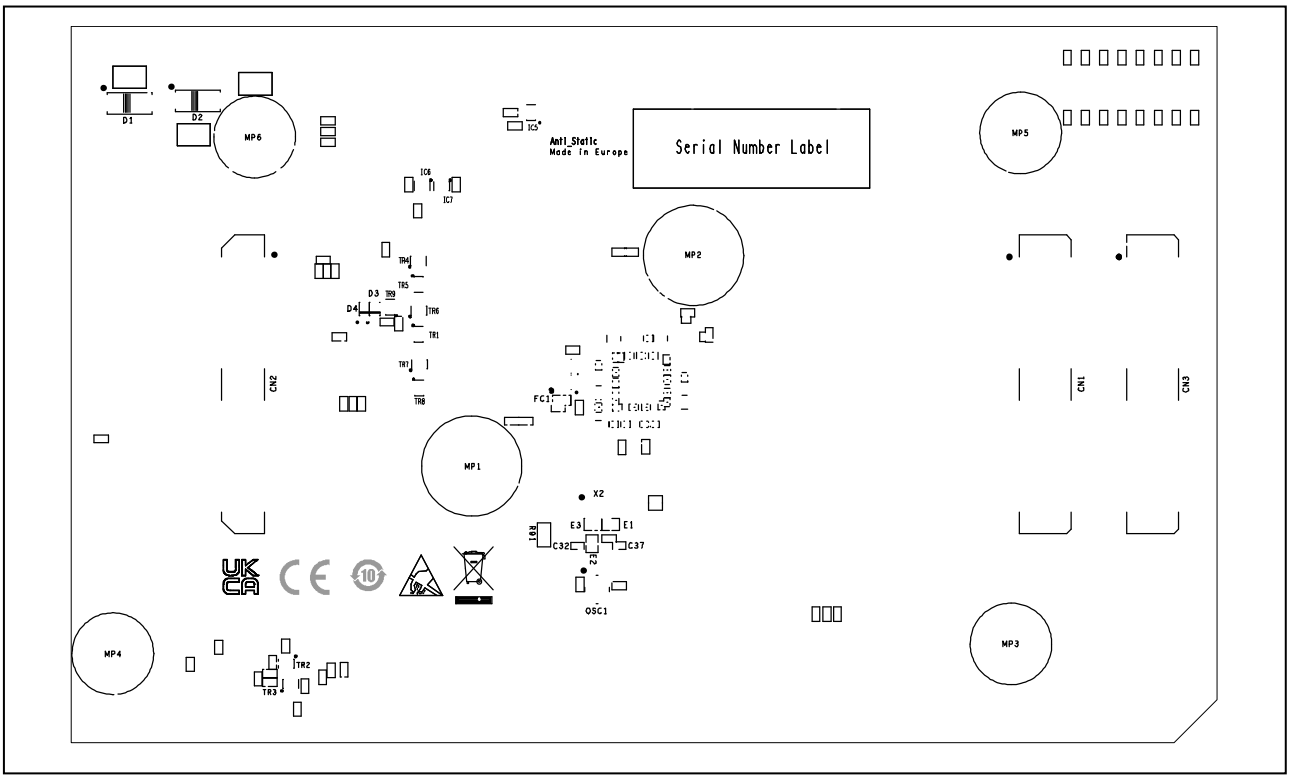


Figure 2.4 Placement of connectors on bottom side of board version D020145_06_V02.1

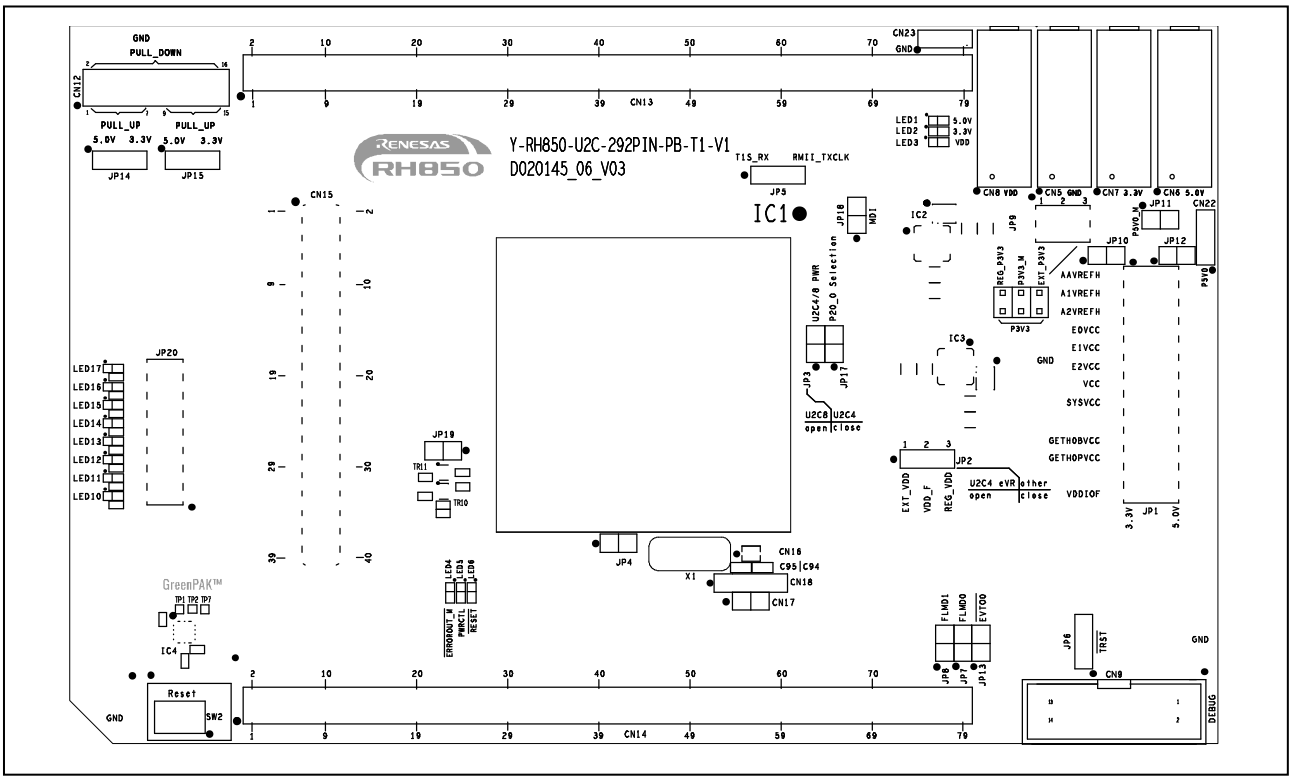


Figure 2.5 Placement of jumpers, connectors and LEDs on top side of board version D020145_06_V03

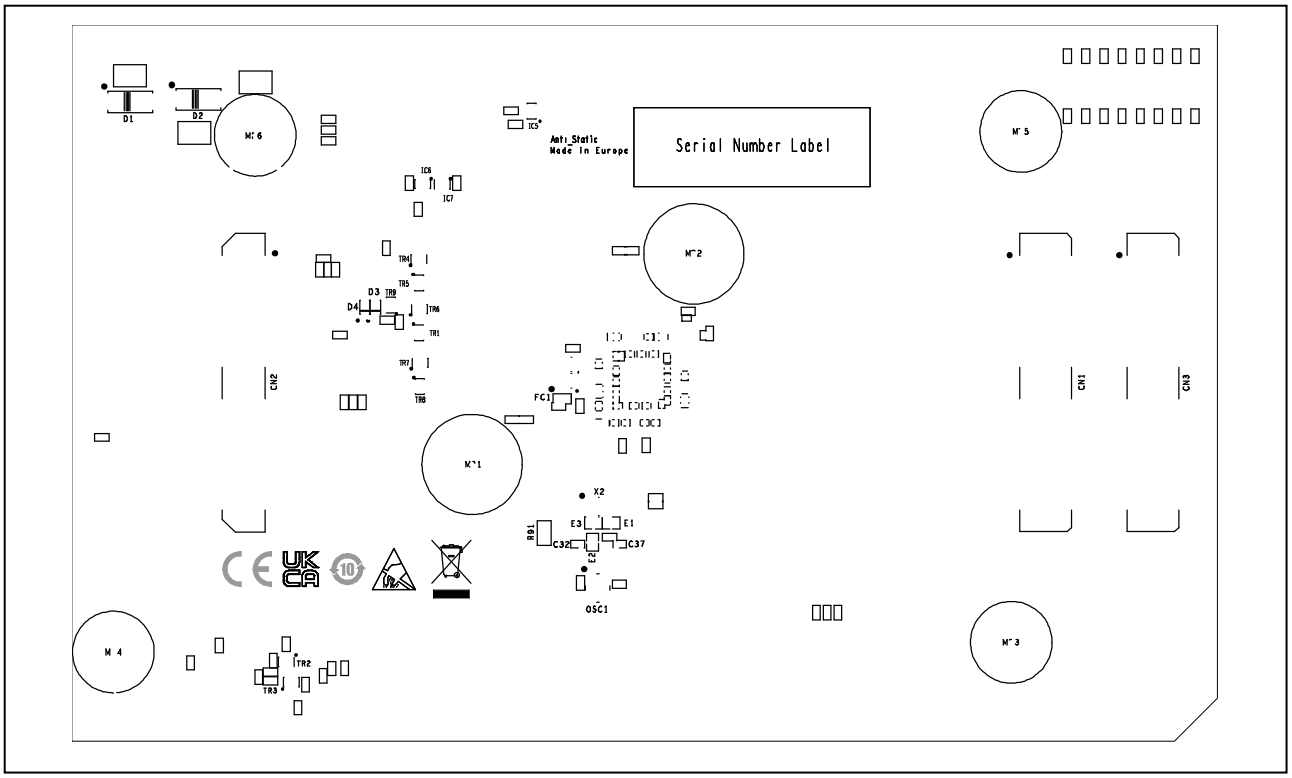


Figure 2.6 Placement of connectors on bottom side of board version D020145_06_V03

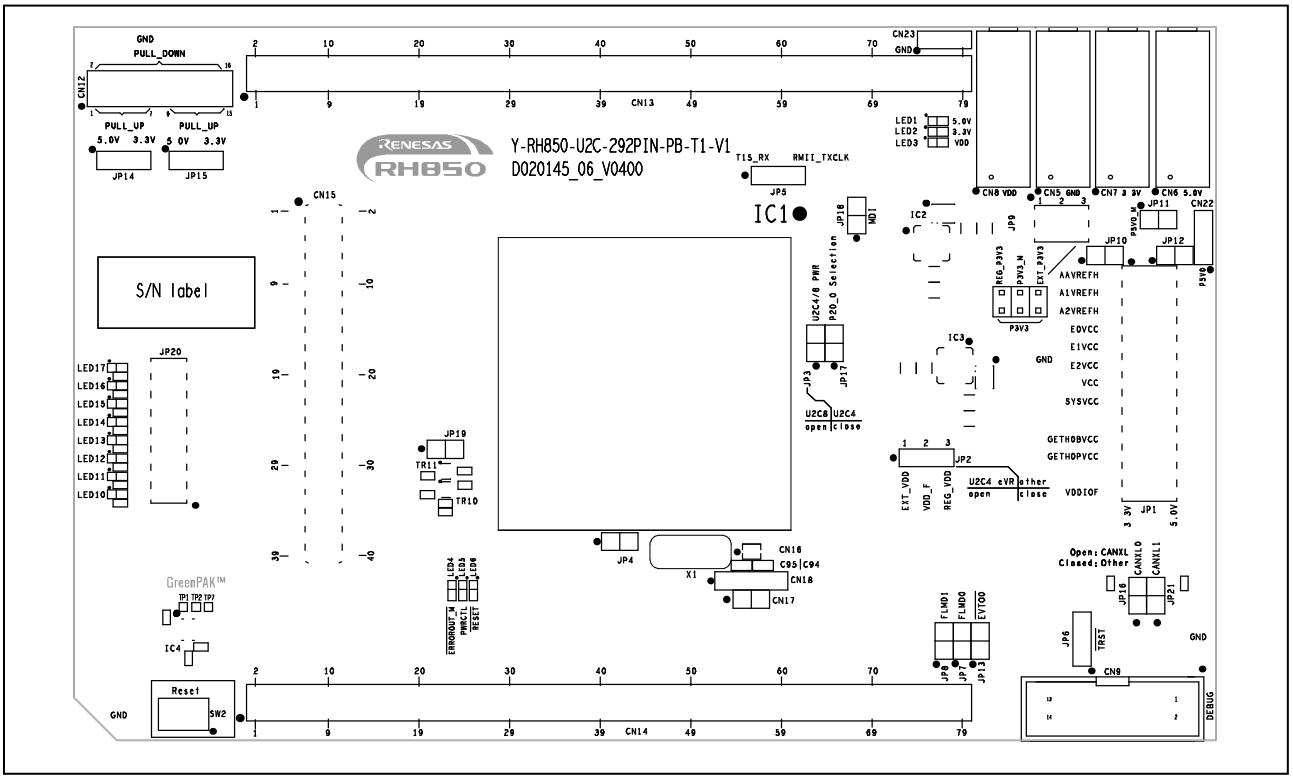


Figure 2.7 Placement of jumpers, connectors and LEDs on top side of board version D020145_06_V0400

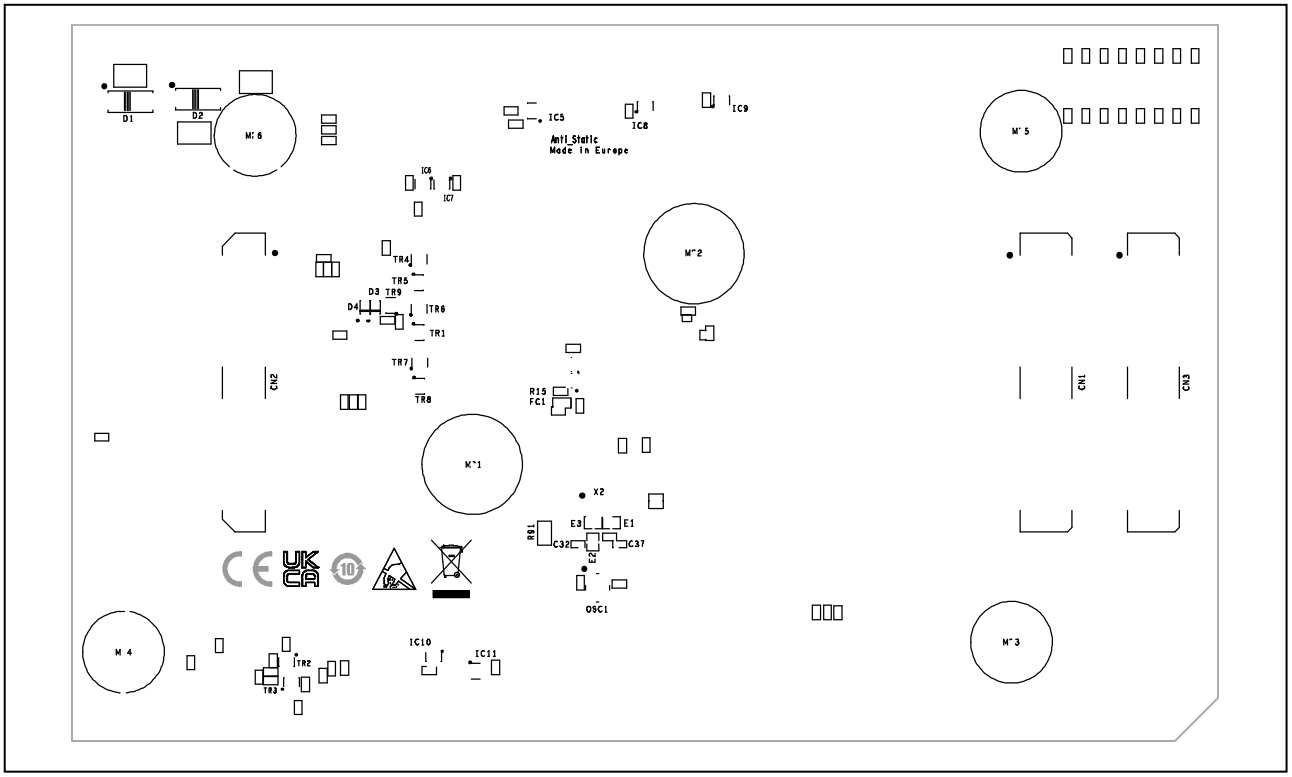


Figure 2.8 Placement of connectors on bottom side of board version D020145_06_V0400

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select +3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
JP2	Core voltage selection	refer to *3.3 Device Core Voltage Selection*
JP3	Device selection JP3[OPEN]: RH850/U2C8 (default) JP3[CLOSED]: RH850/U2C4	refer to *3.4 Voltage Selection for RH850/U2C4* and RH850/U2C
JP4	Pull port P00_7 to GND	
JP5	Select Ethernet function for port signal P20_3 • JP5[1-2]: T1S_RX • JP5[2-3]: RMII_TXCLK	from board revision D020145_06_V03 onwards refer to *6.6 Ethernet Control Port P20_3*
JP6	Select signal source for TRST# signal • JP6[1-2]: Fix TRST# signal to E0VCC • JP6[2-3]: TRST# signal is TRST#_TOOL signal from E2 debug connector (pin 3 on connector CN9)	refer to *5 Debug and Flash Programming Interface*
JP7	Change FLMD0 signal to “H”.	refer to *6.1 Operation Mode Selection*
JP8	Change FLMD1 signal to “GND”.	
JP9	Select +3.3 V power supply source • JP9[1-4]: Get +3.3 V from onboard voltage regulator • JP9[2-5]: Get +3.3 V from main board • JP9[3-6]: Get +3.3 V from external +3.3 V supply on CN7	refer to *3.2 Voltage Distribution*
JP10	Current measurement bridge +3.3 V	refer to *3.5 Current Measurement Bridges*
JP11	Enable +5.0 V supply from main board	refer to *3.1 Board Power Connection*
JP12	Current measurement bridge +5.0 V	refer to *3.5 Current Measurement Bridges*
JP13	Event trigger output EVTO0# for debugger	refer to *5 Debug and Flash Programming Interface*
JP14 JP15	Select pull-up voltage for Pull-Up Pull-Down connector CN12 JP14[1-2]: 5.0 V pull-up on pins 1 / 3 / 5 / 7 JP14[2-3]: 3.3 V pull-up on pins 1 / 3 / 5 / 7 JP15[1-2]: 5.0 V pull-up on pins 9 / 11 / 13 / 15 JP15[2-3]: 3.3 V pull-up on pins 9 / 11 / 13 / 15	refer to *6.9 Pull-Up/Pull-Down Pin Header*
JP16	Select ports for CAN XL 0 connection to an attached main board JP17[OPEN): Select CAN XL 0 function P17_2 connected to B1_P17_2 P17_3 connected to B1_P17_3 JP17[CLOSED): Select other functions P17_2 connected to B2_P17_2 P17_3 connected to B2_P17_3	from board revision D020145_06_V0400 onwards refer to *6.3 CAN-XL Port selection*

Table 2.1 Jumper overview (cont'd)

Jumper	Function	Remark
JP17	Select port P20_0 connection to an attached main board JP17[OPEN]: P20_0 connected to B1_P20_0 (ETH0RXD0) JP17[CLOSED]: P20_0 connected to B2_P20_0 (I2SMCLK)	refer to *0 Ethernet / I2S* Selection
JP18	Ethernet1 MDIO / MDC port selection JP18[OPEN]: ETH1_MDIO = P21_0 ETH1_MDC = P20_11 JP18[CLOSED]: ETH1_MDIO = P04_9 ETH1_MDC = P04_8	from board revision D020145_06_V02.1 onwards refer to *6.5 Ethernet 1 Control Ports MDIO / MDC*
JP19	Jumper for board production test	must be left open
JP20 (CN11)	Enable LED outputs (CN11 for board version D020145_06_V01)	refer to *6.8 Signalling LEDs*
JP21	Select ports for CAN XL 1 connection to an attached main board JP21[OPEN]: Select CAN XL 1 function P24_7 connected to B1_P24_7 P24_8 connected to B1_P24_8 JP21[CLOSED]: Select other functions P24_7 connected to B2_P24_7 P24_8 connected to B2_P24_8	from board revision D020145_06_V0400 onwards refer to *6.3 CAN-XL Port selection*

2.2 LED Overview

The following table provides an overview of all LED.

Table 2.2 LED overview

LED	Function	Color	Remark
LED1	5.0 V power supply P5V0	green	refer to *0 Power Supply* LEDs
LED2	3.3 V power supply int_P3V3	green	
LED3	LED_PG_VDD signal	green	
LED4	LED_ERROROUT_M# / VMONOUT# signal	red	refer to *6.2 System State and RESET*
LED5	LED_PWRCTL signal	red	
LED6	LED_RESET# signal	red	
LED10	Signalling LED	blue	refer to *6.8 Signalling LEDs*
LED11			
LED12			
LED13			
LED14			
LED15			
LED16			
LED17			

2.3 Connector Overview

The following table provides an overview of all connectors.

Table 2.3 Connector overview

Connector	Function	Remark
CN1	Main board connectors	refer to *7.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN5	GND external power supply	refer to *3.1 Board Power Connection*
CN6	+5.0 V external power supply	
CN7	+3.3 V external power supply	
CN8	+1.09 V external power supply	
CN9	E2 emulator debug connector	refer to *5 Debug and Flash Programming Interface*
CN11	Signalling LEDs pin header (only for board version D020145_06_V01)	refer to *6.8 Signalling LEDs*
CN12	Pull up / pull down configuration	refer to *6.9 Pull-Up/Pull-Down Pin Header*
CN13	Device ports connector	refer to *7.3 Device Ports Connectors CN13, CN14 and CN15*
CN14		
CN15		
CN16	Socket for sub-oscillator	refer to *4.4 Sub Oscillator*
CN17	IP0_0 and IP0_1 connector	
CN18	IP0_0 and IP0_1 fixed inputs	
CN19	Connectors for external Reset signal module	only board version D020145_06_V01; refer to *6.2 System State and RESET*
CN20		
CN21		
CN22	+5.0 V connector	
CN23	GND connector	

2.4 Switches Overview

The following table provides an overview of all switches.

Table 2.4 Switches overview

Connector	Function	Remark
SW2	RESET# switch	refer to *6.2 System State and RESET*

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board.
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage.
- 1.09 V for RH850/U2C core voltage VDD.
  Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

Four 4 mm connectors are available to connect external power supplies:

- black connector CN5 for GND (VSS)
- red connector CN6 for 5.0 V (P5V0)
- red connector CN7 for 3.3 V (Ext_P3V3)
- red connector CN8 for 1.09 V (Ext_P1V09)
  Connector CN8 is not assembled at delivery of the board, but separately supplied with the board package.
  Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

If the piggyback board is mounted on a main board, all voltages except for 1.09 V (VDD) can be supplied by the main board. The jumpers JP11 (5.0 V) and JP9[2-5] (3.3 V) are used to enable power supply from main board.

CAUTION

Do not supply the 5 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board if power supply from the main board is enabled.

Connecting external 1.09 V via CN8 (and GND via CN5) is still an option also in this case.

The piggyback board includes 2 onboard voltage regulator circuits. Both use Renesas ISL78234 buck regulator.

IC2 generates the board voltage of 3.3V (P3V3_REG) from 5.0V (P5V0) input voltage on CN6.

IC3 generates the core voltage of 1.09V (P1V09_REG) from 3.3V (P3V3).

Figure 3.1 shows both voltage regulator circuits.

The jumper settings for some general power supply scenarios are described in *8 Jumper Configuration Examples*.

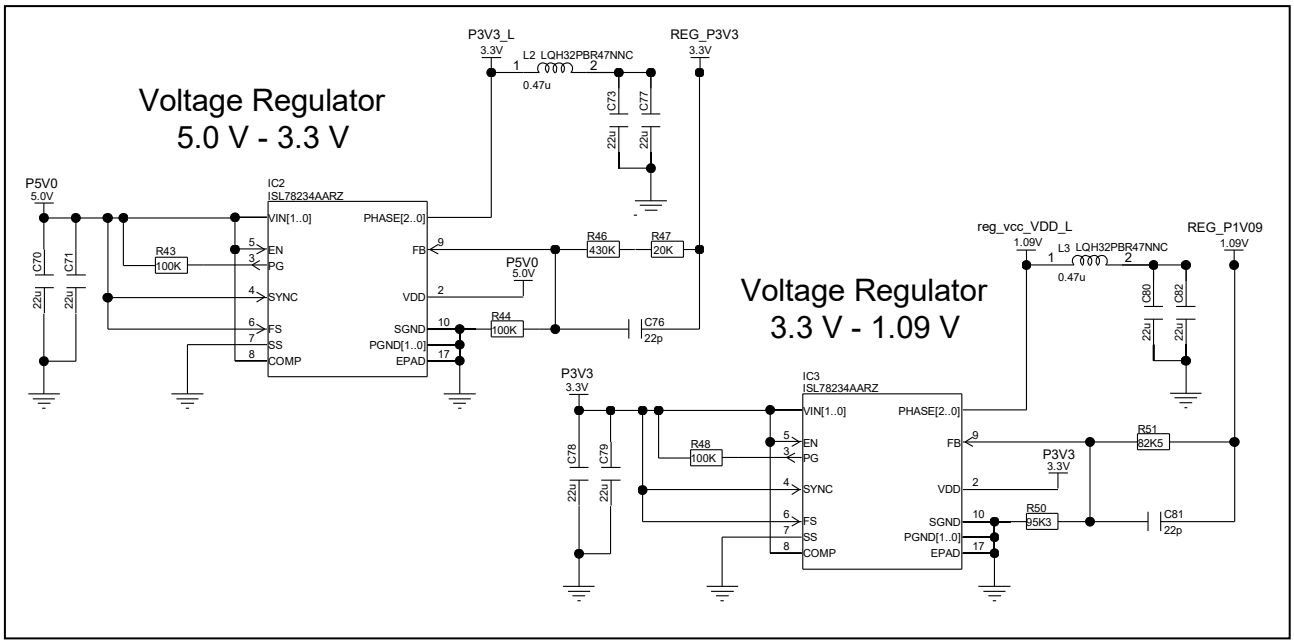


Figure 3.1 Voltage regulator circuit

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC (RH850/U2C8 only)	3.3 V, 5 V	Power supply for I/O ports
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
AAVREFH, A1VREFH, A2VREFH (RH850/U2C8 only)	3.3 V, 5 V	A/D converter's power supplies and reference voltages
VDD_F	1.09 V	Core supply voltage refer to *3.3 Device Core Voltage Selection*
GETH0BVCC (RH850/U2C8 only)	3.3 V	Ethernet power supply, only for RH850/U2C8
GETH0PVCC (RH850/U2C8 only)	3.3 V, 5 V	

Each of these voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V (P3V3) can be selected from external power supply (Ext_P3V3, CN7), main board power supply (P3V3_M) or from the onboard voltage regulator (REG_P3V3) using jumper JP9:

- JP9 [1-4]: 3.3 V supply P3V3 comes from the onboard voltage regulator REG_P3V3.
- JP9 [2-5]: 3.3 V supply P3V3 comes from the main board power supply P3V3_M.
- JP9 [3-6]: 3.3 V supply P3V3 comes from the external power supply CN7 (Ext_P3V3).

The supply for 5.0 V (P5V0) can be selected from external power supply (P5V0, CN6) or from main board power supply (P5V0_M) using jumper JP11:

- JP11 [CLOSED]: 5.0 V supply comes from main board supply P5V0_M.
- JP11 [OPEN]: 5.0 V supply P5V0 comes from the external power supply CN6.

Table 3.2 shows which jumpers to set to select the different device supply voltages, and *Figure 3.2* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
AAVREFH	JP1 [1-2]	JP1 [2-3]
A1VREFH	JP1 [4-5]	JP1 [5-6]
A2VREFH	U2C8: JP1 [7-8] U2C4: ---	U2C8: JP1 [8-9] U2C4: ---
E0VCC	JP1 [10-11]	JP1 [11-12]
E1VCC	JP1 [13-14]	JP1 [14-15]
E2VCC	U2C8: JP1 [16-17] U2C4: ---	U2C8: JP1 [17-18] U2C4: ---
VCC	JP1 [19-20]	JP1 [20-21]
SYSVCC	JP1 [22-23]	JP1 [23-24]
GETH0BVCC	U2C8: JP1 [28-29] U2C4: ---	---
GETH0PVCC	U2C8: JP1 [31-32] U2C4: ---	U2C8: JP1 [32-33] U2C4: ---
VDDIOF	JP1 [37-38]	JP1 [38-39]

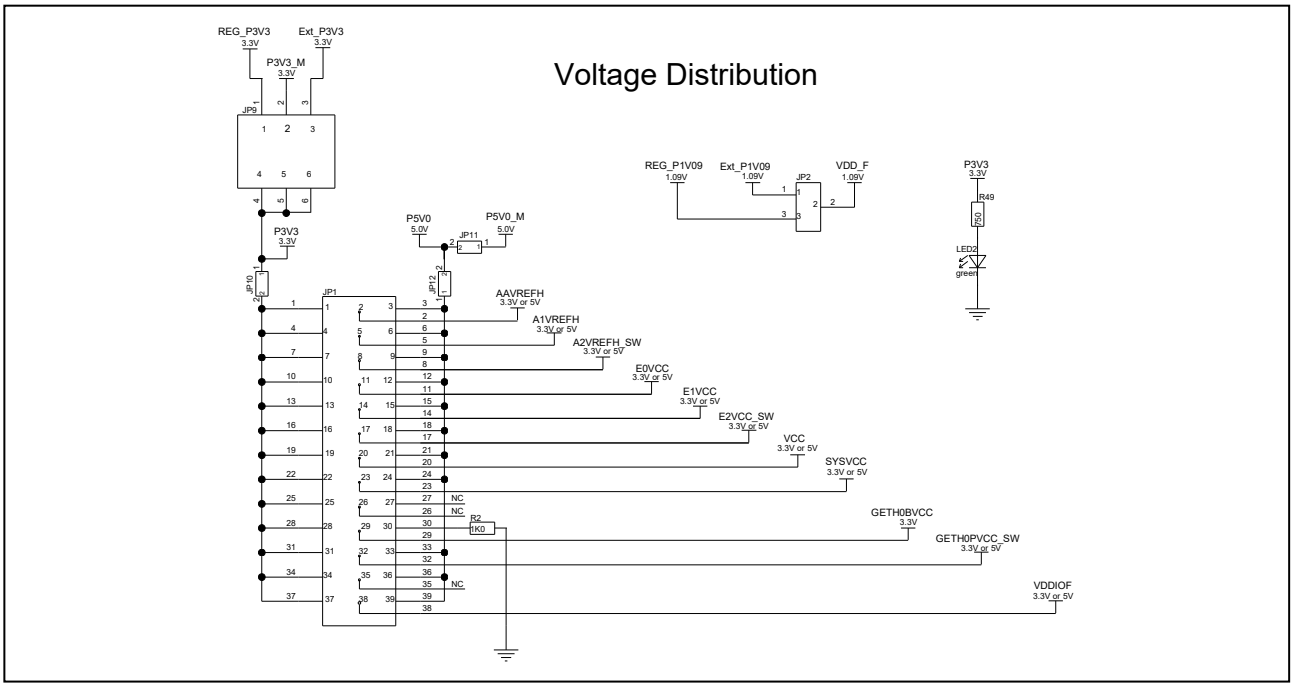


Figure 3.2 Voltage distribution

3.3 Device Core Voltage Selection

The internal core voltage circuits are separated into two independent power domains, the Always-On area (AWO) and the Isolated area (ISO).

The power supply of the Always-On area is derived from SYSVCC. It is always on in all operating modes and stand-by modes.

RH850/U2C devices are available in 2 different versions providing different possibilities for the power supply to the Isolated voltage area (ISO). The ISO area power domain can be supplied by an external power supply (DPS) or by the on-chip voltage regulator (eVR).

The board versions up to version D020145_06_V03 are designed for use with a DPS device using external core voltage supply. Chapter *3.3.1* gives some details on this implementation.

The board version D020145_06_V0400 can be used with eVR (VCC = 3.3 V or 5.0 V) and DPS devices. By default it is assembled to use an RH850/U2C device with eVR circuit designed for 5.0 V power supply. Details are explained in chapter *3.3.2*.

3.3.1 Piggyback Board Version up to D020145_06_V03

This piggyback version has been designed for used with DPS devices with external core voltage supply.

Note

Even though the piggyback board has been designed for use with DPS devices, it is also possible to use eVR devices (with embedded voltage regulator for core voltage supply).
However, when using eVR devices board operation may be slightly unstable, although this is not expected.

The device core voltage VDD (typ.1.09 V) can be

- supplied from external via CN8 (voltage Ext_P1V09)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage REG_P1V09)

VDD source is selected by jumpers in JP2:

JP2[1-2]: VDD_F = Ext_P1V09

JP2[2-3]: VDD_F = REG_P1V09

The circuit diagram for jumper JP2 in included in Figure 3.2 Voltage distribution.

CAUTION

If a device with eVR core power supply is being used jumper JP2 must be open. If JP2 is set to either position the device may be damaged.

3.3.2 Piggyback Board Version D020145_06_V0400 and later

This piggyback version has been designed for use with eVR and DPS devices. Please refer to *Table 1.4 Type names for suitable devices* for the device type numbers.

The device core voltage VDD (typ.1.09 V) can be

- supplied from external via CN8 (voltage Ext_P1V09)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage REG_P1V09)

- generated by the integrated voltage regulator in RH850/U2C. Depending on the device power supply VCC different devices have to be used.

The default assembly of the piggyback board is designed to use devices with embedded voltage regulator (eVR) and a device supply voltage VCC = 5.0 V.

If the board should be used with eVR devices for 3.3 V or DPS devices it is necessary to modify the piggyback board.

Note

To comply with the Electrical Specification within the device UM, it is necessary to modify the piggyback board if it should be used with eVR devices for 3.3 V or DPS devices, as shown in the pictures below.

For the operation under the limited environment of the piggyback board, it is sufficient to use the default circuitry of the 5.0V eVR device use case also for the use cases with 3.3V eVR and DPS devices.

Figure 3.3 shows the circuit diagram for each device type.

Table 3.3 lists the modifications that must be applied for different device types.

Figure 3.4 shows the locations of the components that have to be modified. All these components are located on the lower side of the pcb.

The circuit diagram for jumper JP2 in included in Figure 3.2 Voltage distribution.

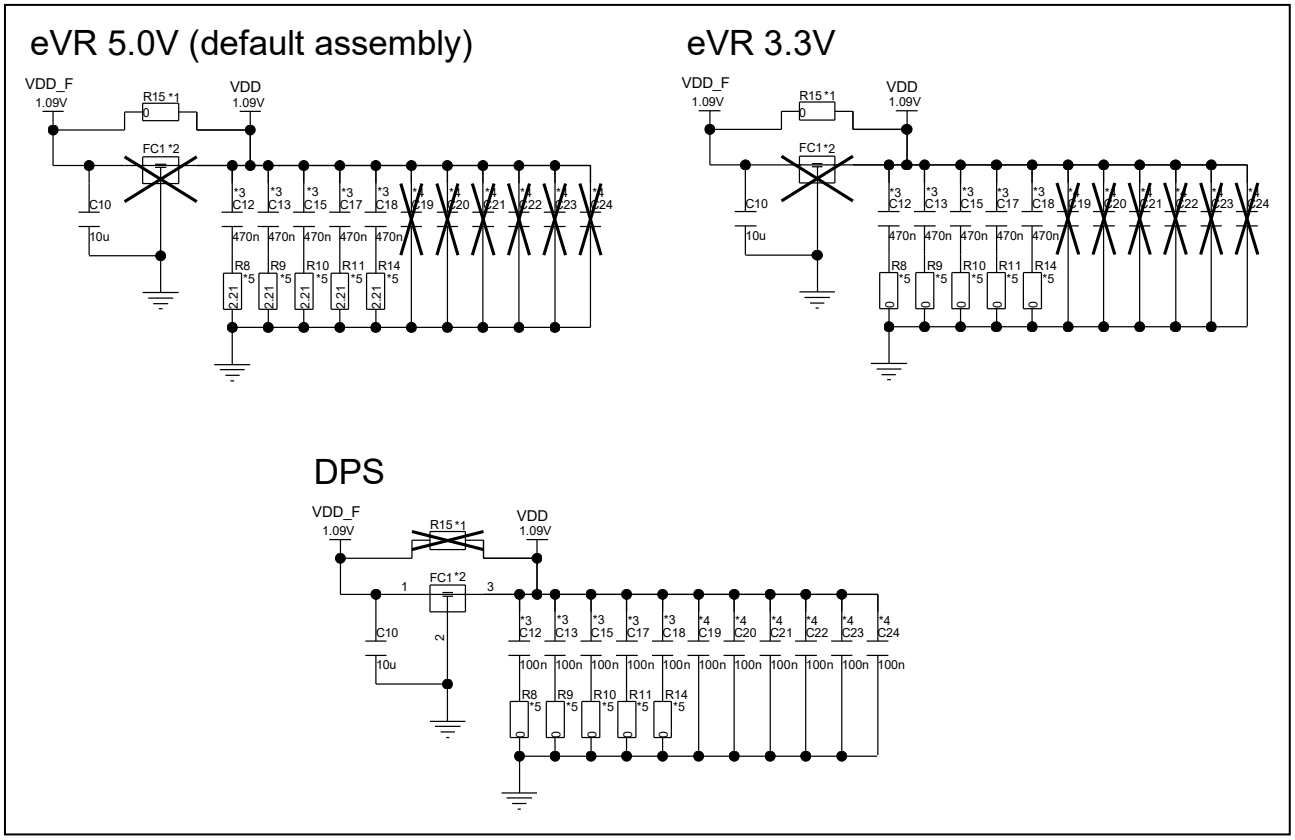


Figure 3.3 Device circuits for different RH850/U2C variants

Table 3.3 Piggyback board modifications for different RH850/U2C device types

Device power supply pin	Device with DPS	Device with eVR VCC = 3.3V	Device with eVR VCC = 5.0V Default setting
Jumper JP2	Select source for core voltage VDD_F JP2[1-2]: VDD_F = Ext_P1V09 JP2[2-3]: VDD_F = REG_P1V09	Open	Open
Group *1 Resistor R15	Open	Populated 0 Ohm	Populated 0 Ohm
Group *2 EMI Filter FC1	Populated	Open	Open
Group *3 Capacitors C12 / C13 / C15 / C17 / C18	Populated 100nF	Populated 470nF	Populated 470nF
Group *4 Capacitors C19 / C20 / C21 / C22 / C23 / C24	100nF	Open	Open
Group *5 Resistors R8 / R9 / R10 / R11 / R14	0 Ohm	0 Ohm	2.21 Ohm

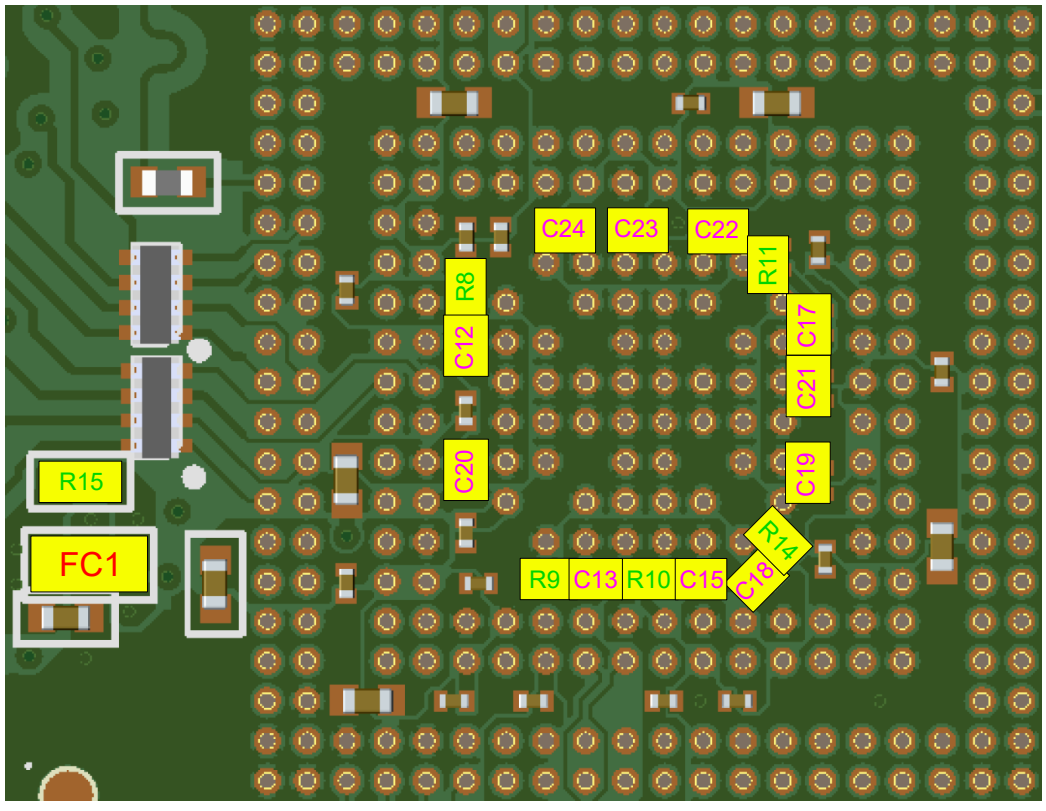


Figure 3.4 Locations of components to be modified

3.4 Voltage Selection for RH850/U2C4 and RH850/U2C8

The piggyback board can be used with RH850/U2C4 and RH850/U2C8 processors. These processors have some differences in the power supply configuration. The piggyback board provides jumper JP3 to configure the power supply for RH850/U2C4 or RH850/U2C8 devices.

Table 3.4 shows the jumper settings.

Figure 3.3 shows the related circuit diagrams.

Table 3.4 RH850/U2C4 / RH850/U2C8 voltage selection jumpers

Jumper	Function
JP3	RH850/U2C device selection ▪ JP3[OPEN]: RH850/U2C8 (default) ▪ JP3[CLOSED]: RH850/U2C4

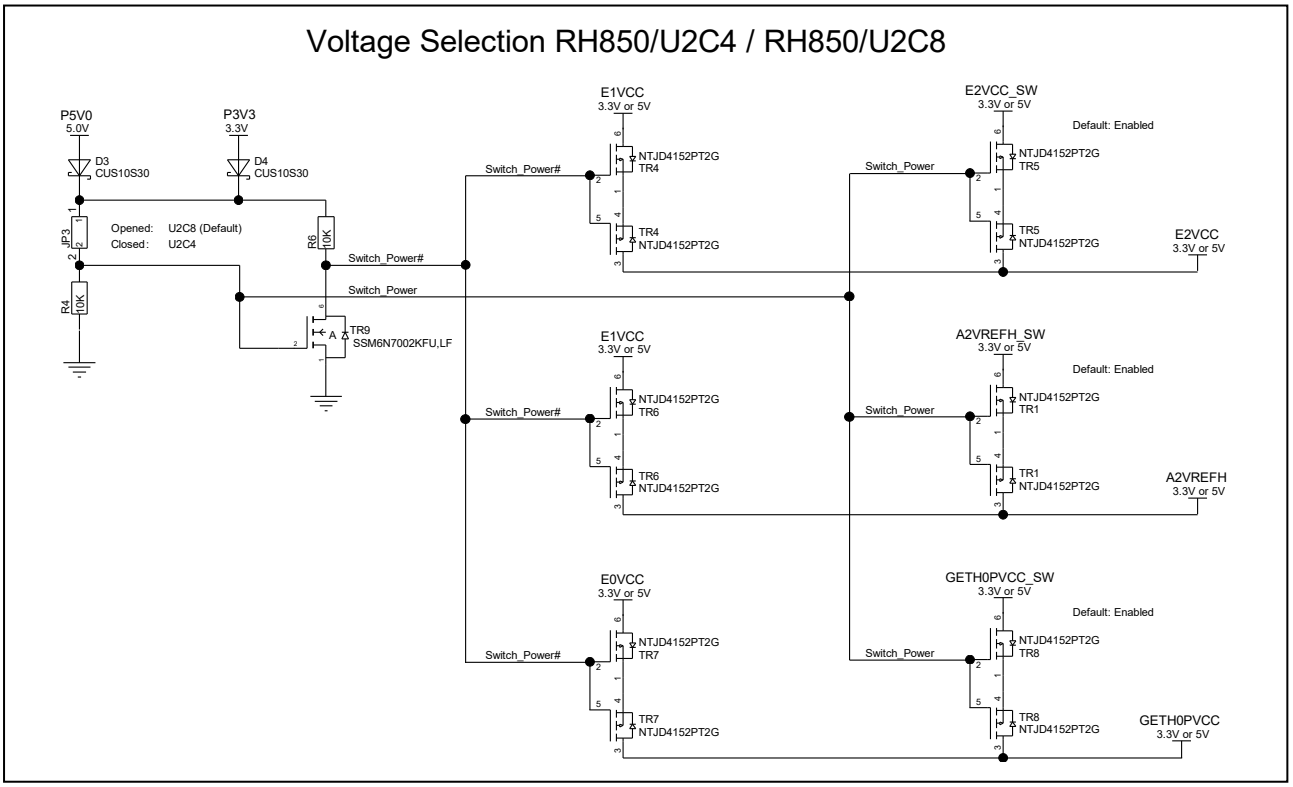


Figure 3.5 Voltage selection RH850/U2C4 / RH850/U2C8

3.5 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP10 and JP12 with an amperemeter.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.2 Voltage distribution*.

3.6 Power Supply LEDs

The following green LEDs indicate the availability of various voltages on the piggyback board:

- LED1 for 5.0 V power rail P5V0
- LED2 for 3.3 V power rail P3V3
- LED3 for 1.09 V device core voltage VDD

4. Clock Supply

The device's operation clock can be generated by

- the on-chip main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals.
- an external oscillator where the clock is fed into the X1 terminal.

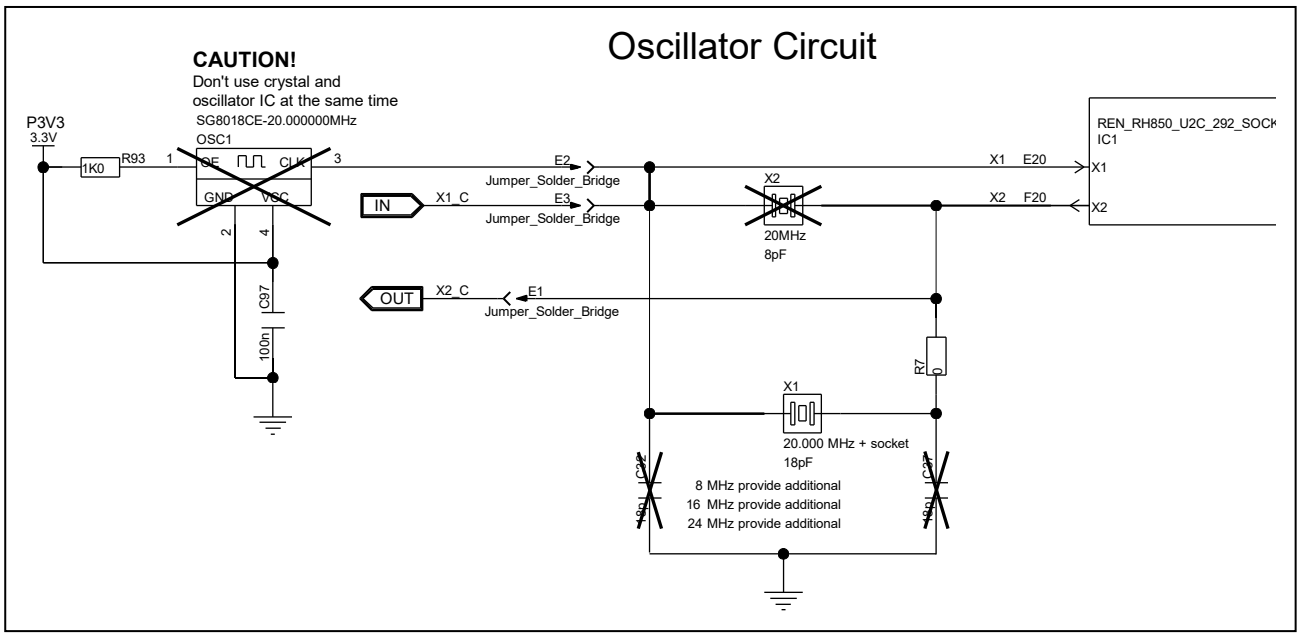


Figure 4.1 Clock supply

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Several resonators for various main oscillator frequencies (8 MHz, 16 MHz, 20 MHz, 24 MHz) are included in the board package.

The 20MHz resonator is by default mounted to the X1 socket.

For package content please refer to *1.1 Package Components.*

CAUTION

Only one oscillator, either X1, X1_C, X2 or OSC1, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via solder bridge E2.

For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 Device Pins X1 and X2 on Connector CN14

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN14 via 0 Ω resistors:

- Device pin X1: Connect to pin 52 of CN14 via solder bridge E3 to supply an external clock to the device.
- Device pin X2: Connect to pin 50 of CN14 via solder bridge E1 for measurement purposes of the clock.

4.4 Sub Oscillator

The pins IP0_0 and IP0_1 can also be used as oscillator pins XT1 and XT2 to connect a real-time clock oscillator.

If no oscillator is connected the pins IP0_0 and IP0_1 can be used as input ports.

If an oscillator is connected the ports are switched to oscillator function by programming the bits in IPIBC0 (Port Input Buffer Control) register and the oscillator is started by programming the SOSCE (Sub OSC Enable) register in RH850.

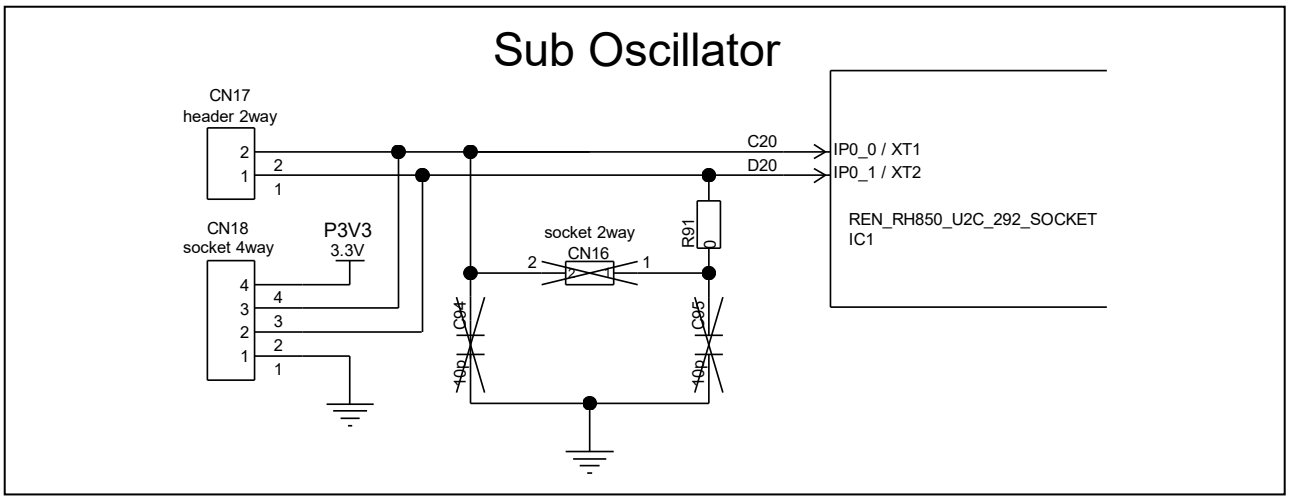


Figure 4.2 Sub Oscillator connnection

5. Debug and Flash Programming Interface

For debugging and flash programming purposes debug and flash programming tools can be connected to connector CN9.

Figure 5.1 shows the circuit diagram including all jumpers.

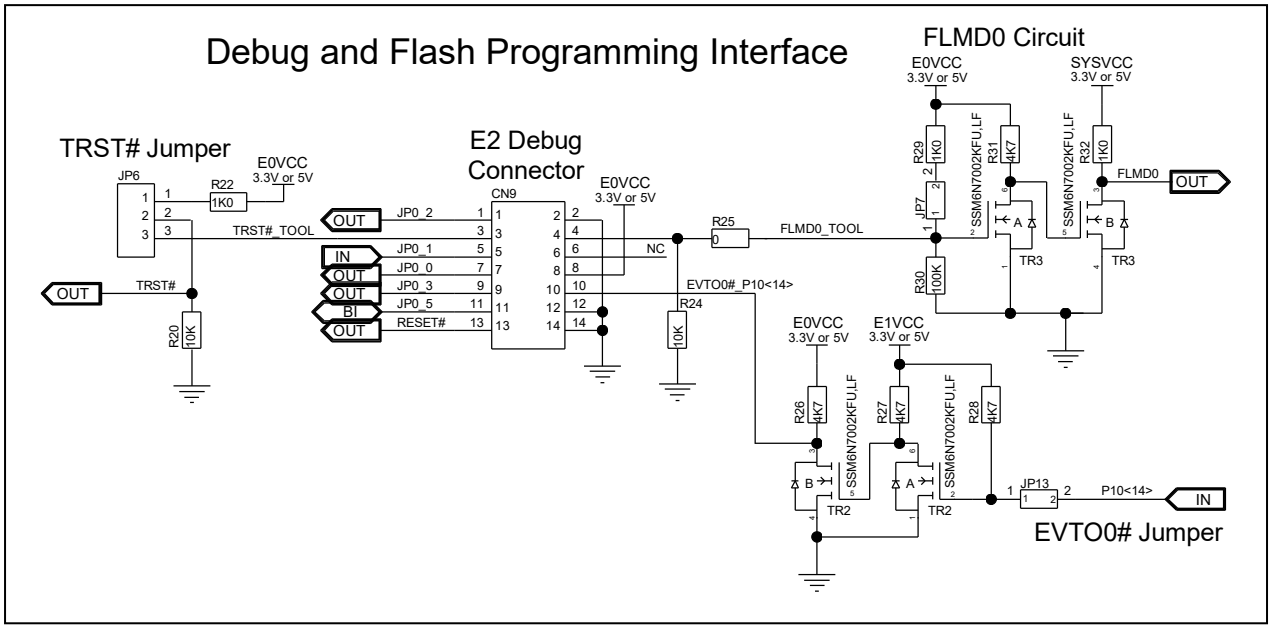


Figure 5.1 Debug and flash programming interface

CN9 is a 14-pin connector for on-chip emulators supporting Nexus JTAG or LPD4 debug interfaces like Renesas E2 Emulator.

The Renesas standard emulator for RH850/U2C is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

RH850/U2C can provide an event trigger signal to the debugger. This is EVTO0# signal. It can be output on port P10_14 (alternative port function). The event trigger output is activated by closing jumper JP13.

The emulator can issue a target reset signal (TRST#) to RH850/U2C. The signal can be activated using jumper JP6.

- JP6[1-2]: Connect TRST# input to E0VCC.
- JP6[2-3]: Connect TRST#_TOOL signal from emulator to TRST# input.

For flash programming RH850/U2C can either be switched to programming mode manually by closing jumper JP7 or by a connected flash programming tool.

- JP7[CLOSED]: FLMD0 = H level, RH850/U2C is in flash programming mode.
- JP7[OPEN]: FLMD0 = FLMD0 controlled by connected programmer, GND if no programmer is connected.

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board provides 2 jumpers to control the RH850 operation mode. *Table 6.1* lists the jumpers and gives details on their function.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP7	FLMD0 pin level ▪ JP7[CLOSED]: FLMD0 = H level ▪ JP7[OPEN]: FLMD0 • controlled by debugger or flash programming tool if a tool is connected via CN9 • GND, if no tool connected
JP8	FLMD1 pin level ▪ JP8[CLOSED]: FLMD1 = GND ▪ JP8 must be closed if Serial Programming Mode with 2-wire UART interface is used by a flash programming tool, that is connected to the board. • JP8[OPEN]: FLMD1 open • Port function of P06_7 can be used.

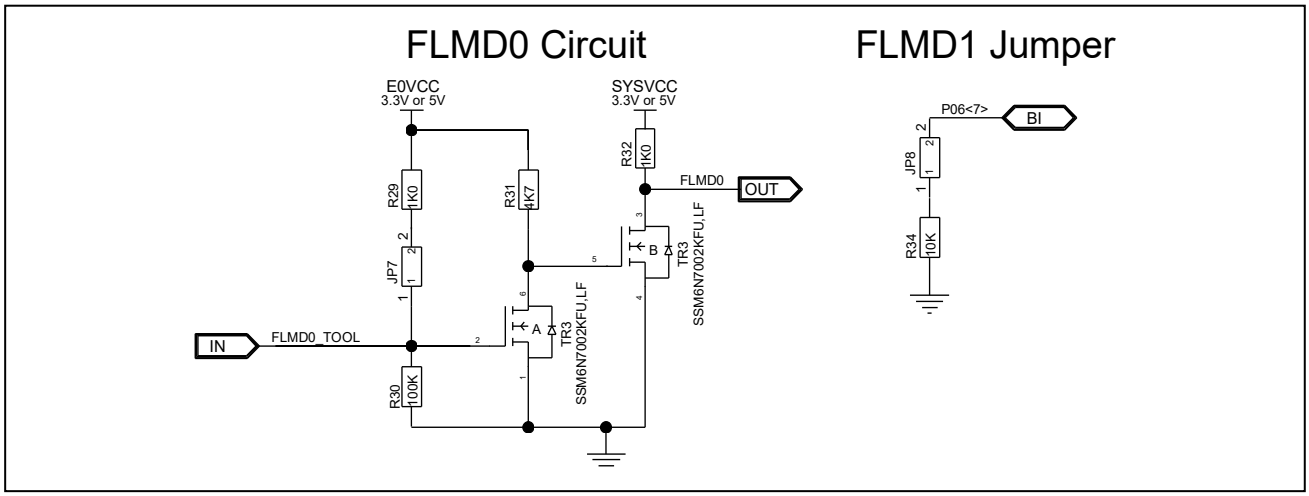


Figure 6.1 Operating mode selection jumpers

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP7.

All other jumpers related to the mode selection can be left open.

6.2 System State and RESET

This piggyback board has a special reset circuit using the Renesas GreenPAK IC SLG46855 (board version D020145_06_V01), SLG7RN47274-APTR (board version D020145_06_V02.1) or SLG7RN47274-AP_r004 (board version D020145_06_V03 and later). This IC is designed to receive various RH850 control signals and switch control LED accordingly. It also receives the signal from the RESET switch SW2 to generate the reset signal for the piggyback board and controls the reset LED.

The piggyback board has 3 LED to indicate control signals and reset status:

- LED4 for a control signal triggered by ERROROUT_M# or VMONOUT#.
- LED5 for a control signal triggered by PWRCTL.
- LED6 for a reset triggered by the reset switch SW2.

The GreenPAK IC also recognizes the availability of the RH850 core supply voltage VDD and switches LED3 to show the presence.

Figure 6.2 shows the circuit of the GreenPAK IC and the reset signal inputs of board version D020145_06_V01. This circuit has additional connectors CN19 – CN21 for external RESET signal inputs.

Figure 6.3 shows the circuit of the GreenPAK IC of board version D020145_06_V02.1. Here the connectors CN19 – CN21 have been removed .

Figure 6.4 shows the circuit of the GreenPAK IC of board version D020145_06_V03 and later. Here the GreenPAK IC has been replaced by a new revision to improve the Reset signal processing.

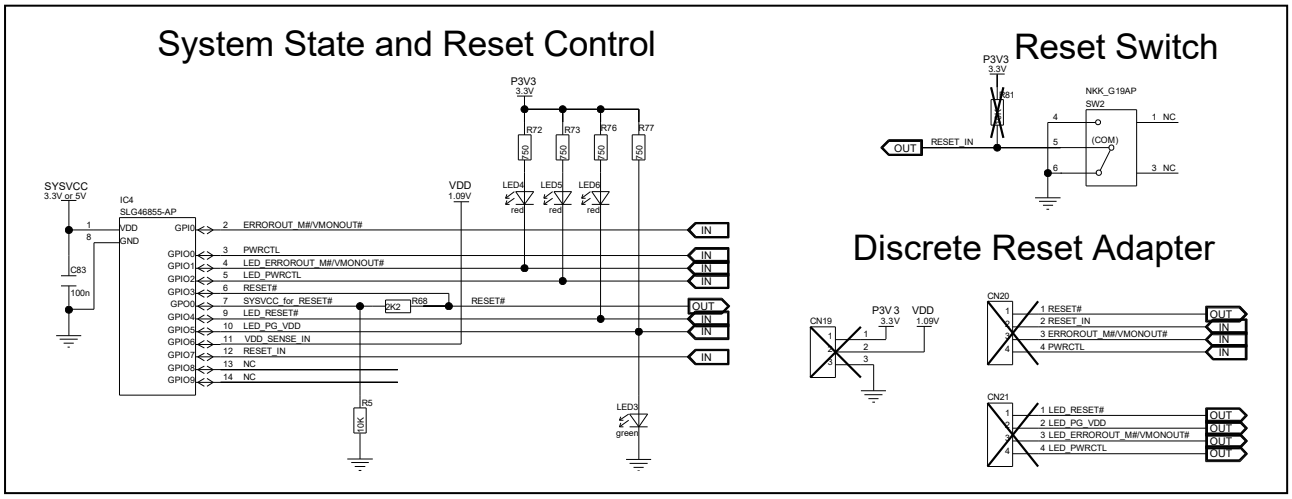


Figure 6.2 RESET circuit of board version D020145_06_V01

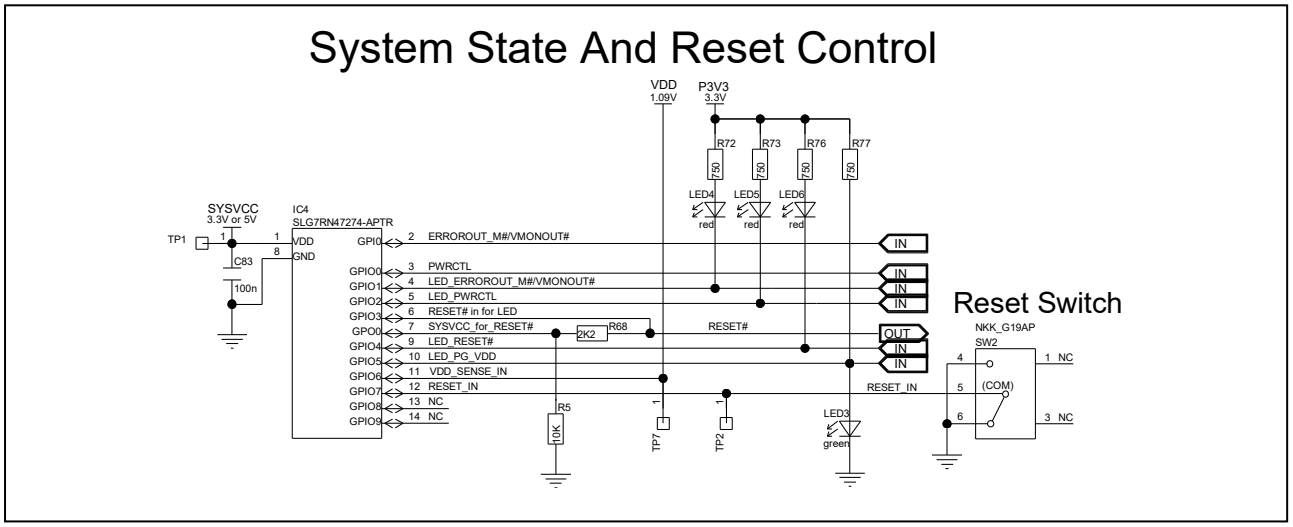


Figure 6.4 RESET circuit of board version D020145_06_V02.1

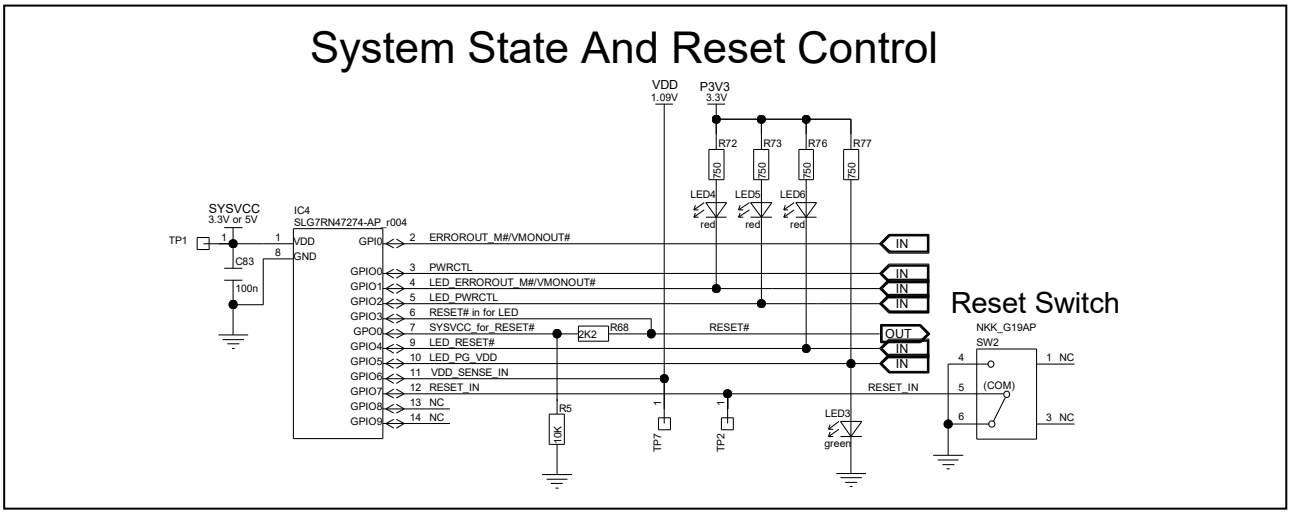


Figure 6.3 RESET circuit of board version D020145_06_V03 and later

6.2.1 RESET Switch

Switch SW2 is used to issue a reset to the RH850.

The SW2 toggle switch allows to activate the reset in two different ways:

- SW2 in left '5-4' (left) position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW2 in right '5-6' (right) position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

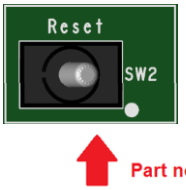


Figure 6.5 Operation of RESET switch

6.3 CAN-XL Port selection

Many I/O ports of RH850 are connected to multiple pins on the main board connectors CN1 – CN3. The ports P17_2/P17_3 and P24_7/P24_8, which support CAN XL interfaces, can also support several other functions.

On boards up to board version D020145_06_V03 these ports were directly connected to the CAN XL pins on connector CN1 (CN1[71-74]), and in parallel they were connected to other functions like SFMA, I2S, FlexRay and MMCA via 33 Ohm serial termination resistor.

But it turned out that this wiring causes problems in CAN XL communication at high speed.

So the circuit was modified for board version D020145_06_V0400.

Now the board has 2 pairs of multiplexers. Using the multiplexers the ports can either be connected to the CAN XL pins on connector CN1 or to the other secondary functions on connectors CN1 – CN3.

Ports P17_2 and P17_3 connections are controlled by jumper JP16.

Ports P24_7 and P24_8 connections are controlled by jumper JP21.

Table 6.2 Port P17_2 / P17_3 function selection

shows P17_2/P17_3 connections for different JP16 settings.

Table 6.3 shows P24_7/P24_8 connections for different JP21 settings.

Figure 6.6 shows the circuit diagrams for the multiplexers.

Table 6.2 Port P17_2 / P17_3 function selection

RH850 Port	JP16[OPEN]	JP16[CLOSED]
P17_2	CANXL0RX (CN1[73])	I2S1RXD (CN3[14]) SFMA0IO1 (CN2[82]) MOT0V_P (CN3[87])
P17_3	CANXL0TX (CN1[71])	I2S1TXD (CN3[12]) SFMA0IO0 (CN2[81]) MOT0V_N (CN3[89])

Table 6.3 Port P24_7 / P24_8 function selection

RH850 Port	JP21[OPEN]	JP21[CLOSED]
P24_7	CANXL1TX (CN1[72])	FLX1TX (CN1[45]) MMCA0DAT3 (CN2[92]) MUX0 (CN1[103])
P24_8	CANXL1RX (CN1[74])	FLX1RX (CN1[47]) MMCA0CLK (CN2[87])

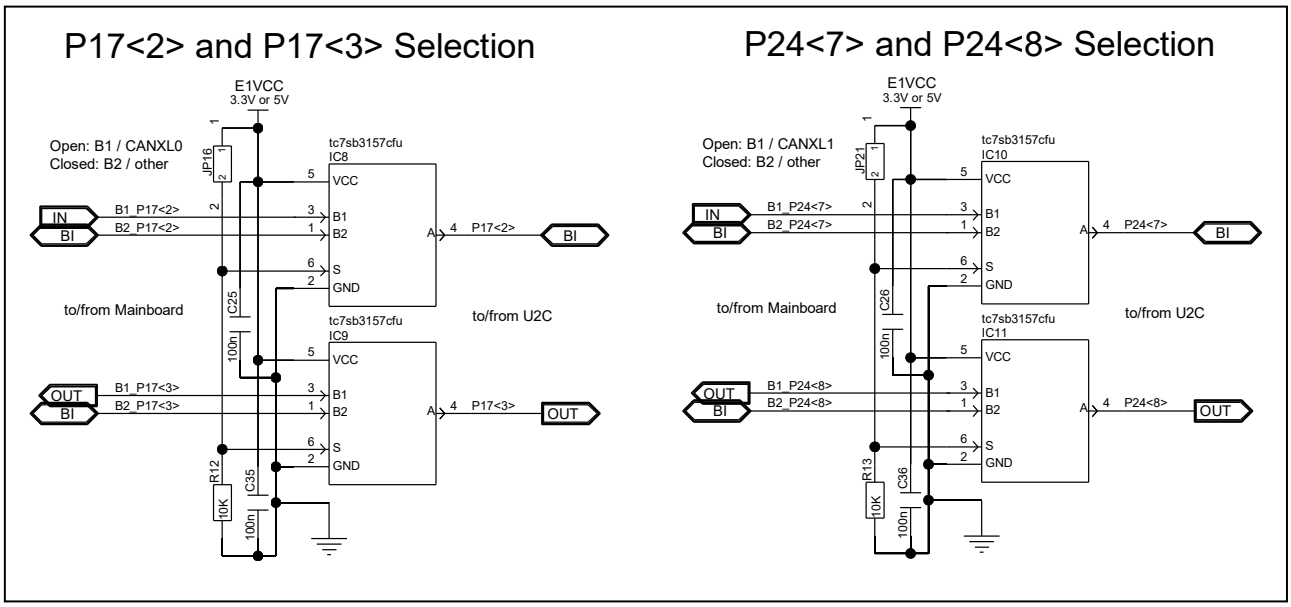


Figure 6.6 CAN XL port selection

6.4 Ethernet / I2S Selection

Port P20_0 can be used to provide either I2SMCLK or ETH0RXD0 signal to an attached main board.

Jumper JP17 is used to select which signal is being used.

Table 6.4 Ethernet / I2S selection

Jumper	Function
JP17 [OPEN]	B1_P20_0 = ETH0RXD0
JP17 [CLOSED]	B2_P20_0 = I2SMCLK

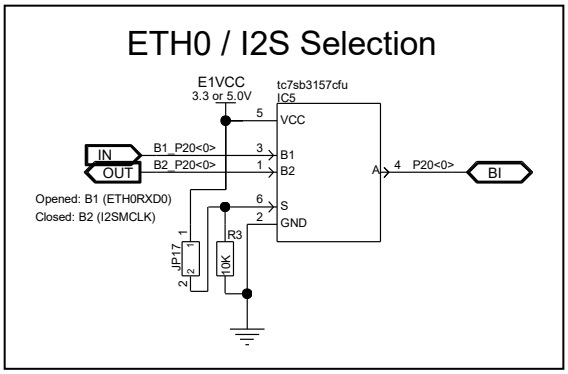


Figure 6.7 Circuit diagram for Ethernet and I2S signal selection

6.5 Ethernet 1 Control Ports MDIO / MDC

The piggyback board Y-RH850-U2C-292PIN-PB-T1-V1 provides the Ethernet 1 control signals ETH1MDIO and ETH1MDC to a connected main board on pins CN2_99 and CN2_100.

With board revision D020145_06_V01 the Ethernet 1 control signals ETH1MDIO and ETH1MDC are fixed to the ports P21_0 (ETH1MDIO) and P20_11 (ETH1MDC).

From board revision D020145_06_V02.1 onwards the control ports can be used either with ports P21_0 (ETH1MDIO) / P20_11 (ETH1MDC) or with ports P04_9 (ETH1MDIO) / P04_8 (ETH1MDC).

Jumper JP18 selects which ports are being used.

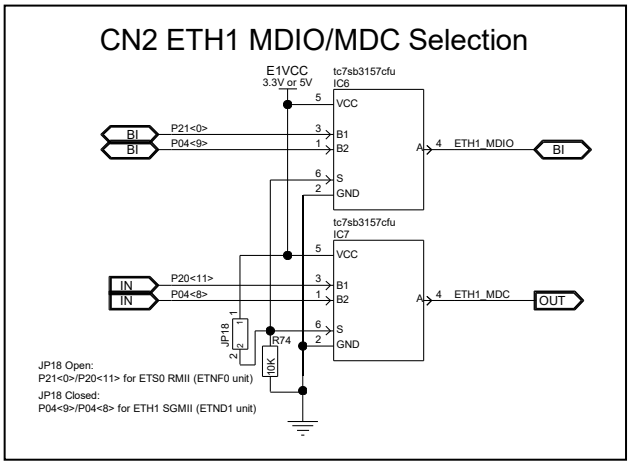


Figure 6.8 Circuit diagram for port selection for Ethernet control signals on board revision D020145_06_V02.1 and later

Table 6.5 Ethernet 1 control port selection from board revision D020145_06_V02.1 onwards

Jumper	Function	Remark
JP18 [OPEN]	ETH1_MDIO = P21_0 ETH1_MDC = P20_11	Used for ETS0 RMII interface (ETNF0)
JP18 [CLOSED]	ETH1_MDIO = P04_9 ETH1_MDC = P04_8	Used for ETH1 SGMII interface (ETND1)

6.6 Ethernet Control Port P20_3

From board revision D020145_06_V03 onwards the piggyback board Y-RH850-U2C-292PIN-PB-T1-V1 allows to use port P20_3 either as T1S_RX signal or as RMII_TXCLK signal.

The function is selected by jumper JP5:

- JP5[1-2]: P20_3 used as T1S_RX (pin 81 on connector CN1)
- JP5[2-3]: P20_3 used as RMII_TXCLK (pin 110 on connector CN2)

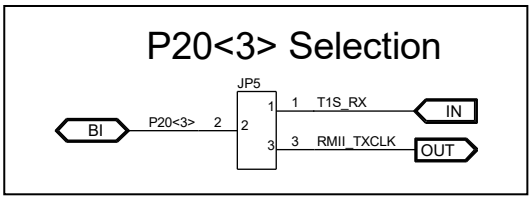


Figure 6.9 Circuit diagram for port selection for port P20_3 on board revision D020145_06_V03 and later

6.7 Series Termination Resistors

The piggyback board includes several series resistors, that can be used as termination resistors for high-speed communication channels. All signals are connected to the main board connectors CN1 – CN3.

On board revision D020145_06_V0400 the parallel connections of ports P17_2 and P17_3 to CAN XL and I2S1 ports and of ports P24_7 and P24_8 to CAN XL and FlexRay ports have been separated by multiplexers. The termination resistors R8 – R11 have been removed. Refer to chapter *6.3 CAN-XL Port selection* for details on the connection.

Table 6.6 lists all resistors and shows to which signal on the main board connector they are connected.

Figure 6.10 and *Figure 6.11* show the circuit diagrams for the series resistors.

Figure 6.12 shows the location of the resistors on the lower side of the –piggyback board.

Table 6.6 Series termination resistors

Resistor	RH850 Port	Signal Name	Connector
R8 *1	P24_7	CANXL1TX / FLX1TX	CN1_72 / CN1_45
R9 *1	P24_8	CANXL1RX / FLX1RX	CN1_74 / CN1_47
R10 *1	P17_2	CANXL0RX / I2S1RXD	CN1_73 / CN3_14
R11 *1	P17_3	CANXL0TX / I2S1TXD	CN1_71 / CN3_12
MR1_1	P21_2	ETH0TXD0	CN1_54
MR1_2	P21_3	ETH0TXD1	CN1_56
MR1_3	P20_10	ETH0TXD3	CN1_60
MR1_4	P20_9	ETH0TXD2	CN1_58
R1	P20_6	ETH0TXER	CN1_64
MR2_1	P22_0	ETH0MDC	CN1_52
MR2_2	P22_1	ETH0MDIO / FLXSTPWT	CN1_51 / CN1_44
MR2_3	P20_5	ETH0TXEN	CN1_66
MR2_4	P21_10	TH0RESET	CN1_69

*1 These resistors are only used on boards up to revision D020145_06_V03.

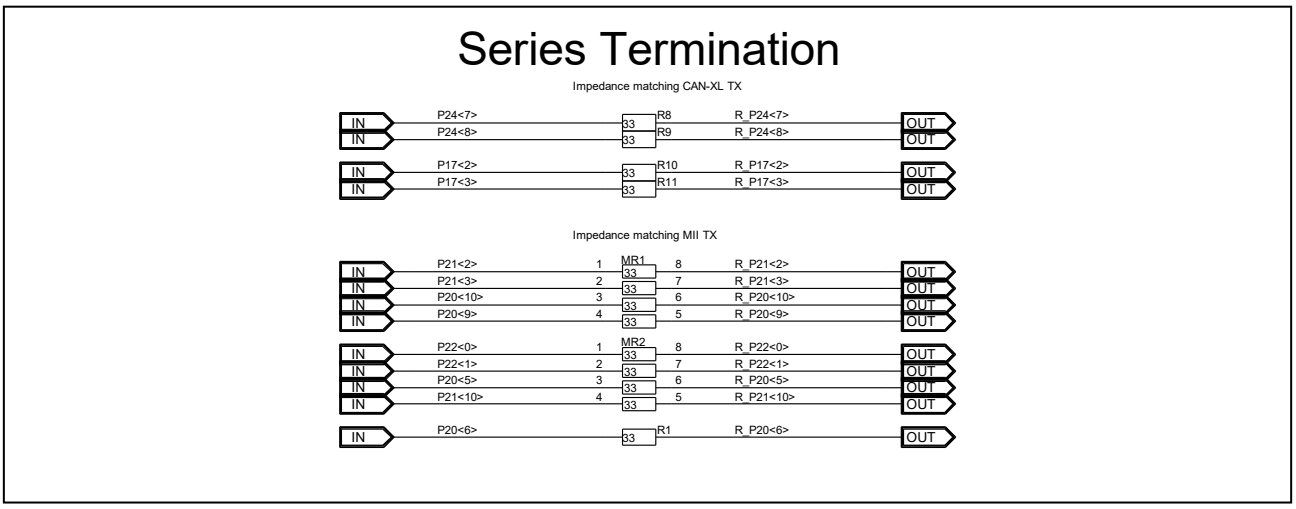


Figure 6.10 Series termination resistors up to board revision D020145_06_V03

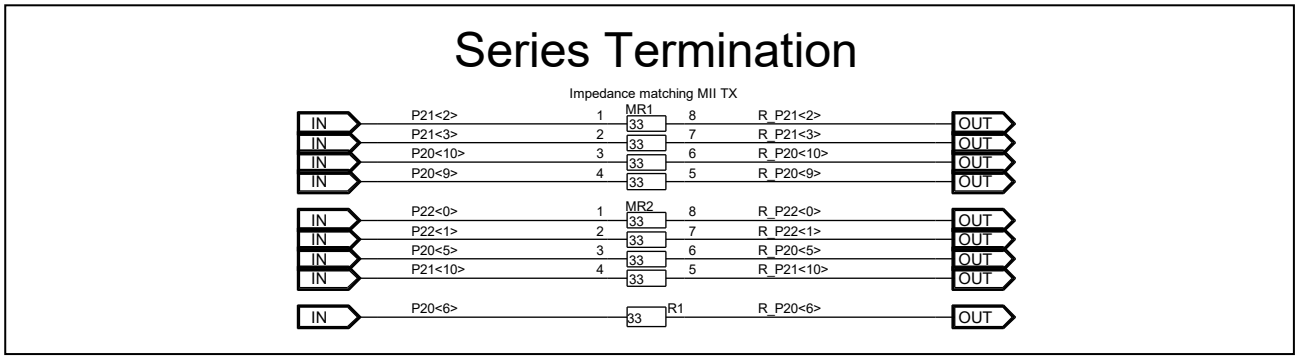


Figure 6.11 Series termination resistors from board revision D020145_06_V0400 onwards

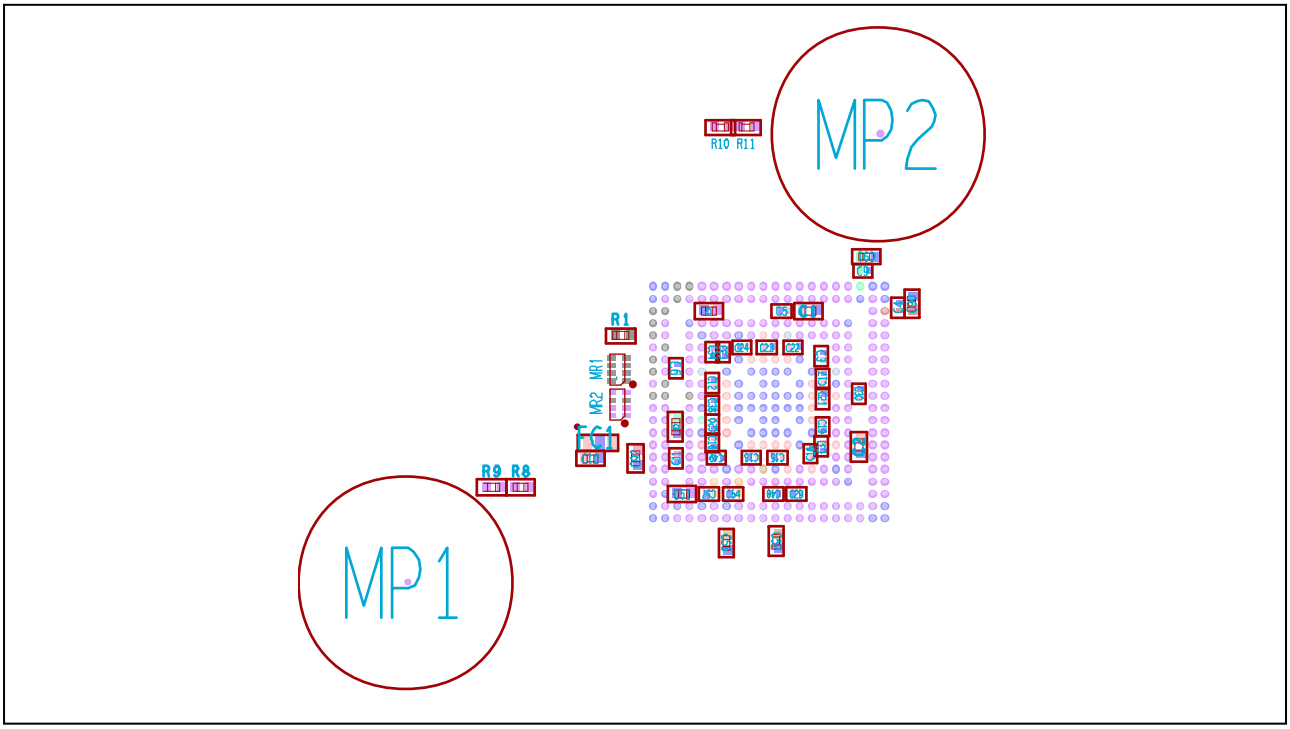


Figure 6.12 Location of series termination resistors

6.8 Signalling LEDs

Eight signalling LEDs provide users the possibility to output visual signals.

The device pins AP4_0 to AP4_2, P02_11, P02_14, P17_7, P21_8 and P21_9 are connected to the odd pins of pin header CN11 (on board revision D0201435_06_V01) or on jumper JP20 (on board revision D020145_06_V02.1 and later).

The LEDs LED10 to LED17 are connected to the even CN11/JP20 pins.

Thus, the LEDs can be either connected to

- the device port pins AP4_0 to AP4_2, P02_11, P02_14, P17_7, P21_8 and P21_9 by closing the connection on CN11/JP20 using a jumper, or
- any device pin by connecting the pin (from the connectors CN13, CN14 or CN15) directly to the even CN11/JP20 pins using separate cables.

Figure 6.13 and Figure 6.14 show the circuit diagrams of these LEDs for different board revisions.

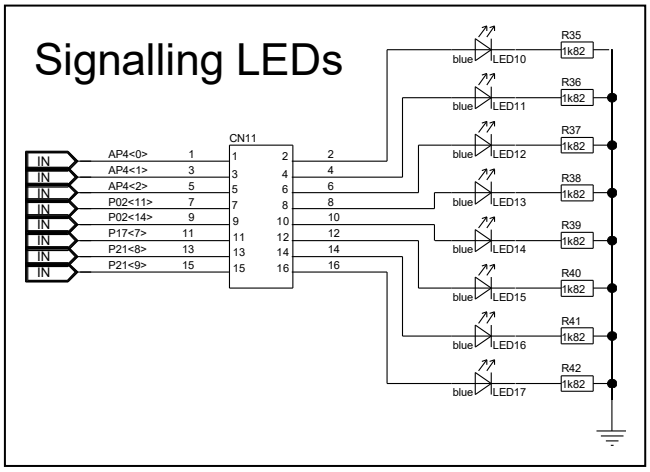


Figure 6.13 Circuit diagram for signalling LEDs on board revision D020145_06_V01

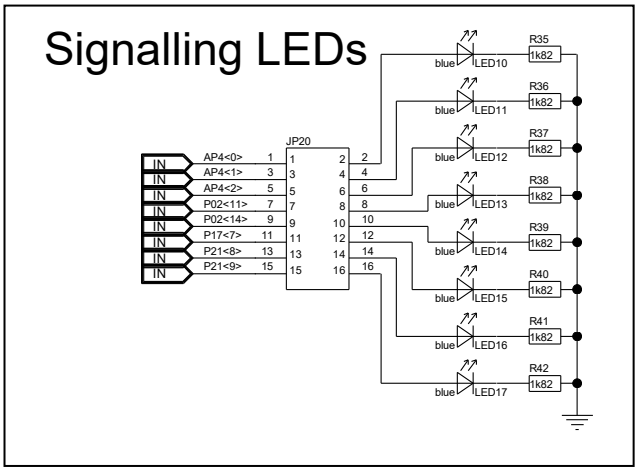


Figure 6.14 Circuit diagram for signalling LEDs from board revision D020145_06_V02.1 onwards

6.9 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins. These can be used to pull-up/pull-down signals on the board or the device by connecting the appropriate CN12 pins to the signals via a separate cables.

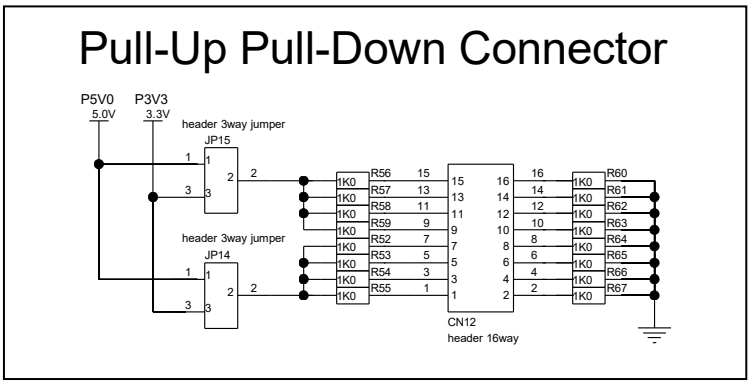


Figure 6.15 Circuit diagram for pull up / pull down signals

The CN12 pins have following pull-up or pull-down voltage levels:

- All even numbered pins are connected to L level, i.e. to GND.
- Odd numbered pins 1, 3, 5 and 7 are connected jumper JP14 and can be pulled up to 3.3 V or 5.0 V.
- Odd numbered pins 9, 11, 13 and 15 are connected jumper JP15 and can be pulled up to 3.3 V or 5.0 V.

Refer to *7.4 Pull-Up/Pull-Down Pin Header CN12* for CN12 details.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.

Refer to *1.2 Supported Main Boards* for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Function on		Device port
	Main Board	Piggyback	
1	VDDA	–	–
3	VDDA	–	–
5	RESET	RESET#	RESET#
7	WAKE	–	–
9	INT0	IRQ27	P06_12
11	INT2	IRQ16	P06_13
13	–	–	–
15	UART0TX	RLIN33TX	P06_3
17	UART0RX	RLIN33RX	P06_2
19	LIN0TX	RLIN30TX	P06_6
21	LIN0RX	RLIN30RX	P06_7
23	IIC0SCL	RI3C0SCL	P03_1
25	IIC0SDA	RI3C0SDA	P03_0
27	CAN0TX	CAN0TX	P02_2
29	CAN0RX	CAN0RX	P02_0
31	SENT0RX	RSENT2RX	P02_9
33	SENT0SPCO	RSENT2SPCO	P02_8
35	PSI5SRX0	–	–
37	PSI5STX0	–	–
39	PSI5SCLK0	–	–
41	FLX0TX	FLXA0TXDA	P24_12
43	FLX0RX	FLXA0RXDA	P24_11

Pin	Function on		Device port
	Main Board	Piggyback	
2	VDDA	–	–
4	VDDA	–	–
6	NMI	NMI	P02_3
8	–	–	–
10	INT1	IRQ34	P02_11
12	INT3	IRQ20	P10_14
14	–	–	–
16	UART1TX	RLIN36TX	P04_15
18	UART1RX	RLIN36RX	P04_14
20	LIN1TX	RLIN31TX	P06_4
22	LIN1RX	RLIN31RX	P06_5
24	IIC1SCL	RI3C1SCL	P06_8
26	IIC1SDA	RI3C1SDA	P06_9
28	CAN1TX	CAN1TX	P04_12
30	CAN1RX	CAN1RX	P04_13
32	SENT1RX	RSENT5RX	P22_3
34	SENT1SPCO	RSENT5SPCO	P22_4
36	PSI5RX0	–	–
38	PSI5TX0	–	–
40	–	–	–
42	FLX0EN	FLXA0TXENA	P24_10
44	FLXSTPWT	FLXA0STPWT	R_P22_1

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
45	FLX1TX	FLXA0TXDB	R_P24_7 *3 B2_P24_7 *4
47	FLX1RX	FLXA0RXDB	R_P24_8 *3 B2_P24_8 *4
49	–	–	–
51	ETH0MDIO	ETH0_MDIO	R_P22_1
53	ETH0RXD0	ETH0_MII_RXD0	B1_P20_0
55	ETH0RXD1	ETH0_MII_RXD1	P20_1
57	ETH0RXD2	ETH0_MII_RXD2	P10_1
59	ETH0RXD3	ETH0_MII_RXD3	P10_2
61	ETH0RXCLK	ETH0_MII_RX_CLK	P10_3
63	ETH0RXER	ETH0_RMII_ER	P20_12
65	ETH0CRSDV	–	–
67	ETH0RXDV	ETH0_MII_RX_DV	P20_2
69	ETH0RESET	P21_10	R_P21_10
71	CANXL0TX	CANXL0TXD	P17_3 *3 B1_P17_3 *4
73	CANXL0RX	CANXL0RXD	P17_2 *3 B1_P17_2 *4
75	CANXL2TX	–	–
77	CANXL2RX	–	–
79	ETH0_T1S_TX	ETS0_TX	P20_4
81	ETH0_T1S_ RX_MDC	ETS0_RX_MDC	P20_3 *1 T1S_RX *2
83	ETH0_T1S_ ED_MDIO	ETS0_ED_MDIO	P20_13
85	DIGIO_0	AP4_3	AP4_3 *5
87	DIGIO_2	AP4_5	AP4_5 *5
89	DIGIO_4	AP4_7	AP4_7 *5
91	DIGIO_6	AP4_1	AP4_1 *5
93	DIGIO_8	P02_11	P02_11
95	DIGIO_10	P17_7	P17_7
97	DIGIO_12	P21_9	P21_9
99	DIGIO_14	P06_3	P06_3
101	–	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
46	FLX1EN	FLXA0TXENB	P24_9
48	FLX1CLK	–	–
50	–	–	–
52	ETH0MDC	ETH0_MDC	R_P22_0
54	ETH0TXD0	ETH0_MII_TXD0	R_P21_2
56	ETH0TXD1	ETH0_MII_TXD1	R_P21_3
58	ETH0TXD2	ETH0_MII_TXD2	R_P20_9
60	ETH0TXD3	ETH0_MII_TXD3	R_P20_10
62	ETH0TXCLK	ETH0_MII_TX_CLK	P21_1
64	ETH0TXER	ETH0_MII_TX_ER	R_P20_6
66	ETH0TXEN	ETH0_MII_TX_EN	R_P20_5
68	ETH0COL	–	–
70	ETH0LINK	ETH0_LINKSTA	P22_2
72	CANXL1TX	CANXL1TXD	P24_7 *3 B1_P24_7 *4
74	CANXL1RX	CANXL1RXD	P24_8 *3 B1_P24_8 *4
76	CANXL3TX	–	–
78	CANXL3RX	–	–
80	ETH1_T1S_TX	–	–
82	ETH1_T1S_ RX_MDC	–	–
84	ETH1_T1S_ ED_MDIO	–	–
86	DIGIO_1	AP4_4	AP4_4 *5
88	DIGIO_3	AP4_6	AP4_6 *5
90	DIGIO_5	AP4_0	AP4_0 *5
92	DIGIO_7	AP4_2	AP4_2 *5
94	DIGIO_9	P02_14	P02_14
96	DIGIO_11	P21_8	P21_8
98	DIGIO_13	P06_2	P06_2
100	DIGIO_15	P06_4	P06_4
102	–	–	–

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
103	MUX0	P24_7	R_P24_7 *3 B2_P24_7 *4
105	MUX2	P22_3	P22_3
107	ADC0	ADCK1I12	AP2_12
109	ADC2	ADCK1I14	AP2_14
111	ADC4	ADCKAI16	AP1_0
113	ADC6	ADCKAI18	AP1_2
115	VDDIOF	VDDIOF	–
117	VDDB	P3V3_M	–
119	VDDB	P3V3_M	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
104	MUX1	P22_2	P22_2
106	–	–	–
108	ADC1	ADCK1I13	AP2_13
110	ADC3	ADCK1I17	AP3_1
112	ADC5	ADCKAI17	AP1_1
114	ADC7	ADCKAI19	AP1_3
116	VDDIOF	VDDIOF	–
118	VDDB	P3V3_M	–
120	VDDB	P3V3_M	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Up to board version D020145_06_V02.1
*2 Board version D020145_06_V03 or later
*3 Up to board version D020145_06_V03
*4 Board version D020145_06_V0400 or later
*5 Only RH850/U2C8

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function on		Device port
	Main Board	Piggyback	
1	CAN2TX	CAN2TX	P06_0
3	CAN2RX	CAN2RX	P06_1
5	CAN4TX	CAN4TX	P06_11
7	CAN4RX	CAN4RX	P06_12
9	LIN2TX	RLIN32TX	P06_0
11	LIN2RX	RLIN32RX	P06_1
13	LIN4TX	RLIN34TX	P04_9
15	LIN4RX	RLIN34RX	P04_8
17	LIN6TX	RLIN36TX	P04_15
19	LIN6RX	RLIN36RX	P04_14
21	LIN8TX	RLIN38TX	P02_1
23	LIN8RX	RLIN38RX	P02_0

Pin	Function on		Device port
	Main Board	Piggyback	
2	CAN3TX	CAN3TX	P10_7
4	CAN3RX	CAN3RX	P10_6
6	CAN5TX	CAN5TX	P02_7
8	CAN5RX	CAN5RX	P02_8
10	LIN3TX	RLIN33TX	P06_3
12	LIN3RX	RLIN33RX	P06_2
14	LIN5TX	RLIN35TX	P24_12
16	LIN5RX	RLIN35RX	P24_11
18	LIN7TX	RLIN37TX	P04_12
20	LIN7RX	RLIN37RX	P04_13
22	LIN9TX	RLIN39TX	P02_6
24	LIN9RX	RLIN39RX	P02_5

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
25	LIN10TX	RLIN310TX	P24_4
27	LIN10RX	RLIN310RX	P24_5
29	LIN12TX	RLIN312TX	P04_6
31	LIN12RX	RLIN312RX	P04_5
33	LIN14TX	RLIN314TX	P22_6
35	LIN14RX	RLIN314RX	P22_5
37	–	–	–
39	CAN12TX	CAN12TX *6	P08_3
41	CAN12RX	CAN12RX *6	P08_2
43	CAN14TX	–	–
45	CAN14RX	–	–
47	CAN6TX	CAN6TX *6	P21_6
49	CAN6RX	CAN6RX *6	P21_5
51	CAN8TX	CAN8TX *6	P03_10
53	CAN8RX	CAN8RX *6	P03_11
55	CAN10TX	CAN10TX *6	P04_3
57	CAN10RX	CAN10RX *6	P04_2
59	–	–	–
61	LIN16TX	RLIN316TX *6	P17_11
63	LIN16RX	RLIN316RX *6	P17_10
65	LIN18TX	RLIN318TX *6	P02_13
67	LIN18RX	RLIN318RX *6	P02_12
69	LIN20TX	–	–
71	LIN20RX	–	–
73	LIN22TX	–	–
75	LIN22RX	–	–
77	–	–	–
79	SFMA0CLK	SFMA0CLK	P17_5
81	SFMA0IO0	SFMA0IO0	R_P17_3 *4 B2_P17_3 *5
83	SFMA0IO2	SFMA0IO2	P17_1
85	–	–	–
87	MMCA0CLK	MMCA0CLK	R_P24_8 *4 B2_P24_8 *5
89	MMCA0DAT0	MMCA0DAT0	P24_10

Pin	Function on		Device port
	Main Board	Piggyback	
26	LIN11TX	RLIN311TX	P10_12
28	LIN11RX	RLIN311RX	P10_11
30	LIN13TX	RLIN313TX	P02_4
32	LIN13RX	RLIN313RX	P02_3
34	LIN15TX	RLIN315TX *6	P17_13
36	LIN15RX	RLIN315RX *6	P17_12
38	–	–	–
40	CAN13TX	CAN13TX *6	P08_0
42	CAN13RX	CAN13RX *6	P08_1
44	CAN15TX	–	–
46	CAN15RX	–	–
48	CAN7TX	CAN7TX *6	P04_1
50	CAN7RX	CAN7RX *6	P04_0
52	CAN9TX	CAN9TX *6	P04_9
54	CAN9RX	CAN9RX *6	P04_8
56	CAN11TX	CAN11TX *6	P04_11
58	CAN11RX	CAN11RX *6	P04_10
60	–	–	–
62	LIN17TX	RLIN317TX *6	P17_9
64	LIN17RX	RLIN317RX *6	P17_8
66	LIN19TX	–	–
68	LIN19RX	–	–
70	LIN21TX	–	–
72	LIN21RX	–	–
74	LIN23TX	RLIN323TX	P06_9
76	LIN23RX	RLIN323RX	P06_8
78	–	–	–
80	SFMA0SSL	SFMA0SSL	P17_4
82	SFMA0IO1	SFMA0IO1	R_P17_2 *4 B2_P17_2 *5
84	SFMA0IO3	SFMA0IO3	P17_0
86	–	–	–
88	MMCA0CMD	MMCA0CMD	P24_9
90	MMCA0DAT1	MMCA0DAT1	P24_11

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
91	MMCA0DAT2	MMCA0DAT2	P24_12
93	MMCA0DAT4	MMCA0DAT4	P24_4
95	MMCA0DAT6	MMCA0DAT6	P24_6
97	–	–	–
99	ETH1MDIO	ETS0_MDIO	P21_0 *1 ETH1_MDIO *2
101	ETH1RXD0	ETS0_RMII_RXD0	P10_4
103	ETH1RXD1	ETS0_RMII_RXD1	P10_5
105	ETH1RXD2	–	–
107	ETH1RXD3	–	–
109	ETH1RXCLK	–	–
111	ETH1RXER	–	–
113	ETH1CRSDV	ETS0_RMII_CRSDV	P10_10
115	ETH1RXDV	–	–
117	ETH1RESET	P10_9	P10_9
119	–	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
92	MMCA0DAT3	MMCA0DAT3	R_P24_7 *4 B2_P24_7 *5
94	MMCA0DAT5	MMCA0DAT5	P24_5
96	MMCA0DAT7	MMCA0DAT7	P24_13
98	–	–	–
100	ETH1MDC	ETS0_MDC	P20_11 *1 ETH1_MDC *2
102	ETH1TXD0	ETS0_RMII_TXD0	P20_8
104	ETH1TXD1	ETS0_RMII_TXD1	P20_7
106	ETH1TXD2	–	–
108	ETH1TXD3	–	–
110	ETH1TXCLK	ETS0_RMII_ REFCLK	P20_3 *1 *2 RMII_TXCLK *3
112	ETH1TXER	–	–
114	ETH1TXEN	ETS0_RMII_TXEN	P10_0
116	ETH1COL	–	–
118	ETH1LINK	–	–
120	–	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Board version D020145_06_V01
*2 Board version D020145_06_V02.1 or later
*3 Board version D020145_06_V03 or later
*4 Up to board version D020145_06_V03
*5 Board version D020145_06_V0400 or later
*6 Only RH850/U2C8

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function on		Device port
	Main Board	Piggyback	
1	CSI0CS0	MSPI0CSS0	P06_9
3	CSI0CS1	MSPI0CSS1	P06_8
5	CSI0CS2	MSPI0CSS6	P06_11
7	CSI0CS3	MSPI0CSS7	P06_10

Pin	Function on		Device port
	Main Board	Piggyback	
2	CSI0CLK	MSPI0SC	P06_6
4	CSI0SI (MSPI3)	MSPI0SI	P06_5
6	CSI0SO	MSPI0SO	P06_7
8	–	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
9	–	–	–
11	I2S0TXD	–	–
13	I2S0RXD	–	–
15	I2S0BCLK	–	–
17	I2S0LRCLK	–	–
19	I2SMCLK	SSIFACK	B2_P20_0
21	CSI1CS2	MSPI1CSS5	P04_5
23	–	–	–
25	–	–	–
27	–	–	–
29	CSI1SCLK	MSPI1SC	P02_3
31	–	–	–
33	MOT0ADU	ADCKAI0	AP0_0
35	MOT0ADV	ADCKAI1	AP0_1
37	MOT0ADW	ADCKAI2	AP0_2
39	MOT0RDCS1	ADCKAI3	AP0_3
41	MOT0RDCS3	ADCKAI4	AP0_4
43	MOT0RDCS2	ADCKAI5	AP0_5
45	MOT0RDCS4	ADCKAI6	AP0_6
47	MOT0RDCCOM	ADCKAI7	AP0_7
49	MOT0RDCRSO	ADCKAI8	AP0_8
51	–	–	–
53	–	–	–
55	AD1_0	ADCKAI9	AP0_9
57	AD1_2	ADCKAI11	AP0_11
59	AD1_4	ADCKAI13	AP0_13
61	AD1_6	ADCKAI15	AP0_15
63	PWM0	PWGC32O	P02_0
65	PWM2	PWGC41O	P02_2
67	PWM4	PWGC43O	P02_4

Pin	Function on		Device port
	Main Board	Piggyback	
10	CSI1CS1	MSPI1CSS2	P02_6
12	I2S1TXD	SSIF1TXD	R_P17_3 *5 B2_P17_3 *6
14	I2S1RXD	SSIF1RXD	R_P17_2 *5 B2_P17_2 *6
16	I2S1BCLK	SSIF1BCK	P17_4
18	I2S1LRCLK	SSIF1LRCK	P17_5
20	–	–	–
22	CSI1CS3	MSPI1CSS6	P04_6
24	CSI1CS0	MSPI1CSS0	P02_2
26	DIGIO_24	MSPI1CSS4	P04_4
28	CSI1SO	MSPI1SO	P02_5
30	CSI1SI	MSPI1SI	P02_4
32	–	–	–
34	MOTAD0 *3 MOT1ADU *2	ADCK1I0	AP2_0
36	MOTAD1 *3 MOT1ADV *2	ADCK1I1	AP2_1
38	MOTAD2 *3 MOT1ADW *2	ADCK1I2	AP2_2
40	MOT1RDCS1	ADCK1I3	AP2_3
42	MOT1RDCS3	ADCK1I4	AP2_4
44	MOT1RDCS2	ADCK1I5	AP2_5
46	MOT1RDCS4	ADCK1I6	AP2_6
48	MOT1RDCCOM	ADCK1I7	AP2_7
50	MOT1RDCRSO	ADCK1I8	AP2_8
52	–	–	–
54	–	–	–
56	AD1_1	ADCKAI10	AP0_10
58	AD1_3	ADCKAI12	AP0_12
60	AD1_5	ADCKAI14	AP0_14
62	AD1_7	ADCK1I18	AP3_2
64	PWM1	PWGC33O	P02_1
66	PWM3	PWGC42O	P02_3
68	PWM5	PWGC44O	P02_5

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
69	PWM6	PWGC45O	P02_6
71	DIGIO16	P02_10	P02_10
73	DIGIO18	P04_7	P04_7
75	DIGIO20	P10_14	P10_14
77	DIGIO22	P21_4	P21_4
79	ENC0	ENCA0E0	P02_9
81	MOT0ERR	–	–
83	MOT0U_P	TSG30O1	P17_0
85	MOT0U_N	TSG30O2	P17_1
87	MOT0V_P	TSG30O3	R_P17_2 *5 B2_P17_2 *6
89	MOT0V_N	TSG30O4	R_P17_3 *5 B2_P17_3 *6
91	MOT0W_P	TSG30O5	P17_4
93	MOT0W_N	TSG30O6	P17_5
95	–	–	–
97	–	–	–
99	–	–	–
101	GND	–	–
103	AD2_0	ADCK1I9	AP2_9
105	AD2_1	ADCK1I10	AP2_10
107	AD2_2	ADCK1I11	AP2_11
109	AD2_3	ADCK1I12	AP2_12
111	AD2_4	ADCK1I13	AP2_13
113	AD2_5	ADCK1I14	AP2_14
115	AD2_6	ADCK1I15	AP2_15

Pin	Function on		Device port
	Main Board	Piggyback	
70	PWM7	PWGC50O	P02_7
72	DIGIO17	P22_2	P22_2
74	DIGIO19	P10_8	P10_8
76	DIGIO21	P17_6	P17_6
78	DIGIO23	P21_7	P21_7
80	ENC1	ENCA0E1	P10_11
82	MOT1ERR	TAPA0ESO	P06_6
84	MOT1U_P	TAPA0UP	P06_1
86	MOT1U_N	TAPA0UN	P06_0
88	MOT1V_P	TAPA0VP	P06_5
90	MOT1V_N	TAPA0VN	P06_4
92	MOT1W_P	TAPA0WP	P06_3
94	MOT1W_N	TAPA0WN	P06_2
96	–	–	–
98	–	–	–
100	ETH0_SO_P	ETH1_SG_TXD_P *7	CN_ETH1_ SG_TXD_P *1 – *4
102	ETH0_SO_N	ETH1_SG_TXD_N *7	CN_ETH1_ SG_TXD_N *1 – *4
104	–	–	–
106	ETH0_SI_P	ETH1_SG_RXD_P *7	ETH1_SG_ RXD_P *1 – *4
108	ETH0_SI_N	ETH1_SG_RXD_N *7	ETH1_SG_ RXD_N *1 – *4
110	–	–	–
112	ETH1_SO_P	ETH1_SG_TXD_P *7	– *1 CN_ETH1_ SG_TXD_P *4
114	ETH1_SO_N	ETH1_SG_TXD_N *7	– *1 CN_ETH1_ SG_TXD_N *4
116	–	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
117	AD2_7	ADCK1I16	AP3_0
119	GND	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
118	ETH1_SI_P	ETH1_SG_RXD_P *7	– *1 ETH1_SG_RXD_P *4
120	ETH1_SI_N	ETH1_SG_RXD_N *7	– *1 ETH1_SG_RXD_N *4
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Board version D020145_06_V01
*2 Board version D020145_06_V02.1
*3 Board version D020145_06_V01, D020145_06_V03 and later
*4 Board version D020145_06_V02.1 and later
*5 Up to board version D020145_06_V03
*6 Board version D020145_06_V0400 or later
*7 Only RH850/U2C8

7.2 Debug Connector CN9

Table 7.4 On-chip debug connector CN9

Pin	Function	Device port
1	TCK / LPDCLK	JP0_2
3	TRST# / LPDRST#	TRST#_TOOL
5	TDO / LPDO	JP0_1
7	TDI / LPDI(LPDIO)	JP0_0
9	TMS / –	JP0_3
11	RDY# / LPDCLKO	JP0_5
13	RESET#	RESET#

Pin	Function	Device port
2	GND	GND
4	FPMD0	FLMD0_TOOL
6	–	–
8	TVDD	E0VCC
10	EVTO	EVTO0#_P10_14
12	GND	GND
14	GND	GND

7.3 Device Ports Connectors CN13, CN14 and CN15

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.3.1 Device Ports Connector CN13

Table 7.5 Device ports connector CN13

Pin	Device port	Pin	Device port
1	AP1_1	2	AP1_0
3	AP0_3	4	AP0_2
5	AP0_1	6	AP0_0
7	AP2_0	8	AP2_2
9	AP2_6	10	AP2_4
11	AP2_1	12	AP2_10
13	AP2_8	14	AP2_5
15	AP2_3	16	AP2_12
17	AP2_13	18	AP2_9
19	AP2_7	20	AP2_14
21	AP2_15	22	AP3_1
23	AP2_11	24	AP3_0
25	AP3_2	26	AP3_3
27	P10_13	28	P10_14
29	P17_12	30	P17_13
31	P10_11	32	P10_12
33	P17_11	34	P17_5
35	P17_6	36	P17_10
37	P10_9	38	P17_3
39	P17_4	40	P10_8
41	P17_1	42	P17_2
43	P17_0	44	P10_7
45	P10_10	46	P17_8
47	P17_9	48	P10_5
49	P10_6	50	P17_7
51	P10_3	52	P10_4
53	P10_1	54	P10_2
55	P10_0	56	P20_0

Table 7.5 Device ports connector CN13 (cont'd)

Pin	Device port	Pin	Device port
57	P20_1	58	P20_2
59	P20_3	60	R_P20_6
61	P20_7	62	P21_5
63	P20_8	64	R_P20_9
65	P21_6	66	R_P20_10
67	P20_11	68	P20_4
69	P21_7	70	P20_12
71	P20_13	72	P21_8
73	P21_0	74	P21_1
75	P21_4	76	P21_9
77	R_P21_2	78	R_P21_3
79	R_P20_5	80	R_P21_10

7.3.2 Device Ports Connector CN14

Table 7.6 Device ports connector CN14

Pin	Device port	Pin	Device port
1	P06_1	2	P06_2
3	P08_2	4	P08_1
5	P04_1	6	P04_0
7	P04_2	8	P08_3
9	P04_14	10	P04_3
11	P04_12	12	P04_15
13	P02_14	14	P04_13
15	P04_9	16	P04_8
17	P04_11	18	P04_10
19	P02_11	20	P02_13
21	P04_7	22	P02_12
23	P04_6	24	P02_10
25	P03_12	26	P04_5
27	P04_4	28	P02_9
29	P03_11	30	P03_10
31	P02_8	32	P02_7
33	P02_6	34	P02_3
35	P02_1	36	P02_5
37	P02_4	38	P03_0

Table 7.6 Device ports connector CN14 (cont'd)

Pin	Device port	Pin	Device port
39	RESETOUT#	40	P03_1
41	P02_2	42	P02_0
43	GETH0BVCC	44	P00_7
45	TRST#	46	–
47	RESET#	48	ETH1_SG_REFCLK / P00_1
49	FLMD0	50	X2_C
51	GETH0VCL	52	X1_C
53	AP4_7	54	AWOVCL
55	PWRCTL	56	AP4_6
57	P24_12	58	ERROROUT_M# / VMONOUT#
59	P24_13	60	P24_11
61	P24_10	62	P24_9
63	AP4_5	64	AP4_4
65	P24_8	66	P24_7
67	AP4_3	68	AP4_2
69	P24_6	70	P24_5
71	R_P22_0	72	AP4_1
73	AP4_0	74	P24_4
75	R_P22_1	76	P22_2
77	P22_4	78	P22_6
79	P22_5	80	P22_3

7.3.3 Device Ports Connector CN15

Table 7.7 Device ports connector CN15

Pin	Device port	Pin	Device port
1	GND	2	GND
3	–	4	–
5	–	6	–
7	AP0_4	8	AP0_5
9	AP1_2	10	AP1_3
11	AP0_6	12	AP0_7
13	AP0_12	14	AP0_13
15	AP0_8	16	AP0_9
17	AP0_14	18	AP0_10
19	AP0_11	20	AP0_15
21	P06_12	22	P06_13

Table 7.7 Device ports connector CN15 (cont'd)

Pin	Device port	Pin	Device port
23	P06_9	24	P06_10
25	P06_11	26	P06_3
27	P06_4	28	P06_7
29	–	30	P06_8
31	P06_5	32	P06_6
33	P08_0	34	P06_0
35	–	36	–
37	–	38	–
39	GND	40	GND

7.4 Pull-Up/Pull-Down Pin Header CN12

Table 7.8 Pull-up and pull-down signal connector CN12

Pin	Function	Pin	Function
1	Level set by jumper JP14: JP14 [1-2]: 5.0 V (P5V0) JP14 [2-3]: 3.3 V (P3V3)	2	Fixed “L” level
3		4	
5		6	
7		8	
9	Level set by jumper JP15: JP15 [1-2]: 5.0 V (P5V0) JP15 [2-3]: 3.3 V (P3V3)	10	
11		12	
13		14	
15		16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically, the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings

All the following board configurations are based on these conditions:

- Normal device operation mode (JP7[OPEN]: FLMD0 = L). When Serial Programming Mode is used by a debugger or programming tool, that is connected to the board, make sure to set JP8 (JP8[CLOSED]: FLMD1 = GND).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN5 (GND), CN6 (+5.0 V) and CN7 (+3.3 V) are assembled on the board.
- If also the core supply voltage of 1.09 V is supplied from an external power supply, the connector CN8 (included in the package) must be assembled on the pcb.

The pictures of the jumper configurations show the settings for eVR devices and DPS devices. On boards up to revision D020145_06_V03 only DPS devices should be used and thus the settings for DPS devices apply.

The pictures always show the jumper configuration for the latest board revision. But the jumper locations are the same for all board revisions, except for the board production test jumper JP19 (it has been added in board revision D020145_06_V02.1). So the shown jumper setting can be used on all board revisions.

8.2.2 Jumper Indicators

The green jumper JP7 for FLMD0 must always be open for ‘normal’ (user mode and debug) operation of the device.

The yellow jumper JP19 is for production test only and must not be set.

The red jumpers are related to the power supply configuration.
Following jumper symbols are used:

-  : Jumper must not be set.
- 

: Jumper must be set in the indicated position

- 1 2 3: Jumper can be set to position [1-2] or position [2-3]
- 1 2 3: Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.2.3 Core Voltage Supply for eVR and DPS Devices

RH850/U2C4 devices are available with different core voltage supply:

- Devices with embedded voltage regulator (eVR device)
- Devices with external core voltage supply (DPS device)

RH850/U2C8 devices are available only as DPS device with external core voltage supply.

The jumper configurations in the following chapters show separate jumper settings for eVR and DPS devices.

CAUTION

If the device being used is RH850/U2C with eVR core power supply (R7F702613 or R7F702616) JP2 must be open. If JP2 is set to either position the device may be damaged.

8.2.4 Stand-Alone Operation with Single External Power Supply 3.3 V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is generated using the on-board voltage regulator IC3. All I/O ports can only use 3.3 V.

Table 8.1 Power supply connectors for single power supply 3.3 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Not connected	Jumpers in JP1 (VCC and VREF selection) are set to 3.3 V position
CN7	3.3 V	Connected, +3.3 V	
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT) Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

CAUTION

This setting cannot be used with RH850/U2C4 with eVR core power supply, VCC = 4.5 V – 5.5 V (R7F702616).

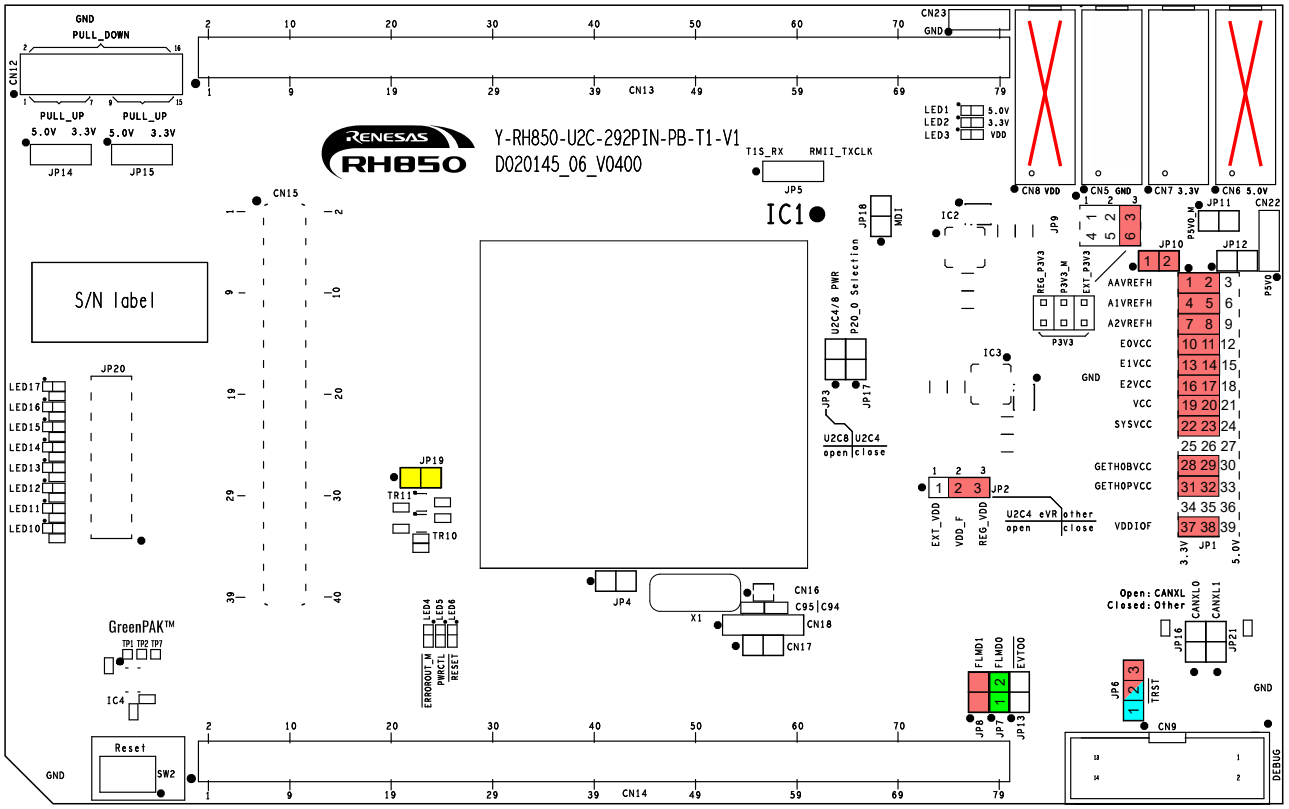


Figure 8.1 Stand-alone operation with 3.3 V external power supply for DPS devices

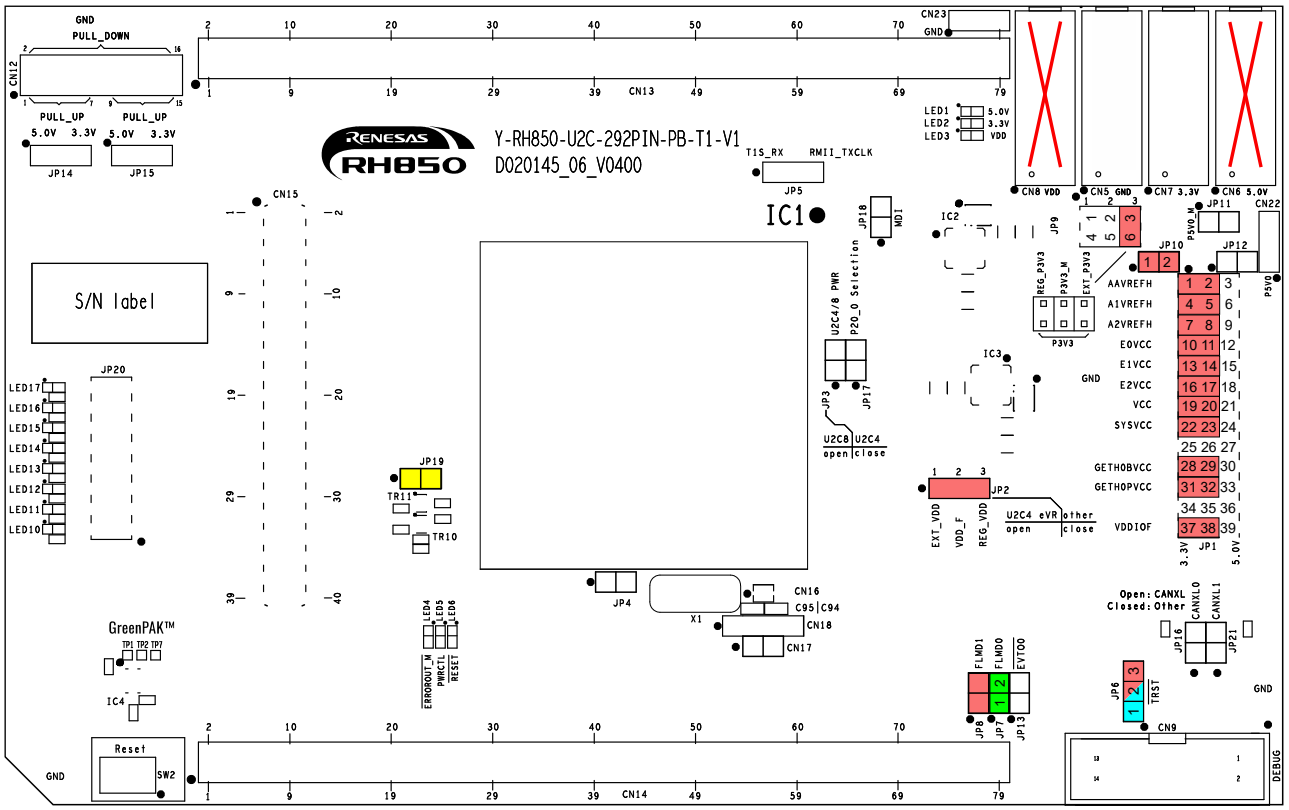


Figure 8.2 Stand-alone operation with 3.3 V external power supply for eVR devices

8.2.5 Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can use 5.0 V from external supply or 3.3 V from on-board voltage regulator.

Table 8.2 Power supply connectors for single power supply 5.0 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	
CN7	3.3 V	Not connected	3.3 V supply (P3V3) from on-board voltage regulator IC2 (JP9[1-4] = SHORT)
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT) Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

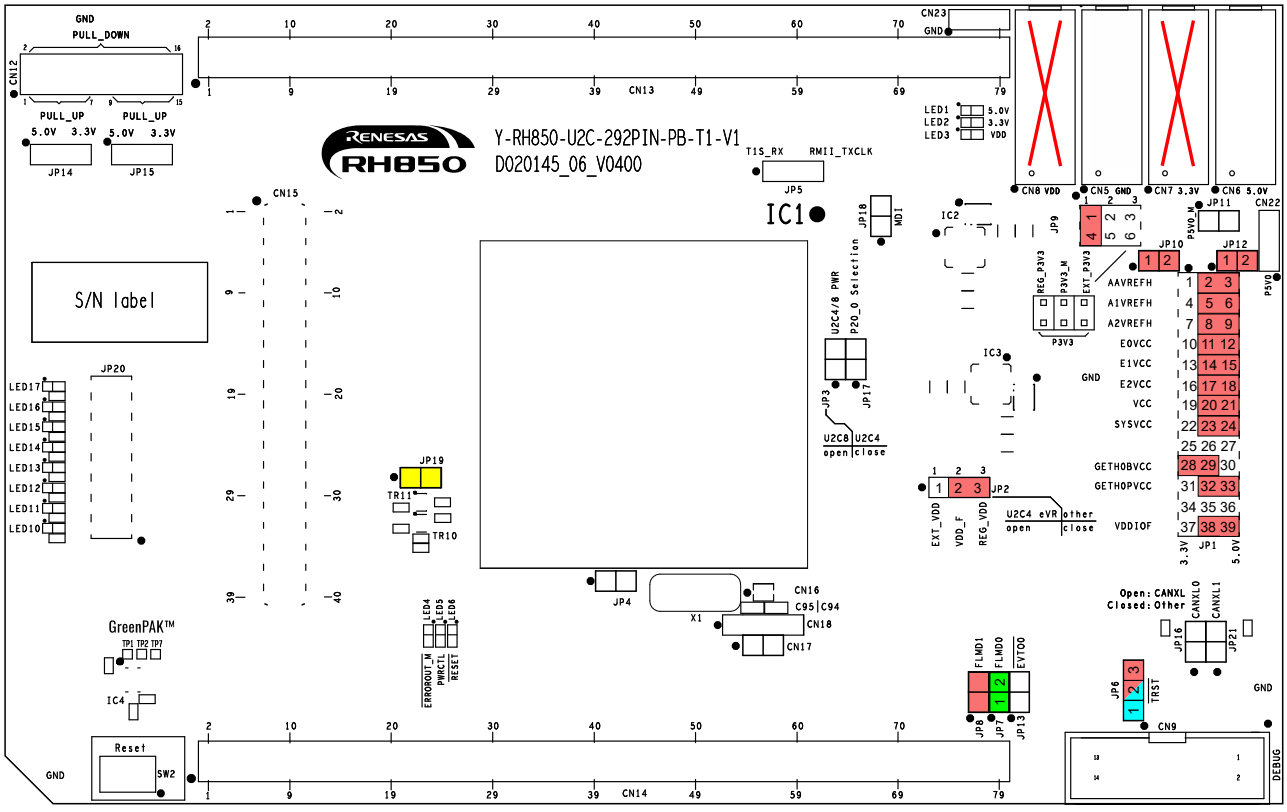


Figure 8.3 Stand-alone operation with 5.0 V external power supply for DPS devices

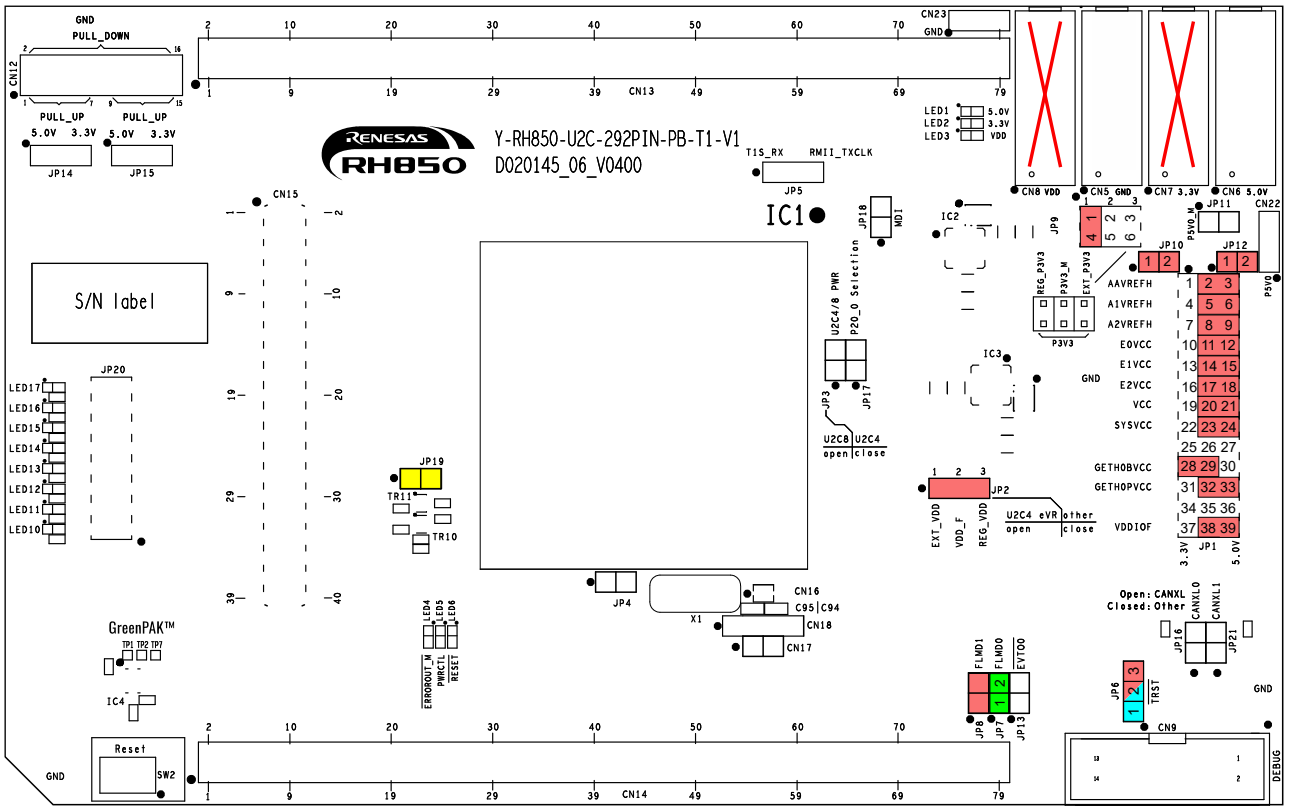


Figure 8.4 Stand-alone operation with 5.0 V external power supply for eVR devices

8.2.6 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.3 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. JP9[3-6] = SHORT: use Ext_P3V3 supply for 3.3 V supply. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	DPS devices: Connected, 1.09 V eVR devices: Not connected	DPS device: VDD from external VDD supply (P1V09_EXT) (JP2[1-2] = SHORT) eVR device: VDD from internal voltage regulator (JP2[OPEN]) Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

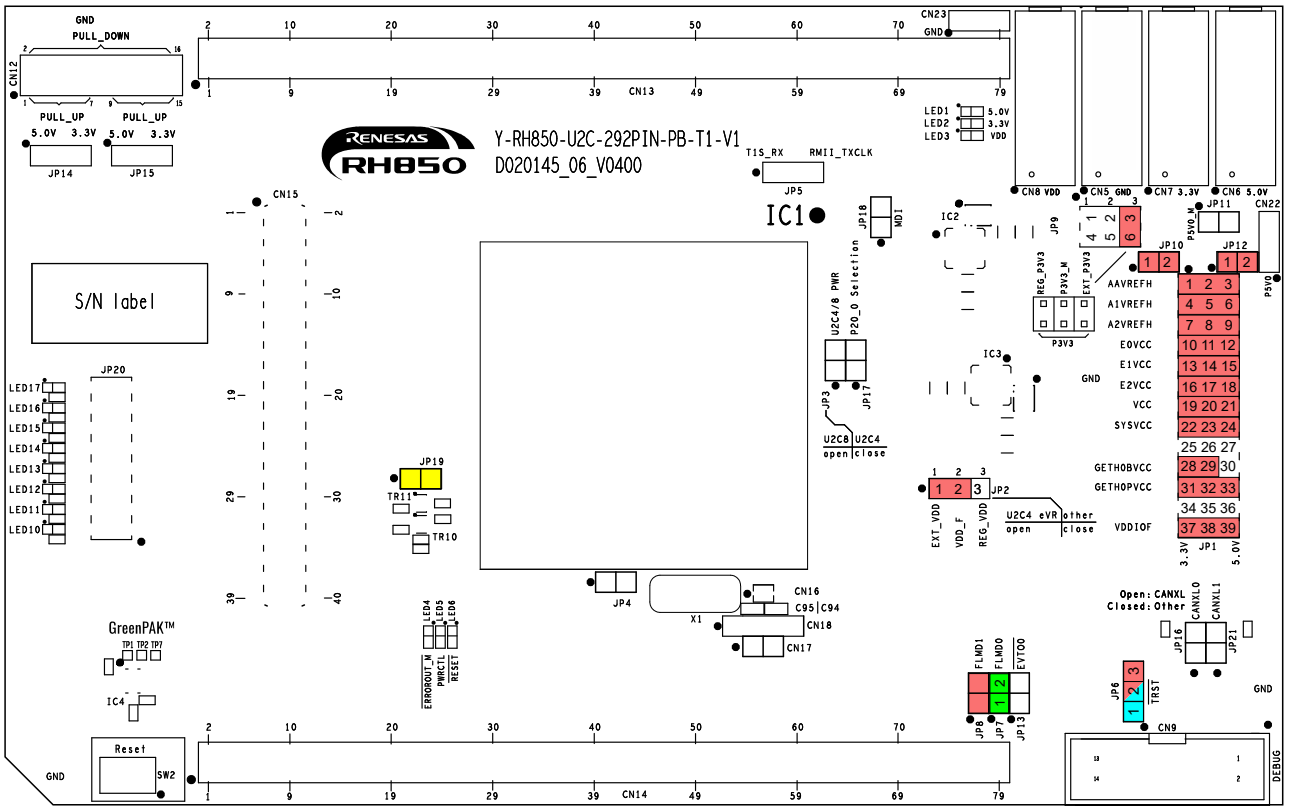


Figure 8.5 Stand-alone operation with all external power supplies for DPS devices

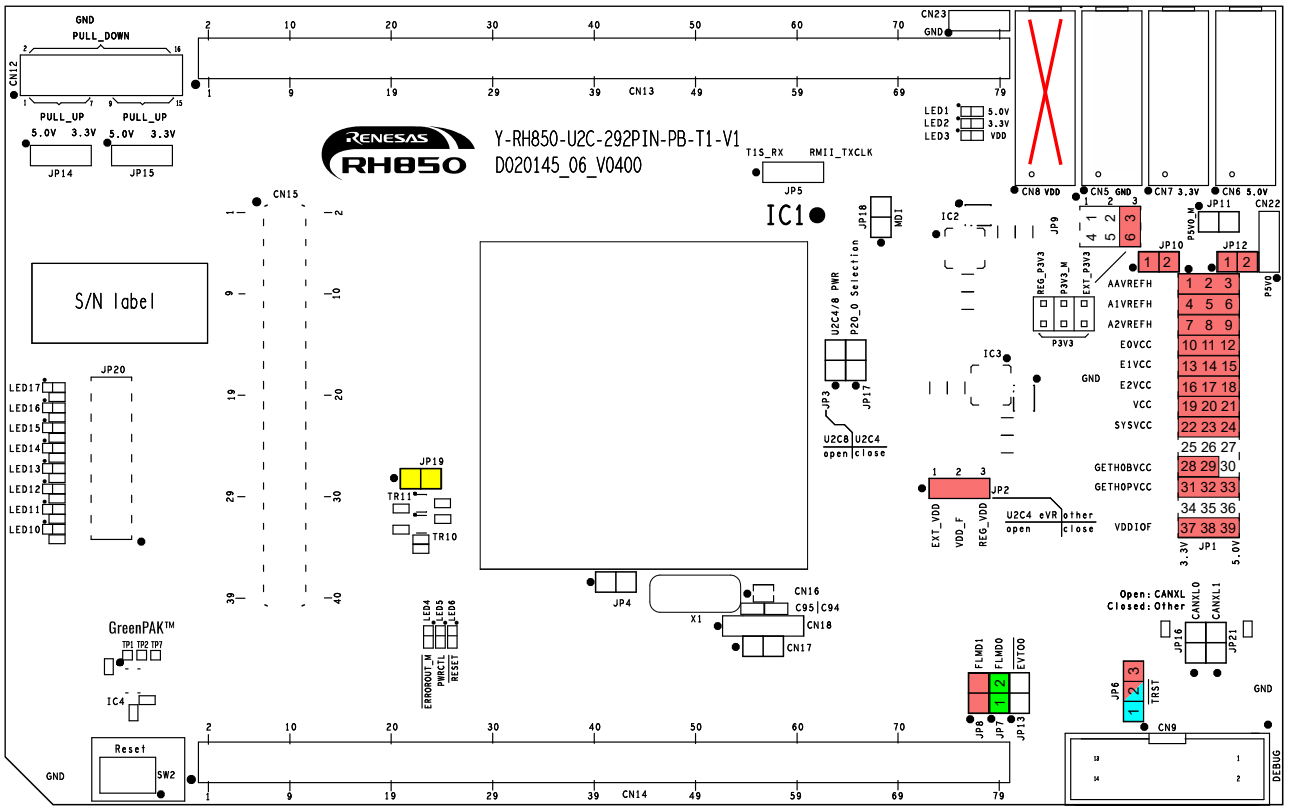


Figure 8.6 Stand-alone operation with all external power supplies for eVR devices

8.2.7 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

The jumpers JP11 (P5V0) and JP9 (P3V3) must be set to connect the main board supply voltages P5V0_M and P3V3_M to the piggyback board power supply rails P5V0 and P3V3.

Do not supply the 5.0 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board.

Table 8.4 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Not connected	
CN6	5.0 V	Not connected	Use jumper JP11[1-2] to connect the 5.0 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Not connected	Use jumper JP9[2-5] to connect the 3.3 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	Not connected	VDD from on-board voltage regulator IC3 (REG_P1V09) (JP2[2-3] = SHORT). Refer to *3.3 Device Core Voltage Selection* for further details about VDD voltage.

Note

For DPS devices this configuration still allows to utilize an external P1V09_EXT voltage (connected to CN8) as the source for VDD voltage. When using external VDD make sure to set jumper JP2[1-2] = SHORT to use external VDD.

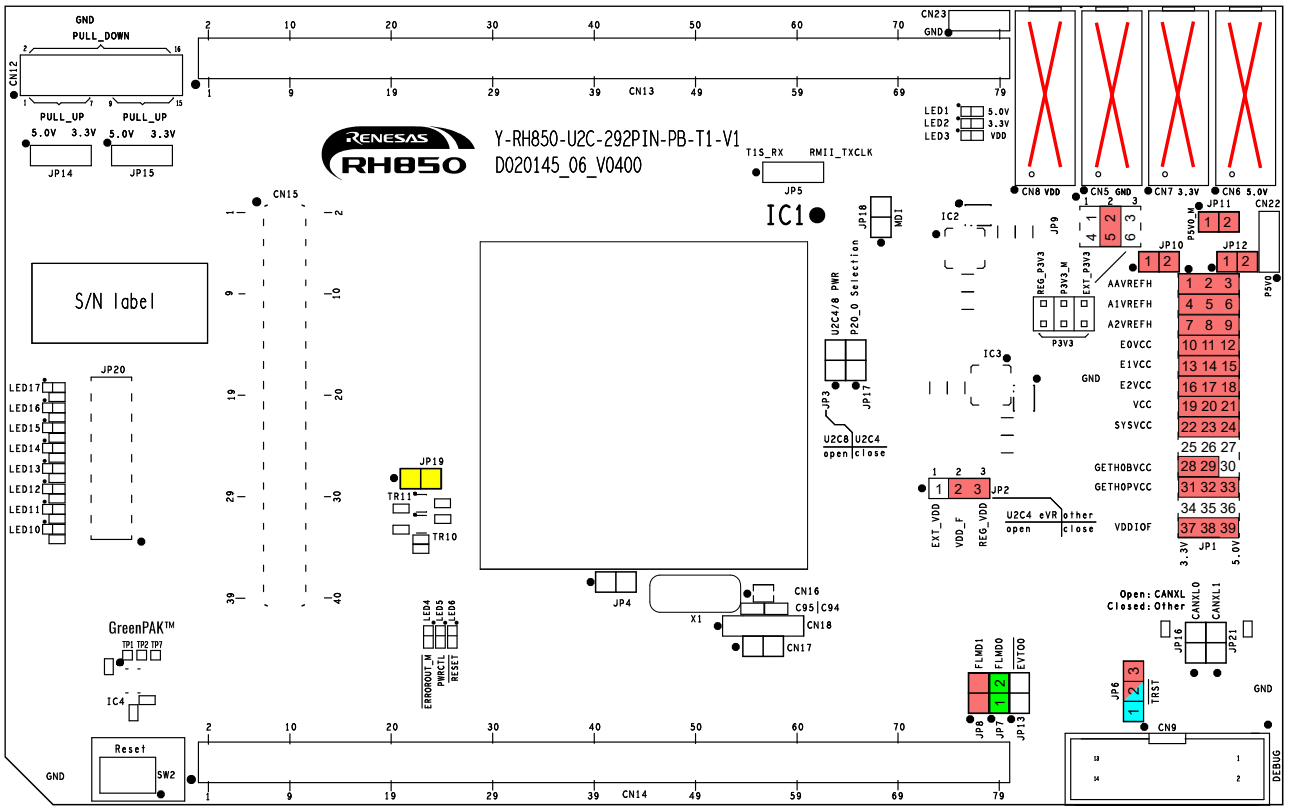


Figure 8.7 Main board operation without external power supply for DPS devices

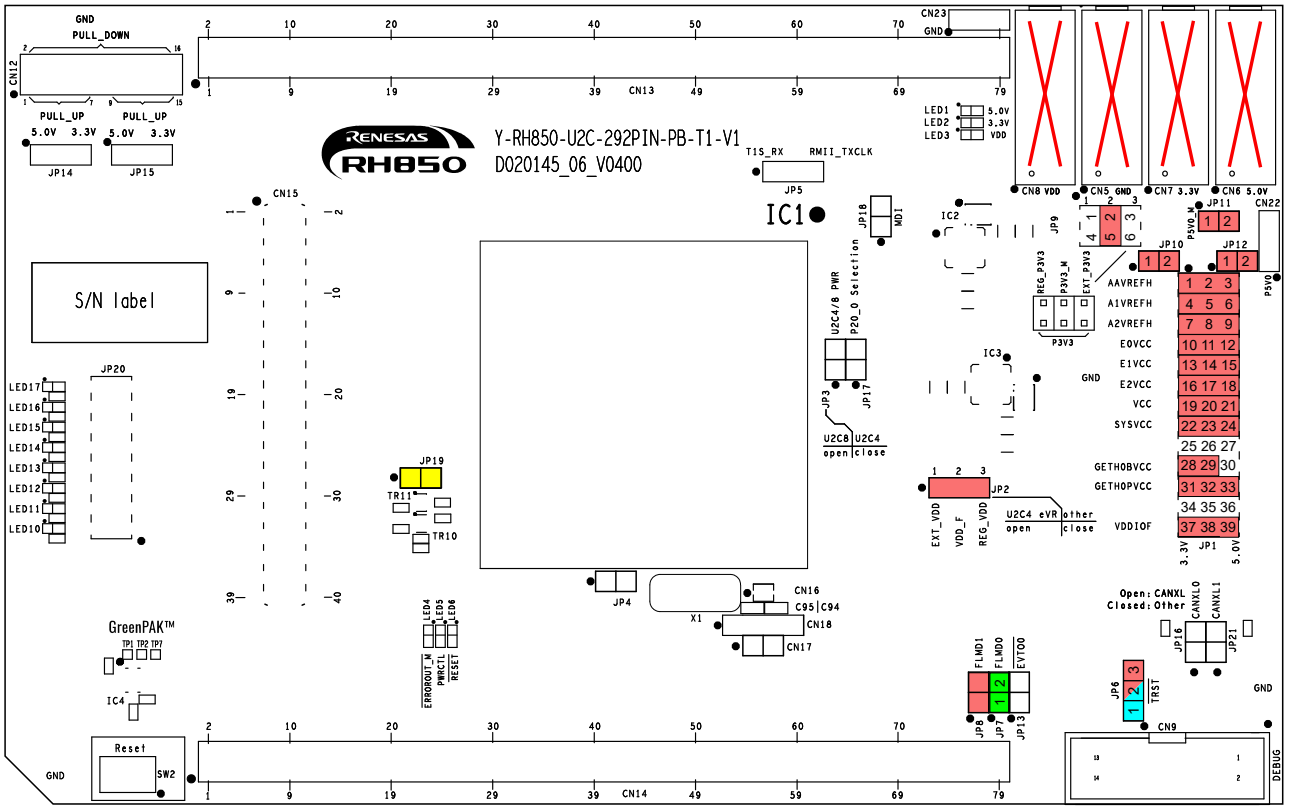


Figure 8.8 Main board operation without external power supply for eVR devices

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW2 into '5-6 ON' position, so that RESET is permanently asserted. Alternatively keep SW2 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW2 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 System State and RESET.*

10. Mechanical Dimensions

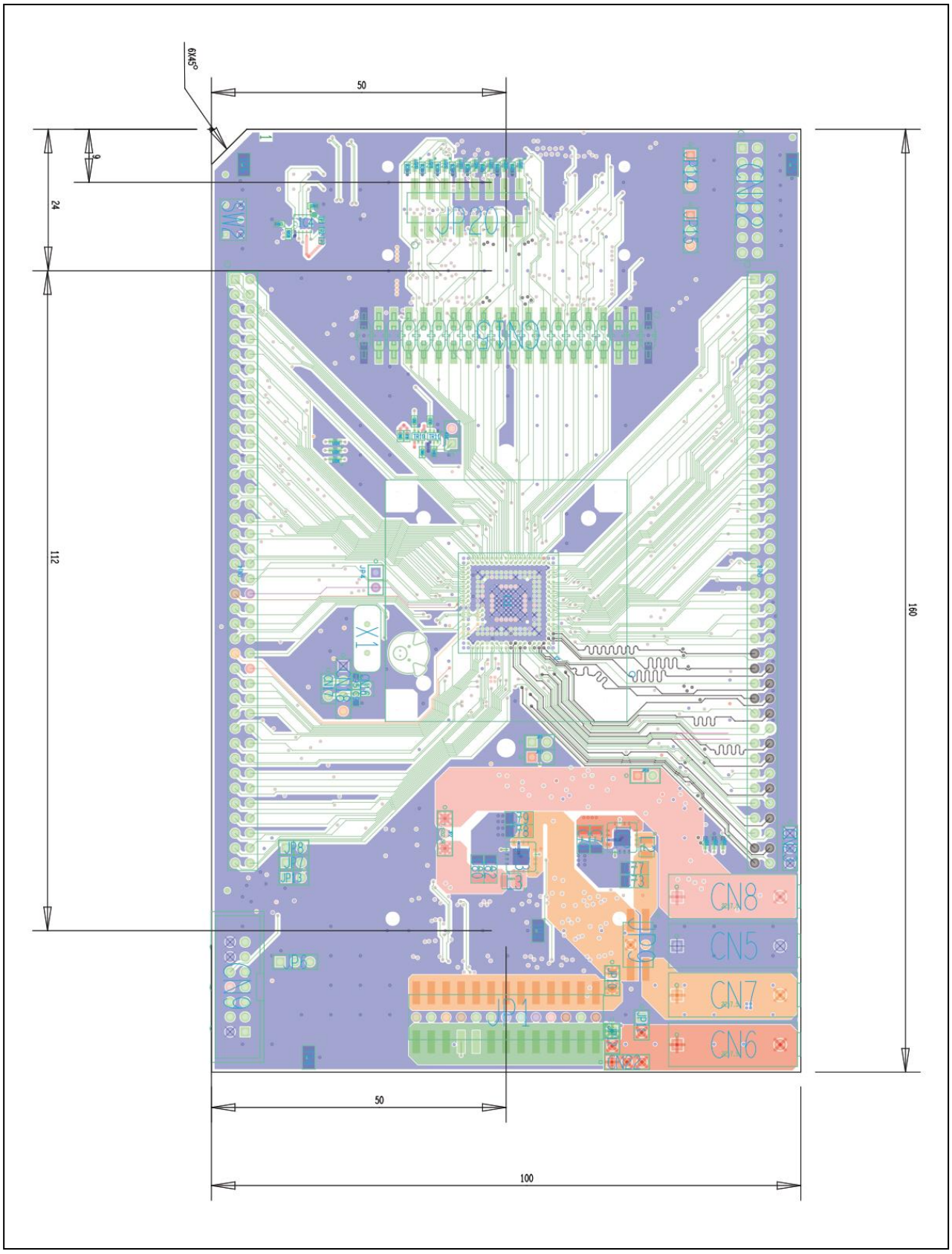


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C32, C37, C94, C95
- Resistor: R81 (board version D020145_06_V01 only)
- Connectors / sockets: CN16, CN19, CN20, CN21
- Oscillators: OSC1, X2

The above components are crossed out in the schematics.

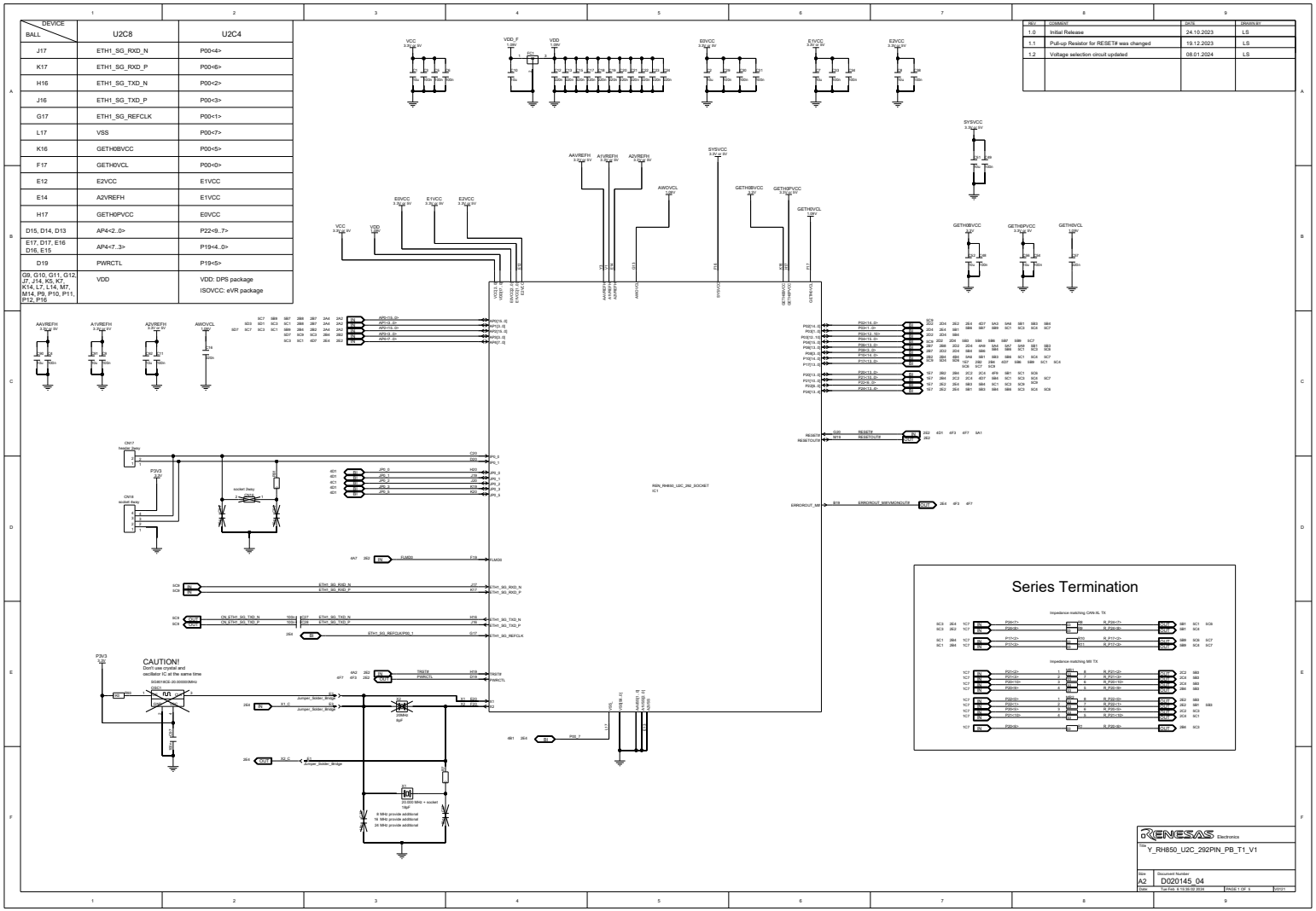
CN19, CN20 and CN21 have been removed in board version D020145_06_V02.1

The following components described in the schematics are provided with but not mounted on the board upon delivery:

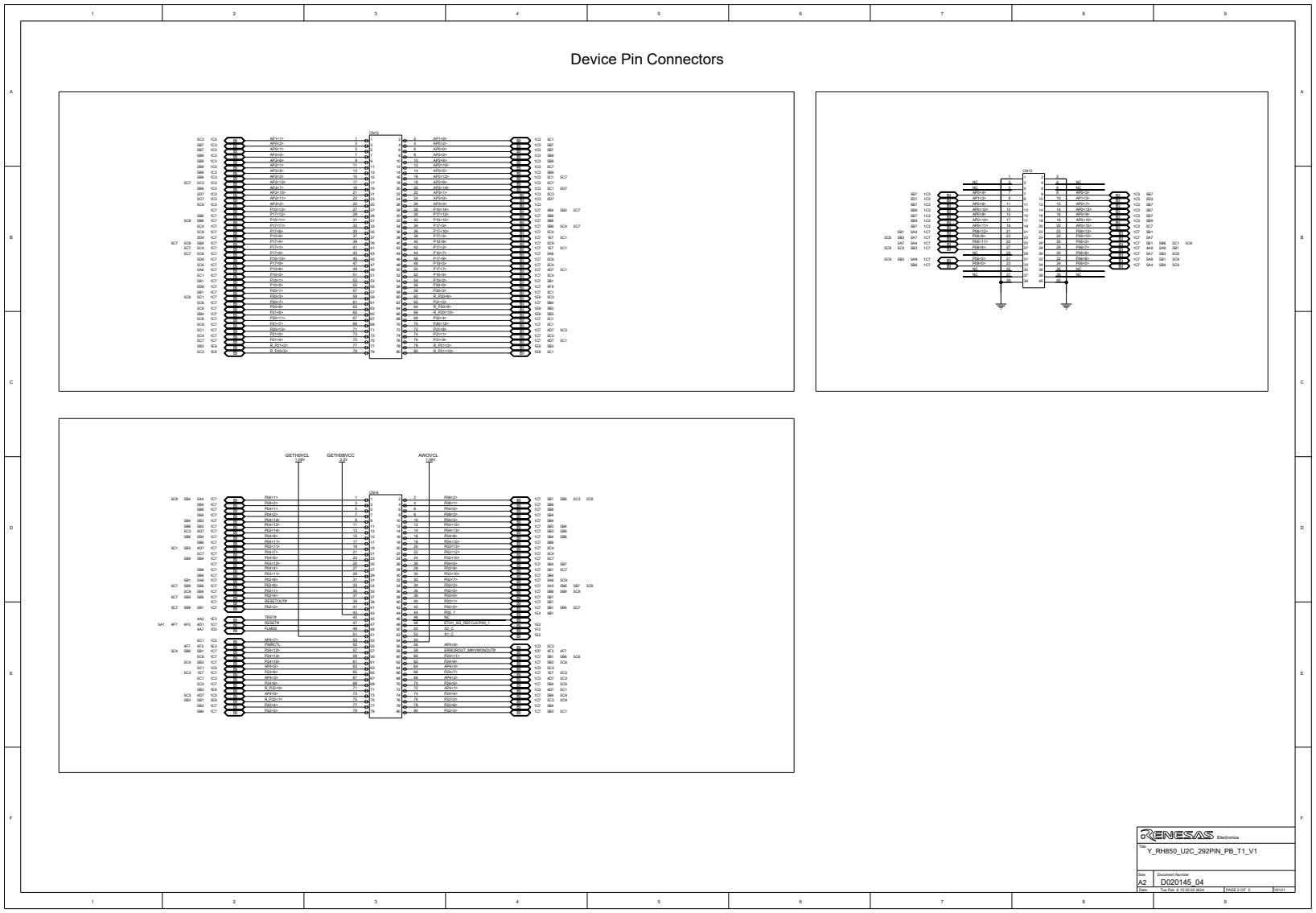
- 1 Hirschmann 4 mm power lab sockets, red for CN8
- Three resonators HC49 (8 / 16 / 24 MHz)
- 31 jumpers, 2.54 mm, black (board version D020145_06_V01)
- 34 jumpers, 2.54 mm, black (board version D020145_06_V02.1)
- 37 jumpers, 2.54 mm, black (board version D020145_06_V03)
- 39 jumpers, 2.54 mm, black (board version D020145_06_V0400)

11.1 Board Version D020145_06_V01

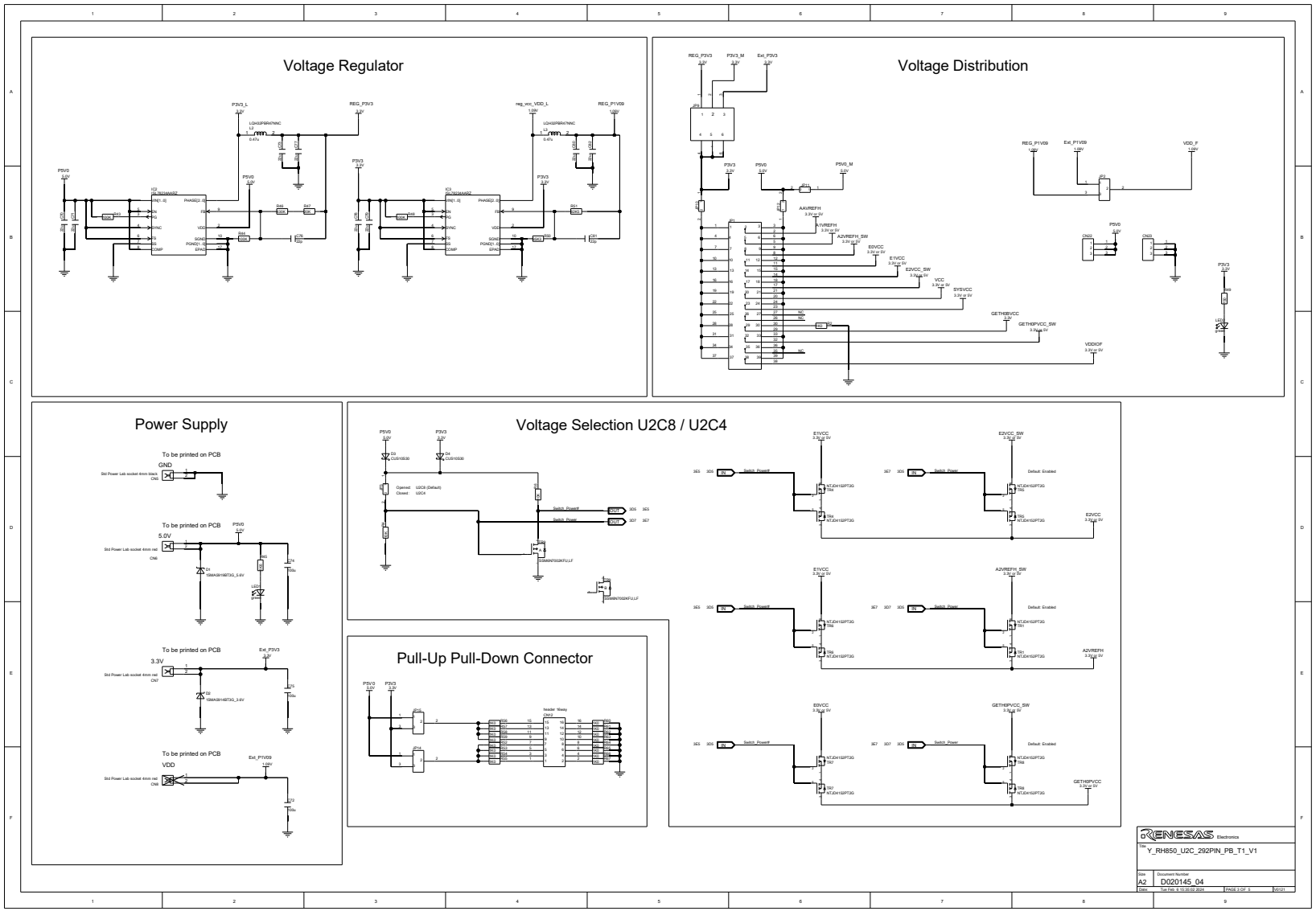
11.1.1 RH850/U2C



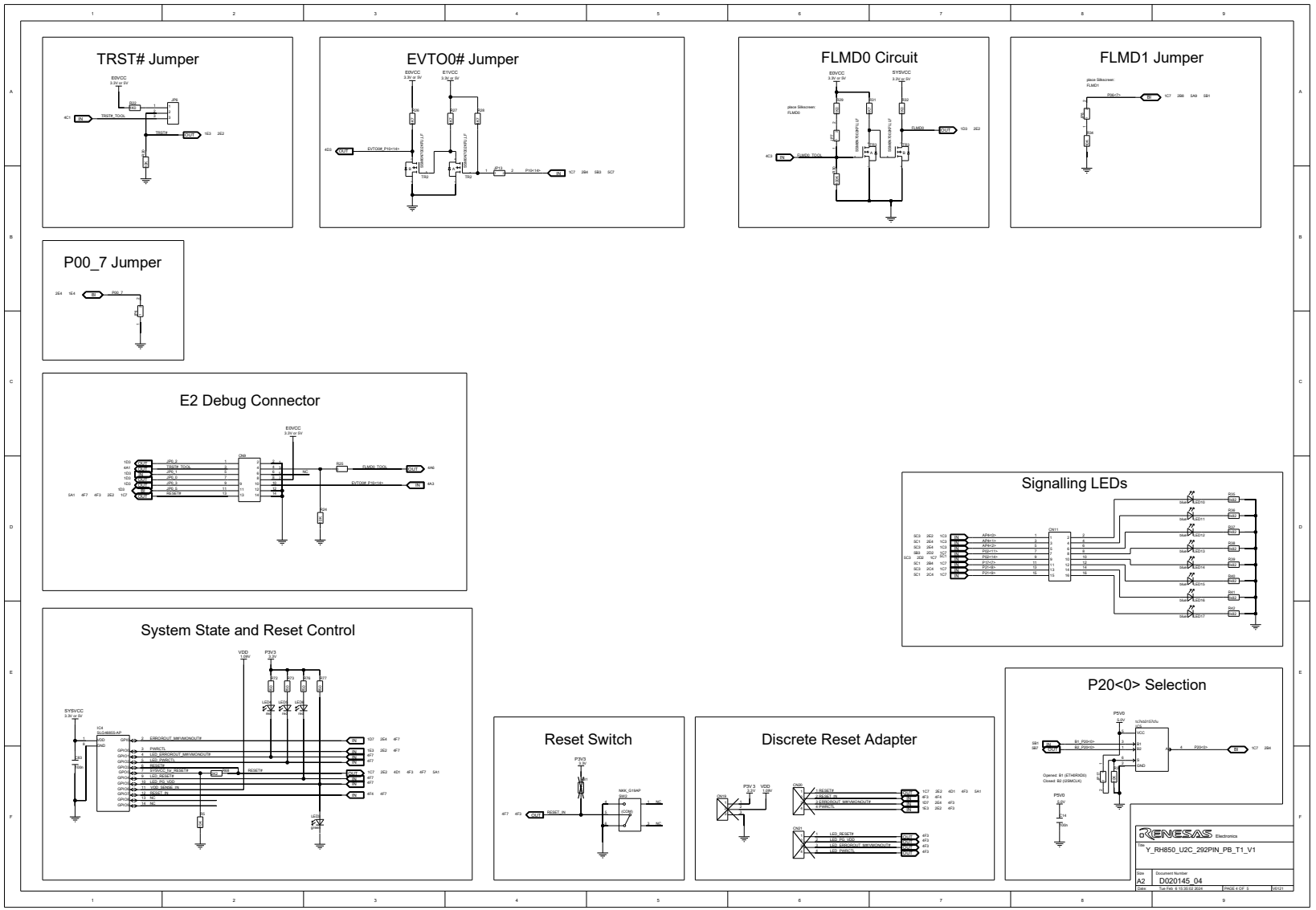
11.1.2 Breakout Connectors



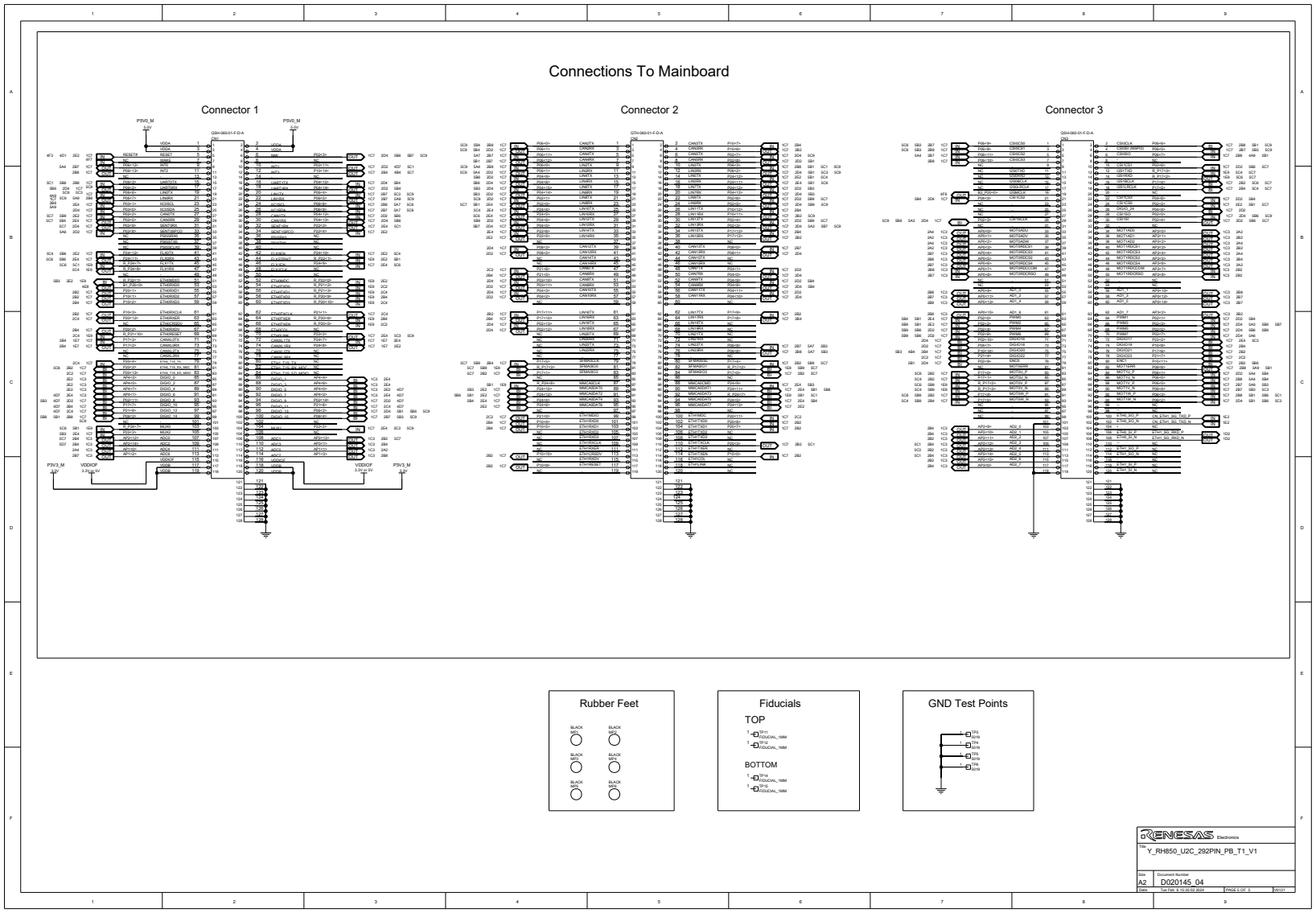
11.1.3 Power Supply



11.1.4 RH850 Configuration

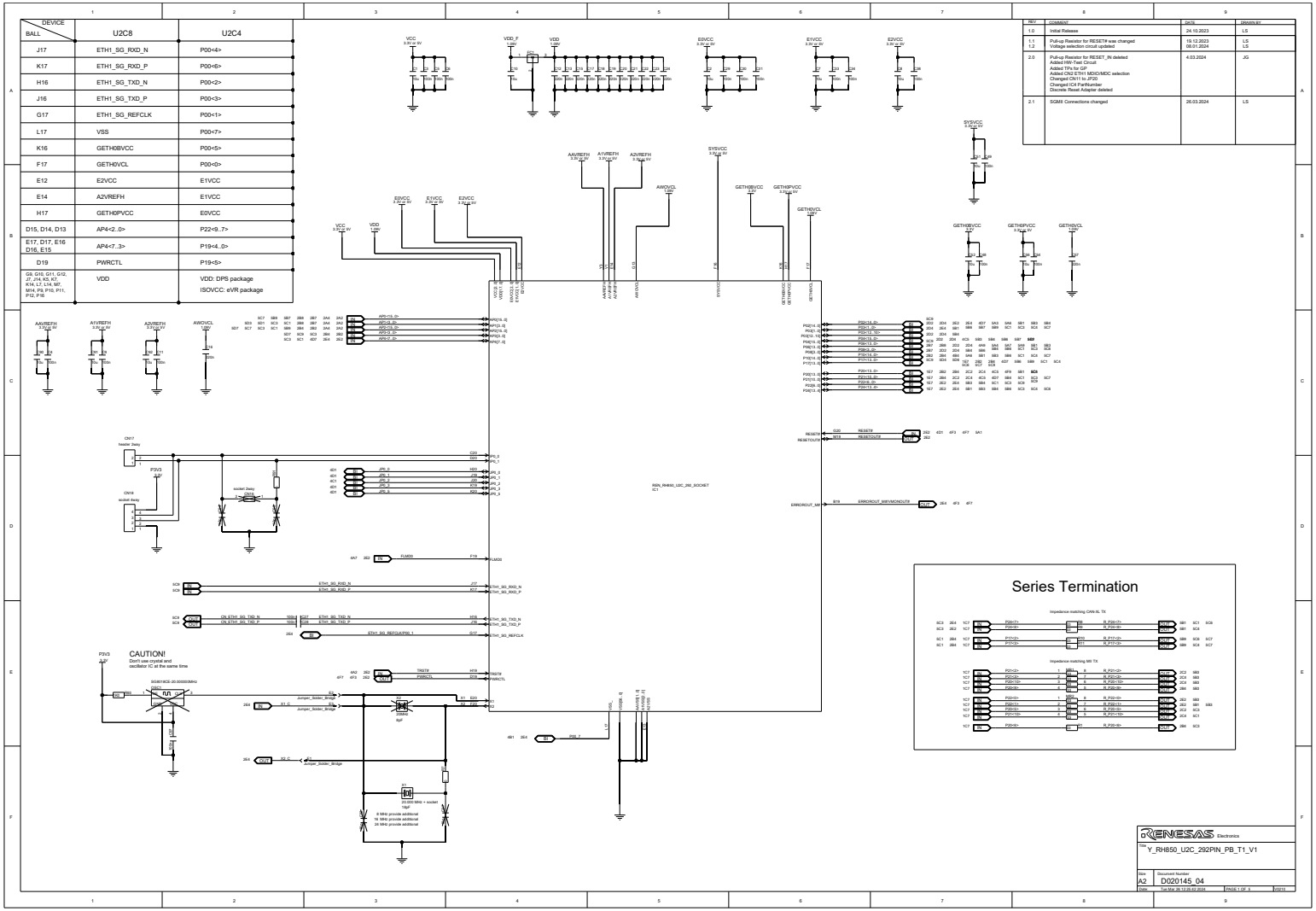


11.1.5 Main Board Connectors

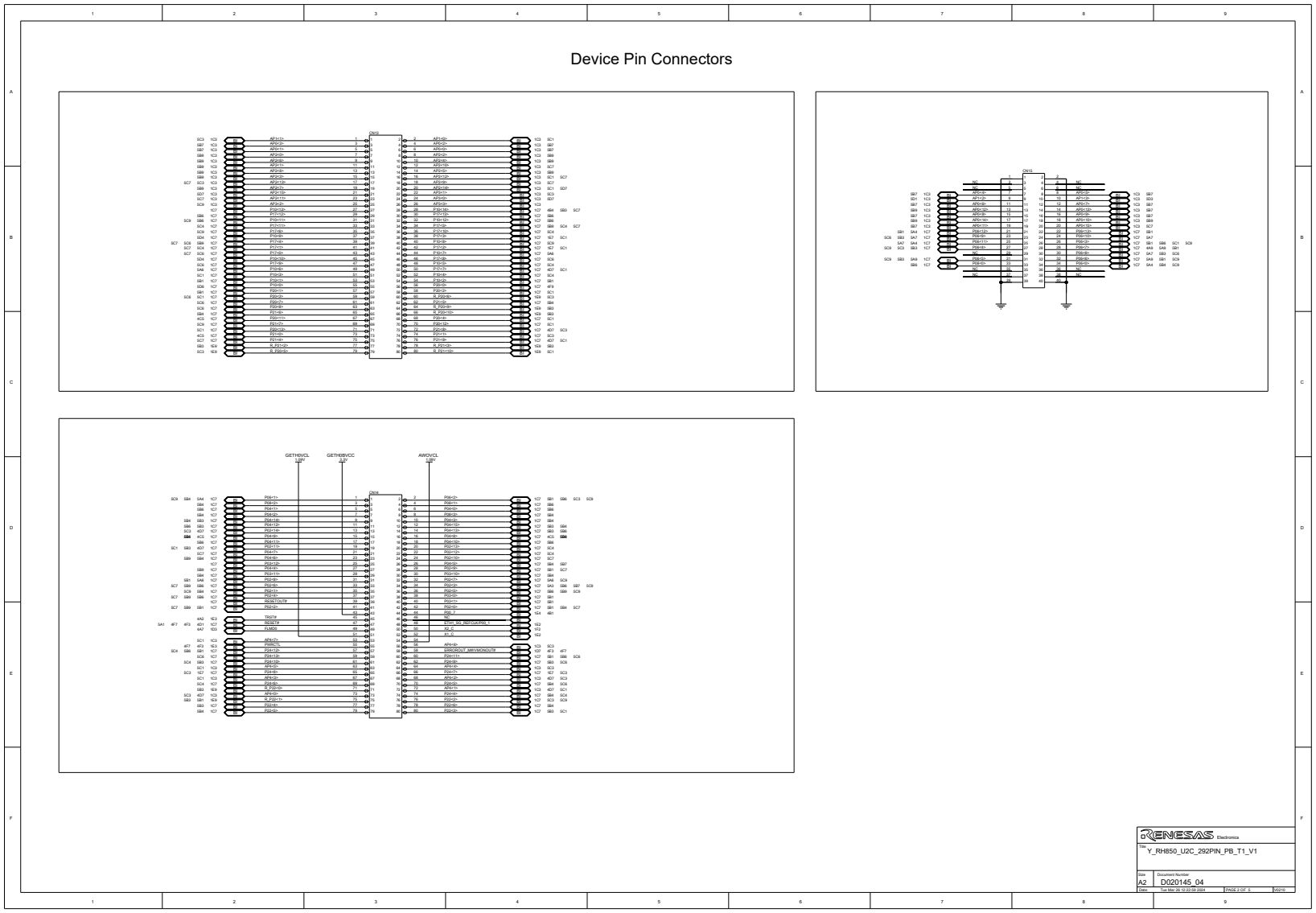


11.2 Board Version D020145_06_V02.1

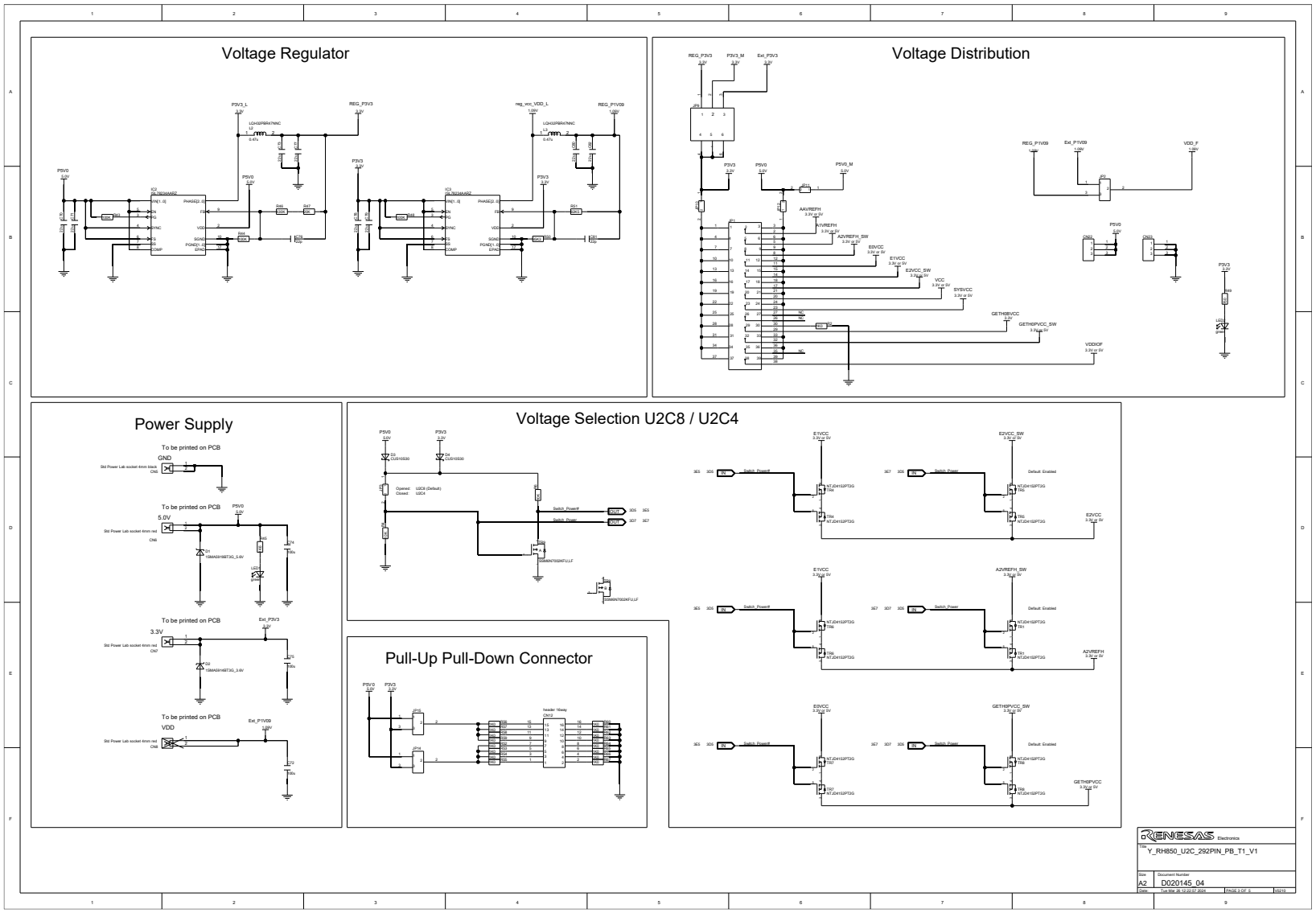
11.2.1 RH850/U2C



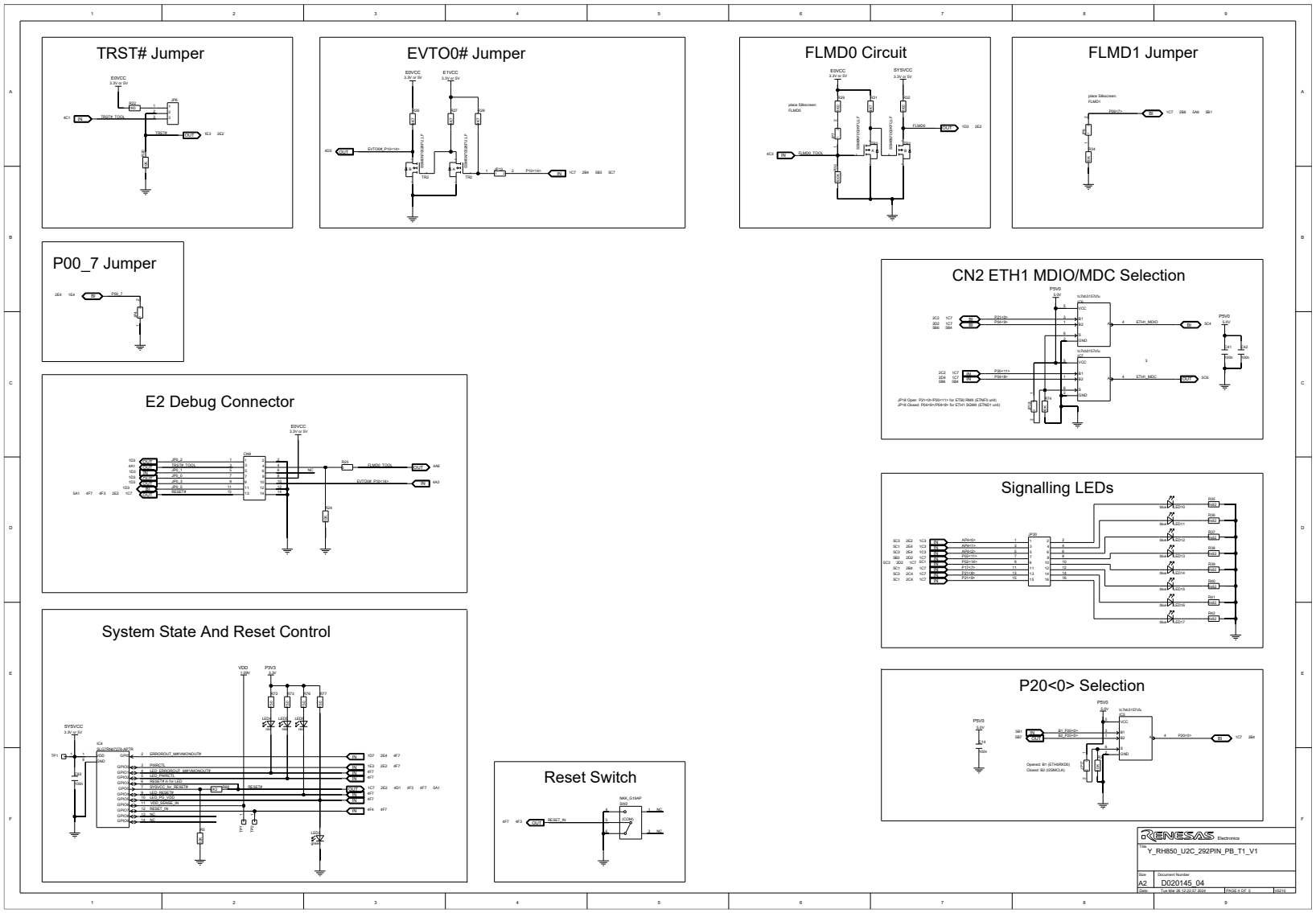
11.2.2 Breakout Connectors



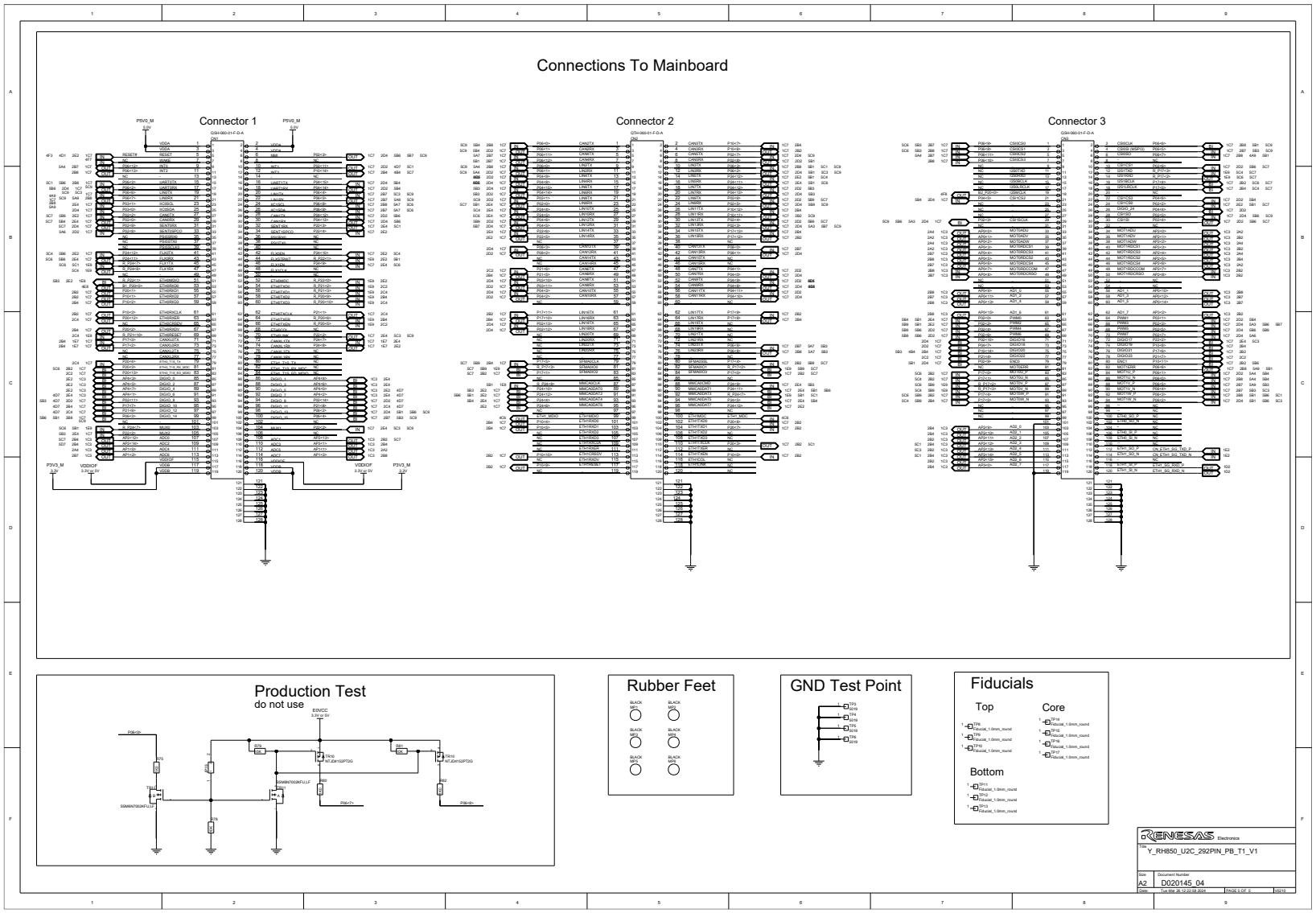
11.2.3 Power Supply



11.2.4 RH850 Configuration

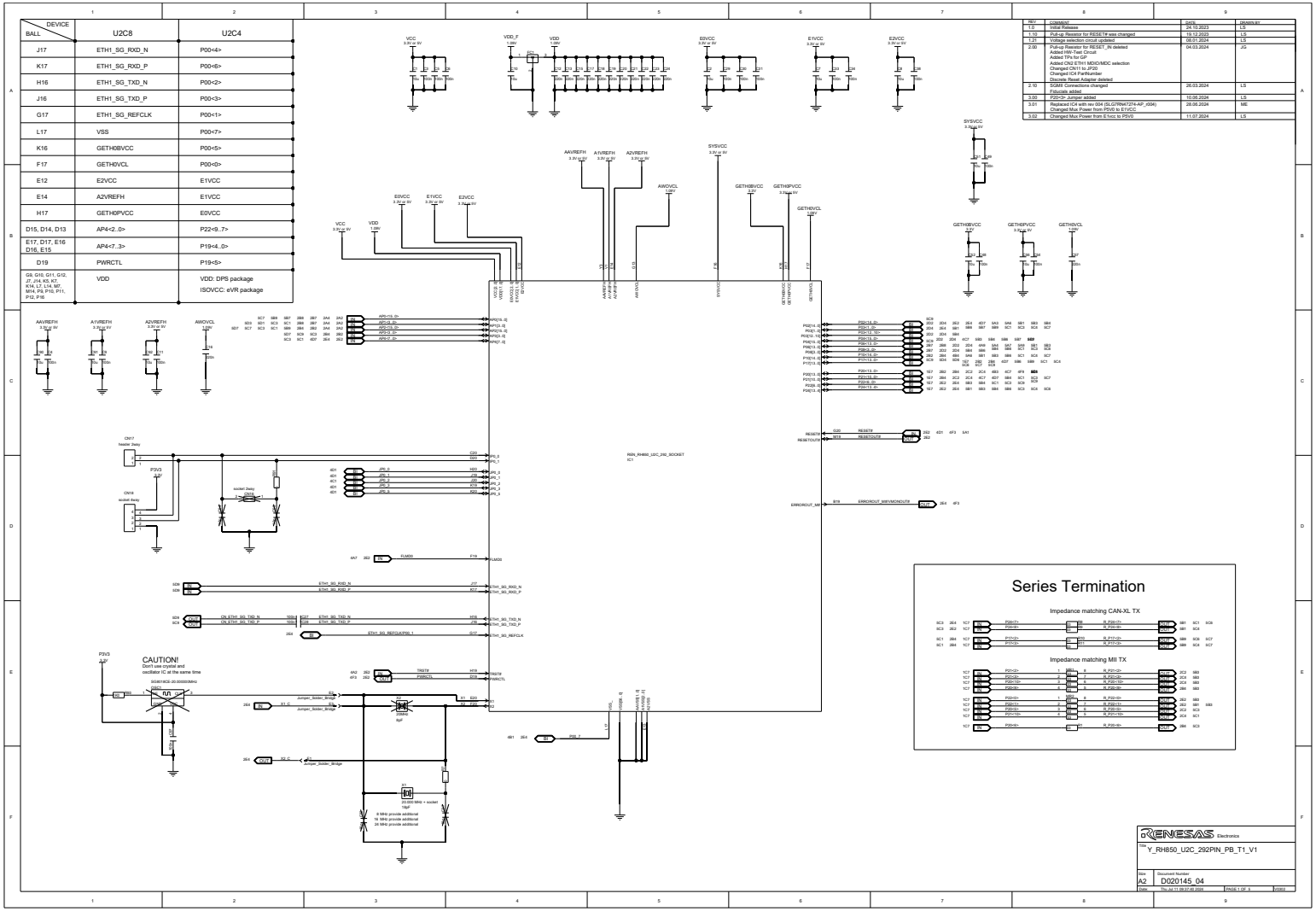


11.2.5 Main Board Connectors

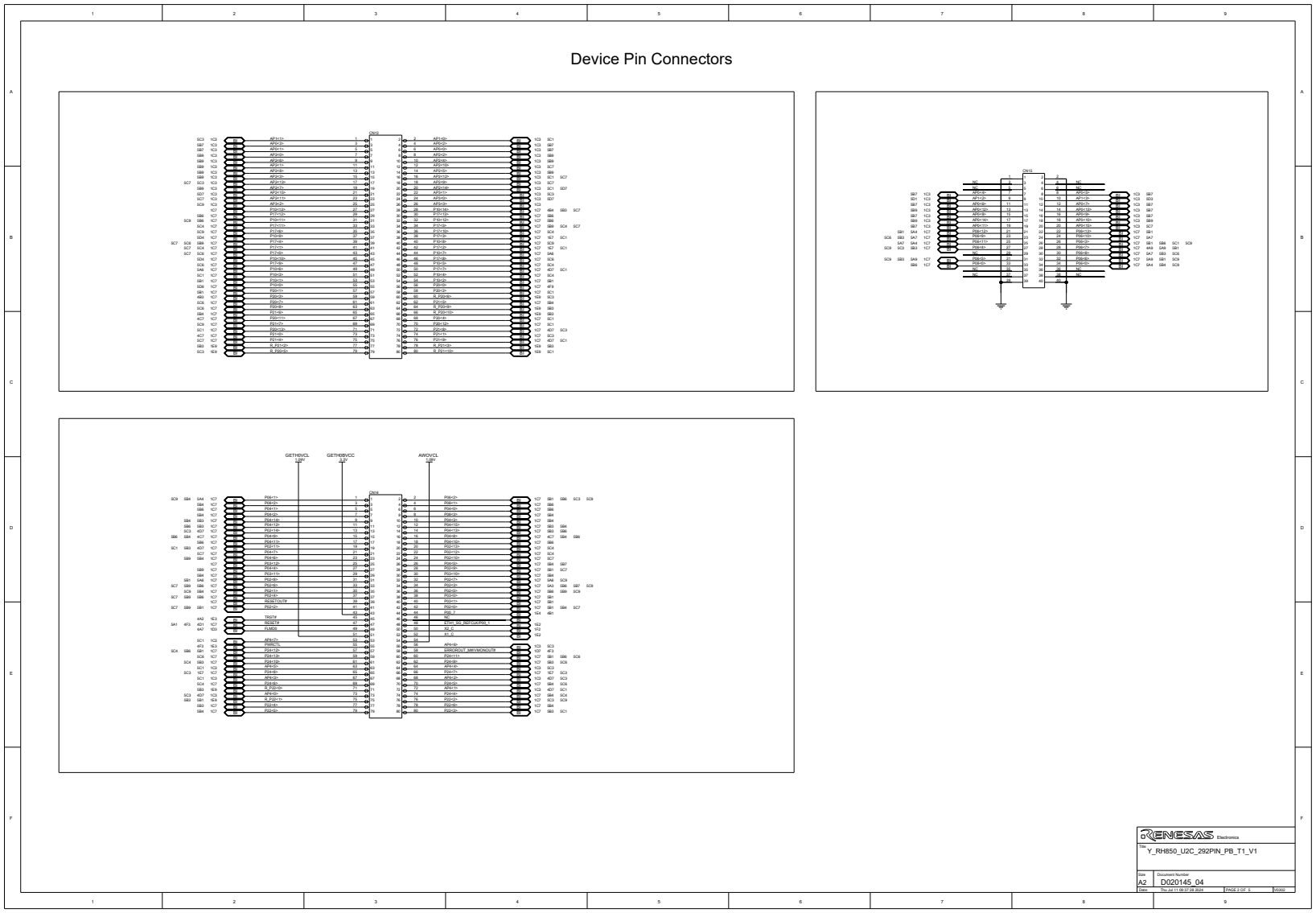


11.3 Board Version D020145_06_V03

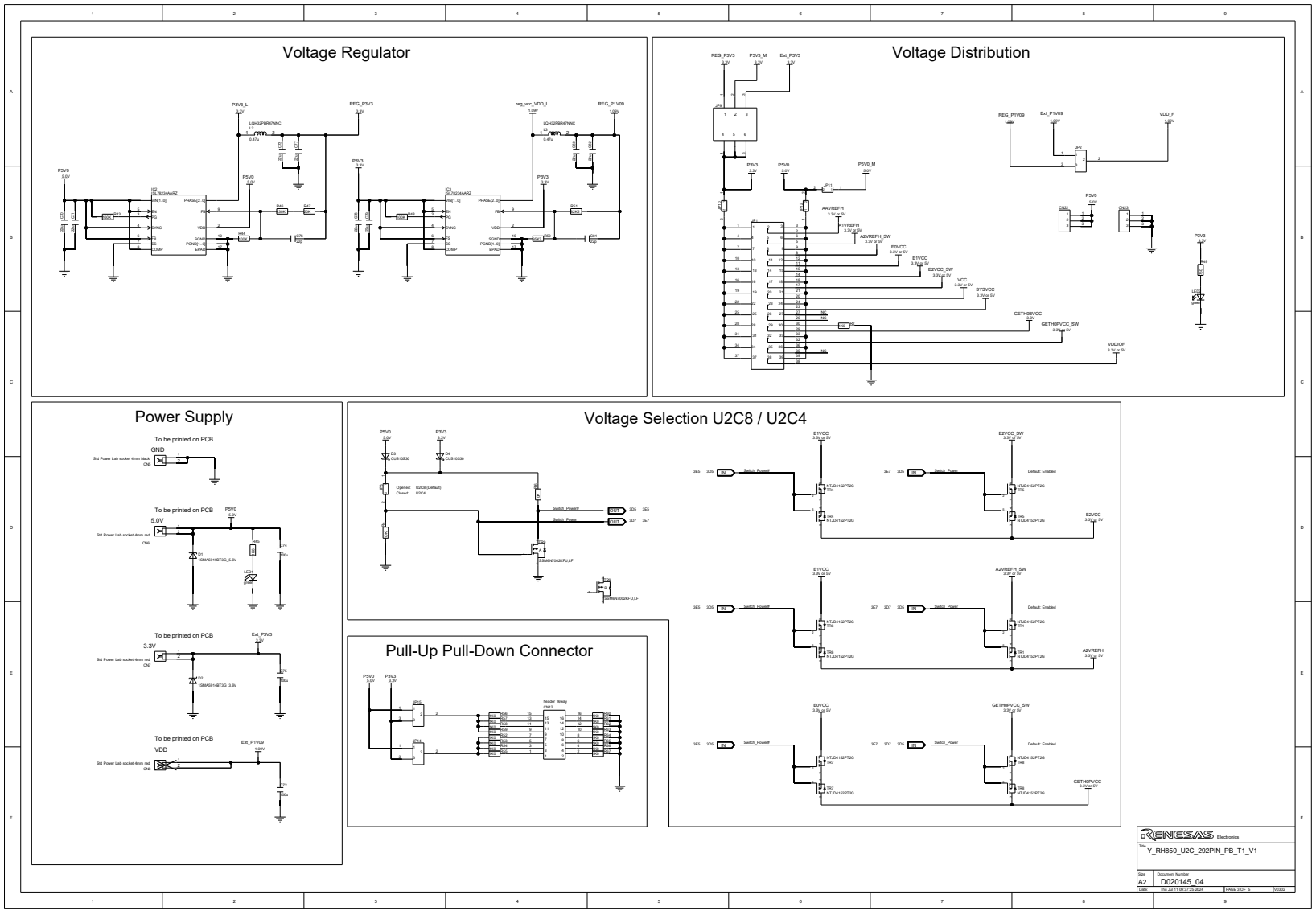
11.3.1 RH850/U2C



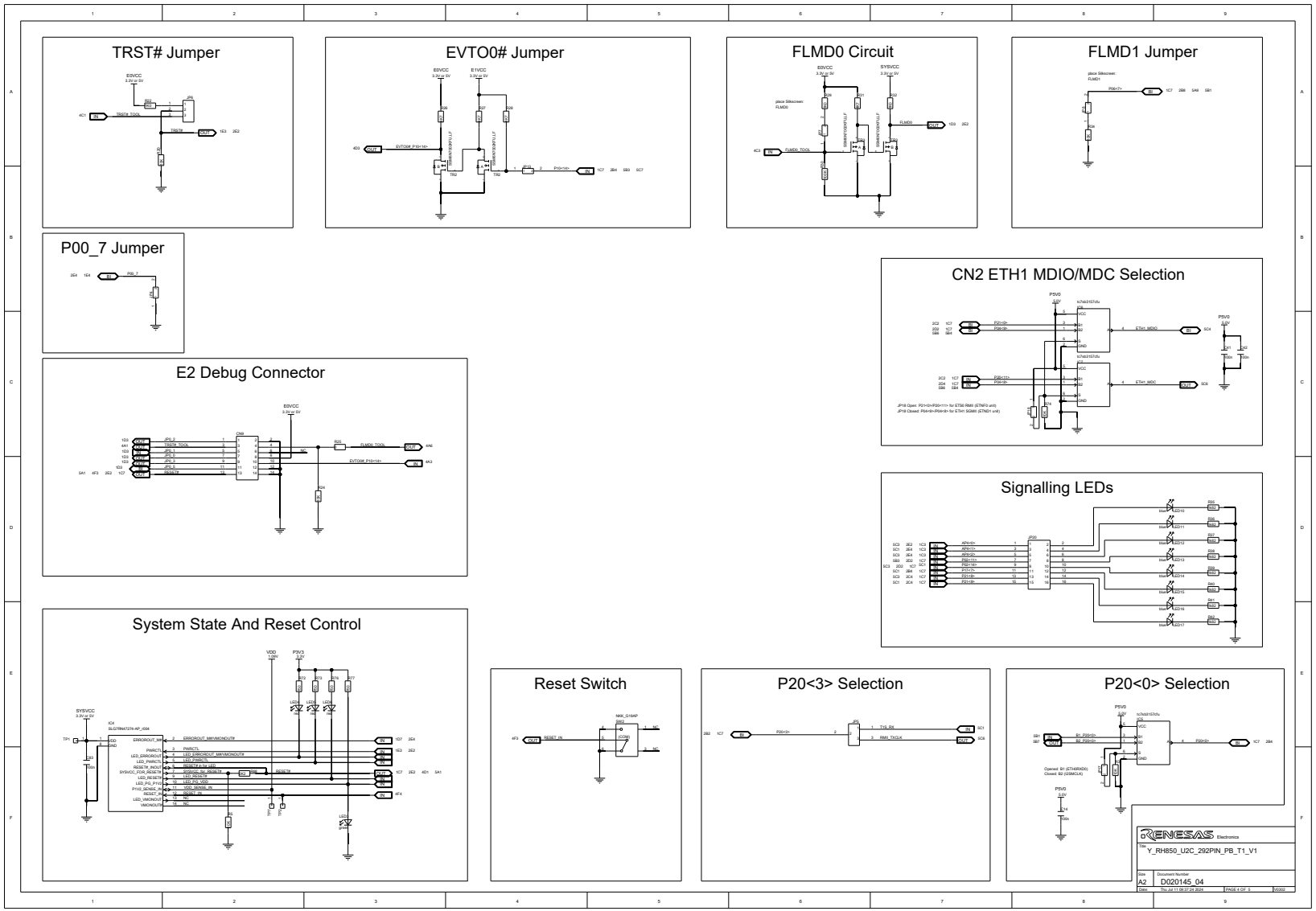
11.3.2 Breakout Connectors



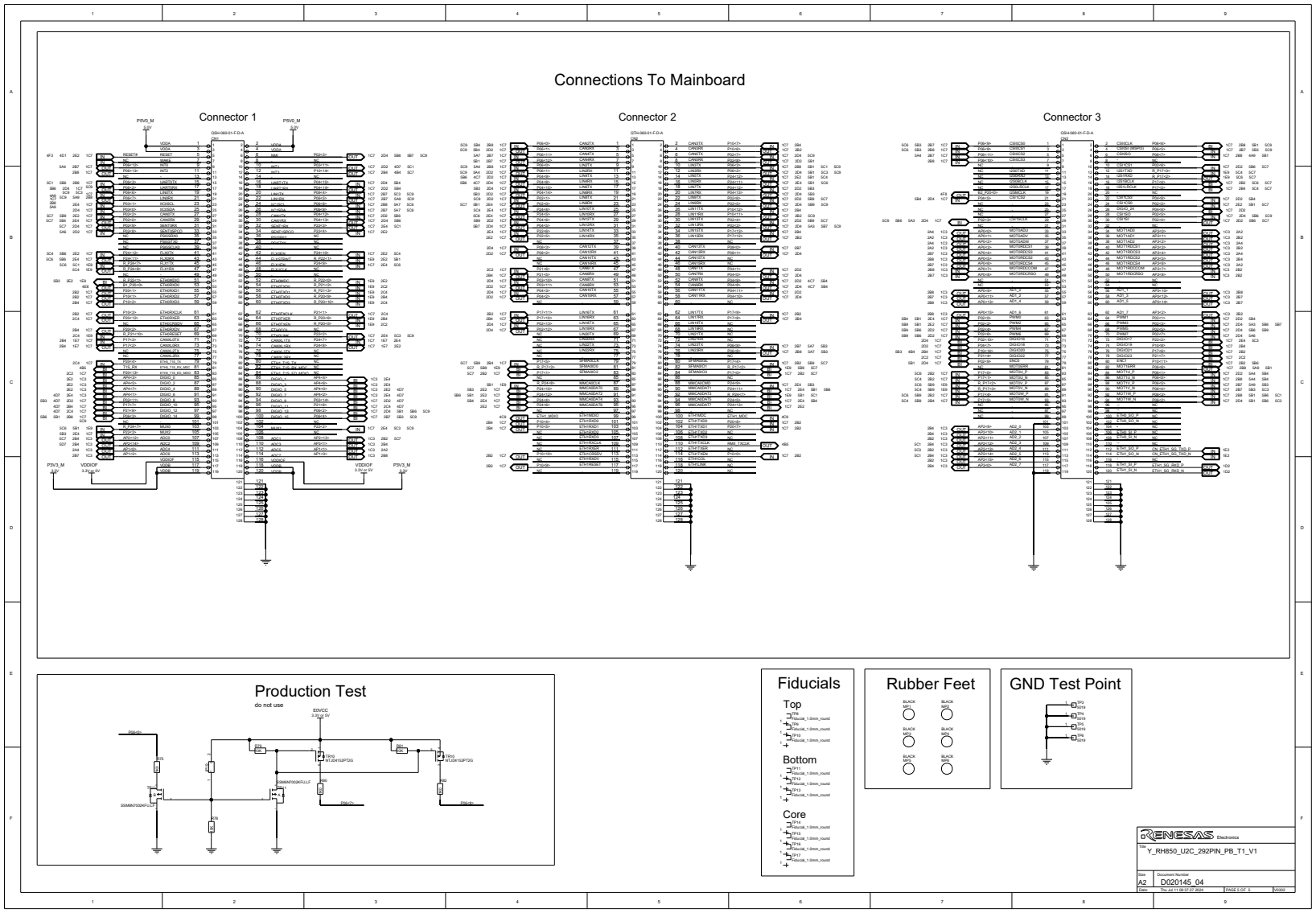
11.3.3 Power Supply



11.3.4 RH850 Configuration

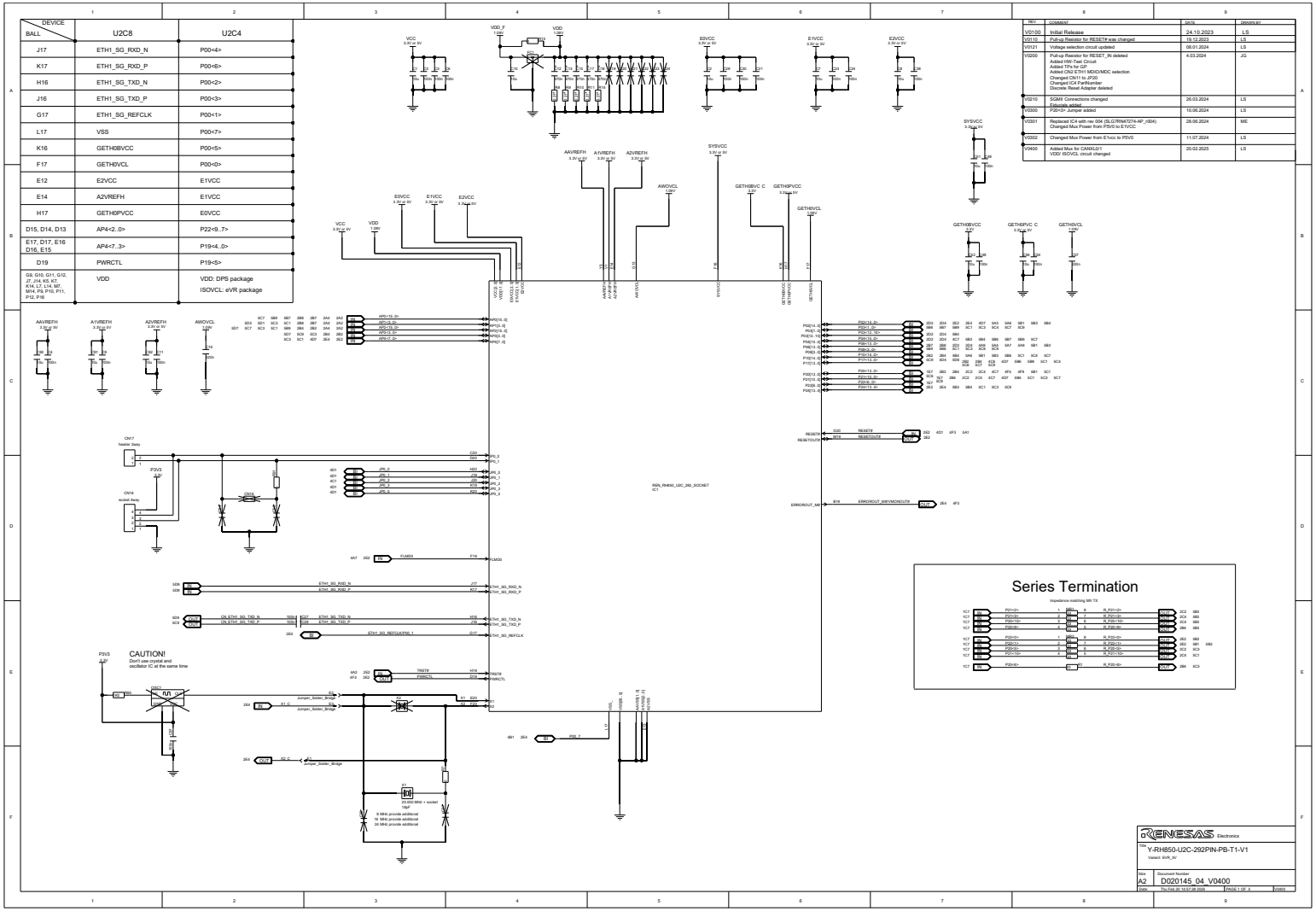


11.3.5 Main Board Connectors

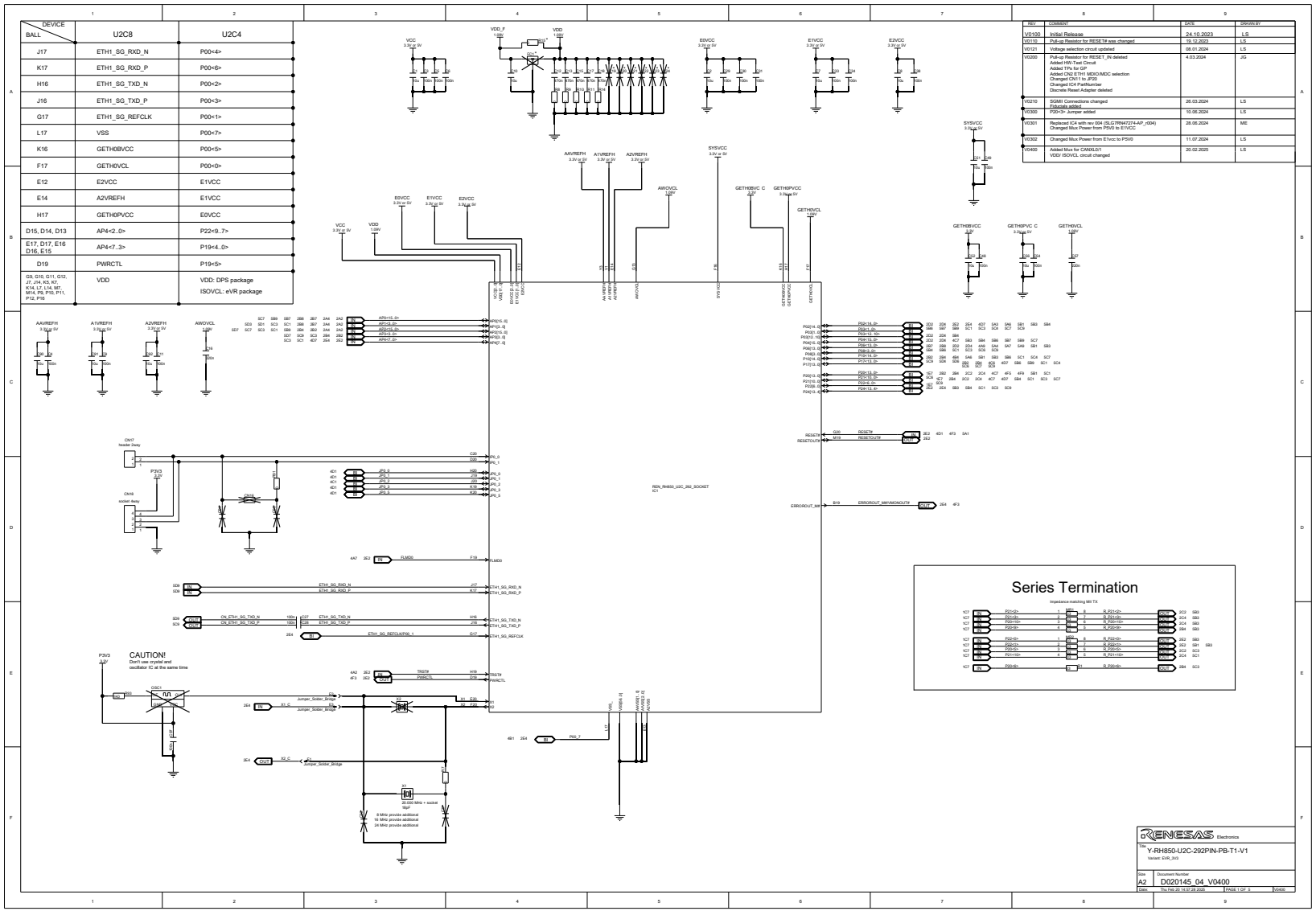


11.4 Board Version D020145_06_V0400

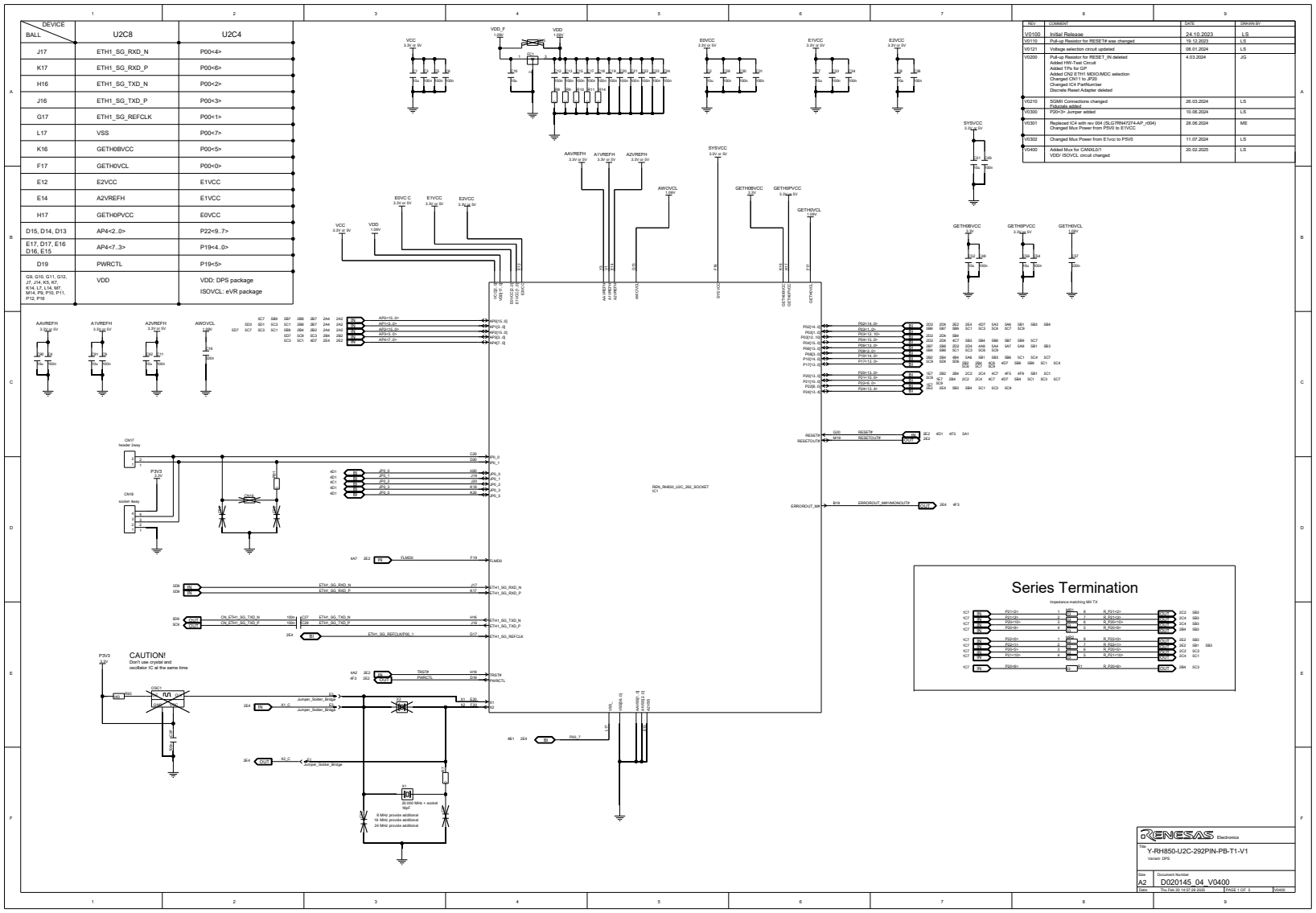
11.4.1 RH850/U2C, eVR 5.0V Circuit



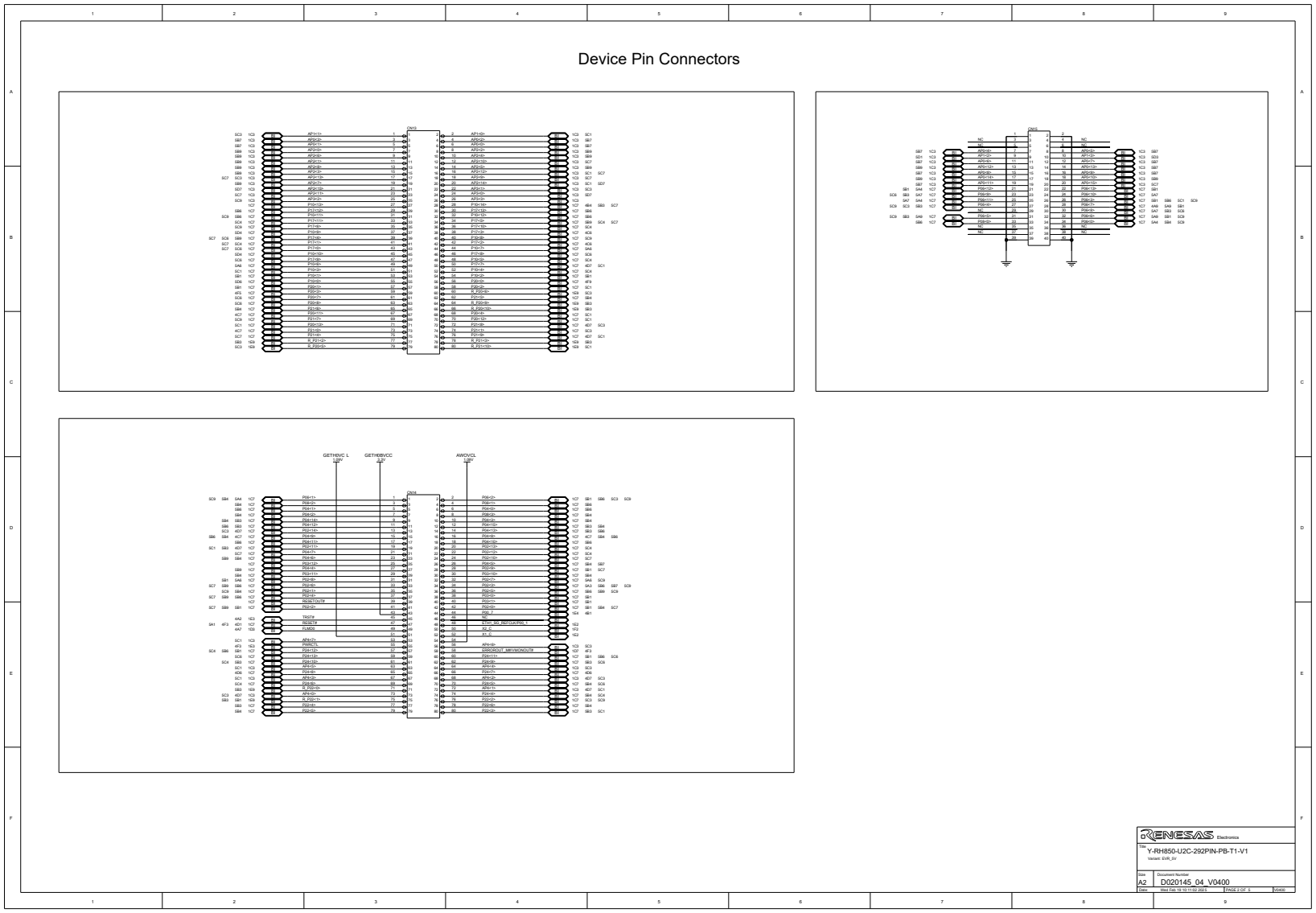
11.4.2 RH850/U2C, eVR 3.3V Circuit



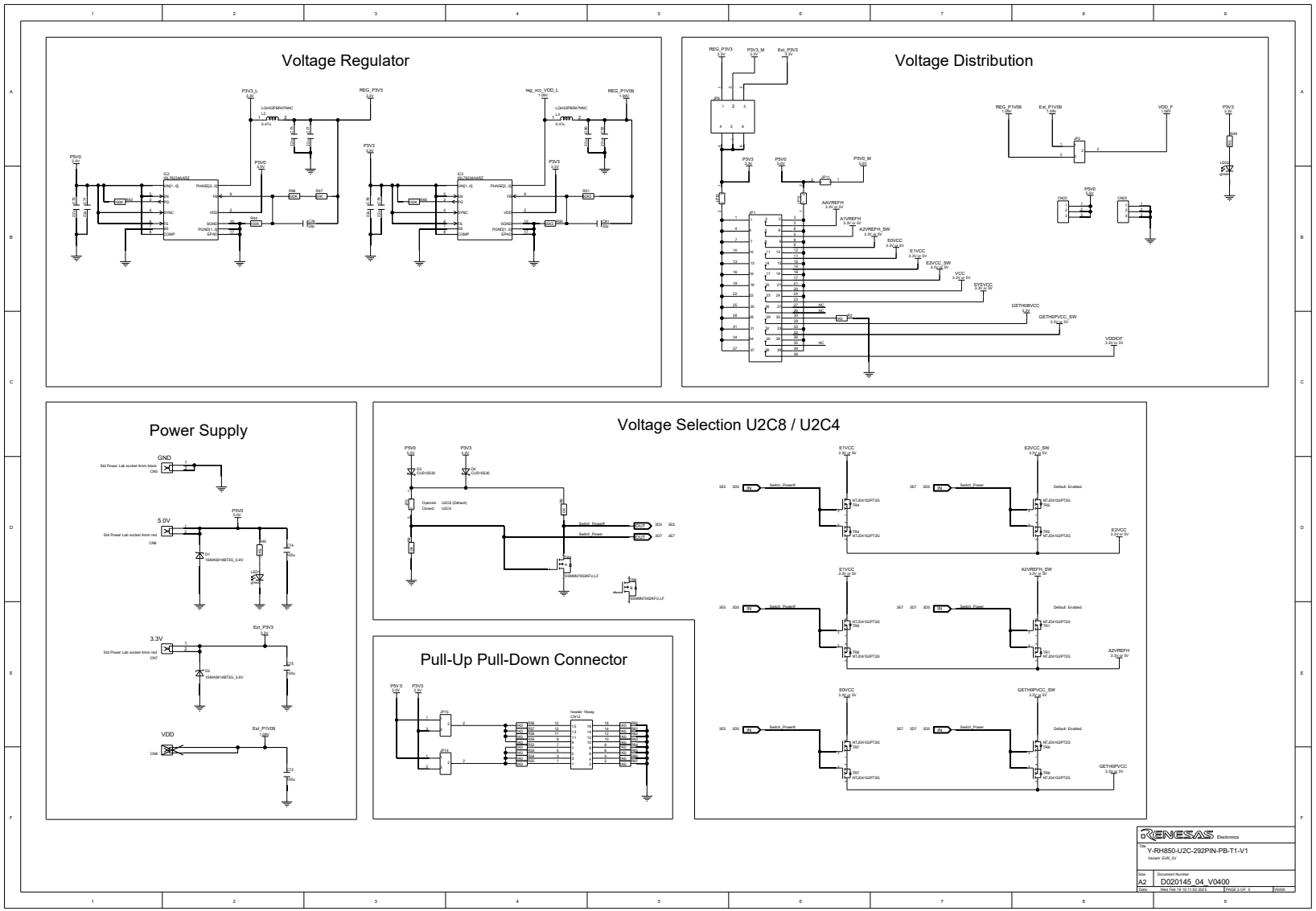
11.4.3 RH850/U2C, DPS Circuit



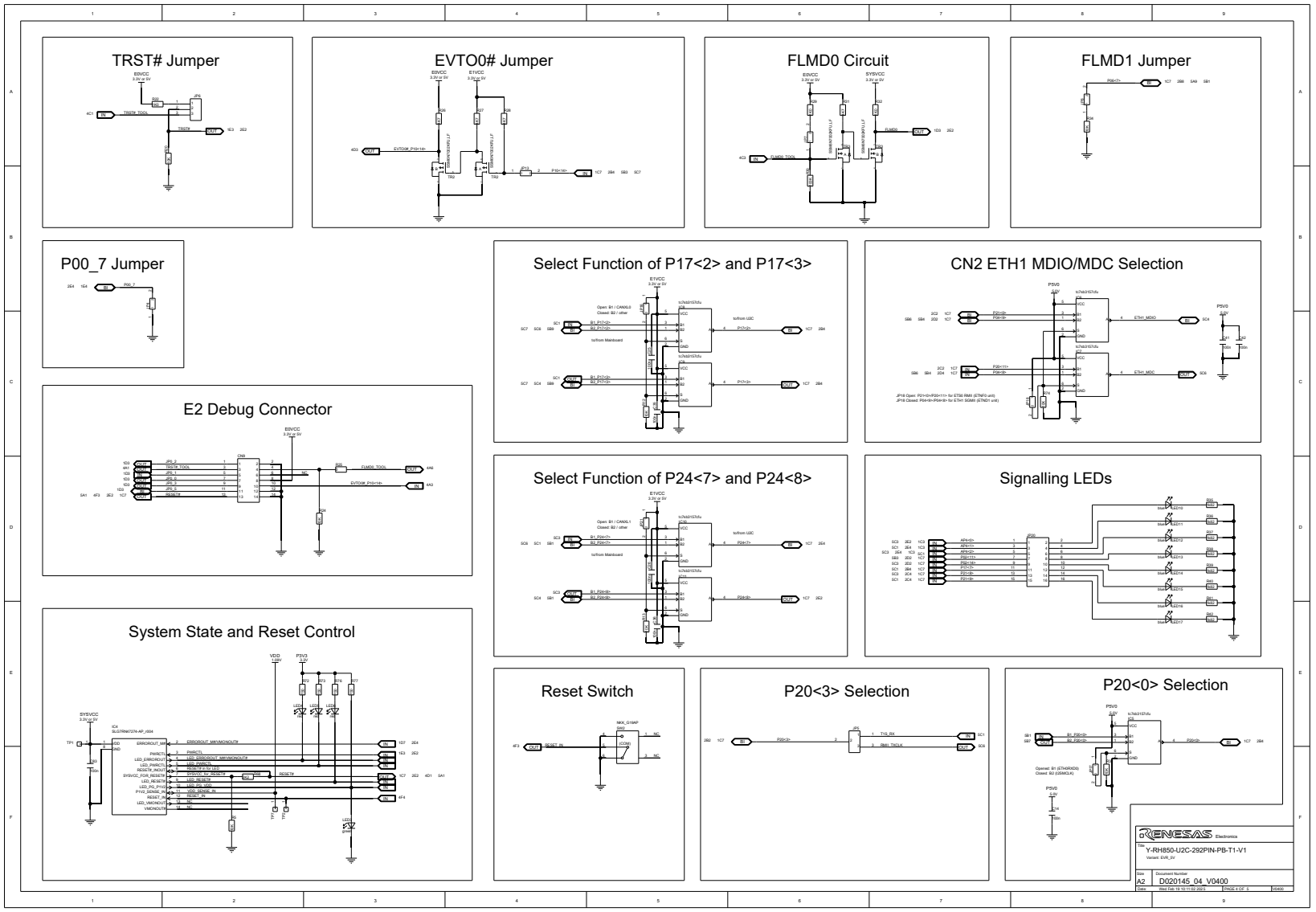
11.4.4 Breakout Connectors



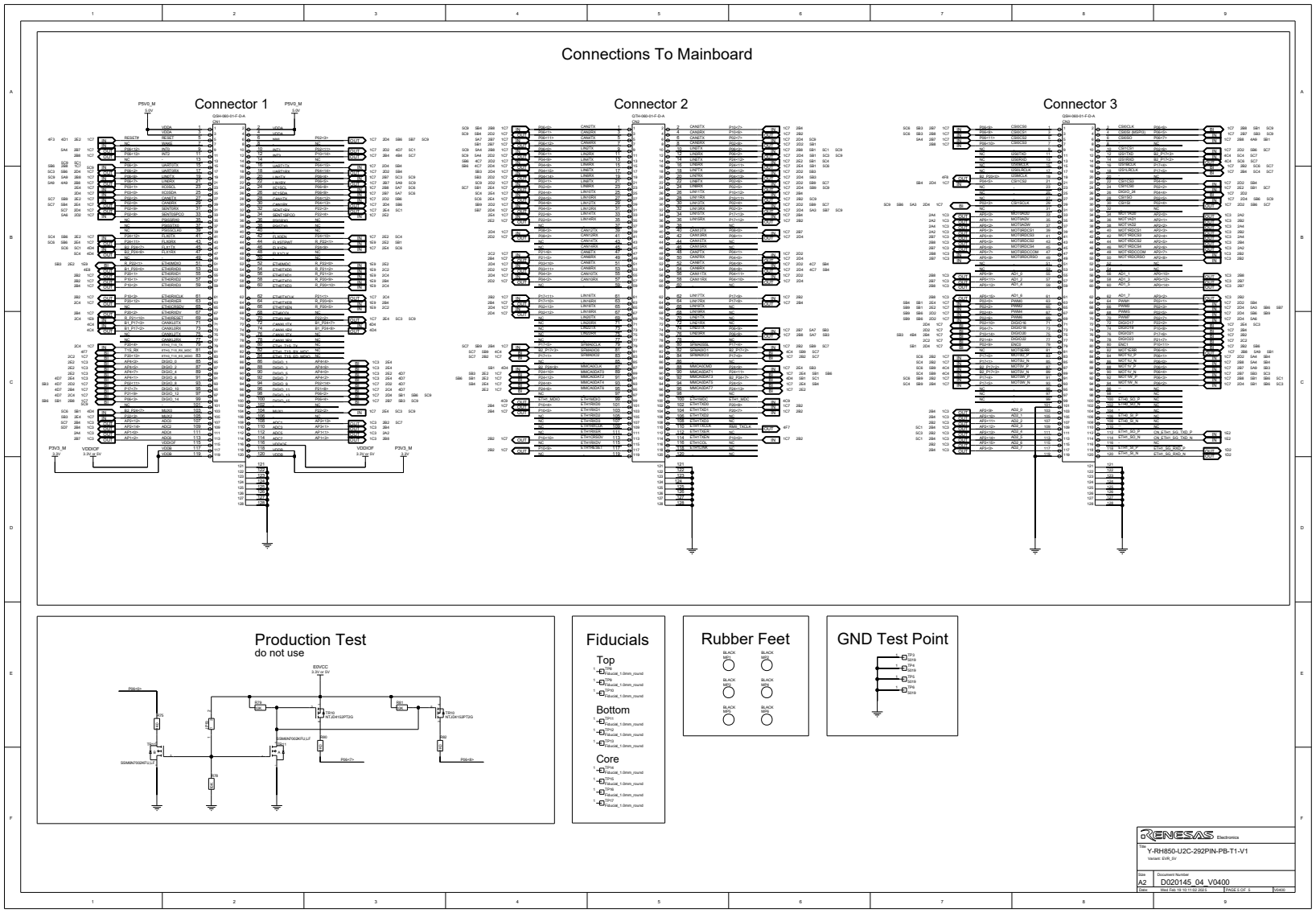
11.4.5 Power Supply



11.4.6 RH850 Configuration



11.4.7 Main Board Connectors



Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2024-03-01	–	Initial release
V2.00	2024-04-05	–	Added information about board revision D020145_06_V02.1
		38, *59*	Added explanation for FLMD1 setting in Serial Programming Mode in *6.1 Operation Mode Selection* and *8.2 Configuration Examples*
V2.01	2024-05-08	*9*	Updated information on differences between board revisions *in Table 1.3 Differences between board versions V01, V02.1, V03 and* V0
V2.02	2024-05-15	*30*	Added caution about setting of jumper JP2 in chapter *3.3 Device Core Voltage Selection.*
V3.00	2024-11-06	*19*	Updated device list in *Table 1.4 Type names for suitable devices.*
		39	Updated GreenPAK IC (IC4) to version V0400 in chapter *6.2 System State and RESET.*
		43	Added jumper JP21 for port P20_3 Ethernet function selection in chapter *6.6 Ethernet Control Port P20_3*.
		43, 80	Corrected comment about Ethernet units being used with different JP18 jumper settings on board revision D020145_06_V02 in chapter *6.5 Ethernet 1 Control Ports MDIO / MDC* and chapter *11.2.4 RH850 Configuration.*
		59	Updated pictures for jumper configuration examples in chapter *8 Jumper Configuration Examples*.
V4.00	2025-06-02	*19*	Added multiplexer for CAN-XL ports.
		30	Modified circuit for core voltage supply to RH850/U2C in chapter *3.3 Device Core Voltage Selection.*
V4.01	2026-04-22		Corrected some typos and updated the document style.

RH850/U2C 292pin Piggyback Board V1 User's Manual: Piggyback Board

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