User's Manual

32

RH850 Evaluation Platform

RH850/U2C 144pin

User's Manual: Piggyback Board

Y-RH850-U2C-144PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2C 144pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2C 144pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document active low signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g. the reset pin is named RESETZ or RESET#.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2C-144PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2C-144PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2C-144PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2C-144PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2C-144PIN-PB-T1-V1

Item	Description	Quantity
D020562	RH850/U2C 144pin piggyback board	1
D020566	Documentation CD	1
D010818-24	WEEE+CE document	1
D020562-24	Product contents List	1
Jumpers (2-way, 0.1")	In the bag	29
Red Hirschmann 4 mm power lab socket	In the bag	1
Resonator, HC49, 8 / 16 / 24 MHz	In the bag	3

Note

Please keep the Y-RH850-U2C-144PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2C-144PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with power supply from main board
  - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.09 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - Support JTAG/LPD debug interface
  - 14-pin connector for E2 emulator
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 8/16/20/24 MHz Crystal Resonator
- Eight general purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the Piggyback Board are available:

Table 1.2 Y-RH850-U2C-144PIN-PB-T1-V1 board versions

Board version	Schematic version
D020562_06_V0100	D020562_04_V0100
D020562_06_V0200	D020562_04_V0200

The table shows the differences of the board versions:

Table 1.3 Y-RH850-U2B-144PIN-PB-T1-V1 board version differences

No.	Modified Function	Detailed Description of Changes	D020562_06_V0100	D020562_06_V0200
1	Port connected to main board connector CN2 pin 33	Changed port that is connected to pin 33 on connector CN2.	CN2_33 connected to port P24_9.	CN2_33 connected to port P24_7.
2	Connection of the CAN XL signals from RH850/U2C to the main board connectors.	Direct connection of CAN XL ports on RH850/U2C to function ports on main board connectors CN1-CN3 replaced by multiplexers.	RH850/U2C ports P17_2/P17_3 (CAN XL 0) and P24_7/P24_8 (CAN XL 1) connected to interface function pins on main board connectors CN1-CN3 via series resistor of 33 Ohm.	RH850/U2C ports P17_2/P17_3 (CAN XL 0) and P24_7/P24_8 (CAN XL 1) connected either to CAN XL ports or other function pins on main board connector selectable by jumper JP5 and JP11.

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

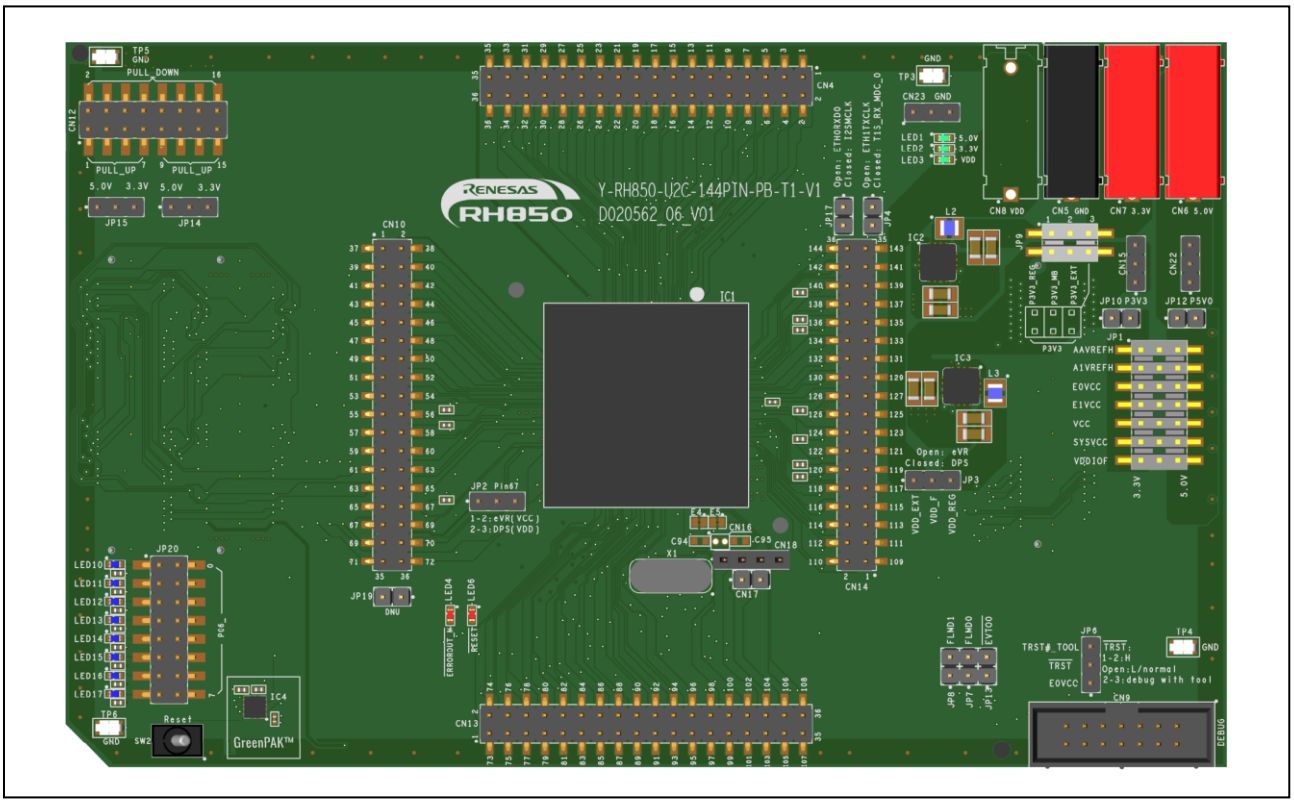


Figure 1.1 Piggyback board top view of board version D020562_06_V01xx

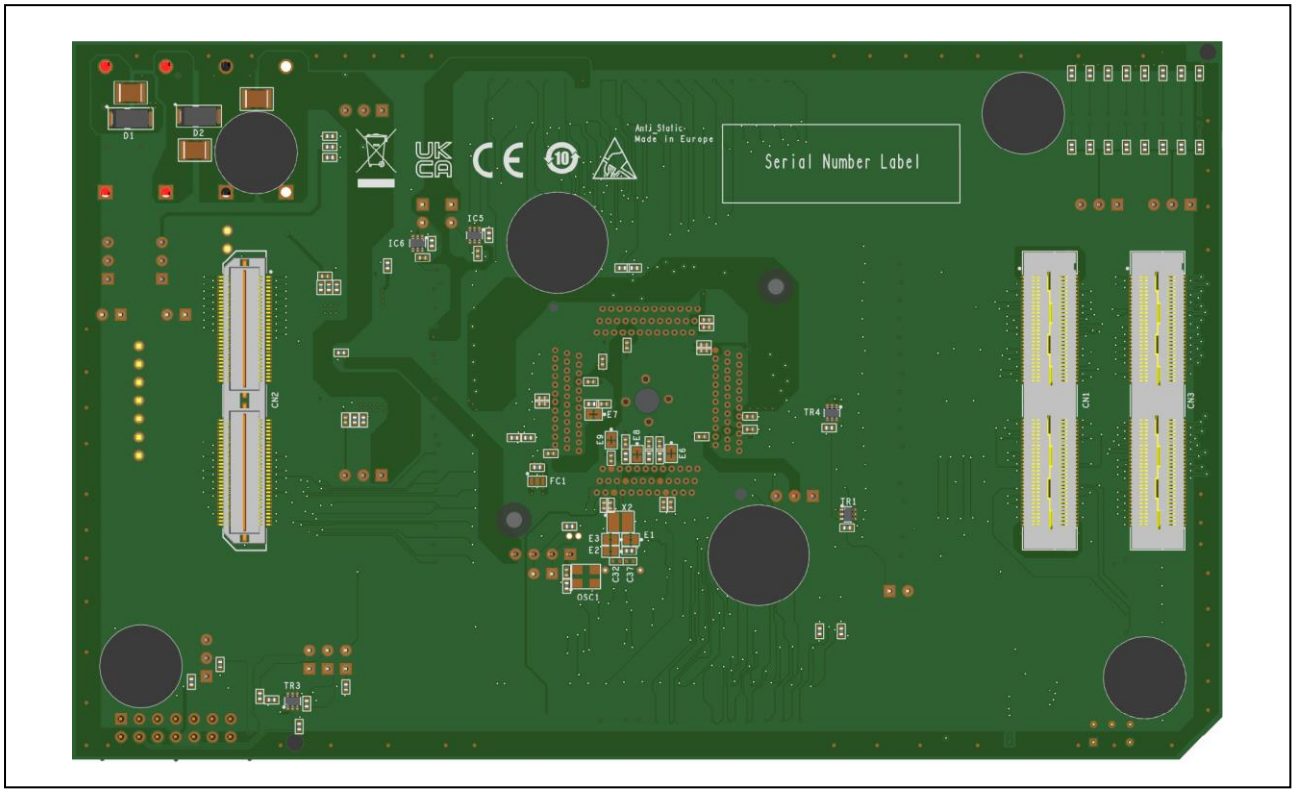


Figure 1.2 Piggyback board bottom view of board version D020562_06_V01xx

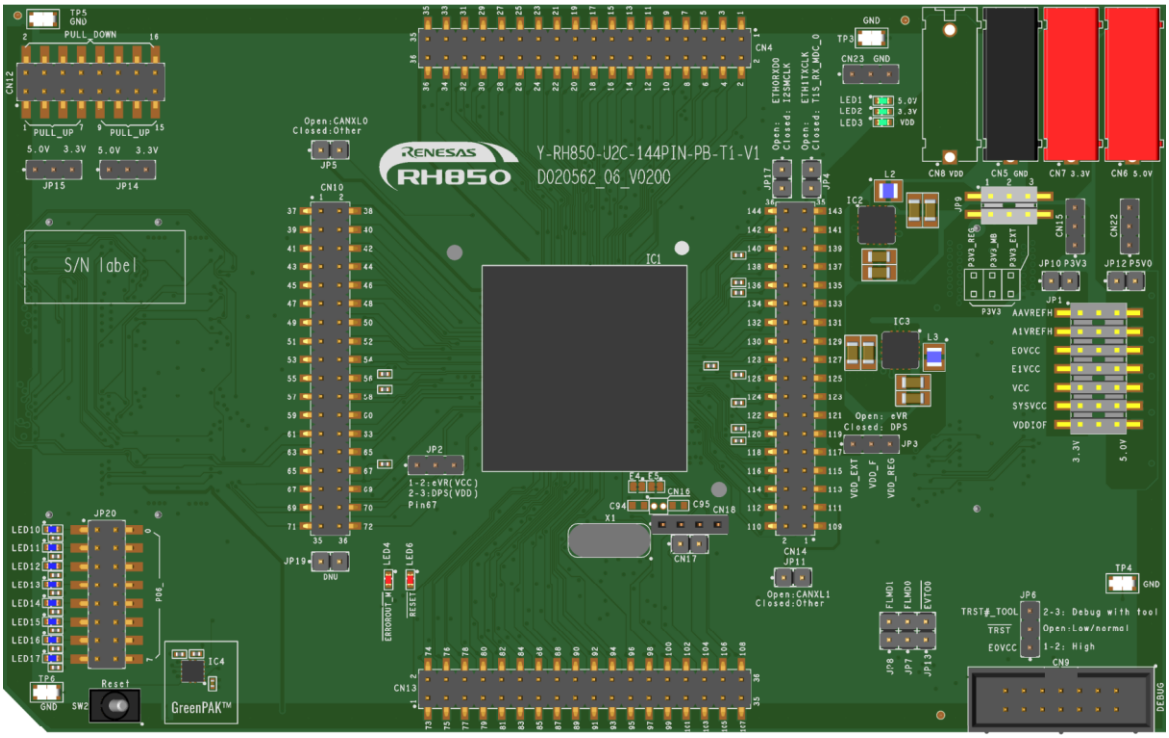


Figure 1.3 Piggyback board top view of board version D020562_06_V0200

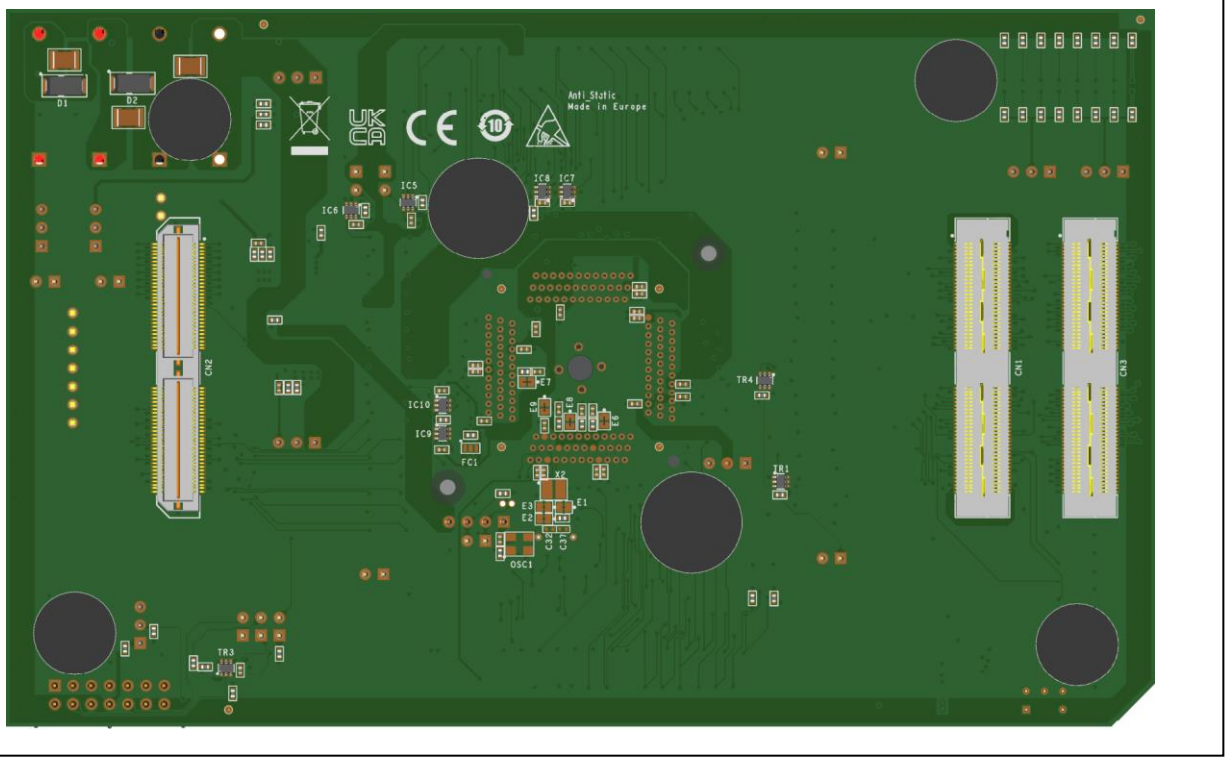


Figure 1.4 Piggyback board bottom view of board version D020562_06_V0200

Following figures provide the drawing of top and bottom views of the piggyback board.

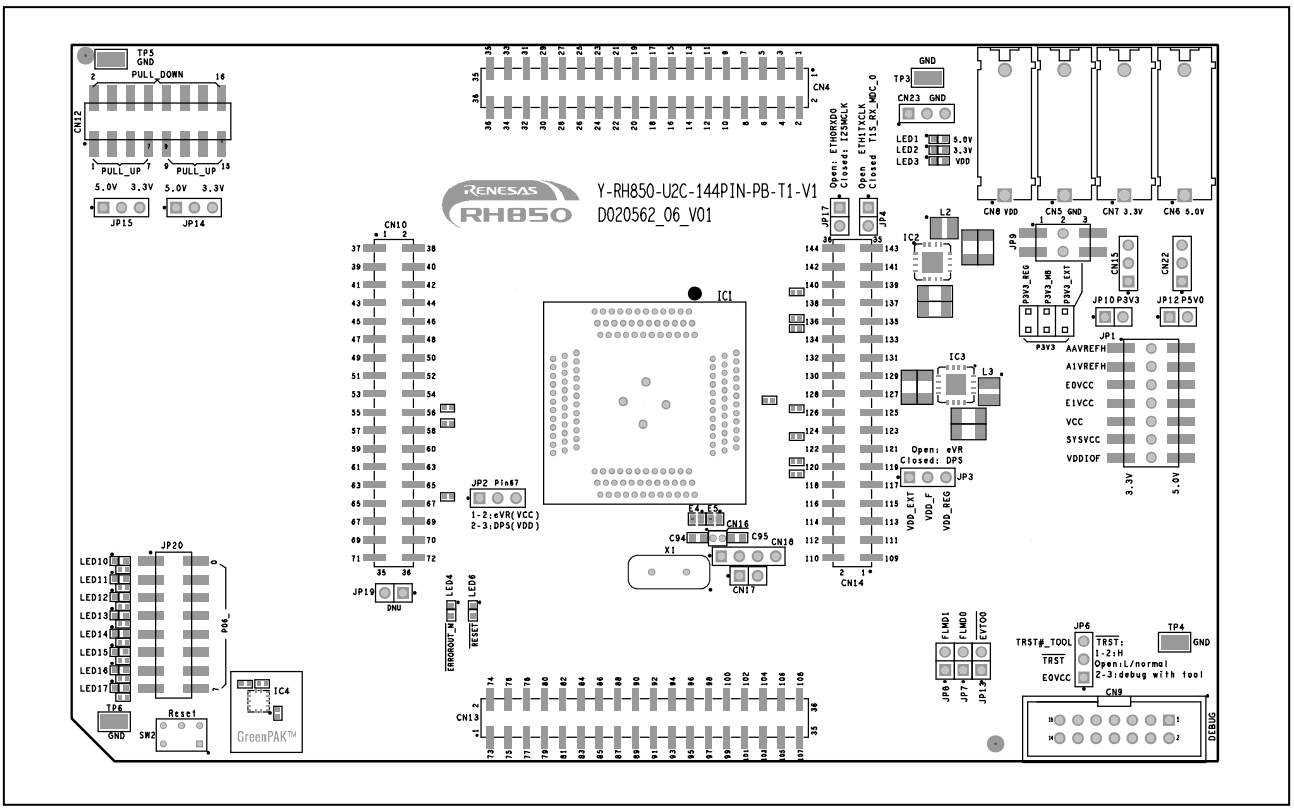


Figure 1.5 Piggyback board top view of board version D020562_06_V01xx

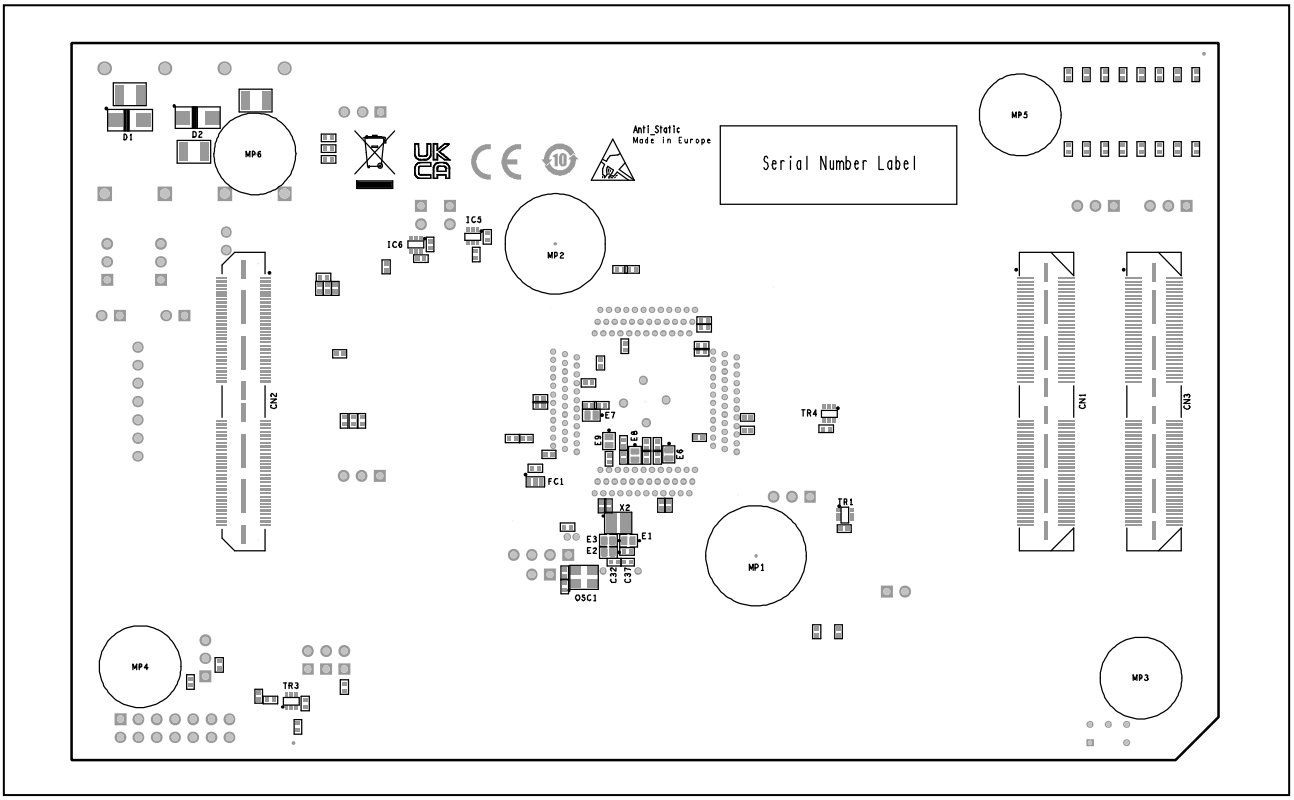


Figure 1.6 Piggyback board bottom view of board version D020562_06_V01xx

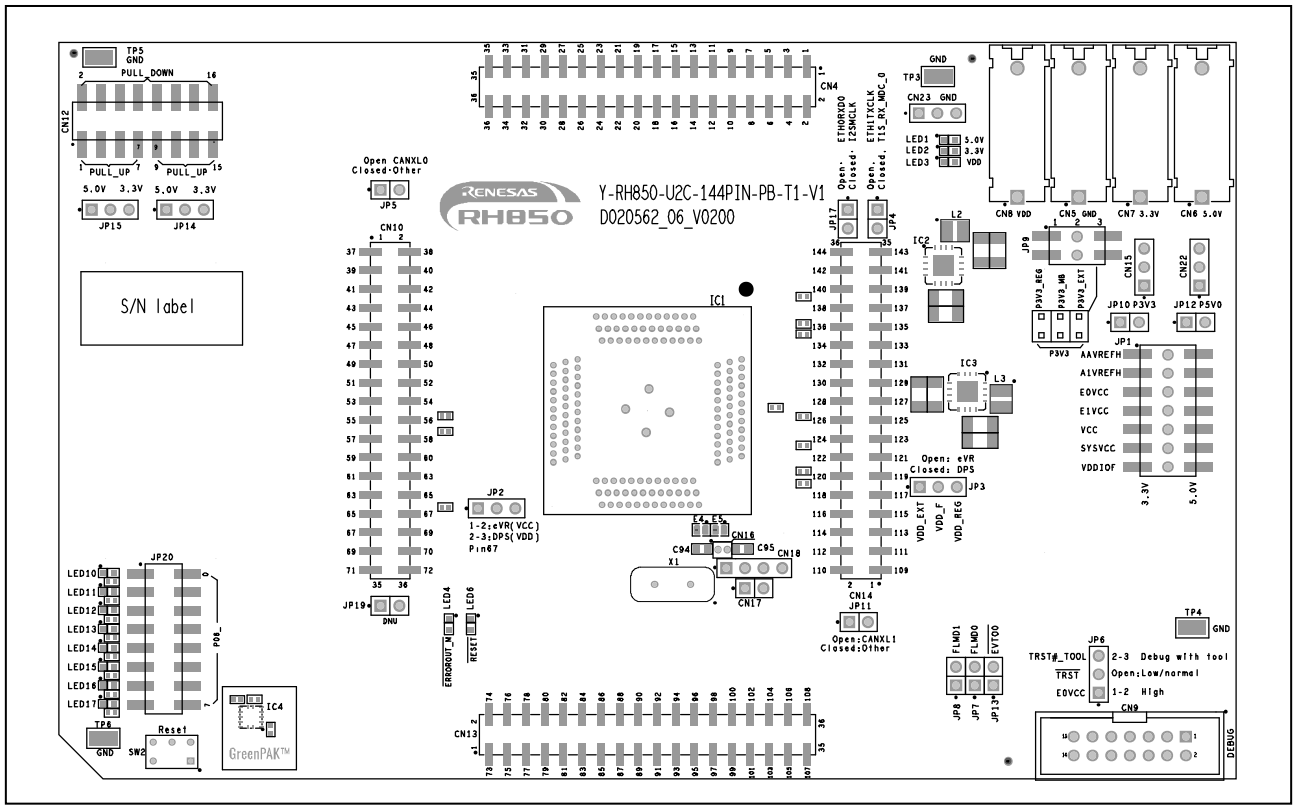


Figure 1.7 Piggyback board top view of board version D020562_06_V0200

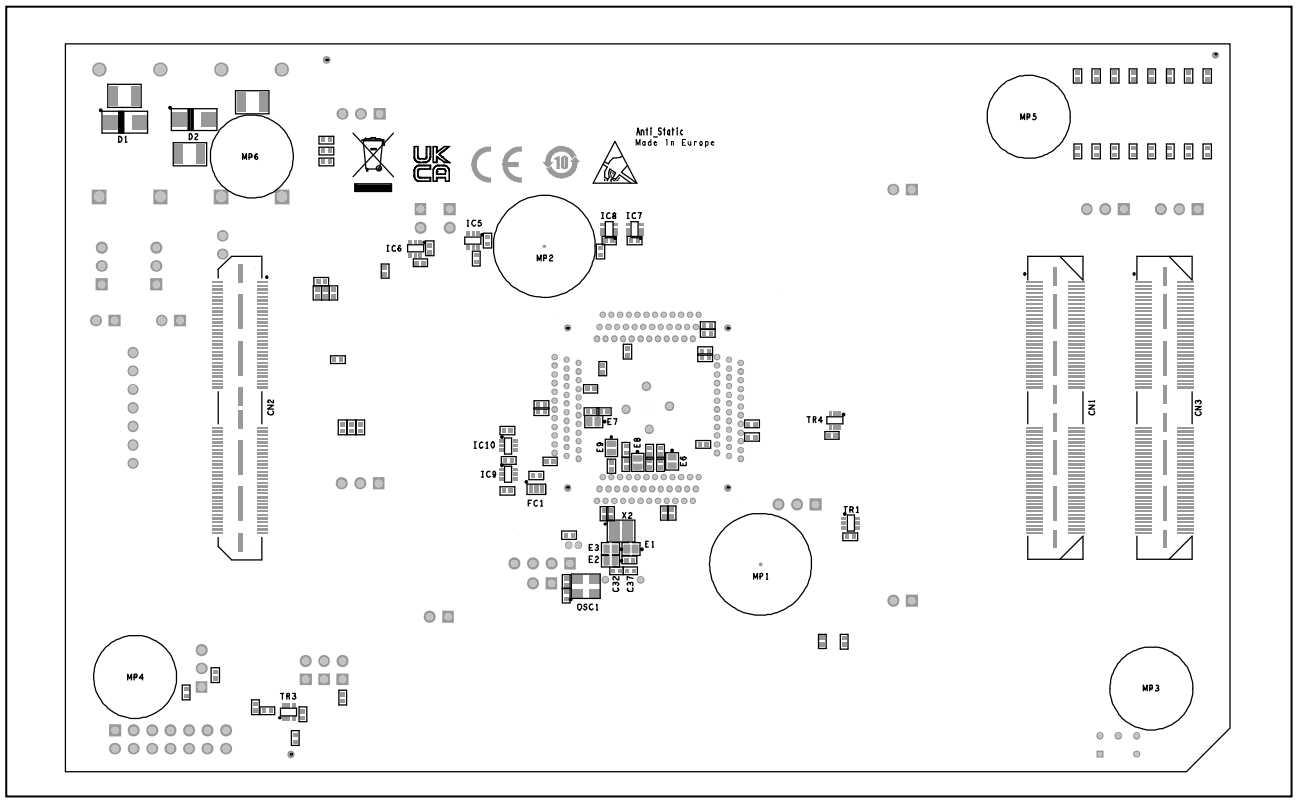


Figure 1.8 Piggyback board bottom view of board version D020562_06_V0200

1.6 Mounting of the Device

The board is designed for use with the following devices.

Table 1.4 Type names for suitable devices

	Device Name	Comments
RH850/U2C4	R7F702606FAFM-C	Core power supply DPS *
	R7F702606AFAFx-C **	
	R7F702614FAFM-C	Core power supply eVR * VCC = VPOC ~ 3.6 V
	R7F702614AFAFx-C **	
	R7F702616AFAFx-C **	Core power supply eVR * VCC = 4.5 V ~ 5.5 V
RH850/U2C2	R7F702615FAFM-C	Core power supply eVR *
	R7F702615AFAFx-C **	

* The isolated area power domain is supplied by an external power supply (DPS) or internal regulator (eVR).

** The character before "-" in device name depends on the assembly site.

The device must be placed inside the socket IC1. To insert the device, align the device package pin 1 with the marking on the pcb. There the A1 pin of the socket is marked with a white dot. Please see *Figure 1.9 Enplas socket OTQ-144SG-0P4-003S-00*.
On the device the index area is available on the corner near the A1 pin.

Figure 1.9 Enplas socket OTQ-144SG-0P4-003S-00

CAUTION

Be careful with the device placement in the socket to avoid damage to the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figures below.

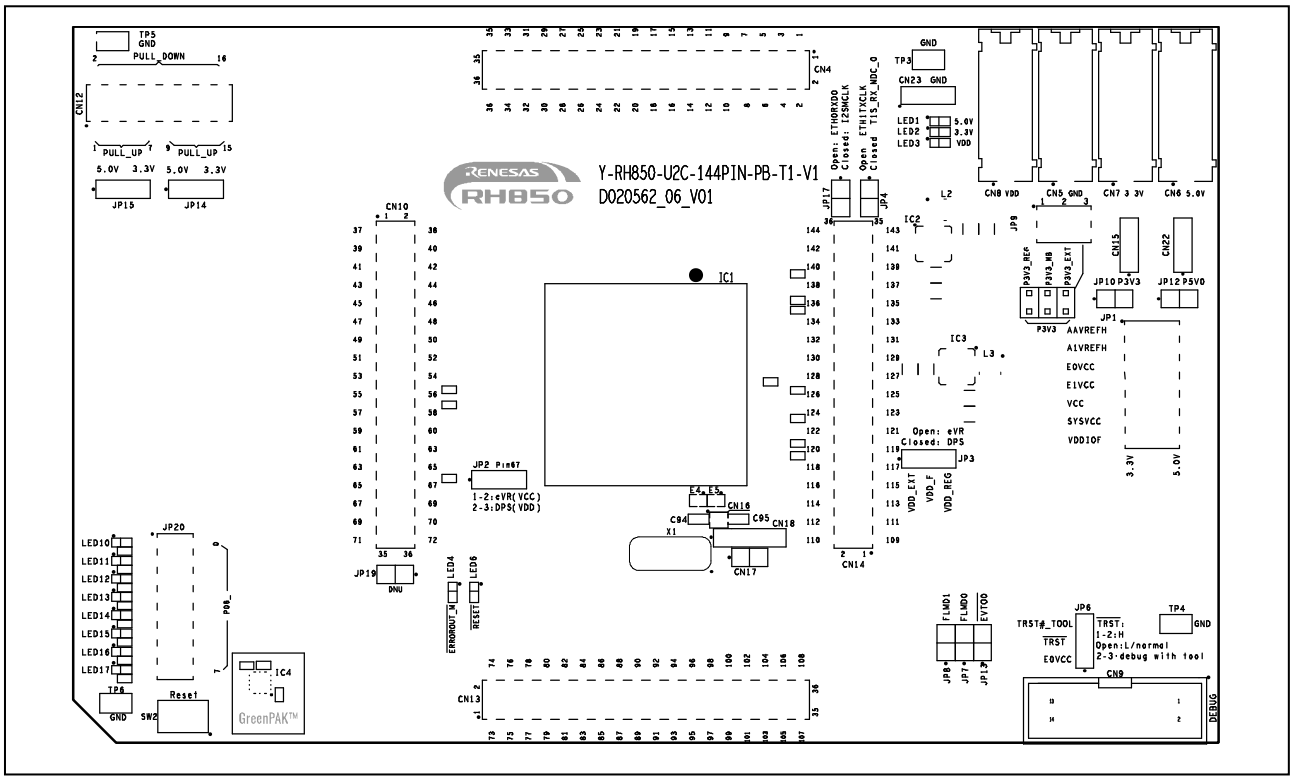


Figure 2.1 Placement of jumpers, connectors and LEDs on top side of board version D020562_06_V01xx

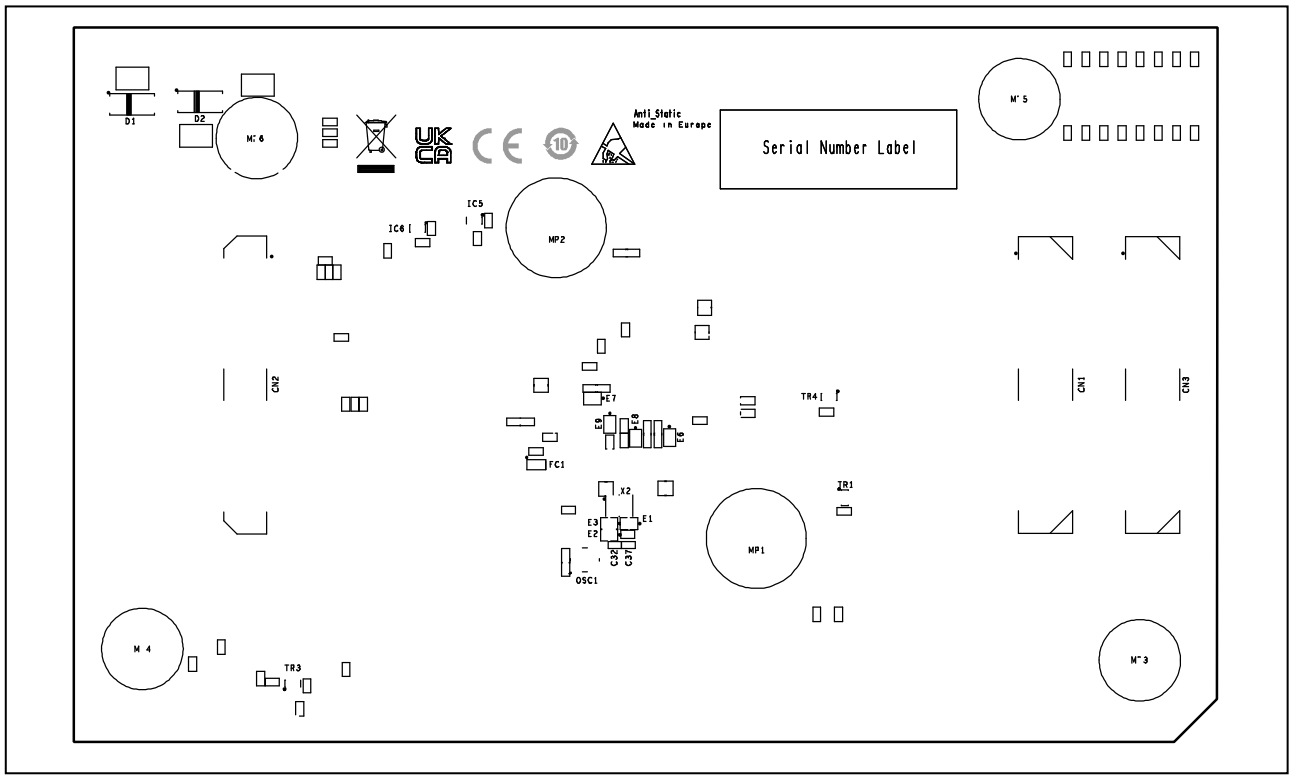


Figure 2.2 Placement of connectors on bottom side of board version D020562_06_V01xx

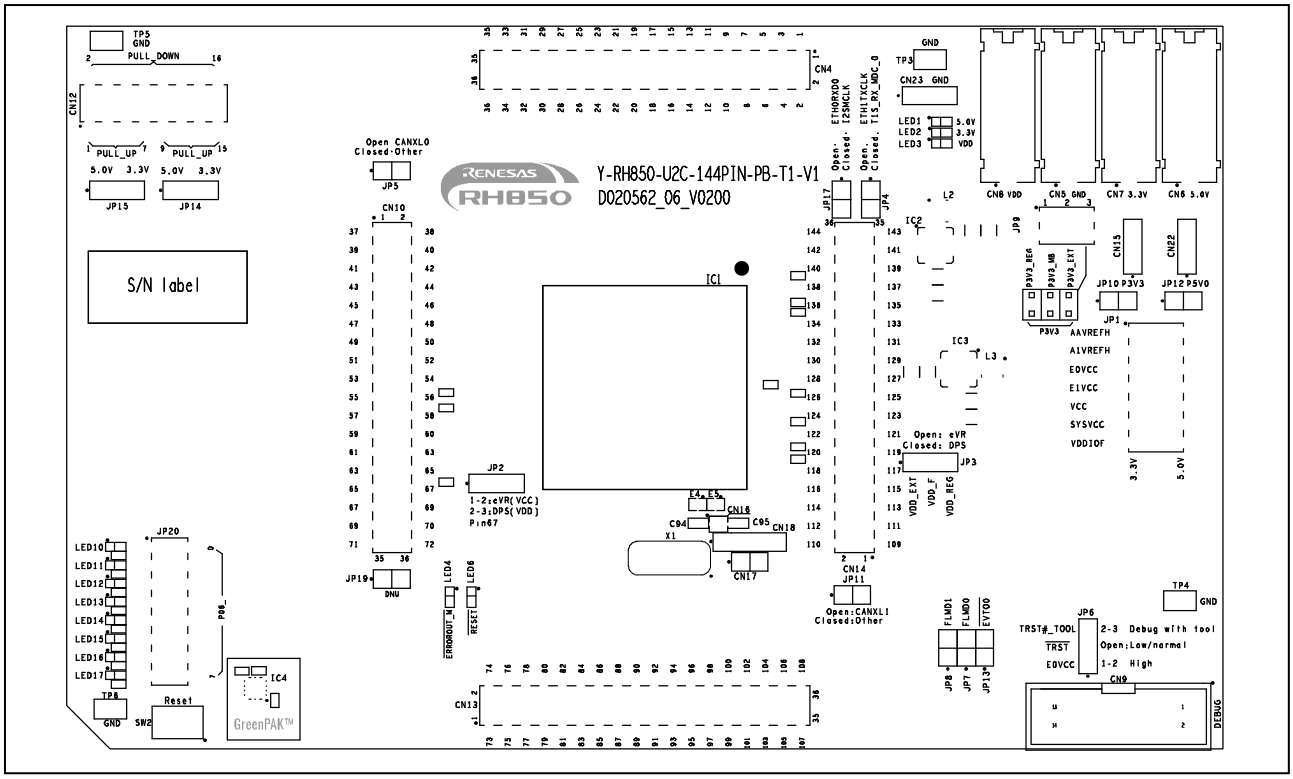


Figure 2.3 Placement of jumpers, connectors and LEDs on top side of board version D020562_06_V0200

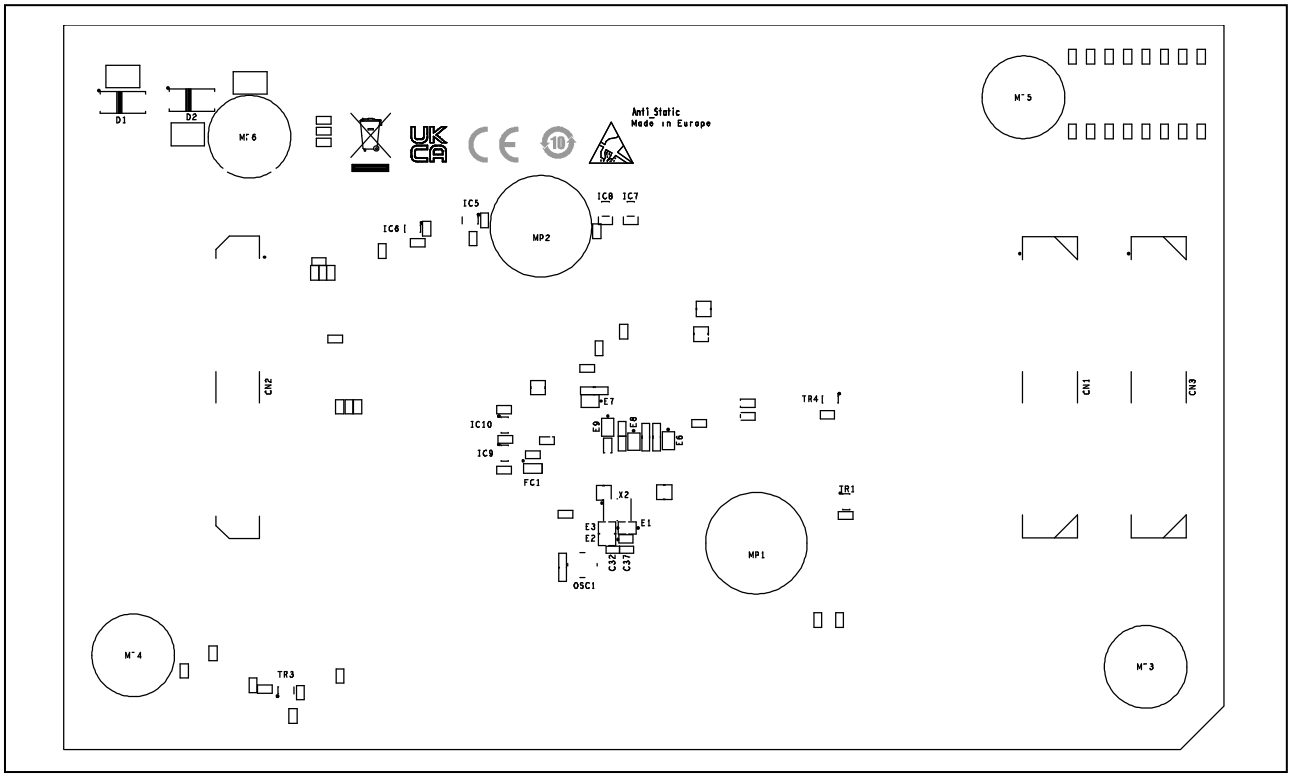


Figure 2.4 Placement of connectors on bottom side of board version D020562_06_V0200

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select +3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
JP2	Device type selection ▪ JP2[1-2]: eVR device ▪ JP2[2-3]: DPS device (U2C4 only)	refer to *3.3 Device Core Voltage (VDD) Selection*
JP3	Core voltage selection for DPS device ▪ JP3[OPEN]: eVR device ▪ JP3[1-2]: VDD supply from external supply CN8 ▪ JP3[2-3]: VDD supply from on-board voltage regulator	
JP4	Select port P20_3 connection for attached main board ▪ JP4[OPEN]: ETH1TXCLK P20_3 connected to B1_P20_3 ▪ JP4[CLOSED]: ETH_T1S_RX_MDC_0 P20_3 connected to B2_P20_3	refer to *6.5 Port P20_3 Selection*
JP5	Select port P17_2 and P17_3 connection for attached main board ▪ JP5[OPEN]: CANXL0 P17_2 connected to B1_P17_2 P17_3 connected to B1_P17_3 ▪ JP5[CLOSED]: SFMA0 / Motor 0 / I2S1 P17_2 connected to B2_P17_2 P17_3 connected to B2_P17_3	refer to *6.3 CAN XL Selection*
JP6	Select signal source for TRST# signal ▪ JP6[1-2]: Fix TRST# signal to E0VCC ▪ JP6[2-3]: TRST# signal is TRST_TOOL# signal from E2 debug connector (pin 3 on connector CN9)	refer to *5 Debug and Flash Programming Interface*
JP7	Change FLMD0 signal to “H”.	refer to *6.1 Operation Mode Selection*
JP8	Change FLMD1 signal to “L”.	
JP9	Select +3.3 V power supply source ▪ JP[1-4]: Get +3.3 V from onboard voltage regulator ▪ JP[2-5]: Get +3.3 V from main board ▪ JP[3-6]: Get +3.3 V from external +3.3 V supply on CN7	refer to *3.2 Voltage Distribution*
JP10	Current measurement bridge +3.3 V	refer to *3.4 Current Measurement Bridges*
JP11	Select port P24_7 and P24_8 connection for attached main board ▪ JP11[OPEN]: CANXL1 P24_7 connected to B1_P24_7 P24_8 connected to B1_P24_8 ▪ JP11[CLOSED]: MMCA / LIN14 / FlexRay 1 / MUX1 P24_7 connected to B2_P24_7 P24_8 connected to B2_P24_8	refer to *6.3 CAN XL Selection*
JP12	Current measurement bridge +5.0 V	refer to *3.4 Current Measurement Bridges*
JP13	Debug port connection EVTO0	refer to *5 Debug and Flash Programming Interface*

Table 2.1 Jumper overview (cont'd)

Jumper	Function	Remark
JP14 JP15	Select pull-up voltage for Pull-Up Pull-Down connector CN12 ▪ JP14[1-2]: 5.0 V pull-up on pins 9 / 11 / 13 / 15 ▪ JP14[2-3]: 3.3 V pull-up on pins 9 / 11 / 13 / 15 ▪ JP15[1-2]: 5.0 V pull-up on pins 1 / 3 / 5 / 7 ▪ JP15[2-3]: 3.3 V pull-up on pins 1 / 3 / 5 / 7	refer to *6.8 Pull-Up/Pull-Down Pin Header*
JP17	Select port P20_0 connection to an attached main board ▪ JP17[OPEN): ETH0RXD0 P20_0 connected to B1_P20_0 ▪ JP17[CLOSED): I2SMCLK P20_0 connected to B2_P20_0	refer to *0* *Port P20_0* Selection
JP19	Jumper for board production test	Must be left open
JP20	Enable signal LED outputs	refer to *6.7 Signalling LEDs*

2.2 LED Overview

The following table provides an overview of all LED.

Table 2.2 LED overview

LED	Function	Color	Remark
LED1	5.0 V power supply P5V0	green	refer to *3.5 Power Supply LEDs*
LED2	3.3 V power supply int_P3V3	green	
LED3	LED_PG_VDD signal	green	refer to *6.2 System State and RESET*
LED4	LED_ERROROUT_M# signal	red	
LED6	LED_RESET# signal	red	
LED10	Signaling LED	blue	refer to *6.7 Signalling LEDs*
LED11			
LED12			
LED13			
LED14			
LED15			
LED16			
LED17			

2.3 Connector Overview

The following table provides an overview of all connectors.

Table 2.3 Connector overview

Connector	Function	Remark
CN1	Main board connectors	refer to *7.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN4	Device ports connector	refer to *0* *Device Ports Connectors CN4, CN10, CN13* and CN14
CN5	GND external power supply	refer to *3.1 Board Power Connection*
CN6	+5.0 V external power supply	
CN7	+3.3 V external power supply	
CN8	+1.09 V external power supply	
CN9	E2 emulator debug connector	refer to *5 Debug and Flash Programming Interface*
CN10	Device ports connector	refer to *0* *Device Ports Connectors CN4, CN10, CN13* and CN14
CN12	Pull-up / pull-down connector	refer to *6.8 Pull-Up/Pull-Down Pin Header*
CN13	Device ports connector	refer to *0* *Device Ports Connectors CN4, CN10, CN13* and CN14
CN14		
CN15	+3.3 V connector	
CN16	Socket for sub-oscillator	refer to *4.4 Sub Oscillator*
CN17	IP0_0 and IP0_1 connector	
CN18	IP0_0 and IP0_1 fixed inputs	
CN22	+5.0 V connector	
CN23	GND connector	

2.4 Switches Overview

The following table provides an overview of all switches.

Table 2.4 Switches overview

Connector	Function	Remark
SW2	RESET# switch	refer to *6.2 System State and RESET*

3. Power Supply

3.1 Board Power Connection

RH850/U2C and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board.
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage.
- 1.09 V for RH850/U2C core voltage VDD.
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as ‘typical’.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm ‘banana-type’ connectors are used to connect external power supplies:
  - black connector CN5 for GND (VSS)
  - red connector CN6 for 5.0 V (P5V0)
  - red connector CN7 for 3.3 V (P3V3_EXT)
  - red connector CN8 for 1.09 V (P1V09_EXT)
    Connector CN8 is not assembled at delivery of the board, but separately supplied with the board package.
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

If the piggyback board is mounted on a main board, all voltages except for 1.09 V (VDD) can be supplied by the main board.

- The jumper JP9[2-5] (3.3 V) is used to enable P3V3 supply from main board.
- P5V0 is supplied from the main board.

CAUTION

Do not supply the 5 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board if power supply from the main board is enabled.

Connecting external 1.09 V via CN8 (and GND via CN5) is still an option also in this case.

The piggyback board has 2 voltage regulator circuits. Both use Renesas ISL78234 buck regulator.

IC2 generates the board voltage of 3.3V (P3V3_REG) from 5.0V (P5V0) input voltage on CN6.

IC3 generates the core voltage of 1.09V (P1V09_REG) from 3.3V (P3V3).

Figure 3.1 shows both voltage regulator circuits.

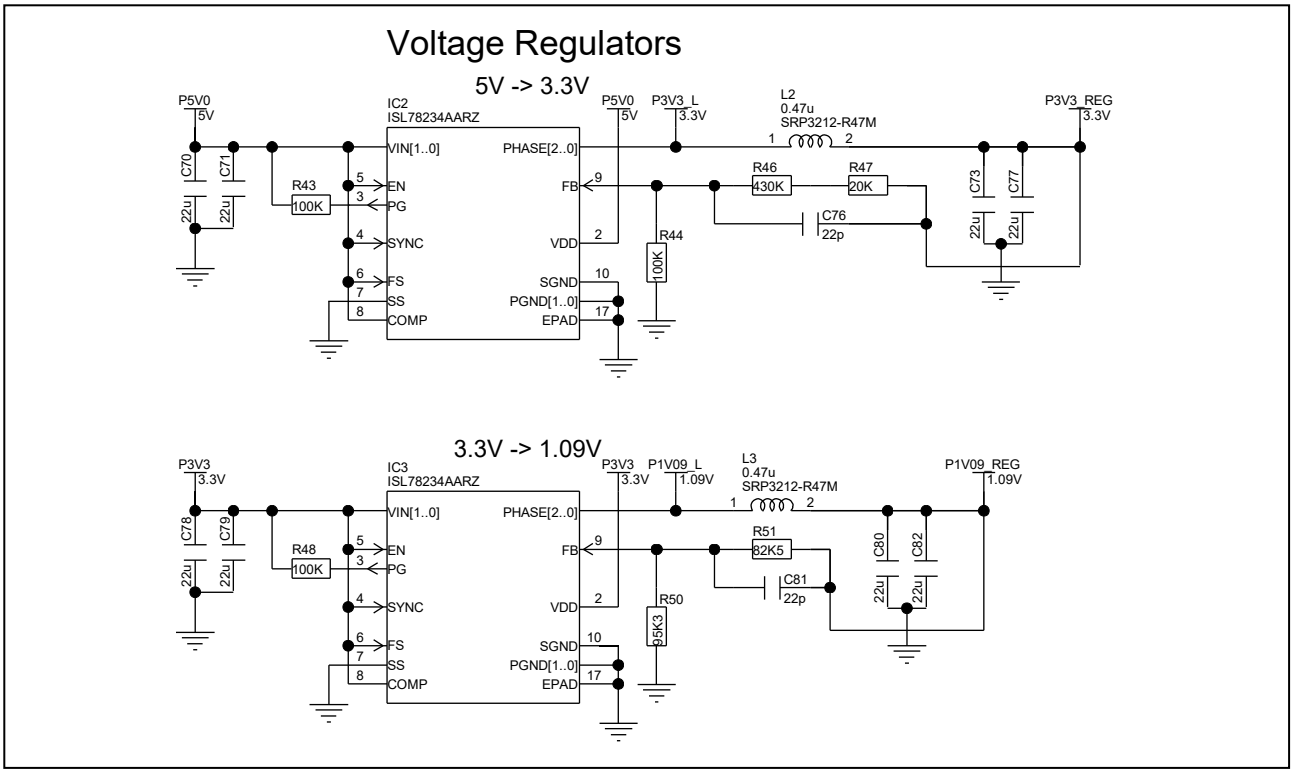


Figure 3.1 Voltage regulator circuit

The jumper settings for some general power supply scenarios are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

Table 3.1 shows the required device power supply pins and their function.

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
AAVREFH, A1VREFH	3.3 V, 5 V	A/D converter's power supplies and reference voltages
E0VCC, E1VCC	3.3 V, 5 V	Power supply for I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
VDD_F	1.09 V	Core supply voltage Refer to *3.3 Device Core Voltage (VDD)* Selection

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V (P3V3) can be selected from external power supply (P3V3_EXT, CN7), main board power supply (P3V3_MB) or from the onboard voltage regulator (P3V3_REG) using jumper JP9:

- JP9 [1-4]: P3V3 comes from the onboard voltage regulator P3V3_REG.
- JP9 [2-5]: P3V3 comes from the main board power supply P3V3_MB.
- JP9 [3-6]: P3V3 comes from the external power supply P3V3_EXT / CN7.

The supply for 5.0 V (P5V0) may come from the external power supply CN6 or from the main board.

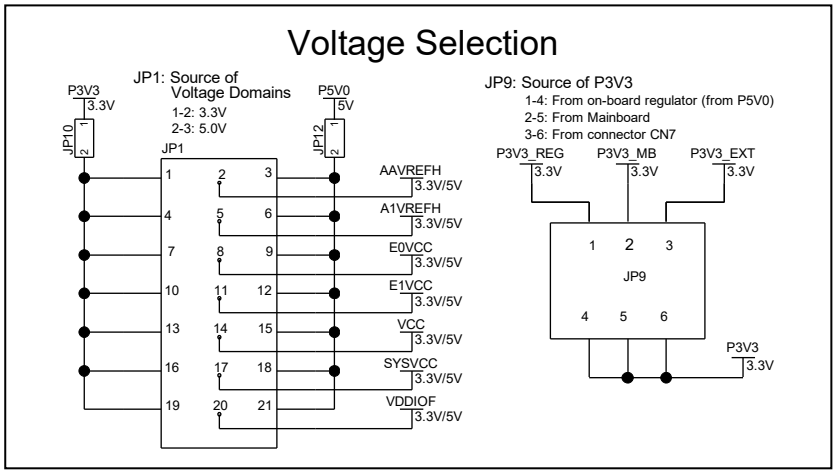


Figure 3.2 Voltage distribution

Note

Please make sure not to supply 5.0 V (P5V0) from connector CN6 and the main board at the same time.

Table 3.2 shows which jumpers to set to select the different device supply voltages, and *Figure 3.2* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
AAVREFH	JP1 [1-2]	JP1 [2-3]
A1VREFH	JP1 [4-5]	JP1 [5-6]
E0VCC	JP1 [7-8]	JP1 [8-9]
E1VCC	JP1 [10-11]	JP1 [11-12]
VCC	JP1 [13-14]	JP1 [14-15]
SYSVCC	JP1 [16-17]	JP1 [17-18]
VDDIOF	JP1 [19-20]	JP1 [20-21]

3.3 Device Core Voltage (VDD) Selection

The piggyback board can be used with RH850/U2C2 and RH850/U2C4 processors. RH850/U2C processors have different options for core voltage generation.

RH850/U2C2 devices have always an embedded voltage regulator (eVR) for internal core voltage generation.

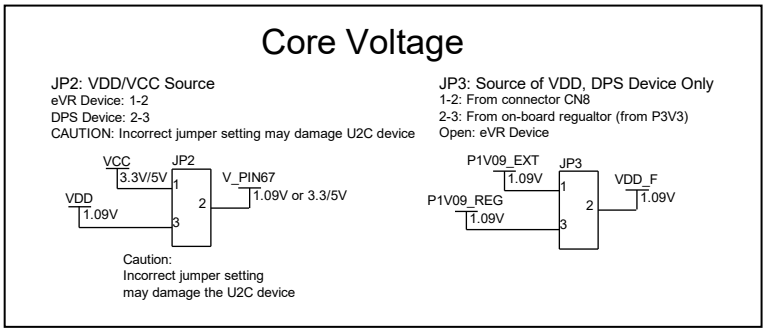


Figure 3.3 Core voltage selection

RH850/U2C4 devices are available as device with embedded voltage regulator (eVR) or with external 1.09V supply (DPS) for core voltage.

The external core voltage VDD (typ.1.09 V) for RH850/U2C4 DPS devices can be

- supplied from external via CN8 (voltage P1V09_EXT)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage P1V09_REG)

Table 3.3 shows the jumper setting for core voltage supply, Figure 3.3 shows the related circuit diagrams.

Table 3.3 eVR / DPS core voltage supply selection

Jumper	Function
JP2	RH850/U2C core voltage supply selection ▪ JP2[1-2]: eVR (U2C2 or U2C4) ▪ JP2[2-3]: DPS (U2C4 only)
JP3	RH850/U2C core voltage supply selection ▪ JP3[OPEN]: eVR device ▪ JP3[1-2]: DPS device, external VDD supply (VDD_F = P1V09_EXT) ▪ JP3[2-3]: DPS device, VDD from on-board voltage regulator (VDD_F = P1V09_REG)

3.4 Current Measurement Bridges

The total current of the 5V0 and 3V3 power rails can be measured by replacing the jumpers JP10 and JP12 with a current meter.

The current of particular power supply pins of the device can be measured via their respective supply selection jumpers, refer to *Figure 3.2 Voltage distribution*.

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED1 for 5.0 V power rail P5V0
- LED2 for 3.3 V power rail P3V3
- LED3 for 1.09 V device core voltage VDD

4. Clock Supply

RH850/U2C supports 2 oscillator circuits.

The ports X1 and X2 are used for the main oscillator.

The ports IP0_0 and IP0_1 can be used to connect a sub-clock for a real time clock function.

Figure 4.1 and *Figure 4.2* show the oscillator circuits.

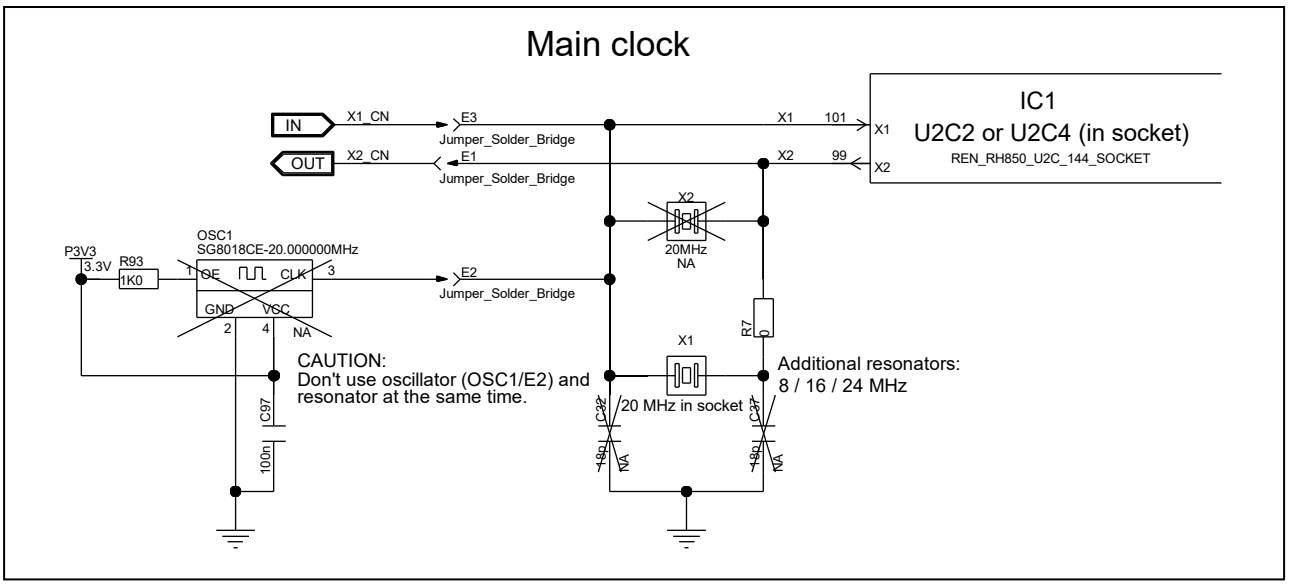


Figure 4.1 Main oscillator circuit

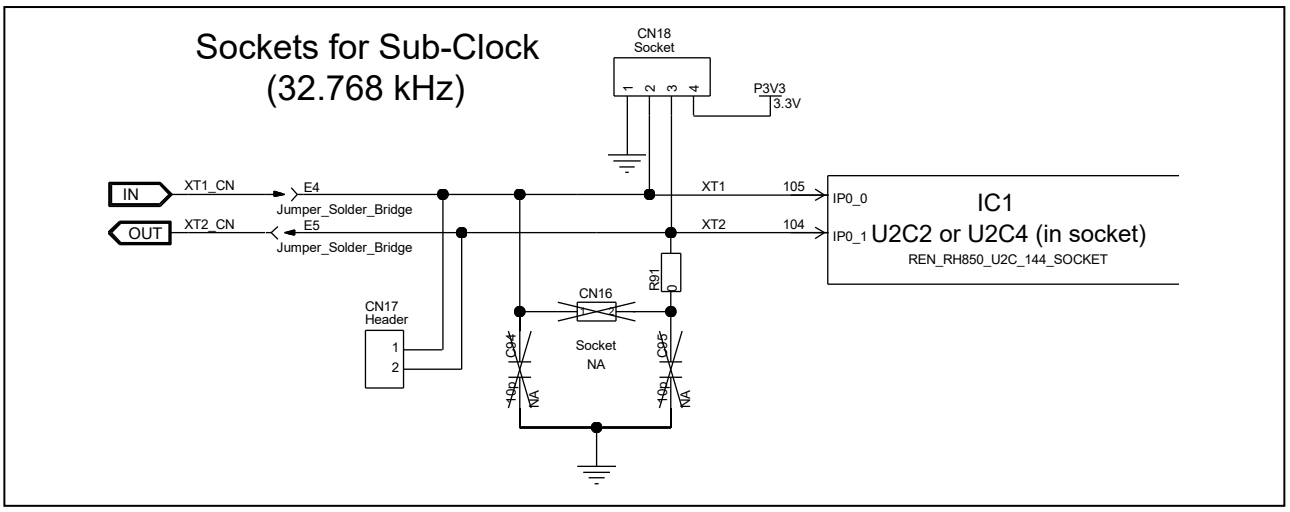


Figure 4.2 Sub-clock oscillator circuit

CAUTION

Only one oscillator, either X1, X1_CN, X2 or OSC1, can be used at any one time for the main oscillator.

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Several resonators for various main oscillator frequencies (8 MHz, 16 MHz, 20 MHz, 24 MHz) are included in the board package. The 20MHz resonator is by default mounted to X1.

For package content please refer to *1.1 Package Components*.

The piggyback board has a foot print on the lower side of the pcb to mount an oscillator of a different physical dimension.

4.2 External Oscillator

The clock signals from an external oscillator can be input to the piggyback board using the pins 29 (X1_CN, clock input) and 27 (X2_CN, clock monitor) on device pin connector CN13.

To use the external clock input the solder bridge E3 must be closed.

To use the clock monitor signal the solder bridge E1 must be closed.

4.3 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via solder bridge E2.

For details about the available circuitry, refer to *Figure 4.1*.

4.4 Sub Oscillator

The pins IP0_0 and IP0_1 can be used as oscillator pins XT1 and XT2 to connect a real-time clock oscillator.

If no oscillator is connected the pins IP0_0 and IP0_1 can be used as input ports.

If an oscillator is connected this oscillator is started by programming the SOSCE (Sub OSC Enable) register.

The piggyback board has 4 possibilities to connect a sub oscillator.

1. The board has solder pads to add an oscillator socket to connector CN16.
2. The board has a 2 pin connector CN17 to input oscillator signal from an external sub clock oscillator.
3. The board has a 4 pin connector CN18 where an external oscillator module can be connected.
4. The oscillator pins IP0_0 and IP0_1 can be connected via solder bridges E4 (IP0_0) and E5 (IP0_1) to the device pin header CN13 (IP0_0: pin 33, IP0_1: pin 32). Thus the sub clock signal can be input to the device header pins.

For details about the available circuitry, refer to *Figure 4.2*.

5. Debug and Flash Programming Interface

For debugging and flash programming purposes debug and flash programming tools can be connected to CN9 connector.

The Renesas standard emulator for RH850/U2C is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

Figure 5.1 shows the circuit diagram for the emulator interface.

CN9 is the debug connector for Renesas E2 emulator.

The piggyback board has three jumpers to enable control signals coming from the emulator.

Jumper JP6 controls the input signal of TRST# to RH850/U2C.

- JP6[OPEN]: TRST# input to RH850/U2C is fixed to “L” level.
- JP6[1-2]: TRST# input to RH850/U2C is fixed to “H” level input.
- JP6[2-3]: TRST# input to RH850/U2C is fixed to “L” level input. If an emulator is connected to connector CN9, the emulator can control this signal.

Jumper JP7 enables the FLMD0 signal connection from the emulator to RH850/U2C.

- JP7[OPEN]: FLMD0 input to RH850/U2C is fixed to “L” level. If an emulator is connected to connector CN9, the emulator can control this signal.
- JP7[CLOSED]: FLMD0 signal input to RH850/U2C is fixed to “H” level input.

RH850/U2C can provide an event trigger signal to a connected emulator. Jumper JP13 enables the EVTO0# signal connection from RH850/U2C to the emulator.

- JP13[OPEN]: EVTO0# signal is not connected to the emulator.
- JP13[CLOSED]: EVTO0# signal can be output to the emulator.

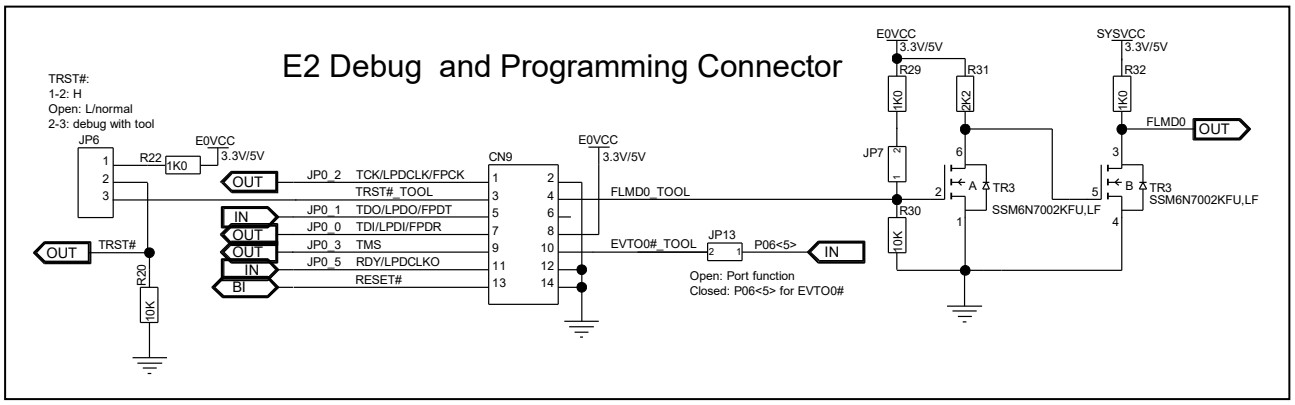


Figure 5.1 E2 debug connector CN9

6. Other Circuitry

6.1 Operation Mode Selection

RH850/U2C has 3 pins related to operating mode selection. The pins are TRST#, FLMD0 and FLMD1. The piggyback board gives the possibility to configure these pins using jumpers JP6, JP7 and JP8.

Table 6.1 shows the functionality of the jumpers, *Figure 6.1* shows the circuit diagrams.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP6	TRST# signal ▪ JP6[OPEN]: TRST# fixed to “L” level ▪ JP6[1-2]: TRST# fixed to “H” level ▪ JP6[2-3]: TRST# control from emulator
JP7	FLMD0 pin level ▪ JP7[CLOSED]: FLMD0 = H level ▪ JP7[OPEN]: FLMD0 • controlled by debugger or programming tool if a tool is connected via CN9 • GND, if no tool connected
JP8	FLMD1 pin level ▪ JP8[CLOSED]: FLMD1 = GND ▪ JP8[OPEN]: FLMD1 open

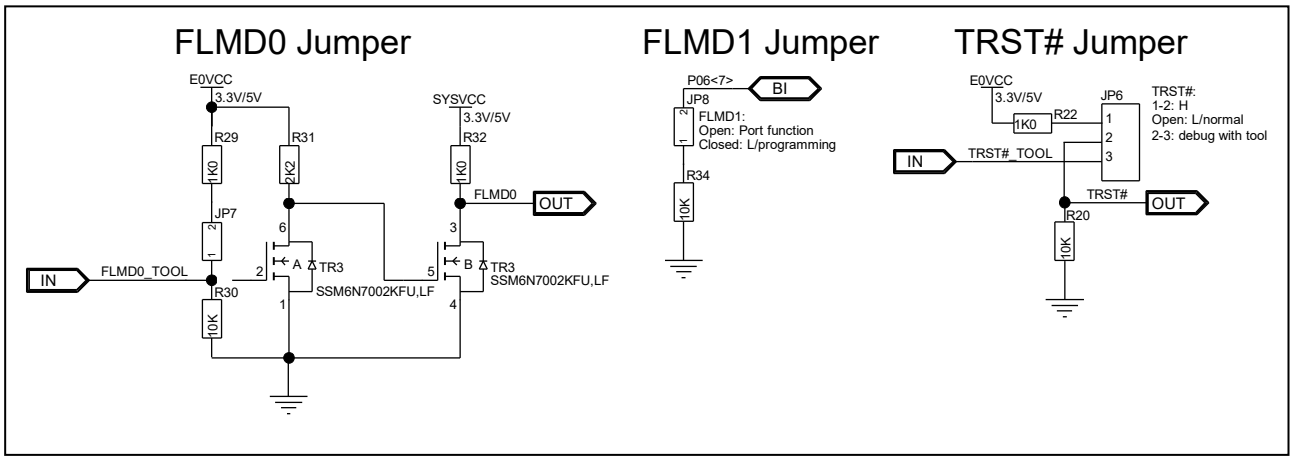


Figure 6.1 Operating mode selection jumpers

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User’s Manual for details, which modes are specified for the used device.

Note

In most cases the ‘normal operating mode’ of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the ‘normal operating mode’ of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP7.

All other jumpers related to the mode selection can be left open.

6.2 System State and RESET

This piggyback board has a special reset circuit using the Renesas GreenPAK IC SLG7RN47274. This IC is designed to receive various RH850 control signals and switch control LEDs accordingly. It also receives the signal from the RESET switch SW2 to generate the reset signal for the piggyback board and controls the reset LED.

The piggyback board has 3 LED to indicate control signals and reset status:

- LED3 is the control LED for RH850/U2C core voltage VDD.
- LED4 is a control signal triggered by ERROROUT_M# or VMONOUT#.
- LED6 is a reset signal triggered by the reset switch SW2.

6.2.1 Circuit Diagram

Figure 6.2 RESET circuit shows the circuit of the GreenPAK IC and the reset signal inputs.

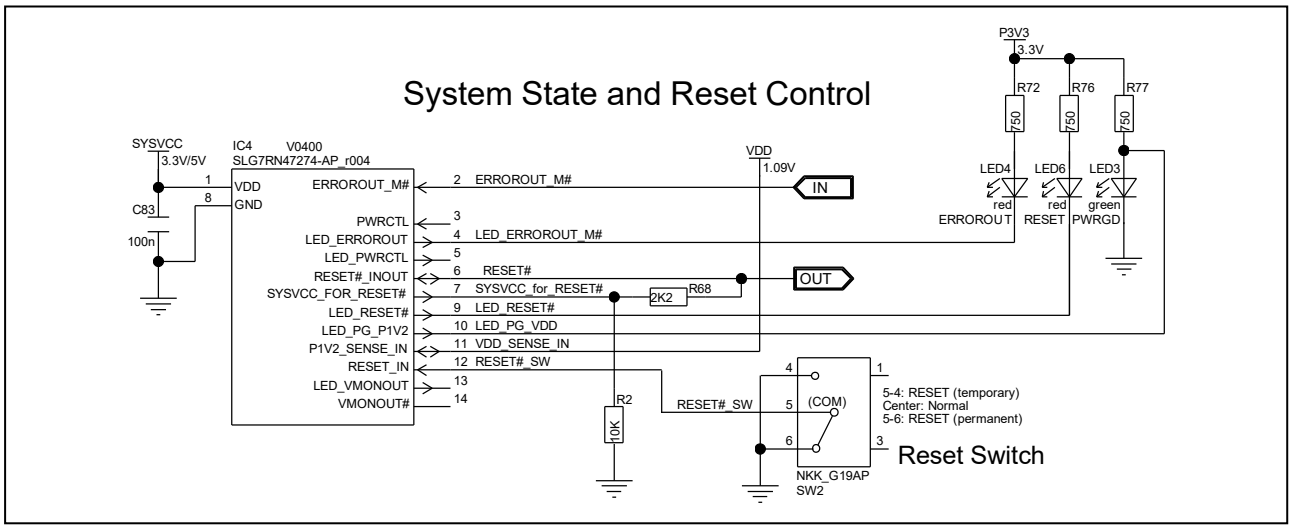


Figure 6.2 RESET circuit

6.2.2 RESET Switch

Switch SW2 is used to issue a reset to the RH850/U2C.

The SW2 toggle switch allows to activate the reset in two different ways:

- SW2 in left '5-4' (left) position: momentary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW2 in right '5-6' (right) position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

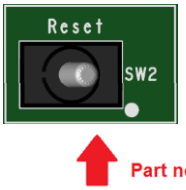


Figure 6.3 Operation of RESET switch

6.3 CAN XL Selection

RH850/U2C Ports P17_2/P17_3 are connected CAN XL 0 ports on connector CN1 pins 71 and 73.
RH850/U2C Ports P24_7/P24_8 are connected CAN XL 1 ports on connector CN1 pins 72 and 74.

On board revision D020562_06_V0100 various functional pins on the main board connectors were connected in parallel, and all of them connected to RH850 ports via series resistor.

It turned out that this layout causes unwanted disturbances if the CAN XL function should be used.

Thus the circuit was modified. In board revision D020562_06_V0200 the CAN XL functions on connector CN2 have been separated from other functional pins on the main board connectors by multiplexers. These multiplexers are controlled by jumpers JP5 and JP11.

Table 6.2 lists the related ports and jumpers and shows which functions are available for which jumper setting.

Figure 6.4 shows the circuit diagrams of the multiplexer circuits.

Table 6.2 CAN XL port selection jumpers

	Jumper JP5 = CLOSED	Jumper JP5 = OPEN	Jumper JP11 = CLOSED	Jumper JP11 = OPEN
Port P17_2	B2_P17_2 (SFMA0IO1 / MOT0V_P / I2S1RXD)	B1_P17_2 (CANXL0RX)	---	---
Port P17_3	B2_P17_2 (SFMA0IO0 / MOT0V_N / I2S1TXD)	B1_P17_3 (CANXL0TX)	---	---
Port P24_7	---	---	B2_P24_7 (FLX1TX / MUX0 / LIN14TX / MMCA0DAT3)	B1_P24_7 (CANXL1TX)
Port P24_8	---	---	B2_P24_8 (FLX1RX / LIN14RX / MMCA0CLK)	B1_P24_8 (CANXL1RX)

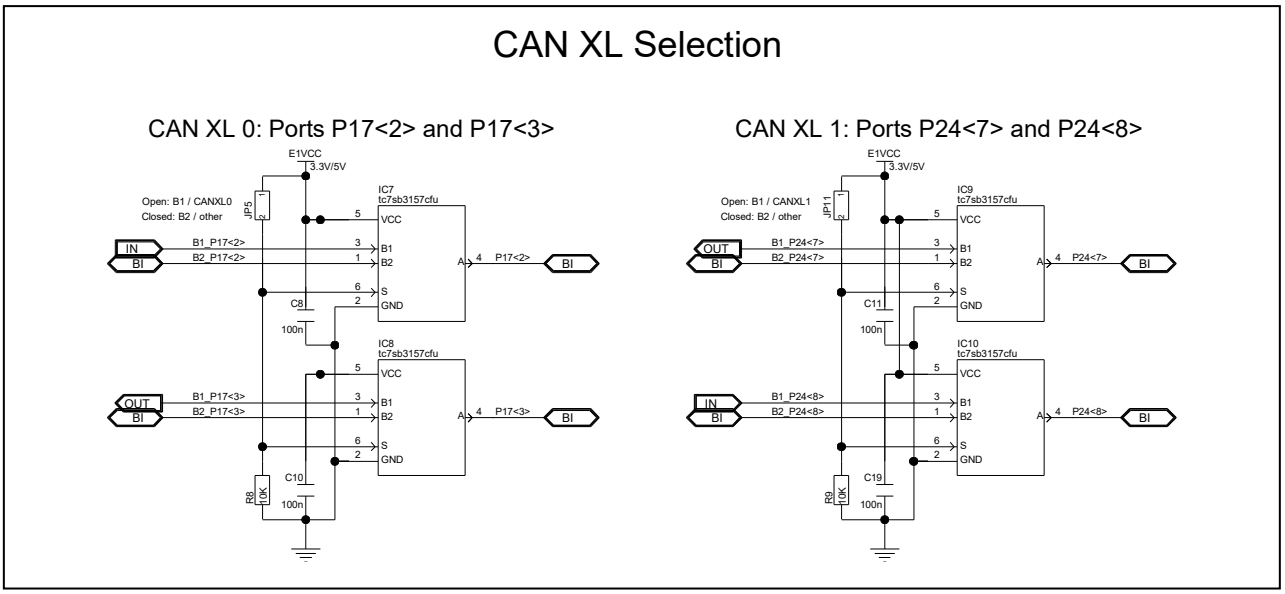


Figure 6.4 CAN XL port selection on board revision D020526_06_V0200

6.4 Port P20_0 Selection

Port P20_0 can be used for I2SMCLK or ETH0RXD0 signal to an attached main board.

Jumper JP17 is used to select which signal is being used.

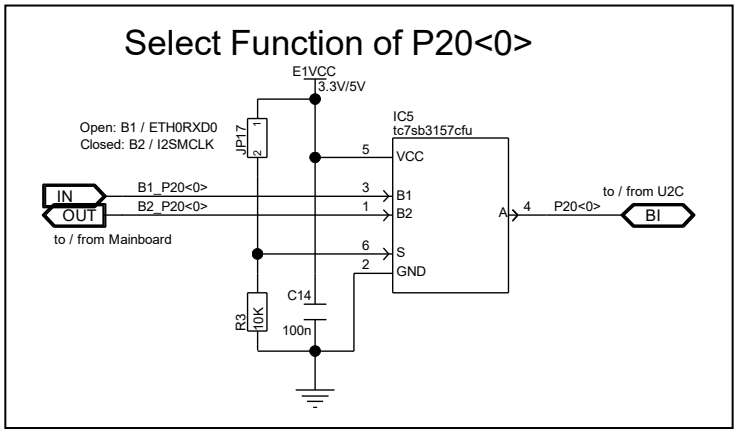


Figure 6.5 Circuit diagram for P20_0 signal selection

Table 6.3 Port P20_0 function selection jumper

Jumper	Function
JP17 [OPEN]	P20_0 = ETH0RXD0
JP17 [CLOSED]	P20_0 = I2SMCLK

6.5 Port P20_3 Selection

Port P20_3 can be used for ETH1TXCLK or ETH_T1S_RX_MDC_0 signal to an attached main board.

Jumper JP4 is used to select which signal is being used.

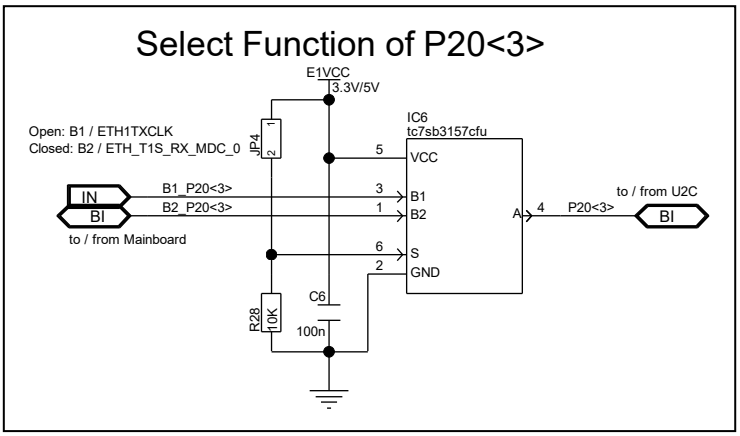


Figure 6.6 Circuit diagram for P20_3 signal selection

Table 6.4 Port P20_3 function selection jumper

Jumper	Function
JP4 [OPEN]	P20_3 = ETH1TXCLK
JP4 [CLOSED]	P20_3 = ETH_T1S_RX_MDC_0

6.6 Series Termination Resistors

The piggyback board includes several series resistors, that can be used as termination resistors for high-speed communication channels. All signals are connected to the main board connectors CN1 – CN3.

On board revision D020562_06_V0100 the series resistors are used for the CAN XL ports and the Ethernet ports. However, it was discovered that this caused disturbances on the CAN XL ports so the CAN XL interface could not be used at full speed.

On board revision D020562_06_V0200 the series resistors are only used for the Ethernet ports. The series resistors for the CAN XL ports were replaced by multiplexers so the CAN XL ports are not connected to other ports anymore. Refer to chapter *6.3 CAN XL Selection* for details on the multiplexers.

The resistors R8 – R11 are only used as series resistors on board revision D020562_06_V0100.

On board revision D020562_06_V0200 R8 and R9 are part of the multiplexer circuit, R10 and R11 don't exist.

The placement for the series resistors for Ethernet ports is the same on both board revisions.

Figure 6.7 shows the circuit diagram for the series resistors on board revision D020562_06_V0100.

Figure 6.8 shows the circuit diagram for the series resistors on board revision D020562_06_V0200.

Figure 6.9 shows the location of the resistors on the lower side of the piggyback board.

Table 6.5 Series termination resistors

Table 6.5 lists all resistors and shows to which signal on the main board connector they are connected.

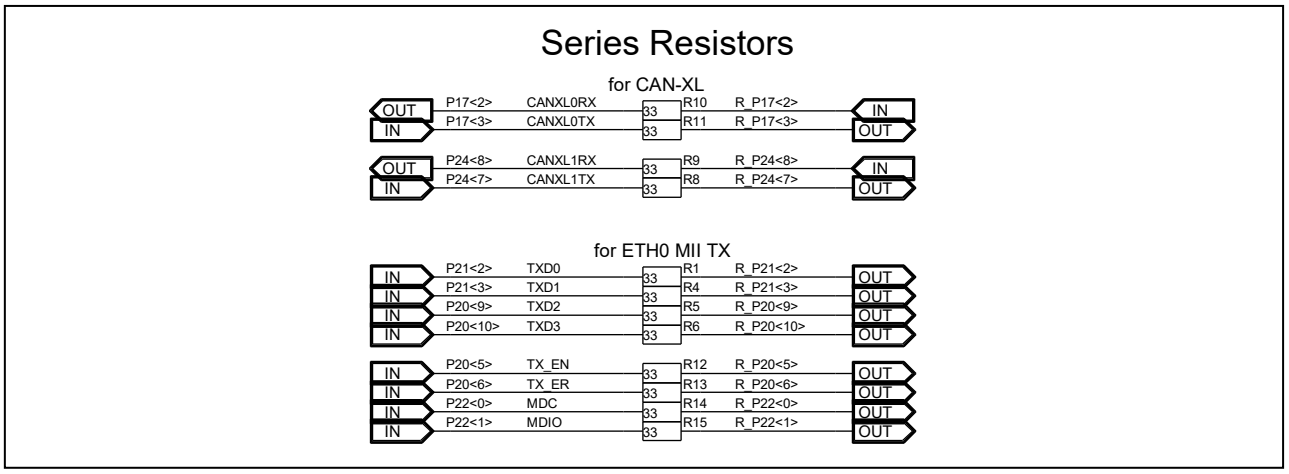


Figure 6.7 Series termination resistors on board revision D020526_06_V0100

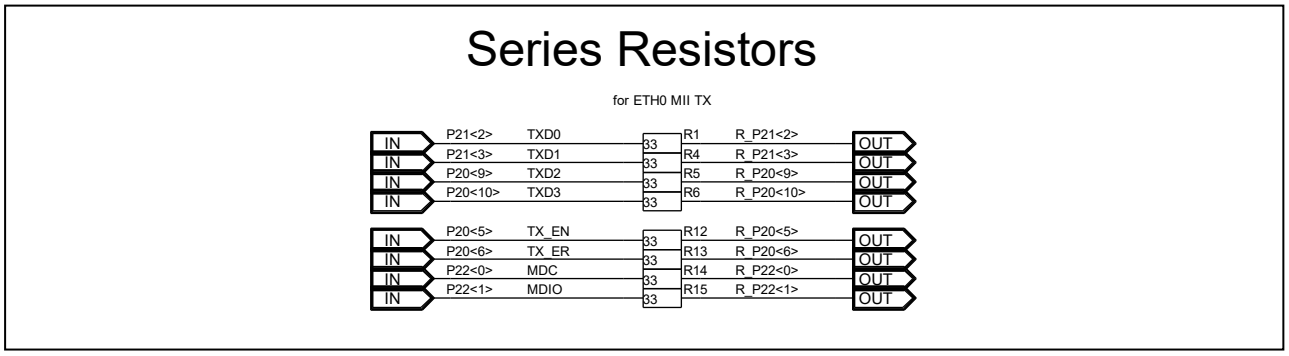


Figure 6.8 Series termination resistors on board revision D020526_06_V0200

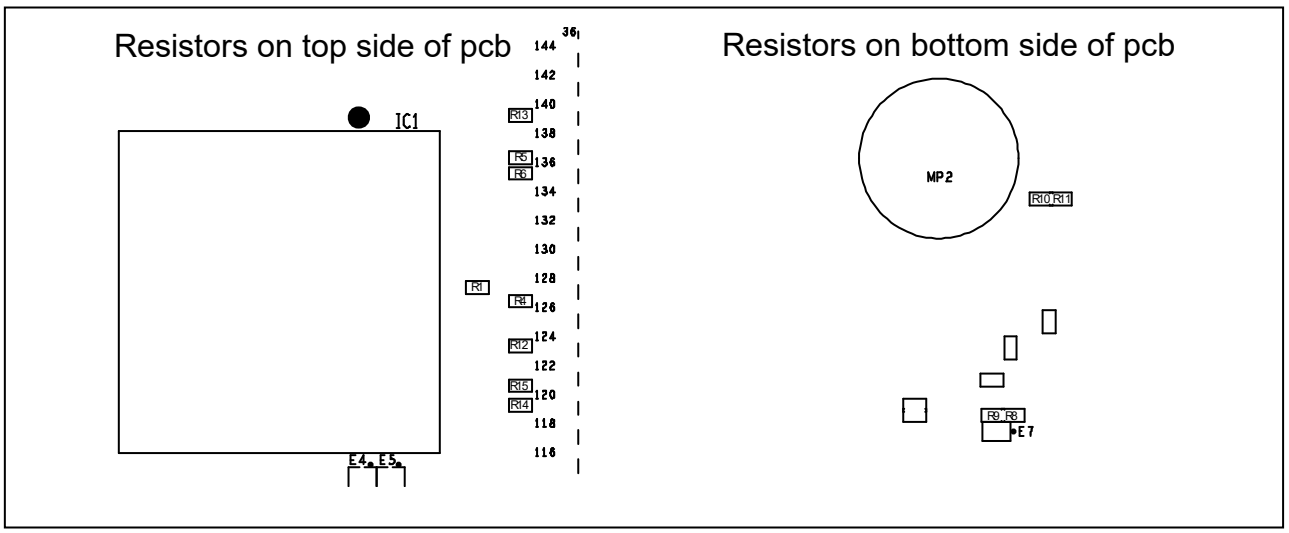


Figure 6.9 Location of series termination resistors

Table 6.5 Series termination resistors

Resistor	RH850 Port	Signal Name	Connector
R8 (only board revision D020562_06_V0100)	P24_7	CANXL1TX / FLX1TX	CN1_72 / CN1_45
R9 (only board revision D020562_06_V0100)	P24_8	CANXL1RX / FLX1RX	CN1_74 / CN1_47
R10 (only board revision D020562_06_V0100)	P17_2	CANXL0RX / I2S1RXD	CN1_73 / CN3_14
R11 (only board revision D020562_06_V0100)	P17_3	CANXL0TX / I2S1TXD	CN1_71 / CN3_12
R1	P21_2	ETH0TXD0	CN1_54
R4	P21_3	ETH0TXD1	CN1_56
R5	P20_9	ETH0TXD2	CN1_58
R6	P20_10	ETH0TXD3	CN1_60
R12	P20_5	ETH0TXEN	CN1_66
R13	P20_6	ETH0TXER	CN1_64
R14	P22_0	ETH0MDC	CN1_52
R15	P22_1	ETH0MDIO	CN1_51

6.7 Signalling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

The device pins P06_0 – P06_7 are connected to the even pins of the jumper JP20.

The LEDs LED10 to LED17 are connected to the odd JP20 pins.

Thus, the LEDs can be either connected to

- the device port pins P06_0 – P06_7 by closing the corresponding jumper on JP20.
- any device pin by connecting the pin (from the connectors CN4, CN10, CN13, and CN14) directly with the odd JP20 pins using a separate cable.

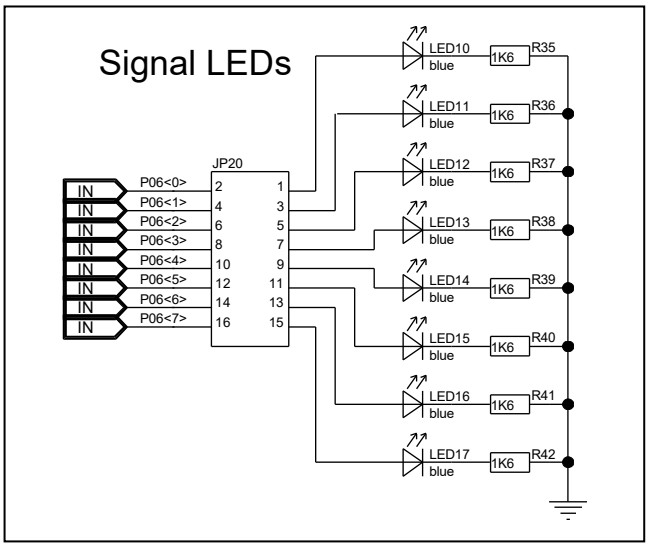


Figure 6.10 Circuit diagram for signalling LEDs

6.8 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- All even numbered pins are connected to L level, i.e. to GND.
- Odd numbered pins 1, 3, 5 and 7 are connected to jumper JP15 and can be pulled up to 3.3 V or 5.0 V.
- Odd numbered pins 9, 11, 13 and 15 are connected to jumper JP14 and can be pulled up to 3.3 V or 5.0 V.

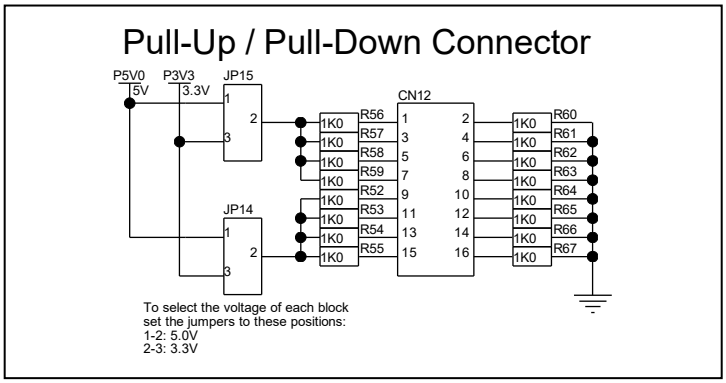


Figure 6.11 Circuit diagram for pull up / pull down signals

Refer to *0*

Pull-Up/Pull-Down Pin Header CN12 for CN12 details.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.

Refer to *0*

Supported Main Boards for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Function on		Device port	Pin	Function on		Device port
	Main Board	Piggyback			Main Board	Piggyback	
1	VDDA	–	–	2	VDDA	–	–
3	VDDA	–	–	4	VDDA	–	–
5	RESET	RESET#	RESET#	6	NMI	NMI	P02_3
7	WAKE	–	–	8	–	–	–
9	INT0	IRQ27	P06_12	10	INT1	IRQ34	P04_4
11	INT2	IRQ16	P06_13	12	INT3	IRQ20	P06_7
13	–	–	–	14	–	–	–
15	UART0TX	RLIN33TX	P06_3	16	UART1TX	RLIN36TX	P04_15
17	UART0RX	RLIN33RX	P06_2	18	UART1RX	RLIN36RX	P04_14
19	LIN0TX	RLIN30TX	P06_6	20	LIN1TX	RLIN31TX	P06_4
21	LIN0RX	RLIN30RX	P06_7	22	LIN1RX	RLIN31RX	P06_5
23	IIC0SCL	RI3C2SCL	P24_11	24	IIC1SCL	RI3C1SCL	P06_8
25	IIC0SDA	RI3C2SDA	P24_12	26	IIC1SDA	RI3C1SDA	P06_9
27	CAN0TX	CAN0TX	P02_2	28	CAN1TX	CAN1TX	P04_12
29	CAN0RX	CAN0RX	P02_0	30	CAN1RX	CAN1RX	P04_13
31	SENT0RX	RSENT2RX	P02_9	32	SENT1RX	RSENT5RX	P04_14
33	SENT0SPCO	RSENT2SPCO	P02_8	34	SENT1SPCO	RSENT5SPCO	P04_15
35	PSI5SRX0	–	–	36	PSI5RX0	–	–
37	PSI5STX0	–	–	38	PSI5TX0	–	–
39	PSI5SCLK0	–	–	40	–	–	–
41	FLX0TX	FLXA0TXDA *1	P24_12	42	FLX0EN	FLXA0TXENA *1	P24_10
43	FLX0RX	FLXA0RXDA *1	P24_11	44	FLXSTPWT	FLXA0STPWT *1	R_P22_1
45	FLX1TX	FLXA0TXDB *1	R_P24_7 *2 B2_P24_7 *3	46	FLX1EN	FLXA0TXENB *1	P24_9
47	FLX1RX	FLXA0RXDB *1	R_P24_8 *2 B2_P24_8 *3	48	FLX1CLK	–	–
49	–	–	–	50	–	–	–
51	ETH0MDIO	ETH0_MDIO *1	R_P22_1	52	ETH0MDC	ETH0_MDC *1	R_P22_0
53	ETH0RXD0	ETH0_MII_RXD0 *1	B1_P20_0	54	ETH0TXD0	ETH0_MII_TXD0 *1	R_P21_2
55	ETH0RXD1	ETH0_MII_RXD1 *1	P20_1	56	ETH0TXD1	ETH0_MII_TXD1 *1	R_P21_3
57	ETH0RXD2	ETH0_MII_RXD2 *1	P10_1	58	ETH0TXD2	ETH0_MII_TXD2 *1	R_P20_9

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
59	ETH0RXD3	ETH0_MII_RXD3 *1	P10_2
61	ETH0RXCLK	ETH0_MII_RX_CLK *1	P10_3
63	ETH0RXER	ETH0_RMII_ER *1	P20_12
65	ETH0CRSDV	–	–
67	ETH0RXDV	ETH0_MII_RX_DV *1	P20_2
69	ETH0RESET	P17_0	P17_0
71	CANXL0TX	CANXL0TXD	R_P17_3 *2 B1_P17_3 *3
73	CANXL0RX	CANXL0RXD	P17_2 *2 B1_P17_2 *3
75	CANXL2TX	–	–
77	CANXL2RX	–	–
79	ETH0_T1S_TX	ETS0_TX *1	P20_4
81	ETH0_T1S_ RX_MDC	ETS0_RX_MDC *1	B2_P20_3
83	ETH0_T1S_ ED_MDIO	ETS0_ED_MDIO *1	P20_13
85	DIGIO_0	P06_10	P06_10
87	DIGIO_2	P06_12	P06_12
89	DIGIO_4	P04_5	P04_5
91	DIGIO_6	–	–
93	DIGIO_8	–	–
95	DIGIO_10	–	–
97	DIGIO_12	–	–
99	DIGIO_14	P06_3	P06_3
101	–	–	–
103	MUX0	P24_7	R_P24_7 *2 B2_P24_7 *3
105	MUX2	P22_3	P22_3
107	ADC0	ADCK1I12	AP2_12
109	ADC2	ADCK1I14	AP2_14
111	ADC4	–	–
113	ADC6	–	–
115	VDDIOF	–	–
117	VDDB	–	–
119	VDDB	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
60	ETH0TXD3	ETH0_MII_TXD3 *1	R_P20_10
62	ETH0TXCLK	ETH0_MII_TX_CLK *1	P21_1
64	ETH0TXER	ETH0_MII_TX_ER *1	R_P20_6
66	ETH0TXEN	ETH0_MII_TX_EN *1	R_P20_5
68	ETH0COL	–	–
70	ETH0LINK	ETH0_LINKSTA *1	P22_2
72	CANXL1TX	CANXL1TXD *1	R_P24_7 *2 B1_P24_7 *3
74	CANXL1RX	CANXL1RXD *1	P24_8 *2 B1_P24_8 *3
76	CANXL3TX	–	–
78	CANXL3RX	–	–
80	ETH1_T1S_TX	–	–
82	ETH1_T1S_ RX_MDC	–	–
84	ETH1_T1S_ ED_MDIO	–	–
86	DIGIO_1	P06_11	P06_11
88	DIGIO_3	P06_13	P06_13
90	DIGIO_5	–	–
92	DIGIO_7	–	–
94	DIGIO_9	–	–
96	DIGIO_11	–	–
98	DIGIO_13	P06_2	P06_2
100	DIGIO_15	P06_4	P06_4
102	–	–	–
104	MUX1	P22_2	P22_2
106	–	–	–
108	ADC1	ADCK1I13	AP2_13
110	ADC3	–	–
112	ADC5	–	–
114	ADC7	–	–
116	VDDIOF	–	–
118	VDDB	–	–
120	VDDB	–	–

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Only RH850/U2C4
*2 Board revision D020562_06_V0100
*3 Board revision D020562_06_V0200

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function on		Device port
	Main Board	Piggyback	
1	CAN2TX	CAN2TX	P06_0
3	CAN2RX	CAN2RX	P06_1
5	CAN4TX	CAN4TX	P06_11
7	CAN4RX	CAN4RX	P06_12
9	LIN2TX	RLIN32TX	P06_0
11	LIN2RX	RLIN32RX	P06_1
13	LIN4TX	RLIN34TX	P06_11
15	LIN4RX	RLIN34RX	P06_10
17	LIN6TX	RLIN36TX	P04_15
19	LIN6RX	RLIN36RX	P04_14
21	LIN8TX	RLIN38TX	P02_1
23	LIN8RX	RLIN38RX	P02_0
25	LIN10TX	RLIN310TX	P24_4
27	LIN10RX	RLIN310RX	P24_5
29	LIN12TX	RLIN312TX *1	P04_6
31	LIN12RX	RLIN312RX *1	P04_5
33	LIN14TX	P24_9 *2 *4 RLIN314TX *1 *3	P24_9 *2 *4 B2_P24_7 *3
35	LIN14RX	RLIN314RX *1	R_P24_8 *2 B2_P24_8 *3
37	–	–	–
39	CAN12TX	–	–
41	CAN12RX	–	–
43	CAN14TX	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
2	CAN3TX	CAN3TX	P10_7
4	CAN3RX	CAN3RX	P10_6
6	CAN5TX	CAN5TX	P02_7
8	CAN5RX	CAN5RX	P02_8
10	LIN3TX	RLIN33TX	P06_3
12	LIN3RX	RLIN33RX	P06_2
14	LIN5TX	RLIN35TX	P24_12
16	LIN5RX	RLIN35RX	P24_11
18	LIN7TX	RLIN37TX	P04_12
20	LIN7RX	RLIN37RX	P04_13
22	LIN9TX	RLIN39TX	P02_6
24	LIN9RX	RLIN39RX	P02_5
26	LIN11TX	RLIN311TX *1	R_P22_1
28	LIN11RX	RLIN311RX *1	R_P22_0
30	LIN13TX	RLIN313TX *1	P02_4
32	LIN13RX	RLIN313RX *1	P02_3
34	LIN15TX	–	–
36	LIN15RX	–	–
38	–	–	–
40	CAN13TX	–	–
42	CAN13RX	–	–
44	CAN15TX	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
45	CAN14RX	–	–
47	CAN6TX	–	–
49	CAN6RX	–	–
51	CAN8TX	–	–
53	CAN8RX	–	–
55	CAN10TX	–	–
57	CAN10RX	–	–
59	–	–	–
61	LIN16TX	–	–
63	LIN16RX	–	–
65	LIN18TX	–	–
67	LIN18RX	–	–
69	LIN20TX	–	–
71	LIN20RX	–	–
73	LIN22TX	–	–
75	LIN22RX	–	–
77	–	–	–
79	SFMA0CLK	SFMA0CLK	P17_5
81	SFMA0IO0	SFMA0IO0	R_P17_3 *2 B2_P17_3 *3
83	SFMA0IO2	SFMA0IO2	P17_1
85	–	–	–
87	MMCA0CLK	MMCA0CLK *1	R_P24_8 *2 B2_P24_8 *3
89	MMCA0DAT0	MMCA0DAT0 *1	P24_10
91	MMCA0DAT2	MMCA0DAT2 *1	P24_12
93	MMCA0DAT4	MMCA0DAT4 *1	P24_4
95	MMCA0DAT6	MMCA0DAT6 *1	P24_6
97	–	–	–
99	ETH1MDIO	ETS0_MDIO *1	P21_0
101	ETH1RXD0	ETS0_RMII_RXD0 *1	P10_4
103	ETH1RXD1	ETS0_RMII_RXD1 *1	P10_5
105	ETH1RXD2	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
46	CAN15RX	–	–
48	CAN7TX	–	–
50	CAN7RX	–	–
52	CAN9TX	–	–
54	CAN9RX	–	–
56	CAN11TX	–	–
58	CAN11RX	–	–
60	–	–	–
62	LIN17TX	–	–
64	LIN17RX	–	–
66	LIN19TX	–	–
68	LIN19RX	–	–
70	LIN21TX	–	–
72	LIN21RX	–	–
74	LIN23TX	RLIN323TX	P06_9
76	LIN23RX	RLIN323RX	P06_8
78	–	–	–
80	SFMA0SSL	SFMA0SSL	P17_4
82	SFMA0IO1	SFMA0IO1	R_P17_2 *2 B2_P17_2 *3
84	SFMA0IO3	SFMA0IO3	P17_0
86	–	–	–
88	MMCA0CMD	MMCA0CMD *1	P24_9
90	MMCA0DAT1	MMCA0DAT1 *1	P24_11
92	MMCA0DAT3	MMCA0DAT3 *1	R_P24_7 *2 B2_P24_7 *3
94	MMCA0DAT5	MMCA0DAT5 *1	P24_5
96	MMCA0DAT7	MMCA0DAT7 *1	P24_13
98	–	–	–
100	ETH1MDC	ETS0_MDC *1	P20_11
102	ETH1TXD0	ETS0_RMII_TXD0 *1	P20_8
104	ETH1TXD1	ETS0_RMII_TXD1 *1	P20_7
106	ETH1TXD2	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
107	ETH1RXD3	–	–
109	ETH1RXCLK	–	–
111	ETH1RXER	–	–
113	ETH1CRSDV	ETS0_RMII_CRSDV *1	P10_10
115	ETH1RXDV	–	–
117	ETH1RESET	P17_1	P17_1
119	–	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
108	ETH1TXD3	–	–
110	ETH1TXCLK	ETS0_RMII_REFCLK *1	B1_P20_3
112	ETH1TXER	–	–
114	ETH1TXEN	ETS0_RMII_TXEN *1	P10_0
116	ETH1COL	–	–
118	ETH1LINK	–	–
120	–	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Only RH850/U2C4
*2 Board revision D020562_06_V0100
*3 Board revision D020562_06_V0200
*4 See precaution in chapter 9.2 LIN14 Connection on Main Board Connector CN2.

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function on		Device port
	Main Board	Piggyback	
1	CSI0CS0	MSPI0CSS0	P06_9
3	CSI0CS1	MSPI0CSS1	P06_8
5	CSI0CS2	MSPI0CSS6	P06_11
7	CSI0CS3	MSPI0CSS7	P06_10
9	–	–	–
11	I2S0TXD	–	–
13	I2S0RXD	–	–
15	I2S0BCLK	–	–
17	I2S0LRCLK	–	–
19	I2S0MCLK	SSIFACK	B2_P20_0
21	CSI1CS2	MSPI1CSS5	P04_5
23	–	–	–
25	–	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
2	CSI0CLK	MSPI0SC	P06_6
4	CSI0SI	MSPI0SI	P06_5
6	CSI0SO	MSPI0SO	P06_7
8	–	–	–
10	CSI1CS1	MSPI1CSS2	P02_6
12	I2S1TXD	SSIF1TXD	R_P17_3 *1 B2_P17_3 *2
14	I2S1RXD	SSIF1RXD	R_P17_2 *1 B2_P17_2 *2
16	I2S1BCLK	SSIF1BCK	P17_4
18	I2S1LRCLK	SSIF1LRCK	P17_5
20	–	–	–
22	CSI1CS3	MSPI1CSS6	P04_6
24	CSI1CS0	MSPI1CSS0	P02_2
26	DIGIO_24	MSPI1CSS4	P04_4

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
27	–	–	–
29	CSI1SCLK	MSPI1SC	P02_3
31	–	–	–
33	MOT0ADU	ADCKAI0	AP0_0
35	MOT0ADV	ADCKAI1	AP0_1
37	MOT0ADW	ADCKAI2	AP0_2
39	MOT0RDCS1	ADCKAI3	AP0_3
41	MOT0RDCS3	ADCKAI4	AP0_4
43	MOT0RDCS2	ADCKAI5	AP0_5
45	MOT0RDCS4	ADCKAI6	AP0_6
47	MOT0RDCCOM	ADCKAI7	AP0_7
49	MOT0RDCRSO	ADCKAI8	AP0_8
51	–	–	–
53	–	–	–
55	AD1_0	ADCKAI9	AP0_9
57	AD1_2	ADCKAI11	AP0_11
59	AD1_4	–	–
61	AD1_6	–	–
63	PWM0	PWGC32O	P02_0
65	PWM2	PWGC41O	P02_2
67	PWM4	PWGC43O	P02_4
69	PWM6	PWGC45O	P02_6
71	DIGIO16	P06_0	P06_0
73	DIGIO18	P04_7	P04_7
75	DIGIO20	P04_6	P04_6
77	DIGIO22	P24_9	P24_9
79	ENC0	ENCA0E0	P02_9
81	MOT0ERR	–	–
83	MOT0U_P	TSG30O1	P17_0
85	MOT0U_N	TSG30O2	P17_1
87	MOT0V_P	TSG30O3	R_P17_2 *1 B2_P17_2 *2
89	MOT0V_N	TSG30O4	R_P17_3 *1 B2_P17_3 *2
91	MOT0W_P	TSG30O5	P17_4

Pin	Function on		Device port
	Main Board	Piggyback	
28	CSI1SO	MSPI1SO	P02_5
30	CSI1SI	MSPI1SI	P02_4
32	–	–	–
34	MOT1ADU	ADCK1I0	AP2_0
36	MOT1ADV	ADCK1I1	AP2_1
38	MOT1ADW	ADCK1I2	AP2_2
40	MOT1RDCS1	ADCK1I3	AP2_3
42	MOT1RDCS3	ADCK1I4	AP2_4
44	MOT1RDCS2	ADCK1I5	AP2_5
46	MOT1RDCS4	ADCK1I6	AP2_6
48	MOT1RDCCOM	ADCK1I7	AP2_7
50	MOT1RDCRSO	ADCK1I8	AP2_8
52	–	–	–
54	–	–	–
56	AD1_1	ADCKAI10	AP0_10
58	AD1_3	–	–
60	AD1_5	–	–
62	AD1_7	–	–
64	PWM1	PWGC33O	P02_1
66	PWM3	PWGC42O	P02_3
68	PWM5	PWGC44O	P02_5
70	PWM7	PWGC50O	P02_7
72	DIGIO17	P22_2	P22_2
74	DIGIO19	P04_5	P04_5
76	DIGIO21	P17_6	P17_6
78	DIGIO23	P24_10	P24_10
80	ENC1	ENCA0E1	P06_0
82	MOT1ERR	TAPA0ESO	P06_6
84	MOT1U_P	TAPA0UP	P06_1
86	MOT1U_N	TAPA0UN	P06_0
88	MOT1V_P	TAPA0VP	P06_5
90	MOT1V_N	TAPA0VN	P06_4
92	MOT1W_P	TAPA0WP	P06_3

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
93	MOT0W_N	TSG30O6	P17_5
95	–	–	–
97	–	–	–
99	–	–	–
101	GND	–	–
103	AD2_0	ADCK1I9	AP2_9
105	AD2_1	ADCK1I10	AP2_10
107	AD2_2	ADCK1I11	AP2_11
109	AD2_3	ADCK1I12	AP2_12
111	AD2_4	ADCK1I13	AP2_13
113	AD2_5	ADCK1I14	AP2_14
115	AD2_6	ADCK1I15	AP2_15
117	AD2_7	–	–
119	GND	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
94	MOT1W_N	TAPA0WN	P06_2
96	–	–	–
98	–	–	–
100	ETH0_SO_P	–	–
102	ETH0_SO_N	–	–
104	–	–	–
106	ETH0_SI_P	–	–
108	ETH0_SI_N	–	–
110	–	–	–
112	ETH1_SO_P	–	–
114	ETH1_SO_N	–	–
116	–	–	–
118	ETH1_SI_P	–	–
120	ETH1_SI_N	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Board revision D020562_06_V0100

*2 Board revision D020562_06_V0200

7.2 Debug Connector CN9

Table 7.4 On-chip debug connector CN9

Pin	Function	Device port
1	TCK / LPDCLK / FPCK	JP0_2
3	TRST	TRST#_TOOL
5	TDO / LPDO / FPDT	JP0_1
7	TDI / LPDI / FPDR	JP0_0
9	TMS	JP0_3
11	RDY / LPDCLKO	JP0_5
13	RESET	RESET#

Pin	Function	Device port
2	GND	GND
4	FPMD0	FLMD0_TOOL
6	FPMD1	–
8	TVDD	E0VCC
10	EVTO	EVTO0#_TOOL
12	GND	GND
14	GND	GND

7.3 Device Ports Connectors CN4, CN10, CN13 and CN14

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.3.1 Device Ports Connector CN4

Table 7.5 Device ports connector CN4

Connector pin	Device pin	Device port
1	1	P10_0
3	3	P10_2
5	5	P10_4
7	7	P10_6
9	9	P10_10
11	11	E1VCC
13	13	R_P17_2 *1 P17_2 *2
15	15	P17_4
17	17	VDD
19	19	AP2_15
21	21	AP2_13
23	23	AP2_11
25	25	AP2_9
27	27	AP2_7
29	29	AP2_5
31	31	AP2_3
33	33	AP2_1
35	35	A1VREFH

Connector pin	Device pin	Device port
2	2	P10_1
4	4	P10_3
6	6	P10_5
8	8	P10_7
10	10	P17_0
12	12	P17_1
14	14	R_P17_3 *1 P17_3 *2
16	16	P17_5
18	18	P17_6
20	20	AP2_14
22	22	AP2_12
24	24	AP2_10
26	26	AP2_8
28	28	AP2_6
30	30	AP2_4
32	32	AP2_2
34	34	AP2_0
36	36	GND

*1 Board revision D020562_06_V0100

*2 Board revision D020562_06_V0200

7.3.2 Device Ports Connector CN10

Table 7.6 Device ports connector CN10

Connector pin	Device pin	Device port
1	37	AAVREFH
3	39	AP0_0
5	41	AP0_2
7	43	AP0_4

Connector pin	Device pin	Device port
2	38	GND
4	40	AP0_1
6	42	AP0_3
8	44	AP0_5

Table 7.6 Device ports connector CN10 (cont'd)

Connector pin	Device pin	Device port	Connector pin	Device pin	Device port
9	45	AP0_6	10	46	AP0_7
11	47	AP0_8	12	48	AP0_9
13	49	AP0_10	14	50	AP0_11
15	51	P06_13	16	42	P06_12
17	53	P06_11	18	54	P06_10
19	55	P06_9	20	56	P06_8
21	57	P06_7	22	58	P06_6
23	59	P06_5	24	60	VCC
25	61	P06_4	26	62	P06_3
27	63	P06_2	28	64	P06_1
29	65	E0VCC	30	66	P06_0
31	67	V_PIN67	32	68	P04_12
33	69	P04_13	34	70	P04_14
35	71	P04_15	36	72	P04_11

7.3.3 Device Ports Connector CN13

Table 7.7 Device ports connector CN13

Connector pin	Device pin	Device port	Connector pin	Device pin	Device port
1	73	P04_7	2	74	P04_6
3	75	P04_5	4	76	P04_4
5	77	P02_9	6	78	P02_8
7	79	P02_7	8	80	P02_6
9	81	P02_5	10	82	P02_4
11	83	P02_3	12	84	E0VCC
13	85	RESETOUT#	14	86	VDD_F
15	87	P02_1	16	88	P02_0
17	89	P02_2	18	90	JP0_5
19	91	JP0_3	20	92	JP0_2
21	93	JP0_1	22	94	JP0_0
23	95	TRST#	24	96	RESET#
25	97	–	26	98	VDD_F
27	99	X2_CN	28	100	GND
29	101	X1_CN	30	102	SYSVCC
31	103	AWOVCL	32	104	XT2_CN
33	105	XT1_CN	34	106	FLMD0

Table 7.7 Device ports connector CN13 (cont'd)

Connector pin	Device pin	Device port
35	107	–
36	108	ERROROUT_M#

7.3.4 Device Ports Connector CN14

Table 7.8 Device ports connector CN14

Connector pin	Device pin	Device port
1	109	P24_13
3	111	E1VCC
5	113	P24_10
7	115	R_P24_8 *1 P24_8 *2
9	117	P24_6
11	119	P24_4
13	121	R_P22_1
15	123	P22_3
17	125	VDD_F
19	127	R_P21_3
21	129	P21_1
23	131	P20_13
25	133	E1VCC
27	135	P20_11
29	137	R_P20_9
31	139	P20_7
33	141	P20_3
35	143	P20_1
2	110	P24_12
4	112	P24_11
6	114	P24_9
8	116	R_P24_7 *1 P24_7 *2
10	118	P24_5
12	120	R_P22_0
14	122	P22_2
16	124	R_P20_5
18	126	VCC
20	128	R_P21_2
22	130	P21_0
24	132	P20_12
26	134	P20_4
28	136	R_P20_10
30	138	P20_8
32	140	R_P20_6
34	142	P20_2
36	144	P20_0

*1 Board revision D020562_06_V0100

*2 Board revision D020562_06_V0200

7.4 Pull-Up/Pull-Down Pin Header CN12

Table 7.9 Pull-up and pull-down signal connector CN12

Pin	Function	Pin	Function
1	Level set by jumper JP15: JP15 [1-2]: 5.0 V (P5V0) JP15 [2-3]: 3.3 V (P3V3)	2	Fixed “L” level
3		4	
5		6	
7		8	
9	Level set by jumper JP14: JP14 [1-2]: 5.0 V (P5V0) JP14 [2-3]: 3.3 V (P3V3)	10	
11		12	
13		14	
15		16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *0*

Jumper Overview.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool is able to provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings

All of the following board configurations are based on these conditions:

- Normal device operation mode (JP7[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN5 (GND), CN6 (+5.0 V) and CN7 (+3.3 V) are assembled on the board.
- If also the core supply voltage of 1.09 V is supplied from an external power supply the connector CN8 (included in the package) has to be assembled on the pcb.

8.2.2 Jumper Indicators

The green jumper JP7 for FLMD0 must always be open for ‘normal’ (user mode and debug) operation of the device.

The yellow jumper JP19 is ONLY for board production test and has to stay open.

The red jumpers are related to the power supply configuration.
Following jumper symbols are used:

- : Jumper must not be set.
- 1 2 3: Jumper must be set in the indicated position
- 1 2 3: Jumper can be set to position [1-2] or position [2-3]
- 1 2 3: Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.2.3 Core Voltage Supply for eVR and DPS Devices

RH850/U2C4 devices are available with different core voltage supply:

- Devices with embedded voltage regulator (eVR device)
- Devices with external core voltage supply (DPS device)

RH850/U2C2 devices are available only as eVR devices with embedded voltage regulator.

The jumper configurations in the following chapters show separate jumper settings for eVR and DPS devices.

CAUTION

If the device being used is RH850/U2C with eVR core power supply (R7F702614, R7F702615 or R7F702616) JP3 must be open. If JP3 is set to either position the device may be damaged.

8.2.4 Stand-Alone Operation with Single External Power Supply 3.3 V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is generated using the on-board voltage regulator IC3. All I/O ports can only use 3.3 V.

Table 8.1 Power supply connectors for single power supply 3.3 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Not connected	Jumpers in JP1 (VCC and VREF selection) are set to 3.3 V position.
CN7	3.3 V	Connected, +3.3 V	
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]). DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP3[2-3] = SHORT). Refer to *3.3 Device Core Voltage (VDD)* Selection for further details about VDD voltage.

CAUTION

This setting cannot be used with RH850/U2C4 with eVR core power supply, VCC = 4.5 V – 5.5 V (R7F702616).

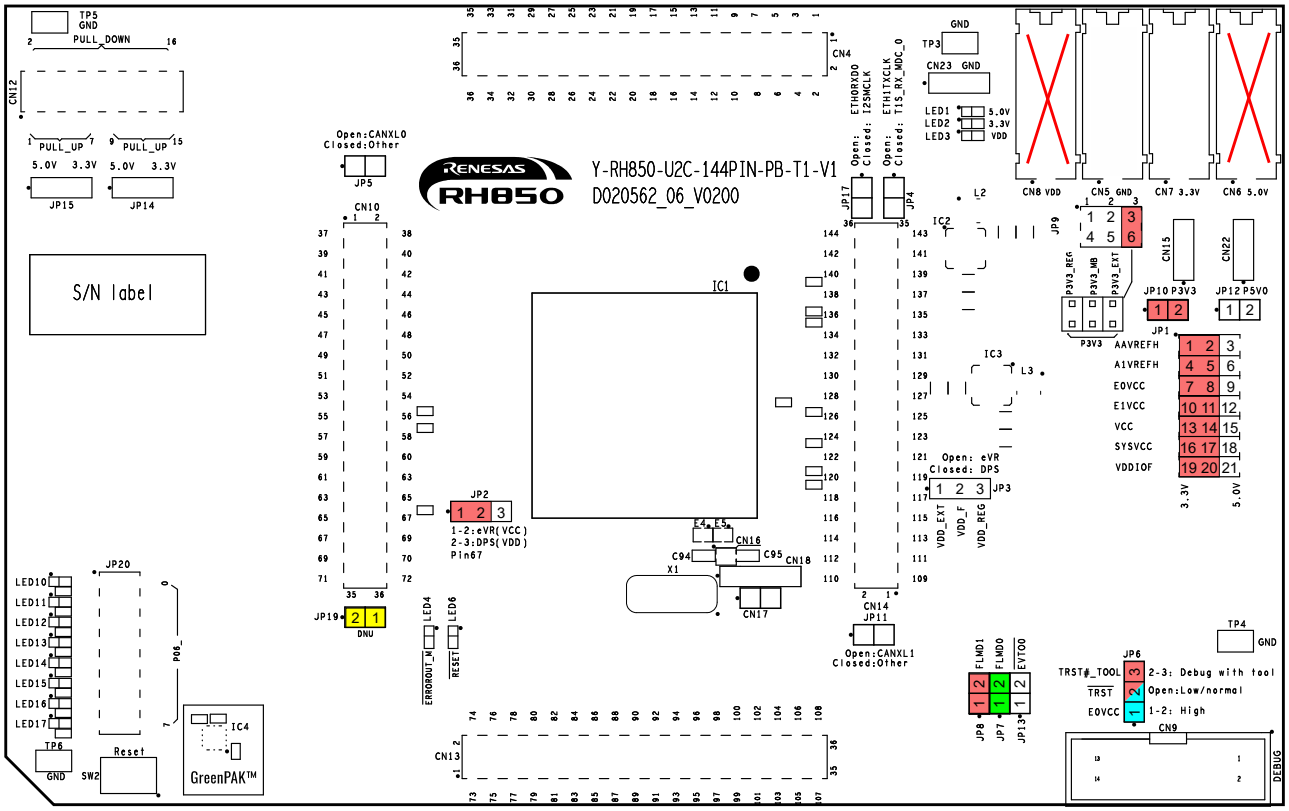


Figure 8.1 Stand-alone operation with 3.3 V external power supply for eVR device

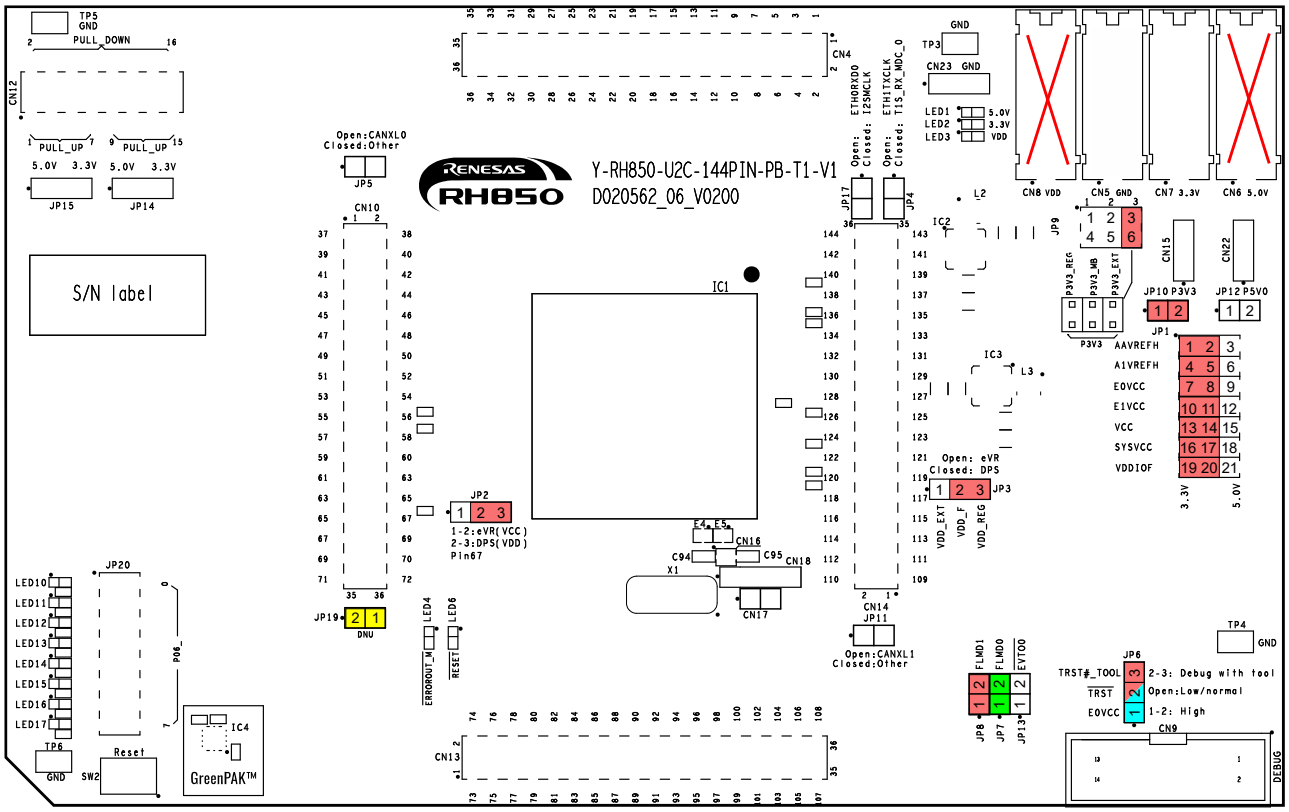


Figure 8.2 Stand-alone operation with 3.3 V external power supply for DPS device

8.2.5 Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can only use 5.0 V.

Table 8.2 Power supply connectors for single power supply 5.0 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	
CN7	3.3 V	Not connected	3.3 V supply (P3V3) from on-board voltage regulator IC2 (JP9[1-4] = SHORT).
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]). DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP3[2-3] = SHORT). Refer to *3.3 Device Core Voltage (VDD)* Selection for further details about VDD voltage.

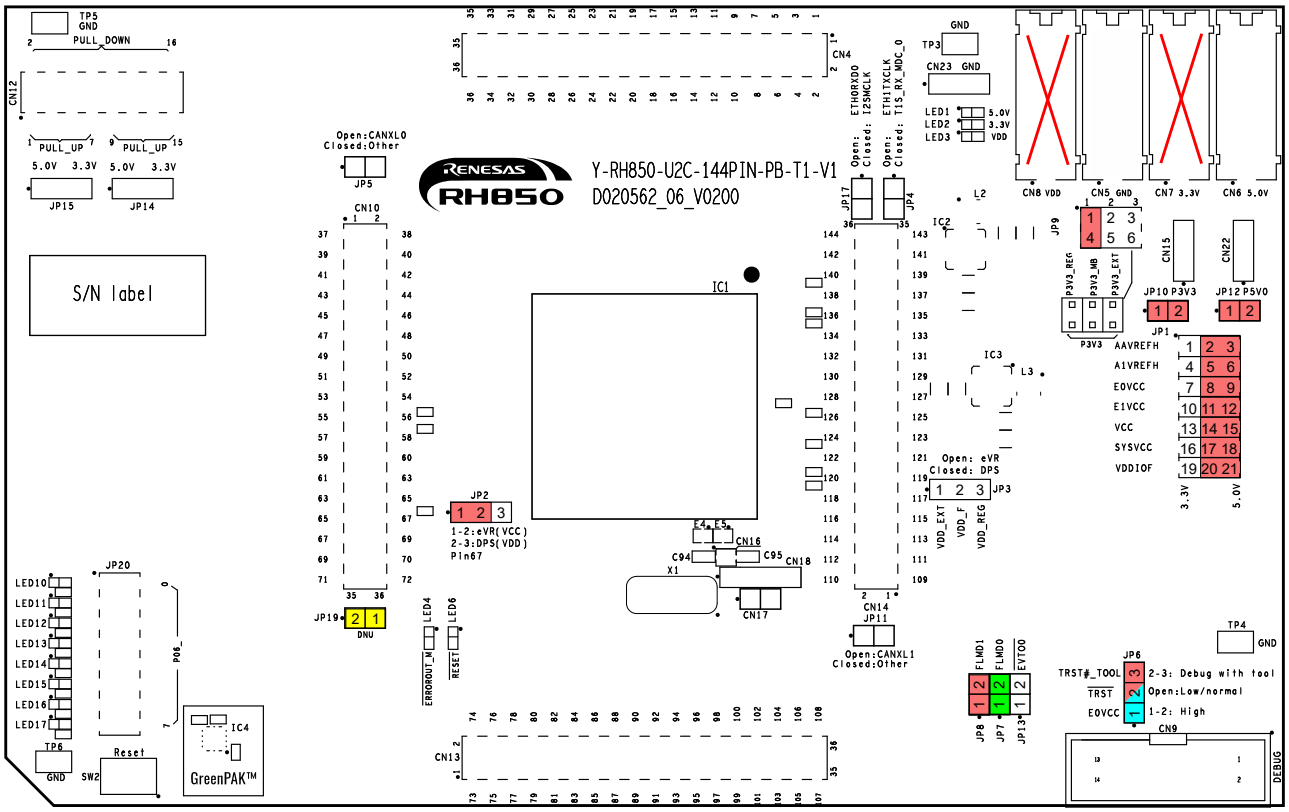


Figure 8.3 Stand-alone operation with 5.0 V external power supply for eVR device

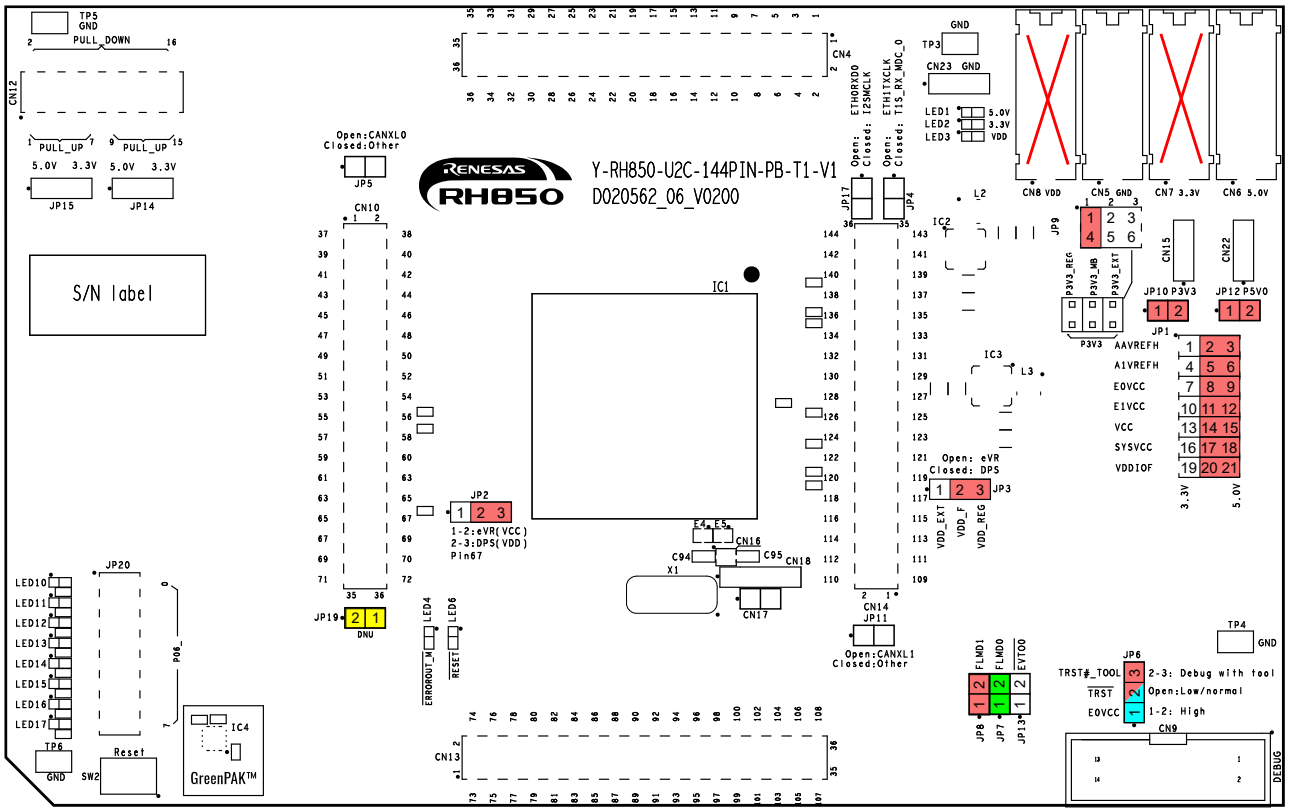


Figure 8.4 Stand-alone operation with 5.0 V external power supply for DPS device

8.2.6 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.3 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. JP9[3-6] = SHORT: use P3V3_ EXT supply for 3.3 V supply. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	eVR devices: Not connected DPS devices: Connected, 1.09 V	eVR device: VDD from internal voltage regulator (JP3[OPEN]) DPS device: VDD from external VDD supply (P1V09_EXT) (JP3[1-2] = SHORT) Refer to *3.3 Device Core Voltage (VDD)* Selection for further details about VDD voltage.

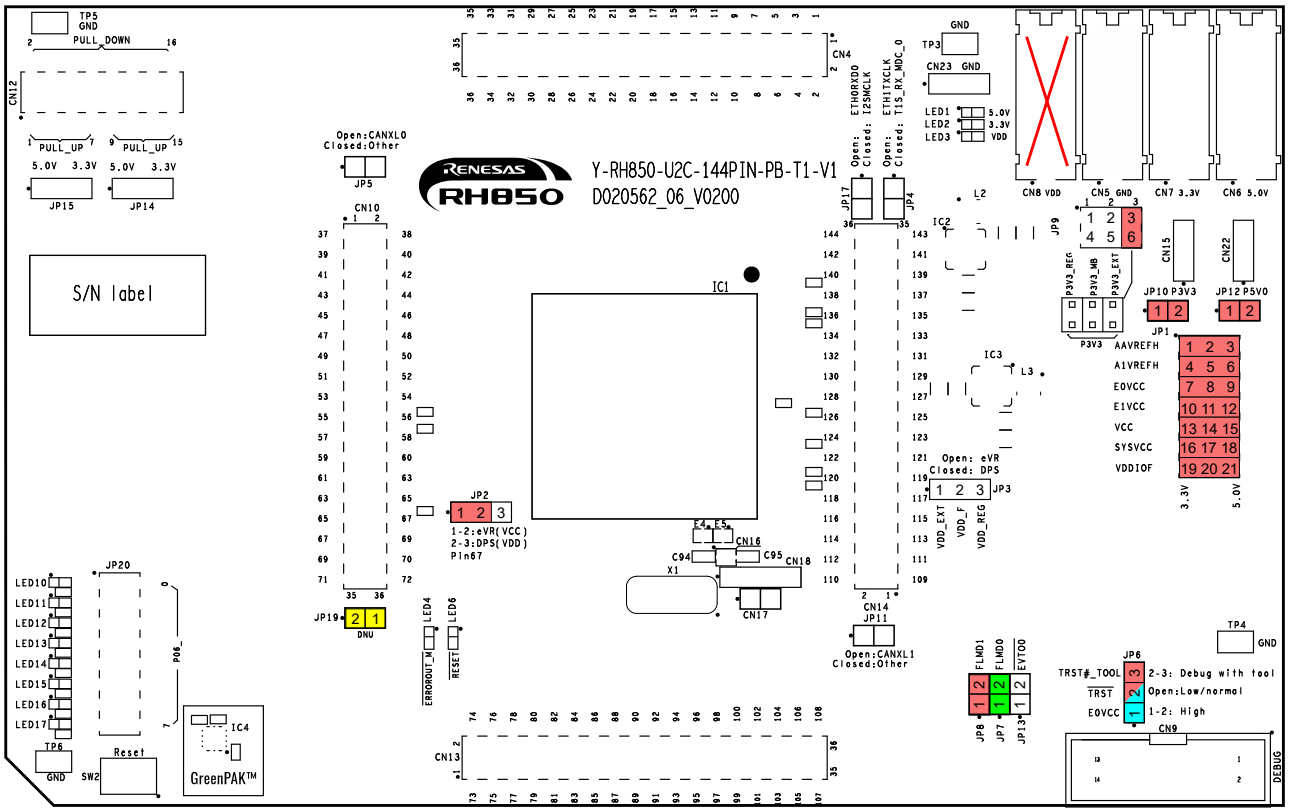


Figure 8.5 Stand-alone operation with all external power supplies for eVR device

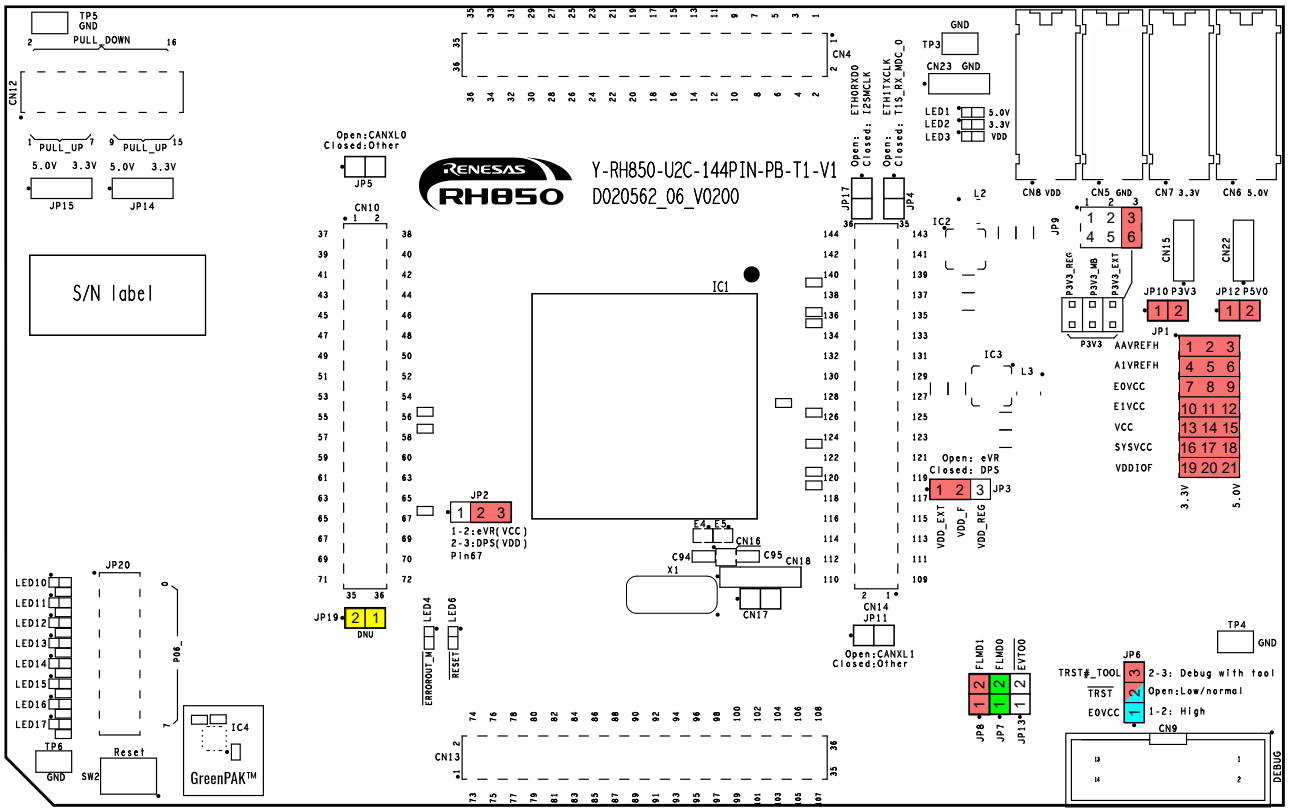


Figure 8.6 Stand-alone operation with all external power supplies for DPS device

8.2.7 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

The jumpers JP9 (P3V3) must be set to connect the main board supply voltage P3V3_MB to the piggyback board power supply rail P3V3.

The 5.0 V supply from the main board is always connected to the P5V0 power rail on the piggyback board.

Do not supply the 5.0 V (CN9) and 3.3 V (CN7) voltage directly to the piggyback board.

Table 8.4 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Not connected	
CN6	5.0 V	Not connected	The 5.0 V supply from the main board is connected to the P5V0 power rail on the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN7	3.3 V	Not connected	Use jumper JP9[2-5] to connect the 3.3 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP1.
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]) DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP3[2-3] = SHORT) Refer to *3.3 Device Core Voltage (VDD)* Selection for further details about VDD voltage.

Note

For DPS devices this configuration still allows to utilize an external P1V09_EXT voltage (connected to CN8) as the source for VDD voltage. When using external VDD make sure to set jumper JP3[1-2] = SHORT to use external VDD.

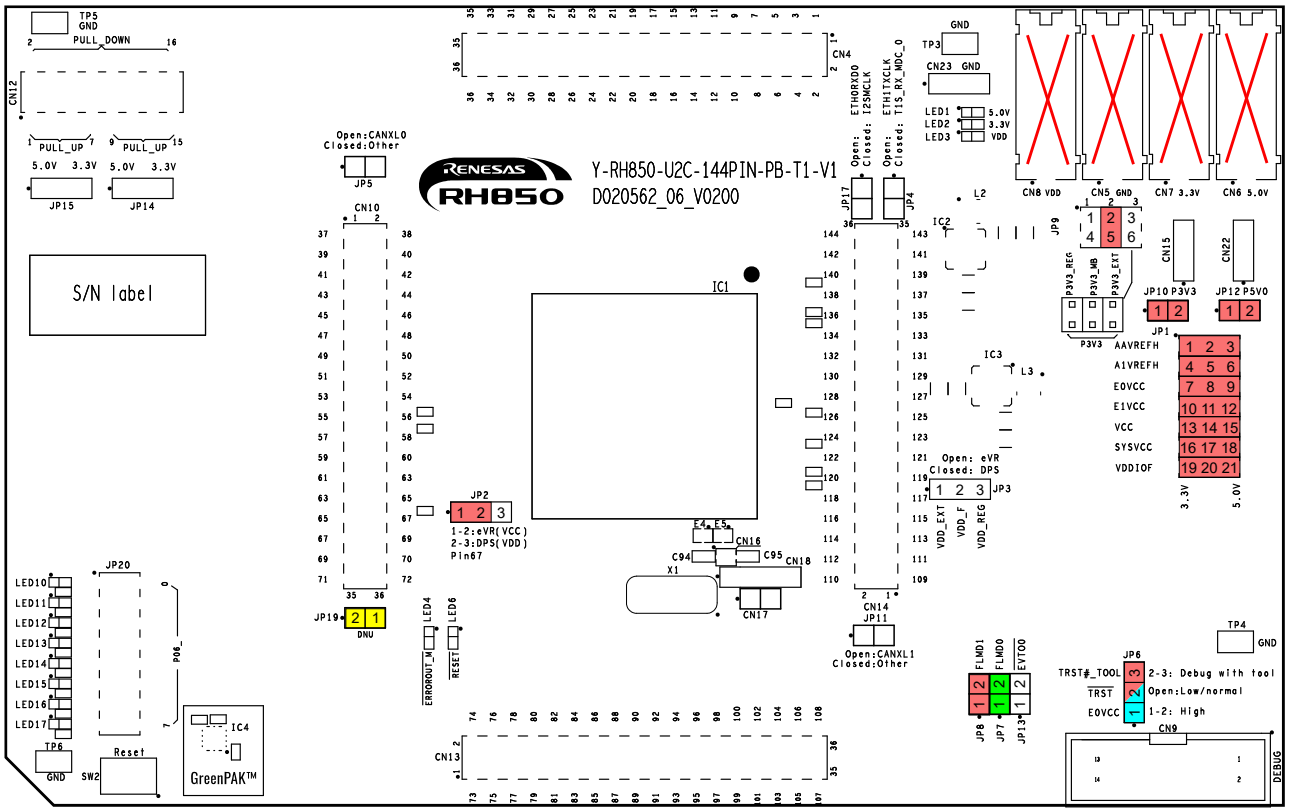


Figure 8.7 Main board operation without external power supply for eVR device

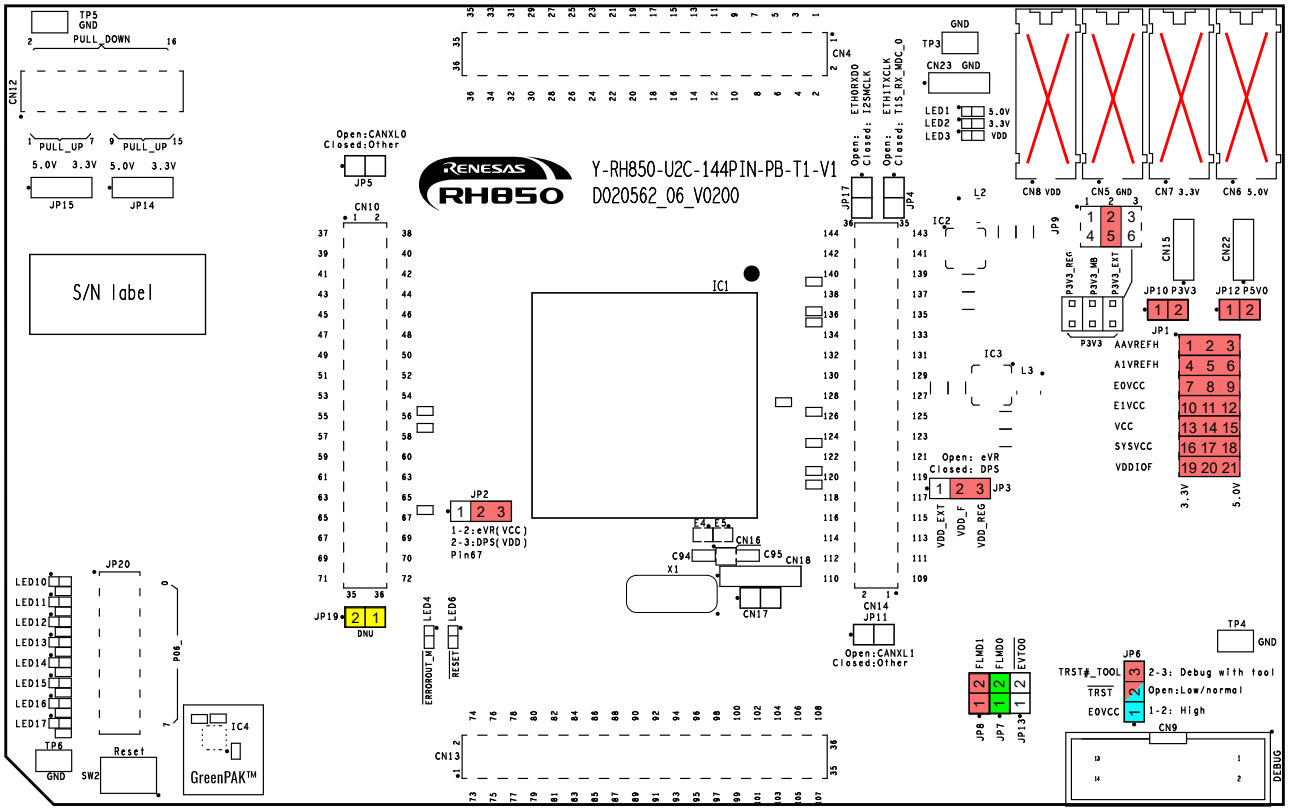


Figure 8.8 Main board operation without external power supply for DPS device

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW2 into '5-6 ON' position, so that RESET is permanently asserted. Alternatively keep SW2 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW2 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 System State and RESET.*

9.2 LIN14 Connection on Main Board Connector CN2

Affected boards: all boards with revision number D020562_06_V01.

Fixed boards: all boards from revision number D020562_06_V02 onwards.

The main board connector CN2 uses the pins 33 and 35 for connection of LIN14 on the main board. Unfortunately, the port connection for pin 33 for RH850/U2C is wrong.

Table 9.1 Connection for LIN14

Main Board Connector CN2		RH850/U2C			
		Board Version D020562_06_V01		Board Version D020562_06_V02	
Pin No.	Function	Port	Function	Port	Function
33	LIN14TX	P24_9	RLIN37TX	P24_7	RLIN314TX (RH850/U2C4) No LIN connection (RH850/U2C2)
35	LIN14RX	P24_8	RLIN314RX (RH850/U2C4) No LIN connection (RH850/U2C2)	P24_8	RLIN314RX (RH850/U2C4) No LIN connection (RH850/U2C2)

The correct connection for pin CN2_33 would be P24_7 of RH850/U2C. This would provide the function RLIN14TX for RH850/U2C4 devices and no LIN functionality for RH850/U2C2 devices.

If the common main board (Y-COMMON-MB-T1-V1) is being used with the RH850/U2C piggyback board it is possible to establish a manual connection from the LIN14 ports on RH850/U2C piggyback board to the LIN transceiver on the main board.

Table 9.2 says which pins to connect, Figure 1.1*Figure 9.1* shows where the pins are located on the boards.

Note

If the manual connection is used make sure the LIN14 port on the main board is **NOT** activated.

Table 9.2 Manual connection from piggyback board to main board

Signal	Piggyback Board Y-RH850-U2C-PB-T1-V1	Main Board Y-COMMON-MB-T1-V1
LIN14TX	CN14, pin 8	CN1_4, pin 5
LIN14RX	CN14, pin 7	CN1_4, pin 6

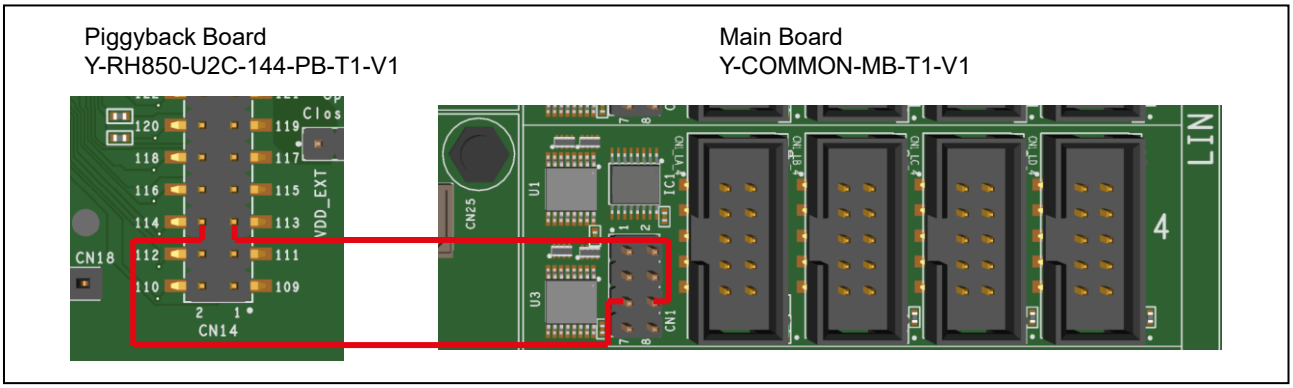


Figure 9.1 Manual connection of LIN14 interface

10. Mechanical Dimensions

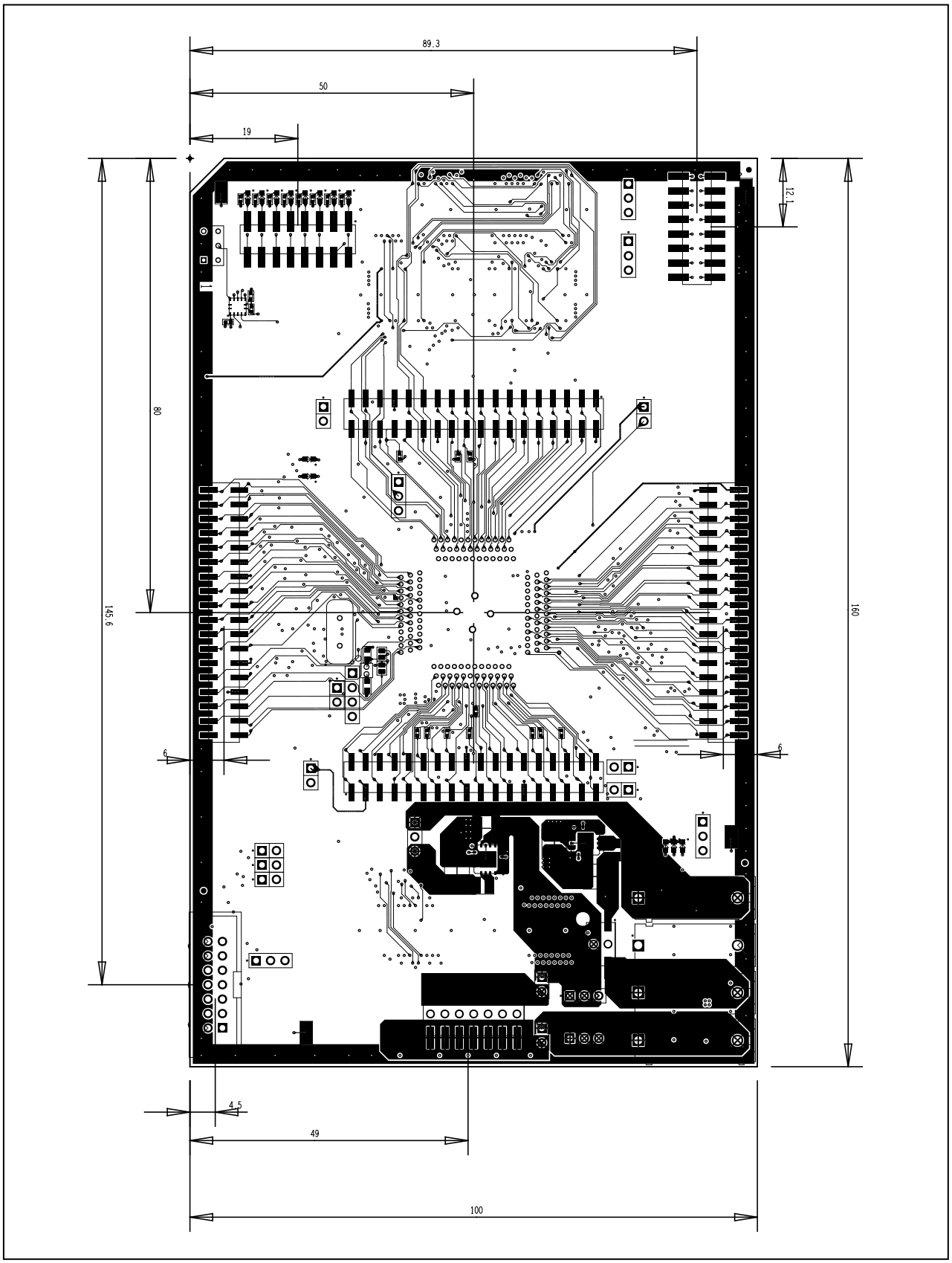


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C32, C37, C94, C95
- Oscillators: OSC1, X2
- Oscillator socket: CN16
- Filters: FC1

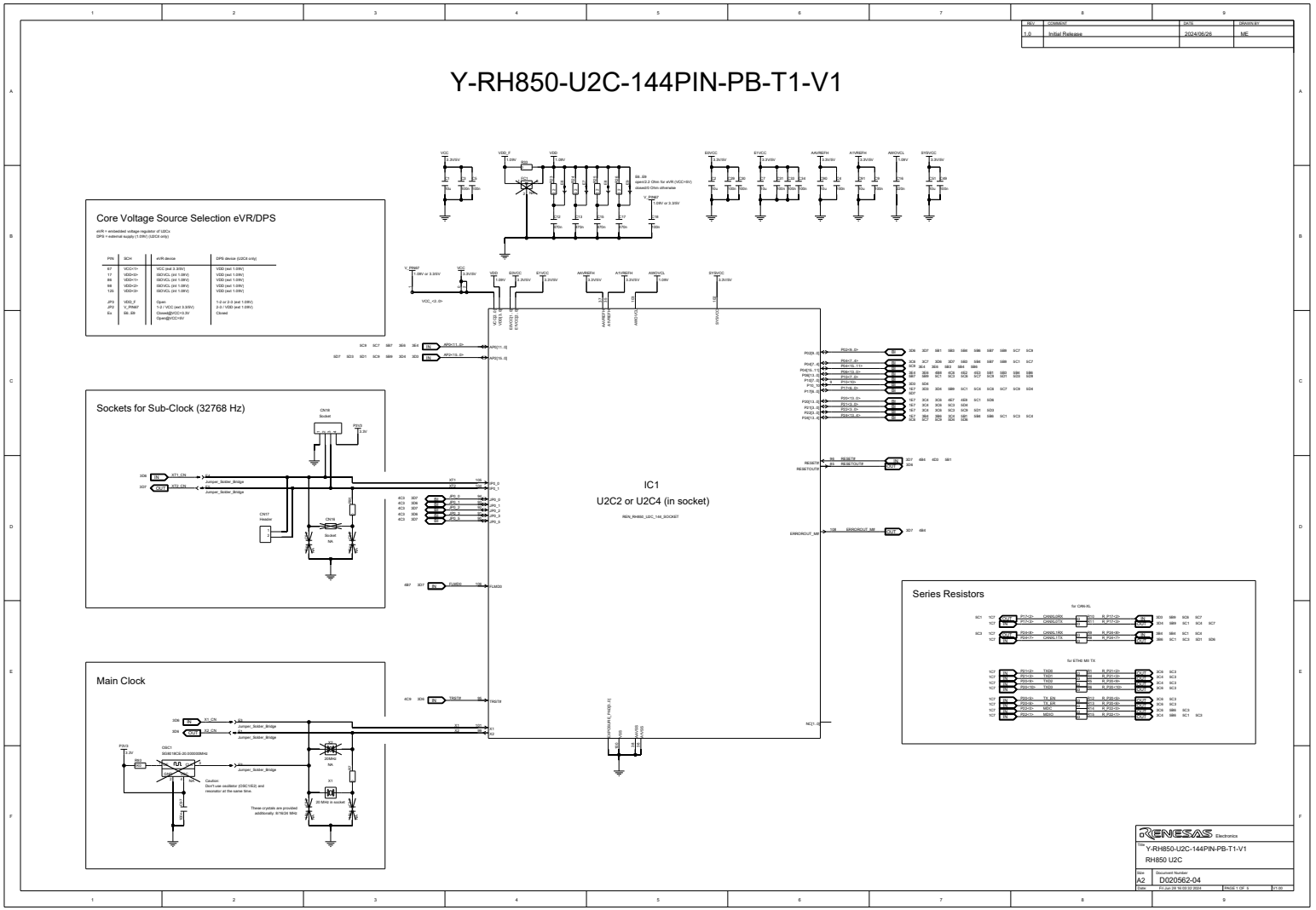
The above components are crossed out in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

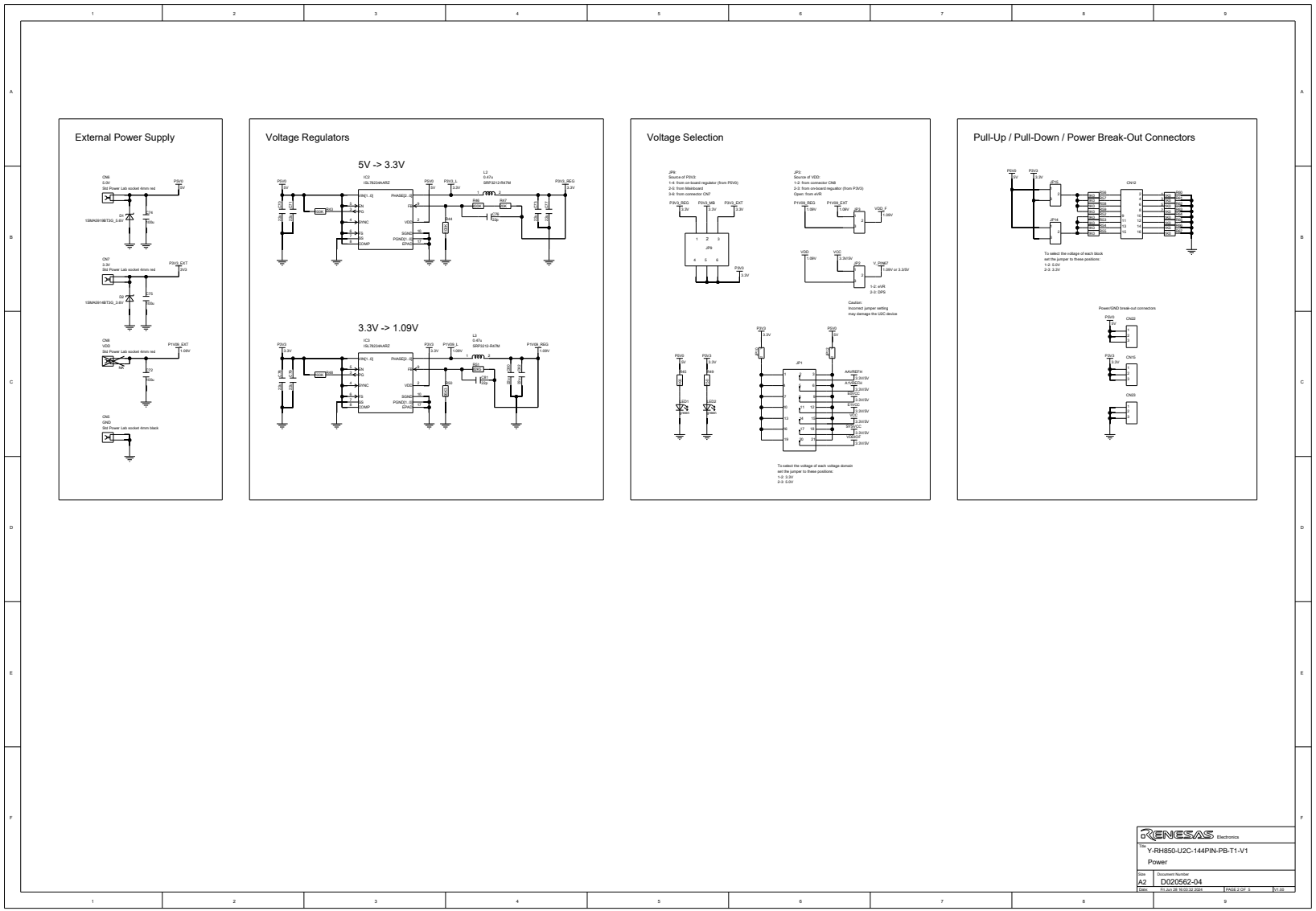
- 1 Hirschmann 4 mm power lab sockets, red for CN8
- Three resonators HC49 (8 / 16 / 24 MHz)
- 29 jumpers, 2.54 mm, black

11.1 Board Version D020562_06_V0100

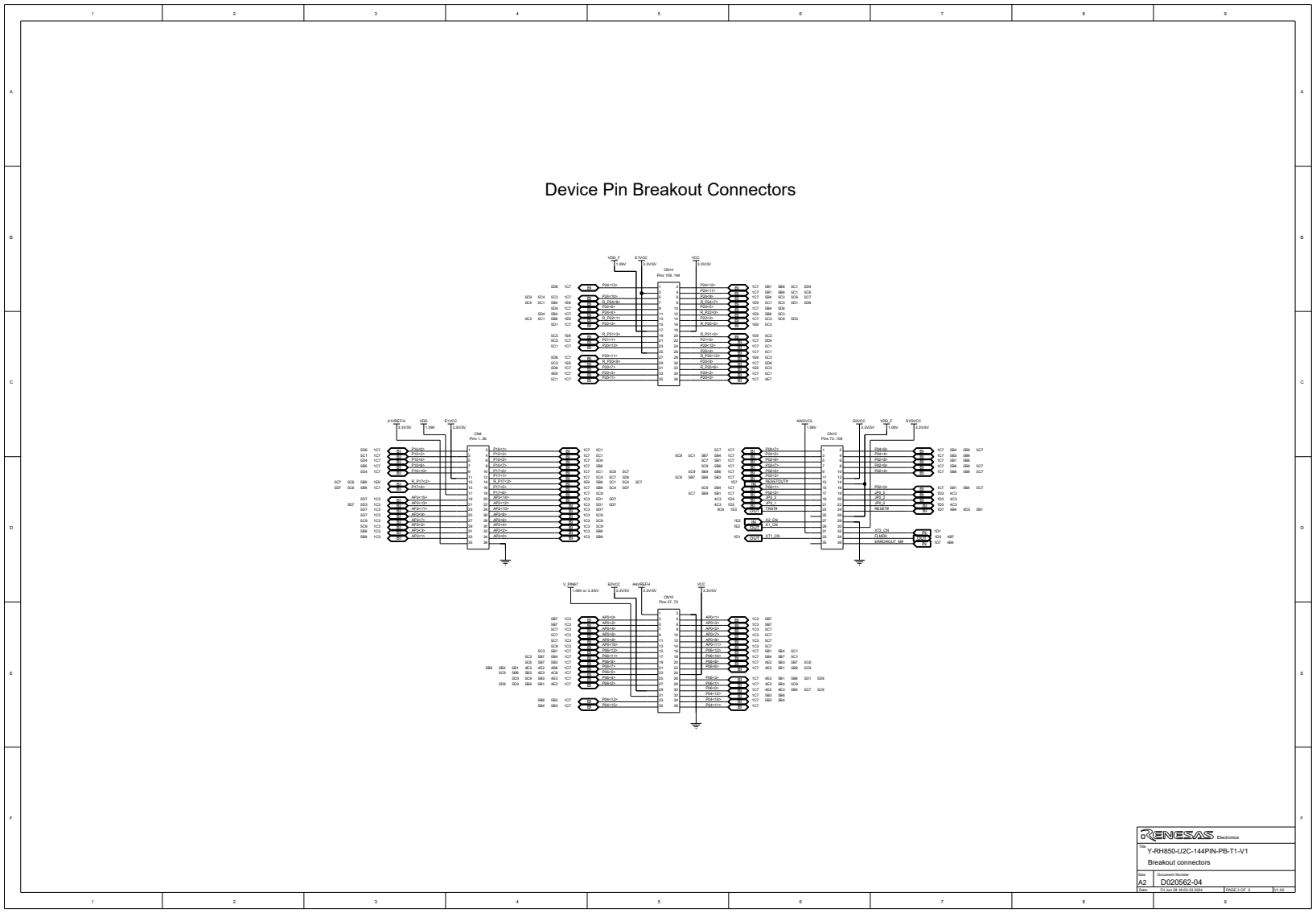
11.1.1 RH850/U2C



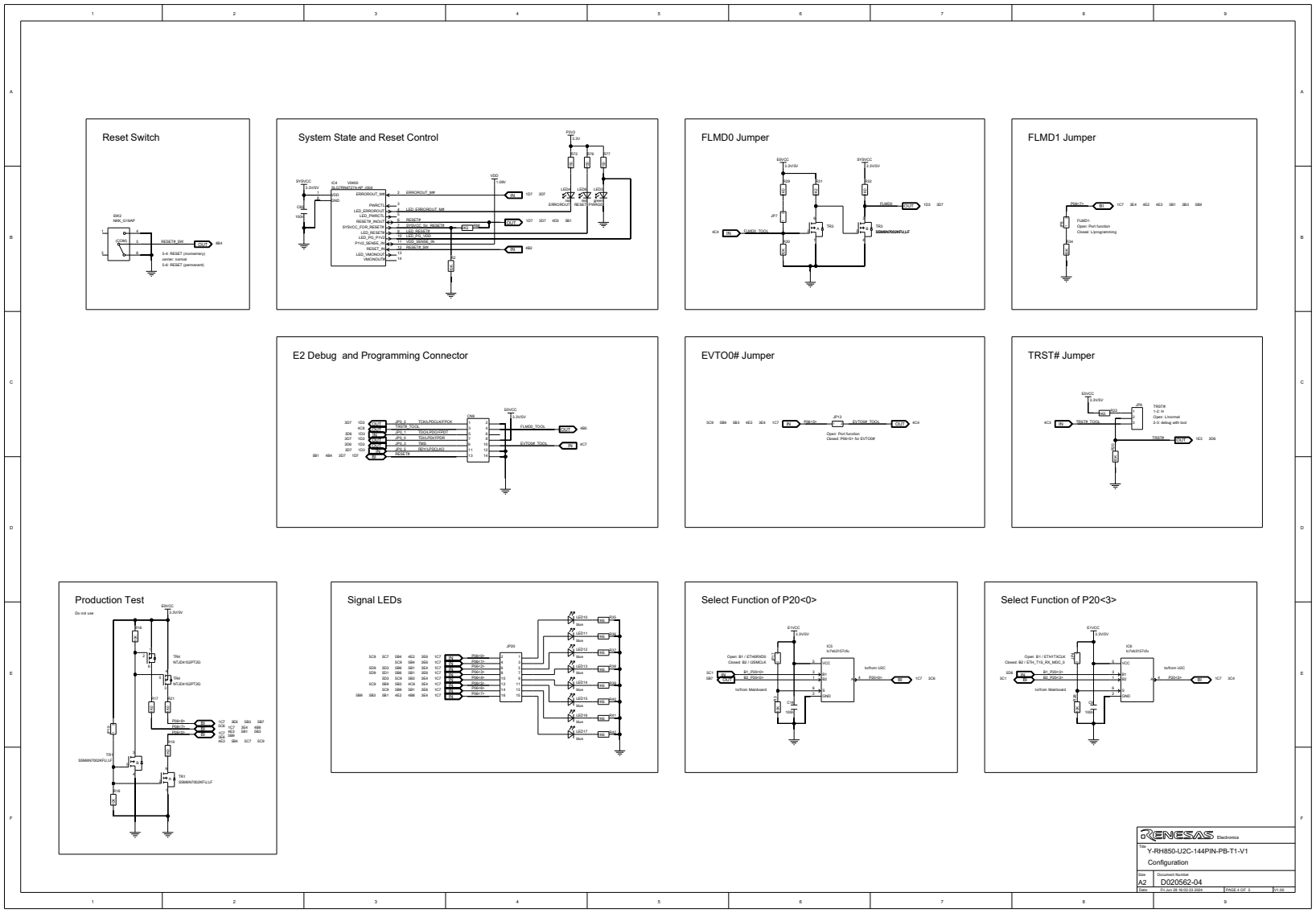
11.1.2 Power Supply



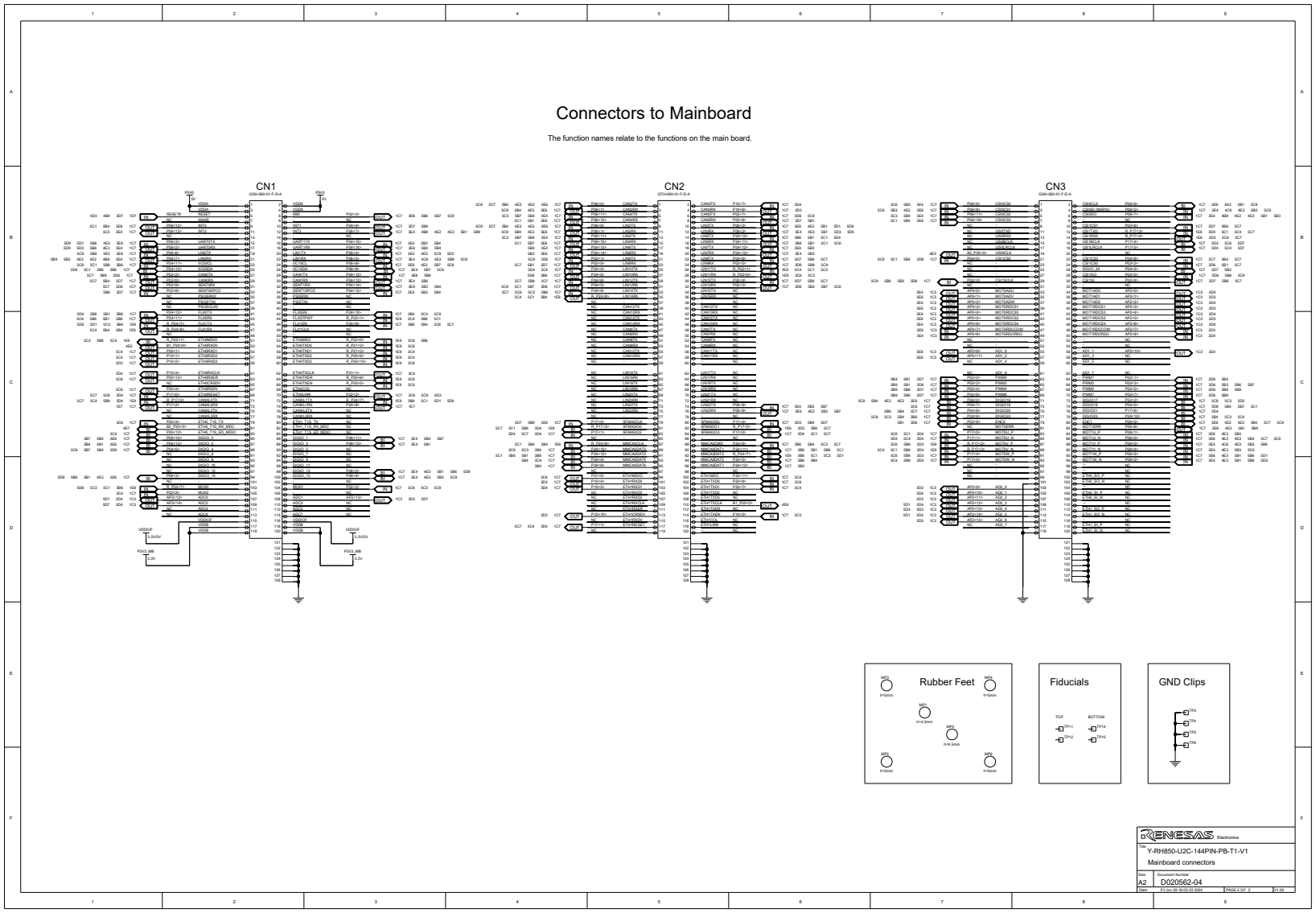
11.1.3 Breakout Connectors



11.1.4 Configuration

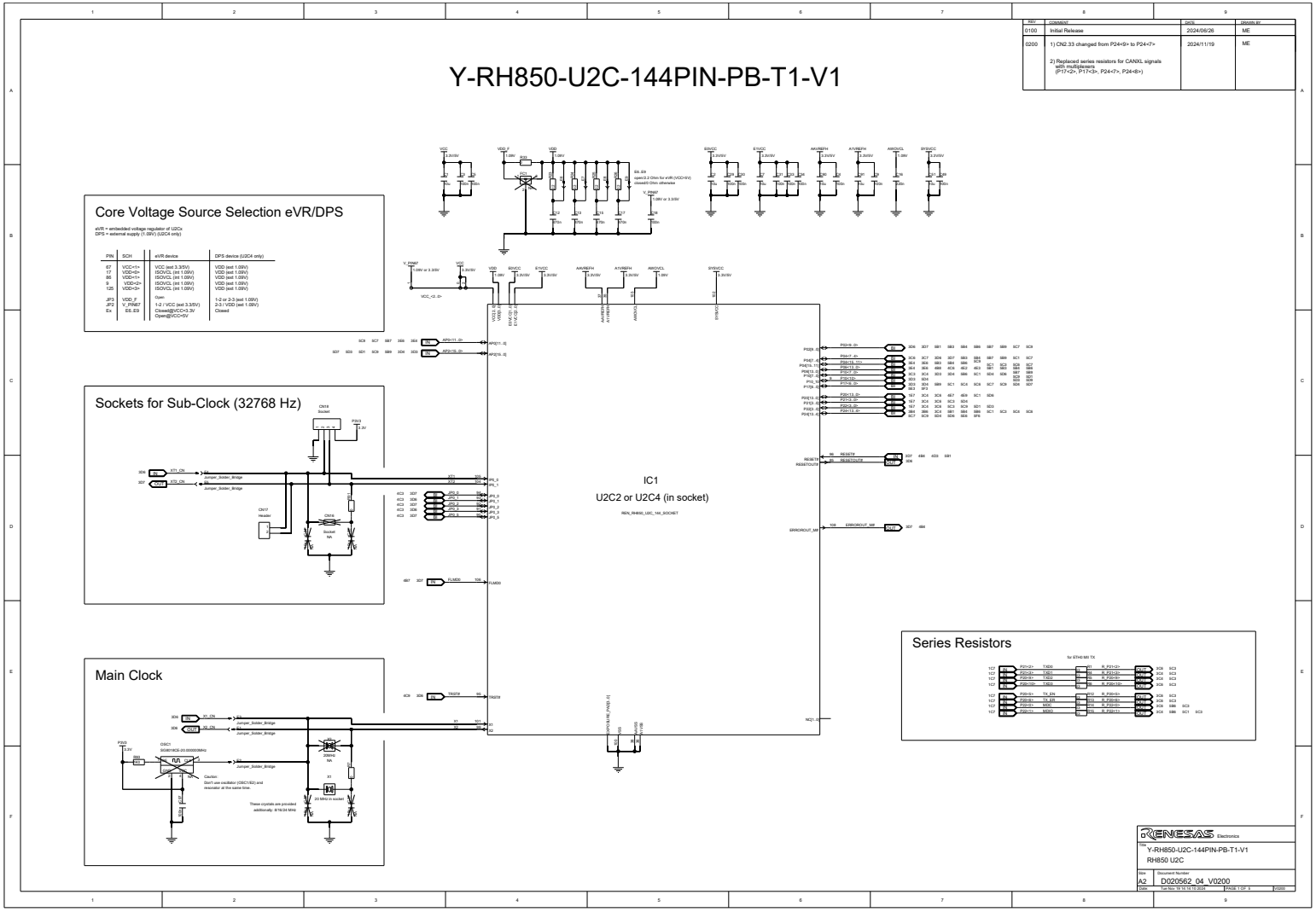


11.1.5 Main Board Connectors

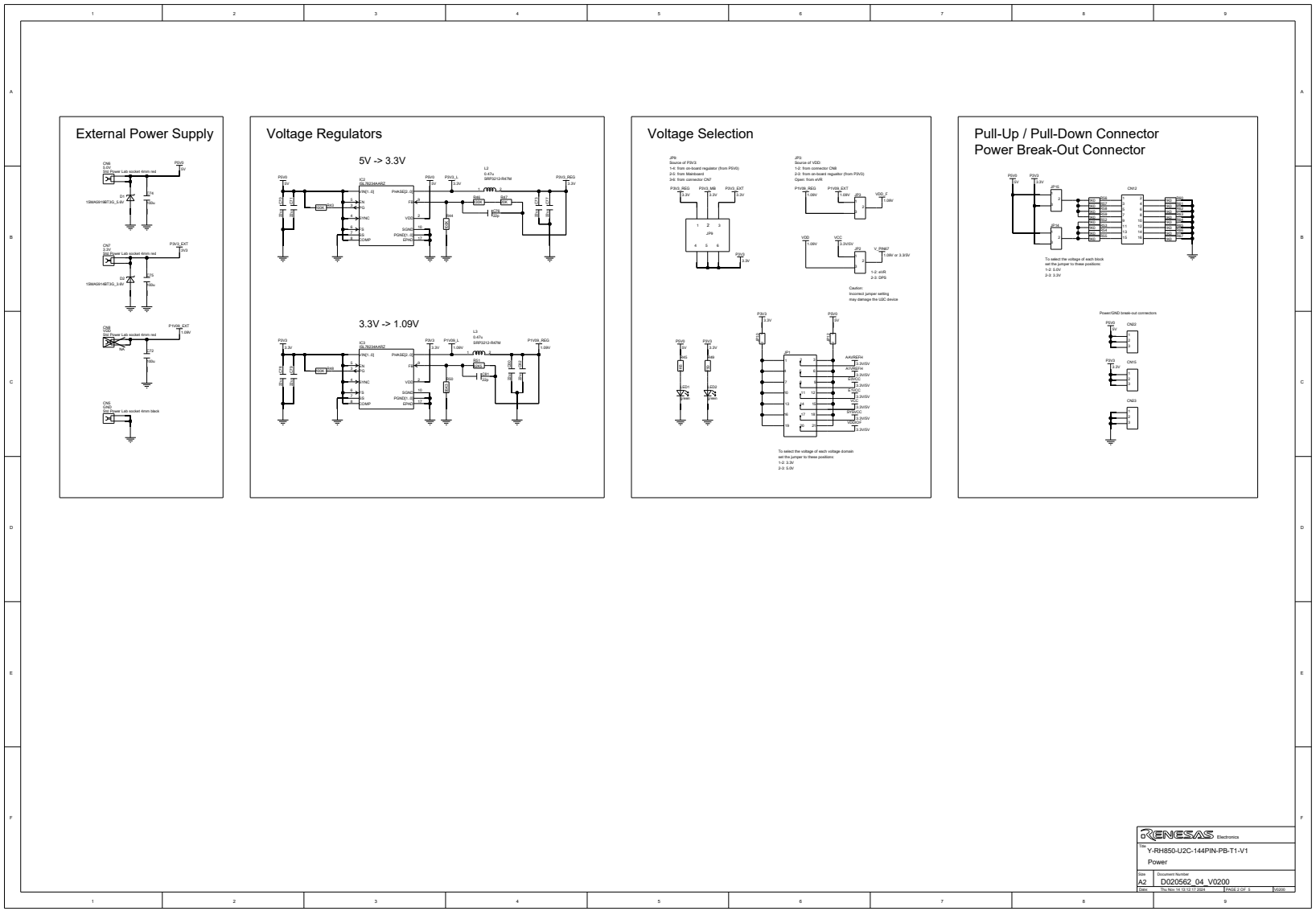


11.2 Board Version D020562_06_V0200

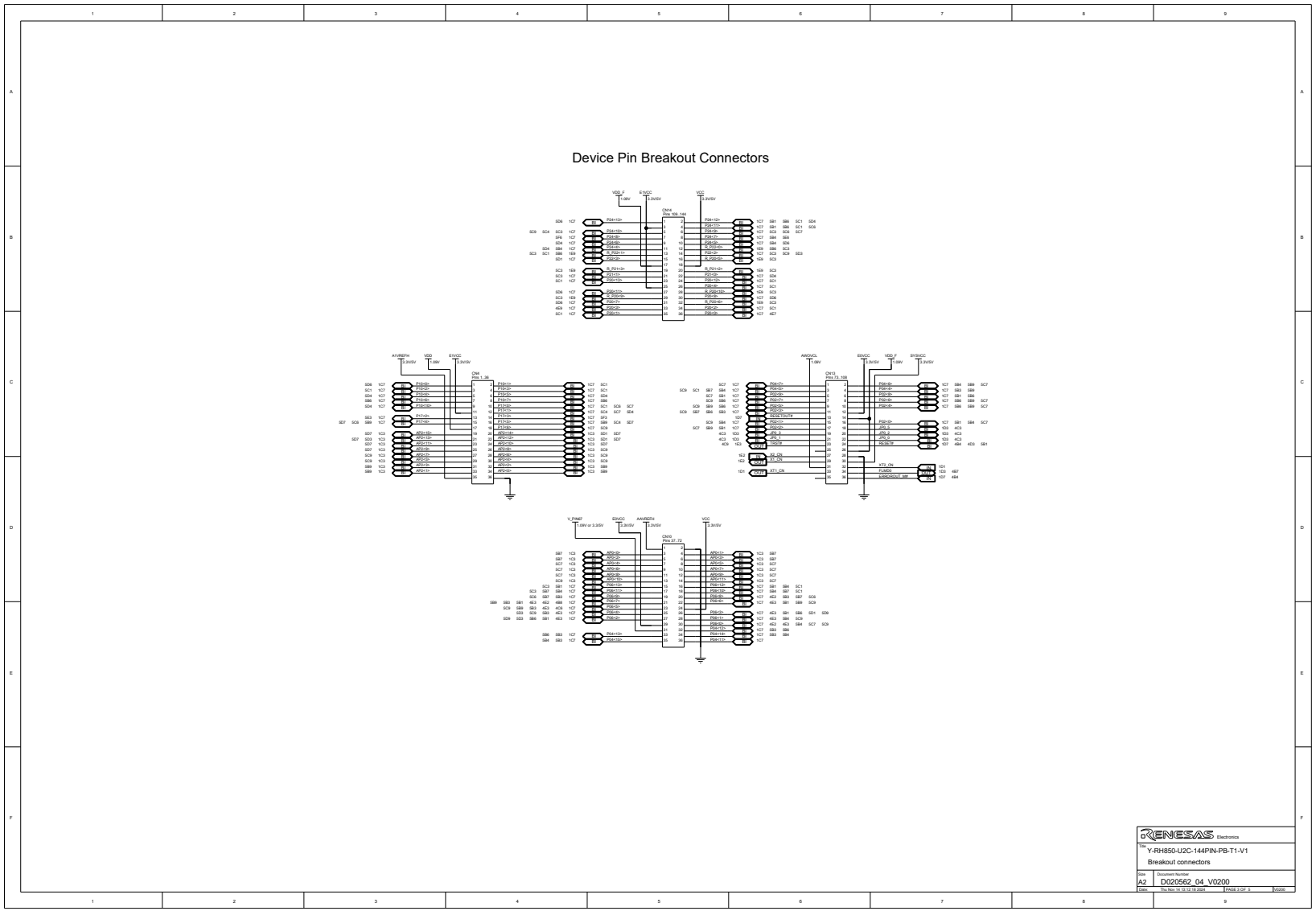
11.2.1 RH850/U2C



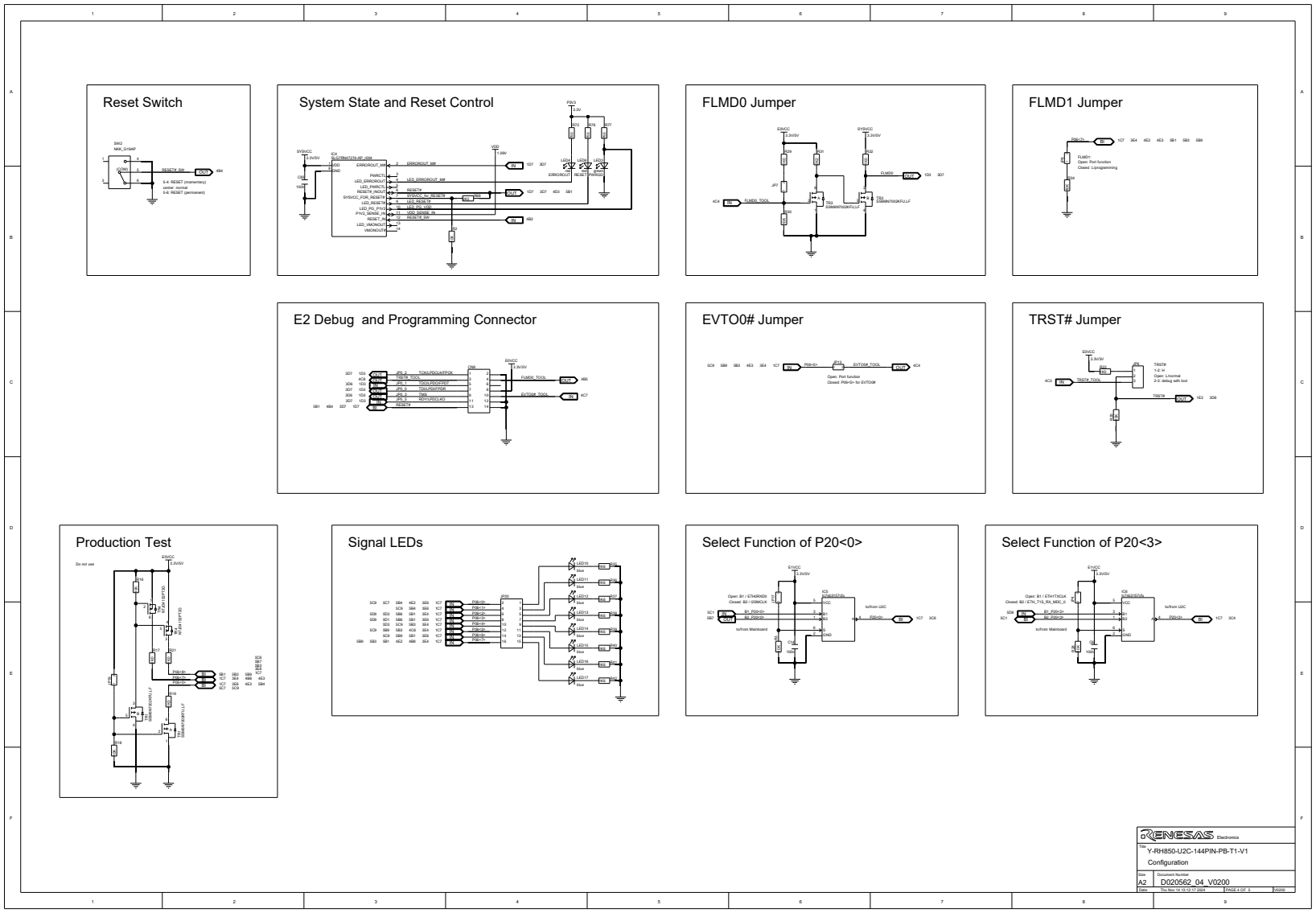
11.2.2 Power Supply



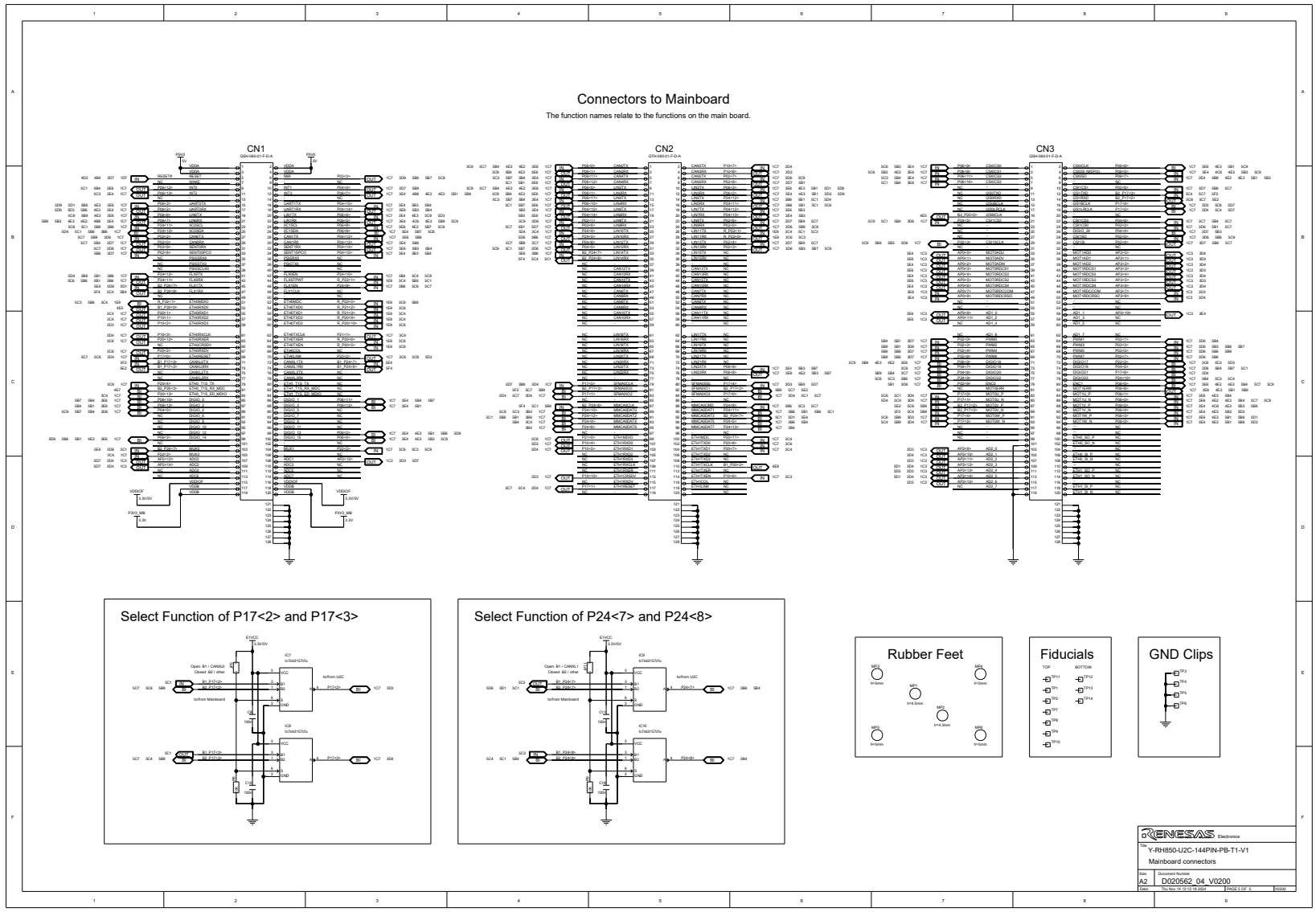
11.2.3 Breakout Connectors



11.2.4 Configuration



11.2.5 Main Board Connectors



Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2024-09-23	–	Initial release
V1.01	2024-11-06	*13*	Updated list of suitable devices and corrected comment for RH850/U2C2 device in *Table 1.4 Type names for suitable devices*.
		46	Updated pictures for jumper configuration examples in chapter *8 Jumper Configuration Examples*.
V2.00	2025-01-20	*8, 56, 69*	CN2.33 changed from P24<9> to P24<7>.
		28, 30	Replaced series resistors for CANXL signals (P17<2>, P17<3>, P24<7>, P24<8>) with multiplexers.
V2.01	2025-06-03	*56*	Updated contents in *Table 9.1 Connection for LIN14*.
		47	Updated information about eVR and DPS devices and added chapter *8.2.3 Core Voltage Supply for eVR and DPS Devices*.
V2.02	2026-04-22		Corrected some typos and updated the document style.

RH850/U2C 144pin Piggyback Board V1 User's Manual: Piggyback Board

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