

RH850 Evaluation Platform

RH850/U2C 100pin

User's Manual: Piggyback Board

Y-RH850-U2C-100PIN-PB-T1-V1

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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1. Overview

The RH850/U2C 100pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2C 100pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
For details regarding the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document active low signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g. the reset pin is named RESETZ or RESET#.
3. In this document the following abbreviations are used:
 - H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal.

1.1 Package Components

The Y-RH850-U2C-100PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2C-100PIN-PB-T1-V1 package contains all of these items. *Table 1.1 Package Components for the Y-RH850-U2C-100PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2C-100PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2C-100PIN-PB-T1-V1

Item	Description	Quantity
D020647	RH850/U2C 100pin piggyback board	1
D020649	Documentation CD	1
D010818-24	WEEE+CE document	1
D020648-24	Product contents list	1
Jumpers (2-way, 0.1")	In the bag	27 (board version D020647_06_V01) 29 (board version D020647_06_V02)
Red Hirschmann 4 mm power lab socket	In the bag	1
Resonator, HC49, 8 / 16 / 24 MHz	In the bag	3

Note

Please keep the Y-RH850-U2C-100PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2C-100PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-V1
- Y-COMMON-MB-T1-V1

1.3 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
 - Combined operation with power supply from main board
 - Stand-alone operation with single power supply (e.g. 3.3 V or 5.0 V only)
 - Stand-alone operation with flexible, individual power supply (typ. 1.09 V, 3.3 V, 5.0 V)
Refer to 3.3 *Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
 - Support JTAG/LPD debug interface
 - 14-pin connector for E2 emulator
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 8/16/20/24 MHz Crystal Resonator
- Eight general purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- Operating temperature from 0 °C to +40 °C

1.4 Piggyback Board Versions

The following versions of the piggyback board are available:

Table 1.2 Y-RH850-U2C-100PIN-PB-T1-V1 board versions

Board Version	Schematic Version
D020647_06_V01	D020647_04_V0100
D020647_06_V02	D020647_04_V0200

Table 1.3 lists all modifications that have been implemented in board versions D020647_06_V01 and D020647_06_V02.

Table 1.3 Differences between board versions V01 and V02

Item	Modified Function	Detailed Description of Changes	D020647_06_V01	D020647_06_V02
1	Power supply on device pin 48.	Pin 48 on RH850/U2C 100 pin package requires different voltages depending on the processor being used.	Pin 48 is always connected to VCC. Only devices with eVR for core voltage generation can be used.	Jumper JP2 has been added. Now voltage on pin 48 can be set to VDD (for devices with DPS core voltage supply) or to VCC (for devices with eVR core voltage supply).
2	CAN XL connections	Added multiplexers to switch functionality of ports P17_2, P17_3, P24_7 and P24_8 to improve signal quality for CAN XL interfaces.	On ports P17_2/P17_3 and P24_7/P24_8 the CAN XL functionality and other functions (e.g. SFMA, I2S, motor control) are separated by serial resistors.	Added multiplexers controlled by jumpers JP5 and JP11 to separate CAN XL ports from other functionalities.

1.5 Piggyback Board Views

Following figures provide the top and bottom views of the piggyback board.

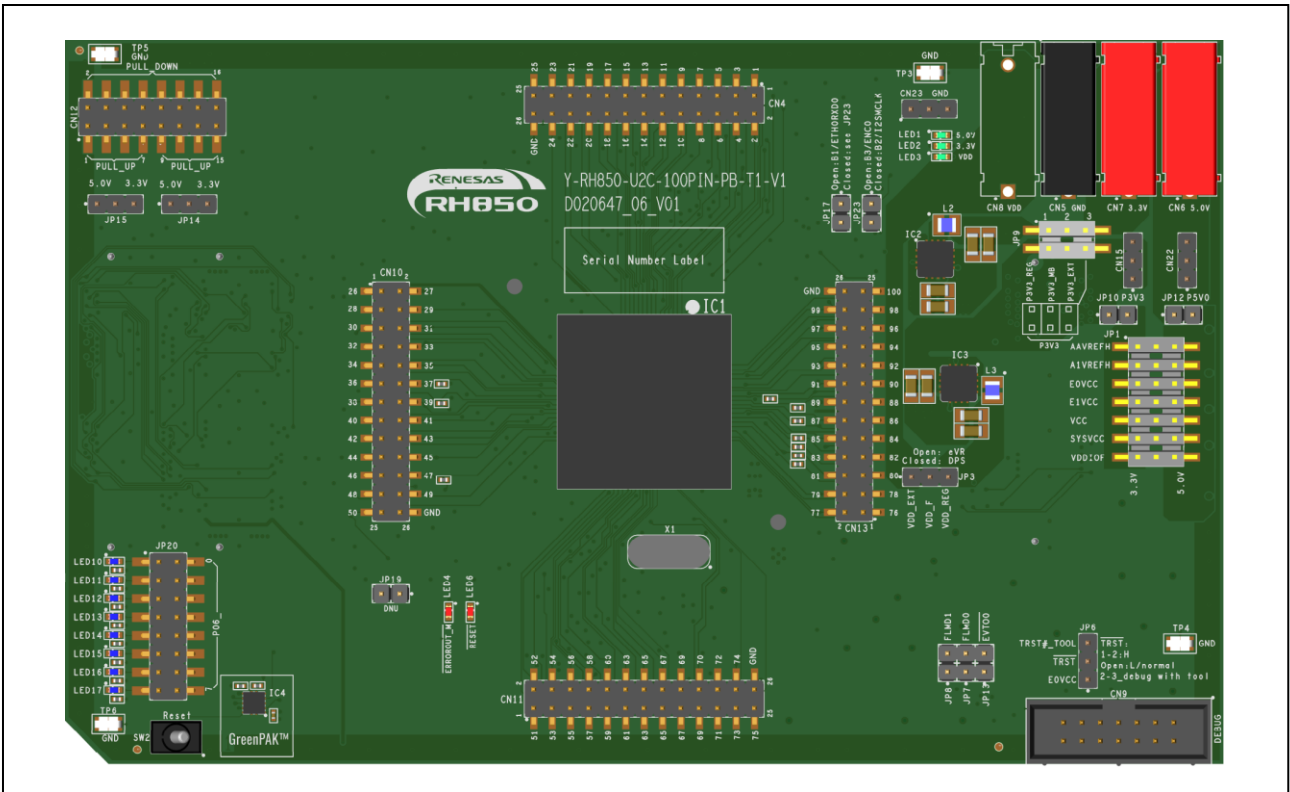


Figure 1.1 Piggyback board top view of board version D020647_06_V01

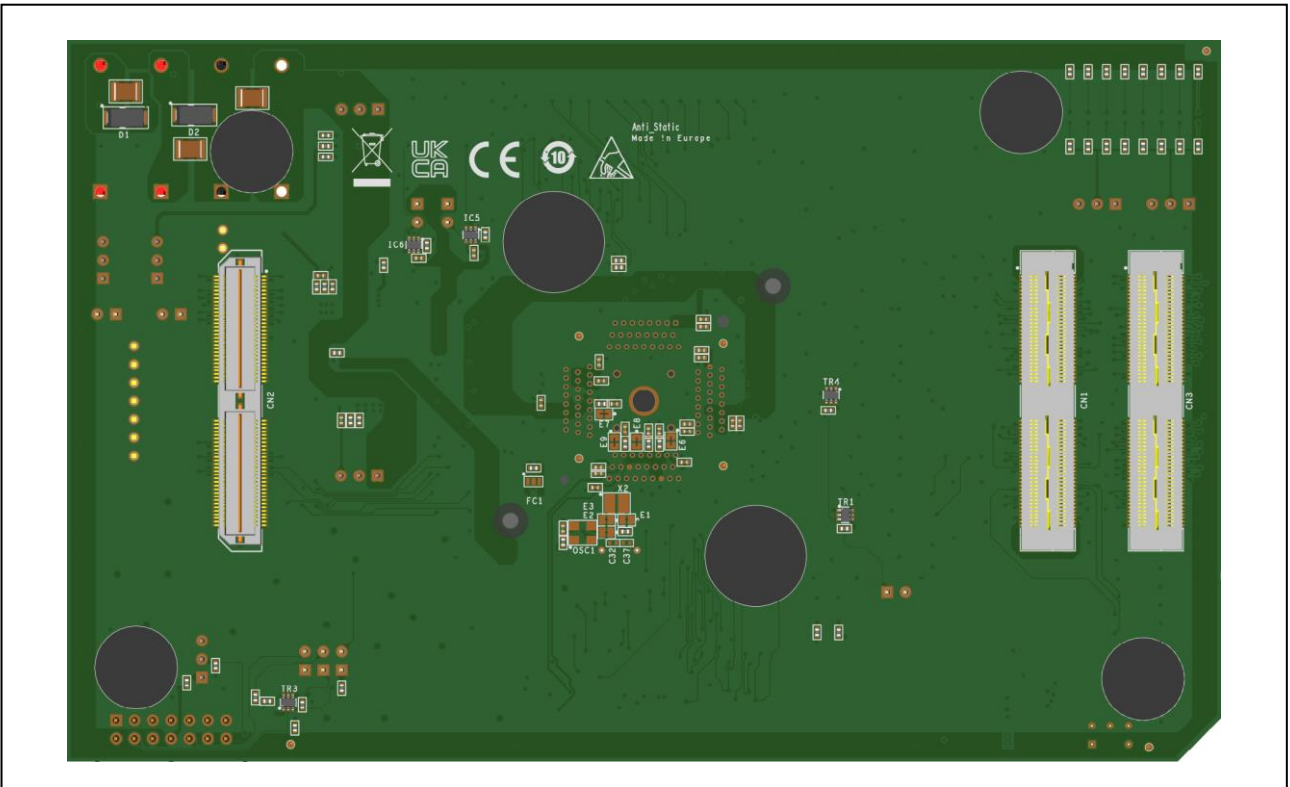


Figure 1.2 Piggyback board bottom view of board version D020647_06_V01

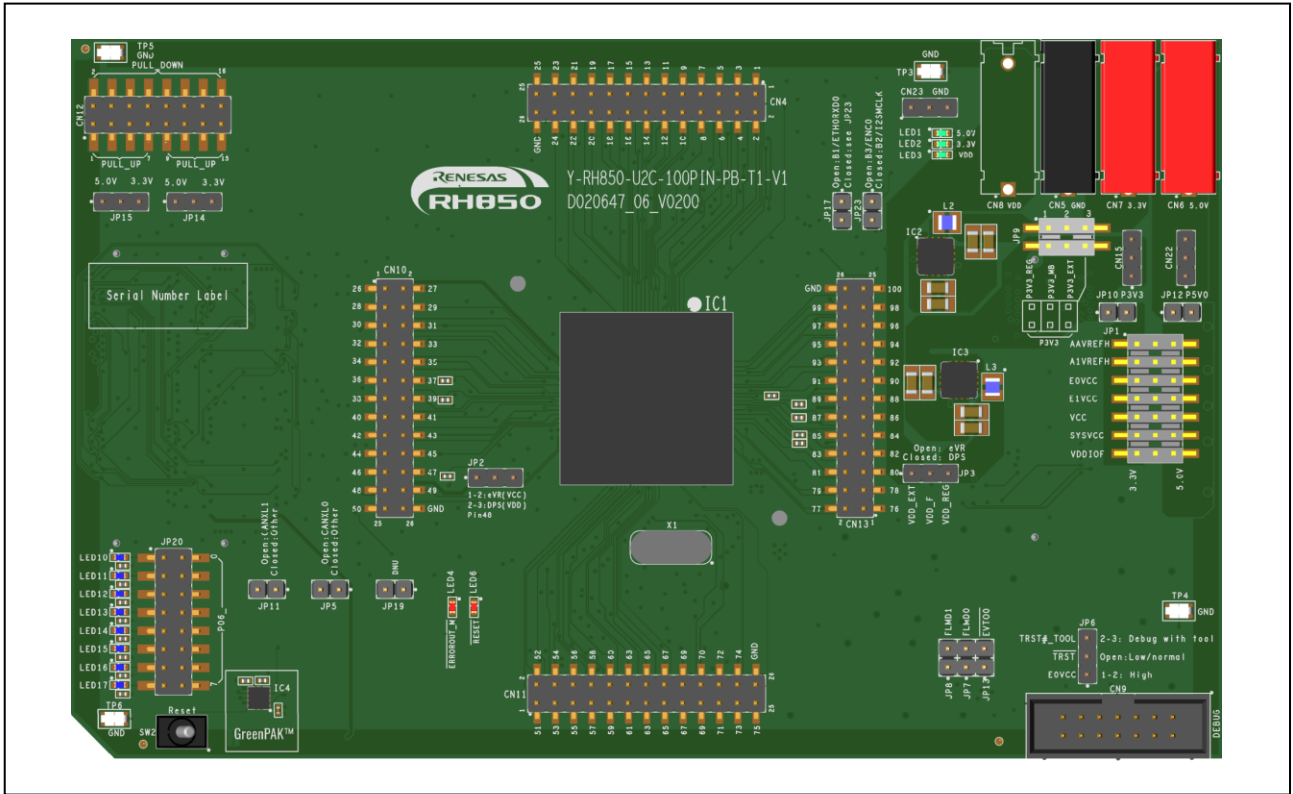


Figure 1.3 Piggyback board top view of board version D020647_06_V02

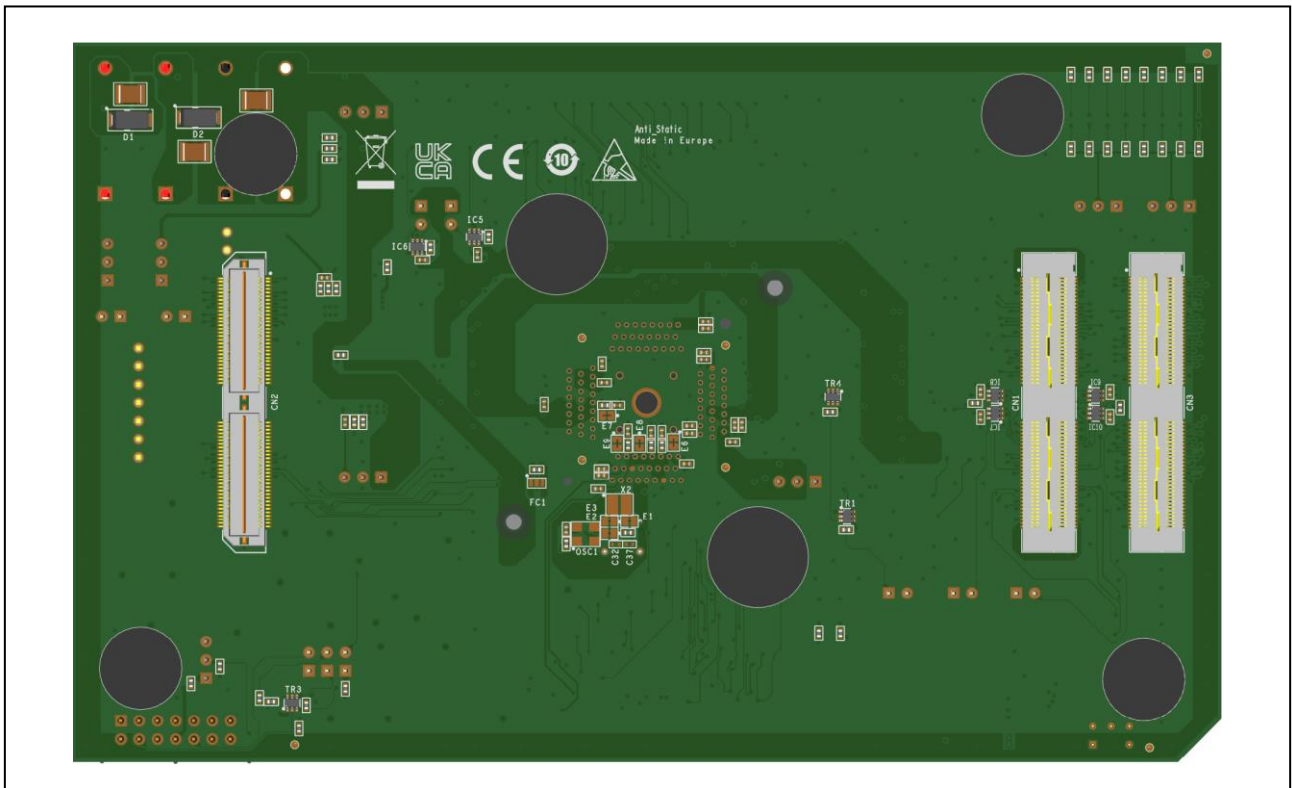


Figure 1.4 Piggyback board bottom view of board version D020647_06_V02

Following figures provide the drawing of top and bottom views of the piggyback board.

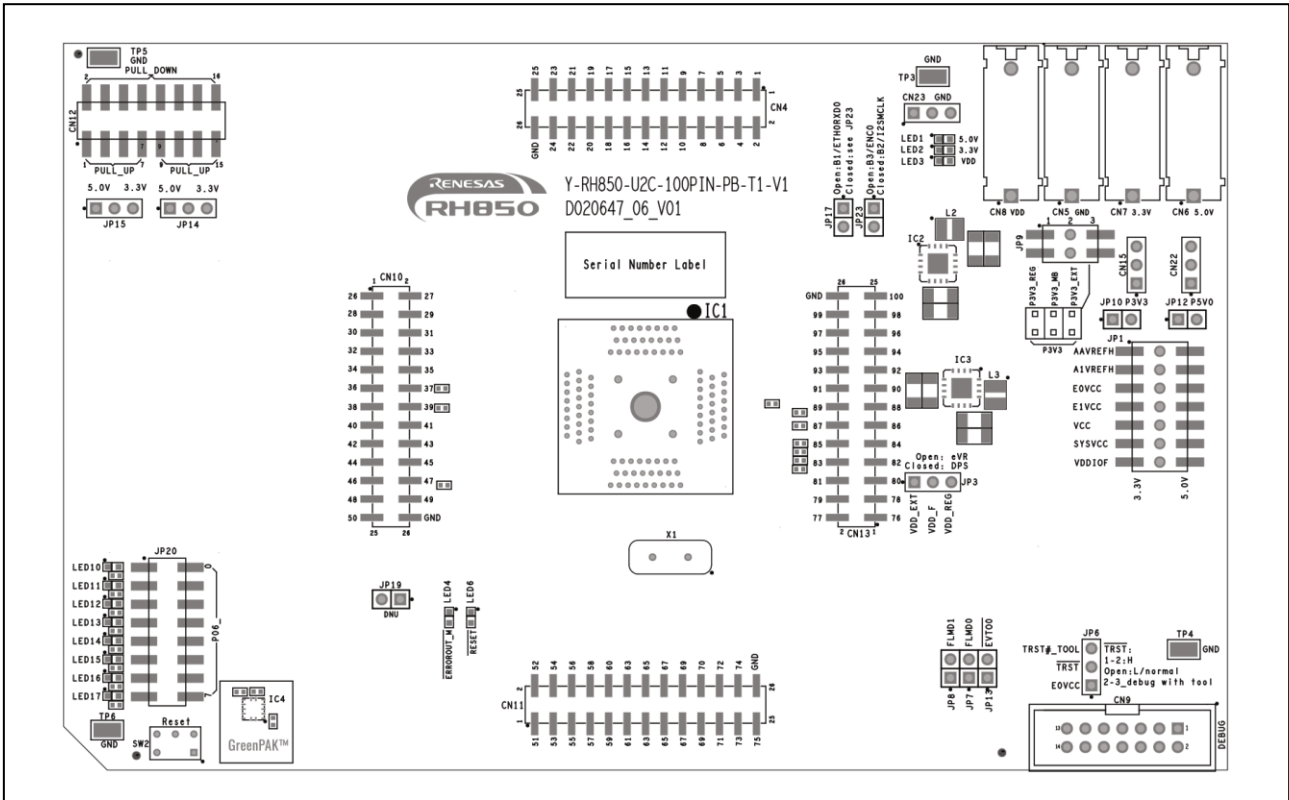


Figure 1.5 Piggyback board top view of board version D020647_06_V01

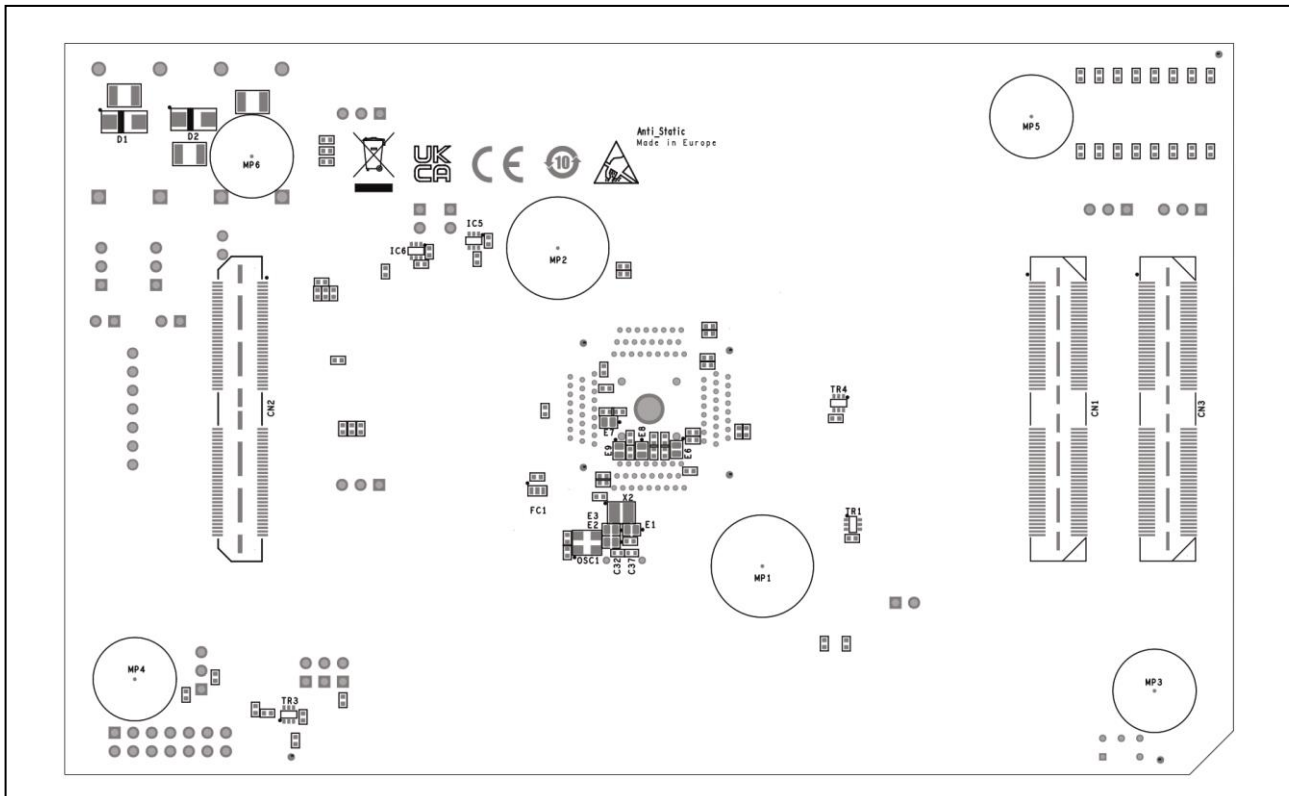


Figure 1.6 Piggyback board bottom view of board version D020647_06_V01

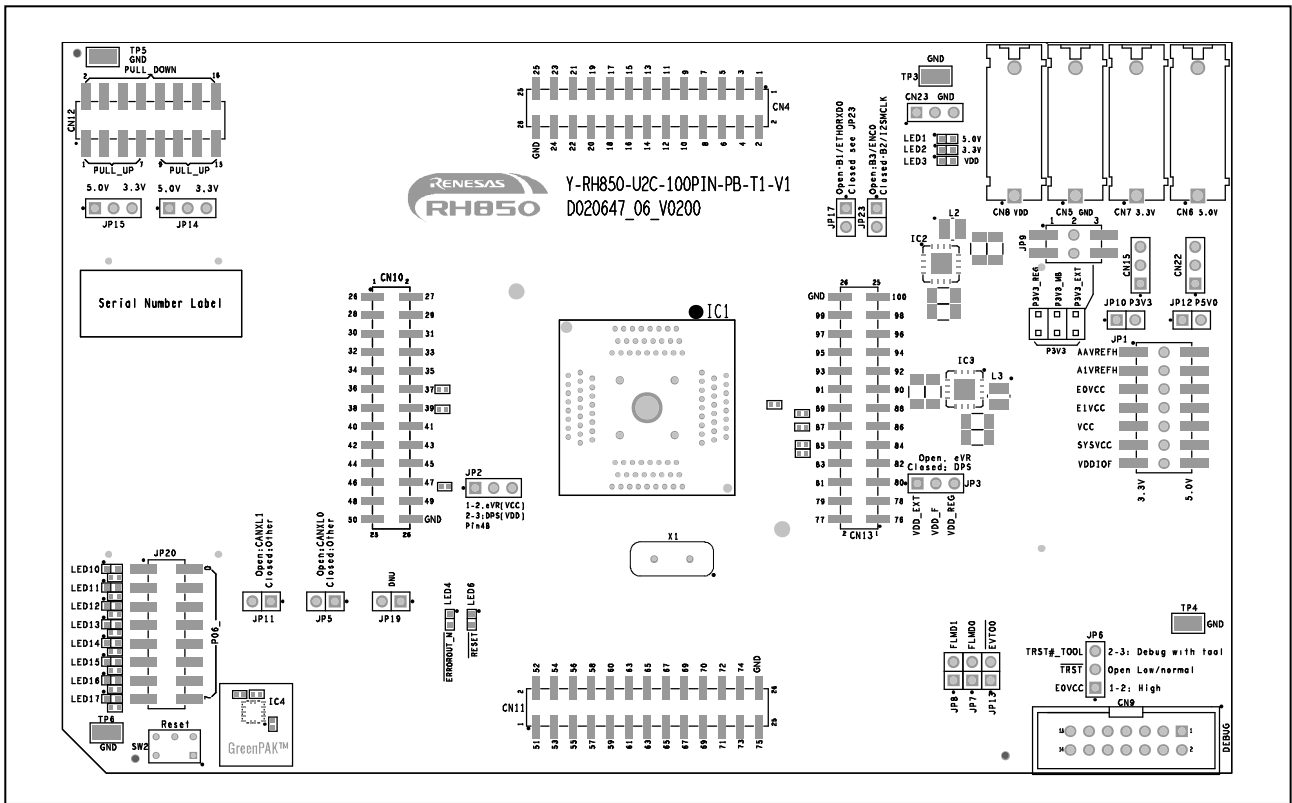


Figure 1.7 Piggyback board top view of board version D020647_06_V02

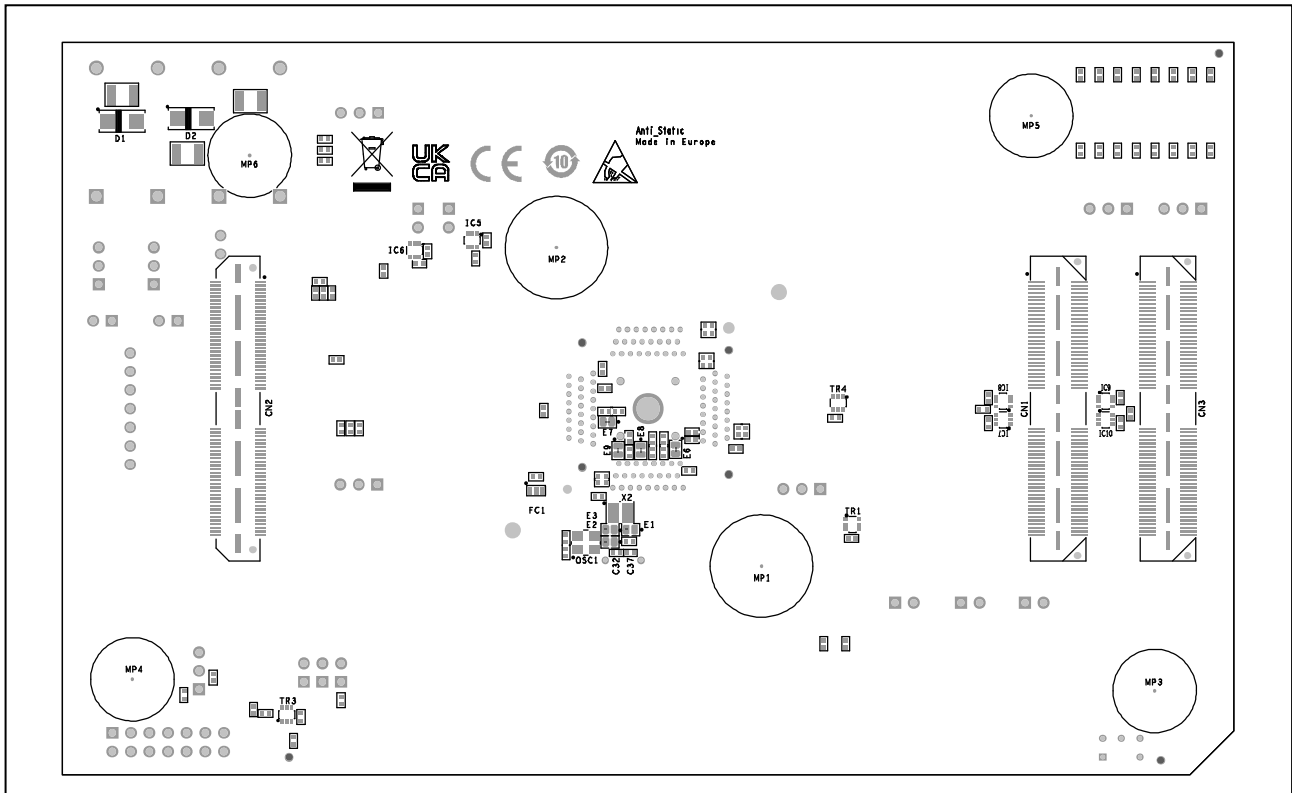


Figure 1.8 Piggyback board bottom view of board version D020647_06_V02

1.6 Mounting of the Device

The board is designed for use with the following devices.

Table 1.4 Type names for suitable devices

	Device Name	Comments
RH850/U2C4	R7F702606AFAFQ-C	Core power supply DPS*
	R7F702606AFAFD-C	DPS devices not supported by board version D020647_06_V01
	R7F702616AFAFQ-C	Core power supply eVR*
	R7F702616AFAFD-C	VCC = 4.5 V ~ 5.5 V
	R7F702613AFAFQ-C	Core power supply eVR*
	R7F702613AFAFD-C	VCC = VPOC ~ 3.6 V
RH850/U2C2	R7F702608AFAFQ-C	Core power supply eVR*
	R7F702608AFAFD-C	

* The isolated area power domain is supplied by an external power supply (DPS) or internal regulator (eVR).

The device must be placed inside the socket IC1. To insert the device, align the device package pin 1 with the marking on the pcb. There pin 1 of the socket is marked with a white dot. Please see *Figure 1.9 Yamaichi socket IC357-1004-254-1-YD*.

On the device the index area is available on the corner near pin 1.

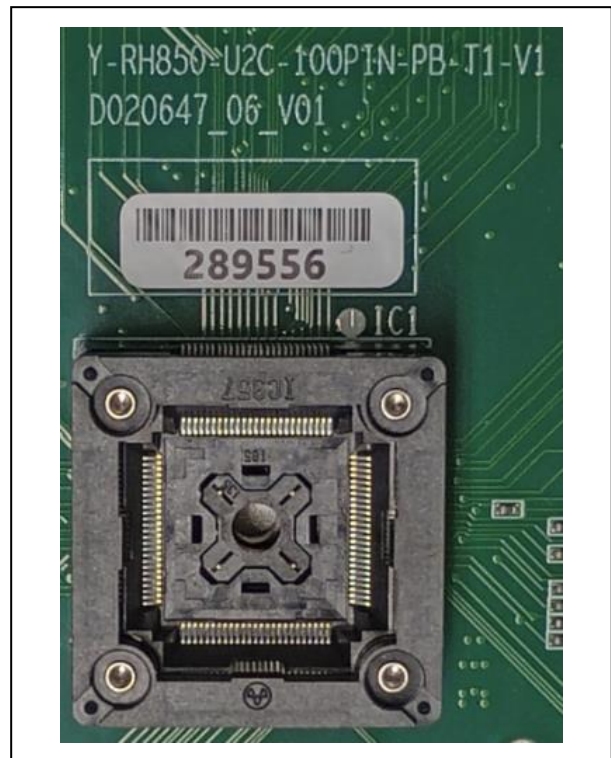


Figure 1.9 Yamaichi socket IC357-1004-254-1-YD

CAUTION

Be careful with the device placement in the socket to avoid damage to the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors and LEDs.

The placement of these components on the board is depicted in the figures below.

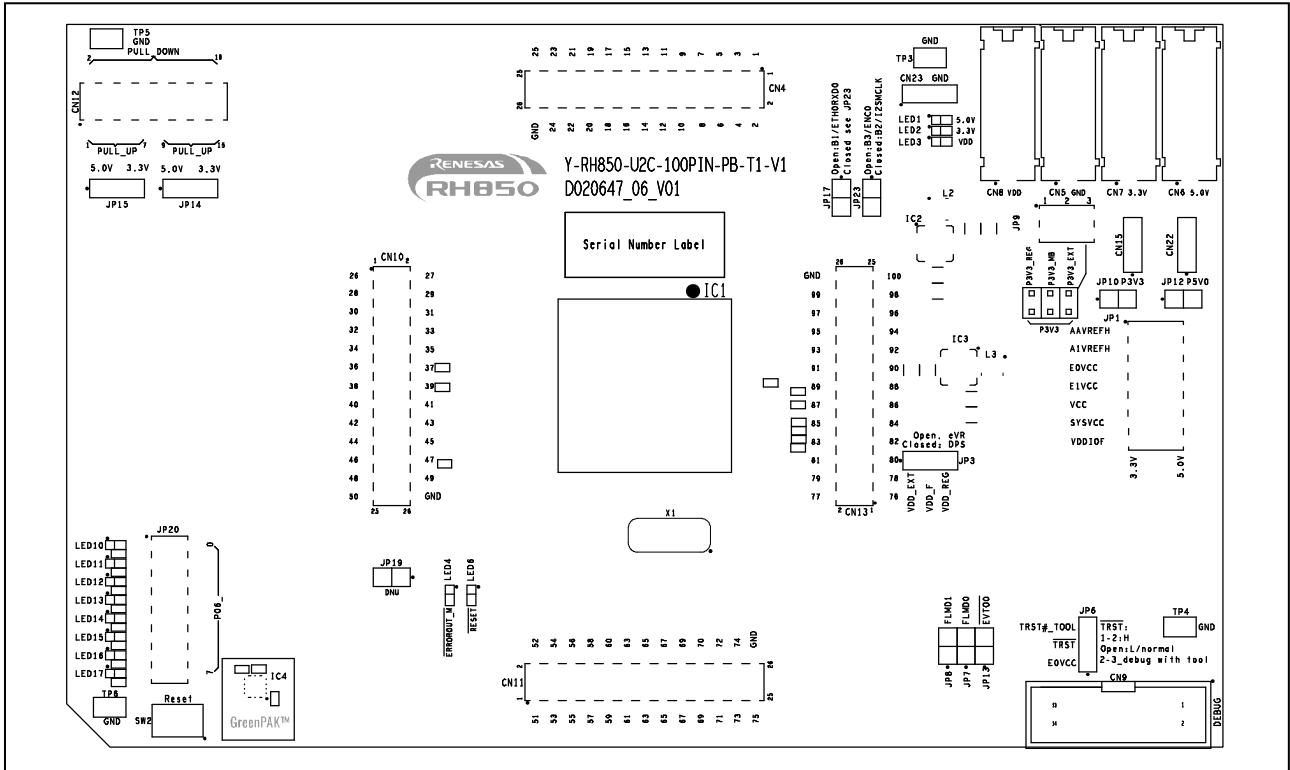


Figure 2.1 Placement of jumpers, connectors and LEDs on top side of board version D020647_06_V01

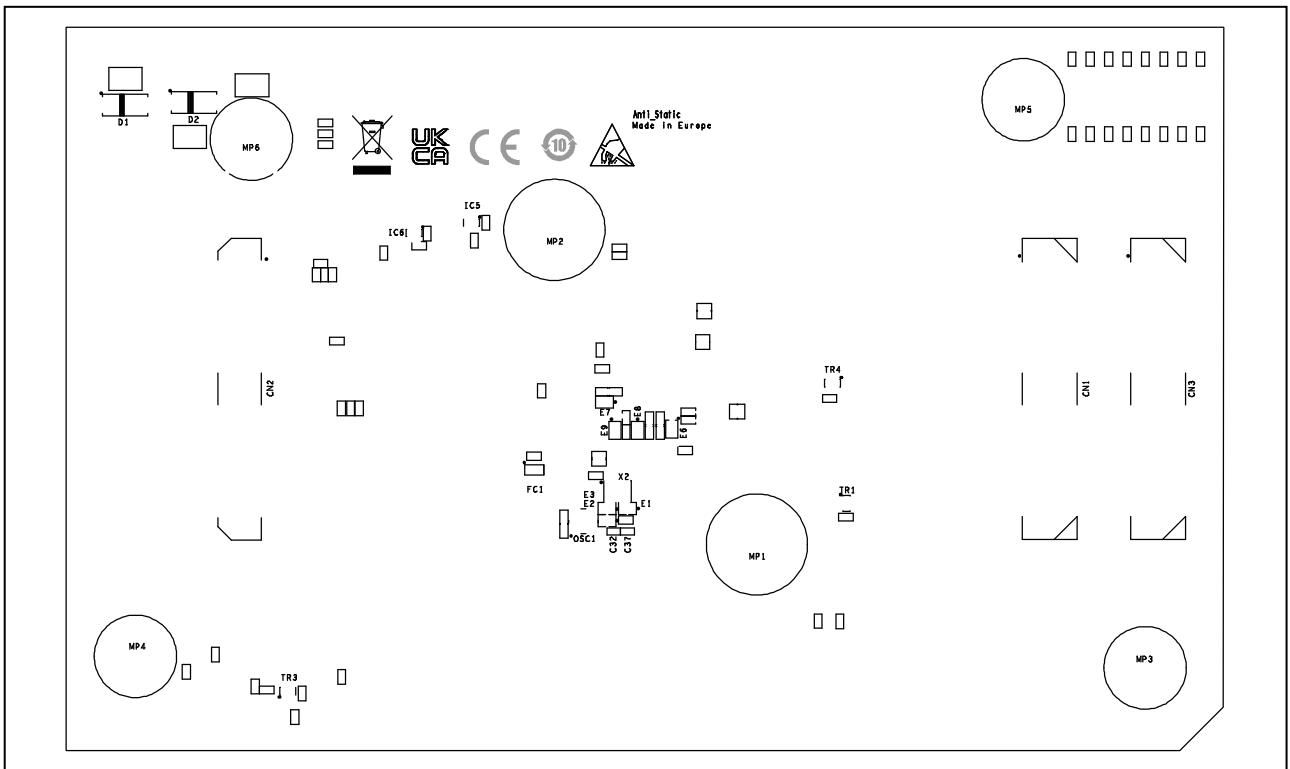


Figure 2.2 Placement of connectors on bottom side of board version D020647_06_V01

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select +3.3 V / +5.0 V power supply configuration	refer to 3.2 <i>Voltage Distribution</i>
JP2	Core voltage selection <ul style="list-style-type: none"> JP2[1-2]: VDD supply from external supply CN8 JP2[2-3]: VDD supply from on-board voltage regulator 	refer to 3.3 <i>Device Core Voltage (VDD) Selection</i>
JP3	Core voltage selection for DPS device <ul style="list-style-type: none"> JP3[OPEN]: eVR device JP3[1-2]: VDD supply from external supply CN8 JP3[2-3]: VDD supply from on-board voltage regulator 	
JP5	Select port P17_2 / P17_3 connection to an attached main board. <ul style="list-style-type: none"> JP5[OPEN]: P17_2 and P17_3 connected to CANXL0 pins on connector CN1. JP5[CLOSED]: P17_2 and P17_3 connected to SFMA0 pins on connector CN2, MOT0 and I2S1 pins on connector CN3. 	refer to 6.4 <i>CAN XL Ports</i>
JP6	Select signal source for TRST# signal <ul style="list-style-type: none"> JP6[1-2]: Fix TRST# signal to E0VCC JP6[2-3]: TRST# signal is TRST_TOOL# signal from E2 debug connector (pin 3 on connector CN9) 	refer to 5 <i>Debug and Flash Programming Interface</i>
JP7	Change FLMD0 signal to "H".	refer to 6.1 <i>Operation Mode Selection</i>
JP8	Change FLMD1 signal to "L".	
JP9	Select +3.3 V power supply source <ul style="list-style-type: none"> JP[1-4]: Get +3.3 V from onboard voltage regulator JP[2-5]: Get +3.3 V from main board JP[3-6]: Get +3.3 V from external +3.3 V supply on CN7 	refer to 3.2 <i>Voltage Distribution</i>
JP10	Current measurement bridge +3.3 V	refer to 3.4 <i>Current Measurement Bridges</i>
JP11	Select port P24_7 / P24_8 connection to an attached main board. <ul style="list-style-type: none"> JP11[OPEN]: P24_7 and P24_8 connected to CANXL1 pins on connector CN1. JP11[CLOSED]: P24_7 and P24_8 connected to FLX1 and MUX on connector CN1, LIN14 and MMCA0 pins on connector CN2. 	refer to 6.4 <i>CAN XL Ports</i>
JP12	Current measurement bridge +5.0 V	refer to 3.4 <i>Current Measurement Bridges</i>
JP13	Debug port connection EVTO0	refer to 5 <i>Debug and Flash Programming Interface</i>
JP14	Select pull-up voltage for Pull-Up Pull-Down connector CN12 <ul style="list-style-type: none"> JP14[1-2]: 5.0 V pull-up on pins 9 / 11 / 13 / 15 JP14[2-3]: 3.3 V pull-up on pins 9 / 11 / 13 / 15 	refer to 6.7 <i>Pull-Up/Pull-Down Pin Header</i>

Table 2.1 Jumper overview

Jumper	Function	Remark
JP15	Select pull-up voltage for Pull-Up Pull-Down connector CN12 <ul style="list-style-type: none"> JP15[1-2]: 5.0 V pull-up on pins 1 / 3 / 5 / 7 JP15[2-3]: 3.3 V pull-up on pins 1 / 3 / 5 / 7 	refer to 6.7 Pull-Up/Pull-Down Pin Header
JP17	Select port P20_0 connection to an attached main board <ul style="list-style-type: none"> JP17[OPEN]: P20_0 connected to B1_P20_0 (ETH0RXD0) JP17[CLOSED]: Output selected by jumper JP23 	refer to 6.3 Port P20_0 Selection
JP19	Jumper for board production test	Must be left open
JP20	Enable signal LED outputs	refer to 6.6 Signal LEDs
JP23	Select port P20_0 connection to an attached main board. Requires that jumper JP17 = CLOSED. <ul style="list-style-type: none"> JP23[OPEN]: P20_0 connected to B3_P20_0 (ENC0) JP23[CLOSED]: P20_0 connected to B2_P20_0 (I2SMCLK) 	refer to 6.3 Port P20_0 Selection

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview

Connector	Function	Remark
CN1	Main board connectors	refer to 7.1 Connectors to the Main Board CN1 to CN3
CN2		
CN3		
CN4	Device ports connector	refer to 7.2 Device Ports Connectors CN4, CN10, CN11 and CN13
CN5	GND external power supply	refer to 3.1 Board Power Connection
CN6	+5.0 V external power supply	
CN7	+3.3 V external power supply	
CN8	+1.09 V external power supply	
CN9	E2 emulator debug connector	refer to 5 Debug and Flash Programming Interface
CN10	Device ports connector	refer to 7.2 Device Ports Connectors CN4, CN10, CN11 and CN13
CN11		
CN12	Pull-up / pull-down connector	refer to 6.7 Pull-Up/Pull-Down Pin Header
CN13	Device ports connector	refer to 7.2 Device Ports Connectors CN4, CN10, CN11 and CN13
CN15	+3.3 V connector	
CN22	+5.0 V connector	
CN23	GND connector	

2.3 Switches Overview

The following table provides an overview of all switches.

Table 2.3 Switches overview

Connector	Function	Remark
SW2	RESET# switch	refer to 6.2 <i>System State and RESET</i>

2.4 LED Overview

The following table provides an overview of all LED.

Table 2.4 LED overview

LED	Function	Color	Remark
LED1	5.0 V power supply P5V0	green	refer to 3.5 <i>Power Supply LEDs</i>
LED2	3.3 V power supply P3V3	green	
LED3	LED_PG_VDD signal	green	refer to 6.2 <i>System State and RESET</i>
LED4	LED_ERROROUT_M# signal	red	
LED6	LED_RESET# signal	red	
LED10	Signal LEDs	blue	refer to 6.6 <i>Signal LEDs</i>
LED11			
LED12			
LED13			
LED14			
LED15			
LED16			
LED17			

3. Power Supply

3.1 Board Power Connection

RH850/U2C and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board.
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage.
- 1.09 V for RH850/U2C core voltage VDD.
Refer to 3.3 *Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as 'typical'.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

Four 4 mm 'banana-type' connectors are available to connect external power supplies:

- black connector CN5 for GND (VSS)
- red connector CN6 for 5.0 V (P5V0)
- red connector CN7 for 3.3 V (P3V3_EXT)
- red connector CN8 for 1.09 V (P1V09_EXT)

Connector CN8 is not assembled at delivery of the board, but separately supplied with the board package.

Refer to 3.3 *Device Core Voltage (VDD) Selection* for further details about VDD voltage.

If the piggyback board is mounted on a main board, all voltages except for 1.09 V (VDD) can be supplied by the main board:

- The jumper JP9[2-5] (3.3 V) is used to enable P3V3 supply from main board.
- P5V0 is always connected to the main board.

CAUTION

Do not supply the 5 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board if power supply from the main board is enabled.

Connecting external 1.09 V via CN8 (and GND via CN5) is still an option also in this case.

The piggyback board has 2 voltage regulator circuits. Both use Renesas ISL78234 buck regulator.

IC2 generates the board voltage of 3.3V (P3V3_REG) from 5.0V (P5V0) input voltage on CN6.

IC3 generates the core voltage of 1.09V (P1V09_REG) from 3.3V (P3V3).

Figure 3.1 shows both voltage regulator circuits.

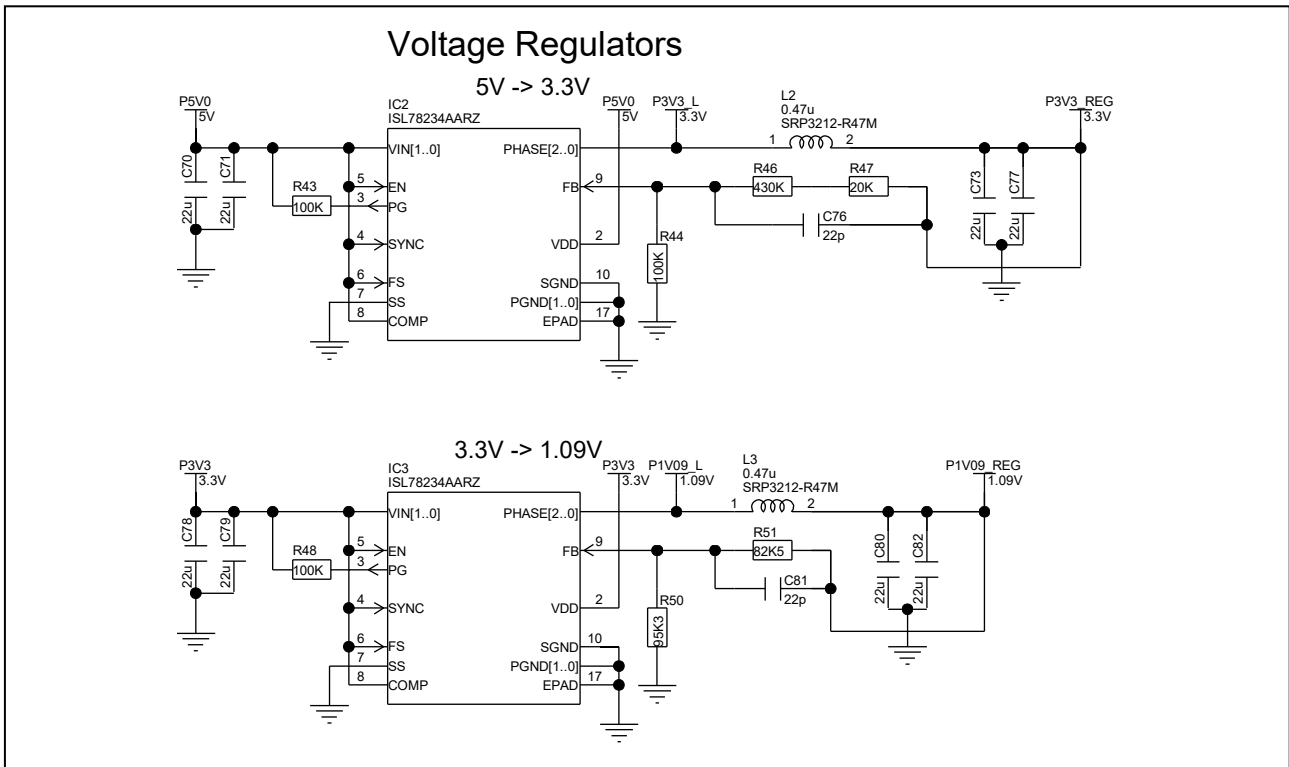


Figure 3.1 Voltage regulator circuit

The jumper settings for some general power supply scenarios are described in 8 Jumper Configuration Examples.

3.2 Voltage Distribution

Table 3.1 shows the required device power supply pins and their functions.

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
AAVREFH, A1VREFH	3.3 V, 5 V	A/D converter's power supplies and reference voltages
E0VCC, E1VCC	3.3 V, 5 V	Power supply for I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SYSVCC	3.3 V, 5 V	Power supply for System Logic and internal voltage regulator power
VDDIOF	3.3 V, 5 V	I/O voltage supply for the main board
VDD_F	1.09 V	Core supply voltage Refer to 3.3 Device Core Voltage (VDD) Selection

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V (P3V3) can be selected from external power supply (P3V3_EXT, CN7), main board power supply (P3V3_MB) or from the onboard voltage regulator (P3V3_REG) using jumper JP9:

- JP9 [1-4]: P3V3 comes from the onboard voltage regulator P3V3_REG.
- JP9 [2-5]: P3V3 comes from the main board power supply P3V3_MB.
- JP9 [3-6]: P3V3 comes from the external power supply P3V3_EXT / CN7.

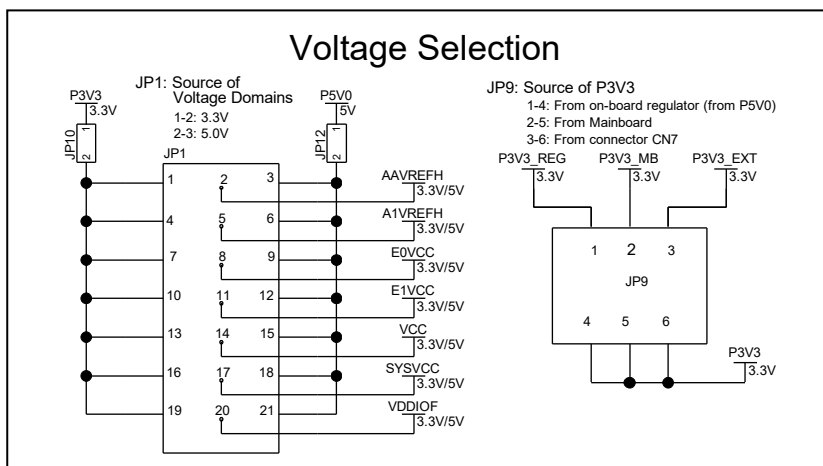


Figure 3.2 Voltage distribution

The supply for 5.0 V (P5V0) may come from the external power supply CN6 or from the main board.

Note

Do not supply the 5 V (CN6) and 3.3 V (CN7) voltage directly to the piggyback board if power supply from the main board is enabled.

Connecting external 1.09 V via CN8 (and GND via CN5) is still an option also in this case.

Table 3.2 shows which jumpers to set to select the different device supply voltages, and Figure 3.2 shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
AAVREFH	JP1 [1-2]	JP1 [2-3]
A1VREFH	JP1 [4-5]	JP1 [5-6]
E0VCC	JP1 [7-8]	JP1 [8-9]
E1VCC	JP1 [10-11]	JP1 [11-12]
VCC	JP1 [13-14]	JP1 [14-15]
SYSVCC	JP1 [16-17]	JP1 [17-18]
VDDIOF	JP1 [19-20]	JP1 [20-21]

3.3 Device Core Voltage (VDD) Selection

The piggyback board can be used with RH850/U2C2 and RH850/U2C4 processors. RH850/U2C processors have different options for core voltage generation.

RH850/U2C2 devices have always an embedded voltage regulator (eVR) for internal core voltage generation.

RH850/U2C4 devices are available as device with embedded voltage regulator (eVR) or with external 1.09V supply (DPS) for core voltage.

The external core voltage VDD (typ.1.09 V) for RH850/U2C4 DPS devices can be

- supplied from external via CN8 (voltage P1V09_EXT)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage P1V09_REG)

Table 3.3 shows the jumper setting for core voltage supply, Figure 3.3 shows the related circuit diagram.

Table 3.3 eVR / DPS core voltage supply selection

Jumper	Function
JP3	RH850/U2C core voltage supply selection <ul style="list-style-type: none"> • JP3[OPEN]: eVR device • JP3[1-2]: DPS device, external VDD supply (VDD_F = P1V09_EXT) • JP3[2-3]: DPS device, VDD from on-board voltage regulator (VDD_F = P1V09_REG)

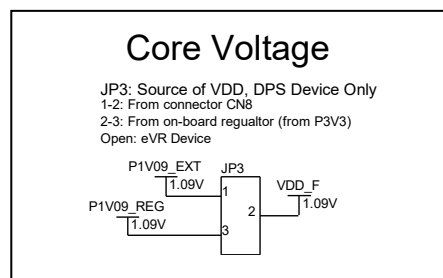


Figure 3.3 Core voltage selection

CAUTION

Board version D020647_06_V01 does not support DPS devices.
 DPS devices are supported in pcb version D020647_06_V02 and later.

3.4 Current Measurement Bridges

The total current of the P5V0 and P3V3 power rails can be measured by replacing the jumpers JP10 and JP12 with a current meter.

The current of specific power supply pins of the device can be measured via their respective supply selection jumpers, refer to Figure 3.2 Voltage distribution.

3.5 Power Supply LEDs

The following green LEDs indicate the presence of various voltages on the piggyback board:

- LED1 for 5.0 V power rail P5V0
- LED2 for 3.3 V power rail P3V3
- LED3 for 1.09 V device core voltage VDD

4. Clock Supply

The ports X1 and X2 are used for the main oscillator.

Figure 4.1 shows the oscillator circuit.

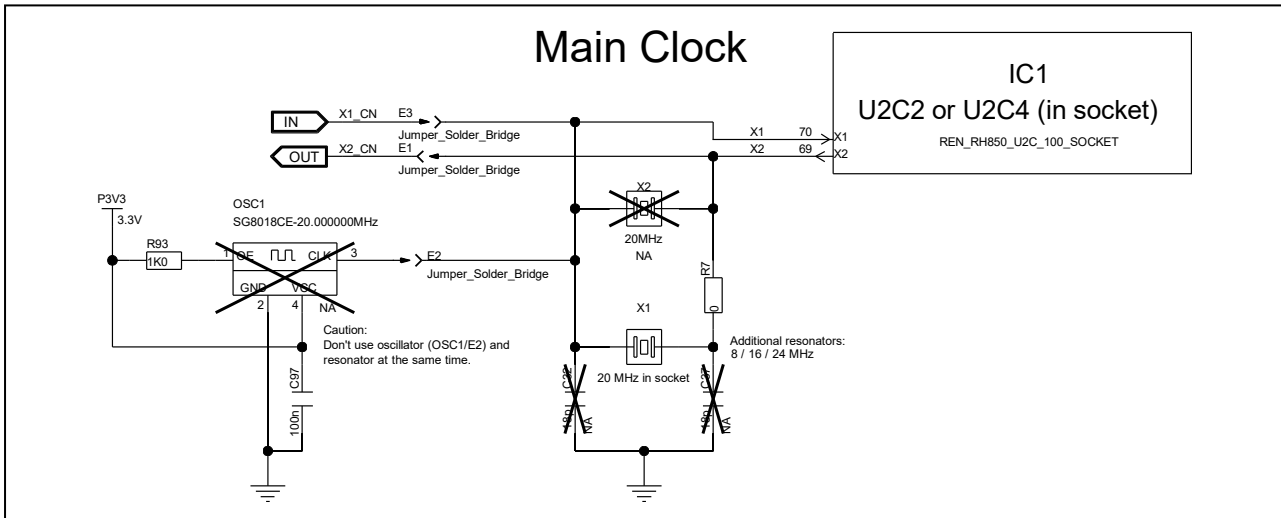


Figure 4.1 Main oscillator circuit

CAUTION

Only one oscillator, either X1, X1_CN, X2 or OSC1, can be used at any one time for the main oscillator.

4.1 Main Oscillator

For operating the on-chip main oscillator the piggyback board provides a socket (X1) for a resonator.

Several resonators for various main oscillator frequencies (8 MHz, 16 MHz, 20 MHz, 24 MHz) are included in the board package. The 20MHz resonator is by default mounted to X1.

For package contents please refer to *1.1 Package Components*.

The piggyback board has a footprint on the lower side of the pcb to mount an oscillator of a different physical dimension.

4.2 External Oscillator

The clock signals from an external oscillator can be input to the piggyback board using the pins 20 (X1_CN, clock input) and 19 (X2_CN, clock monitor) on device pin connector CN11.

To use the external clock input the solder bridge E3 must be closed.

To use the clock monitor signal the solder bridge E1 must be closed.

4.3 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via solder bridge E2.

5. Debug and Flash Programming Interface

For debugging and flash programming purposes debug and flash programming tools can be connected to CN9 connector.

The Renesas standard emulator for RH850/U2C is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

Figure 5.1 shows the circuit diagram for the emulator interface.

CN9 is the debug connector for Renesas E2 emulator.

The piggyback board has three jumpers to enable control signals coming from the emulator.

Jumper JP6 controls the input signal of TRST# to RH850/U2C.

- JP6[OPEN]: TRST# input to RH850/U2C is fixed to “L” level.
- JP6[1-2]: TRST# input to RH850/U2C is fixed to “H” level input.
- JP6[2-3]: TRST# input to RH850/U2C is fixed to “L” level input. If an emulator is connected to connector CN9, the emulator can control this signal.

Jumper JP7 enables the FLMD0 signal connection from the emulator to RH850/U2C.

- JP7[OPEN]: FLMD0 input to RH850/U2C is fixed to “L” level. If an emulator is connected to connector CN9, the emulator can control this signal.
- JP7[CLOSED]: FLMD0 signal input to RH850/U2C is fixed to “H” level input.

RH850/U2C can provide an event trigger signal to a connected emulator. Jumper JP13 enables the EVTO0# signal connection from RH850/U2C to the emulator.

- JP13[OPEN]: EVTO0# signal is not connected to the emulator.
- JP13[CLOSED]: EVTO0# signal can be output to the emulator.

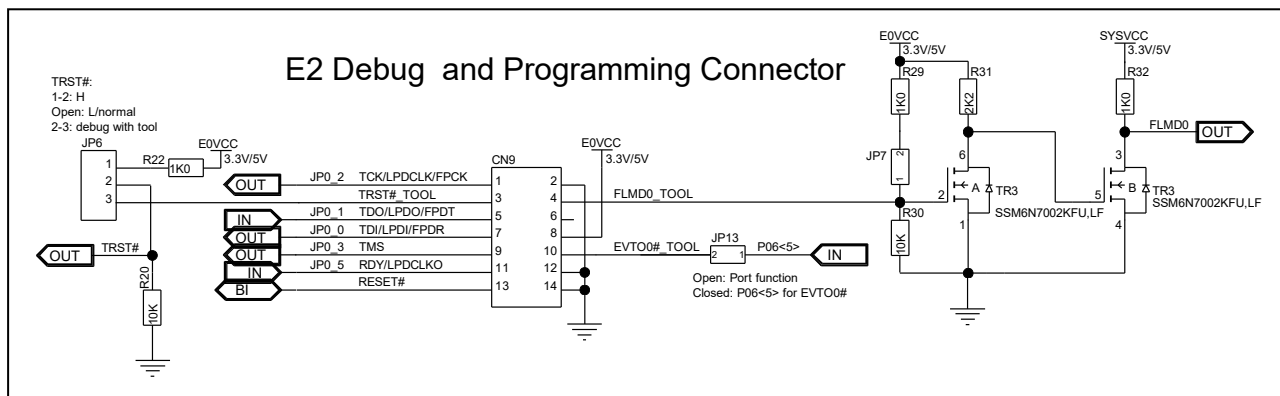


Figure 5.1 E2 debug connector CN9

6. Other Circuitry

6.1 Operation Mode Selection

RH850/U2C has 3 pins related to operating mode selection. The pins are TRST#, FLMD0 and FLMD1. The piggyback board gives the possibility to configure these pins using jumpers JP6, JP7 and JP8.

Table 6.1 shows the functionality of the jumpers, Figure 6.1 shows the circuit diagrams.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP6	TRST# signal <ul style="list-style-type: none"> ▪ JP6[OPEN]: TRST# fixed to “L” level ▪ JP6[1-2]: TRST# fixed to “H” level ▪ JP6[2-3]: TRST# control from emulator
JP7	FLMD0 pin level <ul style="list-style-type: none"> ▪ JP7[CLOSED]: FLMD0 = H level ▪ JP7[OPEN]: FLMD0 <ul style="list-style-type: none"> • controlled by debugger or programming tool if a tool is connected via CN9. • fixed to GND, if no tool connected.
JP8	FLMD1 pin level JP8[CLOSED]: FLMD1 = GND JP8[OPEN]: FLMD1 open

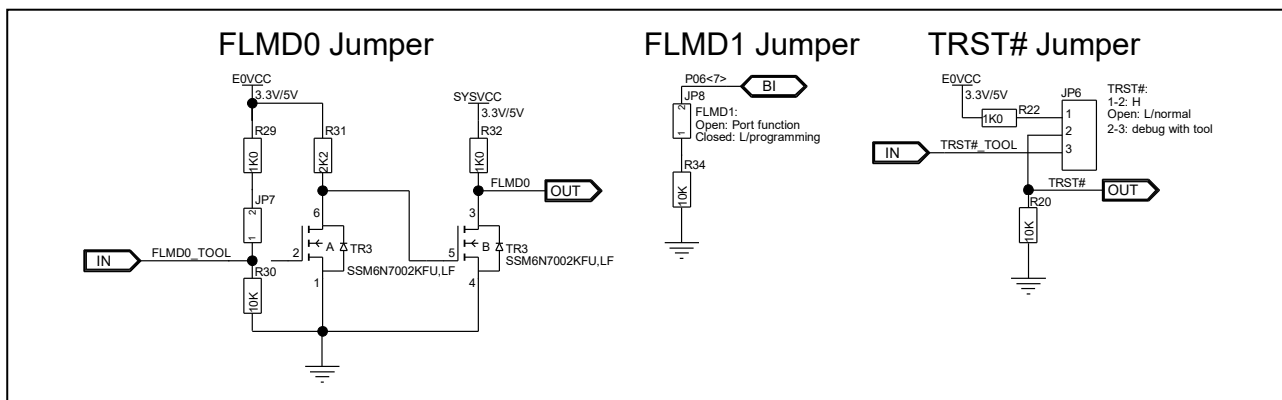


Figure 6.1 Operating mode selection jumpers

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.

This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, remove the jumper JP7.

All other jumpers related to the mode selection can be left open.

6.2 System State and RESET

This piggyback board has a special reset circuit using the Renesas GreenPAK IC SLG7RN47274. This IC is designed to receive various RH850 control signals and switch control LEDs accordingly. It also receives the signal from the RESET switch SW2 to generate the reset signal for the piggyback board and controls the reset LED.

The piggyback board has 3 LEDs to indicate control signals and reset status:

- LED3 is the control LED for RH850/U2C core voltage VDD.
- LED4 is a control signal triggered by ERROROUT_M#.
- LED6 is a reset signal triggered by the reset switch SW2.

Figure 6.2 shows the circuit of the GreenPAK IC and the reset signal inputs.

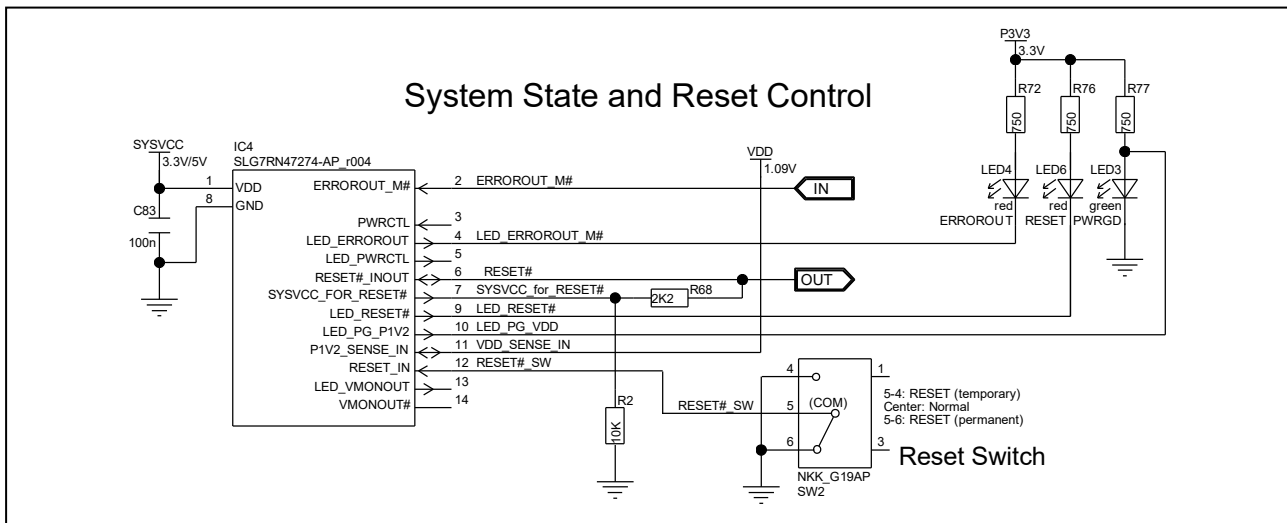


Figure 6.2 RESET circuit

6.2.1 RESET Switch

Switch SW2 is used to issue a reset to the RH850/U2C.

The SW2 toggle switch allows to activate the reset in two different ways:

- SW2 in left '5-4' (left) position: temporary reset
Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW2 in right '5-6' (right) position: permanent reset
For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

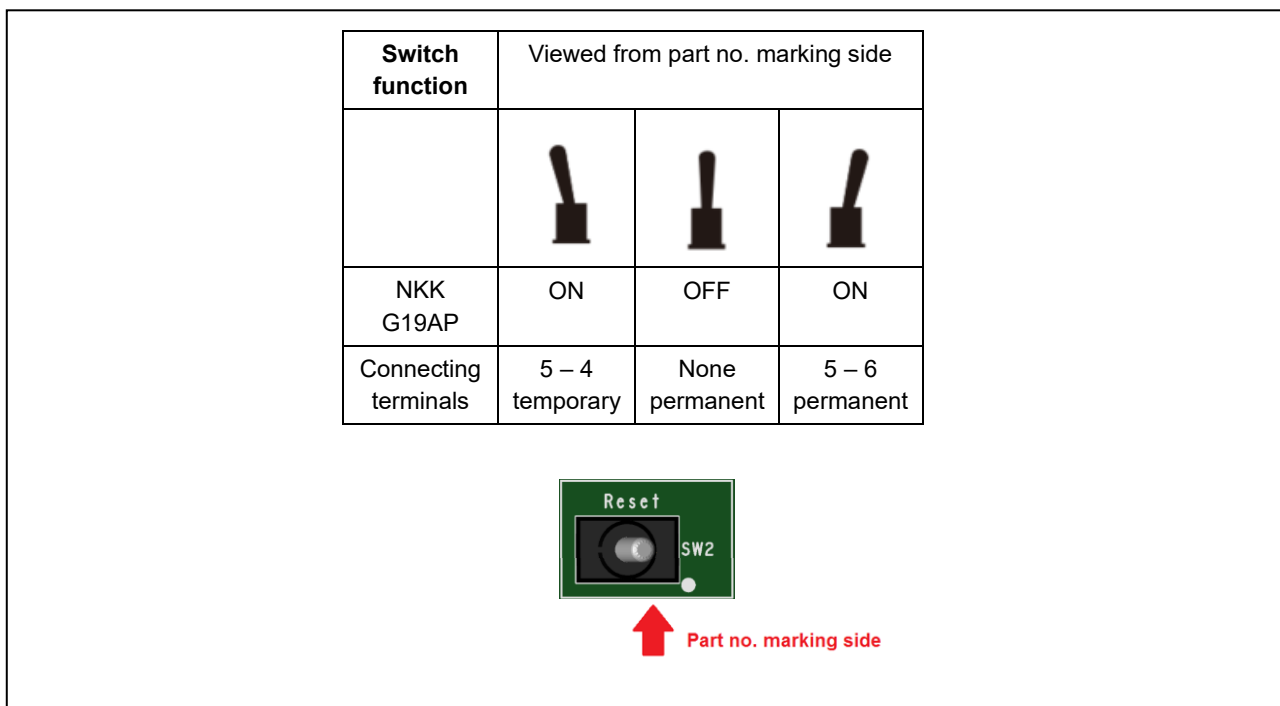


Figure 6.3 Operation of RESET switch

6.3 Port P20_0 Selection

Port P20_0 can be used for I2SMCLK, ETH0RXD0, or ENC0 signal to an attached main board.

Jumper JP17 and jumper JP23 are used to select which signal is being used.

Figure 6.4 shows the circuit diagram for the port function selection.

Table 6.2 shows the summary of the jumper setting.

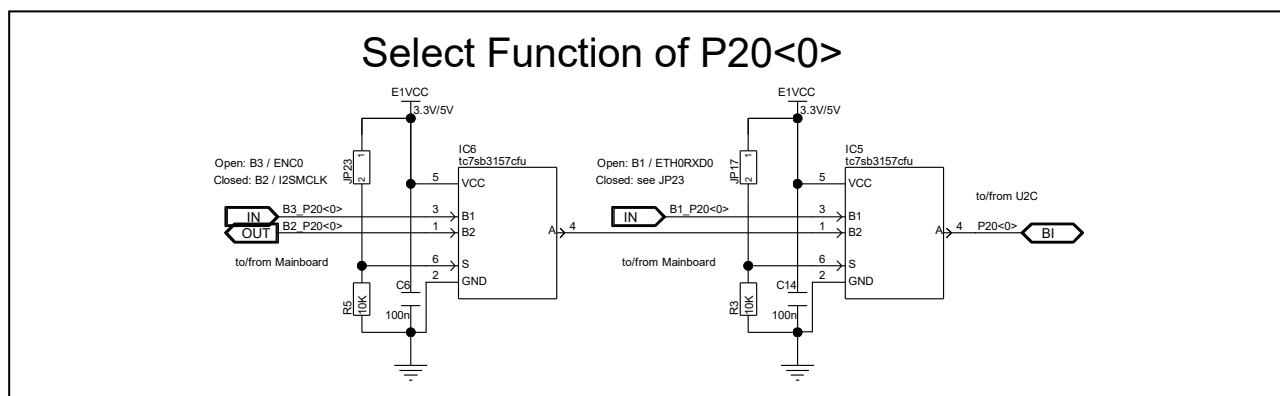


Figure 6.4 Circuit diagram for P20_0 signal selection

Table 6.2 Port P20_0 function selection jumper

Jumper	Function
JP17 [OPEN]	P20_0 = ETH0RXD0
JP17 [CLOSED]	Function selected by jumper JP23 <ul style="list-style-type: none"> JP23[OPEN] : P20_0 = ENC0 JP23[CLOSED] : P20_0 = I2SMCLK

6.4 CAN XL Ports

RH850/U2C has 2 CAN XL interfaces, that can be used with CAN XL modules mounted on a connected main board (Y-COMMON-MB-T1-V1).

On board version D020647_06_V01 these ports are, only separated by termination resistors, connected to many other peripherals like

- Motor control circuits
- SFMA interface
- MMCA interface
- I2S interface
- FlexRay interface

These connections, including the necessary wiring on the pcb, may affect the CAN XL signals. To avoid such interferences the CAN XL signal are separated from the other peripheral circuits.

On board version D020647_06_V01 separation is done using serial resistors.

On board version D020647_06_V02 separation is done by multiplexers. The jumpers JP22 (CANXL0) and JP23 (CANXL1) control the multiplexers.

Figure 6.5 shows the switches that are used to separate the CAN XL signals from other peripheral circuits.

Table 6.3 lists the port connections for different jumper settings.

Table 6.3 Connections for ports P17_2 / P17_3 and P24_7 / P24_8

RH850 Port	Jumper Setting	Signal Name	Connector
P17_2	JP22[OPEN]	CANXL0RX	CN1_73
	JP22[CLOSED]	SFMA0IO1 / MOT0V_P / I2S1RXD	CN2_82 / CN3_87 / CN3_14
P17_3	JP22[OPEN]	CANXL0TX	CN1_71
	JP22[CLOSED]	SFMA0IO0 / MOT0V_N / I2S1TXD	CN2_81 / CN3_89 / CN3_12
P24_7	JP23[OPEN]	CANXL1TX	CN1_72
	JP23[CLOSED]	MMCA0DAT3 / FLX1TX	CN2_92 / CN1_45
P24_8	JP23[OPEN]	CANXL1RX	CN1_74
	JP23[CLOSED]	MMCA0CLK / FLX1RX	CN2_87 / CN1_47

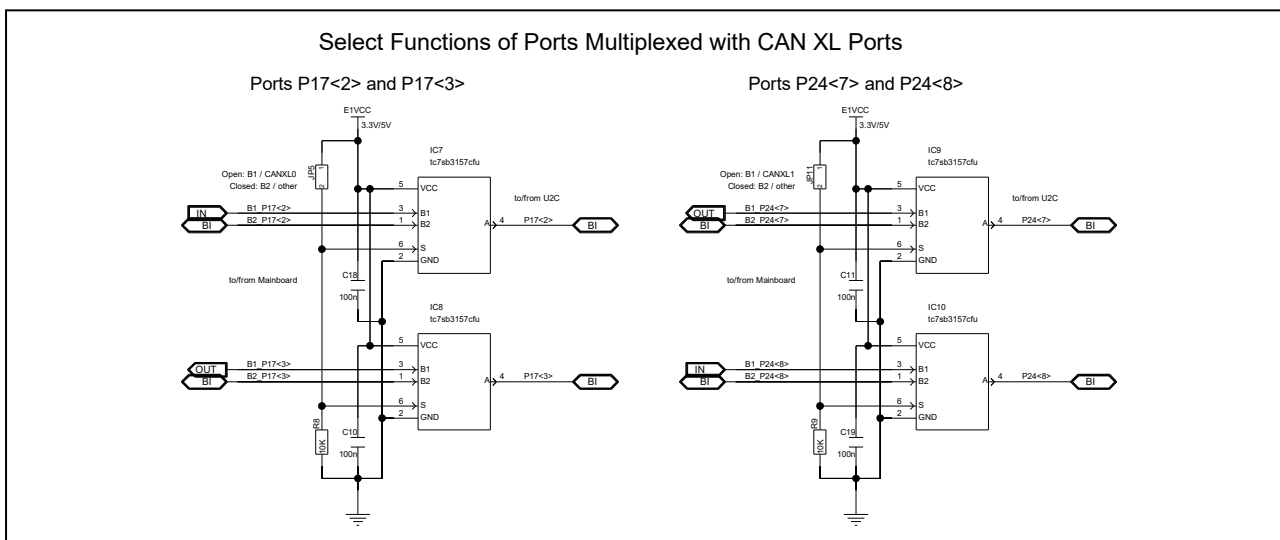


Figure 6.5 CAN XL port selection on board version and D020647_06_V02

6.5 Series Resistors

The piggyback board includes several series resistors, that can be used as termination resistors for the Ethernet channel ETH0 (R1, R4, R12, R14, R15), or for decoupling the CAN XL signals from signals for other functions (e.g. FLX1, SFMA0, I2S1) sharing the same ports (R8 – R11).

On board version D020647_06_V02 the resistors R8 – R11 have been replaced by multiplexers (see chapter 6.4 CAN XL Ports).

Table 6.4 lists all resistors and shows to which signal on the main board connector they are connected.

Figure 6.6 shows the circuit diagrams for the series resistors.

Figure 6.7 shows the location of the resistors on the piggyback board. These positions apply to all board versions, except that board version D020746_06_V02 does not have resistors R8 – R11.

Table 6.4 Series resistors

Resistor	RH850 Port		Main Board	
	Port	Signal Name	Connector	Signal Name
R8 *	P24_7	CANXL1TX	CN1_72 CN1_45 / CN1_103 / CN2_33 / CN2_92	CANXL1TX FLX1TX / MUX0 / LIN14TX / MMCA0DAT3
R9 *	P24_8	CANXL1RX	CN1_74 CN1_47 / CN2_35 / CN2_87	CANXL1RX FLX1RX / LIN14RX / MMCA0CLK
R10 *	P17_2	CANXL0RX	CN1_73 CN2_82 / CN3_14 / CN3_87	CANXL0RX SFMA0IO1 / I2S1RXD / MOT0V_P
R11 *	P17_3	CANXL0TX	CN1_71 CN2_81 / CN3_12 / CN3_89	CANXL0TX SFMA0IO0 / I2S1TXD / MOT0V_N
R1	P21_2	TXD0	CN1_54	ETH0TXD0
R4	P21_3	TXD1	CN1_56	ETH0TXD1
R12	P20_5	TX_EN	CN1_66	ETH0TXEN
R14	P22_0	MDC	CN1_52	ETH0MDC
R15	P22_1	MDIO	CN1_44	ETH0MDIO

* Only for board versions D020647_06_V01

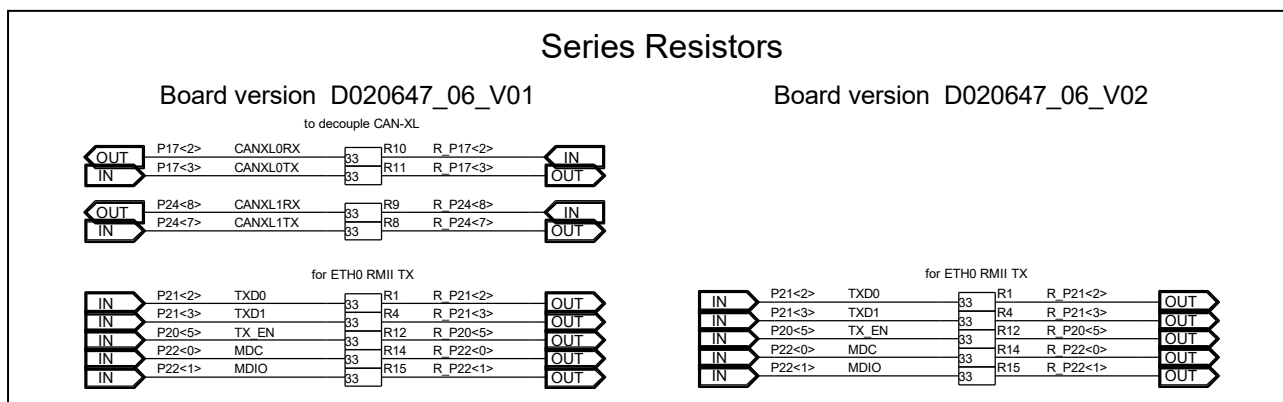


Figure 6.6 Series resistors

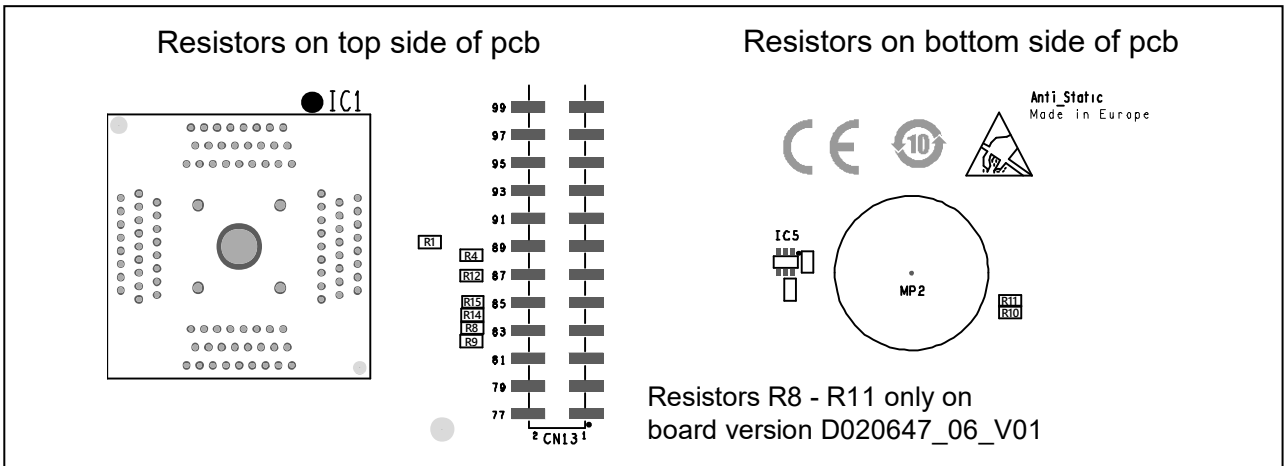


Figure 6.7 Series resistor placement

6.6 Signal LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

The device pins P06_0 – P06_7 are connected to the even pins of the jumper JP20.

The LEDs LED10 to LED17 are connected to the odd JP20 pins.

Thus, the LEDs can be either connected to

- the device port pins P06_0 – P06_7 by closing the corresponding jumper on JP20.
- any device pin by connecting the pin (from the connectors CN4, CN10, CN11, and CN13) directly with the odd JP20 pins using a separate cable.

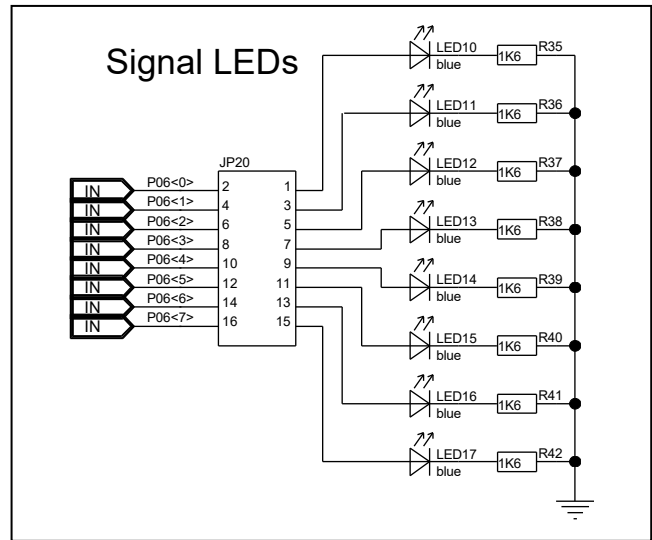


Figure 6.8 Circuit diagram for signalling LEDs

6.7 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN12 provides fixed voltage levels at its pins, that can be used to pull-up/pull-down a signal on the board or the device, respectively, by connecting a CN12 pin to the signal via a separate cable.

The CN12 pins have following pull-up or pull-down voltage levels:

- All even numbered pins are connected to L level, i.e. to GND.
- Odd numbered pins 1, 3, 5 and 7 are connected to jumper JP15 and can be pulled up to 3.3V or 5.0V.
- Odd numbered pins 9, 11, 13 and 15 are connected to jumper JP14 and can be pulled up to 3.3V or 5.0V.

Refer to 7.4 Pull-Up/Pull-Down Pin Header CN12 for CN12 details.

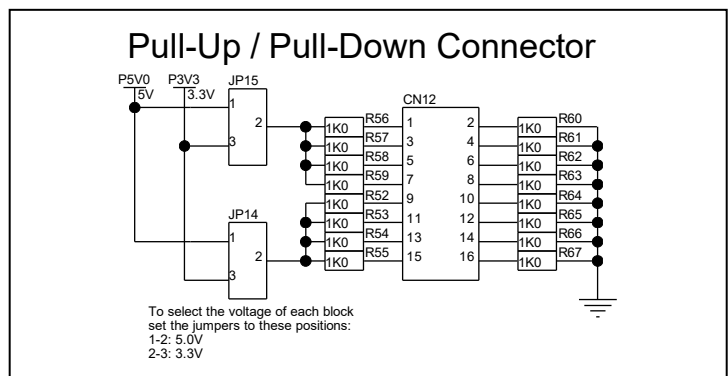


Figure 6.9 Circuit diagram for pull up / pull down signals

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a main board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the main board, please refer to the User's Manual of any supported main board.

Refer to 1.2 *Supported Main Boards* for a list of supported main boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Function on		Device port
	Main Board	Piggyback	
1	VDDA	–	–
3	VDDA	–	–
5	RESET	RESET#	RESET#
7	WAKE	–	–
9	INT0	IRQ27	P06_12
11	INT2	IRQ16	P06_13
13	–	–	–
15	UART0TX	RLIN33TX	P06_3
17	UART0RX	RLIN33RX	P06_2
19	LIN0TX	RLIN30TX	P06_6
21	LIN0RX	RLIN30RX	P06_7
23	IIC0SCL	RI3C2SCL	P24_11
25	IIC0SDA	RI3C2SDA	P24_12
27	CAN0TX	CAN0TX	P02_2
29	CAN0RX	CAN0RX	P02_0
31	SENT0RX	RSENT6RX	P06_13
33	SENT0SPCO	RSENT6SPCO	P06_12
35	PSI5SRX0	–	–
37	PSI5STX0	–	–
39	PSI5SCLK0	–	–
41	FLX0TX	FLXA0TXDA *1	P24_12
43	FLX0RX	FLXA0RXDA *1	P24_11
45	FLX1TX	FLXA0TXDB *1	R_P24_7 *2 B2_P24_7 *3

Pin	Function on		Device port
	Main Board	Piggyback	
2	VDDA	–	–
4	VDDA	–	–
6	NMI	NMI	P02_3
8	–	–	–
10	INT1	IRQ25	P02_0
12	INT3	IRQ20	P06_7
14	–	–	–
16	UART1TX	RLIN36TX	P04_15
18	UART1RX	RLIN36RX	P04_14
20	LIN1TX	RLIN31TX	P06_4
22	LIN1RX	RLIN31RX	P06_5
24	IIC1SCL	RI3C1SCL	P06_8
26	IIC1SDA	RI3C1SDA	P06_9
28	CAN1TX	CAN1TX	P17_4
30	CAN1RX	CAN1RX	P17_5
32	SENT1RX	RSENT5RX	P04_14
34	SENT1SPCO	RSENT5SPCO	P04_15
36	PSI5RX0	–	–
38	PSI5TX0	–	–
40	–	–	–
42	FLX0EN	FLXA0TXENA *1	P24_10
44	FLXSTPWT	FLXA0STPWT *1	R_P22_1
46	FLX1EN	FLXA0TXENB *1	P24_9

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
47	FLX1RX	FLXA0RXDB *1	R_P24_8 *2 B2_P24_8 *3
49	–	–	–
51	ETH0MDIO	ETH0_MDIO *1	R_P22_1
53	ETH0RXD0	ETH0_MII_RXD0 *1	B1_P20_0
55	ETH0RXD1	ETH0_MII_RXD1 *1	P20_1
57	ETH0RXD2	–	–
59	ETH0RXD3	–	–
61	ETH0RXCLK	–	–
63	ETH0RXER	ETH0_RMII_ER *1	P20_12
65	ETH0CRSDV	–	–
67	ETH0RXDV	ETH0_MII_RX_DV *1	P20_2
69	ETH0RESET	P17_0	P17_0
71	CANXL0TX	CANXL0TXD	P17_3 *2 B1_P17_3 *3
73	CANXL0RX	CANXL0RXD	P17_2 *2 B1_P17_2 *3
75	CANXL2TX	–	–
77	CANXL2RX	–	–
79	ETH0_T1S_TX	ETS0_TX *1	P20_4
81	ETH0_T1S_RX_MDC	ETS0_RX_MDC *1	P20_3
83	ETH0_T1S_ED_MDIO	ETS0_ED_MDIO *1	P20_13
85	DIGIO_0	P06_10	P06_10
87	DIGIO_2	P06_12	P06_12
89	DIGIO_4	P21_0	P21_0
91	DIGIO_6	–	–
93	DIGIO_8	–	–
95	DIGIO_10	–	–
97	DIGIO_12	–	–
99	DIGIO_14	P06_3	P06_3
101	–	–	–
103	MUX0	P24_7	R_P24_7 *2 B2_P24_7 *3
105	MUX2	P22_3	P22_3
107	ADC0	ADCK1112	AP2_12
109	ADC2	ADCK1114	AP2_14

Pin	Function on		Device port
	Main Board	Piggyback	
48	FLX1CLK	–	–
50	–	–	–
52	ETH0MDC	ETH0_MDC *1	R_P22_0
54	ETH0TXD0	ETH0_MII_TXD0 *1	R_P21_2
56	ETH0TXD1	ETH0_MII_TXD1 *1	R_P21_3
58	ETH0TXD2	–	–
60	ETH0TXD3	–	–
62	ETH0TXCLK	ETH0_MII_TX_CLK *1	P21_1
64	ETH0TXER	–	–
66	ETH0TXEN	ETH0_MII_TX_EN *1	R_P20_5
68	ETH0COL	–	–
70	ETH0LINK	ETH0_LINKSTA *1	P22_2
72	CANXL1TX	CANXL1TXD *1	P24_7 *2 B1_P24_7 *3
74	CANXL1RX	CANXL1RXD *1	P24_8 *2 B1_P24_8 *3
76	CANXL3TX	–	–
78	CANXL3RX	–	–
80	ETH1_T1S_TX	–	–
82	ETH1_T1S_RX_MDC	–	–
84	ETH1_T1S_ED_MDIO	–	–
86	DIGIO_1	P06_11	P06_11
88	DIGIO_3	P06_13	P06_13
90	DIGIO_5	–	–
92	DIGIO_7	–	–
94	DIGIO_9	–	–
96	DIGIO_11	–	–
98	DIGIO_13	P06_2	P06_2
100	DIGIO_15	P06_4	P06_4
102	–	–	–
104	MUX1	P22_2	P22_2
106	–	–	–
108	ADC1	ADCK1113	AP2_13
110	ADC3	–	–

Table 7.1 Main board connector CN1 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
111	ADC4	–	–
113	ADC6	–	–
115	VDDIOF	VDDIOF	–
117	VDDDB	P3V3_MB	–
119	VDDDB	P3V3_MB	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

*1 Only RH850/U2C4

*2 Board version D020647_06_V01

*3 Board version D020647_06_V02 and later

Pin	Function on		Device port
	Main Board	Piggyback	
112	ADC5	–	–
114	ADC7	–	–
116	VDDIOF	VDDIOF	–
118	VDDDB	P3V3_MB	–
120	VDDDB	P3V3_MB	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function on		Device port
	Main Board	Piggyback	
1	CAN2TX	CAN2TX	P06_0
3	CAN2RX	CAN2RX	P06_1
5	CAN4TX	–	–
7	CAN4RX	–	–
9	LIN2TX	RLIN32TX	P06_0
11	LIN2RX	RLIN32RX	P06_1
13	LIN4TX	RLIN34TX	P06_11
15	LIN4RX	RLIN34RX	P06_10
17	LIN6TX	RLIN36TX	P04_15
19	LIN6RX	RLIN36RX	P04_14
21	LIN8TX	RLIN38TX	P02_1
23	LIN8RX	RLIN38RX	P02_0
25	LIN10TX	RLIN310TX	P06_12
27	LIN10RX	RLIN310RX	P06_13
29	LIN12TX	–	–
31	LIN12RX	–	–
33	LIN14TX	P24_7	R_P24_7 ^{*2} B2_P24_7 ^{*3}
35	LIN14RX	P24_8	R_P24_8 ^{*2} B2_P24_8 ^{*3}

Pin	Function on		Device port
	Main Board	Piggyback	
2	CAN3TX	CAN3TX	P06_4
4	CAN3RX	CAN3RX	P06_5
6	CAN5TX	–	–
8	CAN5RX	–	–
10	LIN3TX	RLIN33TX	P06_3
12	LIN3RX	RLIN33RX	P06_2
14	LIN5TX	RLIN35TX	P24_12
16	LIN5RX	RLIN35RX	P24_11
18	LIN7TX	RLIN37TX	P02_3
20	LIN7RX	RLIN37RX	P02_2
22	LIN9TX	RLIN39TX	P02_6
24	LIN9RX	RLIN39RX	P02_5
26	LIN11TX	RLIN311TX ^{*1}	R_P22_1
28	LIN11RX	RLIN311RX ^{*1}	R_P22_0
30	LIN13TX	–	–
32	LIN13RX	–	–
34	LIN15TX	–	–
36	LIN15RX	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
37	–	–	–
39	CAN12TX	–	–
41	CAN12RX	–	–
43	CAN14TX	–	–
45	CAN14RX	–	–
47	CAN6TX	–	–
49	CAN6RX	–	–
51	CAN8TX	–	–
53	CAN8RX	–	–
55	CAN10TX	–	–
57	CAN10RX	–	–
59	–	–	–
61	LIN16TX	–	–
63	LIN16RX	–	–
65	LIN18TX	–	–
67	LIN18RX	–	–
69	LIN20TX	–	–
71	LIN20RX	–	–
73	LIN22TX	–	–
75	LIN22RX	–	–
77	–	–	–
79	SFMA0CLK	SFMA0CLK	P17_5
81	SFMA0IO0	SFMA0IO0	R_P17_3 ^{*2} B2_P17_3 ^{*3}
83	SFMA0IO2	SFMA0IO2	P17_1
85	–	–	–
87	MMCA0CLK	MMCA0CLK ^{*1}	R_P24_8 ^{*2} B2_P24_8 ^{*3}
89	MMCA0DAT0	MMCA0DAT0 ^{*1}	P24_10
91	MMCA0DAT2	MMCA0DAT2 ^{*1}	P24_12
93	MMCA0DAT4	–	–
95	MMCA0DAT6	–	–
97	–	–	–
99	ETH1MDIO	–	–
101	ETH1RXD0	–	–
103	ETH1RXD1	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
38	–	–	–
40	CAN13TX	–	–
42	CAN13RX	–	–
44	CAN15TX	–	–
46	CAN15RX	–	–
48	CAN7TX	–	–
50	CAN7RX	–	–
52	CAN9TX	–	–
54	CAN9RX	–	–
56	CAN11TX	–	–
58	CAN11RX	–	–
60	–	–	–
62	LIN17TX	–	–
64	LIN17RX	–	–
66	LIN19TX	–	–
68	LIN19RX	–	–
70	LIN21TX	–	–
72	LIN21RX	–	–
74	LIN23TX	RLIN323TX	P06_9
76	LIN23RX	RLIN323RX	P06_8
78	–	–	–
80	SFMA0SSL	SFMA0SSL	P17_4
82	SFMA0IO1	SFMA0IO1	R_P17_2 ^{*2} B2_P17_2 ^{*3}
84	SFMA0IO3	SFMA0IO3	P17_0
86	–	–	–
88	MMCA0CMD	MMCA0CMD ^{*1}	P24_9
90	MMCA0DAT1	MMCA0DAT1 ^{*1}	P24_11
92	MMCA0DAT3	MMCA0DAT3 ^{*1}	R_P24_7 ^{*2} B2_P24_7 ^{*3}
94	MMCA0DAT5	–	–
96	MMCA0DAT7	–	–
98	–	–	–
100	ETH1MDC	–	–
102	ETH1TXD0	–	–
104	ETH1TXD1	–	–

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
105	ETH1RXD2	–	–
107	ETH1RXD3	–	–
109	ETH1RXCLK	–	–
111	ETH1RXER	–	–
113	ETH1CRSDV	–	–
115	ETH1RXDV	–	–
117	ETH1RESET	–	–
119	–	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

*1 Only RH850/U2C4

*2 Board version D020647_06_V01

*3 Board version D020647_06_V02 and later

Pin	Function on		Device port
	Main Board	Piggyback	
106	ETH1TXD2	–	–
108	ETH1TXD3	–	–
110	ETH1TXCLK	–	–
112	ETH1TXER	–	–
114	ETH1TXEN	–	–
116	ETH1COL	–	–
118	ETH1LINK	–	–
120	–	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function on		Device port
	Main Board	Piggyback	
1	CSI0CS0	MSPI0CSS0	P06_9
3	CSI0CS1	MSPI0CSS2	P21_0
5	CSI0CS2	MSPI0CSS6	P06_11
7	CSI0CS3	MSPI0CSS7	P06_10
9	–	–	–
11	I2S0TXD	–	–
13	I2S0RXD	–	–
15	I2S0BCLK	–	–
17	I2S0LRCLK	–	–
19	I2S0MCLK	SSIFACK	B2_P20_0
21	CSI1CS2	MSPI1CSS5	R_P22_1
23	–	–	–
25	–	–	–
27	–	–	–
29	CSI1SCLK	MSPI1SC	P02_3
31	–	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
2	CSI0CLK	MSPI0SC	P06_6
4	CSI0SI	MSPI0SI	P06_5
6	CSI0SO	MSPI0SO	P06_7
8	–	–	–
10	CSI1CS1	MSPI1CSS2	P02_6
12	I2S1TXD	SSIF1TXD	R_P17_3 ^{*2} B2_P17_3 ^{*3}
14	I2S1RXD	SSIF1RXD	R_P17_2 ^{*2} B2_P17_2 ^{*3}
16	I2S1BCLK	SSIF1BCK	P17_4
18	I2S1LRCLK	SSIF1LRCK	P17_5
20	–	–	–
22	CSI1CS3	MSPI1CSS6	P22_2
24	CSI1CS0	MSPI1CSS0	P02_2
26	DIGIO_24	P22_3	P22_3
28	CSI1SO	MSPI1SO	P02_5
30	CSI1SI	MSPI1SI	P02_4
32	–	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
33	MOT0ADU	ADCK110	AP2_0
35	MOT0ADV	ADCK111	AP2_1
37	MOT0ADW	ADCK112	AP2_2
39	MOT0RDCS1	ADCK113	AP2_3
41	MOT0RDCS3	ADCK114	AP2_4
43	MOT0RDCS2	ADCK115	AP2_5
45	MOT0RDCS4	ADCK116	AP2_6
47	MOT0RDCCOM	ADCK117	AP2_7
49	MOT0RDCRSO	ADCK118	AP2_8
51	–	–	–
53	–	–	–
55	AD1_0	ADCK119	AP2_9
57	AD1_2	ADCK1111	AP2_11
59	AD1_4	–	–
61	AD1_6	–	–
63	PWM0	PWGC320	P02_0
65	PWM2	PWGC410	P02_2
67	PWM4	PWGC430	P02_4
69	PWM6	PWGC450	P02_6
71	DIGIO16	P06_0	P06_0
73	DIGIO18	P02_0	P02_0
75	DIGIO20	P02_2	P02_2
77	DIGIO22	P24_9	P24_9
79	ENC0	ENCA0E0	B3_P20_0
81	MOT0ERR	–	–
83	MOT0U_P	TSG3001	P17_0
85	MOT0U_N	TSG3002	P17_1
87	MOT0V_P	TSG3003	R_P17_2 ^{*2} B2_P17_2 ^{*3}
89	MOT0V_N	TSG3004	R_P17_3 ^{*2} B2_P17_3 ^{*3}
91	MOT0W_P	TSG3005	P17_4
93	MOT0W_N	TSG3006	P17_5
95	–	–	–
97	–	–	–
99	–	–	–
101	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
34	MOT1ADU	ADCK110	AP2_0
36	MOT1ADV	ADCK111	AP2_1
38	MOT1ADW	ADCK112	AP2_2
40	MOT1RDCS1	ADCK113	AP2_3
42	MOT1RDCS3	ADCK114	AP2_4
44	MOT1RDCS2	ADCK115	AP2_5
46	MOT1RDCS4	ADCK116	AP2_6
48	MOT1RDCCOM	ADCK117	AP2_7
50	MOT1RDCRSO	ADCK118	AP2_8
52	–	–	–
54	–	–	–
56	AD1_1	ADCK1110	AP2_10
58	AD1_3	–	–
60	AD1_5	–	–
62	AD1_7	–	–
64	PWM1	PWGC330	P02_1
66	PWM3	PWGC420	P02_3
68	PWM5	PWGC440	P02_5
70	PWM7	PWGC210	P21_0
72	DIGIO17	P22_2	P22_2
74	DIGIO19	P02_1	P02_1
76	DIGIO21	P02_6	P02_6
78	DIGIO23	P24_10	P24_10
80	ENC1	ENCA0E1	P06_0
82	MOT1ERR	TAPA0ESO	P06_6
84	MOT1U_P	TAPA0UP	P06_1
86	MOT1U_N	TAPA0UN	P06_0
88	MOT1V_P	TAPA0VP	P06_5
90	MOT1V_N	TAPA0VN	P06_4
92	MOT1W_P	TAPA0WP	P06_3
94	MOT1W_N	TAPA0WN	P06_2
96	–	–	–
98	–	–	–
100	ETH0_SO_P	–	–
102	ETH0_SO_N	–	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function on		Device port
	Main Board	Piggyback	
103	AD2_0	ADCKAI0	AP0_0
105	AD2_1	ADCKAI1	AP0_1
107	AD2_2	ADCKAI2	AP0_2
109	AD2_3	ADCKAI3	AP0_3
111	AD2_4	–	–
113	AD2_5	–	–
115	AD2_6	–	–
117	AD2_7	–	–
119	GND	–	–
121	GND	–	–
123	GND	–	–
125	GND	–	–
127	GND	–	–

Pin	Function on		Device port
	Main Board	Piggyback	
104	–	–	–
106	ETH0_SI_P	–	–
108	ETH0_SI_N	–	–
110	–	–	–
112	ETH1_SO_P	–	–
114	ETH1_SO_N	–	–
116	–	–	–
118	ETH1_SI_P	–	–
120	ETH1_SI_N	–	–
122	GND	–	–
124	GND	–	–
126	GND	–	–
128	GND	–	–

*1 Only RH850/U2C4

*2 Board version D020647_06_V01

*3 Board version D020647_06_V02 and later

7.2 Device Ports Connectors CN4, CN10, CN11 and CN13

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.2.1 Device Ports Connector CN4

Table 7.4 Device ports connector CN4

Connector pin	Device pin	Device port
1	1	P10_0
3	3	P17_1
5	5	P17_3
7	7	P17_5
9	9	AP2_14
11	11	AP2_12
13	13	AP2_10
15	15	AP2_8
17	17	AP2_6

Connector pin	Device pin	Device port
2	2	P17_0
4	4	P17_2
6	6	P17_4
8	8	VDD
10	10	AP2_13
12	12	AP2_11
14	14	AP2_9
16	16	AP2_7
18	18	AP2_5

Table 7.4 Device ports connector CN4 (cont'd)

Connector pin	Device pin	Device port
19	19	AP2_4
21	21	AP2_2
23	23	AP2_0
25	25	GND

Connector pin	Device pin	Device port
20	20	AP2_3
22	22	AP2_1
24	24	A1VREFH
26	–	GND

7.2.2 Device Ports Connector CN10

Table 7.5 Device ports connector CN10

Connector pin	Device pin	Device port
1	26	AAVREFH
3	28	AP0_0
5	30	AP0_2
7	32	P06_13
9	34	P06_11
11	36	P06_9
13	38	P06_7
15	40	P06_5
17	42	P06_4
19	44	P06_2
21	46	E0VCC
23	48	VCC
25	50	P04_15

Connector pin	Device pin	Device port
2	27	GND
4	29	AP0_1
6	31	AP0_3
8	33	P06_12
10	35	P06_10
12	37	P06_8
14	39	P06_6
16	41	VCC
18	43	P06_3
20	45	P06_1
22	47	P06_0
24	49	P04_14
26	–	GND

7.2.3 Device Ports Connector CN11

Table 7.6 Device ports connector CN11

Connector pin	Device pin	Device port
1	51	P02_6
3	53	P02_4
5	55	E0VCC
7	57	VDD
9	59	P02_0
11	61	JP0_5
13	63	JP0_2
15	65	JP0_0
17	67	RESET#
19	69	X2_CN
21	71	SYSVCC

Connector pin	Device pin	Device port
2	52	P02_5
4	54	P02_3
6	56	RESETOUT#
8	58	P02_1
10	60	P02_2
12	62	JP0_3
14	64	JP0_1
16	66	TRST#
18	68	VDD
20	70	X1_CN
22	72	AWOVCL

Table 7.6 Device ports connector CN11 (cont'd)

Connector pin	Device pin	Device port
23	73	FLMD0
25	75	ERROROUT_M#

Connector pin	Device pin	Device port
24	74	GND
66	–	GND

7.2.4 Device Ports Connector CN13

Table 7.7 Device ports connector CN13

Connector pin	Device pin	Device port
1	76	P24_12
3	78	P24_10
5	80	P24_8
7	82	R_P22_0
9	84	P22_2
11	86	R_P20_5
13	88	VCC
15	90	R_P21_2
17	82	P21_0
19	94	P20_12
21	96	P20_4
23	98	P20_2
25	100	P20_0

Connector pin	Device pin	Device port
2	77	P24_11
4	79	P24_9
6	81	P24_7
8	83	R_P22_1
10	85	P22_3
12	87	VDD
14	89	R_P21_3
16	91	P21_1
18	93	P20_13
20	95	E1VCC
22	97	P20_3
24	99	P20_1
26	–	GND

7.3 Debug Connector CN9

Table 7.8 On-chip debug connector CN9

Pin	Function	Device port
1	TCK / LPDCLK / FPCK	JP0_2
3	TRST	TRST#_TOOL
5	TDO / LPDO / FPDT	JP0_1
7	TDI / LPDI / FPDR	JP0_0
9	TMS	JP0_3
11	RDY / LPDCLKO	JP0_5
13	RESET	RESET#

Pin	Function	Device port
2	GND	GND
4	FPMD0	FLMD0_TOOL
6	FPMD1	–
8	TVDD	E0VCC
10	EVTO	EVTO0#_TOOL
12	GND	GND
14	GND	GND

7.4 Pull-Up/Pull-Down Pin Header CN12

Table 7.9 Pull-up and pull-down signal connector CN12

Pin	Function	Pin	Function
1	Level set by jumper JP15: JP15 [1-2]: 5.0 V (P5V0) JP15 [2-3]: 3.3 V (P3V3)	2	Fixed "L" level
3			
5			
7			
9	Level set by jumper JP14: JP14 [1-2]: 5.0 V (P5V0) JP14 [2-3]: 3.3 V (P3V3)	6	
11			
13			
15			
		8	
		10	
		12	
		14	
		16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.

The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings that allow to operate the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool can provide sufficient current on the power supply rails to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Configuration Examples

8.2.1 General Settings

All of the following board configurations are based on these conditions:

- Normal device operation mode (JP7[OPEN]: FLMD0 = L).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN5 (GND), CN6 (+5.0 V) and CN7 (+3.3 V) are assembled on the board.
- If also the core supply voltage of 1.09 V is supplied from an external power supply the connector CN8 (included in the package) has to be assembled on the pcb.





8.2.2 Jumper Indicators

The **green** jumper JP7 for FLMD0 must always be open for 'normal' (user mode and debug) operation of the device.

The **yellow** jumper JP19 is ONLY for board production test and must stay open.

The **red** jumpers are related to the power supply configuration.

Following jumper symbols are used:

- : Jumper must not be set.
- : Jumper must be set in the indicated position
- : Jumper can be set to position [1-2] or position [2-3]
- : Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.2.3 Core Voltage Supply for eVR and DPS Devices

RH850/U2C devices are available with different core voltage supply:

- Devices with embedded voltage regulator (eVR device)
- Devices with external core voltage supply (DPS device)

The jumper configurations in the following chapters show separate jumper settings for eVR and DPS devices.

8.2.4 Stand-Alone Operation with Single External Power Supply 3.3 V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is generated using the on-board voltage regulator IC3. All I/O ports can only use 3.3 V.

Table 8.1 Power supply connectors for single power supply 3.3 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Not connected	Jumpers in JP1 (VCC and VREF selection) are set to 3.3 V position.
CN7	3.3 V	Connected, +3.3 V	
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]). DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP3[2-3] = SHORT). Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

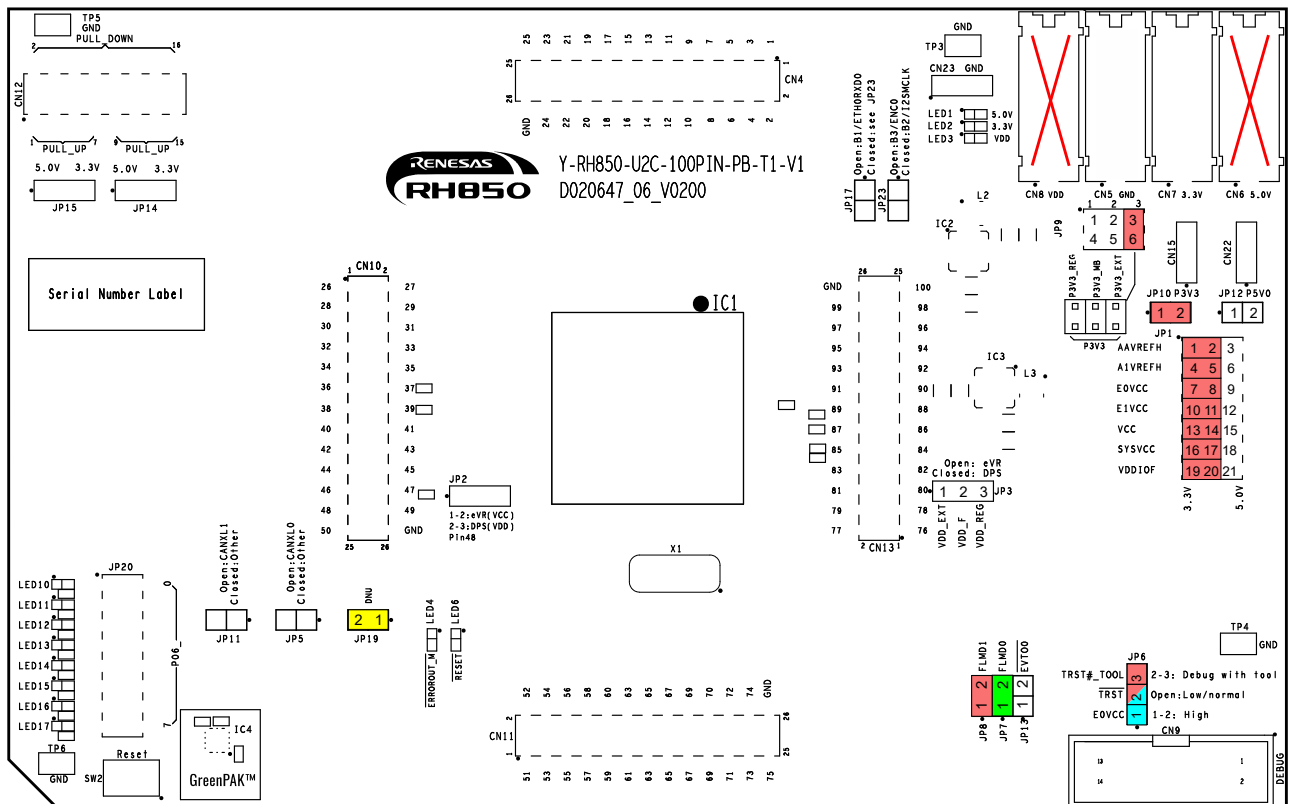


Figure 8.1 Stand-alone operation with 3.3 V external power supply for eVR device

8.2.5 Stand-Alone Operation with Single External Power Supply 5.0 V: Minimum Configuration 2

This example enables to operate the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board.

Table 8.2 Power supply connectors for single power supply 5.0 V

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	
CN7	3.3 V	Not connected	3.3 V supply (P3V3) from on-board voltage regulator IC2 (JP9[1-4] = SHORT).
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]). DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP2[2-3] = SHORT). Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

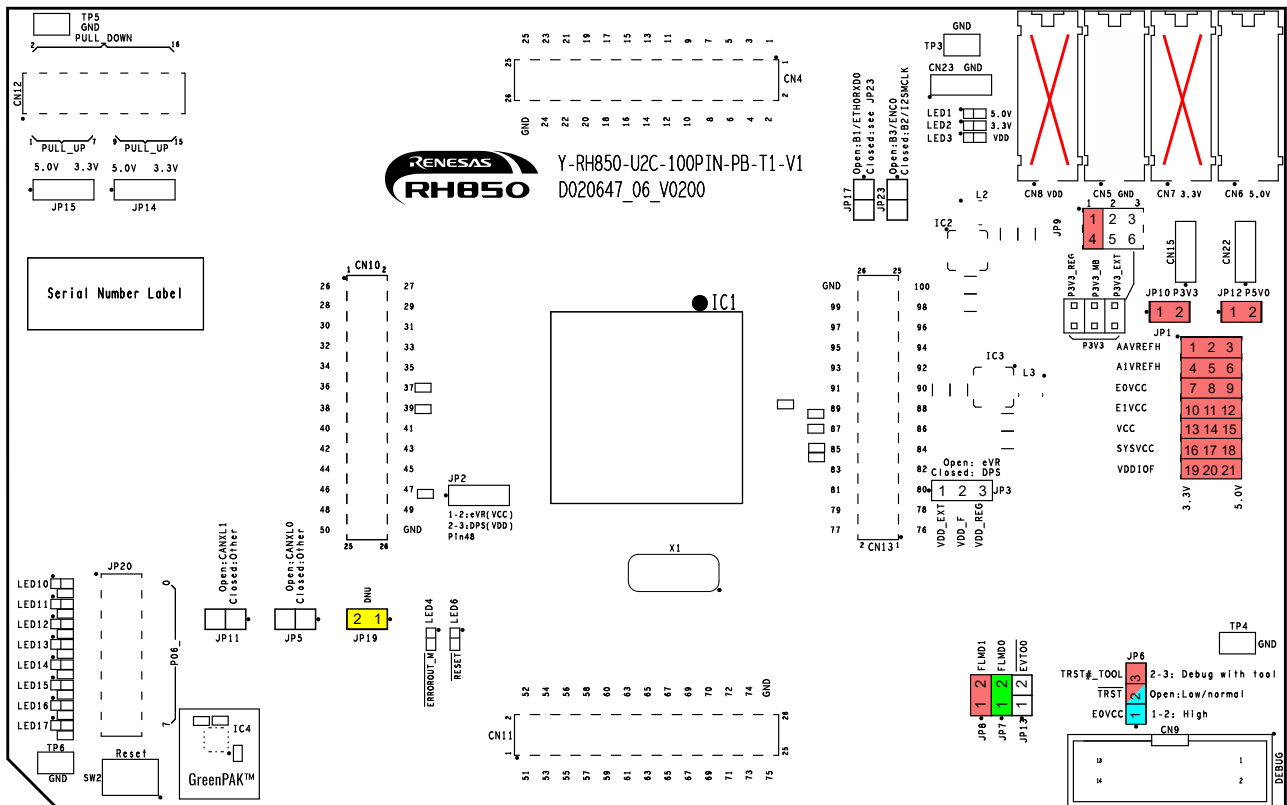


Figure 8.3 Stand-alone operation with 5.0 V external power supply for eVR device

8.2.6 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.3 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Connected, GND	
CN6	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to 3.2 Voltage Distribution for details on possible settings of jumpers in JP1.
CN7	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. JP9[3-6] = SHORT: use P3V3_EXT supply for 3.3 V supply. Refer to 3.2 Voltage Distribution for details on possible settings of jumpers in JP1.
CN8	1.09 V	Connected, 1.09 V	eVR device: VDD from internal voltage regulator (JP3[OPEN]) DPS device: VDD from external VDD supply (P1V09_EXT) (JP3[1-2] = SHORT) Refer to 3.3 Device Core Voltage (VDD) Selection for further details about VDD voltage.

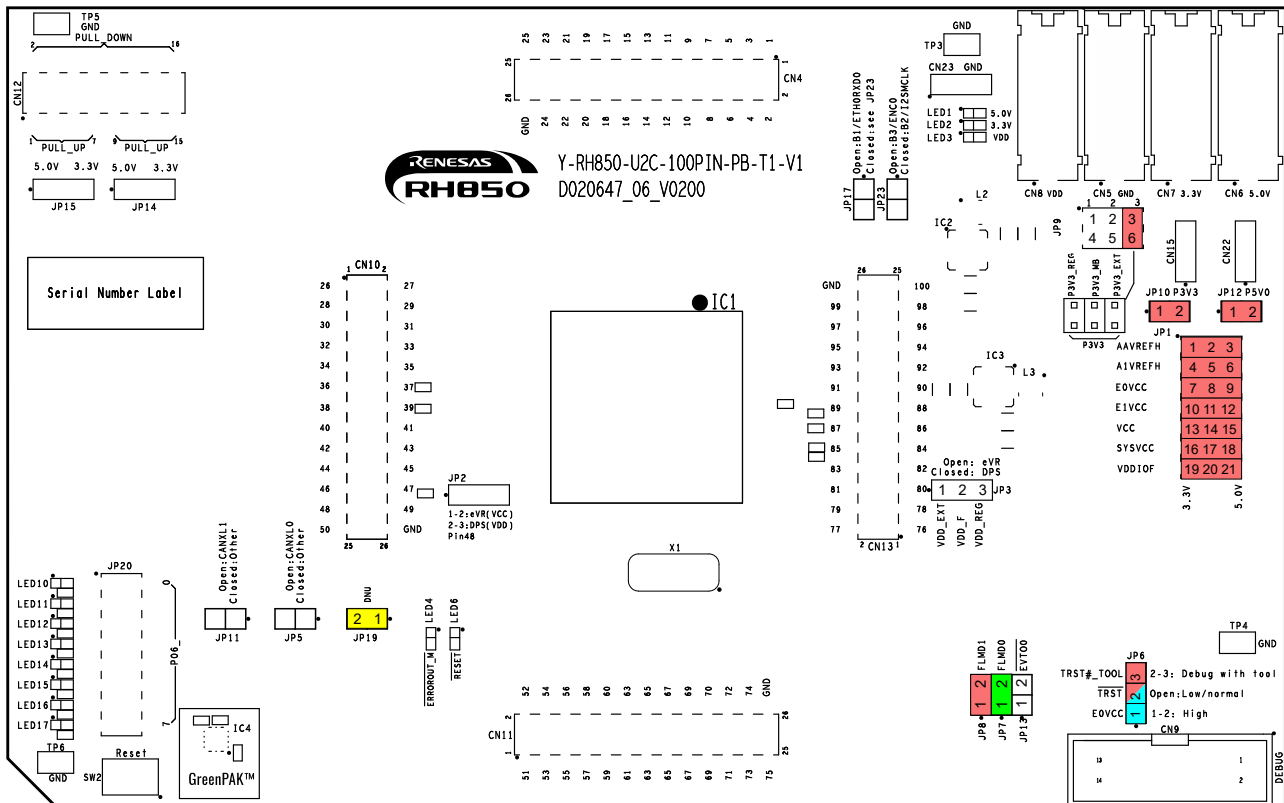


Figure 8.5 Stand-alone operation with all external power supplies for eVR device

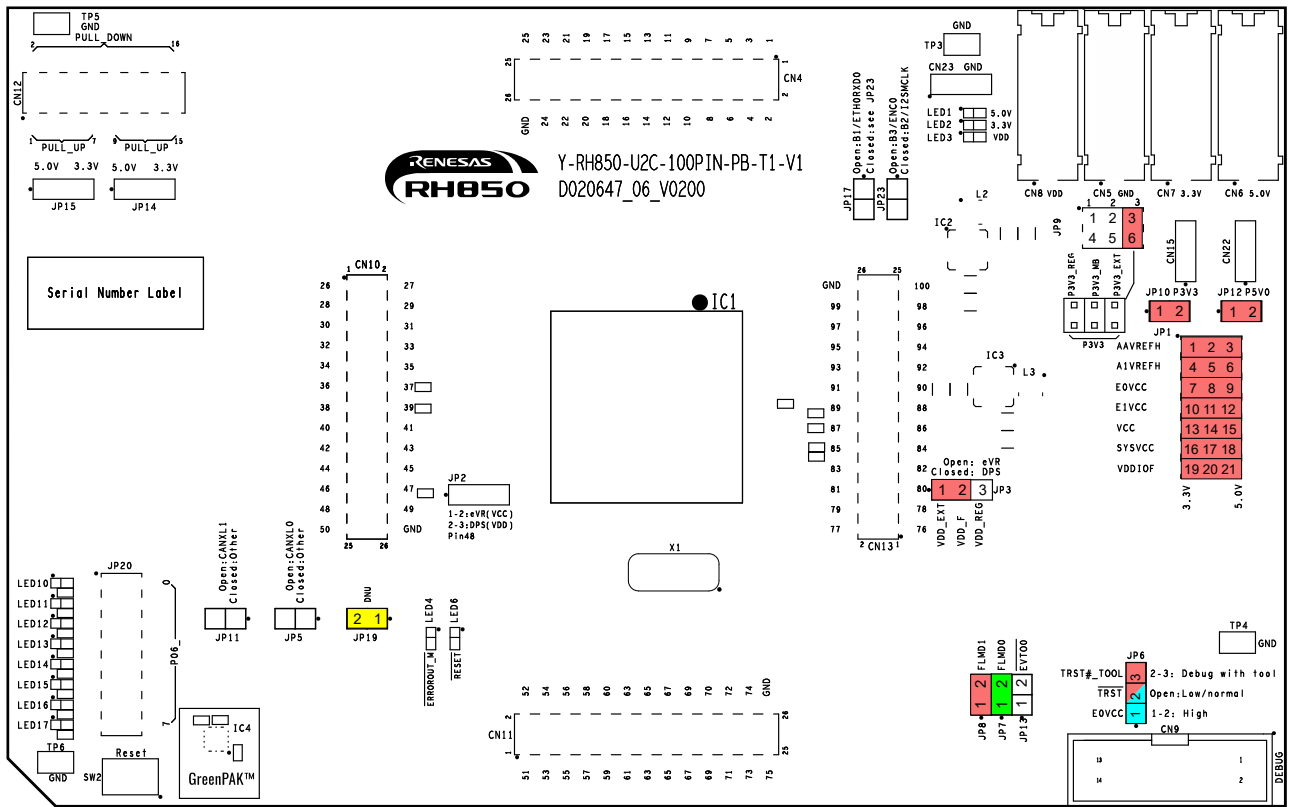


Figure 8.6 Stand-alone operation with all external power supplies for DPS device

8.2.7 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which provides 3.3 V and 5.0 V.

The jumpers JP9 (P3V3) must be set to connect the main board supply voltage P3V3_MB to the piggyback board power supply rail P3V3.

The 5.0 V supply from the main board is always connected to the P5V0 power rail on the piggyback board.

Do not supply the 5.0 V (CN9) and 3.3 V (CN7) voltage directly to the piggyback board.

Table 8.4 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN5	GND	Not connected	
CN6	5.0 V	Not connected	The 5.0 V supply from the main board is connected to the P5V0 power rail on the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to 3.2 <i>Voltage Distribution</i> for details on possible settings of jumpers in JP1.
CN7	3.3 V	Not connected	Use jumper JP9[2-5] to connect the 3.3 V supply from the main board to the piggyback board. Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP1. Refer to 3.2 <i>Voltage Distribution</i> for details on possible settings of jumpers in JP1.
CN8	1.09 V	Not connected	eVR device: VDD from internal voltage regulator (JP3[OPEN]) DPS device: VDD from on-board voltage regulator IC3 (P1V09_REG) (JP3[2-3] = SHORT) Refer to 3.3 <i>Device Core Voltage (VDD) Selection</i> for further details about VDD voltage.

Note

For DPS devices this configuration still allows to utilize an external P1V09_EXT voltage (connected to CN8) as the source for VDD voltage. When using external VDD make sure to set jumper JP3[1-2] = SHORT to use external VDD.

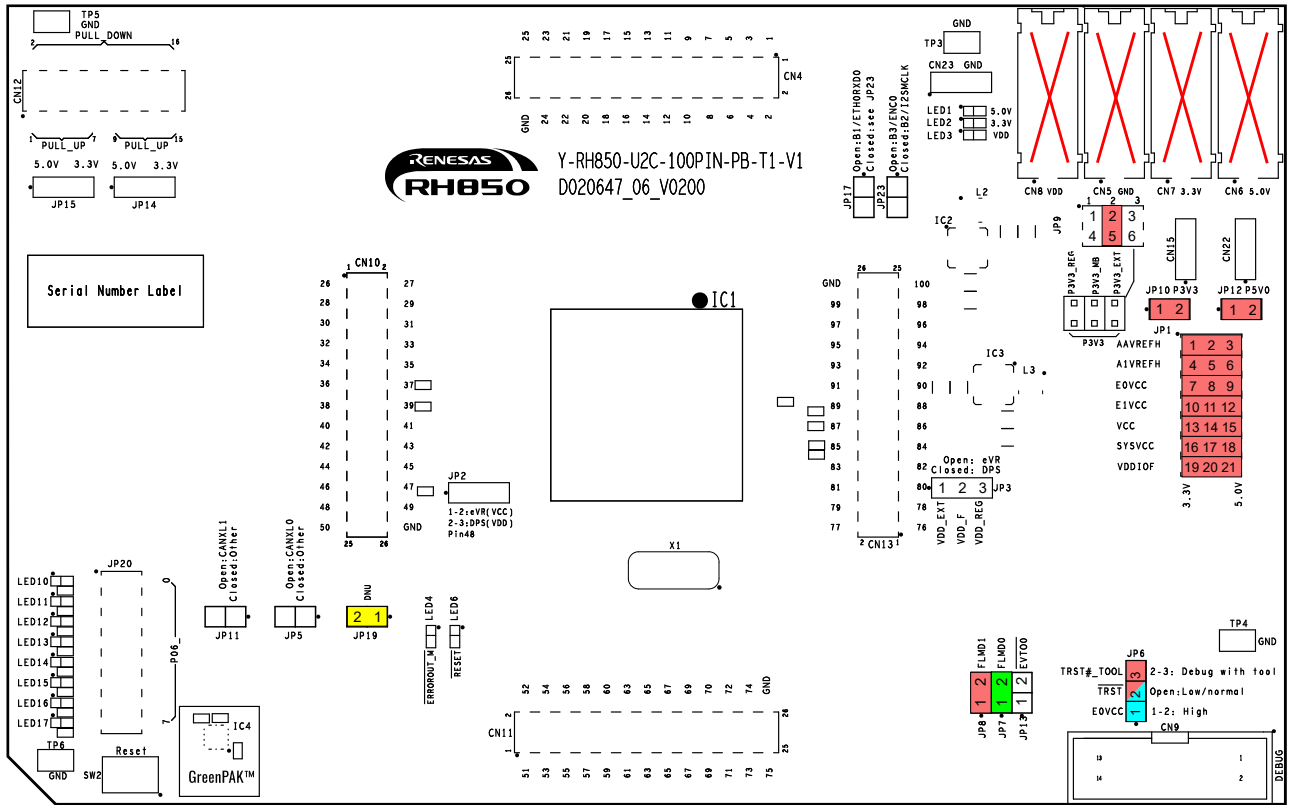


Figure 8.7 Main board operation without external power supply for eVR device

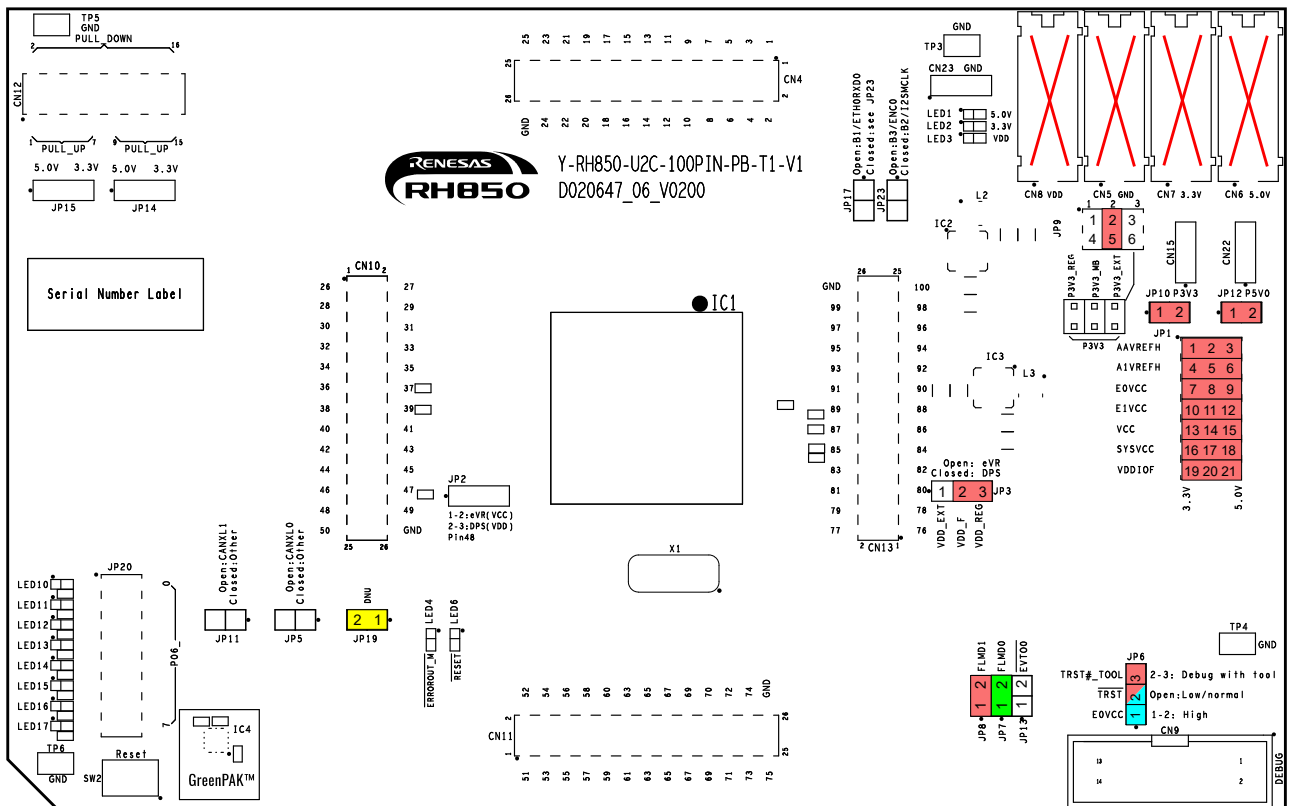


Figure 8.8 Main board operation without external power supply for DPS device

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW2 into '5-6 ON' position, so that RESET is permanently asserted. Alternatively keep SW2 manually in '5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW2 into the 'OFF' position.

For details how to apply a RESET, please refer to *6.2 System State and RESET*.

10. Mechanical Dimensions

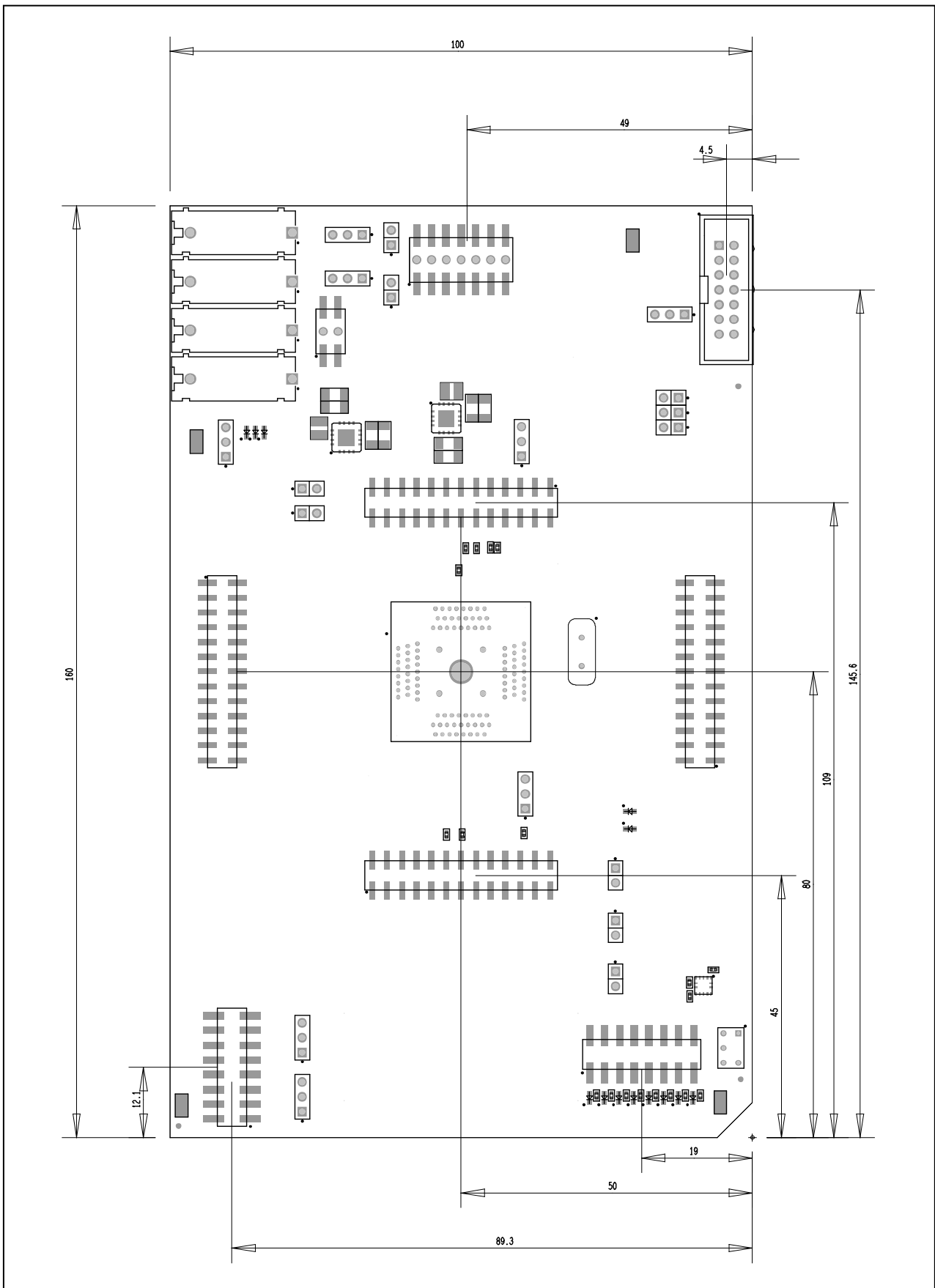


Figure 10.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is in sole responsibility of the customer.

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C32, C37
- Oscillators: OSC1, X2
- Filters: FC1

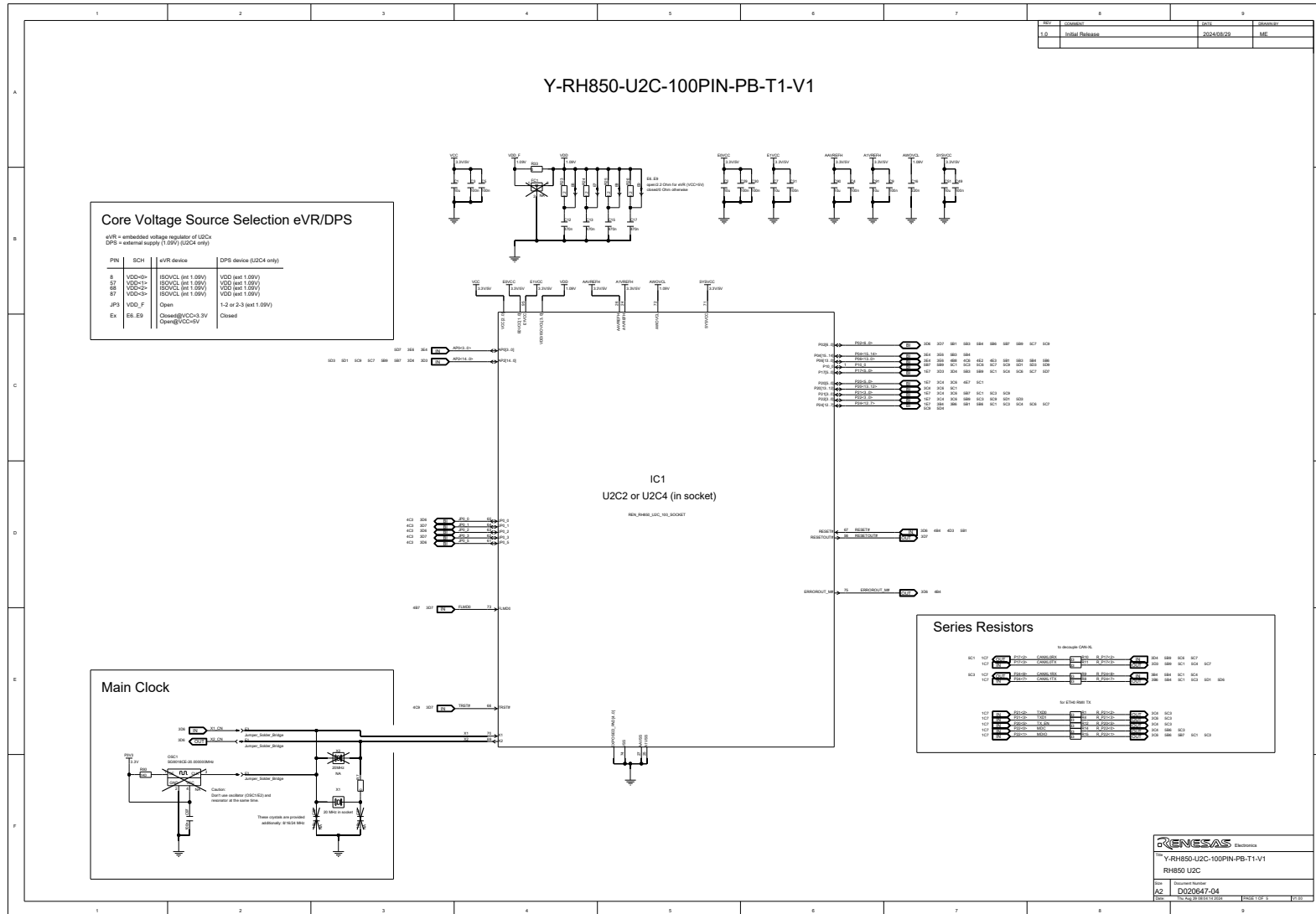
The above components are crossed out in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

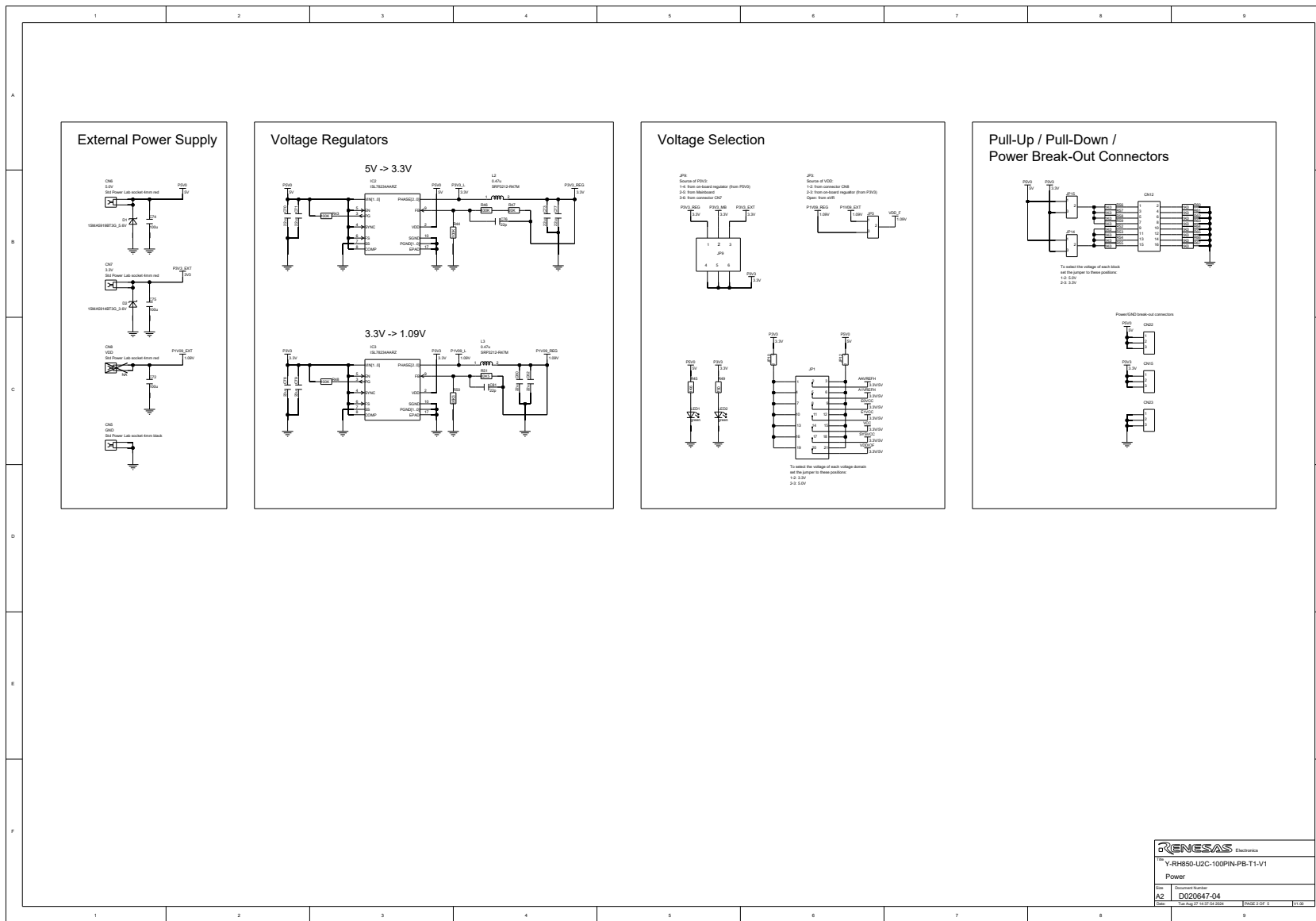
- 1 Hirschmann 4 mm power lab sockets, red, for CN8
- Three resonators HC49 (8 / 16 / 24 MHz)
- 27 jumpers, 2.54 mm, black (board version D020746_06_V01)
- 29 jumpers, 2.54 mm, black (board version D020746_06_V02)

11.1 Board Version D020647_06_V01

11.1.1 RH850/U2C

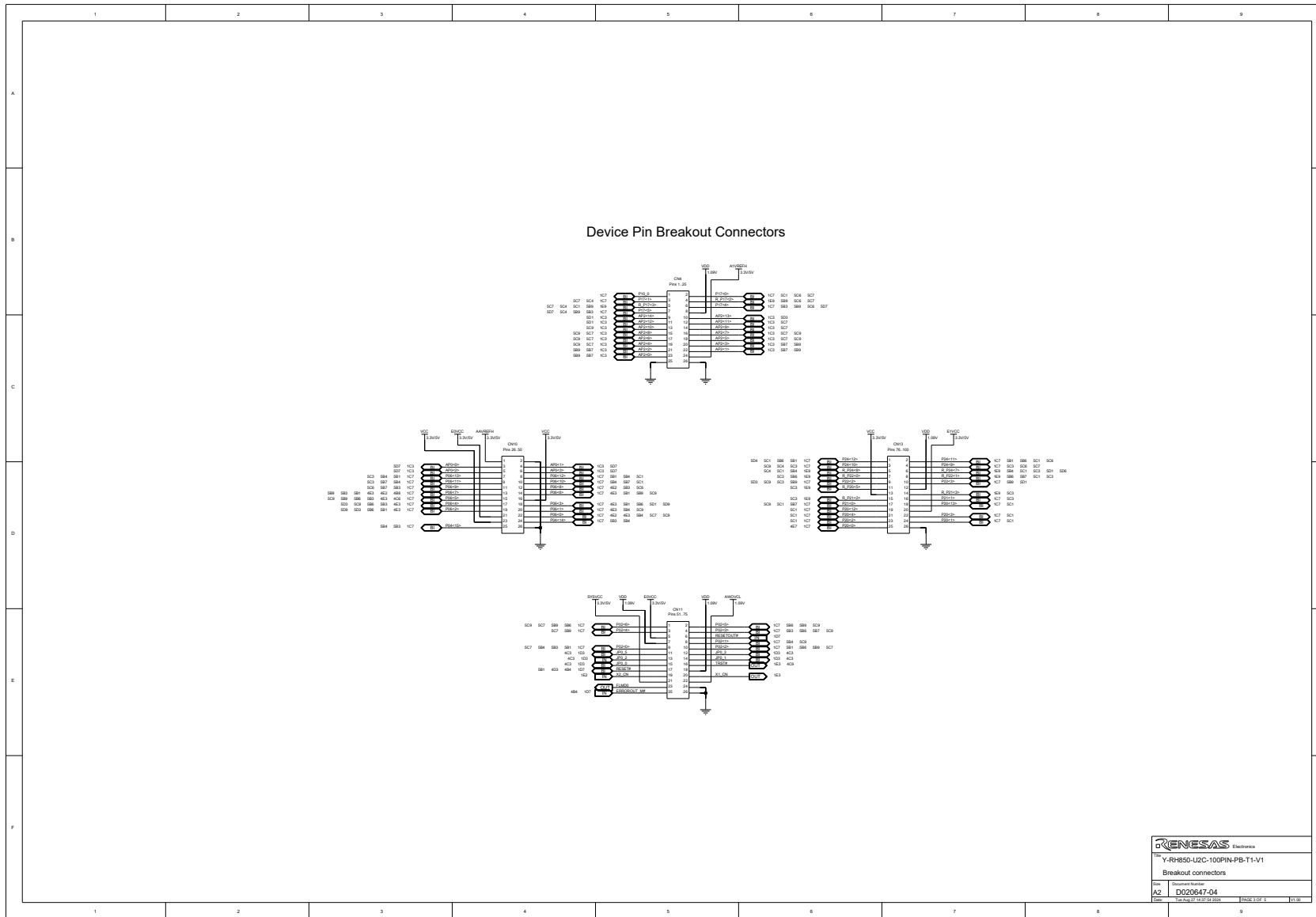


11.1.2 Power Supply



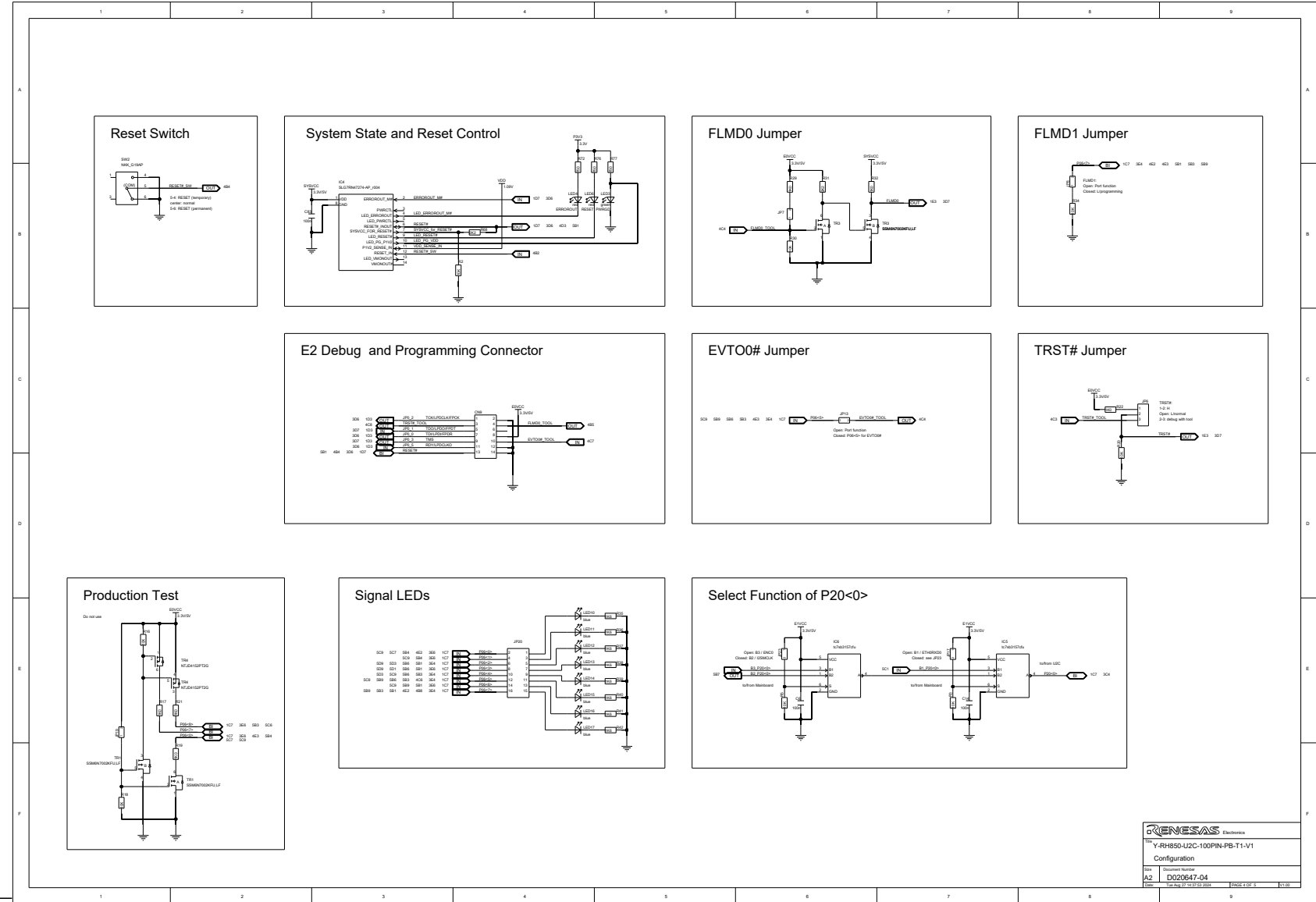
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Y-RH850-U2C-100PIN-PB-T1-V1	
Power	
Rev.	Document Number
A2	D020647-04
Date	Form No. 01 (10/07) 3rd Edition
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11.1.3 Breakout Connectors



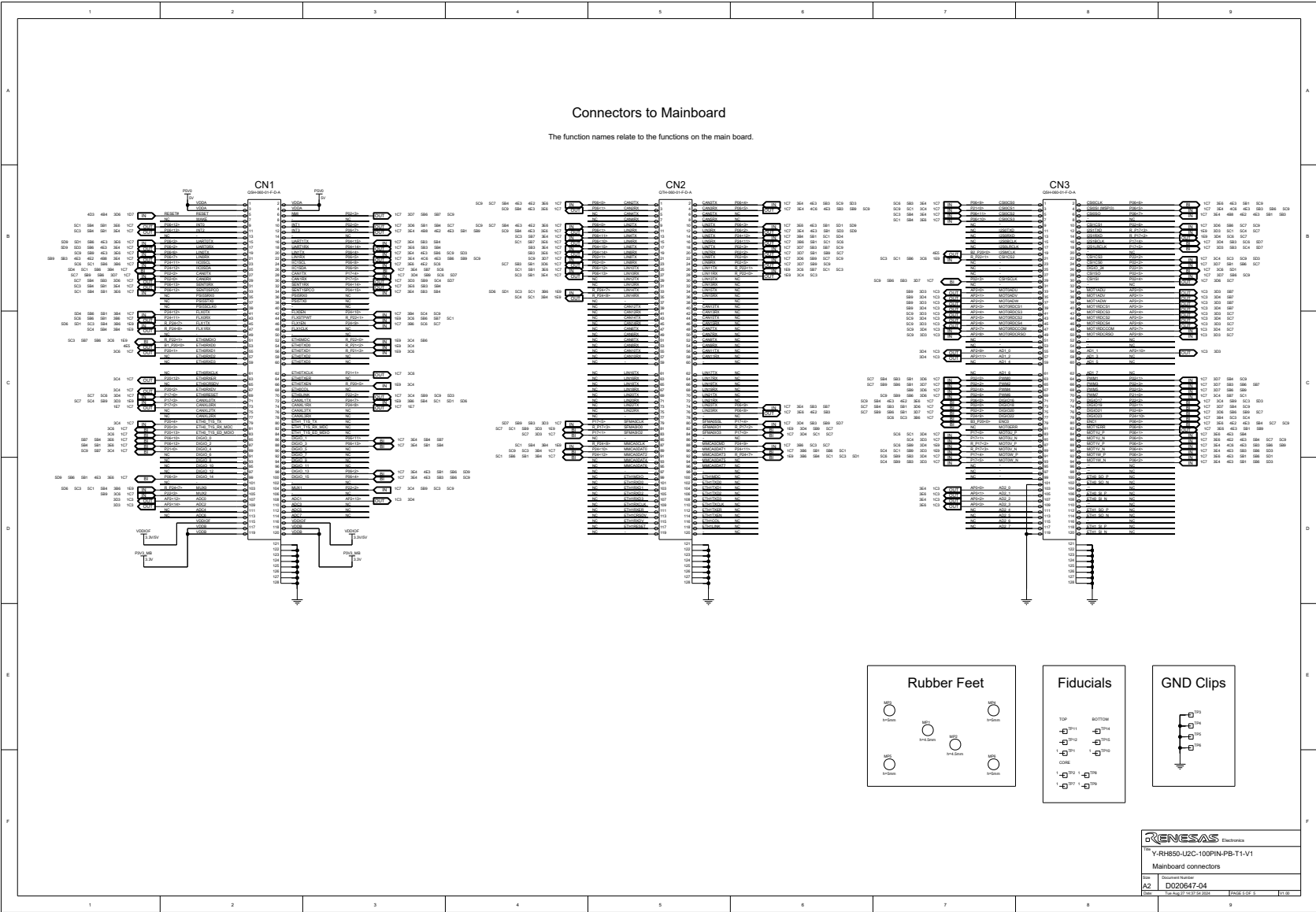
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11.1.4 Configuration



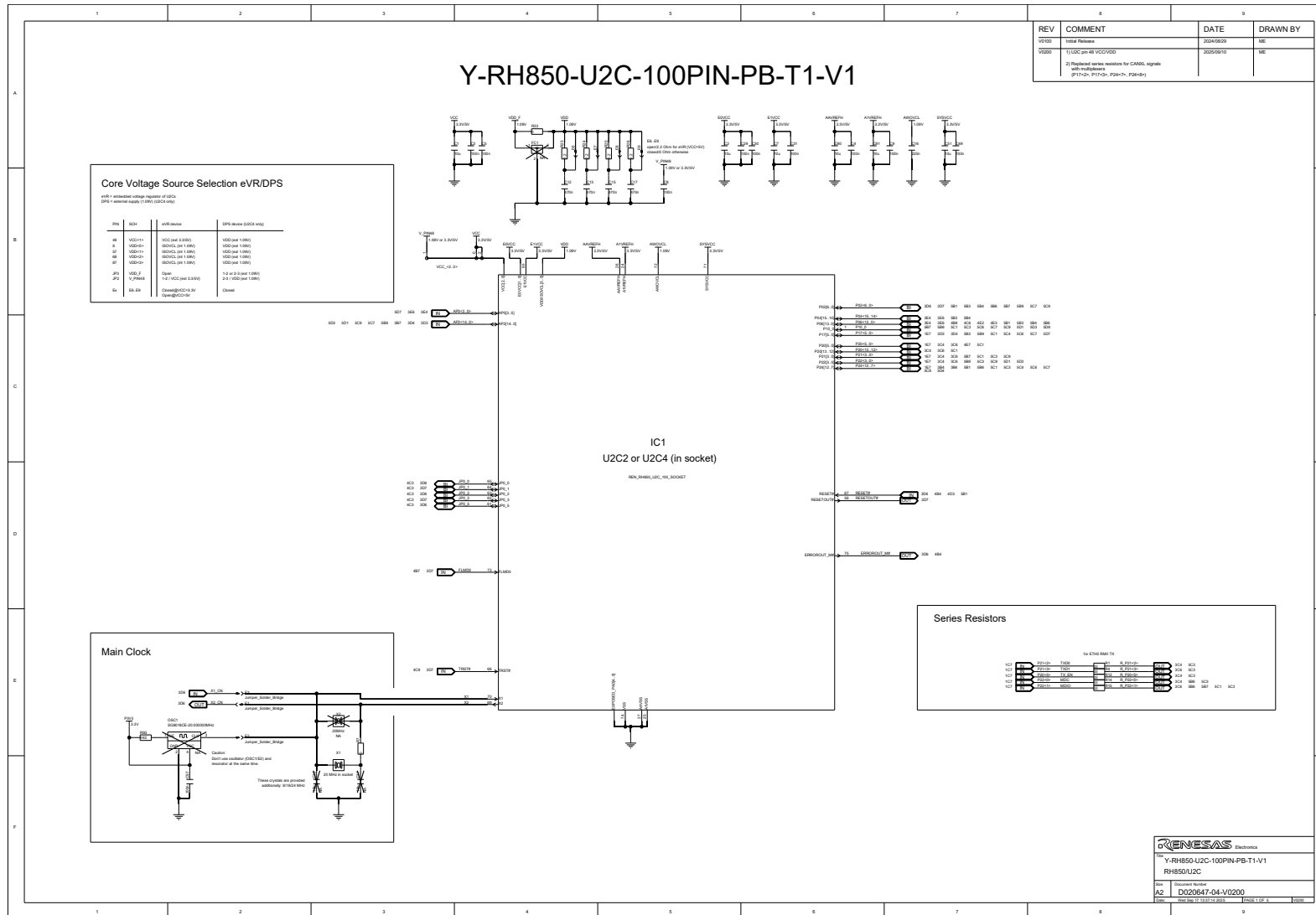
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Page	1 of 5

11.1.5 Main Board Connectors

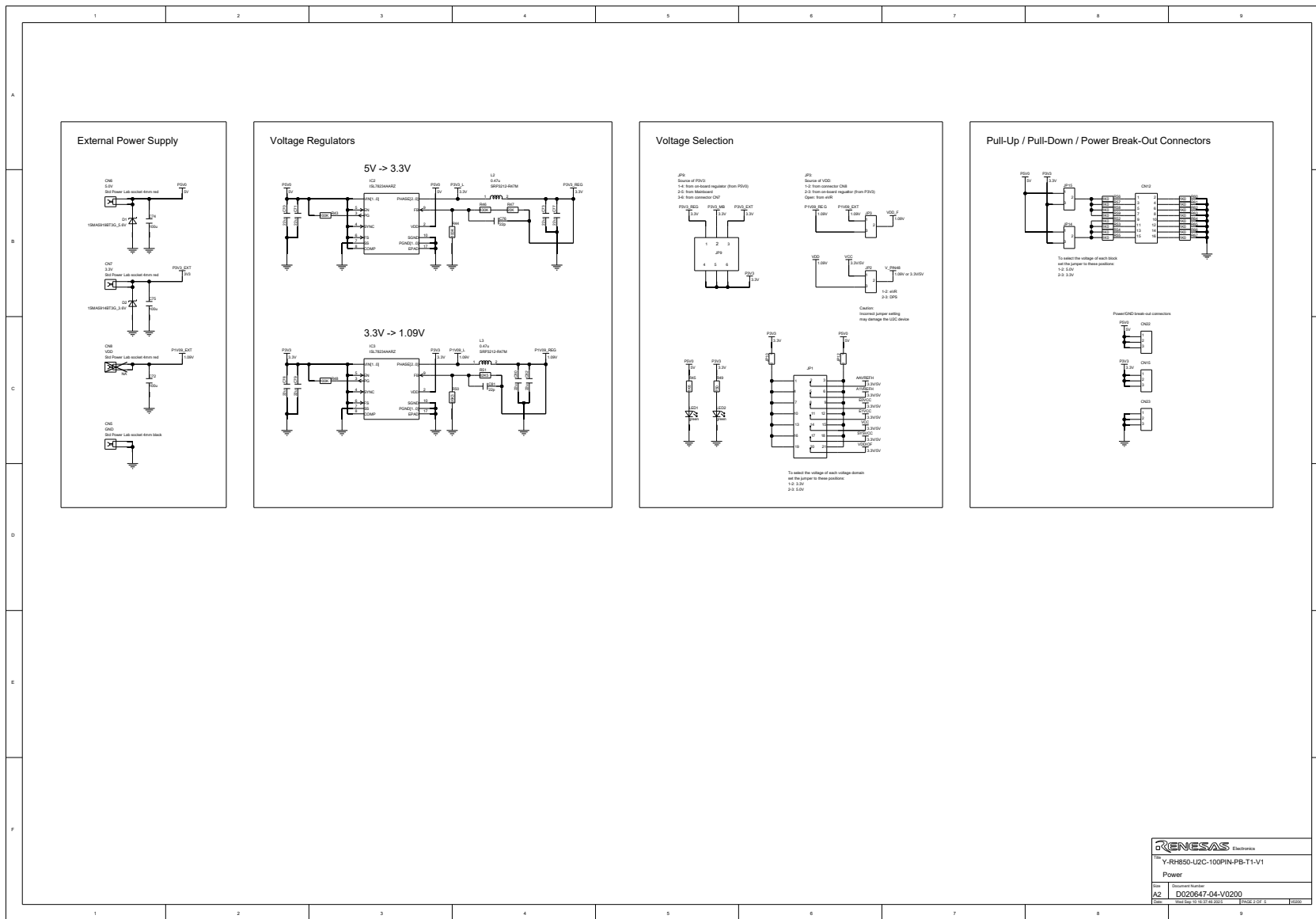


11.2 Board Version D020647_06_V02

11.2.1 RH850/U2C

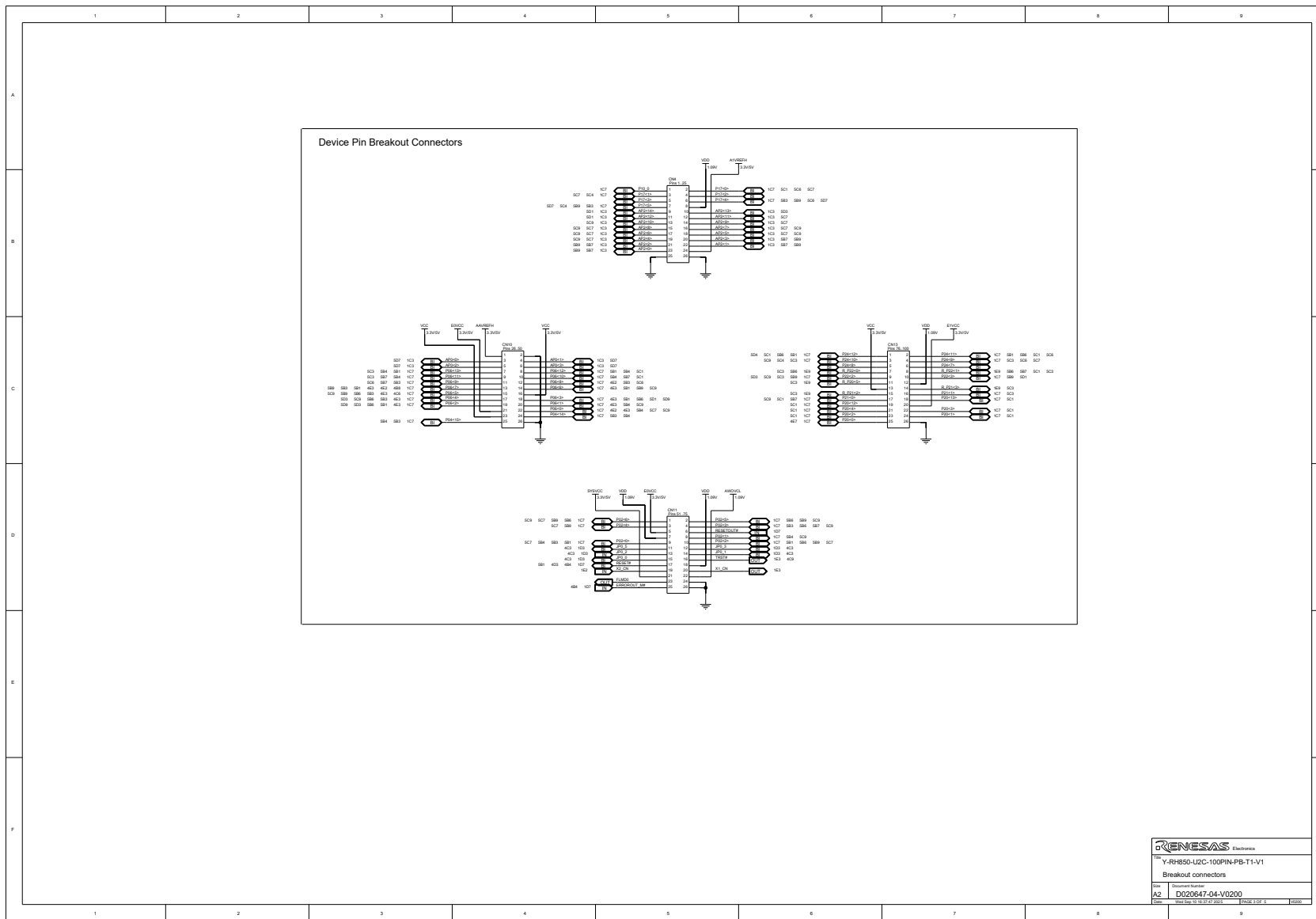


11.2.2 Power Supply

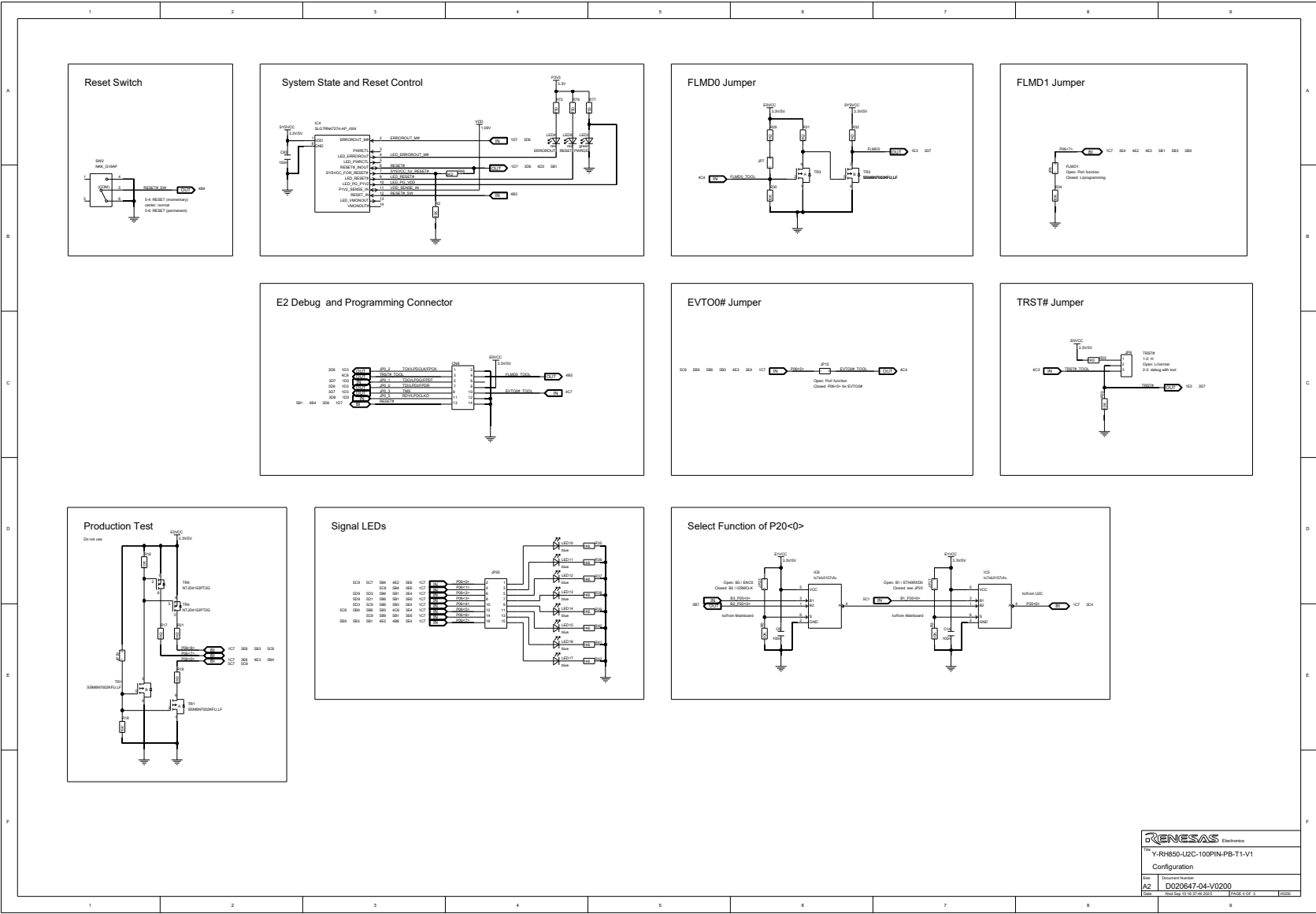


Y-RH850-U2C-100PIN-PB-T1-V1	
Power	
Rev.	Document Number
A2	D020647-04-V0200
Date	First Iss. 10/10/19 Rev. 02/2025

11.2.3 Breakout Connectors

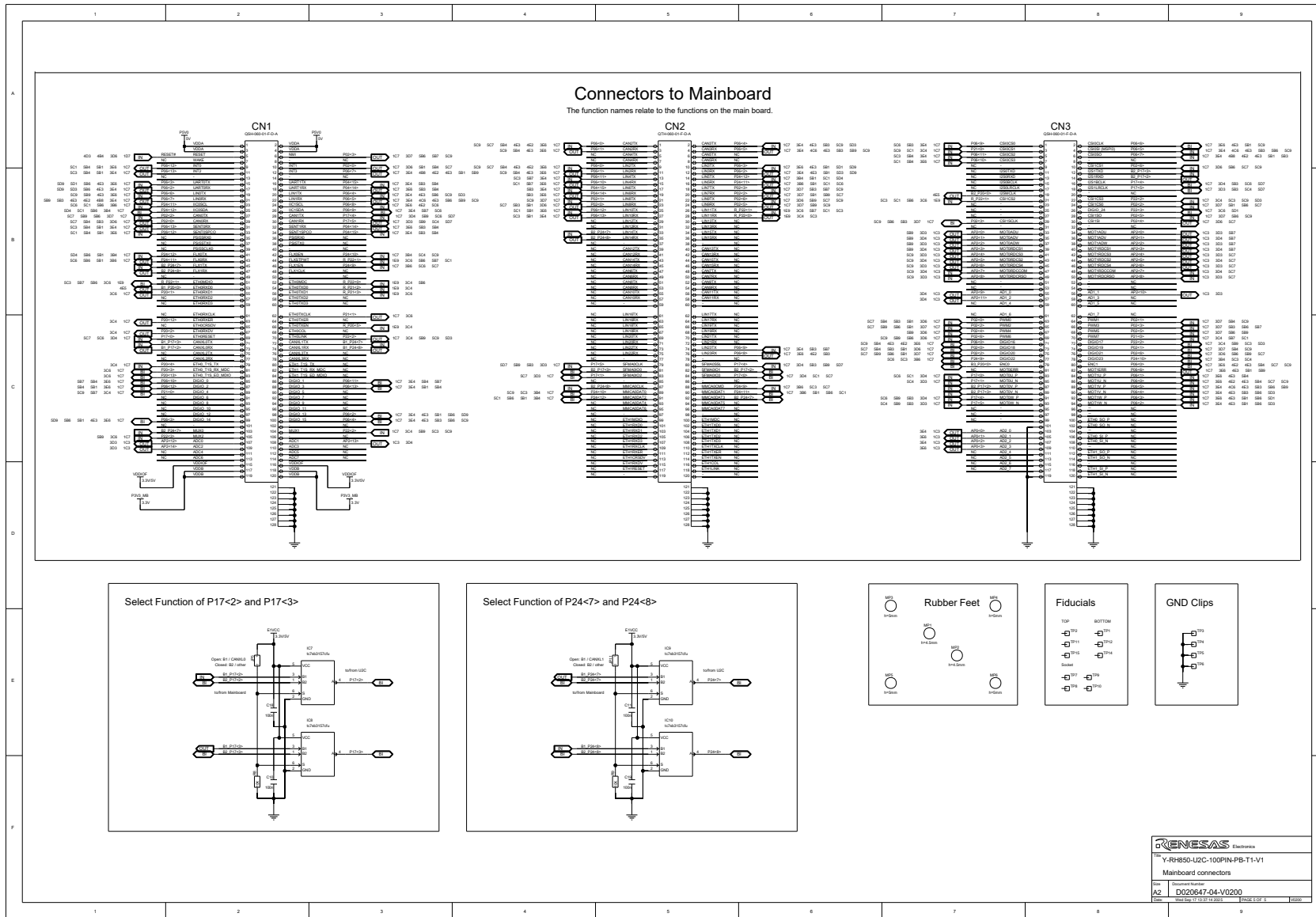


11.2.4 Configuration



RENESAS Electronics	
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Configuration	
Rev.	Document Number
A2	D020647-04-V0200
Date	Issue Date: 12/10/2024

11.2.5 Main Board Connectors



Revision History

Rev.	Date	Description	
		Page	Summary
V1.00	2025-02-07	–	Initial release
V1.01	2025-03-14	13, 22	Added caution about usage of DPS device with board version D020647_06_V01 in chapter 1.6 <i>Mounting of the Device</i> and chapter 3.3 <i>Device Core Voltage (VDD) Selection</i> .
V2.00	2026-02-13		Update for new pcb version D020647_06_V02.
V2.01	2026-04-22		Corrected some typos and updated the document style.

RH850/U2C 100pin Piggyback Board V1 User's Manual: Piggyback Board

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**SALES OFFICES****Renesas Electronics Corporation**<http://www.renesas.com>Refer to "<http://www.renesas.com/>" for the latest and detailed information.**Renesas Electronics America Inc.**1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351**Renesas Electronics Canada Limited**9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004**Renesas Electronics Europe Limited**Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804**Renesas Electronics Europe GmbH**Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327**Renesas Electronics (China) Co., Ltd.**Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679**Renesas Electronics (Shanghai) Co., Ltd.**Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999**Renesas Electronics Hong Kong Limited**Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022**Renesas Electronics Taiwan Co., Ltd.**13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670**Renesas Electronics Singapore Pte. Ltd.**80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300**Renesas Electronics Malaysia Sdn.Bhd.**Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510**Renesas Electronics India Pvt. Ltd.**No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777**Renesas Electronics Korea Co., Ltd.**17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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