User's Manual

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RH850 Evaluation Platform

RH850/U2B 373pin

User's Manual: Piggyback Board

Y-RH850-U2B-373PIN-PB-T1-V1

The newest version of this document can be obtained from the product homepage:
Y-RH850-U2B-373PIN-PB-T1-V1

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (Max.) and VIH (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (Max.) and VIH (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Overview

The RH850/U2B 373pin piggyback board is part of the RH850 Evaluation Platform and serves as a simple and easy to use platform for evaluating the features and performance of Renesas Electronics' 32-bit RH850/U2B 373pin microcontrollers.

Notes

1. This document describes the functionality of the piggyback board and guides the user through its operation.
   For details on the operation of the microcontroller, refer to the device's Hardware User's Manual.
2. In this document active low signals are marked by an appended 'Z' or '#' to the pin or signal name. E.g., the reset pin is named RESETZ or RESET#.
3. In this document following abbreviations are used:
   – H level, L level: high or low signal level of a digital signal, the absolute voltage value depends on the signal

1.1 Package Components

The Y-RH850-U2B-373PIN-PB-T1-V1 product package consists of the following items. After you have unpacked the box, check if your Y-RH850-U2B-373PIN-PB-T1-V1 package contains all these items. *Table 1.1 Package Components for the Y-RH850-U2B-373PIN-PB-T1-V1* shows the packing components of the Y-RH850-U2B-373PIN-PB-T1-V1 package.

Table 1.1 Package Components for the Y-RH850-U2B-373PIN-PB-T1-V1

Item	Description	Quantity
D018705	RH850/U2B 373pin piggyback board	1
D018173-24	Product contents list	1
Jumpers (2-way, 0.1")	In the bag	47 (min. quantity)
D018487	Y-RH850-DEBUG-ADAPTER-F14T46	1
Red Hirschmann 4 mm power lab socket	In the bag	1
Würth PCB Terminal Block	In the bag	2 (only for board version D018705_06_V01)

connector (including cable adapter plug)		
TE MATEnet 1000BASE-T1 Ethernet Port connector	In the bag	2 (only for board version D018705_06_V01)
TE MATEnet 1000BASE-T1 Ethernet connection cable (1m)	In the bag	1 (only for board version D018705_06_V01)
Resonator, HC49, 16 / 24 / 25 / 40 MHz	In the bag	4
Resistors, 100 Ohm	In the bag	20

Note

Please keep the Y-RH850-U2B-373PIN-PB-T1-V1 box at hand for later reuse in sending the product for repairs or for other purposes. Always use the original box when transporting the Y-RH850-U2B-373PIN-PB-T1-V1. If packing of your product is not complete, it may be damaged during transportation.

1.2 Supported Main Boards

This piggyback board can be used as a standalone board, or it can be mated with a main board. The following main boards are supported:

- Y-RH850-X1X-MB-T1-V1
- Y-RH850-X1X-MB-T2-Vx
- Y-RH850-X2X-MB-T1-Vx
- Y-COMMON-MB-T1-V1

1.3 Supported Microcontroller Devices

The board is designed for use with the devices listed in Table 1.2.

Table 1.2 Devices that can be used with Y-RH850-U2B-373pin-PB-T1-V1

	FCC device	MP device	Comments
RH850/U2B10	R7F702Z2*EDBA	R7F70254*FABA-C	FCC: Sixth through ninth characters of the part name indicate U2Bx (BGA373) PKG: The last 2 characters of the part name indicate BGA373.

Note

None of the available devices that can be used with this piggyback board supports SGMII Ethernet interfaces. Thus pcb with board version D018705_06_V02 does not have the Ethernet interfaces populated.

On pcb with board version D018705_06_V01 the Ethernet interfaces are populated, but they cannot be used as the processor does not support it. Configure the board as described in section 8.2 according to the device being used.

1.4 Main Features

- Burn-in socket for mounting of the device
- Several power set-up options
  - Combined operation with powering from main board
  - Stand-alone operation with single power supply (3.3 V or 5.0 V only)
  - Stand-alone operation with flexible, individual power supply (typ. 1.12 V, 3.3 V, 5.0 V)
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
- Debugging and programming interface:
  - 46-pin Aurora Debug Connector (e.g., for using E2 OCD Emulator using the 46 pin to 14 pin adapter Y-RH850-DEBUG-ADAPTER-F14T46, included)
- Pin headers for direct access to each device pin
- Reset switch
- External clock circuit with an exchangeable 16/20/24/25/40 MHz Crystal Resonator
- General purpose signaling LEDs
- Jumpers for device mode selection and other configuration options
- On-board interface connector for
  - Renesas High-Speed Serial I/F (RHSIF)
  - Renesas High Speed Bus (RHSB)
  - Multichannel Serial Peripheral Interface (MSPI)
- Operating temperature from 0 °C to +40 °C

1.5 Piggyback Board Views

The following figures show the top and bottom views of the piggyback board.

The figures show boards of all available versions with all components that are assembled at shipment. The board versions differ in the assembled components as in

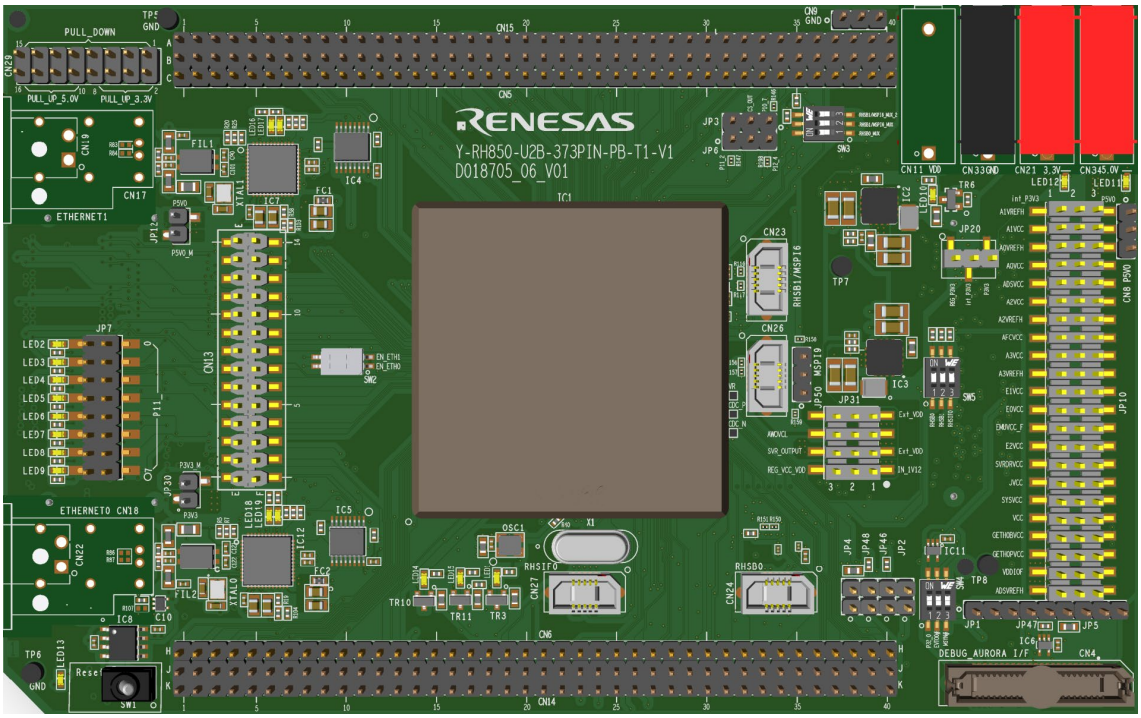


Figure 1.1 Piggyback board top view of board version D018705_06_V01

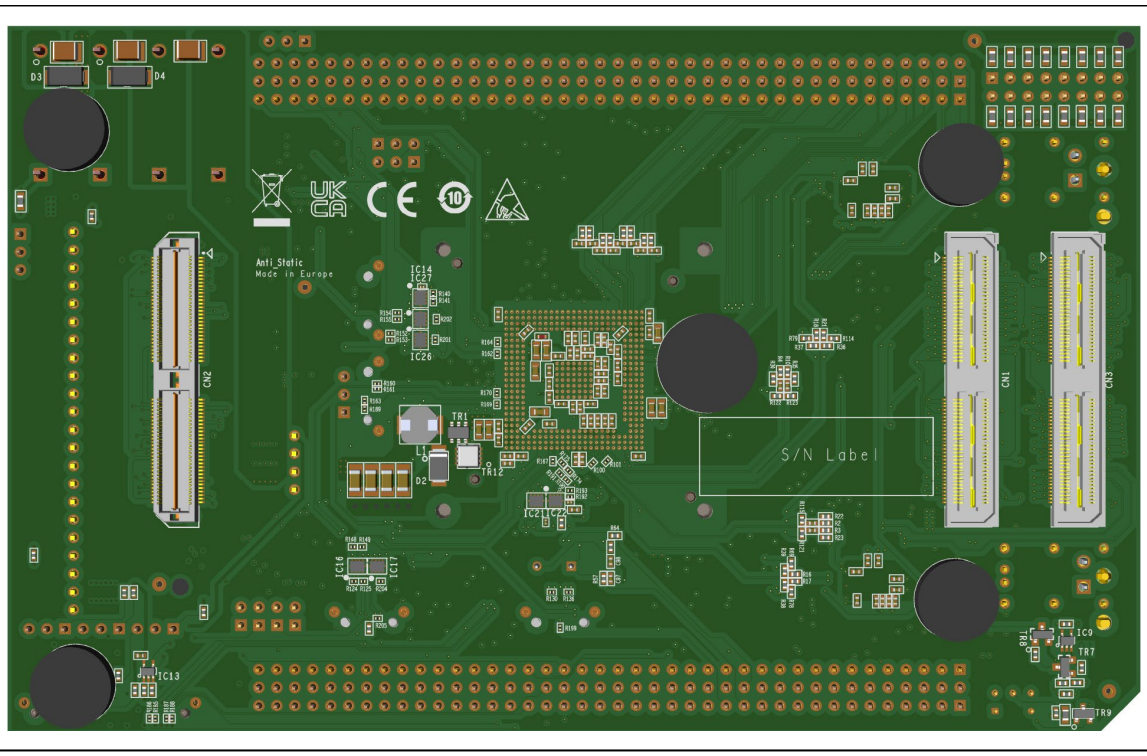


Figure 1.2 Piggyback board bottom view of board version D018705_06_V01

the later version D018705_06_V02 some circuits, that are not supported by RH850/U2B10, are not populated.

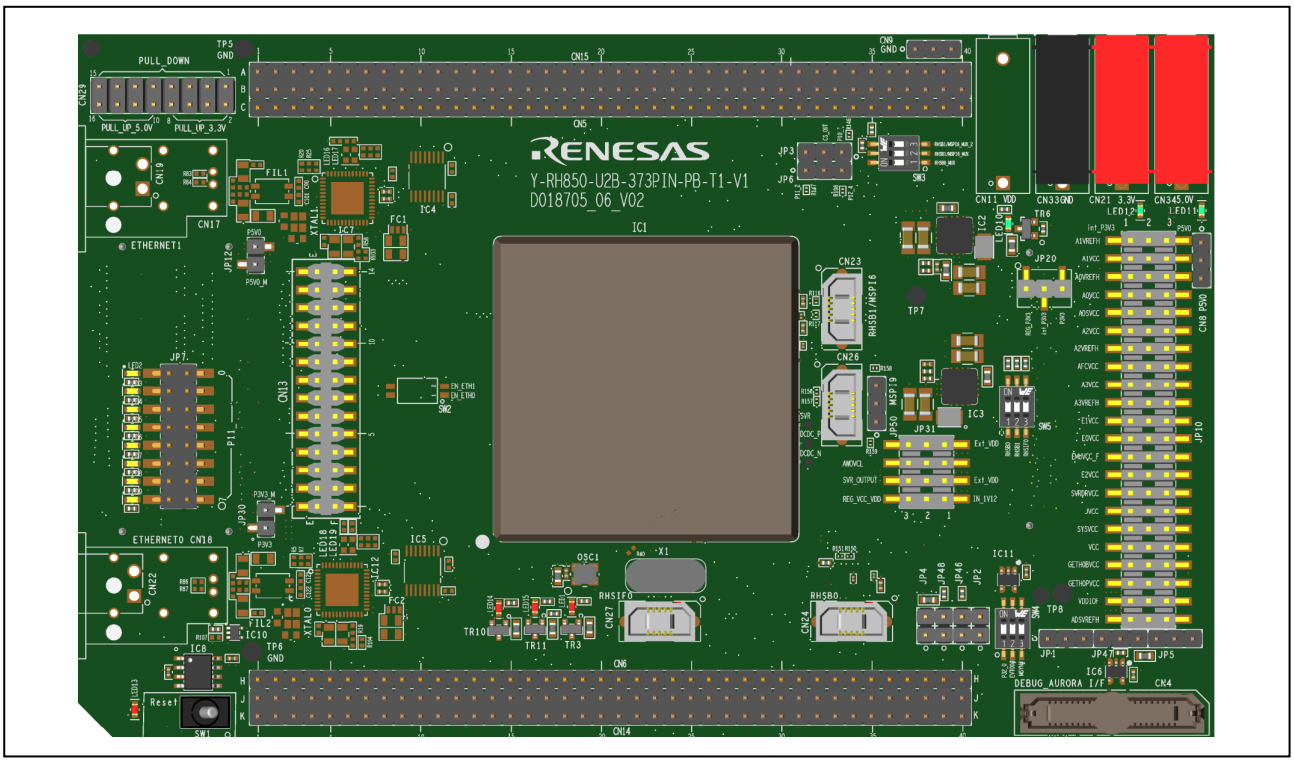


Figure 1.3 Piggyback board top view of board version D018705_06_V02

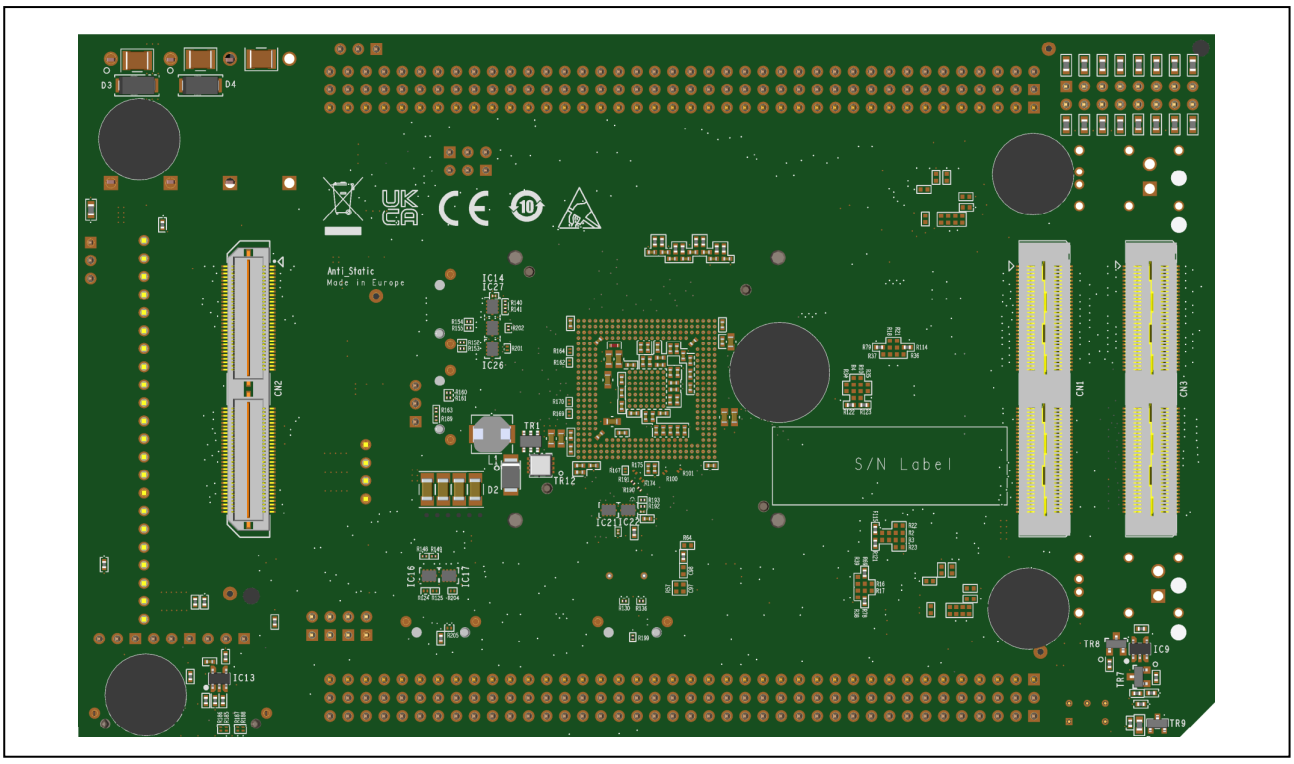


Figure 1.4 Piggyback board bottom view of board version D018705_06_V02

Following figures show the drawing of top and bottom views of the piggyback board.

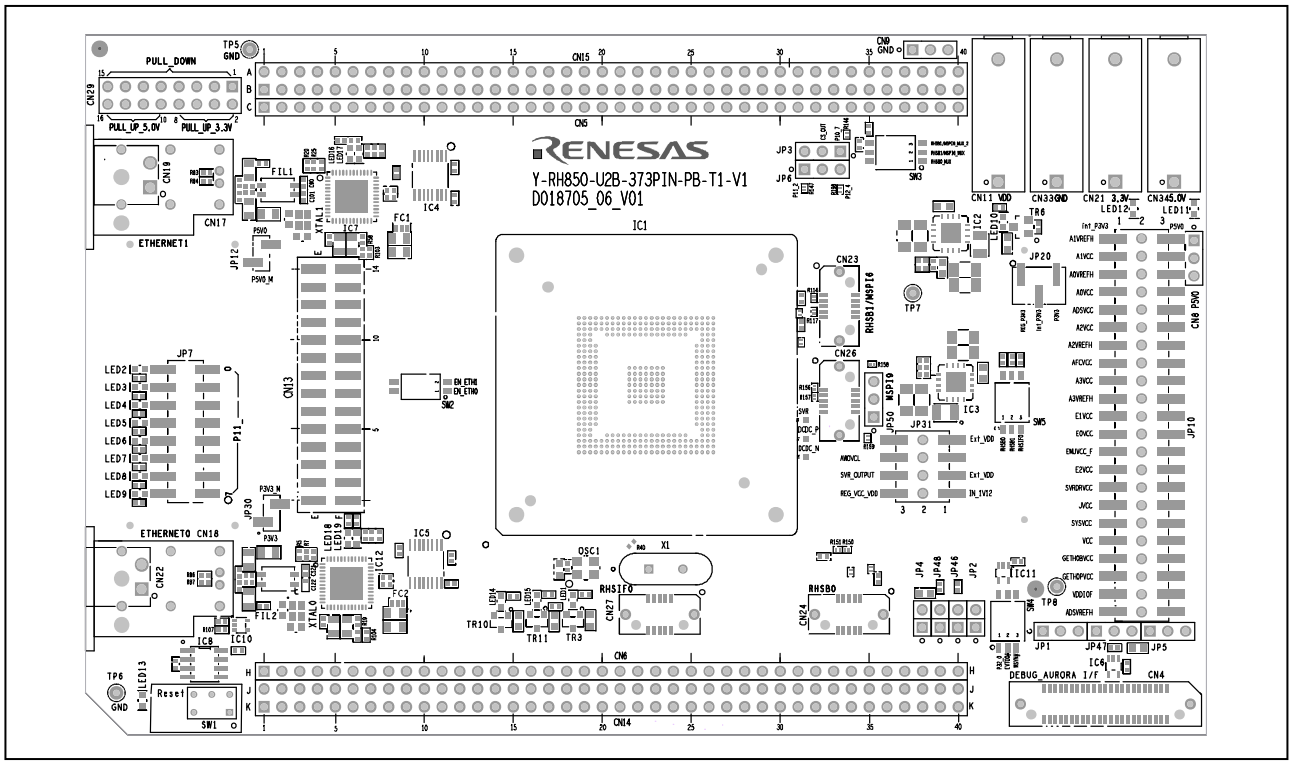


Figure 1.5 Piggyback Board top view of board version D018705_06_V01

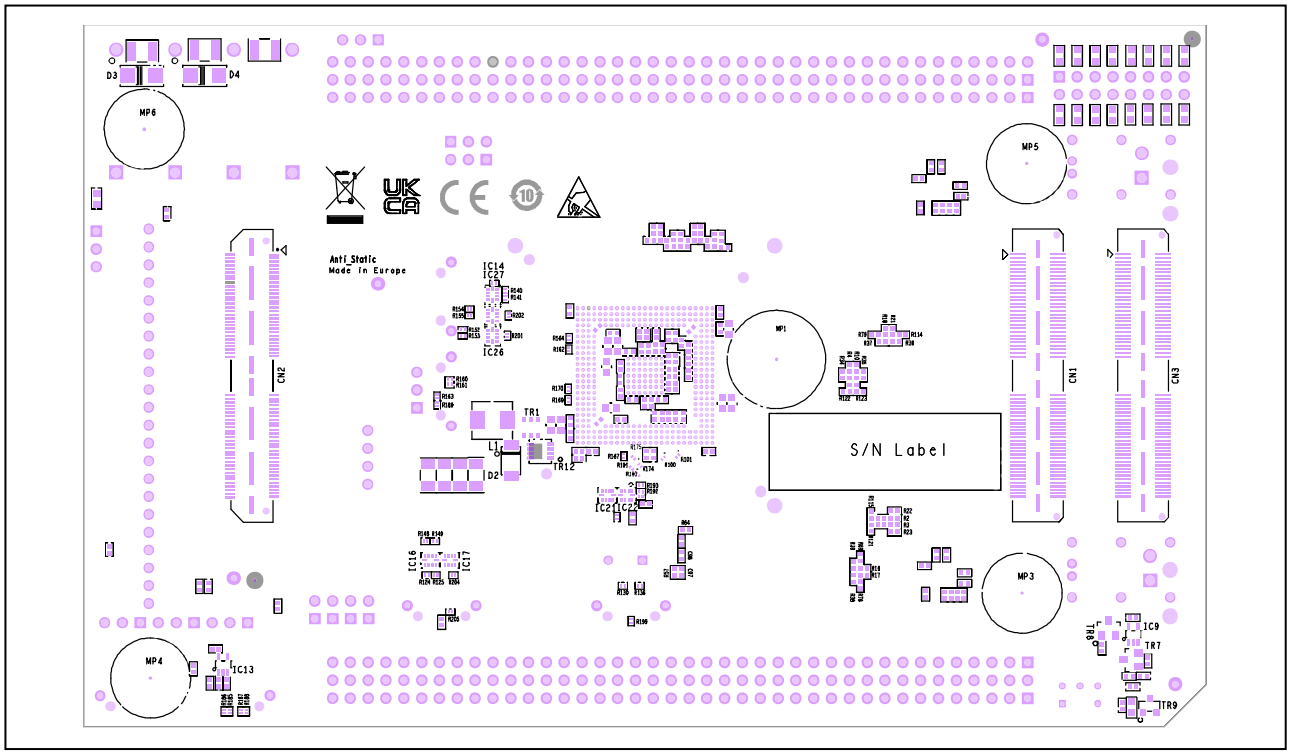


Figure 1.6 Piggyback Board bottom view of board version D018705_06_V01

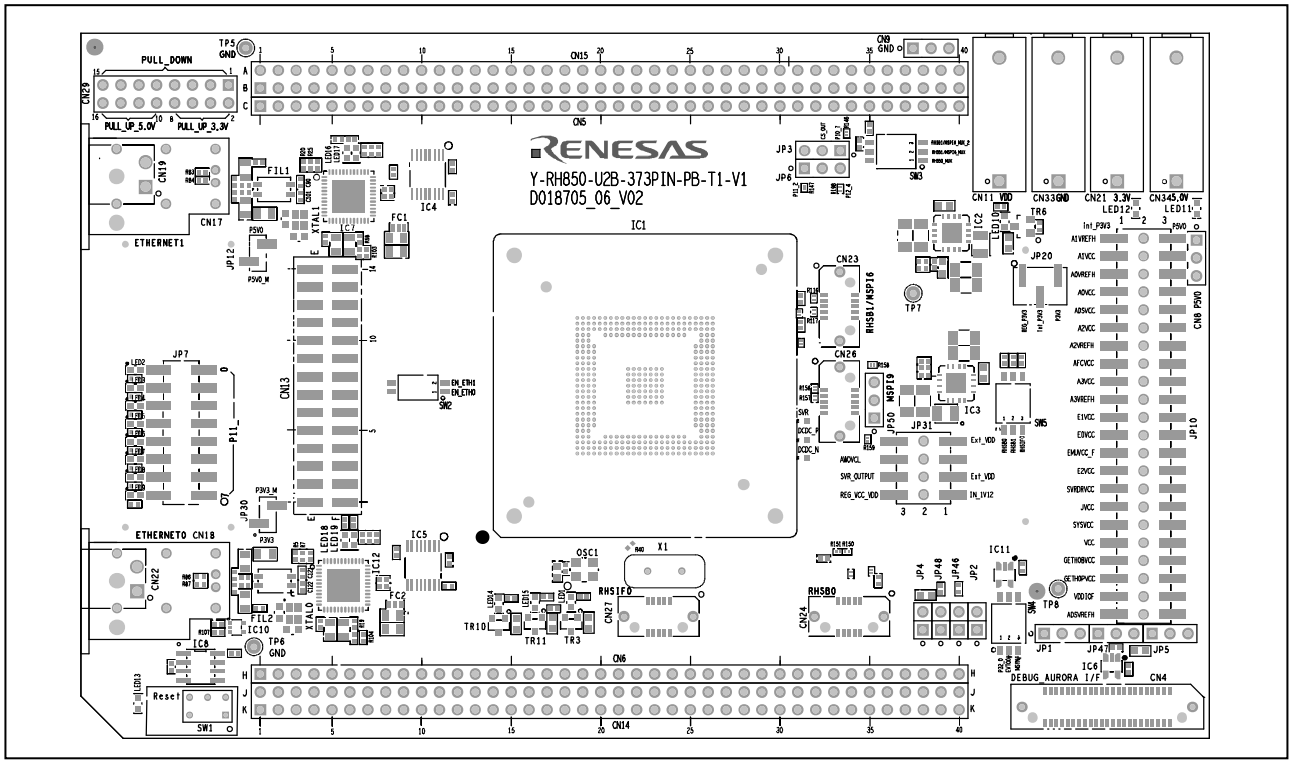


Figure 1.7 Piggyback Board top view of board version D018705_06_V02

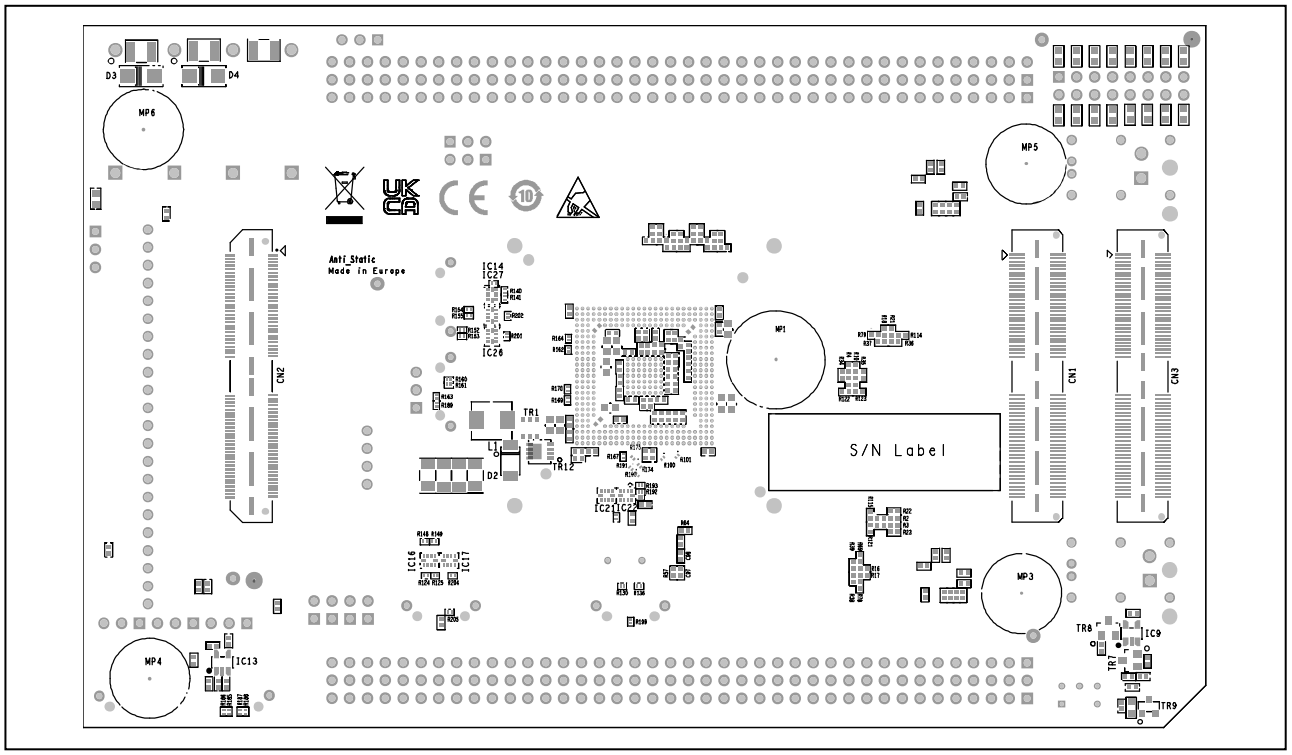


Figure 1.8 Piggyback Board bottom view of board version D018705_06_V02

1.6 Mounting of the Device

The device must be placed inside the socket IC1. To insert the device, align the device package A1 pin with the marking on the pcb.
The A1pin of the socket is marked with a circle on the pcb at the lower left corner of the socket. In Figure 1.9 it is marked with a white dot.

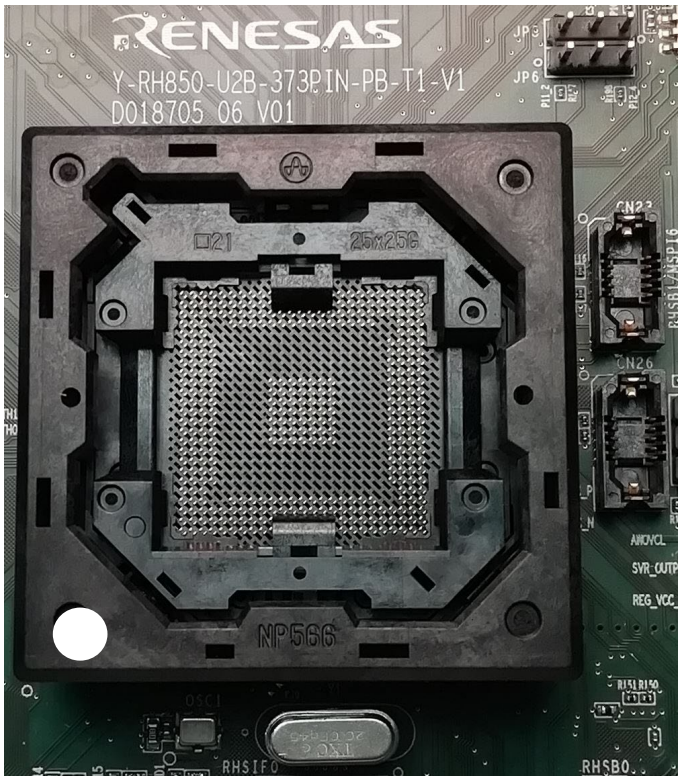


Figure 1.9 Yamaichi NP566-373-024-X socket

The A1 pin of the device is marked with a dot on the device package.

CAUTION

Be careful with the device placement in the socket to avoid damage to the device.

2. Jumpers, Connectors, Switches and LEDs

This section provides complete lists of all jumpers, connectors, and LEDs.

The placement of these components on the board is depicted in the figure below.

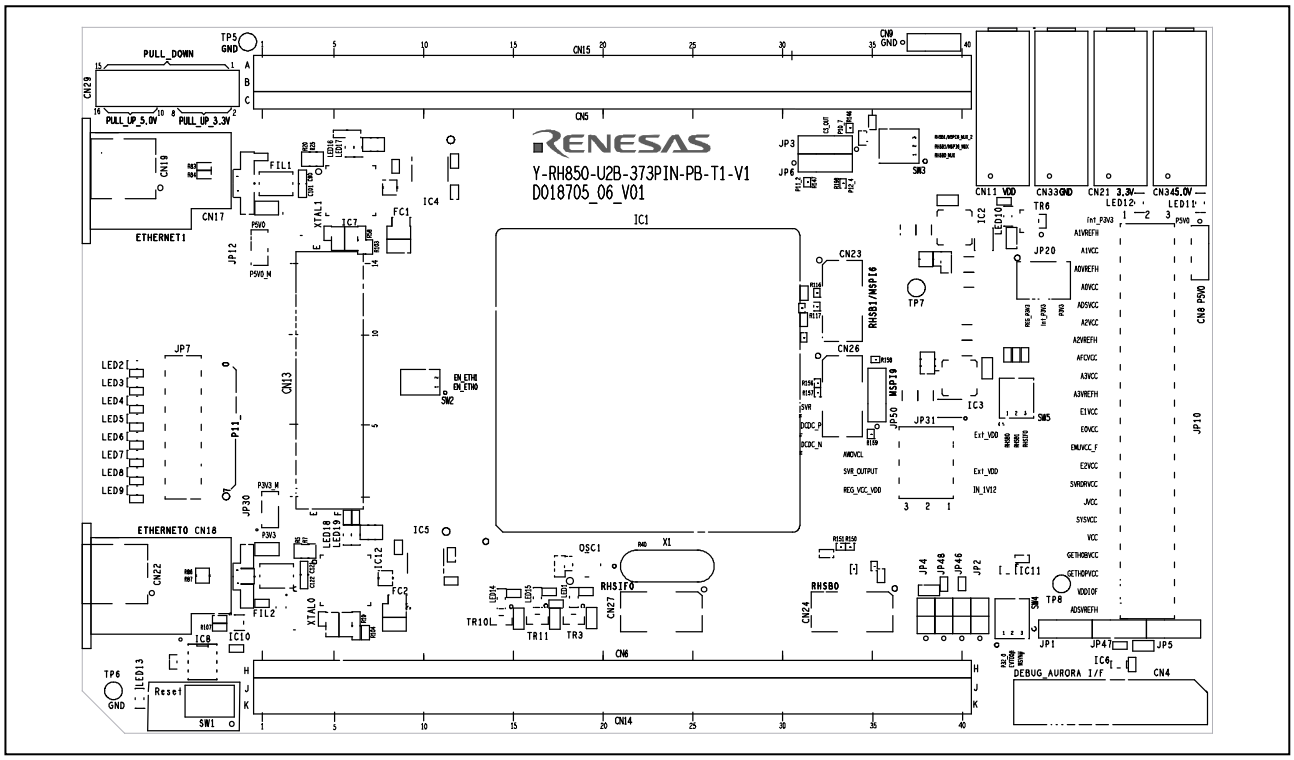


Figure 2.1 Placement of jumpers, connectors and LEDs on top side

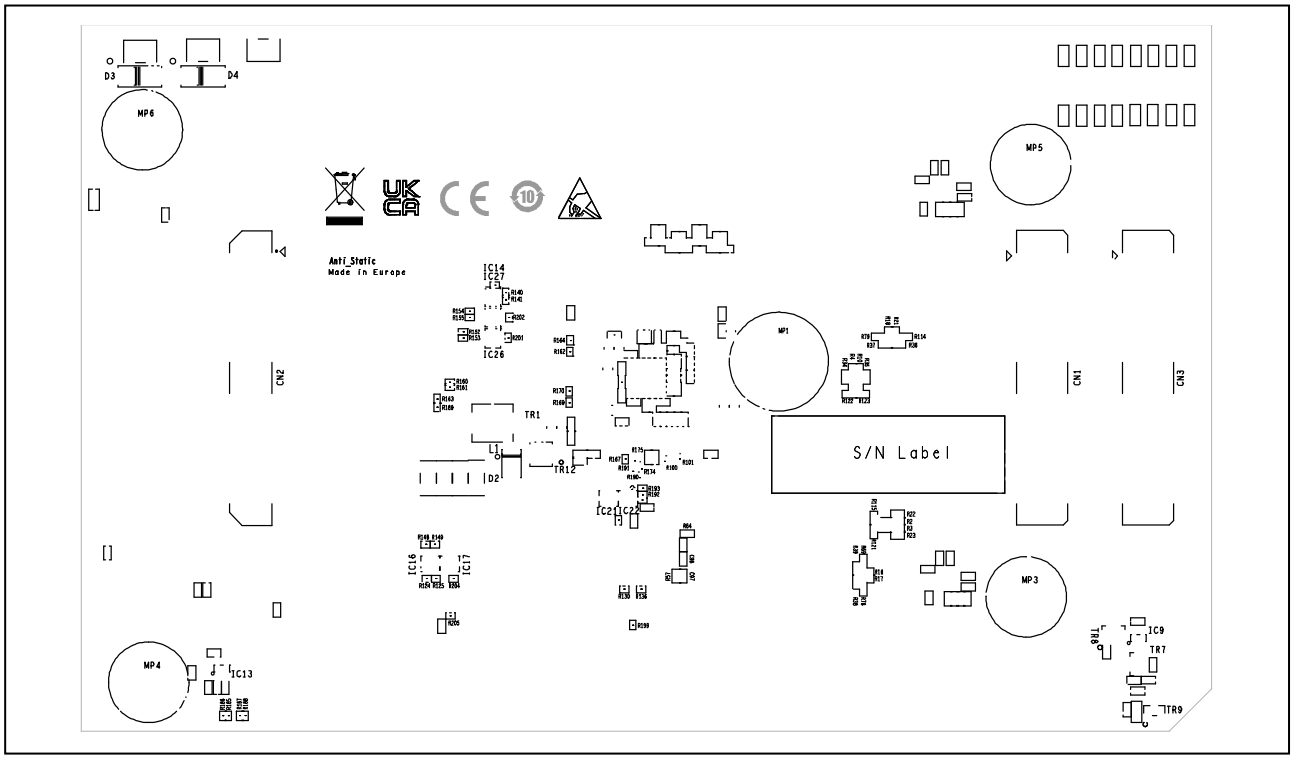


Figure 2.2 Placement of connectors on bottom side

2.1 Jumper Overview

The following table provides an overview of all jumpers.

Table 2.1 Jumper overview

Jumper	Function	Remark
JP1	Select signal source for AURORES# input on RH850/U2B • JP1[2-1]: TRST# signal from Aurora debug I/F connector CN4 • JP1[2-3]: AURORES#_VCC signal from Aurora debug I/F connector CN4	refer to *5 Debug and Flash Programming Interfaces*
JP2	Enable signaling of PWRCTL for SYSVCC • JP2[1-2]: PWRCTL control of SYSVCC is signaled by LED15	refer to *6.1 Operation Mode Selection*
JP3, JP6	Select port for CS_OUT/SSI_IN signal on CN23.6 • JP3[1-2]: connect to RHSB1CSD0 (P10_7) • JP3[2-3]: Select port using jumper JP6 ○ JP6[1-2]: connect to MSPI6CSS0 (P11_2) ○ JP6[2-3]: connect to MSPI6SSI (P12_4)	refer to *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6* and *7.5 RHSB1/MSPI6 Connector CN23*
JP4	Swap TX and RX signals of RHSIF0 interface available at CN27	refer to *6.8 Renesas High-Speed Serial I/F RHSIF0*
JP5	Select signal source for TRST# signal • JP5[1-2]: Fix TRST# signal to SYSVCC • JP5[2-3]: TRST# signal is TRST# input from Aurora debug interface connector (pin 12 on connector CN4)	refer to *5 Debug and Flash Programming Interfaces*
JP7	Enable LED outputs	refer to *6.3 Signaling LEDs*
JP10	Select +3.3 V / +5.0 V power supply configuration	refer to *3.2 Voltage Distribution*
JP12	Enable +5.0 V power supply from main board	refer to *3.1 Board Power Connection*
JP20	Select +3.3 V power supply source • JP20[1-2]: Get 3.3 V from onboard voltage regulator • JP20[2-3]: Get 3.3V from external power supply CN21 or from main board	refer to *3.2 Voltage Distribution*
JP30	Enable +3.3 V power supply from main board	refer to *3.1 Board Power Connection*
JP31	Device core voltage configuration	refer to *3.3 Device Core Voltage (VDD) Selection*
JP46	Change FLMD0 signal to “H”.	refer to *6.1 Operation Mode Selection*
JP47	SBMD input selection • JP47[1-2]: connect to SYSVCC • JP47[2-3]: connect to GND	
JP48	Change FLMD1 signal to “H”.	
JP50	Select CS_OUT port for MSPI9 • JP50[1-2]: CS_OUT is from port P12_5 • JP50[2-3]: CS_OUT is from port P11_10	

2.2 Connector Overview

The following table provides an overview of all connectors.

Table 2.2 Connector overview (cont'd)

Connector	Function	Remark
CN1	Main Board connectors	refer to *7.1 Connectors to the Main Board CN1 to CN3*
CN2		
CN3		
CN4	Debug connector	refer to *5 Debug and Flash Programming Interfaces* and *7.2 Debug Connector CN4*
CN5	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN6, CN13, CN14 and* CN15
CN6		
CN8	P5V0 pin header	refer to *3.2 Voltage Distribution*
CN9	GND pin header	
CN11	+1.12 V external power supply	refer to *3.1 Board Power Connection*
CN13	Device ports connector	refer to *7.3 Device Ports Connectors CN5, CN6, CN13, CN14 and CN15*
CN14		
CN15		
CN17	Ethernet interface connector	the connectors are only delivered with board version D018705_06_V01 refer to *6.9 Automotive Ethernet Interfaces ETN0 and ETN1*
CN18		
CN19		
CN21	+3.3 V external power supply	refer to *3.1 Board Power Connection*
CN22	Ethernet interface connector	the connector is only delivered with board version D018705_06_V01 refer to *6.9 Automotive Ethernet Interfaces ETN0 and ETN1*
CN23	RHSB1 / MSPI6 interface connector	refer to *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
CN24	RHSB0 interface connector	refer to *6.5 Renesas High-Speed Bus RHSB0*
CN26	MSPI9 interface connector	refer to *6.7 Renesas Multichannel Serial Peripheral Interface MSPI9*
CN27	RHSIF0 interface connector	refer to *6.8 Renesas High-Speed Serial I/F RHSIF0*
CN29	Pull up / pull down configuration	refer to *6.4 Pull-Up/Pull-Down Pin Header*
CN33	GND external power supply	refer to *3.1 Board Power Connection*
CN34	+5.0 V external power supply	refer to *3.1 Board Power Connection*

2.3 Switches Overview

The following table provides an overview of all switches.

Table 2.3 Switches overview

Connector	Function	Remark
SW1	RESET#	refer to *6.2 RESET Switch*
SW2	Enable Ethernet outputs	populated only on-board version D018705_06_V01 **both switches must be set to "OFF".** refer to *6.9 Automotive Ethernet Interfaces ETN0 and ETN1*
SW3	Port selection RHSB0 / RHSB1 / MSPI6	refer to *6.5 Renesas High-Speed Bus RHSB0* and *6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6*
SW5	Enable control for RHSB0 / RHSB1 / MSPI6 multiplexers.	
SW4	Debug port connection EVTO0 / MSYN#	refer to *5 Debug and Flash Programming Interfaces*

2.4 LED Overview

The following table provides an overview of all LED.

Table 2.4 LED overview

LED	Function	Color	Remark
LED1	Device ERROROUT_M# signal	red	
LED2	Signaling LED	yellow	connection via JP7, refer to *6.3 Signaling LEDs*
LED3			
LED4			
LED5			
LED6			
LED7			
LED8			
LED9			
LED10	1.12 V device core voltage VDD	green	refer to *3.4 Power Supply LEDs*
LED11	5.0 V power supply P5V0	green	
LED12	3.3 V power supply int_P3V3	green	
LED13	Reset switch SW1 on	red	refer to *6.2 RESET Switch*
LED14	Device VMONOUT# signal	red	
LED15	Device PWRCTL signal	red	
LED16	Ethernet channel 1 activity LED	red	populated only on-board version D018705_06_V01 refer to *6.9 Automotive Ethernet Interfaces ETN0 and ETN1*
LED17		green	
LED18	Ethernet channel 0 activity LED	red	
LED19		green	

3. Power Supply

3.1 Board Power Connection

The device and the board require various power supply voltages:

- 3.3 V for most of the digital circuitry on the device and on the board
- 5.0 V in case some ports shall be operated with 5.0 V I/O voltage
- 1.12 V for the device's VDD core voltage supply
  Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.

Note

Within this document all voltage values are considered as 'typical'.

Refer to the 'Electrical Characteristics' section of the Hardware User's Manual for allowed voltage ranges.

The following connectors are available to supply external voltages:

- Four 4 mm 'banana-type' connectors are used to connect external power supplies:
  - black connector CN33 for GND (VSS)
  - red connector CN34 for 5 V
  - red connector CN21 for 3.3 V
  - red connector CN11 for 1.12 V
    Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
    Connector CN11 is not assembled at delivery of the board, but separately supplied with the board package.

In case the piggyback board is mounted on a Main Board, all voltages except for 1.12 V (VDD) can be supplied by the Main Board. The jumpers JP12 (5.0 V) and JP30 (3.3 V) are used to enable power supply from main board

CAUTION

Do not power on the piggyback board when no RH850 microcontroller is installed in socket IC1 because the switching regulator in the SVR power supply circuit doesn't have defined control signals when the microcontroller is not installed and may be damaged.

If you want to power on the piggyback board without microcontroller, make sure jumper CN10[43-44-45] (SVRDRVCC) is open.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to "Fixed" (output) in bit SVRENDCDCHZ in option byte 25.

Do not supply the 5 V (CN34) and 3.3 V (CN21) voltage directly to the piggyback board in case the power supply from the Main Board is enabled.

Connecting external 1.12 V via CN11 (and GND via CN9) is still an option also in this case.

For some general power supply scenarios, the jumper settings are described in *8 Jumper Configuration Examples*.

3.2 Voltage Distribution

The following table shows the required device power supply pins and their function:

Table 3.1 Device power supply pins

Device power supply pin	Voltage	Function
E0VCC, E1VCC, E2VCC	3.3 V, 5 V	Power supply for I/O ports
EMUVDD	1.09 V	Power supply for debug circuits, only available on FCC devices
EMUVCC	3.3 V	
J0VCC, J1VCC	3.3 V, 5 V	
SYSVCC	3.3 V, 5 V	Power supply for system logic and internal voltage regulator power I/O ports
VCC	3.3 V, 5 V	Power supply for on-chip flash memory
SVRDRVCC	3.3 V, 5 V	Power supply for on-chip Switching Voltage Regulator (SVR)
SVRAVCC	3.3 V, 5 V	Connected to SYSVCC
LVDVCC	3.3V, 5 V	RHSIF/RHSB supply voltage
OSCVCC	3.3 V, 5 V	Power supply for OSC
GETH0BVCC	3.3 V	Power supply for Ethernet
GETH0PVCC	3.3 V, 5 V	
VDDIOF	3.3 V, 5 V	I/O voltage supply for the Main Board
A0VCC, A1VCC, A2VCC, A3VCC	3.3 V, 5 V	A/D Converter's power supplies and reference voltages
A0VREFH, A1VREFH, A2VREFH, A3VREFH, ADSVREFH	3.3 V, 5 V	
ADSVCC, AFCVCC	3.3 V, 5 V	
VDD	1.09 V	Core supply voltage Refer to *3.3 Device Core Voltage (VDD) Selection*

Each of the above voltages can be selected from 5.0 V or 3.3 V (where applicable, see table above) by a set of jumpers.

The supply for 3.3 V can be selected from external power supply / main board power supply or from the onboard voltage regulator using jumper JP20:

- JP20 [1-2]: 3.3 V supply comes from the onboard voltage regulator.
- JP20 [2-3]: 3.3 V supply comes from the external power supply or from the main board power supply.

Table 3.2 Voltage Selection shows which jumpers to set to select the different device supply voltages, and *Figure 3.1 Voltage distribution* shows the schematic for it.

Table 3.2 Voltage Selection

Device power supply pin	Connection for 3.3 V	Connection for 5.0 V
A1VREFH	JP10 [1-2]	JP10 [2-3]
A1VCC	JP10 [4-5]	JP10 [5-6]
A0VREFH	JP10 [7-8]	JP10 [8-9]
A0VCC	JP10 [10-11]	JP10 [11-12]
ADSVCC	JP10 [13-14]	JP10 [14-15]
A2VCC	JP10 [16-17]	JP10 [17-18]
A2VREFH	JP10 [19-20]	JP10 [20-21]
AFCVCC	JP10 [22-23]	JP10 [23-24]
A3VCC	JP10 [25-26]	JP10 [26-27]
A3VREFH	JP10 [28-29]	JP10 [29-30]
E1VCC	JP10 [31-32]	JP10 [32-33]
E0VCC (LVDVCC)	JP10 [34-35]	JP10 [35-36]
EMUVCC	JP10 [37-38]	---
E2VCC	JP10 [40-41]	JP10 [41-42]
SVRDRVCC	JP10 [43-44]	JP10 [44-45]
JVCC	JP10 [46-47]	JP10 [47-48]
SYSVCC (SVRAVCC)	JP10 [49-50]	JP10 [50-51]
VCC (OSCVCC)	JP10 [52-53]	JP10 [53-54]
GETH0BVCC	JP10 [55-56]	--- *
GETH0PVCC	JP10 [58-59]	JP10 [59-60]: NC
VDDIOF	JP10 [61-62]	JP10 [62-63]
ADSVREFH	JP10 [64-65]	JP10 [65-66]

JP10

	int_P3V3		P5V0
A1VREFH	1	2	3
A1VCC	4	5	6
A0VREFH	7	8	9
A0VCC	10	11	12
ADSVCC	13	14	15
A2VCC	16	17	18
A2VREFH	19	20	21
AFCVCC	22	23	24
A3VCC	25	26	27
A3VREFH	28	29	30
E1VCC	31	32	33
E0VCC	34	35	36
EMUVCC	37	38	39
E2VCC	40	41	42
SVRDRVCC	43	44	45
JVCC	46	47	48
SYSVCC	49	50	51
VCC	52	53	54
GETH0BVCC	55	56	57
GETH0PVCC	58	59	60
VDDIOF	61	62	63
ADSVREFH	64	65	66

Note * JP10 [56-57]: Connected to GND via 4.7kΩ pull-down

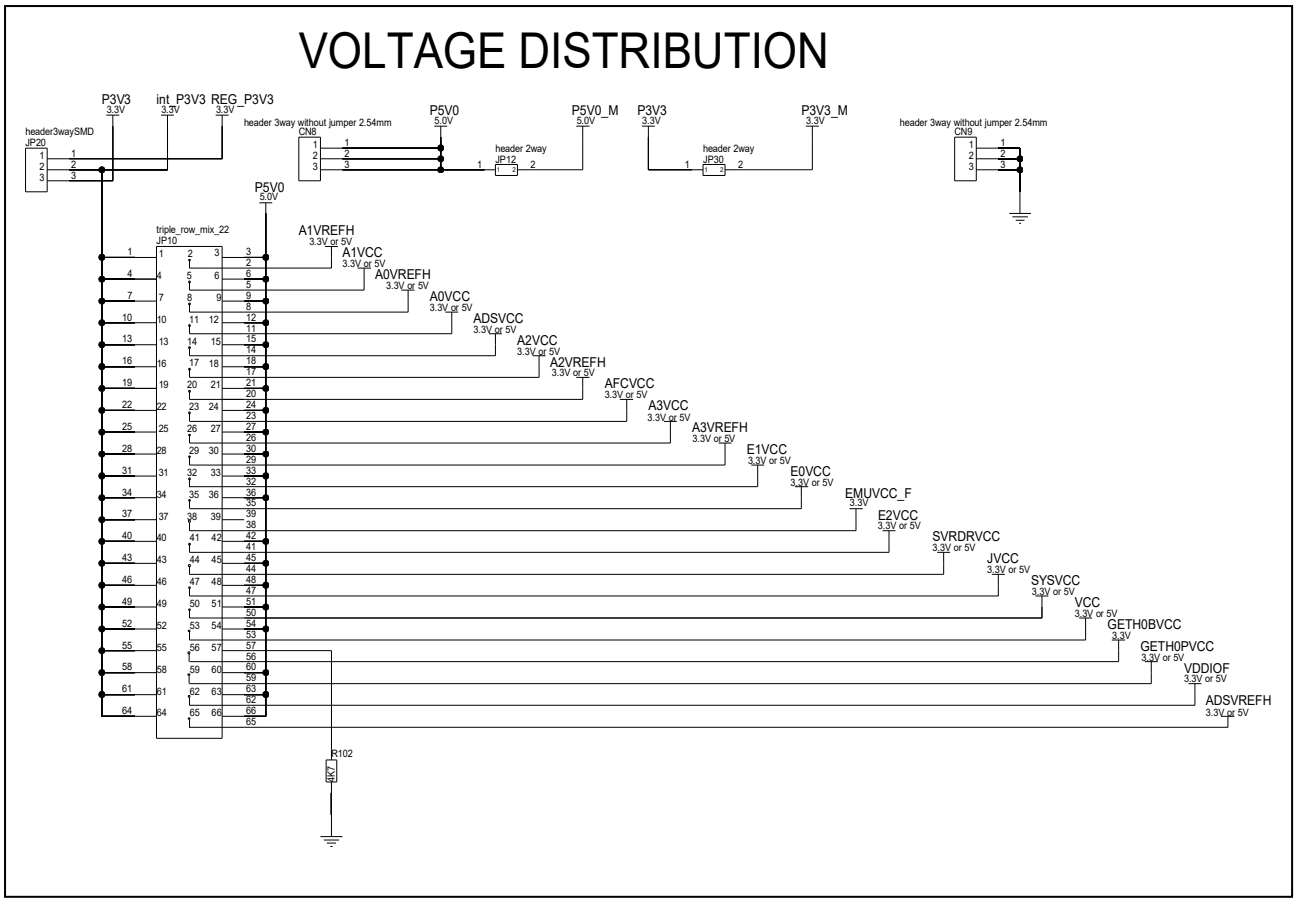


Figure 3.1 Voltage distribution

3.3 Device Core Voltage (VDD) Selection

The device core voltage VDD (typ.1.12 V) can be

- supplied from external via CN11 (voltage IN_1v12)
- generated from the P3V3 power rail by use of the on-board voltage regulator IC3 (voltage reg_vcc_VDD, only if 5.0V is supplied to the piggyback board)
- generated by the on-chip Switching Voltage Regulator (SVR) in combination with device external power transistors TR1, TR12 (voltage SVR_OUTPUT)

Note

The IN_1v12 and reg_vcc_VDD voltages have a level of typical 1.12 V, which is higher than the typical device core voltage VDD of 1.09 V. The 30 mV difference is supposed to compensate voltage drops over the power rails on the board, in particular over the jumpers.

Selection of the VDD source is achieved by use of the jumpers in JP31:

JP31[1-2]: Ext_VDD = IN_1v12

JP31[2-3]: Ext_VDD = reg_vcc_VDD

JP31[4-5]: VDD = Ext_VDD

JP31[5-6]: VDD = SVR_OUTPUT

JP31[10-11] enables the output of the supply voltage to the device debug circuit EMUVDD.

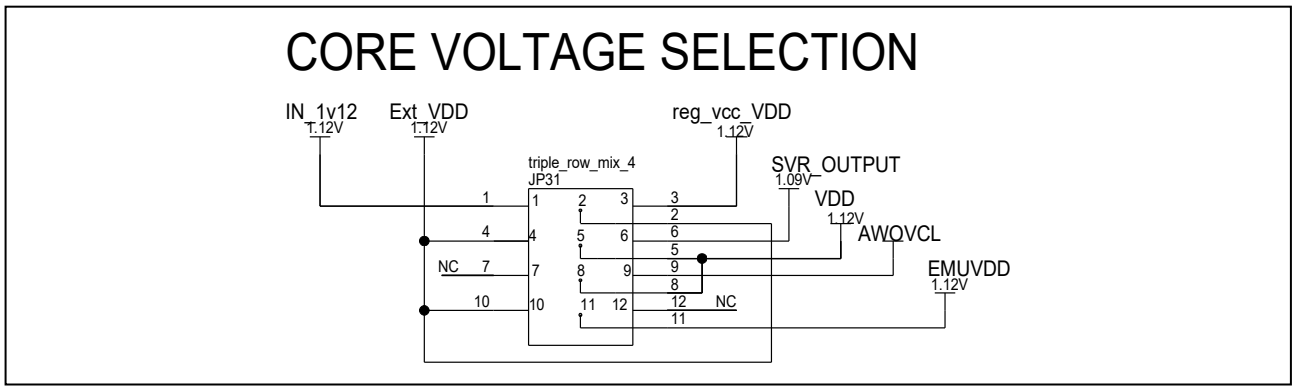


Figure 3.2 Device core voltage (VDD) selection

3.4 Power Supply LEDs

The following green LEDs show the correct operation of various voltages on the piggyback board:

- LED10 for 1.12 V device core voltage VDD
- LED11 for 5.0 V power rail P5V0
- LED12 for 3.3 V power rail P3V3

4. Clock Supply

The device's operation clock can be generated by

- the on-chip main oscillator circuit in combination with an off-chip resonator, connected to the X1, X2 terminals.
- an off-chip oscillator where the clock is fed into the X1 terminal.

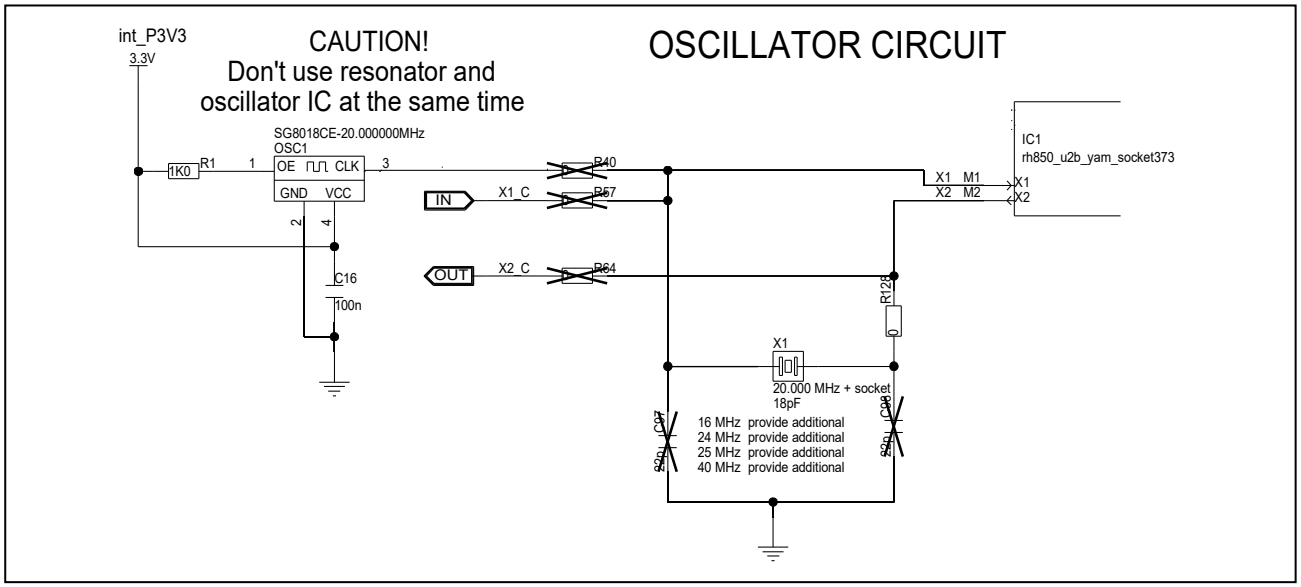


Figure 4.1 Clock supply

4.1 Main Oscillator

The piggyback board provides a socket (X1) to be able to use the on-chip main oscillator with an external resonator.

Several resonators for various main oscillator frequencies (16 MHz, 20 MHz, 24 MHz, 25MHz, 40 MHz) are included in the board package.

By default, the 20MHz resonator is mounted to X1.

For package content please refer to *1.1 Package Components*

CAUTION

Only one oscillator, either X1 or OSC1, can be used at any one time for the main oscillator.

4.2 Programmable Oscillator

Instead of using the on-chip main oscillator a programmable crystal oscillator (OSC1) circuit can be used on the board.

The available footprint and circuitry are designed for a SG-8018CE programmable crystal oscillator from Epson Toyocom. The output of this oscillator can be connected to X1 terminal via resistor R40.

For details about the available circuitry, refer to *Figure 4.1 Clock supply*.

CAUTION

A resonator mounted on socket X1 must not be used in parallel to another clock source.

4.3 X1 and X2 on CN14

To minimize disturbance on the resonator signal the device pins X1 and X2 are by default not connected to a pin header. If needed the pins can be connected to CN14 via 0 Ω resistors:

- Device pin X1: Connect to pin 25 of CN14 via R57 to supply an external clock to the device.
- Device pin X2: Connect to pin 26 of CN14 via R64 for measurement purposes of the clock.

5. Debug and Flash Programming Interfaces

For debugging and flash programming purposes debug and flash programming tools can be connected to the CN4 connector.

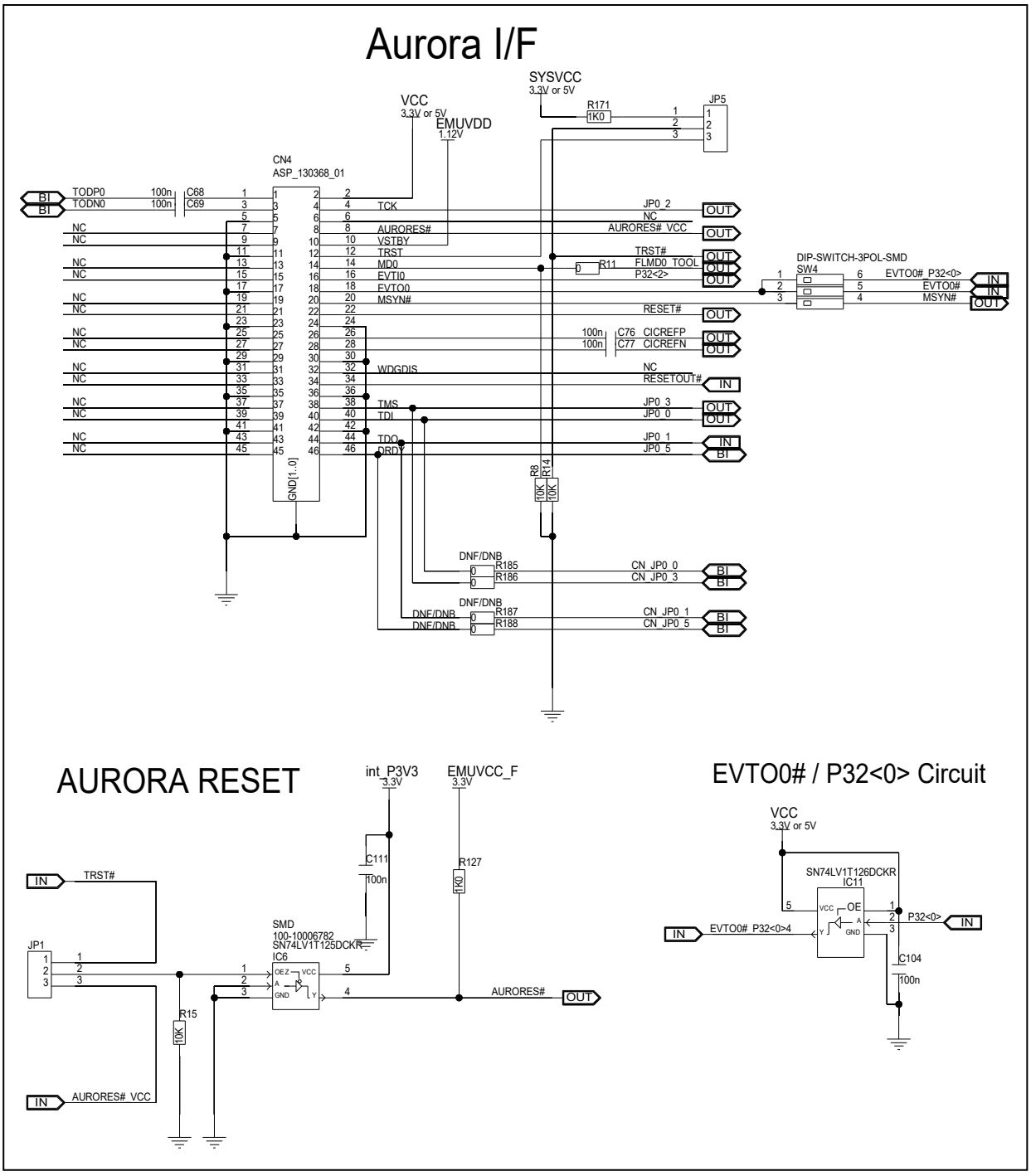


Figure 5.1 Debug connector CN4 and Aurora Reset circuit

Refer to *7.2 Debug Connector CN4* for details about the CN4 pin assignment.

Refer to *8.2 Operation using FCC Device or Mass Production Device* for details about the usage of SW4 and its related signals.

The Renesas standard emulator for RH850/U2B is the E2 emulator. This can be used as emulator for debugging or as flash programmer.

To connect the E2 emulator to Y-RH850-U2B-468PIN-PB-T1-V1 you have to use the adapter Y-RH850-DEBUG-ADAPTER-F14T46.

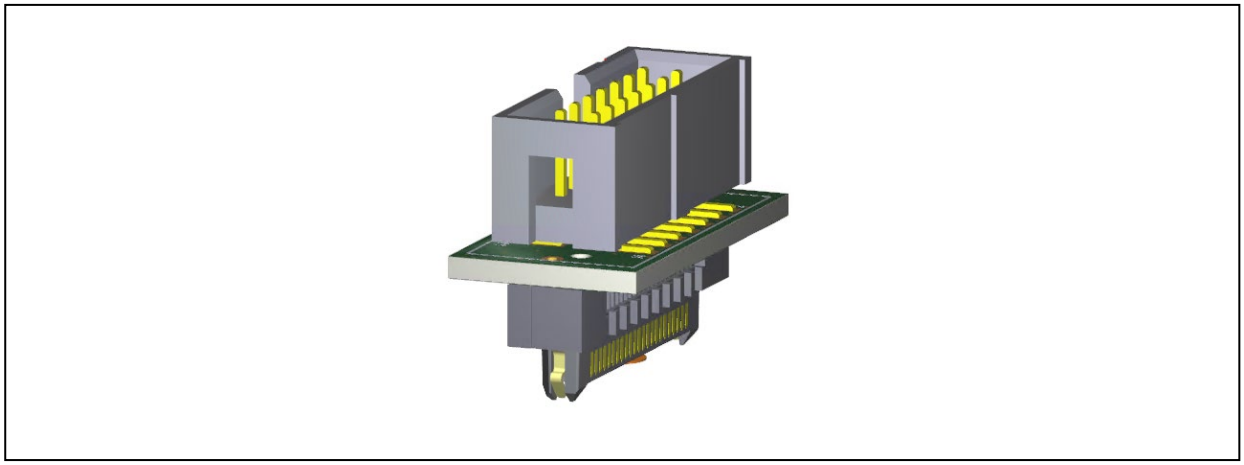


Figure 5.2 Outline view of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

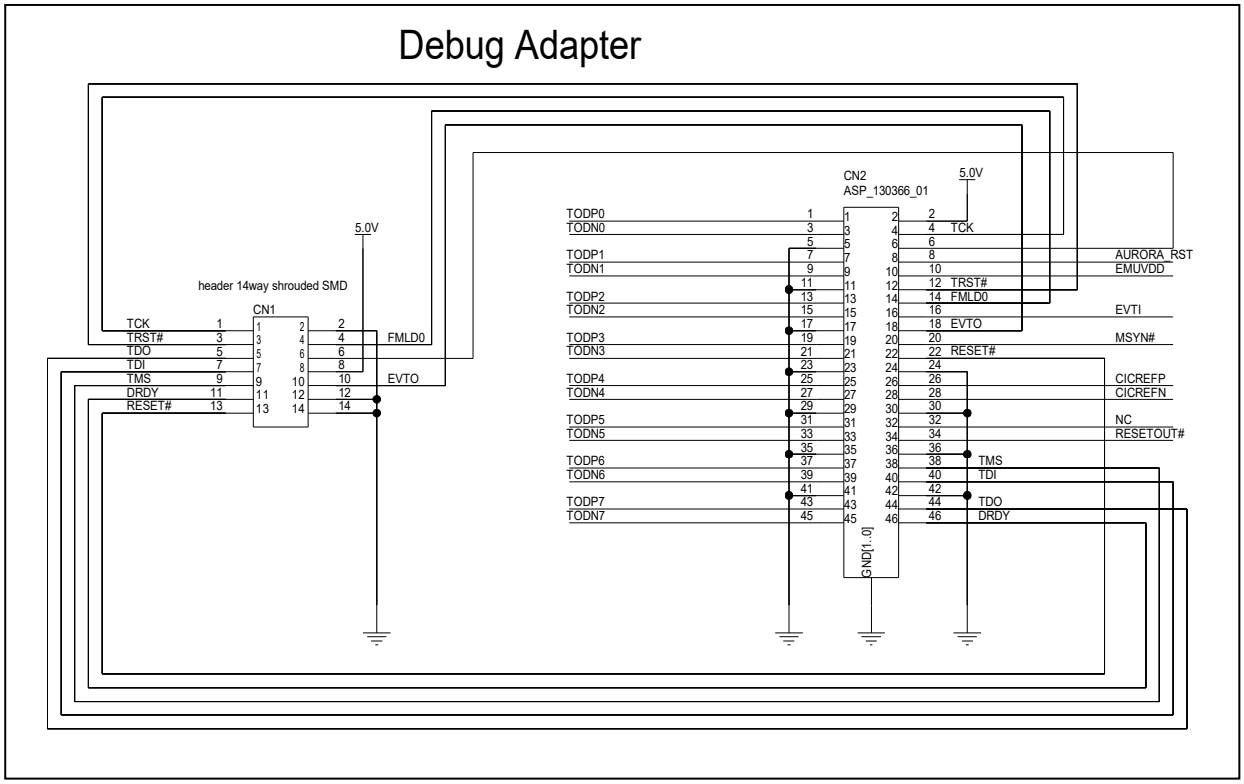


Figure 5.3 Circuit diagram of debug adapter Y-RH850-DEBUG-ADAPTER-F14T46

6. Other Circuitry

6.1 Operation Mode Selection

The piggyback board gives the possibility to configure the following jumpers to select the device operating mode.

Table 6.1 Device operation mode selection jumpers

Jumper	Function
JP46	FLMD0 pin level • JP46[SHORT]: FLMD0 = H level; do not connect a debugger or programming tool. • JP46[OPEN]: FLMD0 is – controlled by debugger or programming tool if a tool is connected via CN4 – GND if no tool is connected
JP47	SBMD pin level (RH850/U2B20 and RH850/U2B24 only, for RH850/U2B10 jumper JP47 can be left open) • JP47[1-2]: connect to SYSVCC (SBMD = 1), please leave JP31_9 open (AWOVCL connected to GND via capacitor C47) • JP47[2-3]: connect to GND (SBMD = 0), please connect JP31[8-9] with a jumper (AWOVCL connect to VDD) • JP47[OPEN]: Use for RH850/U2B10 only
JP48	FLMD1 pin level • JP48[SHORT]: FLMD1 = H level – Port function of port P6_13 can be used • JP48[OPEN]: FLMD1 = L level – JP48 must be open if Serial Programming Mode is used by a debugger or flash programming tool, that is connected to the board
JP2	Enable PWRCTL signaling • JP2[SHORT]: PWRT signal is shown on LED15

CAUTION

Be careful in configuration of the operation mode related pins. The wrong configuration and operation of the device outside of its specification can cause irregular behavior of the device and long-term damage cannot be excluded. Be sure to check the corresponding Hardware User's Manual for details, which modes are specified for the used device.

Note

In most cases the 'normal operating mode' of the device will be used.
This mode is for execution of the user program. The on-chip debug functions also use this mode.

To select the 'normal operating mode' of the device, the FLMD0 pin must be pulled low. To do so, please leave jumper JP46 open.

All other jumpers related to the mode selection can be left open.

6.2 RESET Switch

The SW1 is used to issue a RESET to the device.

The SW1 toggle switch allows to activate the RESET in two different ways:

- SW1 in left '5-4(ON)' position: temporary reset
  Releasing the switch's lever returns the switch to its middle 'OFF' position and thus releases the reset.
- SW1 in right '5-6 ON' position: permanent reset
  For reset release the switch has to be moved back manually to its middle 'OFF' position.

The left and right switch position is defined from the side of the part number marking, which is highlighted with a red arrow in the figure below.

The lighted red LED13 indicates that SW1 is "on", i.e. in position '5-4 (ON)' or '5-6 ON'.

Note

LED13 does not light up when RESET is asserted by any other means than SW1.

Switch function	Viewed from part no. marking side		
			
NKK G19AP	ON	OFF	ON
Connecting terminals	5 – 4 momentary	None permanent	5 – 6 permanent

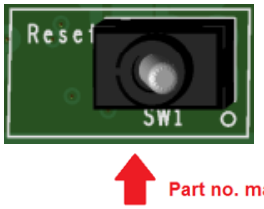


Figure 6.1 Operation of RESET switch

6.3 Signaling LEDs

Eight LEDs are provided to allow visual observation of the output state of device port pins.

Device pins P11_0 to P11_3, P11_5 to P11_7 and P22_0 are connected to the odd pins of the pin header JP7, while the LEDs 2 to 9 are connected to the even JP7 pins.

Thus, the LEDs can be either connected to

- the device port pins P11_0 to P11_3, P11_5 to P11_7 or P22_0 by closing the connection on JP7 using a jumper, or
- any device pin by connecting the pin (from the connectors CN5, CN13, CN14, CN15 or CN16) directly with the even JP7 pins using a separate cable.

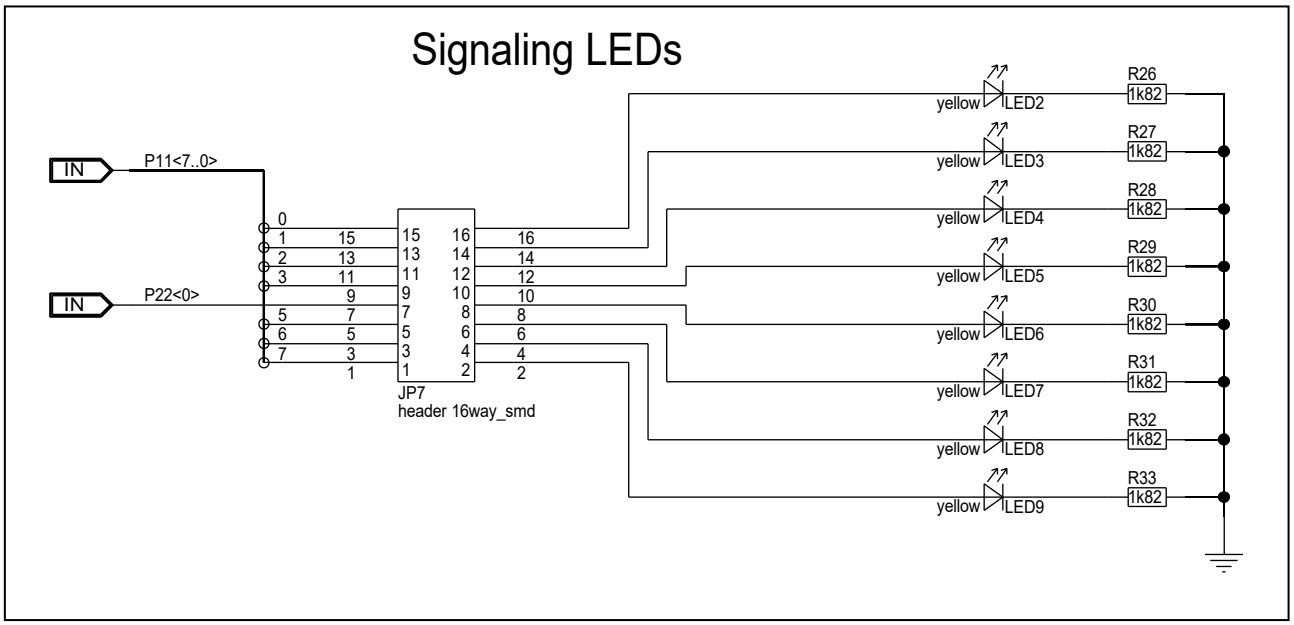


Figure 6.2 Circuit diagram for signaling LEDs

6.4 Pull-Up/Pull-Down Pin Header

The Pull-up/Pull-down pin header CN29 provides fixed voltage levels at its pins, which can be used to pull-up/pull-down a signal on the board or the device by connecting a CN29 pin to the signal via a separate cable.

All pull-up or pull-down resistors use 1kΩ resistors.

The CN29 pins have following pull-up or pull-down voltage levels:

- All odd numbered pins are connected to L level.
- Even numbered pins 2, 4, 6, 8 are connected to int_P3V3, which means 3.3 V. The source for the 3.3V supply is selected using jumper JP20:
  - JP20[1-2]: 3.3 V input from external power supply via connector CN21 or from a connected main board (jumper JP30[1-2] closed).
  - JP20[2-3]: 3.3 V comes from REG_P3V3 generated by the onboard voltage regulator.
- Even numbered pins 10, 12, 14, 16 are connected to P5V0, which means 5.0 V. P5V0 is either provided from external power supply (connector CN34) or from a connected main board (jumper JP12[1-2] closed).

Refer to *7.9 Pull-Up/Pull-Down Pin Header CN29* for CN29 details.

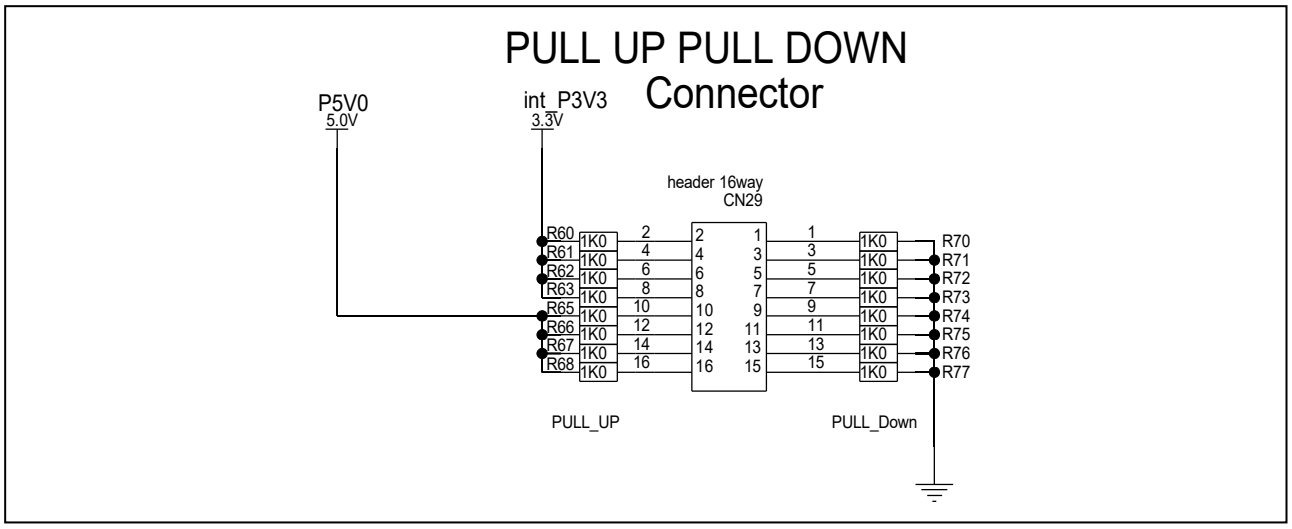


Figure 6.3 Circuit diagram for pull up / pull down signals

6.5 Renesas High-Speed Bus RHSB0

The piggyback board provides access to the high-speed bus interface RHSB0 on connector CN24.

The signal output of RHSB0 to connector CN24 is enabled by switch SW5-1.

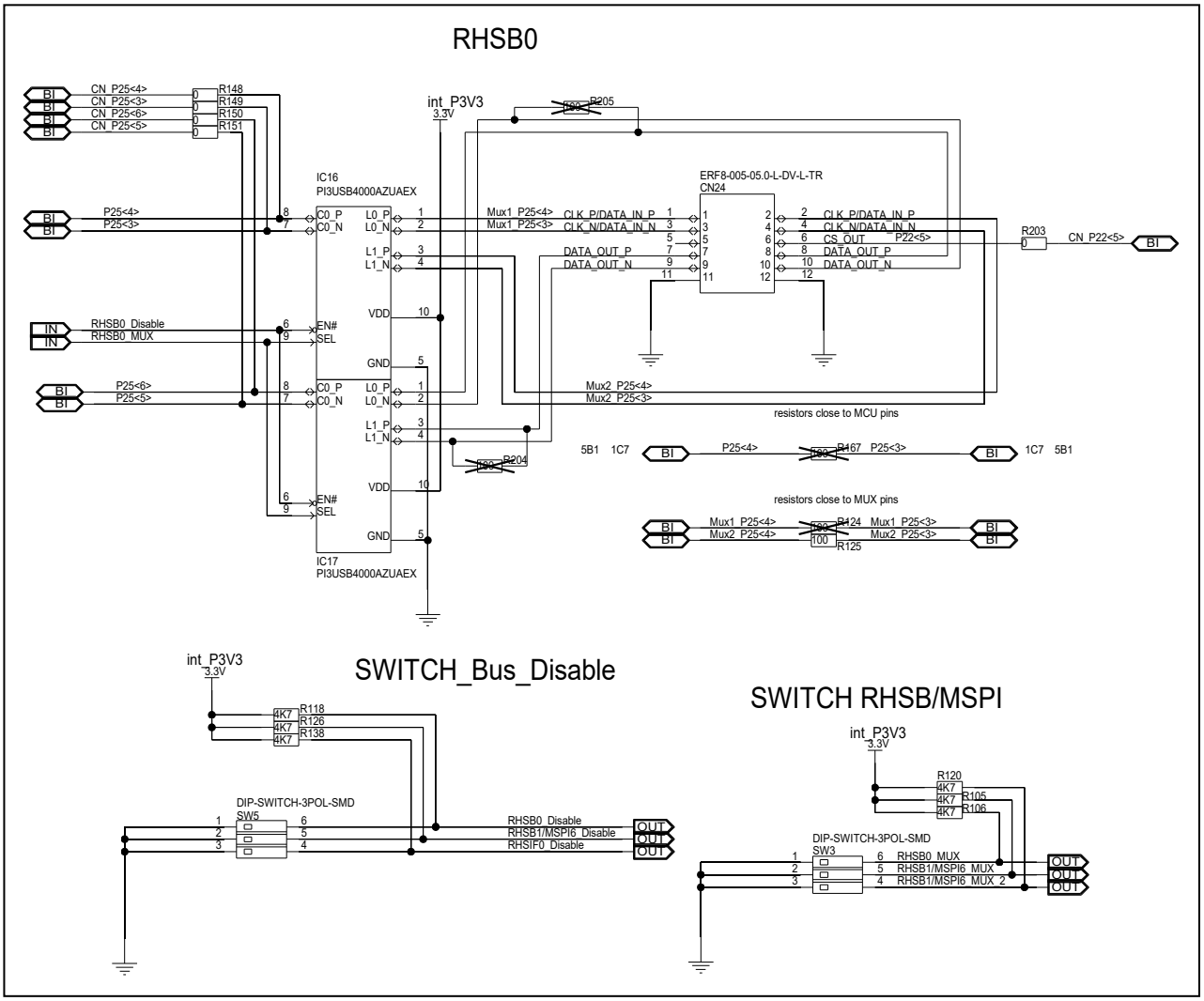


Figure 6.4 Circuit diagram for RHSB0 interface

The pin configuration on connector CN24 can be modified using the RHSB0_MUX signal from switch SW3-1.

Refer to *7.6 RHSB0 Connector CN24* for the possibility to configure the pin assignment on CN24.

CAUTION

**The piggyback board can apply 100Ω termination resistors for different use cases.
See in this document the attachment 'Guideline for termination resistors.xlsx' for the detailed information.**

Notes

1. The signals on the RHSB0 interface are connected to connectors CN3, CN6 and CN14. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R148-R151, R203.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.6 Renesas High-Speed Bus RHSB1 and Multichannel Serial Peripheral Interface MSPI6

The CN23 connector can be used to connect to the device's RHSB1 and MSPI6 interface.

The signal output of RHSB1 or MSPI6 to connector CN23 is enabled by switch SW5-2.

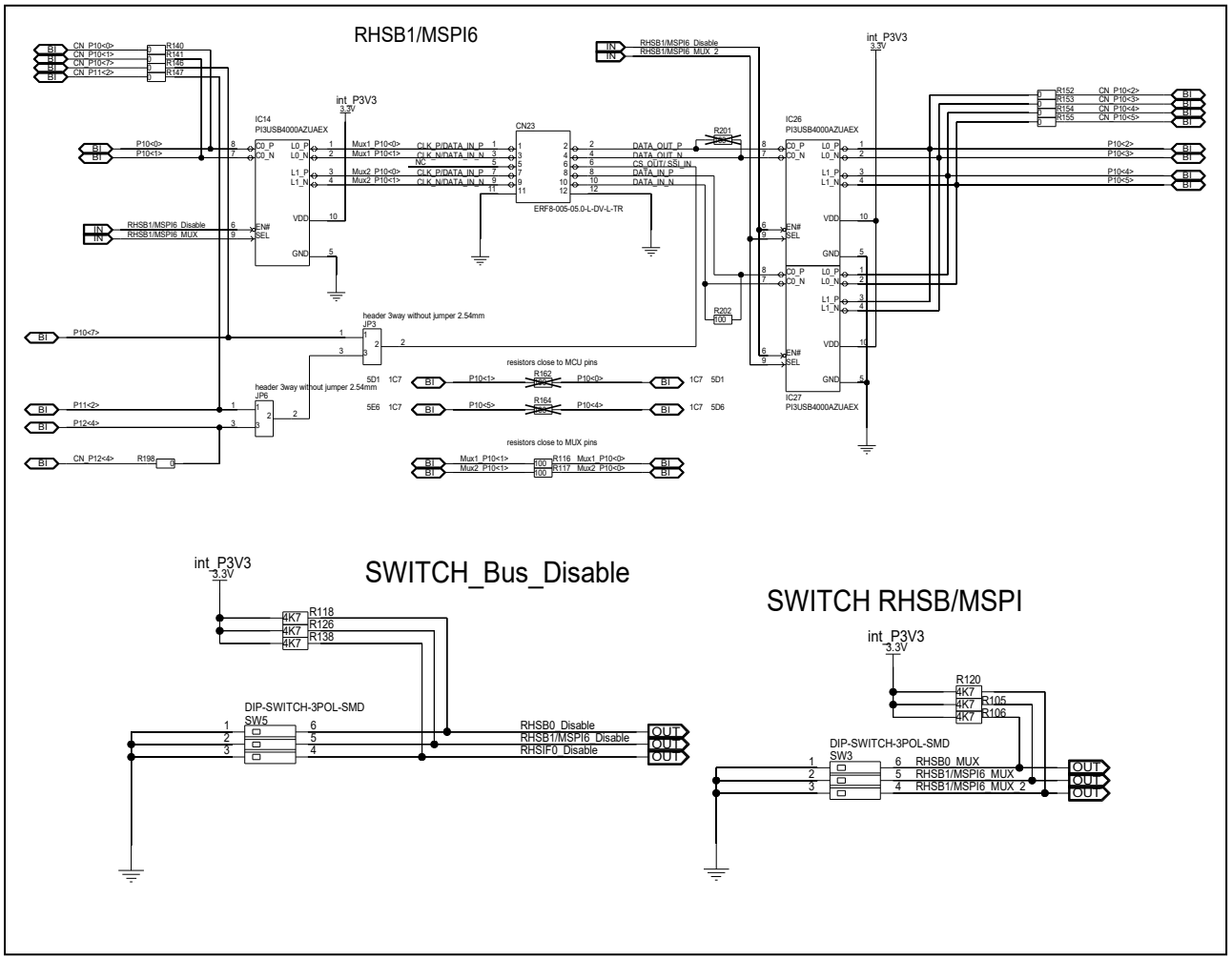


Figure 6.5 Circuit diagram for RHSB1/MSPI6 interface

The pin configuration on connector CN23 can be changed using the RHSB1/MSPI6_MUX signal from switch SW3-2 and the RHSB1/MSPI6_MUX_2 signal from switch SW3-3.

Refer to *7.5 RHSB1/MSPI6 Connector CN23* for the CN23 pin assignment.

CAUTION

**The piggyback board can apply 100Ω termination resistors for different use cases.
See in this document the attachment 'Guideline for termination resistors.xlsx' for the detailed information.**

Notes

1. The signals on the RHSB1/MSPI6 interface are connected to connectors CN1–CN3, CN5 and CN15. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R140, R141, R146, R147, R152-R155, R198.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.7 Renesas Multichannel Serial Peripheral Interface MSPI9

Connector CN26 provides access to the MSPI9 interface.

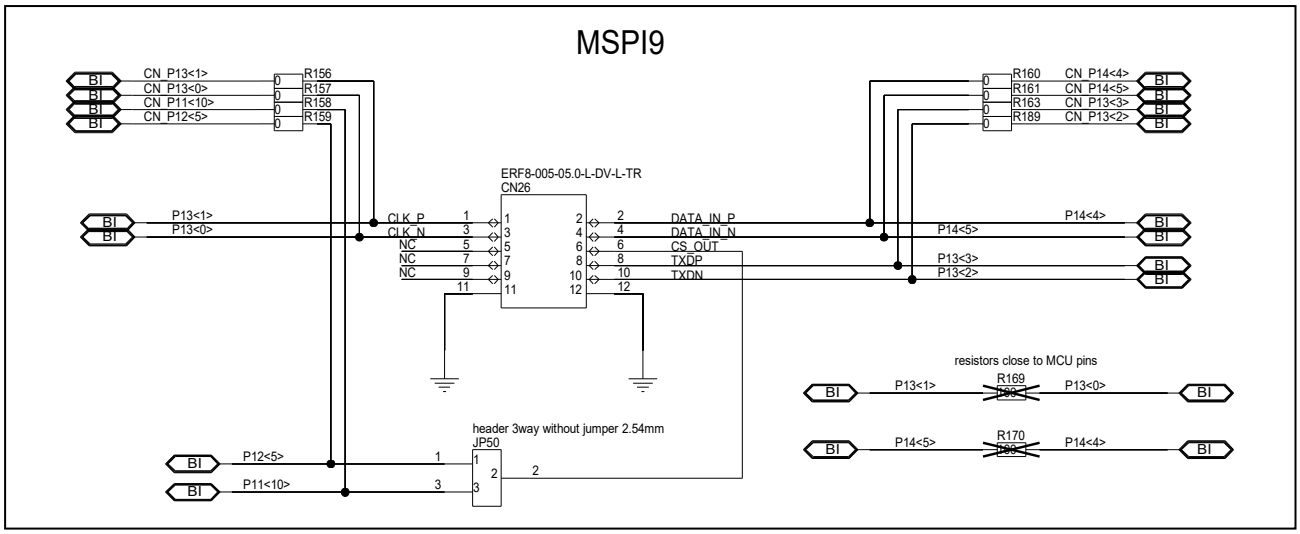


Figure 6.6 Circuit diagram for MSPI9 interface

Refer to *7.7 MSPI9 Connector CN26* for the CN26 pin assignment.

Notes

The signals on the RHSIF0 interface are connected to connectors CN1 - CN3, CN6, CN14 and CN15. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R156-R161, R163, R189.

6.8 Renesas High-Speed Serial I/F RHSIF0

Connector CN27 provides access to the RHSIF0 interface.

The signal output of RHSIF0 to connector CN27 is enabled by switch SW5-3.

Rx and Tx signals available at CN27 can be swapped by setting the jumper JP4:

- JP4[SHORT]:
  - RXDP/RXDN at CN27 pins 1 and 3
  - TXDP/TXDN at CN27 pins 7 and 9
- JP4[OPEN]:
  - RXDP/RXDN at CN27 pins 7 and 9
  - TXDP/TXDN at CN27 pins 1 and 3

Refer to *7.8 RHSIF0 Connector CN27* for the CN27 pin assignment.

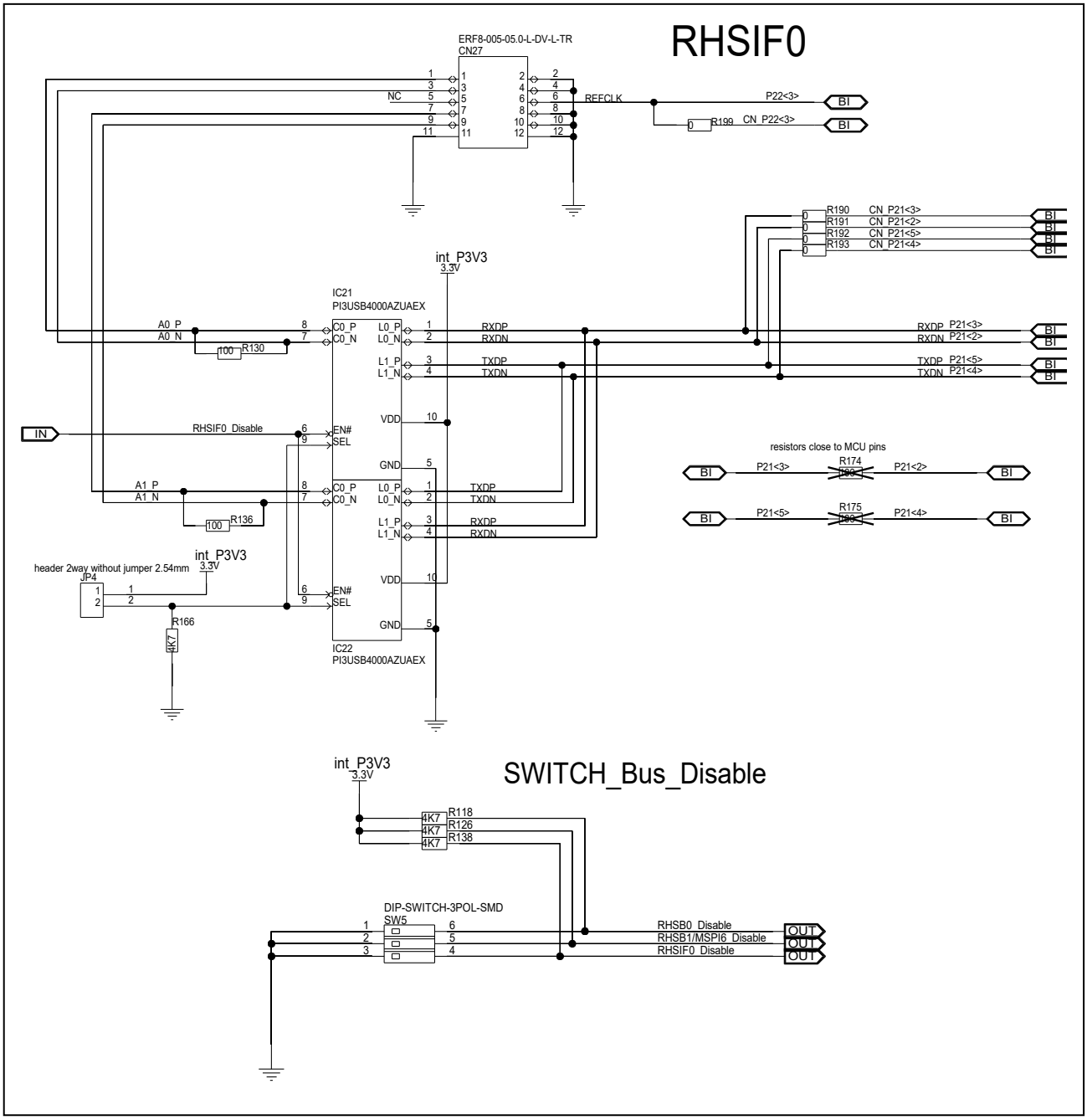


Figure 6.7 Circuit diagram for RHSIF0 interface

Notes

1. The signals on the RHSIF0 interface are connected to connectors CN1, CN3, CN6 and CN14. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R190-R193, R199.
2. Swapping the Rx/Tx signals allows board-to-board communication e.g. with another piggyback board via separate cables.

6.9 Automotive Ethernet Interfaces ETN0 and ETN1

The Ethernet interfaces are only populated on pcb of board version D018705_06_V01. But the devices that can be used with this piggyback board do not support Ethernet SGMII interfaces. Thus, Ethernet SGMII interfaces cannot be used on pcb of board version D018705_06_V01.

The Ethernet interfaces are not populated on pcb of board version D018705_06_V02.

6.10 Low Pass Filter

The piggyback board includes a set of low pass filters to filter input signals to analog input ports.

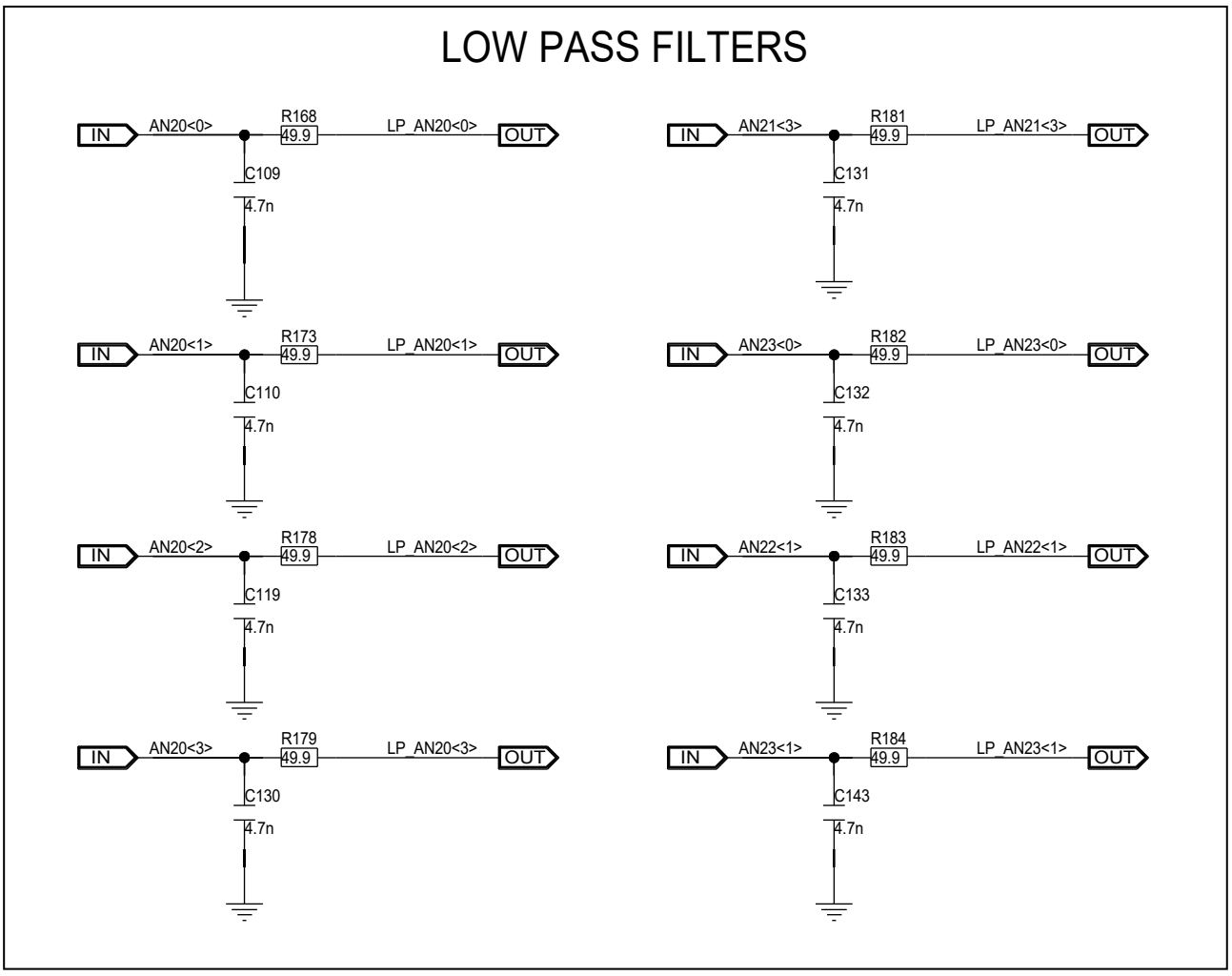


Figure 6.8 Circuit diagram for low pass filters

The analog input ports on RH850/U2B can be accessed through the device port connectors CN13 and CN15. Inputs including the low pass filter can be identified by the leading "LP_" in the pin name.

Please refer to *7.3.1 Device Ports Connector CN5* and *7.3.5 Device Ports Connector CN15* for details on the pin assignments.

7. Connectors

7.1 Connectors to the Main Board CN1 to CN3

Three connectors (CN1 to CN3) are available to connect the piggyback board to a Main Board.

The signals of each connector are summarized in the following tables.

Note

Regarding the function on the Main Board, please refer to the User's Manual of any supported Main Board.
Refer to *1.2 Supported Main Boards* for a list of supported Main Boards.

7.1.1 Main Board Connector CN1

Table 7.1 Main board connector CN1

Pin	Main Board function	Piggyback board device port	Pin	Main Board function	Piggyback board device port
1	VDDA	–	2	VDDA	–
3	VDDA	–	4	VDDA	–
5	RESET	RESET#	6	NMI	P25_2
7	WAKE	–	8	–	–
9	INT0	P23_2	10	INT1	P23_3
11	INT2	P23_4	12	INT3	P23_5
13	–	–	14	–	–
15	UART0TX	P12_6	16	UART1TX	P33_1
17	UART0RX	CN_P12_5 *	18	UART1RX	P33_0
19	LIN0TX	P34_0	20	LIN1TX	P20_7
21	LIN0RX	P34_2	22	LIN1RX	P20_6
23	IIC0SCL	CN_P10_7 *	24	IIC1SCL	P00_6
25	IIC0SDA	P10_8	26	IIC1SDA	P00_7
27	CAN0TX	CN_P21_4 *	28	CAN1TX	P02_7
29	CAN0RX	CN_P21_5 *	30	CAN1RX	P02_10
31	SENT0RX	P00_0	32	SENT1RX	P00_4
33	SENT0SPCO	P00_1	34	SENT1SPCO	P00_5
35	PSI5SRX0	P02_10	36	PSI5RX0	P02_0
37	PSI5STX0	P02_8	38	PSI5TX0	P02_1

Table 7.1 Main board connector CN1 (cont'd)

Pin	Main Board function	Piggyback board device port
39	PSI5SCLK0	P02_6
41	FLX0TX	P12_1
43	FLX0RX	P12_7
45	FLX1TX	P22_11
47	FLX1RX	P12_8
49	–	–
51	ETH0MDIO	CN_P10_4 *
53	ETH0RXD0	P11_3
55	ETH0RXD1	CN_P11_2 *
57	ETH0RXD2	CN_P10_3 *
59	ETH0RXD3	CN_P10_0 *
61	ETH0RXCLK	CN_P10_1 *
63	ETH0RXER	P11_6
65	ETH0CRSDV	–
67	ETH0RXDV	P11_7
69	ETH0RESET	P10_8
71	–	–
73	USB0UDMF	–
75	USB0UDPF	–
77	–	–
79	–	–
81	–	–
83	–	–
85	DIGIO_0	P11_0
87	DIGIO_2	CN_P11_2 *
89	DIGIO_4	P22_0
91	DIGIO_6	P11_6
93	DIGIO_8	P11_8
95	DIGIO_10	CN_P10_0 *
97	DIGIO_12	CN_P10_2 *

Pin	Main Board function	Piggyback board device port
40	–	–
42	FLX0EN	P12_0
44	FLXSTPWT	CN_P12_4 *
46	FLX1EN	P12_9
48	FLXCLK	–
50	–	–
52	ETH0MDC	CN_P10_2 *
54	ETH0TXD0	P11_8
56	ETH0TXD1	P11_9
58	ETH0TXD2	P11_5
60	ETH0TXD3	P11_1
62	ETH0TXCLK	P11_4
64	ETH0TXER	CN_P11_10 *
66	ETH0TXEN	P11_0
68	ETH0COL	–
70	ETH0LINK	CN_P10_7 *
72	–	–
74	USB0UDMH	–
76	USB0UDPH	–
78	–	–
80	–	–
82	–	–
84	–	–
86	DIGIO_1	P11_1
88	DIGIO_3	P11_3
90	DIGIO_5	P11_5
92	DIGIO_7	P11_7
94	DIGIO_9	P11_9
96	DIGIO_11	CN_P10_1 *
98	DIGIO_13	CN_P10_3 *

Table 7.1 Main board connector CN1 (cont'd)

Pin	Main Board function	Piggyback board device port	Pin	Main Board function	Piggyback board device port
99	DIGIO_14	CN_P10_4 *	100	DIGIO_15	CN_P10_5 *
101	–	–	102	–	–
103	MUX0	P34_0	104	MUX1	P34_2
105	MUX2	P34_1	106	–	–
107	ADC0	AN02_0	108	ADC1	AN02_1
109	ADC2	AN02_2	110	ADC3	AN02_3
111	ADC4	AN03_0	112	ADC5	AN03_1
113	ADC6	AN03_2	114	ADC7	AN03_3
115	VDDIOF	–	116	VDDIOF	–
117	VDDB	–	118	VDDB	–
119	VDDB	–	120	VDDB	–
121	GND	–	122	GND	–
123	GND	–	124	GND	–
125	GND	–	126	GND	–
127	GND	–	128	GND	–

Note * By default these signals are connected to CN1. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R140, R141, R146, R147, R152-R155, R159, R192, R193, R198.

7.1.2 Main Board Connector CN2

Table 7.2 Main board connector CN2

Pin	Function	Device port	Pin	Function	Device port
1	CAN2TX	P02_1	2	CAN3TX	P02_2
3	CAN2RX	P02_4	4	CAN3RX	P02_3
5	CAN4TX	CN_P10_5 *	6	CAN5TX	P14_2
7	CAN4RX	P10_6	8	CAN5RX	P14_0
9	LIN2TX	P22_2	10	LIN3TX	P32_6
11	LIN2RX	CN_P22_3 *	12	LIN3RX	P32_4
13	LIN4TX	P12_6	14	LIN5TX	P33_1
15	LIN4RX	CN_P12_5 *	16	LIN5RX	P33_0
17	LIN6TX	P00_11	18	LIN7TX	P01_7
19	LIN6RX	P00_10	20	LIN7RX	P01_5

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function	Device port	Pin	Function	Device port
21	LIN8TX	P22_11	22	LIN9TX	P10_12
23	LIN8RX	P22_12	24	LIN9RX	P10_11
25	LIN10TX	P10_14	26	LIN11TX	P23_6
27	LIN10RX	P10_13	28	LIN11RX	P23_5
29	LIN12TX	P32_3	30	LIN13TX	P33_5
31	LIN12RX	P32_2	32	LIN13RX	P33_2
33	LIN14TX	P33_13	34	LIN15TX	P20_3
35	LIN14RX	P33_11	36	LIN15RX	P20_2
37	–	–	38	–	–
39	–	–	40	–	–
41	–	–	42	–	–
43	–	–	44	–	–
45	–	–	46	–	–
47	CAN6TX	P02_6	48	CAN7TX	P20_5
49	CAN6RX	P02_5	50	CAN7RX	P20_4
51	CAN8TX	P33_3	52	CAN9TX	P34_4
53	CAN8RX	P33_6	54	CAN9RX	P34_3
55	–	–	56	–	–
57	–	–	58	–	–
59	–	–	60	–	–
61	LIN16TX	P02_8	62	LIN17TX	P34_3
63	LIN16RX	P02_9	64	LIN17RX	P34_4
65	LIN18TX	P14_6	66	LIN19TX	P14_8
67	LIN18RX	CN_P14_5 *	68	LIN19RX	P14_7
69	LIN20TX	P00_3	70	LIN21TX	P00_8
71	LIN20RX	P00_2	72	LIN21RX	P00_9
73	LIN22TX	CN_P10_0 *	74	LIN23TX	P32_1
75	LIN22RX	CN_P10_1 *	76	LIN23RX	P32_0
77	–	–	78	–	–
79	SFMA0CLK	P20_4	80	SFMA0SSL	P20_5

Table 7.2 Main board connector CN2 (cont'd)

Pin	Function	Device port	Pin	Function	Device port
81	SFMA0IO0	P20_0	82	SFMA0IO1	P20_1
83	SFMA0IO2	P20_2	84	SFMA0IO3	P20_3
85	–	–	86	–	–
87	MMCA0CLK	CN_P13_0 *	88	MMCA0CMD	CN_P14_5 *
89	MMCA0DAT0	CN_P13_1 *	90	MMCA0DAT1	CN_P13_2 *
91	MMCA0DAT2	CN_P13_3 *	92	MMCA0DAT3	P14_1
93	MMCA0DAT4	P14_0	94	MMCA0DAT5	P14_2
95	MMCA0DAT6	P14_3	96	MMCA0DAT7	CN_P14_4 *
97	–	–	98	–	–
99	ETH1MDIO	P14_2	100	ETH1MDC	P14_3
101	ETH1RXD0	P13_8	102	ETH1TXD0	P14_12
103	ETH1RXD1	P13_9	104	ETH1TXD1	P14_10
105	ETH1RXD2	P13_10	106	ETH1TXD2	P14_7
107	ETH1RXD3	P13_11	108	ETH1TXD3	P14_9
109	ETH1RXCLK	P13_13	110	ETH1TXCLK	P14_11
111	ETH1RXER	P13_14	112	ETH1TXER	P14_8
113	ETH1CRSDV	–	114	ETH1TXEN	P14_6
115	ETH1RXDV	P13_12	116	ETH1COL	–
117	ETH1RESET	P12_3	118	ETH1LINK	CN_P14_4 *
119	–	–	120	–	–
121	GND	–	122	GND	–
123	GND	–	124	GND	–
125	GND	–	126	GND	–
127	GND	–	128	GND	–

Note * By default these signals are connected to CN2. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R140, R141, R155-R157, R159-R161, R163, R189, R199.

7.1.3 Main Board Connector CN3

Table 7.3 Main board connector CN3

Pin	Function	Device port	Pin	Function	Device port
1	CSI0CS0	P23_2	2	CSI0CLK	P23_7
3	CSI0CS1	P23_4	4	CSI0SI (MSPI3)	P23_6

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port	Pin	Function	Device port
5	CSI0CS2	P23_3	6	CSI0SO	P23_5
7	CSI0CS3	P23_0	8	–	–
9	–	–	10	CSI1CS1	P33_4
11	–	–	12	–	–
13	PSI5SRX1	P33_2	14	PSI5RX1	P02_9
15	PSI5STX1	P33_0	16	PSI5TX1	P02_7
17	PSI5SCLK1	P33_1	18	–	–
19	–	–	20	–	–
21	CSI1CS2	P33_7	22	CSI1CS3	P33_8
23	–	–	24	CSI1CS0	P22_5
25	–	–	26	DIGIO_24	P22_6
27	–	–	28	CSI1SO	CN_P22_3 *1
29	CSI1SCLK	P33_6	30	CSI1SI	P33_3
31	–	–	32	–	–
33	MOT0ADU (RFU)	AN00_0	34	AD0 (RFU)	AN10_0
35	MOT0ADV (RFU)	AN00_1	36	AD1 (RFU)	AN10_1
37	MOT0ADW (RFU)	AN00_2	38	AD2 (RFU)	AN10_2
39	MOT0RDCS1 (RFU)	AN24_3	40	RDCS1 (RFU)	AN27_2
41	MOT0RDCS3 (RFU)	AN24_2	42	RDCS3 (RFU)	AN27_1
43	MOT0RDCS2 (RFU)	AN24_0	44	RDCS2 (RFU)	AN26_0
45	MOT0RDCS4 (RFU)	AN24_1	46	RDCS4 (RFU)	AN26_2
47	MOT0RDCCOM (RFU)	AN25_1	48	RDCCOM (RFU)	AN27_3
49	MOT0RDCRSO (RFU)	AN25_0	50	RDCRSO (RFU)	AN26_3
51	–	–	52	–	–
53	–	–	54	–	–
55	AD1_0	AN11_0	56	AD1_1	AN11_1
57	AD1_2	AN11_2	58	AD1_3	AN11_3
59	AD1_4	AN12_0	60	AD1_5	AN12_1
61	AD1_6	AN12_2	62	AD1_7	AN12_3
63	PWM0	P33_0	64	PWM1	P33_1

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
65	PWM2	P33_2
67	PWM4	P33_4
69	PWM6	P33_6
71	DIGIO16	P20_0
73	DIGIO18	P20_2
75	DIGIO20	P20_4
77	DIGIO22	P20_6
79	ENC0	CN_P10_5 *1
81	–	–
83	MOT0U_P (RFU)	CN_P21_2 *1
85	MOT0U_N (RFU)	CN_P21_3 *1
87	MOT0V_P (RFU)	CN_P21_4 *1
89	MOT0V_N (RFU)	CN_P21_5 *1
91	MOT0W_P (RFU)	CN_P25_4 *1
93	MOT0W_N (RFU)	CN_P25_3 *1
95	–	–
97	–	–
99	–	–
101	GND	–
103	–	AN04_1
105	–	AN04_3
107	–	AN01_3
109	–	AN01_2
111	–	AN23_3
113	–	AN22_2
115	–	AN23_2
117	–	AN22_3
119	GND	–
121	GND	–
123	GND	–

Pin	Function	Device port
66	PWM3	P33_3
68	PWM5	P33_5
70	PWM7	P33_7
72	DIGIO17	P20_1
74	DIGIO19	P20_3
76	DIGIO21	P20_5
78	DIGIO23	P20_7
80	ENC1	P10_6
82	–	–
84	O1 (RFU)	CN_P13_0 *1
86	O2 (RFU)	CN_P13_1 *1
88	O3 (RFU)	CN_P13_2 *1
90	O4 (RFU)	CN_P13_3 *1
92	O5 (RFU)	CN_P14_5 *1
94	O6 (RFU)	CN_P14_4 *1
96	–	–
98	–	–
100	ETH0_SO_P	CN_ETH0_SG_TXD_P *2
102	ETH0_SO_N	CN_ETH0_SG_TXD_N *2
104	–	–
106	ETH0_SI_P	CN_ETH0_SG_RXD_P *2
108	ETH0_SI_N	CN_ETH0_SG_RXD_N *2
110	–	–
112	ETH1_SO_P	CN_ETH1_SG_TXD_P *2
114	ETH1_SO_N	CN_ETH1_SG_TXD_N *2
116	–	–
118	ETH1_SI_P	CN_ETH1_SG_RXD_P *2
120	ETH1_SI_N	CN_ETH1_SG_RXD_N *2
122	GND	–
124	GND	–

Table 7.3 Main board connector CN3 (cont'd)

Pin	Function	Device port
125	GND	–
127	GND	–

Pin	Function	Device port
126	GND	–
128	GND	–

Note *1 By default these signals are connected to CN3. In order to minimize signal interference, they can be disconnected by removing 0 Ω resistors R148, R149, R155-R157, R160, R161, R163, R189-R193, R199.

*2 By default these signals are not connected to CN3 in order to minimize signal interference. If required they can be connected via 0 Ω resistors R22, R23, R34-R39.

(RFU) Ready for use with future main boards, actually main boards do not support this function.

7.2 Debug Connector CN4

Table 7.4 On-chip debug connector CN4

Pin	Function	Device port
1		TODP0
3		TODN0
5	GND	
7	–	–
9	–	–
11	GND	
13	–	–
15	–	–
17	GND	
19	–	–
21	–	–
23	GND	
25	–	–
27	–	–
29	GND	
31	–	–
33	–	–
35	GND	
37	–	–
39	–	–
41	GND	
43	–	–
45	–	–

Pin	Function	Device port
2	VCC	
4	TCK	JP0_2
6	–	–
8	AURORES#	AURORES#_VCC
10	VSTBY	EMUVDD
12	TRST	Controlled by JP5 JP5 [1-2]: SYSVCC JP5 [2-3]: TRST#
14	MD0	FLMD0_TOOL
16	EVTI0	P32_2
18	EVTO0	Controlled by SW4 SW4-2 [ON]: EVTO0# SW4-3 [ON]: EVTO0#_P32_0
20	MSYN#	MSYN#
22		RESET#
24	GND	
26		CICREFP
28		CICREFN
30	GND	
32	WDGDIS	–
34		RESETOUT#
36	GND	
38	TMS	JP0_3
40	TDI / LPDIO / FPDR	JP0_0
42	GND	
44	TDO / LPDO / FPDT	JP0_1
46	DRDY	JP0_5

7.3 Device Ports Connectors CN5, CN6, CN13, CN14 and CN15

The device port connectors enable easy connection to almost all ports of the device.

CAUTION

The pin headers are directly connected to the pins, therefore special care must be taken to avoid any electrostatic or other damage to the device.

7.3.1 Device Ports Connector CN5

Table 7.5 Device ports connector CN5

Pin	PCB Silk	Device port
1	C1	AN05_0
2	C2	AN06_2
3	C3	AN04_1
4	C4	AN03_2
5	C5	AN02_1
6	C6	AN02_0
7	C7	AN00_3
8	C8	AN00_1
9	C9	LP_ AN20_3
10	C10	LP_ AN20_0
11	C11	LP_ AN22_1
12	C12	LP_AN23_0
13	C13	AN23_2
14	C14	AN22_2
15	C15	AN25_0
16	C16	AN24_1
17	C17	AN24_2
18	C18	AN26_2
19	C19	AN26_3
20	C20	AN31_0
21	C21	AN31_1
22	C22	AN31_3
23	C23	P02_11

Table 7.5 Device ports connector CN5 (cont'd)

Pin	PCB Silk	Device port
24	C24	P00_5
25	C25	P00_10
26	C26	P02_6
27	C27	P02_5
28	C28	P00_2
29	C29	P00_7
30	C30	P02_0
31	C31	P01_4
32	C32	P01_6
33	C33	P10_8
34	C34	CN_P10_7 *
35	C35	P10_13
36	C36	CN_P10_2 *
37	C37	P10_10
38	C38	P11_9
39	C39	P11_8
40	C40	P11_0

Note * By default these signals are connected to CN5. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R146 and R155.

7.3.2 Device Ports Connector CN6

Table 7.6 Device ports connector CN6

Pin	PCB Silk	Device port
1	H1	P30_2
2	H2	P33_6
3	H3	P33_7
4	H4	P34_3
5	H5	P34_2
6	H6	P32_1
7	H7	P32_2
8	H8	P32_4
9	H9	P23_0

Table 7.6 Device ports connector CN6 (cont'd)

Pin	PCB Silk	Device port
10	H10	P23_6
11	H11	P23_2
12	H12	P23_4
13	H13	ETH_SG_REFCLK
14	H14	P22_0
15	H15	CN_P21_2 *
16	H16	P22_4
17	H17	P22_6
18	H18	P22_7
19	H19	CN_P25_6 *
20	H20	RAMSVCL
21	H21	P22_13
22	H22	RESETOUT#
23	H23	PWRCTL
24	H24	ERROROUT_M#
25	H25	VMONOUT#
26	H26	P20_3
27	H27	P20_1
28	H28	P20_4
29	H29	P14_0
30	H30	P14_3
31	H31	P14_6
32	H32	P14_9
33	H33	CN_P13_2 *
34	H34	CN_P14_4 *
35	H35	P12_0
36	H36	P12_3
37	H37	P12_6
38	H38	P13_8
39	H39	P13_13

Table 7.6 Device ports connector CN6 (cont'd)

Pin	PCB Silk	Device port
40	H40	P11_5

Note * By default these signals are connected to CN6. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R150, R160, R189, R191.

7.3.3 Device Ports Connector CN13

Table 7.7 Device ports connector CN13

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
1	F1	P24_9	2	E1	P24_8
3	F2	P24_10	4	E2	P24_11
5	F3	–	6	E3	P30_1
7	F4	P30_0	8	E4	P33_2
9	F5	P33_1	10	E5	AN12_3
11	F6	AN11_2	12	E6	AN12_1
13	F7	P33_0	14	E7	AN11_3
15	F8	AN12_0	16	E8	AN11_1
17	F9	AN11_0	18	E9	AN12_2
19	F10	AN10_3	20	E10	AN10_2
21	F11	AN10_1	22	E11	AN10_0
23	F12	AN05_3	24	E12	AN05_1
25	F13	P23_8	26	E13	P23_10
27	F14	P23_9	28	E14	P23_11

7.3.4 Device Ports Connector CN14

Table 7.8 Device ports connector CN14

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
1	K1	P33_3	2	J1	P33_4
3	K2	P30_3	4	J2	P33_5
5	K3	P30_4	6	J3	P34_1
7	K4	P33_8	8	J4	P34_0
9	K5	P33_9	10	J5	P33_10
11	K6	P34_4	12	J6	P33_11
13	K7	P32_0	14	J7	P33_12

Table 7.8 Device ports connector CN14 (cont'd)

Pin	PCB Silk	Device port
15	K8	P32_3
17	K9	P23_1
19	K10	P23_5
21	K11	P23_7
23	K12	GETH0VCL
25	K13	X1_C
27	K14	CN_P22_3 *1
29	K15	P22_1
31	K16	CN_P21_5 *1
33	K17	CN_P21_4 *1
35	K18	CN_P25_3 *1
37	K19	P22_8
39	K20	P22_9
41	K21	P22_11
43	K22	TRST#
45	K23	SBMD
47	K24	JP0_2
49	K25	CN_JP0_1 *2
51	K26	CN_JP0_5 *2
53	K27	P20_5
55	K28	P14_1
57	K29	P20_7
59	K30	P14_7
61	K31	CN_P13_0 *1
63	K32	P14_12
65	K33	P14_11
67	K34	P12_1
69	K35	P12_8
71	K36	P12_9
73	K37	P13_10

Pin	PCB Silk	Device port
16	J8	P33_13
18	J9	P32_5
20	J10	P32_6
22	J11	P23_3
24	J12	GETH1VCL
26	J13	X2_C
28	J14	P25_2
30	J15	CN_P21_3 *1
32	J16	P22_2
34	J17	P22_5
36	J18	CN_P25_4 *1
38	J19	CN_P25_5 *1
40	J20	P22_10
42	J21	P22_12
44	J22	FLMD0
46	J23	RESET#
48	J24	CN_JP0_0 *2
50	J25	CN_JP0_3 *2
52	J26	P20_2
54	J27	P20_6
56	J28	P20_0
58	J29	P14_8
60	J30	P14_2
62	J31	CN_P13_1 *1
64	J32	P14_10
66	J33	CN_P13_3 *1
68	J34	CN_P14_5 *1
70	J35	CN_P12_5 *1
72	J36	P12_2
74	J37	P12_7

Table 7.8 Device ports connector CN14 (cont'd)

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
75	K38	P13_11	76	J38	P13_9
77	K39	P13_14	78	J39	P13_12
79	K40	P10_11	80	J40	P11_3

Note *1 By default these signals are connected to CN14. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R148, R149, R151, R156, R159, R161, R163, R190, R192, R193, R199.

*2 By default these signals are not connected to CN14 to minimize signal interference. If required, they can be connected via 0 Ω resistors R185-R188.

7.3.5 Device Ports Connector CN15

Table 7.9 Device ports connector CN15

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
1	B1	AN06_3	2	A1	AN06_1
3	B2	AN06_0	4	A2	AN05_2
5	B3	AN03_3	6	A3	AN04_2
7	B4	AN04_0	8	A4	AN03_0
9	B5	AN02_3	10	A5	AN04_3
11	B6	AN02_2	12	A6	AN03_1
13	B7	AN01_0	14	A7	AN01_3
15	B8	AN01_1	16	A8	AN01_2
17	B9	AN00_0	18	A9	AN00_2
19	B10	LP_AN20_2	20	A10	LP_AN20_1
21	B11	LP_AN21_3	22	A11	LP_AN23_1
23	B12	AN22_3	24	A12	AN23_3
25	B13	AN21_0	26	A13	AN22_0
27	B14	AN21_1	28	A14	AN24_0
29	B15	AN21_2	30	A15	AN24_3
31	B16	AN25_1	32	A16	AN25_3
33	B17	AN25_2	34	A17	AN26_0
35	B18	AN27_0	36	A18	AN26_1
37	B19	AN27_1	38	A19	AN27_2
39	B20	AN30_0	40	A20	AN27_3
41	B21	AN30_2	42	A21	AN30_1

Table 7.9 Device ports connector CN15 (cont'd)

Pin	PCB Silk	Device port	Pin	PCB Silk	Device port
43	B22	AN31_2	44	A22	AN30_3
45	B23	P02_10	46	A23	P00_11
47	B24	P02_9	48	A24	P02_8
49	B25	P00_4	50	A25	P02_7
51	B26	P00_9	52	A26	P00_3
53	B27	P02_4	54	A27	P00_8
55	B28	P02_3	56	A28	P02_2
57	B29	P00_1	58	A29	P02_1
59	B30	P00_0	60	A30	P01_5
61	B31	P00_6	62	A31	P01_7
63	B32	P01_3	64	A32	P01_8
65	B33	P10_9	66	A33	P10_6
67	B34	P10_14	68	A34	CN_P10_4 *
69	B35	P10_12	70	A35	CN_P10_5 *
71	B36	CN_P10_3 *	72	A36	CN_P12_4 *
73	B37	CN_P10_0 *	74	A37	CN_P10_1 *
75	B38	CN_P11_10 *	76	A38	P11_7
77	B39	P11_4	78	A39	P11_6
79	B40	CN_P11_2 *	80	A40	P11_1

Note * By default these signals are connected to CN15. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R140, R141, R147, R153-R155, R198.

7.4 Ethernet Connector CN17, CN18, CN19 and CN22

The connectors are delivered only with pcb of board version D018705_06_V01. They must not be used.

The connectors are not included with pcb of board version D018705_06_V02.

7.5 RHSB1/MSPI6 Connector CN23

Table 7.10 RHSB1/MSPI6 connector CN23

Pin	SW3-2 = ON (RHSB1/MSPI6_MUX)		SW3-2 = OFF (RHSB1/MSPI6_MUX)	
	Device port	Function	Device port	Function
1	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)	–	–
3	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)	–	–
7	–	–	P10_0	CLK_P, DATA_IN_P (RHSB1MCSIP / RHSB1FCLP / MSPI6_SCKP)
9	–	–	P10_1	CLK_N, DATA_IN_N (RHSB1MCSIN / RHSB1FCLN / MSPI6_SCKN)

Pin	Device port	Function
5	-	-
6	JP3[1-2]: P10_7 JP3[2-3] and JP6[1-2]: P11_2 JP3[2-3] and JP6[2-3]: P12_4	RHSB1CSD0 MSPI6CSS0 MSPI6SSI
11	–	GND
12	–	GND

Pin	SW3-3 = ON (RHSB1/MSPI6_MUX_2)		SW3-3 = OFF (RHSB1/MSPI6_MUX_2)	
	Device port	Function	Device port	Function
2	P10_4	DATA_IN_P (MSPI6_SIP)	P10_2	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)
4	P10_5	DATA_IN_N (MSPI6_SIN)	P10_3	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)
8	P10_4	DATA_OUT_P (RHSB1MCSOP / RHSB1SOP / MSPI6_SOP)	P10_2	DATA_IN_P (MSPI6_SIP)
10	P10_5	DATA_OUT_N (RHSB1MCSON / RHSB1SON / MSPI6_SON)	P10_3	DATA_IN_N (MSPI6_SIN)

Note

The signals on the RHSB1/MSPI6 interface are connected to connectors CN1–CN3, CN5 and CN15. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R140, R141, R146, R147, R152-R155, R198.

7.6 RHSB0 Connector CN24

Table 7.11 RHSB0 connector CN24

Pin	SW3_1 = ON (RHSB0_MUX)		SW3_1 = OFF (RHSB0_MUX)	
	Device port	Function	Device port	Function
1	P25_4	CLK_P/DATA_IN_P	–	–
2	–	–	P25_4	CLK_P/DATA_IN_P
3	P25_3	CLK_P/DATA_IN_N	–	–
4	–	–	P25_3	CLK_P/DATA_IN_N
5	–	–		–
6	P22_5	CS_OUT	P22_5	CS_OUT
7	–	–	P25_5	DATA_OUT_P
8	P25_6	DATA_OUT_P	–	–
9	–	–	P25_5	DATA_OUT_N
10	P25_5	DATA_OUT_N	–	–
11	–	GND		GND
12	–	GND		GND

Note

The signals on the RHSB0 interface are connected to connectors CN3 and CN14. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R148-R151, R203.

7.7 MSPI9 Connector CN26

Table 7.12 MISP9 connector CN26

Pin	Device port	Function
1	P13_1	CLK_P
2	P14_4	DATA_IN_P
3	P13_0	CLK_N
4	P14_5	DATA_IN_N
5	–	–
6	P12_5 (JP50[1-2] = ON) P11_10 (JP50[2-3] = ON)	CS_OUT
7	–	–
8	P13_3	TXDP
9	–	–
10	P13_2	TXDN
11	–	GND
12	–	GND

Note

The signals on the RHSIF0 interface are connected to connectors CN1 - CN3, CN6, CN14 and CN15. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R156-R161, R163, R189.

7.8 RHSIF0 Connector CN27

Table 7.13 RHSIF0 connector CN27

Pin	JP4 connected		JP4 open	
	Device port	Function	Device port	Function
1	P21_3	RXDP	P21_5	TXDP
2	–	GND	–	GND
3	P21_2	RXDN	P21_4	TXDN
4	–	GND	–	GND
5	–	–	–	–
6	P22_3	REFCLK	P22_3	REFCLK
7	P21_5	TXDP	P21_3	RXDP
8	–	GND	–	GND
9	P21_4	TXDN	P21_2	RXDN
10	–	GND	–	GND
11	–	GND	–	GND
12	–	GND	–	GND

Note

The signals on the RHSIF0 interface are connected to connectors CN1, CN3, CN6 and CN14. To minimize signal interference, they can be disconnected by removing 0 Ω resistors R190-R193, R199.

7.9 Pull-Up/Pull-Down Pin Header CN29

Table 7.14 Pull-up/pull down connector CN29

Pin	Function
1	fixed L level
3	
5	
7	
9	
11	
13	
15	

Pin	Function
2	fixed H level, 3.3V
4	
6	
8	
10	fixed H level, 5.0V
12	
14	
16	

8. Jumper Configuration Examples

Several functions of the board can be configured via jumpers.
The board is shipped without any jumpers set.

For a complete list of jumpers refer to *2.1 Jumper Overview*.

For jumper settings related to the device operation mode, refer to *6.1 Operation Mode Selection*.

The following sections show some jumper settings, which allow to use the piggyback board in different power supply configurations.

8.1 Stand-Alone Operation with Power Supply by Debugger

Basically, the piggyback board can solely be powered by a connected debugger. Please make sure the debug tool can provide sufficient current on the power supply rails in order to operate the board in a useful manner.

Due to the limited current capability of Renesas' E2 Emulator, powering the board only via this debugger is not feasible.

In case of using another debug tool check its specification whether powering the piggyback board with the tool is possible.

8.2 Operation using FCC Device or Mass Production Device

It is possible to use a device with more debug functions called FCC device or a mass production device with the piggyback board. There are some differences between FCC devices and mass production (MP) devices.

Jumper JP1

- When using an MP device do open jumper JP1.
- When using the FCC device the AURORES# signal has to be provided to the device. On the CN4 debug connector there are 2 signals that can be used for this signal.
  - If the AURORES# signal on CN4 is to be used for the FCC device put a jumper to JP1[2-3].
  - If the TRST# signal on CN4 is to be used for the FCC device put a jumper to JP1[1-2].

Switch SW4

- When using an MP device, or an FCC device with a debug tool that does not support Aurora interface, the signals EVTO0 and MSYN# are not needed on the processor. The switches SW4-1, SW4-2 and SW4-3 must be set OFF.
- When using an FCC device with a debug tool supporting Aurora interface the signals EVTO0 and MSYN# on connector CN4 must be connected to the device. SW4-1 must be set to ON to select the MSYN# signal.
  For EVTO0 control set
  - SW4-2 to ON to select the device EVTO# signal or
  - SW4-3 to ON to select P32_0.

Power supply for debug interface

Some power supply jumpers must only be connected when the device is an FCC device. They are not needed when an MP device is used.

- JP10[37-38]: This jumper must be set to supply 3.3V to EMUVCC
- JP10[46-47-48]: This jumper must be set to provide supply voltage to JVCC. The voltage level must be the same as for VCC.
  - JP10[46-47]: use 3.3V as JVCC
  - JP10[47-48]: use 5.0V as JVCC
- JP31 has a jumper to enable EMUVDD supply for an FCC device. This is not needed when an MP device is used.
  - JP31[10-11]: use onboard VDD as EMUVDD

Table 8.1 Power supply jumper settings for FCC devices and MP devices

Purpose	Jumper	RH850/U2B10 RH850/U2B20 RH850/U2B24	RH850/U2B10-FCC RH850/U2B20-FCC RH850/U2B24-FCC
AURORES# Config	JP1	---	O
PWRCTL Config	JP2	U2B10: --- U2B20, U2B24: O	U2B10-FCC: --- U2B20-FCC, U2B24-FCC: O
Port Select for CS_OUT on CN23	JP3	O	O
TX and RX Signal swap on RHSIF0 Interface	JP4	O	O
TRST# Signal Source Select	JP5	O	O
FLMD0 Config	JP46	---	---
SBMD Config	JP47	--- (U2B10) / O (U2B20, U2B24) Please refer to *Table 6.1 Device operation mode selection jumpers*	--- (U2B10-FCC) / O (U2B20-FCC, U2B24-FCC) Please refer to *Table 6.1 Device operation mode selection jumpers*
FLMD1 Config	JP48	---	---
LED Output Config	JP7	O	O
A1VREFH Config	JP10[1-2-3]	O	O
A1VCC Config	JP10[4-5-6]	O	O
A0VREFH Config	JP10[7-8-9]	O	O
A0VCC Config	JP10[10-11-12]	O	O
ADSVCC Config	JP10[13-14-15]	O	O
A2VCC Config	JP10[16-17-18]	O	O
A2VREFH Config	JP10[19-20-21]	O	O
AFCVCC Config	JP10[22-23-24]	O	O
A3VCC Config	JP10[25-26-27]	O	O
A3VREFH Config	JP10[28-29-30]	O	O
E1VCC Config	JP10[31-32-33]	O	O
E0VCC Config	JP10[34-35-36]	O	O
EMUVCC Config	JP10[37-38-39]	---	JP10[37-38]
E2VCC Config	JP10[40-41-42]	O	O
SVRDRVCC Config	JP10[43-44-45]	O	O
JVCC Config	JP10[46-47-48]	O, same as VCC Config	O

Table 8.1 Power supply jumper settings for FCC devices and MP devices (cont'd)

Purpose	Jumper	RH850/U2B10 RH850/U2B20 RH850/U2B24	RH850/U2B10-FCC RH850/U2B20-FCC RH850/U2B24-FCC
SYSVCC Config	JP10[49-50-51]	O	O
VCC Config	JP10[52-53-54]	O	O
GETH0BVCC Config	JP10[55-56-57]	U2B10: open, U2B20, U2B24: JP10[55-56]	U2B10-FCC: open, U2B20-FCC, U2B24-FCC: JP10[55-56]
GETH0PVCC Config	JP10[58-59-60]	U2B10: NC (JP10[59-60] or open) U2B20, U2B24: JP10[58-59]	U2B10-FCC: NC (JP10[59-60] or open) U2B20-FCC, U2B24-FCC: JP10[58-59]
VDDIOF Config	JP10[61-62-63]	O	O
ADVSREFH Config	JP10[64-65-66]	O	O
+5.0V power supply from main board	JP12	O	O
int_P3V3 Config	JP20	O	O
+3.3V power supply from main board	JP30	O	O
Ext_VDD Config	JP31[1-2-3]	O	O
VDD Config	JP31[4-5-6]	O	O
VDD Config	JP31[7-8-9]	O	O
EMUVDD Config	JP31[10-11-12]	---	JP31[10-11]
Ethernet enable switch	SW2	U2B10: OFF U2B20, U2B24: O	U2B10-FCC: OFF U2B20-FCC, U2B24-FCC: O
Debug port connection EVTO0 / MSYN#	SW4	OFF	O

--- : Jumper open

O : possible setting

The lines marked in yellow are for use with FCC devices only.

8.3 Configuration Examples

8.3.1 General Settings

All the following board configurations are based on these conditions:

- Normal device operation mode (JP46[OPEN]: FLMD0 = L).
  - When using Serial Programming Mode by a debugger or programming tool, that is connected to the board, make sure to open jumper JP48 (JP48[OPEN]: FLMD1 = GND).
- All voltages for all functions are activated.
- Clock supply: assuming one of the resonators, coming with the board, are plugged into X1 socket.
- For connection to external power supplies the 'banana-type' connectors CN8 (GND), CN9 (+5.0 V) and CN21 (*3.3 V) are assembled on the board.
- If also the core supply voltage of 1.12 V will be supplied from an external power supply the connector CN11 (included in the package) has to be assembled on the pcb.

8.3.2 Jumper Indicators

The green jumper JP46 for FLMD0 must always be open for ‘normal’ (user mode and debug) operation of the device.

The red jumpers are related to the power supply configuration.
Following jumper symbols are used:

-  : Jumper must not be set.
-  : Jumper must be set in the indicated position, in this case position [2-3]
-  : Jumper can be set to position [1-2] or position [2-3]
-  : Jumper with optional setting. The red setting [2-3] is the default setting. The blue setting [1-2] is the optional setting.

Note

The pin 1 of a jumper can be identified by

- a small circle near the jumper
- a square soldering pad.

8.3.3 Stand-Alone Operation with Single External Power Supply 3.3V: Minimum Configuration 1

This example enables to operate the board with only the 3.3 V external power supply. VDD is provided from SVR controller.
Since no 5 V voltage is available, all I/O ports can only use 3.3 V.

Table 8.2 Power supply connectors for single power supply 3.3V

Connector	Name	Ext. Power Supply	Remarks
CN11	1.12 V	Not connected	VDD from SVR_OUTPUT (JP31[6-5]) from on-chip Switching Voltage Regulator. SVR must be switched on and configured in the option bytes by a flash programming tool (e.g. RFP) beforehand. Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Connected, +3.3 V	
CN33	GND	Connected, GND	
CN34	5.0 V	Not connected	Jumpers in JP10 (VCC and VREF selection) are set to 3.3 V position JP10[1-2]

Note

・AWOVCL: Regarding AWOVCL setting (JP31[7-8-9]) please refer to *Table 6.1 Device operation mode selection jumpers*
・PWRCTL: for U2B10: JP2[open]

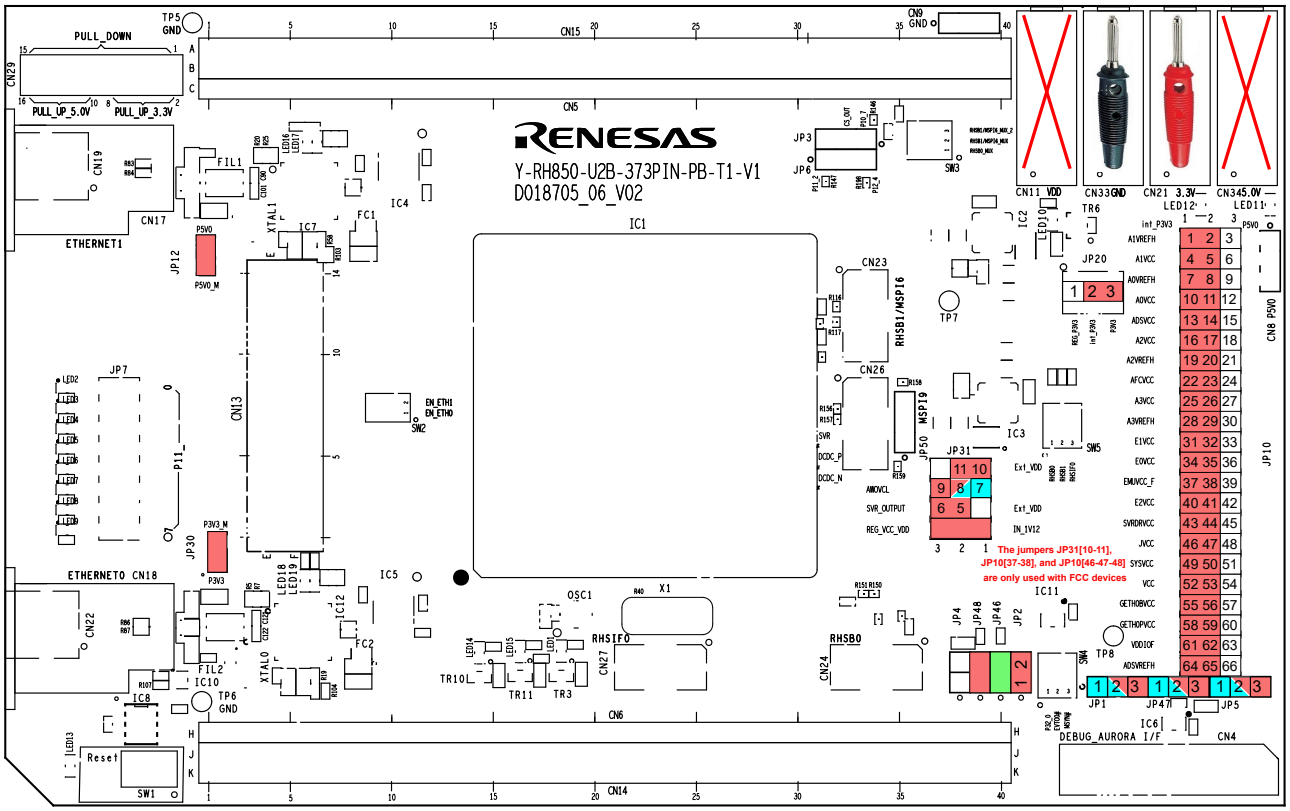


Figure 8.1 Stand-alone operation with single external power supply 3.3V

8.3.4 Stand-Alone Operation with Single External Power Supply 5.0V: Minimum Configuration 2

This example enables us to use the board with only the 5.0 V external power supply. VDD is generated using the voltage generator on the piggyback board. All I/O ports can only use 5.0 V.

Table 8.3 Power supply connectors for single power supply 5.0V

Connector	Name	Ext. Power Supply	Remarks
CN11	1.12 V	Not connected	VDD from onboard voltage regulator (JP31[5-4]) and JP31[2-3] Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Not connected	Jumpers in JP10 (VCC and VREF selection) are set to 5.0 V position. 3.3V from onboard voltage regulator (JP20[1-2]) EMUVCC can only be connected to 3.3V (JP10[37-38]).
CN33	GND	Connected, GND	
CN34	5.0 V	Connected, 5.0 V	

Note

- GETH0BVCC: U2B10: open, U2B20 and U2B24: JP10[55-56]
- GETH0PVCC: U2B10: NC(JP10[59-60] or open), U2B20 and U2B24: JP10[58-59]
- PWRCTL: for U2B10: JP2[open]
- SMBD input selection (JP47): Please refer to *Table 6.1 Device operation mode selection jumpers*

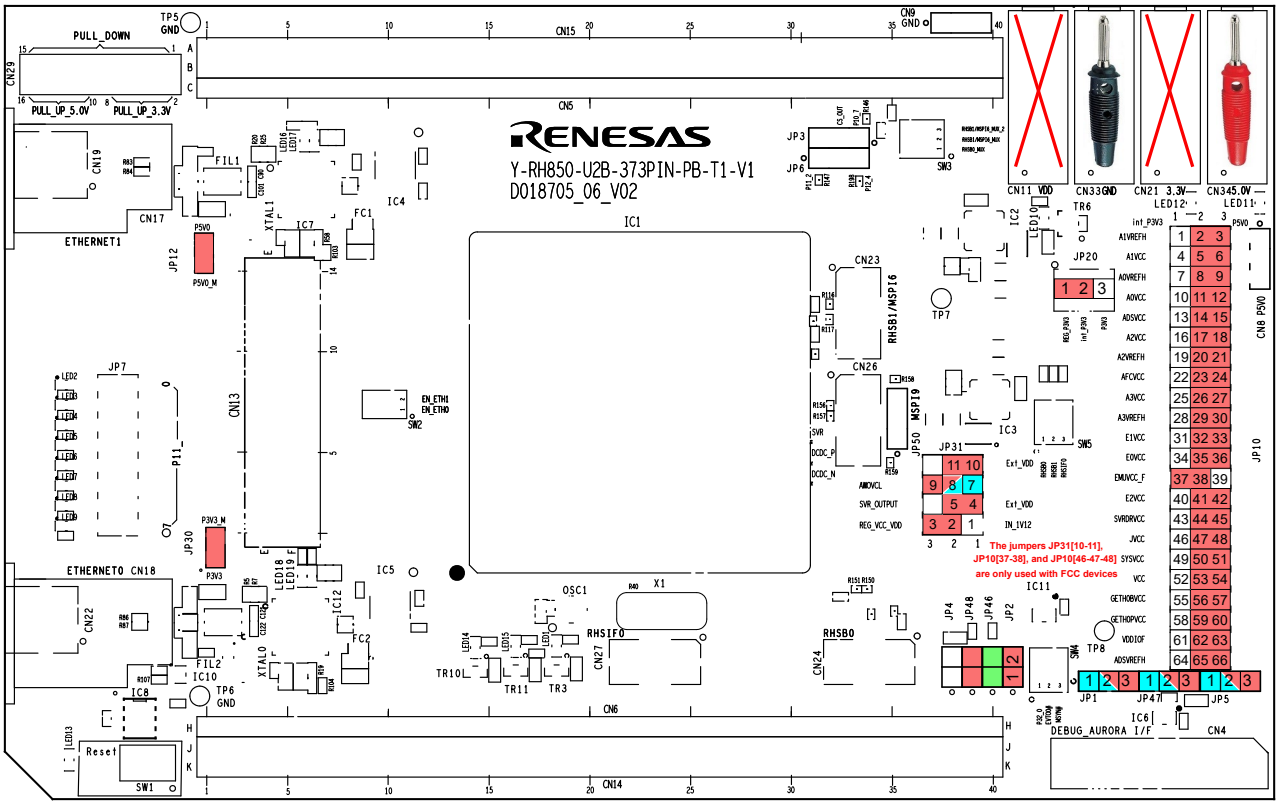


Figure 8.2 Stand-alone operation with single external power supply 5.0V

8.3.5 Stand-Alone Operation with All External Power Supplies: Maximum Configuration

This example assumes all external power supplies are connected and used.

Table 8.4 Power supply connectors to use all external power supplies

Connector	Name	Ext. Power Supply	Remarks
CN11	1.12 V	Connected, 1.12 V	JP31[1-2] and JP31[4-5]: use IN_1v12 for VDD voltage. Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Connected, 3.3 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP10. JP20[2-3]: use p3V3 supply for 3.3 V. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP10.
CN33	GND	Connected, GND	
CN34	5.0 V	Connected, 5.0 V	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP10. Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP10.

Note

- CN11 : solder connector for CN11 to the piggyback board
- GETH0BVCC : U2B10: open, U2B20 and U2B24: JP10[55-56]
- GETH0PVCC : U2B10: NC(JP10[59-60] or open), U2B20 and U2B24: JP10[58-59]
- PWRCTL: for U2B10: JP2[open]

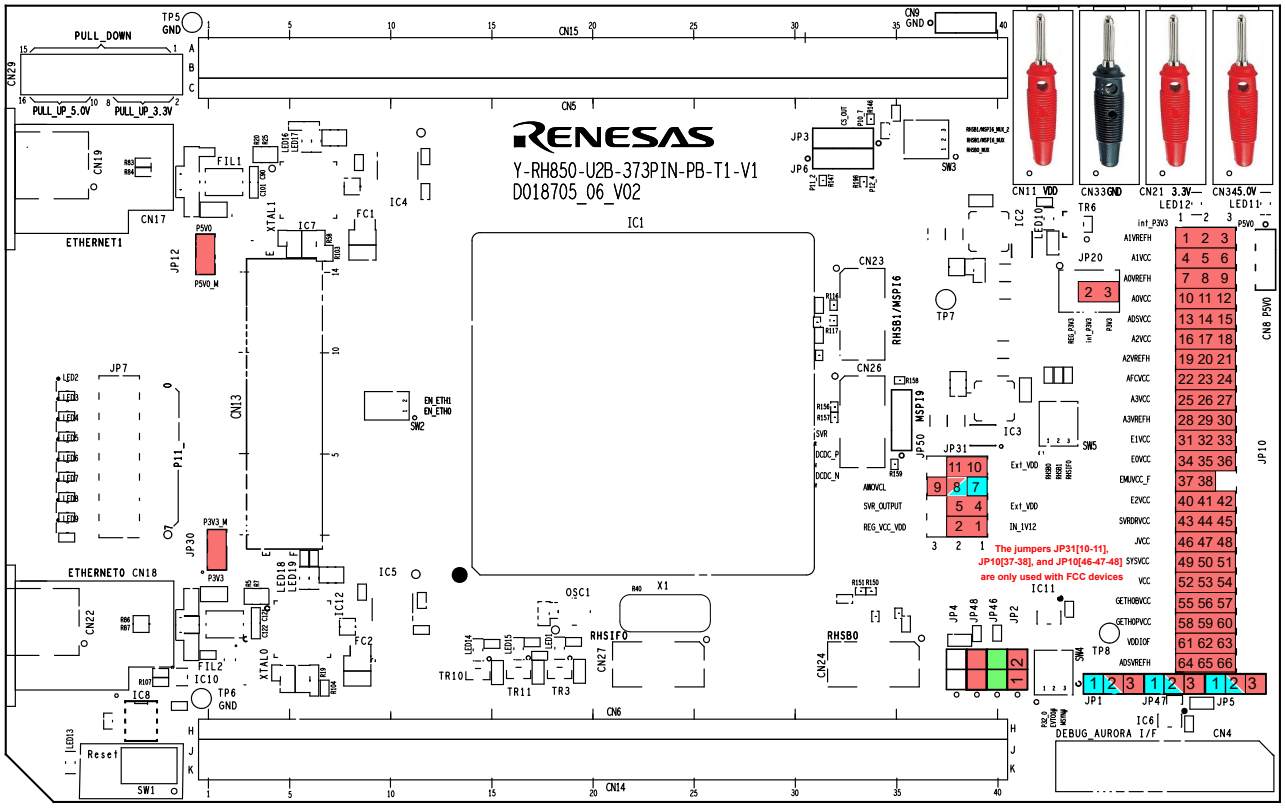


Figure 8.3 Stand-alone operation with all external power supplies

8.3.6 Operation on the Main Board: No External Supply

This example assumes the piggyback board is plugged onto a Main Board, which supplies 3.3 V and 5.0 V.

Do not supply the 5V (CN34) and 3.3V (CN21) voltage directly to the piggyback board

Table 8.5 Power supply connectors to use power supply from main board

Connector	Name	Ext. Power Supply	Remarks
CN11	1.12 V	Not connected	VDD supply: – JP31[2-3] and JP31[4-5]: use reg_vcc_VDD from onboard voltage regulator for supply of VDD voltage – JP31[6-5]: use SVR_OUTPUT from on-chip Switching Voltage Regulator Refer to *3.3 Device Core Voltage (VDD) Selection* for further details about VDD voltage.
CN21	3.3 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP10 3.3V from main board (JP20[2-3]) or from onboard voltage regulator (JP20[1-2]) Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP10.
CN33	GND	Not connected	
CN34	5.0 V	Not connected	Select desired 3.3 V / 5.0 V for VCC and VREF supply voltages via jumpers in JP10 Refer to *3.2 Voltage Distribution* for details on possible settings of jumpers in JP10.
JP12	P5V0_M		Use jumper JP12[1-2] to connect the 5.0 V supply from the main board to the piggyback board
JP30	P3V3_M		Use jumper JP30[1-2] to connect the 3.3 V supply from the main board to the piggyback board

Note

This configuration still allows the use an external IN_1v12 voltage (connected to CN11) as the source for VDD voltage. In this case set JP31[1-2] and JP31[4-5].

・GETH0BVCC：U2B10: open, U2B20 and U2B24: JP10[55-56]

・GETH0PVCC：U2B10: NC(JP10[59-60] or open), U2B20 and U2B24: JP10[58-59]

・PWRCTL: for U2B10: JP2[open]

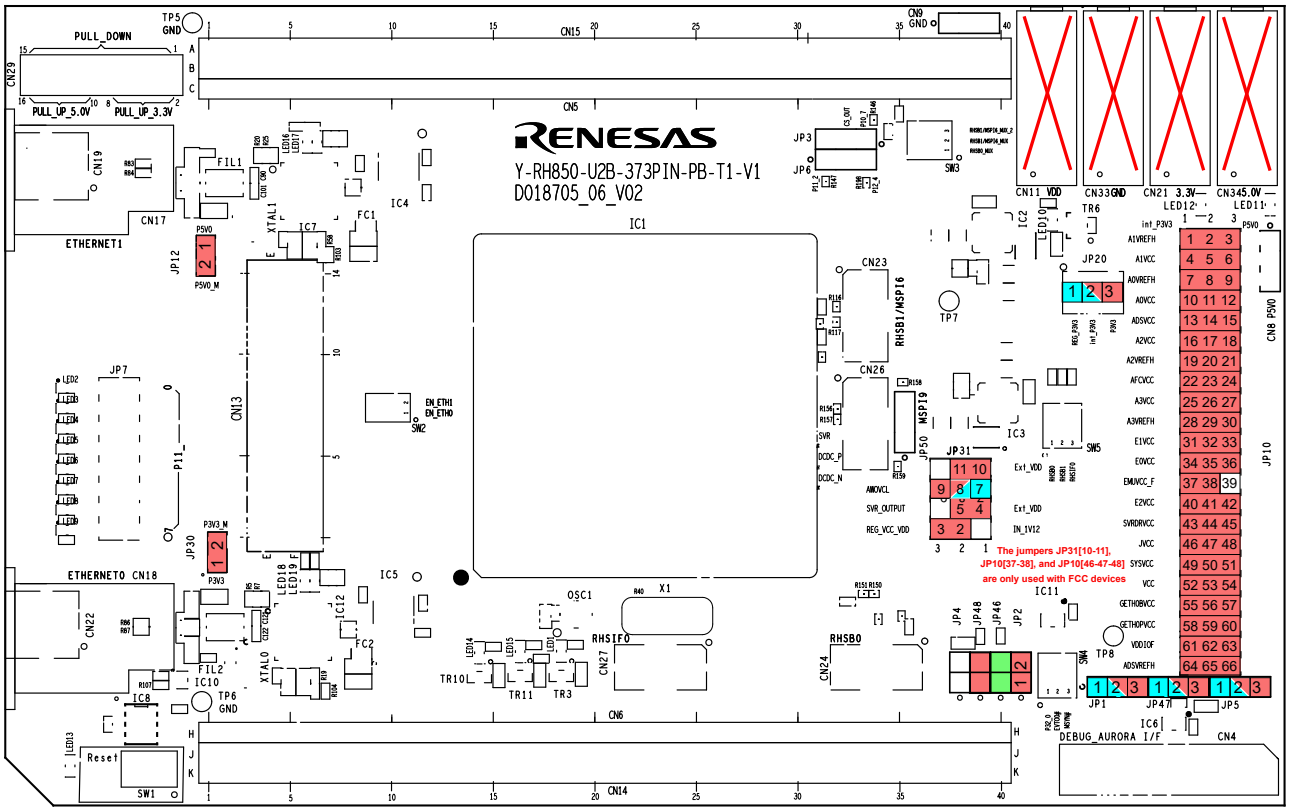


Figure 8.4 Main board operation without external power supply

CAUTION

Do not supply 5V (CN34) and 3.3V (CN21) directly to the piggyback board if these voltages are already supplied by the main board.

9. Precautions

9.1 Power-Off Sequence

A dedicated sequence needs to be applied when the power supply to the board is turned off.

Please follow the below sequence:

1. At first turn the RESET switch SW1 into '5-6 ON' position, so that RESET is permanently asserted.
   Alternatively keep SW1 manually in' 5-4 (ON)' position.
2. Turn off the board power supply.
3. After the power supply has shut down, release RESET by returning SW1 into the 'OFF' position.

For details how to apply a RESET, please refer to section *6.2 RESET Switch*.

9.2 Power On Piggyback Board Without RH850 Microcontroller installed

The piggyback board Y-RH850-U2B-373PIN-PB-T1-V1 is not designed to be powered on when the RH850 microcontroller is not installed in socket IC1.

If the microcontroller is not installed the SVR power supply circuit does not have the control signals SVRNGATE and SVRPGATE and may be damaged.

If for some reason the board has to be powered on without a microcontroller mounted in socket IC1 please make sure the jumper CN10[43-44-45] (SVRDRVCC) is open. In this case no power is supplied to the SVR control circuit, and it will not be damaged.

If the piggyback board is being used with the microcontroller installed please make sure the ports SVRNGATE and SVRPGATE are set to “Fixed” (output) in bit SVRENDCDCHZ in option byte 25.

10. Mechanical Dimensions

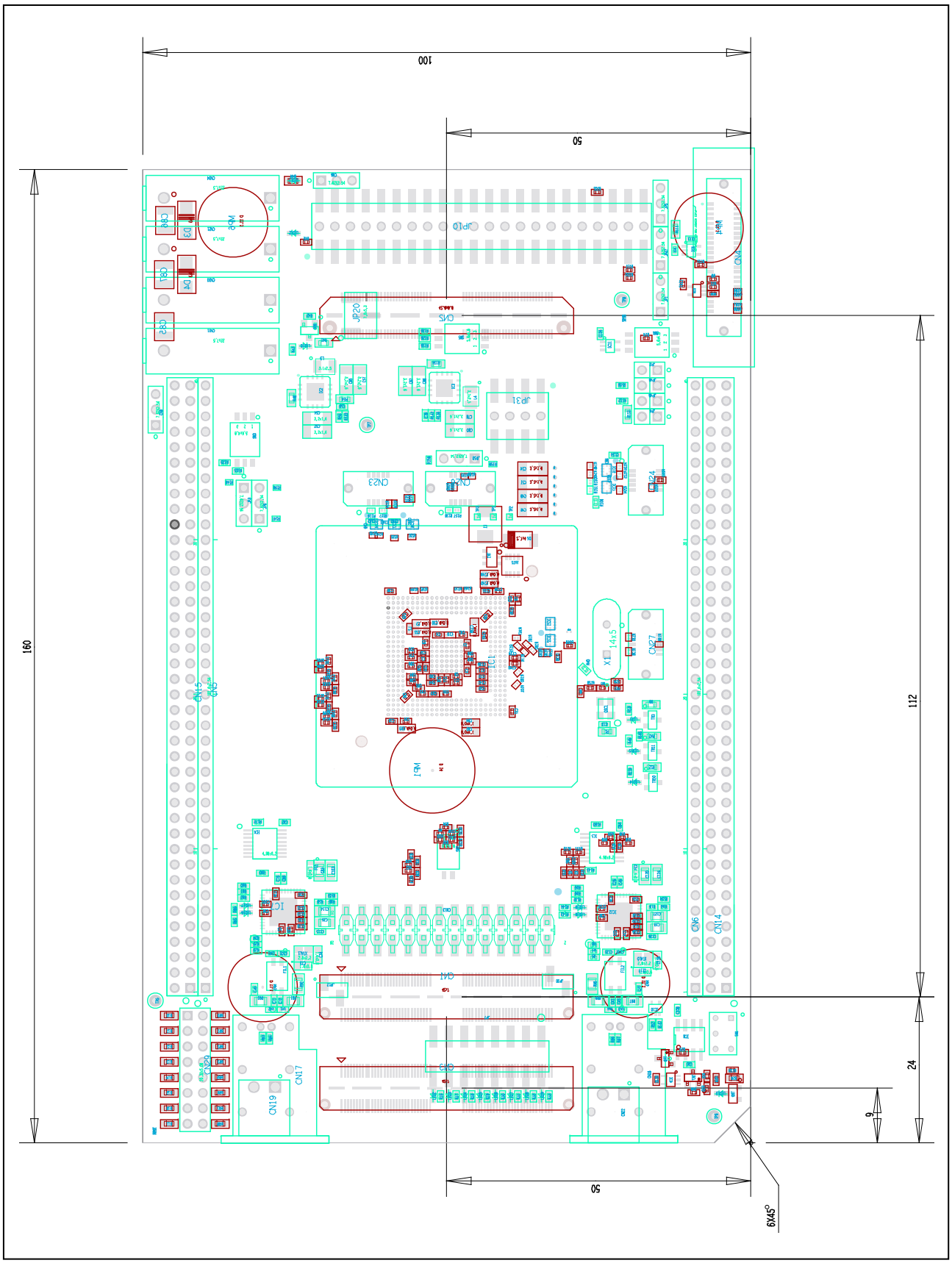


Figure 9.1 Mechanical dimensions

11. Schematics

CAUTION

The schematics shown in this document are not intended to be used as a reference for mass production. Any usage in an application design is the sole responsibility of the customer.

11.1 Board Version D018705_06_V01

The following components described in the schematics are not provided with the board upon delivery:

- Capacitors: C90, C97, C98, C101, C121, C122
- Resistors: R5, R7, R19, R20, R22, R23, R25, R34-R39, R57, R58, R64, R69, R78, R79, R83, R84, R86, R87, R100, R101, R103, R104, R107, R114, R115, R121-R123, R185-R188,

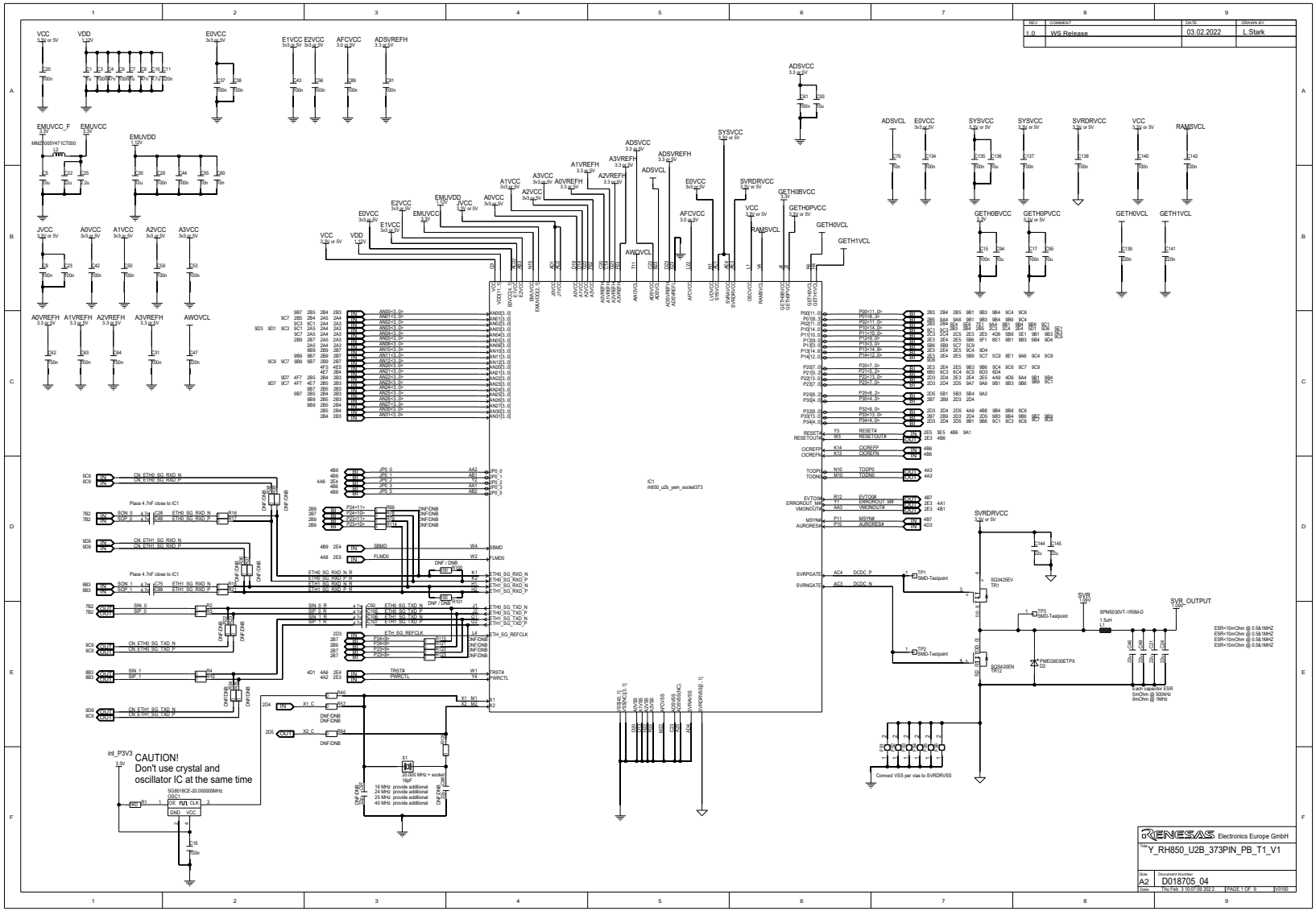
The above components are marked with "DNF/DNB" in the schematics.

The following components described in the schematics are provided with but not mounted on the board upon delivery:

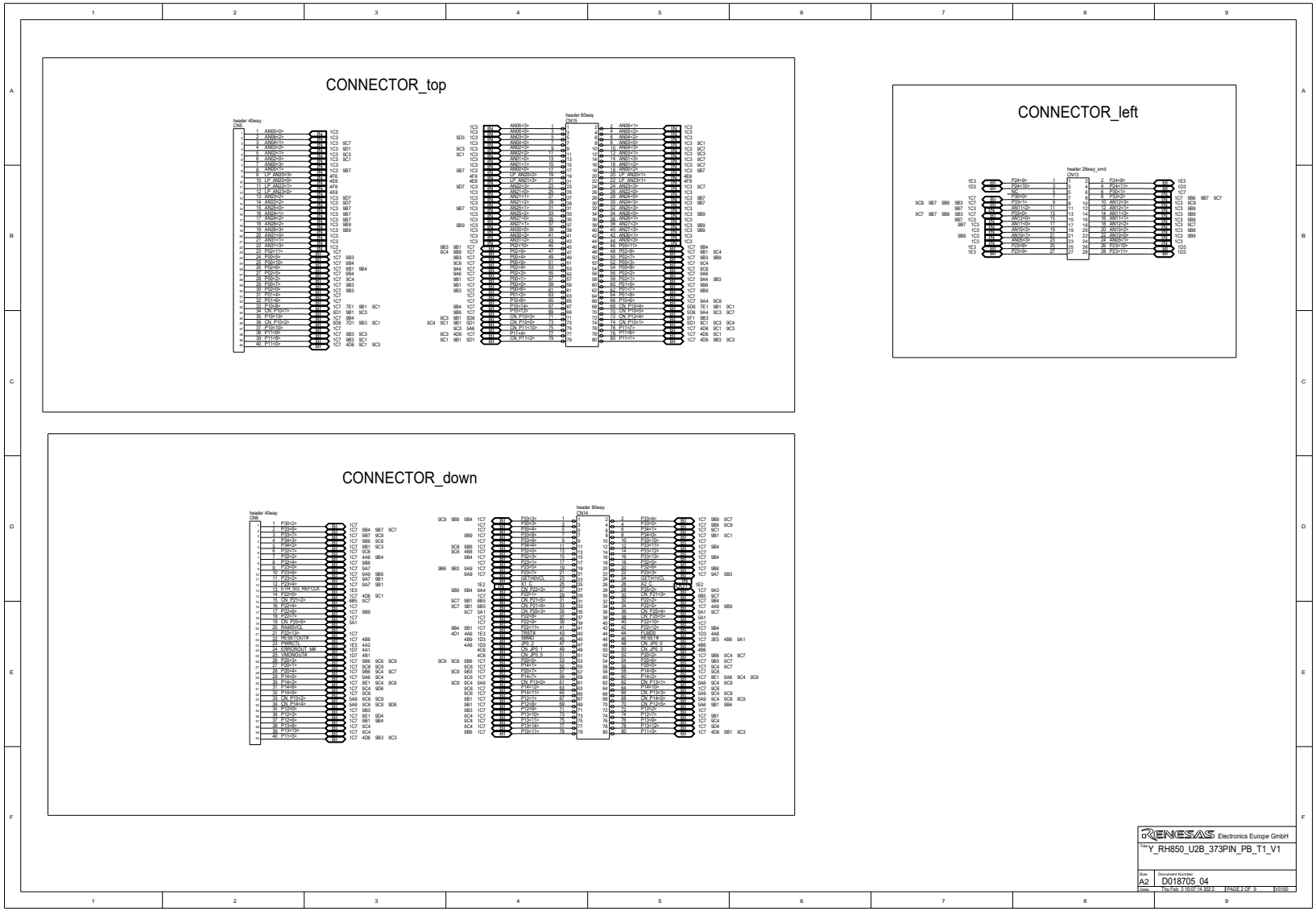
- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Four resonators HC49 (16/24/25/40 MHz)
- 47 jumpers, 2.54 mm, black
- Würth PCB Terminal Block connector (CN19, CN22)
- TE MATEnet 1000BASE-T1 Ethernet Port connector (CN17, CN18)
- Resistors 100 Ohm: R124, R162, R164, R167, R169, R170, R174, R175, R201, R204, R205

The above components are marked with "DNF / TD" in the schematics.

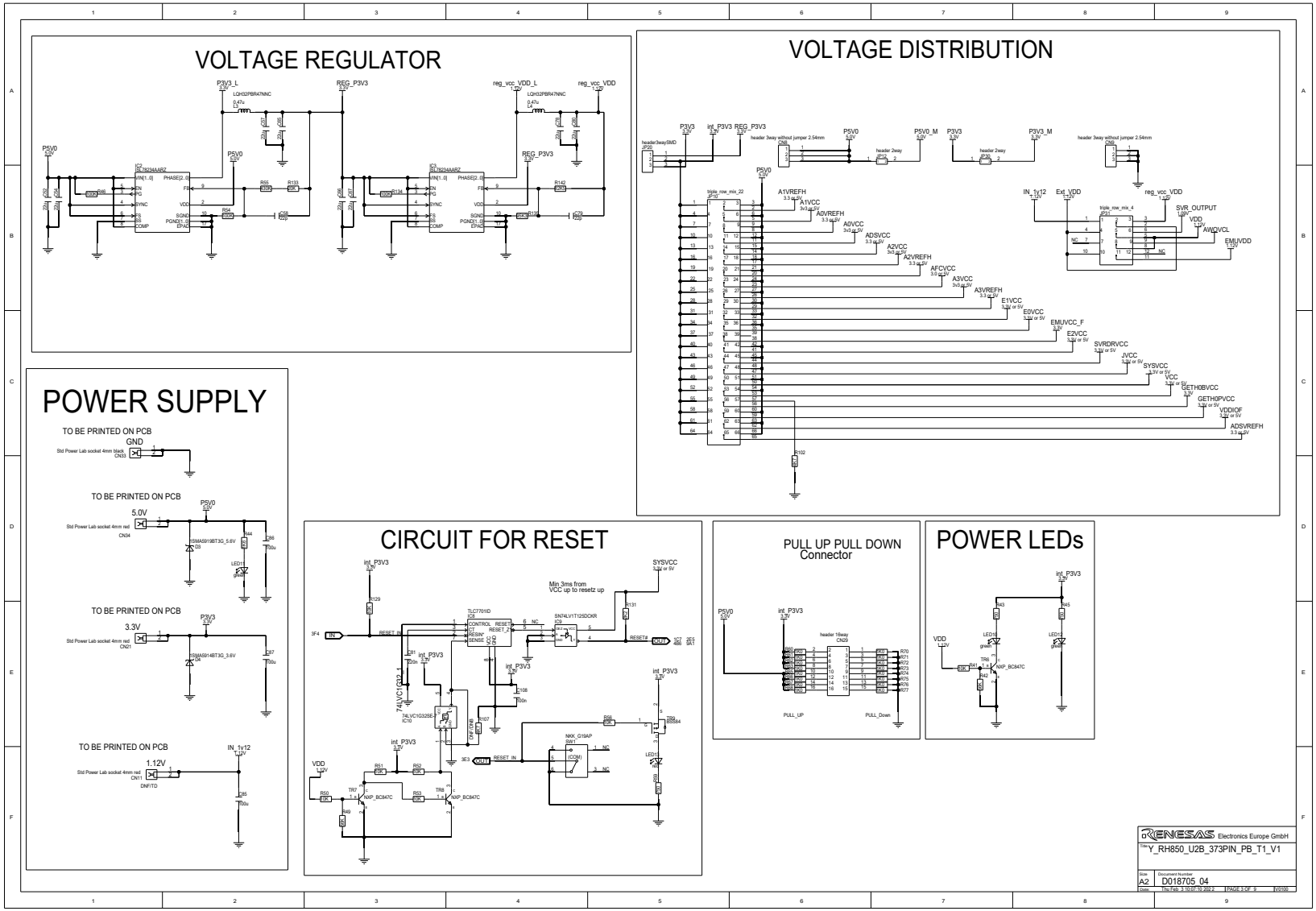
11.1.1 Page 1


REV | COMMENT | DATE | DRAWN BY
1.0 | WS Release | 03.02.2022 | L.Stark
RENESAS Electronics Europe GmbH
Title: Y_RH850_U2B_373PIN_PB_T1_V1
Size: A2 | Document Number: D018705_04
Date: Thu Feb 3 10:07:59 2022 | PAGE 1 OF 9 | V0100
CAUTION!
Don't use crystal and
oscillator IC at the same time
IC1
rh850_u2b_yam_socket373
SVR_OUTPUT
Connect VSS per vias to SVRDRVSS

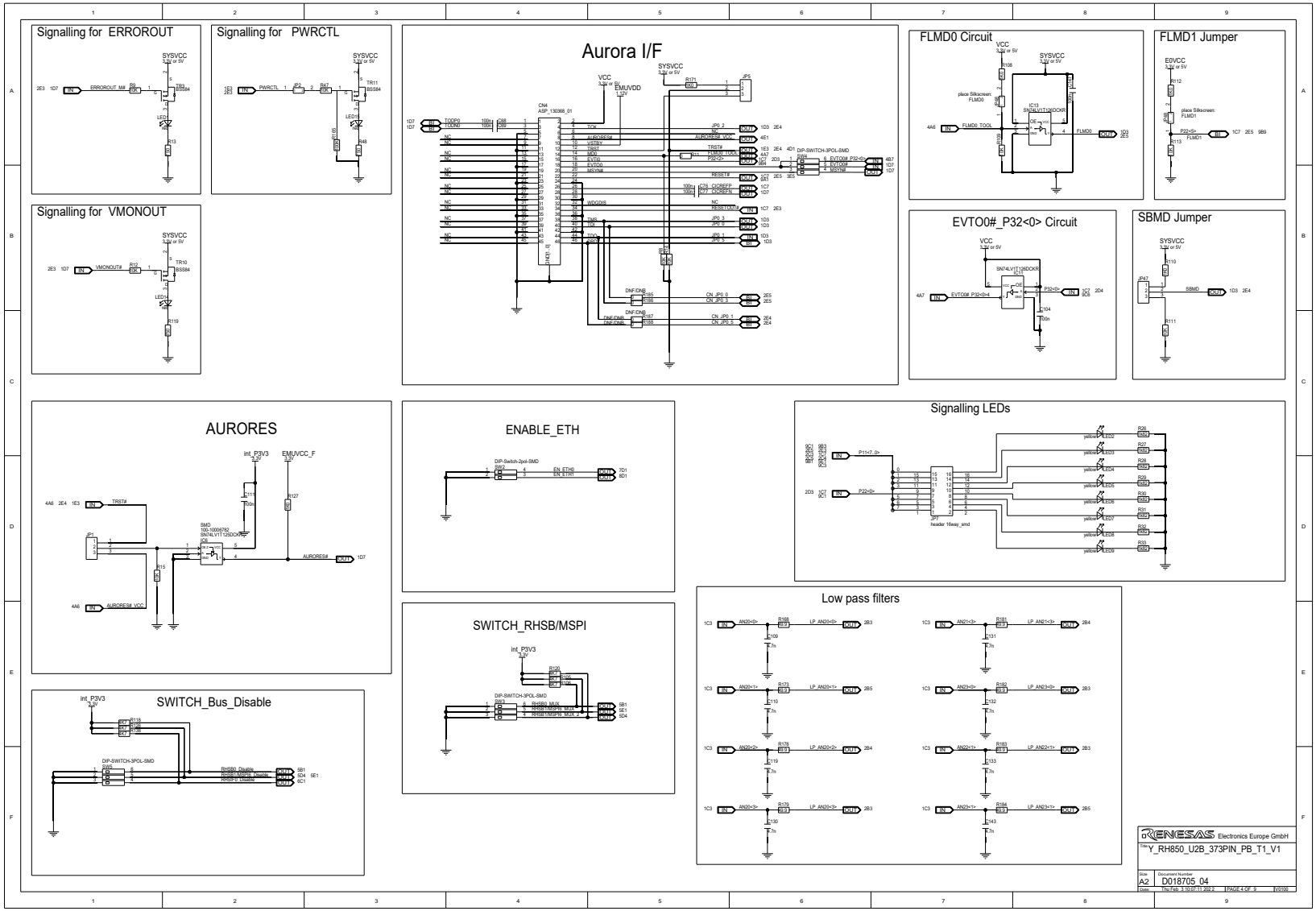
11.1.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D018705_04

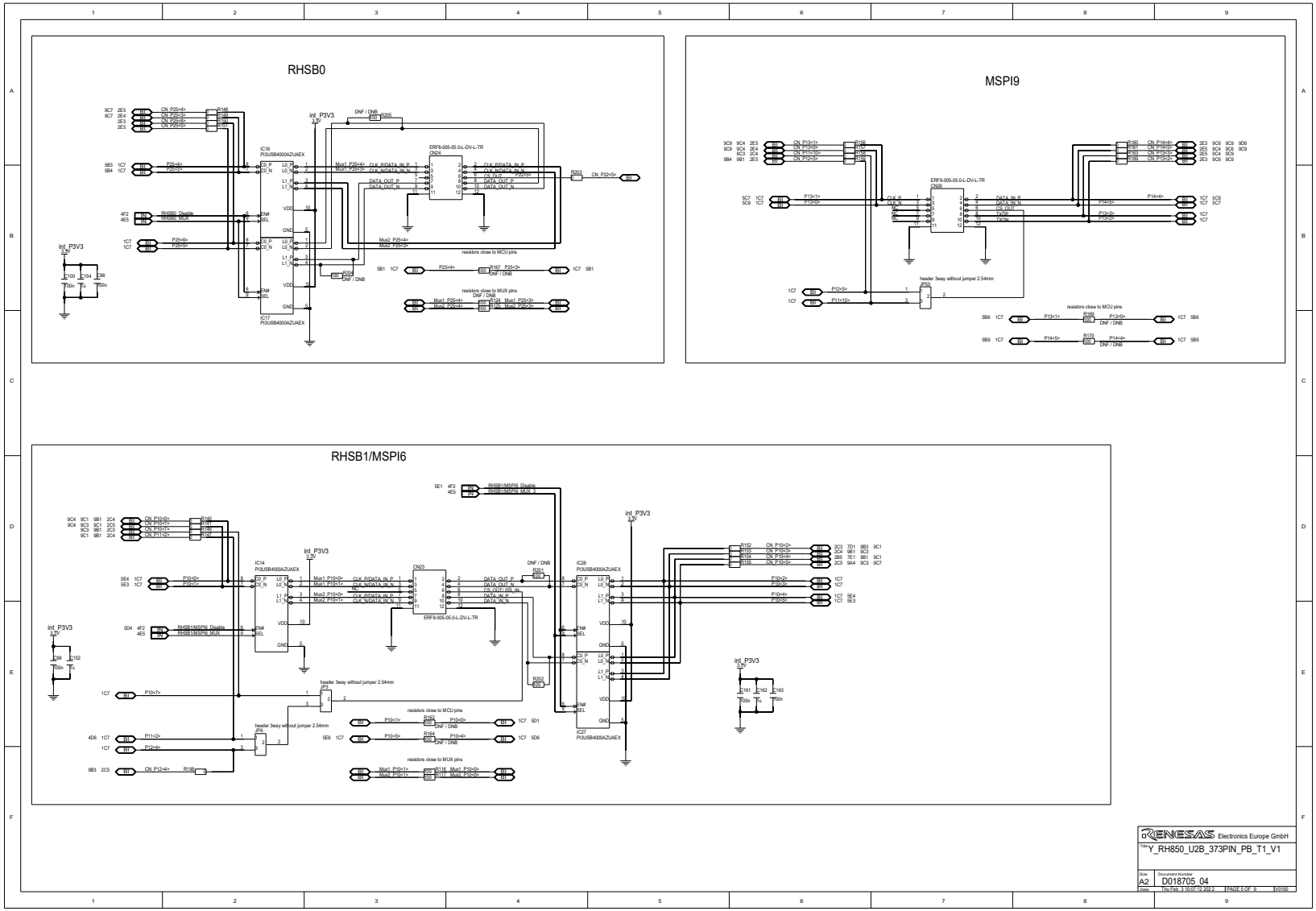
11.1.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
TO BE PRINTED ON PCB
GND
5.0V
3.3V
1.12V
CIRCUIT FOR RESET
PULL UP PULL DOWN
Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

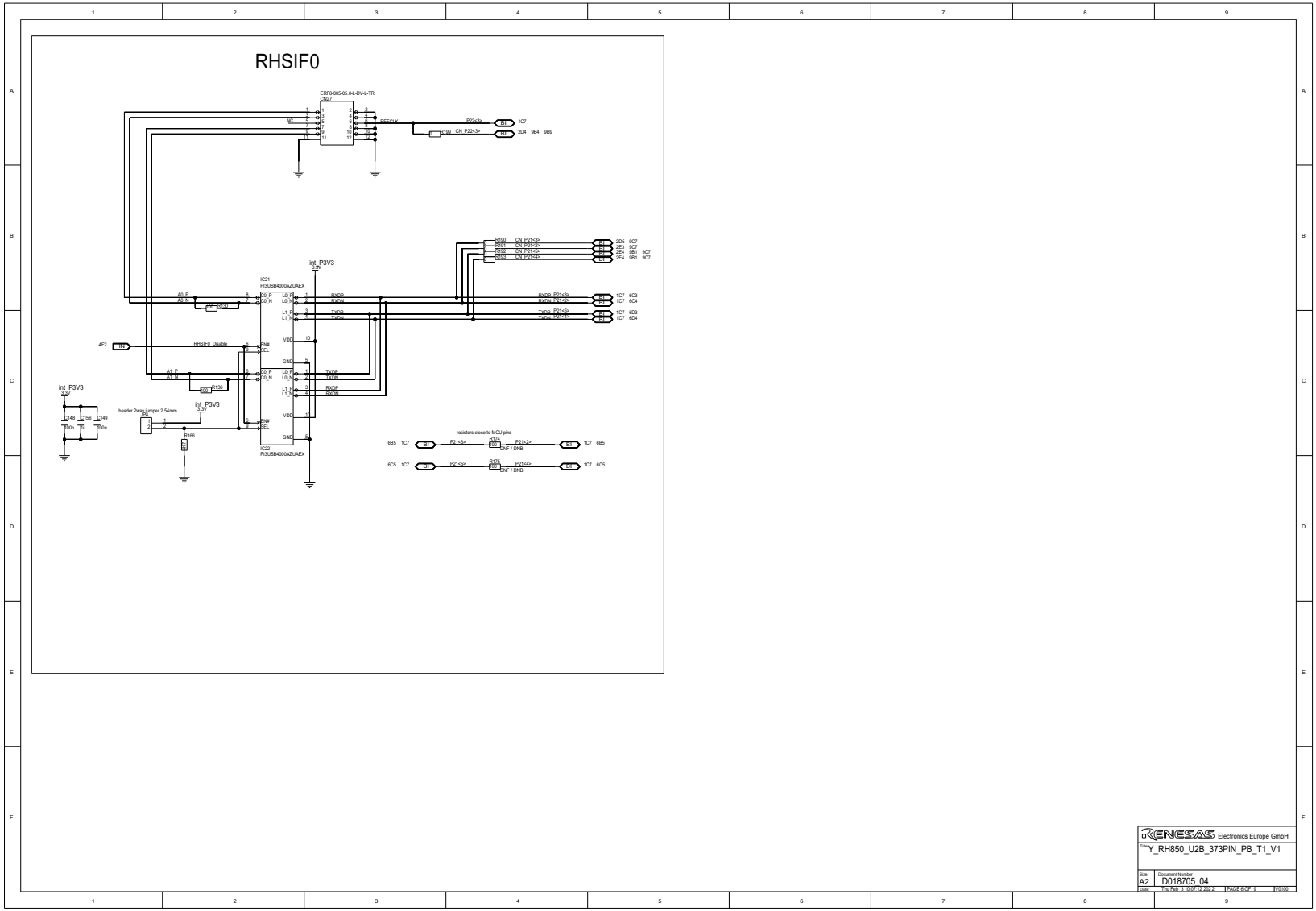
11.1.4 Page 4


Signalling for ERROROUT
Signalling for PWRCTL
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
EVTO0#_P32<0> Circuit
SBMD Jumper
AURORES
ENABLE_ETH
Signalling LEDs
SWITCH_RHSB/MSPI
Low pass filters
SWITCH_Bus_Disable
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

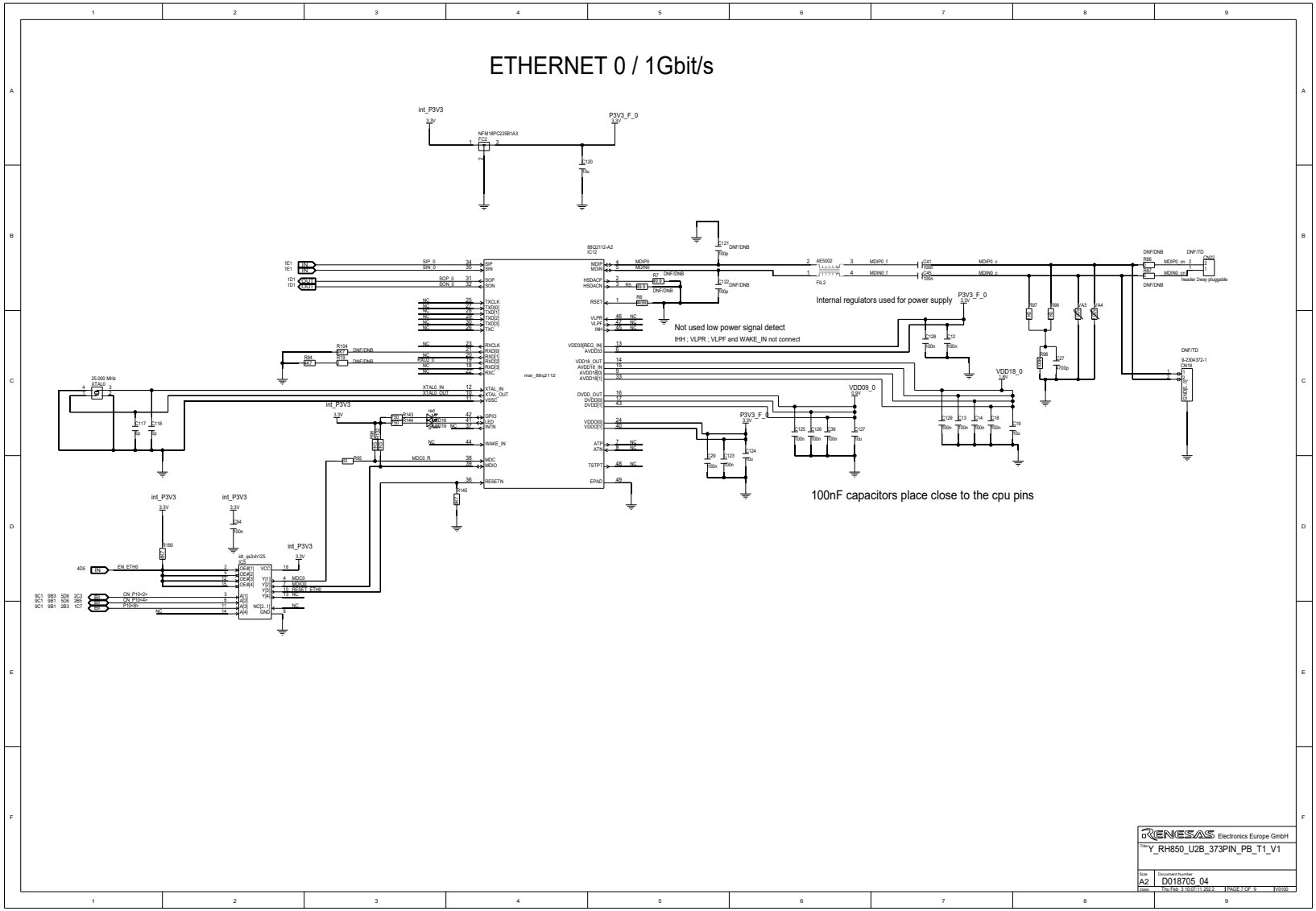
11.1.5 Page 5


RHSB0
MSPI9
RHSB1/MSPI6
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D018705_04

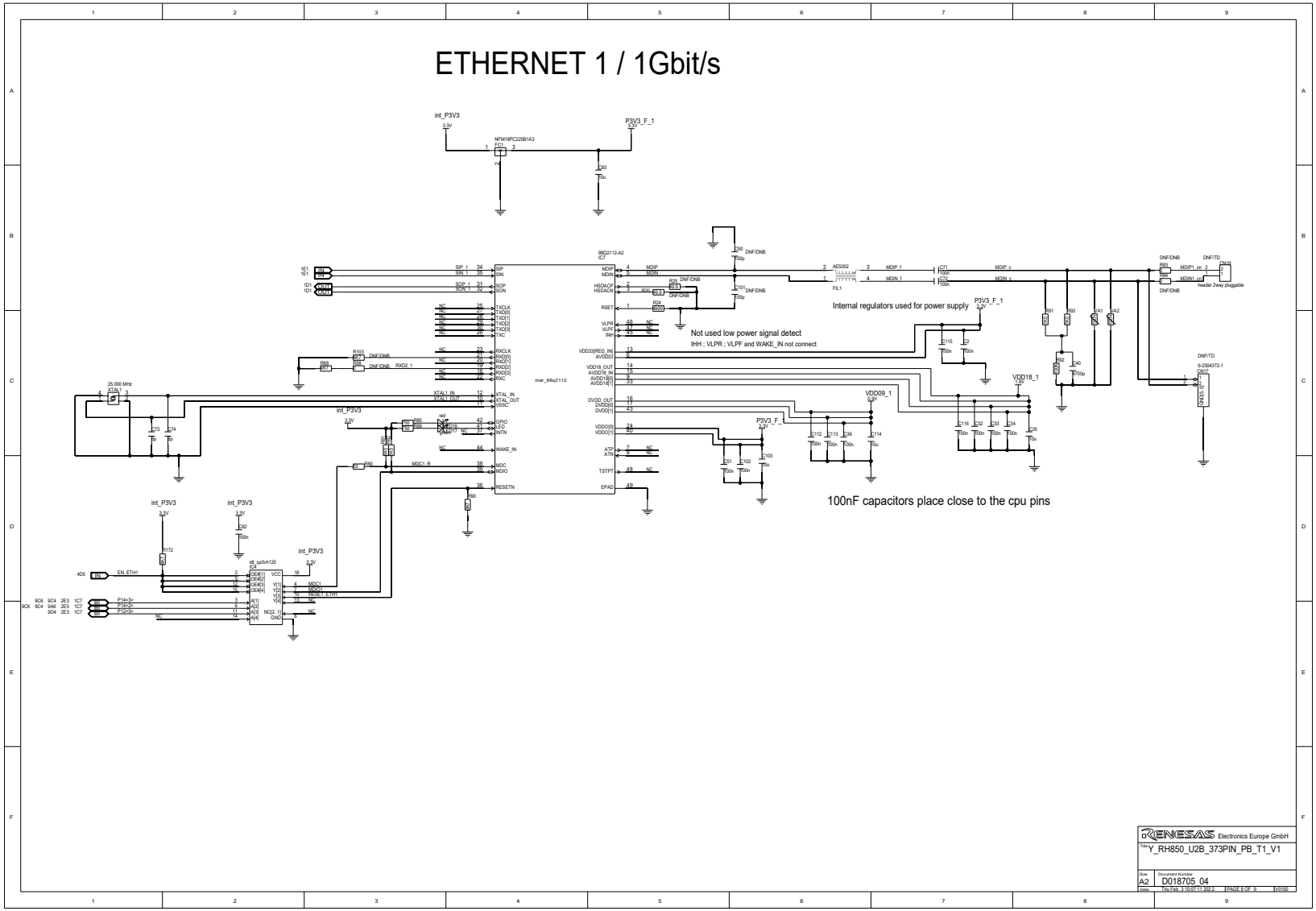
11.1.6 Page 6


RHSIF0
Int_P3V3
RHSIF0_Disable
header 2way jumper 2.54mm
resistors close to MCU pins
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

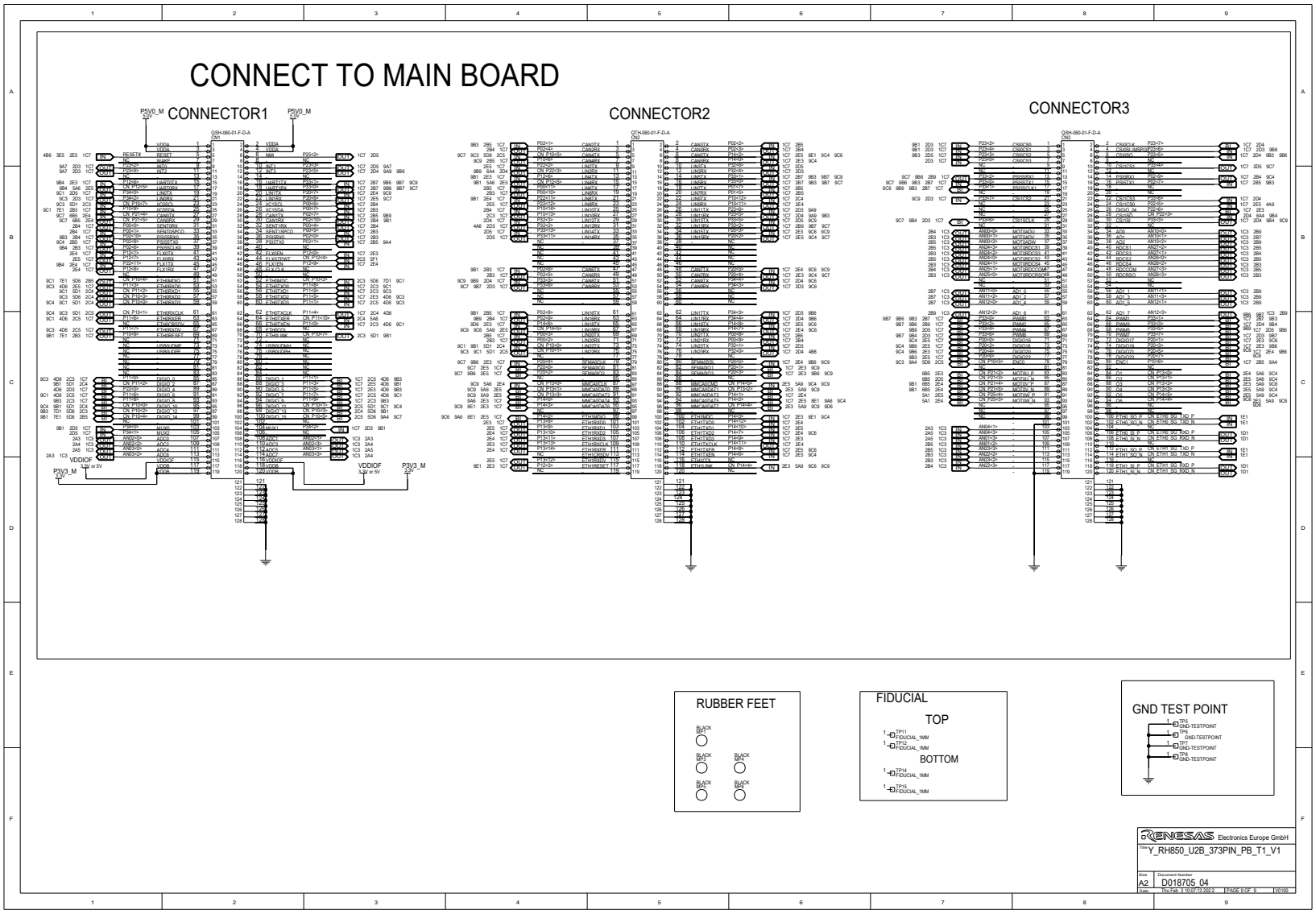
11.1.7 Page 7


ETHERNET 0 / 1Gbit/s
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

11.1.8 Page 8


ETHERNET 1 / 1Gbit/s
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

11.1.9 Page 9


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIAL
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D0187O5_04

11.2 Board Version D018705_06_V02

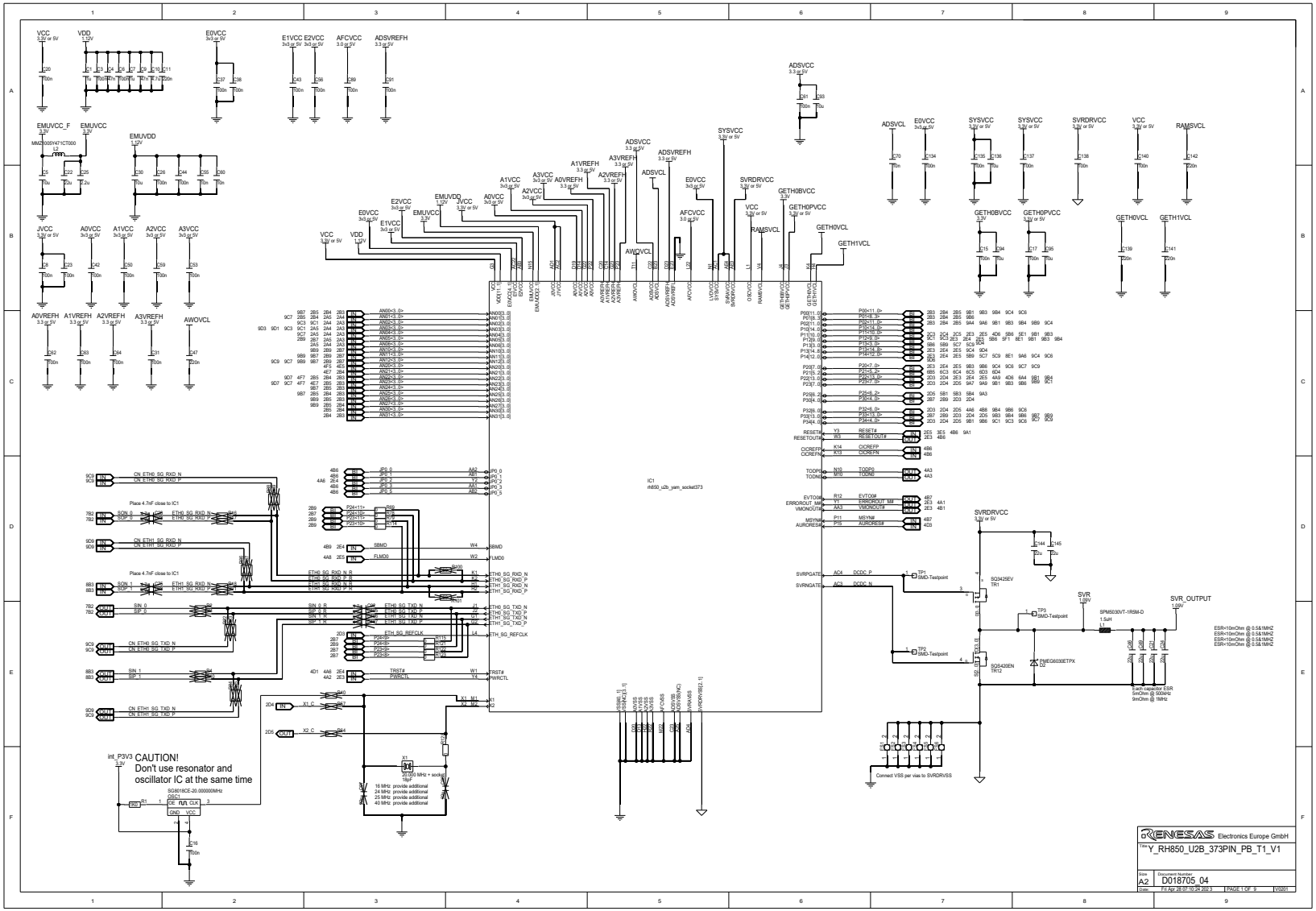
Not all components shown in the schematic are populated in production.

Components, which are not populated, are crossed out in the schematic like this: 

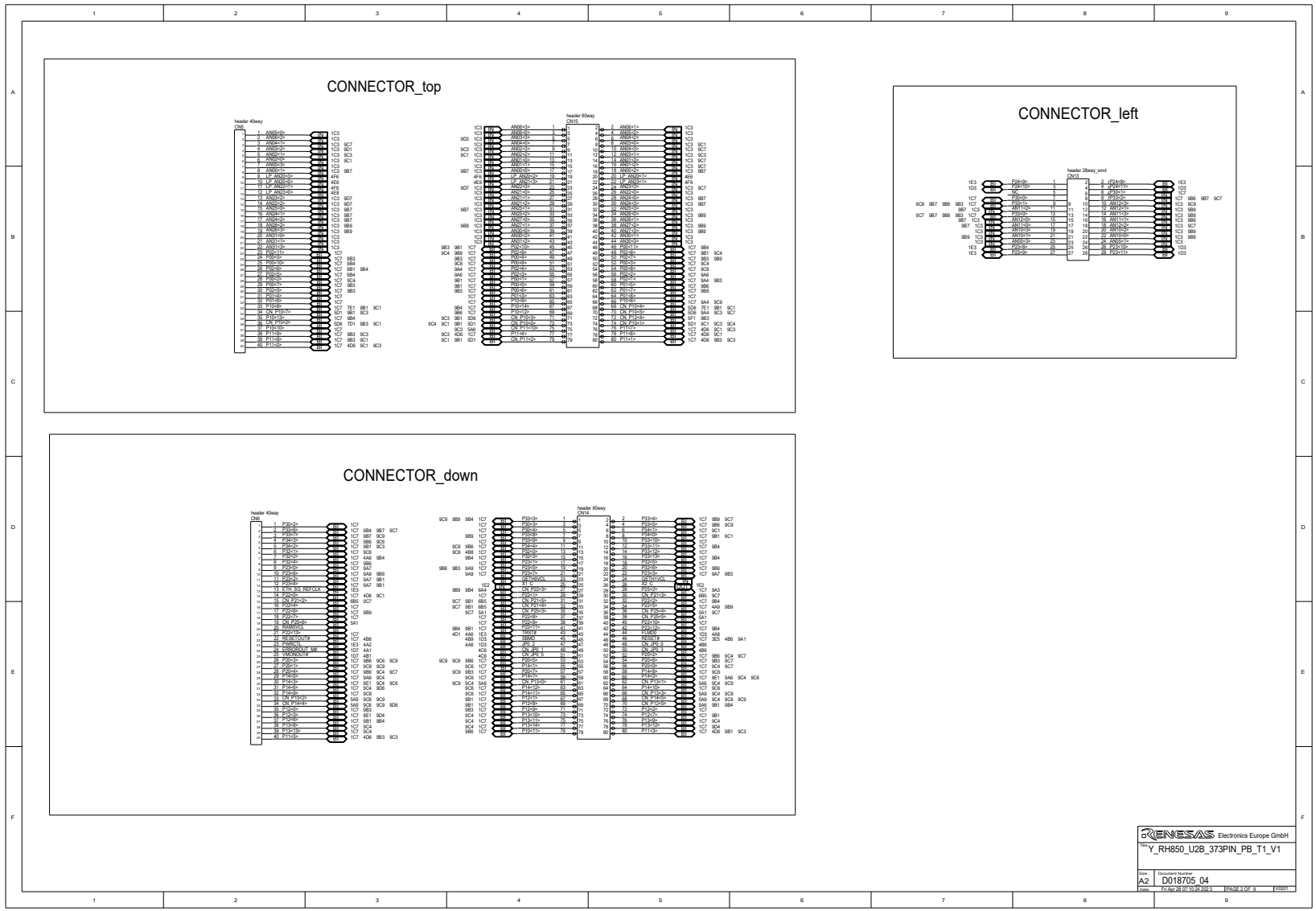
The following components, which are described in the schematics, are provided with the board but not mounted on the board upon delivery. These components have no special marking in the schematics other than that they are crossed out as not assembled components.

- 1 Hirschmann 4 mm power lab sockets, red for CN11
- Four resonators HC49 (16/24/25/40 MHz)
- 47 jumpers, 2.54 mm, black
- Resistors 100 Ohm: R124, R162, R164, R167, R169, R170, R174, R175, R201, R204, R205

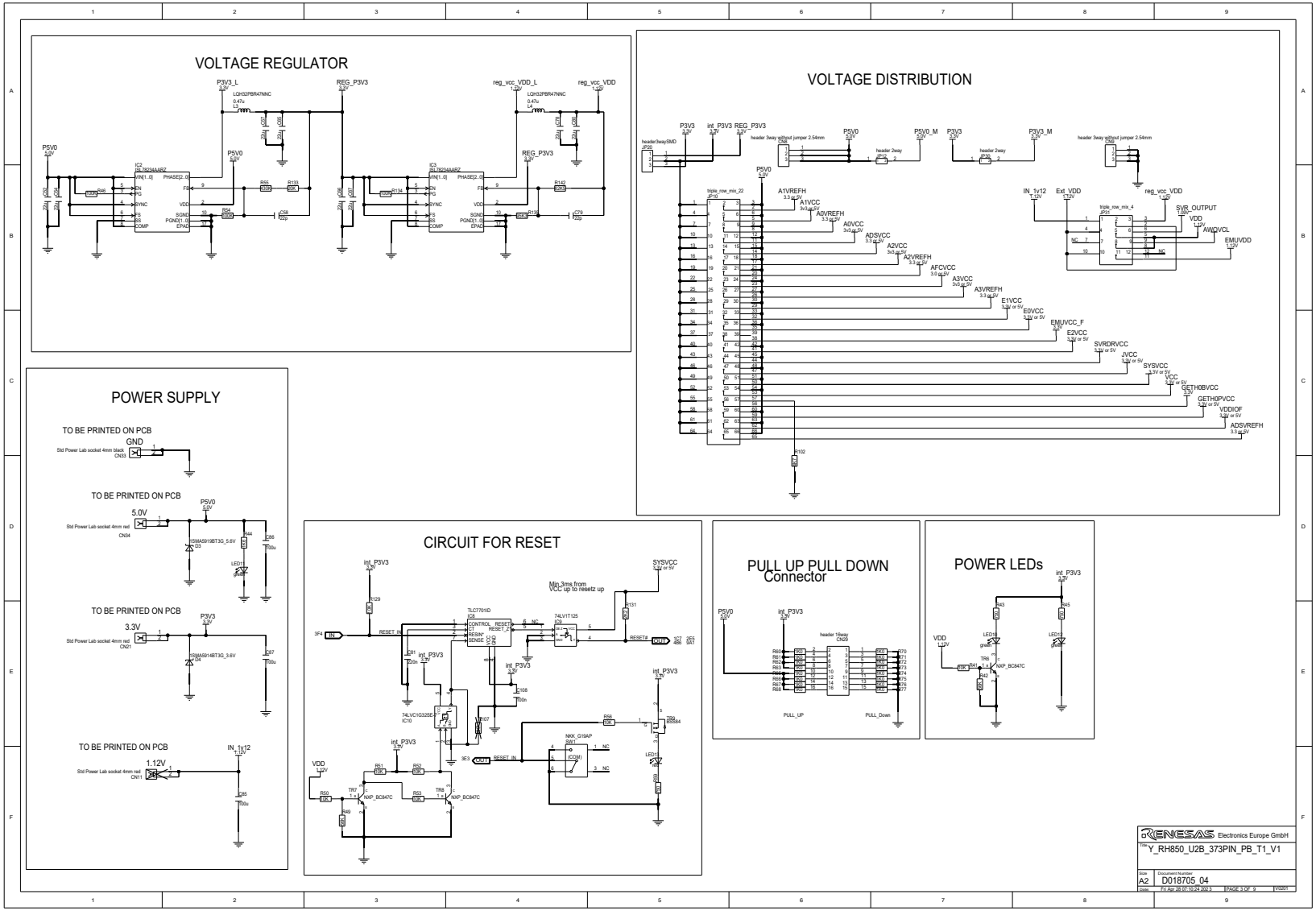
11.2.1 Page 1


RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_373PIN_PB_T1_V1
Size A2
Document Number D018705_04
Date Fri Apr 26 07:10:34 202 3
PAGE 1 OF 9
V0201
int_P3V3 CAUTION!
Don't use resonator and
oscillator IC at the same time
37.000 MHz + socket
16 MHz provide additional
24 MHz provide additional
25 MHz provide additional
40 MHz provide additional
IC1
rh850_u2b_yam_socket373
SVR_OUTPUT
Connect VSS per vias to SVRDRVSS

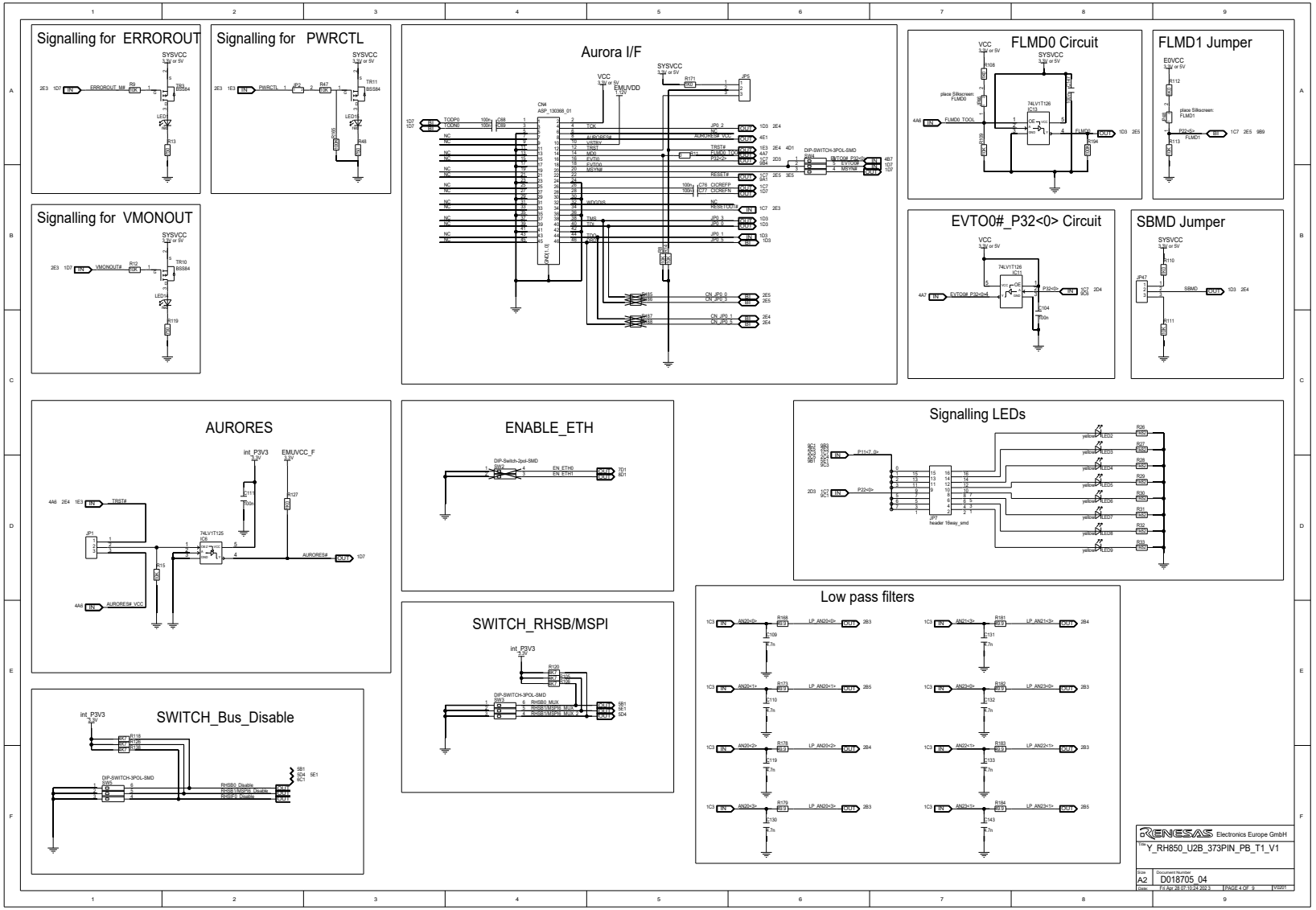
11.2.2 Page 2


CONNECTOR_top
CONNECTOR_left
CONNECTOR_down
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D018705_04

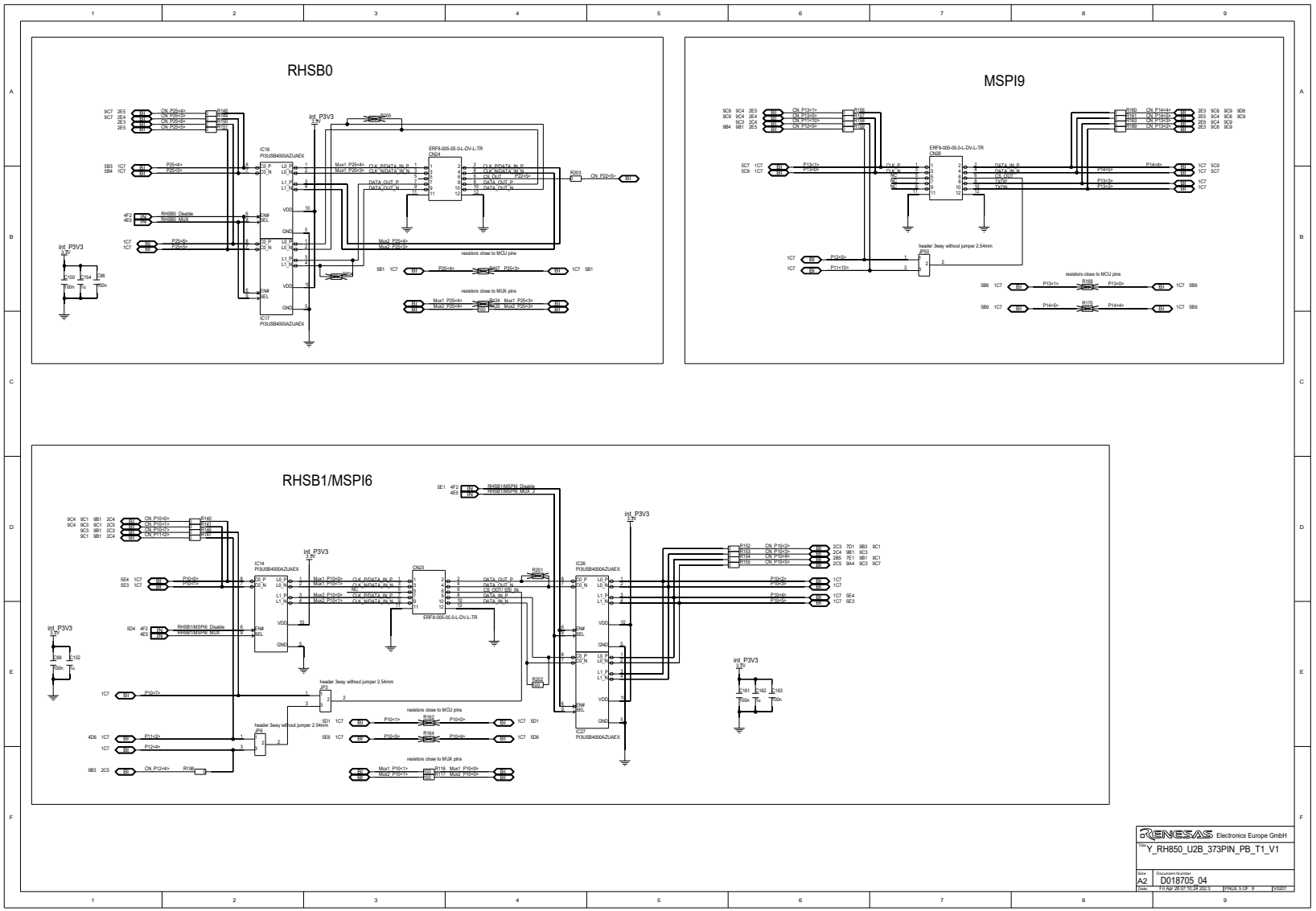
11.2.3 Page 3


VOLTAGE REGULATOR
VOLTAGE DISTRIBUTION
POWER SUPPLY
CIRCUIT FOR RESET
PULL UP PULL DOWN Connector
POWER LEDs
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D0018705_04

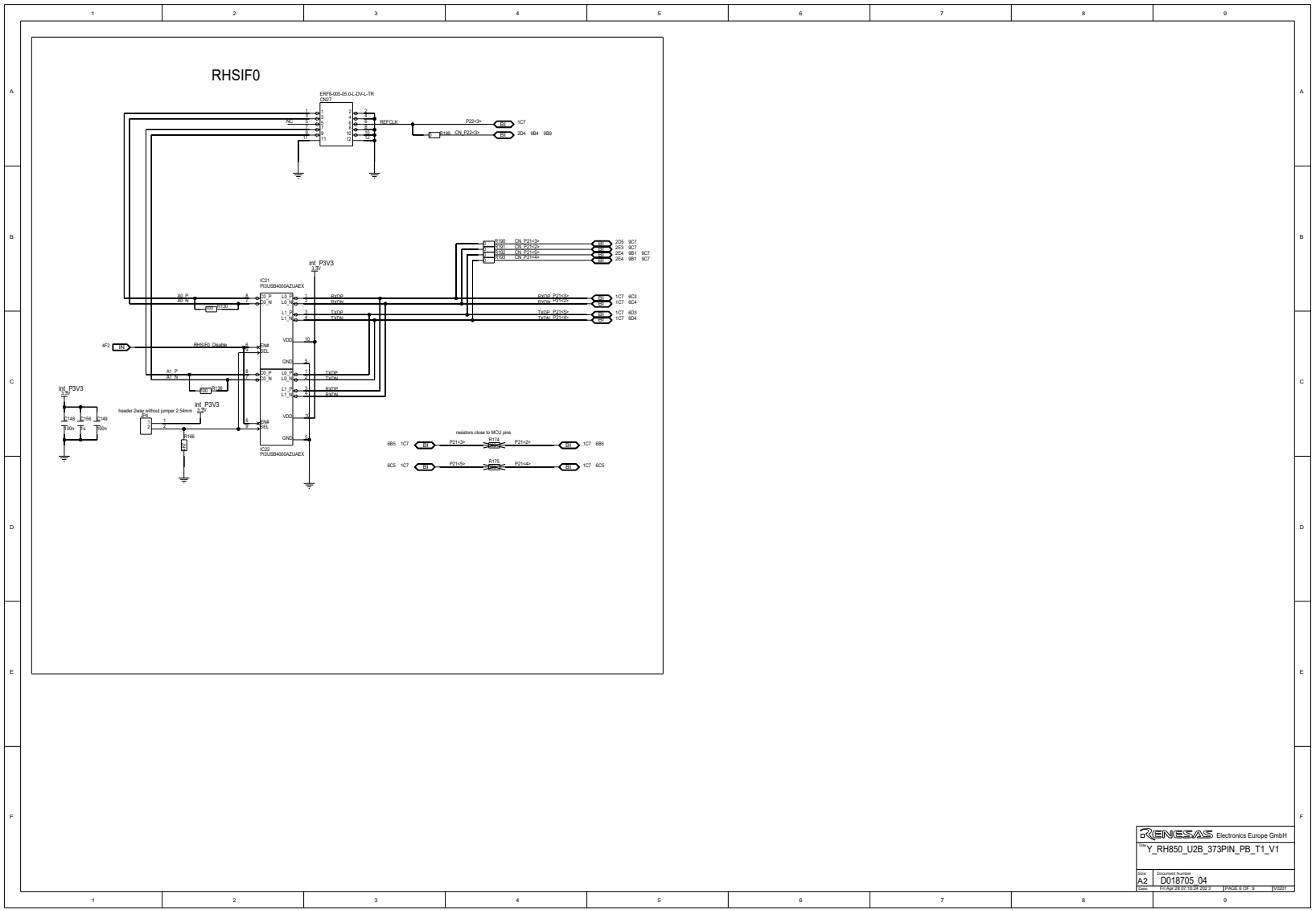
11.2.4 Page 4


Signalling for ERROROUT
Signalling for PWRCTL
Signalling for VMONOUT
Aurora I/F
FLMD0 Circuit
FLMD1 Jumper
EVTO0#_P32<0> Circuit
SBMD Jumper
AURORES
ENABLE_ETH
Signalling LEDs
SWITCH_RHSB/MSPI
Low pass filters
SWITCH_Bus_Disable
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D0187O5_04

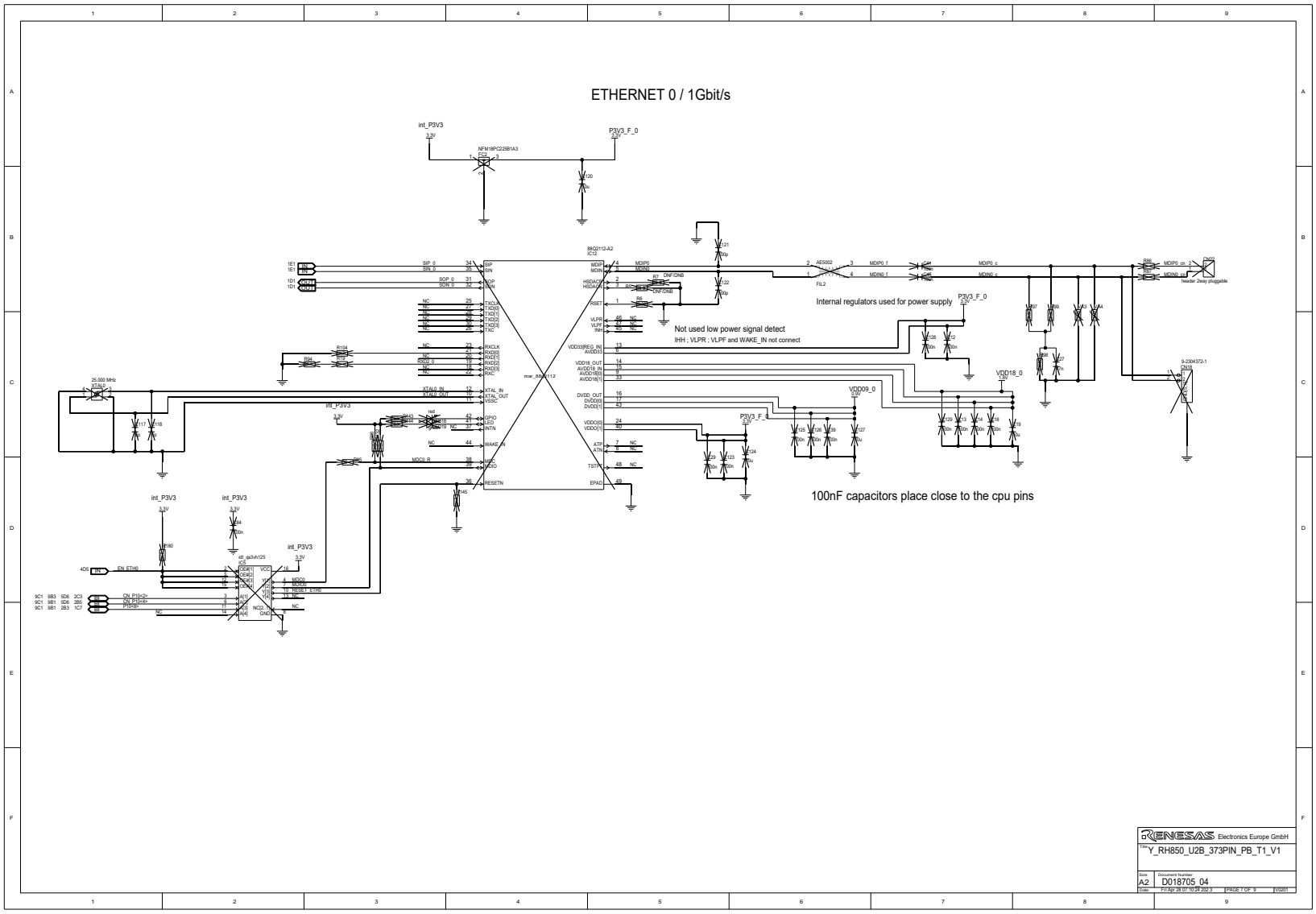
11.2.5 Page 5


RHSB0
MSPI9
RHSB1/MSPI6
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
A2
D0187O5_04

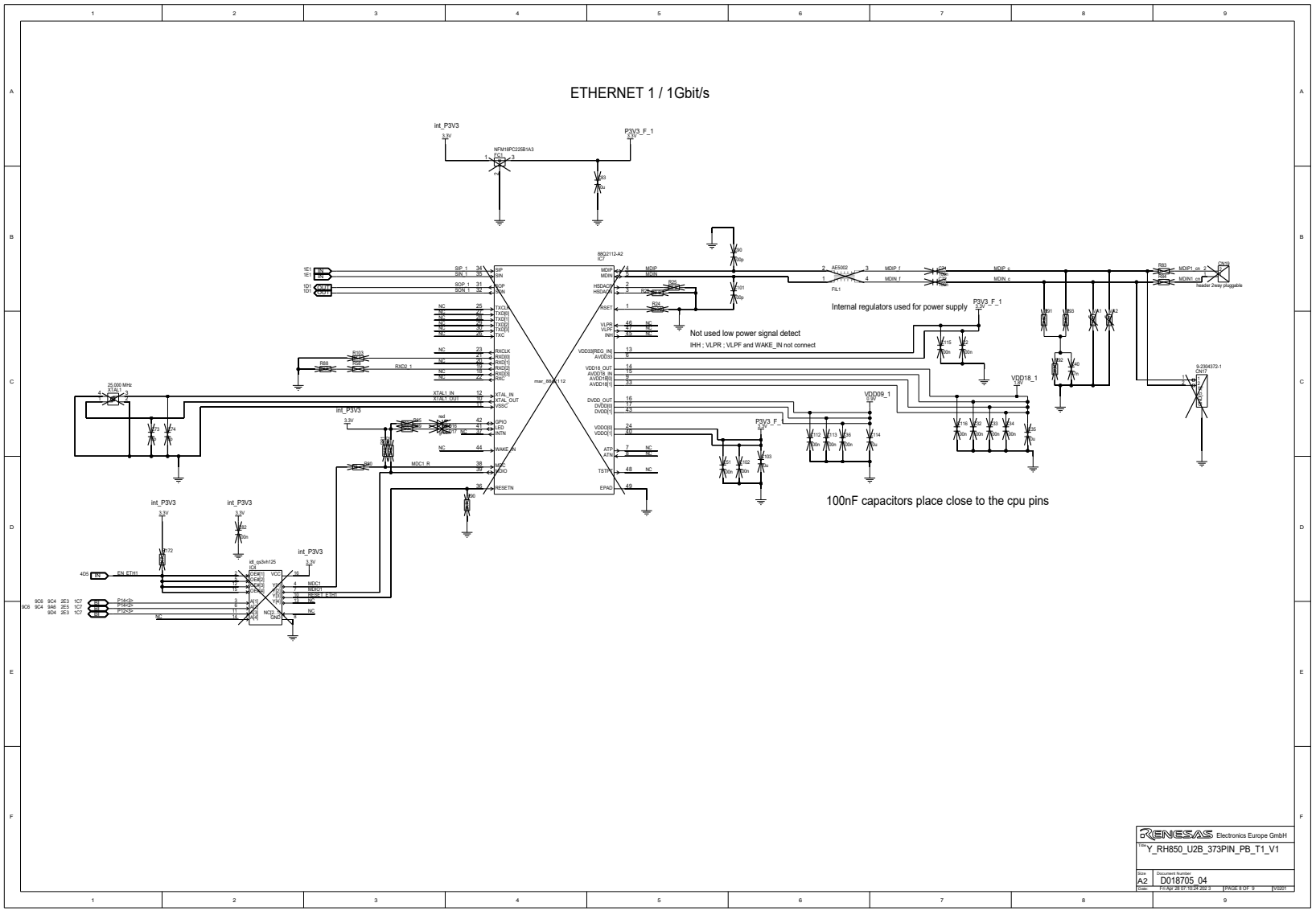
11.2.6 Page 6


RHSIF0
ERF8-005-05.0-L-DV-L-TR
CN27
REFCLK
P22<3>
R199 CN_P22<3>
int_P3V3
3.3V
IC21
PI3USB4000AZUAEX
A0_P
A0_N
R190
R191
R192
R193
CN_P21<3>
CN_P21<2>
CN_P21<1>
CN_P21<0>
RXDP
RXDN
TXDP
TXDN
RXDP_P21<3>
RXDN_P21<2>
TXDP_P21<1>
TXDN_P21<0>
4P2
IN
RHSIF0_Disable
ENB
SEL
VDD
GND
A1_P
A1_N
R197
R198
IC22
PI3USB4000AZUAEX
header 2way without jumper 2.54mm
J54
R196
C148
C156
C149
100n
1u
100n
resistors close to MCU pins
R174
R175
P21<3>
P21<2>
P21<1>
P21<0>
RENESAS Electronics Europe GmbH
Title Y_RH850_U2B_373PIN_PB_T1_V1
Size A2
Document Number D018705_04
Date Fri Apr 28 07:10:26 2023
Sheet PAGE 6 OF 9
V1.0.01

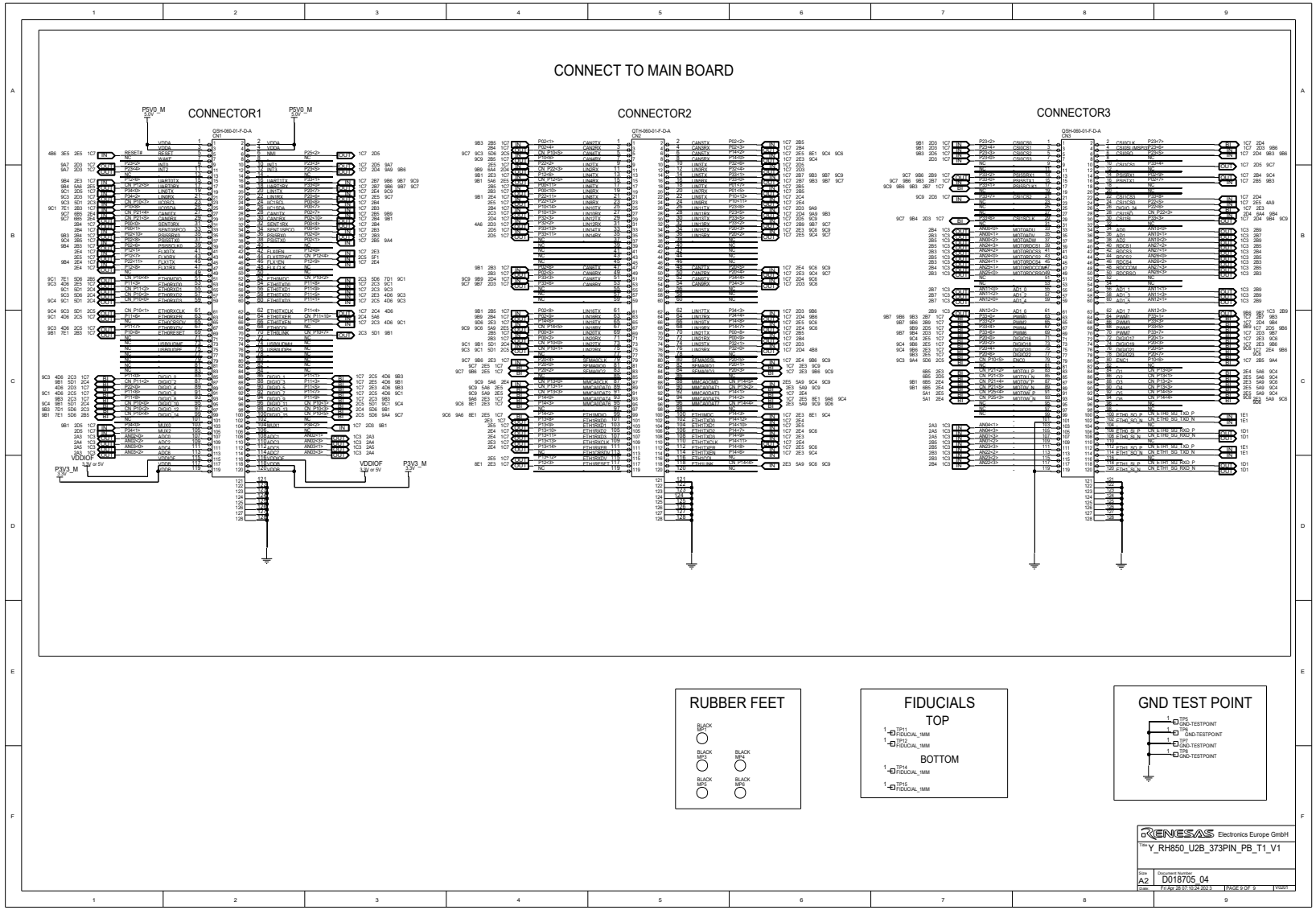
11.2.7 Page 7


ETHERNET 0 / 1Gbit/s
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

11.2.8 Page 8


ETHERNET 1 / 1Gbit/s
Internal regulators used for power supply
Not used low power signal detect
IHH ; VLPR ; VLPF and WAKE_IN not connect
100nF capacitors place close to the cpu pins
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

11.2.9 Page 9


CONNECT TO MAIN BOARD
CONNECTOR1
CONNECTOR2
CONNECTOR3
RUBBER FEET
FIDUCIALS
TOP
BOTTOM
GND TEST POINT
RENESAS Electronics Europe GmbH
Y_RH850_U2B_373PIN_PB_T1_V1
D018705_04

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
V1.00	2022-05-18	–	Initial release
V2.00	2023-04-28	–	Revised hardware
V2.01	2023-08-02	81 - 89	Updated schematics to version V2.01.
V2.02	2023-10-26	19, 68	Added precaution about power on of piggyback board without a microcontroller mounted. Caution in *3.1 Board Power Connection*. *9.2 Power On Piggyback Board Without RH850 Microcontroller installed*
V2.03	2025-05-15	28, 62	Added explanation for FLMD1 setting in Serial Programming Mode
		23	Updated explanation for core voltage generation in chapter *3.3 Device Core Voltage (VDD) Selection.*
		7	Updated package component list in *Table 1.1*.

RH850/U2B 373pin Piggyback Board V1 User's Manual: Piggyback Board

Publication Date: Rev.2.03 May 15, 2025

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