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Renesas Starter Kit for H8SX1582

User's Manual RENESAS SINGLE-CHIP MICROCOMPUTER H8SX FAMILY

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Chapter 1. Preface

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Glossary

BRR	Baud Rate Register
ERR	Error Rate
HMON	Embedded Monitor
RTE	Renesas Technology Europe Ltd.
RSK	Renesas Starter Kit
RSO	Renesas Solutions Corp.

Chapter 2.Purpose

This RSK is an evaluation tool for Renesas microcontrollers.

Features include:

- Renesas Microcontroller Programming.
- User Code Debugging.
- User Circuitry such as switches, LEDs and potentiometer(s).
- Sample Application.
- Sample peripheral device initialisation code.

The CPU board contains all the circuitry required for microcontroller operation.

This manual describes the technical details of the RSK hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

Chapter 3. Power Supply

3.1.Requirements

This CPU board operates from a 5V power supply.

A diode provides reverse polarity protection only if a current limiting power supply is used.

All CPU boards are supplied with an E8 debugger. This product is able to power the CPU board with up to 300mA. When the CPU board is connected to another system that system should supply power to the CPU board.

All CPU boards have an optional centre positive supply connector using a 2.0mm barrel power jack.

Warning

The CPU board is neither under not over voltage protected. Use a centre positive supply for this board.

3.2. Power - Up Behaviour

When the RSK is purchased the CPU board has the 'Release' or stand alone code from the example tutorial code pre-programmed into the Renesas microcontroller. On powering up the board the user LEDs will start to flash. Switch 2 will cause the LEDs to flash at a rate controlled by the potentiometer.

Chapter 4.Board Layout

4.1.Component Layout

The following diagram shows top layer component layout of the board.



Figure 4-1: Board Layout

4.2.Board Dimensions

The following diagram gives the board dimensions and connector positions. All through hole connectors are on a common 0.1" grid for easy interfacing.



Figure 4-2 : Board Dimensions

Chapter 5.Block Diagram

Figure 5-1 shows the CPU board components and their connectivity.



Figure 5-1: Block Diagram

Figure 5-2 shows the connections to the RSK.



Figure 5-2 : RSK Connctions

Chapter 6.User Circuitry

6.1.Switches

There are four switches located on the CPU board. The function of each switch and its connection are shown in Table 6-1.

Switch	Function	Microcontroller
RES	When pressed; the CPU board microcontroller is reset.	RESn
SW1/BOOT*	Connects to an IRQ input for user controls.	IRQ8-A, Pin 58
	The switch is also used in conjunction with the RES switch to place	(Port 2, pin 0)
	the device in BOOT mode when not using the E8 debugger.	
SW2*	Connects to an IRQ line for user controls.	IRQ9-A, Pin59
		(Port 2, pin 1)
SW3*	Connects to the ADC trigger input. Option link allows connection to	ADTRG, Pin 57
	IRQ line. The option is a pair of 0R links.	(Port 1, pin 7)
		OR
		IRQ10-A, Pin 60
		(Port 2, pin 2)

Table 6-1: Switch Functions

*Refer to schematic for detailed connectivity information.

6.2.LEDs

There are six LEDs on the CPU board. The green 'POWER' LED lights when the board is powered. The orange BOOT LED indicates the device is in BOOT mode when lit. The four user LEDs are connected to an IO port and will light when their corresponding port pin is set low.

Table 6-2, below, shows the LED pin references and their corresponding microcontroller port pin connections.

LED Reference (As	Microcontroller Port Pin	Microcontroller Pin	Polarity
shown on silkscreen)	function	Number	
LED0	Port I 0	113	Active Low
LED1	Port I 1	115	Active Low
LED2	Port I 2	118	Active Low
LED3	Port I 3	12	Active Low

Table 6-2:LED Port

6.3.Potentiometer

A single turn potentiometer is connected to ANO of the microcontroller. This may be used to vary the input analog voltage value to this pin between AVCC and Ground.

6.4.Serial port

The microcontroller programming serial port (SCI4) is connected to the E8 connector. This serial port can optionally be connected to the RS232 transceiver by moving option resistors and fitting the D connector in position J9. The connections to be moved are listed in the following table.

Description	Function	Fit For E8	Remove for E8	Fit for RS232	Remove for RS232
SCI4 Tx	Programming Serial Port	R15	R14	R14	R15
SCI4 Rx	Programming Serial Port	R12	R13	R13	R12
SCI4 Clk	Programming Serial Port	R10	NA	NA	NA

Table 6-3 - Serial Option Links

The board is designed to accept a straight through RS232 cable. A secondary microcontroller serial port is available and connected to the application headers. Please refer to the schematic diagram for more details on the available connections.

The serial baud rates supported by this CPU board are shown below. Note: these values are calculated from the frequency value of the main oscillating source fitted by default on this CPU board.

6MHz x 4 = 24MHz					Asynchi	onous Se	erial Baud	Rate Eva	aluation			
Ν	0			1			2 3		2			
	BRR	Rate	ERR	BRR	Rate	ERR	BRR	Rate	ERR	BRR	Rate	ERR
110										106	110	-0.44
300							155	300	0.16	38	300	0.16
1200				155	1202	0.16	38	1202	0.16	9	1172	-2.34
2400				77	2404	0.16	19	2344	-2.34	4	2344	-2.34
4800	155	4808	0.16	38	4808	0.16	9	4688	-2.34	1	5859	22.07
9600	77	9615	0.16	19	9375	-2.34	4	9375	-2.34	0	11719	22.07
19200	38	19231	0.16	9	18750	-2.34	1	23438	22.07			
38400	19	37500	-2.34	4	37500	-2.34	0	46875	22.07			
57600	12	57692	0.16	2	62500	8.51						
115200	6	107143	-6.99	1	93750	-18.62						
230400	2	250000	8.51									
250000	2	250000	0.00									
375000	1	375000	0.00									
750000	0	750000	0.00									

Table 6-4 : BRR Settings

6.5.LCD Module

A LCD module can be connected to the connector J13. Any module that conforms to the pin connections and has a KS0066u compatible controller can be used with the tutorial code. The LCD module uses a 4bit interface to reduce the pin allocation. No contrast control is provided; this must be set on the display module.

Table 6-5 shows the pin allocation and signal names used on this connector.

The module supplied with the CPU board only supports 5V operation.

	J13						
Pin Circuit Net Name		Device	Pin	Circuit Net Name	Device		
		Pin			Pin		
1	Ground	-	2	5V Only	-		
3	No Connection	-	4	DLCDRS	51		
5	R/W (Wired to Write only)	-	6	DLCDE	55		
7	No Connection	-	8	No connection	-		
9	No Connection	-	10		-		
11	DLCD4	68	12	DLCD5	67		
13	DLCD6	66	14	DLCD7	61		



6.6.Option Links

Table 6-6 below describes the function of the option links contained on this CPU board. The default configuration is indicated by **BOLD** text.

		Option Link Set	tings	
Reference	Function	Fitted	Alternative (Removed)	Related To
R10	Programming	Connects SCK to E8	SCK disconnected from E8	R12, R13,
	Serial Port			R14, R15
R12	Programming	Connects E8 to Programming	MUST be removed if R13 fitted.	R13
	Serial Port	Serial port.		
R15	Programming	Connects E8 to Programming	Should be removed if R14 fitted.	R14
	Serial Port	Serial port.		
R13	Programming	Connects RS232 port to	MUST be removed if R12 fitted.	R12
	Serial Port	Programming SCI port		
R14	Programming	Connects RS232 port to	Should be removed if R15 fitted.	R15
	Serial Port	Programming SCI port		
R62	RS232 Driver	Enables RS232 Serial Transceiver	MUST be removed if R18 Fitted	R18, R13,
				R14
R18	RS232 Driver	Disables RS232 Serial	MUST be removed if R62 Fitted	R62, R13,
		Transceiver		R14
R36	Serial Connector	Connects Alternate serial to D	Disconnects Alternate serial from D	R31
		connector	connector.	
R31	Serial Connector	Connects Alternate serial to D	Disconnects Alternate serial from D	R36
		connector	connector.	
R35	Alternate Serial	Connects Alternate Serial to	Should be removed if External serial	R37, JA6
		RS232 Transceiver	device.	
R37	Alternate Serial	Connects Alternate Serial to	MUST be removed if External serial	R35, JA6
		RS232 Transceiver	device.	
R53	External	Connects External Ring header	Disconnects sensitive microcontroller	R55
	Oscillator	pins to Microcontroller	signals from external pins.	
R55	External	Connects External Ring header	Disconnects sensitive microcontroller	R53
	Oscillator	pins to Microcontroller	signals from external pins.	
R46	Power	Supply to microcontroller	Fit Low ohm resistor to measure current	R63
R63	Analogue Power	Connects 5V supply to	Analogue supply MUST be provided from	JA1
		Analogue supply	external interface pins.	
R58	SW3	Connects SW3 to Analogue	Disconnected	R59
		Trigger input		
R59	SW3	Connects SW3 to IRQ input	Disconnected	R58
	L	· · ·		L

Table 6-7: 2-Pin jumpers

6.7.Oscillator Sources

A crystal oscillator is fitted on the CPU board and used to supply the main clock input to the Renesas microcontroller. Table 6-8 details the oscillators that are fitted and alternative footprints provided on this CPU board:

Component							
		Value : Package	Manufacturer				
Crystal (X1)	Fitted	6MHz : HC/49U	Approved	See <u>www.renesas.com</u> for details			
			CPU board	Magna Frequency Components	X6M0GCBE494SM*		
				C-Mac	LFXTAL017159		

Table 6-8: Oscillators / Resonators

Warning: When replacing the default oscillator with that of another frequency, the debugging monitor will not function unless the following are corrected:

- FDT programming kernels supplied are rebuilt for the new frequency
- The supplied HMON debugging monitor is updated for baud rate register settings.

The user is responsible for code written to support operating speeds other than the default. See the HMON User Manual for details of making the appropriate modifications in the code to accommodate different operating frequencies.

6.8.Reset Circuit

The CPU Board includes a simple latch circuit that links the mode selection and reset circuit. This provides an easy method for swapping the device between Boot Mode, User Boot Mode and User mode. This circuit is not required on customers boards as it is intended for providing easy evaluation of the operating modes of the device on the RSK. Please refer to the hardware manual for more information on the requirements of the reset circuit.

The reset circuit operates by latching the state of the boot switch on pressing the reset button. This control is subsequently used to modify the mode pin states as required.

The mode pins should change state only while the reset signal is active to avoid possible device damage.

The reset is held in the active state for a fixed period by a pair of resistors and a capacitor. Please check the reset requirements carefully to ensure the reset circuit on the user's board meets all the reset timing requirements.

Chapter 7.Modes

The CPU board supports User mode, Boot mode and User Boot mode. User mode may be used to run and debug user code, while Boot mode may only be used to program the Renesas microcontroller with program code. User Boot mode can only be used to program the User Mat (the main area of 768Kbytes of Flash ROM on the device). It does not support programming of the user boot area. User Boot mode is used to run a user supplied boot-loader program stored in the user boot MAT (the smaller area, 8Kbytes, of Flash ROM). To program the user boot MAT, the device must be in Boot mode. Further details of programming the MATs are available in the H8SX/1582 hardware manual.

When using the E8 debugger supplied with the RSK the mode transitions are executed automatically. The CPU board provides the capability of changing between User and Boot / User Boot modes using a simple latch circuit. This is only to provide a simple mode control on this board when the E8 is not in use.

To manually enter boot mode, press and hold the SW1/BOOT. The mode pins are held in their boot states while reset is pressed and released. Release the boot button. The BOOT LED will be illuminated to indicate that the microcontroller is in boot mode.

More information on the operating modes can be found in the device hardware manual.

7.1.FDT Settings

In the following sections the tables identify the FDT settings required to connect to the board using the E8Direct debugger interface. The 'A' interface is inverted on the RSK board. This is to ensure the board can function in a known state when the E8 is connected but not powered. The E8 Debugger contains the following 'pull' resistors.

E8 Pin	Resistor
А	Pull Down (100k)
В	Pull Up (100k)
С	Pull Down (100k)
D	Pull Up (100k)

Table 7-1: E8 Mode Pin drives

7.1.1.Boot mode

The boot mode settings for this CPU board are shown in Table 7-2 below:

MD1	MD0	LSI State after Reset	FDT S	ettings
		End	А	В
1	0	Boot Mode	0	0

Table 7-2: Mode pin settings

The following picture shows these settings made in the E8Direct configuration dialog from HEW.

Pin Settings		×
Workspace Workspace Industrial C Display Device Inage Traget files UCD.met	Please select the pin settings BOOT Mode using Clock Mode Operating Mode: 1: Boot Mode	V
12 E8 B1 S Comme.möt 12 14 Motor Control Device Image 14 14 2 Device Image 15 14 2 Device Image 14 2 Device Image Device Image 15 14 2 Device Image 16 Device Image Data.mot Device Image 17 10 Data.mot Device.mot 17 10 Data.mot Device.mot 17 16 Device.mot Device.mot 18 14 15 5 14	C D B BOOT Mode C I I Outputs BOOT Mode I I I Setting I I I	A I = 0x11 □ = 0x00
	< Back. Next >	Cancel

Figure 7-1: Boot Mode FDT configuration

7.1.2.User Boot mode

A Note on Mats:

The H8SX/1582 possesses two distinct areas of Flash, User MAT (768KByte) and User Boot MAT (8KByte). The User Boot MAT is a separate area of FLASH from User MAT, intended to hold user boot code.

A custom boot stub could be programmed into User Boot MAT which allows programming and erasing of the User MAT in User Mode, without erasing the contents of the User Boot MAT. Once User Boot Mode is entered, code contained in the User Boot MAT is executed. This differs to Boot mode, as Boot mode erases all User MAT and requires an auto-baud on a fixed SCI port to be performed. The existence of the User Boot Mat therefore allows an alternative communications port to be used for further code download to the User MAT. Programming of the User Boot Mat may only be performed in boot mode.

The user may place the H8SX/1582 device provided on a CPU board for the H8SX1582 board in user boot mode by fitting jumper J13. The Boot procedure must then be performed for entry into user boot mode. The Boot LED should light, suggesting a transition to user boot mode.

The user boot mode settings for this CPU board are shown in Table 7-3 below:

MD1	MD0	LSI State after Reset End	FDT Settings A B	
			A B	
0	1	User Boot Mode	1	1

Table 7-3: Mode pin settings

7.1.3.User Mode

For the device to enter User Mode, reset must be held active while the microcontroller mode pins are held in states specified for User Mode operation. 100K pull up and pull down resistors are used to set the pin states during reset.

The H8SX/1582 supports 4 user modes. The memory map in all of these modes is 16Mbyte in size. The default user mode for CPU board supporting H8SX1582 is 7.

MD1	MD0	LSI State after Reset	FDT S	ettings
		End	Α	В
1	1	User Mode	0	1

Pin Settings		×
Workspace of DA FF 55	Please select the pin settings	
7 Control Display- 10 Display-	Operating Mode: 3: User Mode	
Motor Control	C D B USER Mode IT IT Outputs	A 📈 = 0x11
8 92 1A 20 95 Drive mot	USER Mode 🗖 🗖 🔽 Setting	☐ = 0x10
6 F0 56 FD 5 F1 A F1	USER Program Mode Setting	☐ = 0x10
	< <u>B</u> ack <u>N</u> ext>	Cancel

Table 7-4: Mode pin settings

Figure 7-2: User mode FDT configuration

Chapter 8. Programming Methods

All of the Flash ROM on the device (i.e. both MATs) can be programmed when the device is in Boot mode. Once in boot mode, the boot-loader program pre-programmed into the microcontroller executes and attempts a connection with a host (for example a PC). On establishing a connection with the microcontroller, the host may then transmit program data to the microcontroller via the appropriate programming port.

Table 8-1 below shows the programming port for this Renesas Microcontroller and its associated pins

Programming Po	Programming Port Table – Programming port pins and their CPU board signal names								
SCI4 TXD4, PIN 5 RXD4, PIN 7 SCK4, PIN 8									
CPU board Signal Name	PTTX	PTRX	РТСК						

Table 8-1: Serial Port Boot Channel

8.1.Serial Port Programming

This sequence is not required when debugging using the E8 supplied with the kit.

The microcontroller must enter boot mode for programming, and the programming port must be connected to a host for program download. To execute the boot transition, and allow programs to download to the microcontroller, the user must perform the following procedure:

Connect a 1:1 serial cable between the host PC and the CPU board

Depress the BOOT switch and keep this held down

Depress the RESET switch once, and release

Release the BOOT switch

The Flash Development Toolkit (FDT) is supplied to allow programs to be loaded directly on to the board using this method.

8.2.E10A Header

This device supports an optional E10A debugging interface. The E10A provides additional debugging features including hardware breakpoints and hardware trace capability. (Check with the website at <u>www.renesas.com</u> or your distributor for a full feature list).

To utilise the E10A the user will need to fit a 14 way boxed header to J7. To enable the E10A functions the user should also fit a jumper link in position J6.

When J6 is fitted the microcontroller will not operate correctly unless operated via the E10A.

Chapter 9.Headers

9.1. Microcontroller Headers

Table 9-1 to Table 9-4 show the microcontroller pin headers and their corresponding microcontroller connections. The header pins connect directly to the microcontroller pin unless otherwise stated.

		J	1		
Pin	Circuit Net Name	Device	Pin	Circuit Net Name	Device
		Pin			Pin
1	SCIbRX	1	2	SCIbCK	2
3	PIN3	3	4	UC_VCC	4
5	PTTX	5	6	GROUND	6
7	PTRX	7	8	РТСК	8
9	TDO	9	10	PIN10	10
11	TRIGb	11	12	LED3	12
13	PIN13	13	14	MO_Up	14
15	MO_Vp	15	16	PIN16	16
17	MO_Wp	17	18	CTSRTS	18
19	PIN19	19	20	PIN20	20
21	PIN21	21	22	PIN22	22
23	TRISTn	23	24	GROUND	24
25	MO_Un	25	26	UC_VCC	26
27	MO_Vn	27	28	MO_UD	28
29	PIN29	29	30	MO_Wn	30

Table 9-1: J1

		J	2		
Pin	Circuit Net Name	Device	Pin	Circuit Net Name	Device
		Pin			Pin
1	PIN31	31	2	PIN32	32
3	PIN33	33	4	PIN34	34
5	PIN35	35	6	IO_0	36
7	PIN37	37	8	I0_1	38
9	IO_2	39	10	IO_3	40
11	IO_4	41	12	IO_5	42
13	PIN43	43	14	IO_6	44
15	IO_7	45	16	UC_VCC	46
17	IRQ0	47	18	GROUND	48
19	IRQ1	49	20	GROUND	50
21	DLCDRS	51	22	IRQ2	52
23	IRQ3	53	24	SCIaTX	54
25	SCIaRX	55	26	SCIaCK	56
27	ADTRG	57	28	SW1	58
29	SW2	59	30	SW3	60

Table 9-2: J2

		J	13		
Pin	Circuit Net Name	Device	Pin	Circuit Net Name	Device
		Pin			Pin
1	DLCD7	61	2	GROUND	62
3	PIN63	63	4	UC_VCC	64
5	DLCDE	65	6	DLCD6	66
7	DLCD5	67	8	DLCD4	68
9	TMR0	69	10	TMR1	70
11	PIN71	71	12	PIN72	72
13	PIN73	73	14	TRSTn	74
15	TMS	75	16	TDI	76
17	ТСК	77	18	PIN78	78
19	RESn	79	20	NMI	80
21	TRIGa	81	22	UC_VCC	82
23	CON_XTAL	83	24	CON_EXTAL	84
25	GROUND	85	26	EMLE	86
27	SCICTX	87	28	PIN88	88
29	SCICRX	89	30	SCIcCK	90

Table 9-3: J3

		~	J4		
Pin	Circuit Net Name	Device	Pin	Circuit Net Name	Device
		Pin			Pin
1	E8_BUSY	91	2	MD1_E8B	92
3	AD4	93	4	AD5	94
5	AD6	95	6	AD7	96
7	AD0	97	8	AD1	98
9	AD2	99	10	AVcc	100
11	AD3	101	12	AVss	102
13	AD_POT	103	14	AVcc	104
15	PIN105	105	16	PIN106	106
17	PIN107	107	18	PIN108	108
19	PIN109	109	20	PIN110	110
21	PIN111	111	22	MD0_E8A	112
23	LED0	113	24	IIC_SDA	114
25	LED1	115	26	PIN116	116
27	IIC_SCL	117	28	LED2	118
29	IIC_EX	119	30	SCIbTX	120

Table 9-4: J4

9.2. Application Headers

					JA1				
Pin	Generic Hea	der Name	CPU board	Device	Pin	Header N	Header Name		Device
			Signal Name	Pin				Signal Name	Pin
1	Regulated Su	ipply 1	5V		2	Regulated Supp	oly 1	GROUND	
3	Regulated Su	ipply 2	3V3		4	Regulated Supp	oly 2	GROUND	
5	Analogue Su	oply	AVcc	100,104	6	Analogue Supp	ly	AVss	102
7	Analogue Re	ference	AVref		8	ADTRG	ADTRG		57
9	ADC0	10	AD0	97	10	ADC1	11	AD1	98
11	ADC2	12	AD2	99	12	ADC3	13	AD3	101
13	DAC0		DAC0		14	DAC1		DAC1	
15	IOPort		IO_0	36	16	IOPort		10_1	38
17	IOPort		IO_2	39	18	IOPort		10_3	40
19	IOPort		IO_4	41	20	IOPort		IO_5	42
21	IOPort		10_6	44	22	IOPort		10_7	45
23	Open drain	IRQAEC	IRQ3	53	24	I ² C Bus - (3rd pin)		IIC_EX	119
25	I ² C Bus		IIC_SDA	114	26	I ² C Bus		IIC_SCL	117

Table 9-5 and Table 9-6 below show the standard application header connections.

Table 9-5: JA1 Standard Generic Header

					JA2			
Pin	Generic Head	er Name	CPU board	Device	Pin	Header Name	CPU board	Device
			Signal Name	Pin			Signal Name	Pin
1	Open drain		RESn	79	2	External Clock Input	EXTAL	84*
3	Open drain		NMIn	80	4	Regulated Supply 1	Vss1	
5	Open drain out	out	WDT_OVF		6	Serial Port	SCIaTX	54
7	Open drain	WUP	IRQ0	47	8	Serial Port	SCIaRX	55
9	Open drain		IRQ1	49	10	Serial Port	SCIaCK	56
11	Up/down		MO_UD	28	12	Serial Port Handshake	CTS/RTS	18
13	Motor control		MO_Up	14	14	Motor control	MO_Un	25
15	Motor control		MO_Vp	15	16	Motor control	MO_Vn	27
17	Motor control		MO_Wp	17	18	Motor control	MO_Wn	30
19	Output		TMR0	69	20	Output	TMR1	70
21	Input		TRIGa	81	22	Input	TRIGb	11
23	Open drain		IRQ2	52	24	Tristate Control	TRSTn	74
25	SPARE		-		26	SPARE	-	

Table 9-6: JA2 Standard Generic Header

	JA5												
Pin	Generic He	eader Name	CPU board	Device	Pin	Heade	r Name	CPU board	Device				
			Signal Name	Pin				Signal Name	Pin				
1	ADC4	14	AD4	93	2	ADC5	15	AD5	94				
3	ADC6	16	AD6	95	4	ADC7	17	AD7	96				
5	CAN	•	CAN1TX		6	CAN		CAN1RX					
7	7 CAN		CAN2TX		8	CAN		CAN2RX					
9	9 Reserved				10	Reserved							
11	Reserved				12	Reserved							
13	Reserved				14	Reserved							
15	Reserved				16	Reserved							
17	Reserved				18	Reserved							
19	Reserved				20	Reserved							
21	Reserved				22	Reserved							
23	Reserved				24	Reserved							

Table 9-7: JA5 Optional Generic Header

JA6									
Pin	Generic Header Name		CPU board	Device	Pin	Header Name		CPU board	Device
			Signal	Pin				Signal Name	Pin
			Name						
1	DMA		DREQ		2	DMA		DACK	
3	DMA		TEND		4	Standby (Open drain)		STBYn	
5	Host Serial	SCIdTX	RS232TX	5*	6	Host Serial	SCIdRX	RS232RX	7*
7	Serial Port		SCIbRX	1	8	Serial Port		SCIbTX	120
9	Serial Port	Synchronous	SCIcTX	87	10	Serial Port		SCIbCK	2
11	Serial Port	Synchronous	SCIcCK	90	12	Serial Port	Synchronous	SCIcRX	89
13	Reserved				14	Reserved			
15	Reserved				16	Reserved			
17	Reserved				18	Reserved			
19	Reserved				20	Reserved			
21	Reserved				22	Reserved			
23	23 Reserved				24	Reserved			
25	25 Reserved				26	Reserved			

Table 9-8: JA6 Optional Generic Header

* Marked pins are affected by option links.

Chapter 10.Code Development

10.1.Overview

Note: For all code debugging using Renesas software tools, the CPU board must either be connected to a PC serial port via a serial cable or a PC USB port via an E8. An E8 is supplied with the RSK product.

The HMON embedded monitor code is modified for each specific Renesas microcontroller. HMON enables the High-performance Embedded Workshop (HEW) development environment to establish a connection to the microcontroller and control code execution. Breakpoints may be set in memory to halt code execution at a specific point.

Unlike other embedded monitors, HMon is designed to be integrated with the user code. HMon is supplied as a library file and several configuration files. When debugging is no longer required, removing the monitor files and library from the code will leave the user's code operational.

The HMON embedded monitor code must be compiled with user software and downloaded to the CPU board, allowing the users' code to be debugged within HEW.

Due to the continuous process of improvements undertaken by Renesas the user is recommended to review the information provided on the Renesas website at <u>www.renesas.com</u> to check for the latest updates to the Compiler and Debugger manuals.

10.2.Compiler Restrictions

The compiler supplied with this RSK is fully functional for a period of 60 days from first use. After the first 60 days of use have expired, the compiler will default to a maximum of 64k code and data. To use the compiler with programs greater than this size you will need to purchase the full tools from your distributor.

Warning: The protection software for the compiler will detect changes to the system clock. Changes to the system clock back in time may cause the trial period to expire prematurely.

10.3.Mode Support

The HMON library is built to support 16Mbyte Advanced Mode only for the H8SX family.

10.4.Breakpoint Support

The device does not include a user break controller. No breakpoints can be located in ROM code. However, code located in RAM may have multiple breakpoints limited only by the size of the On-Chip RAM. To debug with breakpoints in ROM you need to purchase the E10A-USB on-chip debugger at additional cost.

10.5.Code located in RAM

Double clicking in the breakpoint column in the HEW code window sets the breakpoint. Breakpoints will remain unless they are double clicked to remove them. (See the Tutorial Manual for more information on debugging with the HEW environment.)

10.6.HMon Code Size

HMON is built along with the user's code. Certain elements of the HMON code must remain at a fixed location in memory. The following table details the HMON components and their size and location in memory. For more information, refer to the map file when building code.

Section	Description	Start	Size
		Location	(H′bytes)
RESET_VECTOR	HMON Reset Vector (Vector 0)	H' 0000 0000	0x0004
	Required for Start-up of HMON		
SCI_VECTORS	HMON Serial Port Vectors (Vector 160, 161, 162, 163)	H'0000 0280	0x000C
PHMON	HMON Code	H'0000 3000	0x278C
CHMON	HMON Constant Data	H'0000 5730	0x0136
BHMON	HMON Un-initialised data	Variable	0x021F
UGenU	FDT Kernel.	H'0000 1000	0xEA8
	This is at a fixed location and must not be moved. Should the		
	kernel need to be moved it must be re-compiled.		
CUser_Vectors Pointer used by HMON to point to the start of user co		H'0000 0800	0x0004

10.7.Memory Map

The memory map shown in this section visually describes the locations of program code sections related to HMON, the FDT kernels and the supporting code within the ROM/RAM memory areas of the microcontroller.



10.8.Baud Rate Setting

HMON is initially set to connect at 250000Baud. The value set in the baud rate register for the microcontroller must be altered if the user wishes to change either the serial communication baud rate of the serial port or the operating frequency of the microcontroller. This value is defined in the hmonserialconfiguser.h file, as SCI_CFG_BRR (see the Serial Port section for baud rate register setting values). The project must be re-built and the resulting code downloaded to the microcontroller once the BRR value is changed. Please refer to the HMON User Manual for further information.

10.9.Interrupt mask sections

HMON has an interrupt priority of 6. The serial port has an interrupt priority of 7. Modules using interrupts should be set to lower than this value (6 or below), so that serial communications and debugging capability is maintained.



Chapter 11. Component Placement

Chapter 12. Additional Information

For details on how to use High-performance Embedded Workshop (HEW), refer to the HEW manual available on the CD or installed in the Manual Navigator.

For information about the H8SX/1582 series microcontrollers refer to the H8SX/1582 Series Hardware Manual

For information about the H8SX/1582 assembly language, refer to the H8 Series Programming Manual

Further information available for this product can be found on the Renesas website at:

http://www.renesas.com/rsk

General information on Renesas Microcontrollers can be found on the following website.

Global: <u>http://www.renesas.com/</u>

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