

V850E2/Px4 Application Board

User's Manual: Hardware

RENESAS MCU
V850 P Series

AB-050-PX4 Rev.: 1.0

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1. Introduction

The AB-050-Px4 is designed as a simple and easy to use Starter Board to support users with the first steps when starting with the V850E2/Px4.

The Starter Board is prepared to hold a V850E2/Px4 device (uPD70350x),

With the Nexus Debug interface and the Flash Programming interface for the Renesas PG-FP5 Flash Programmer the standard Renesas programming interfaces are directly available.

To enable further application development the board features drivers for 2 high speed CAN interfaces, 3 RS-232 interfaces, 3 LIN bus interfaces and 2 FlexRay interfaces.

With on-board voltage regulator and reset generator a simple external DC power supply is sufficient to operate the board.

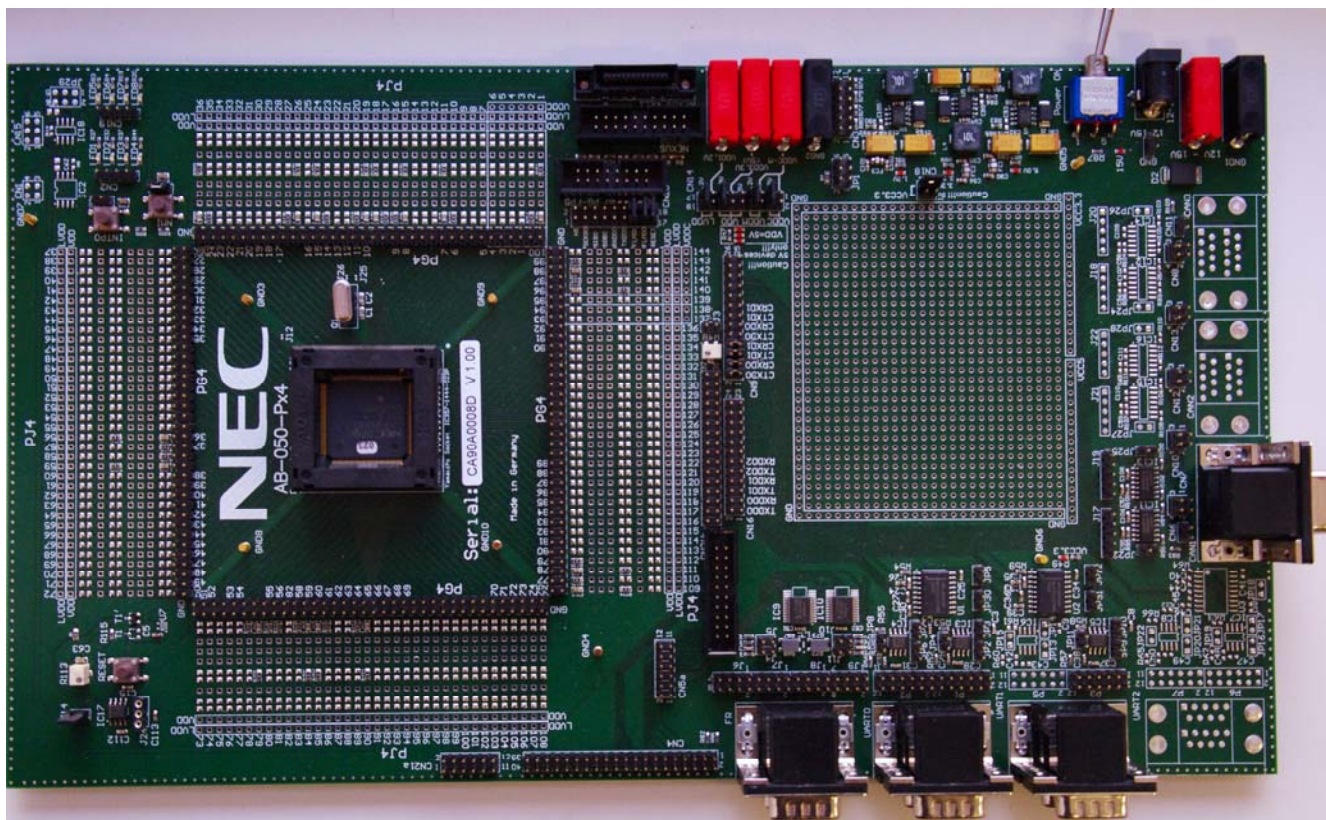


Figure 1. AB-050-Px4

2. Board description

2.1 Overview

Basically the board is divided into two areas, an 'Electrical Area' and a 'Functional Area'.

In Figure 2 the Electrical Area is marked yellow and the Functional Area is marked blue.

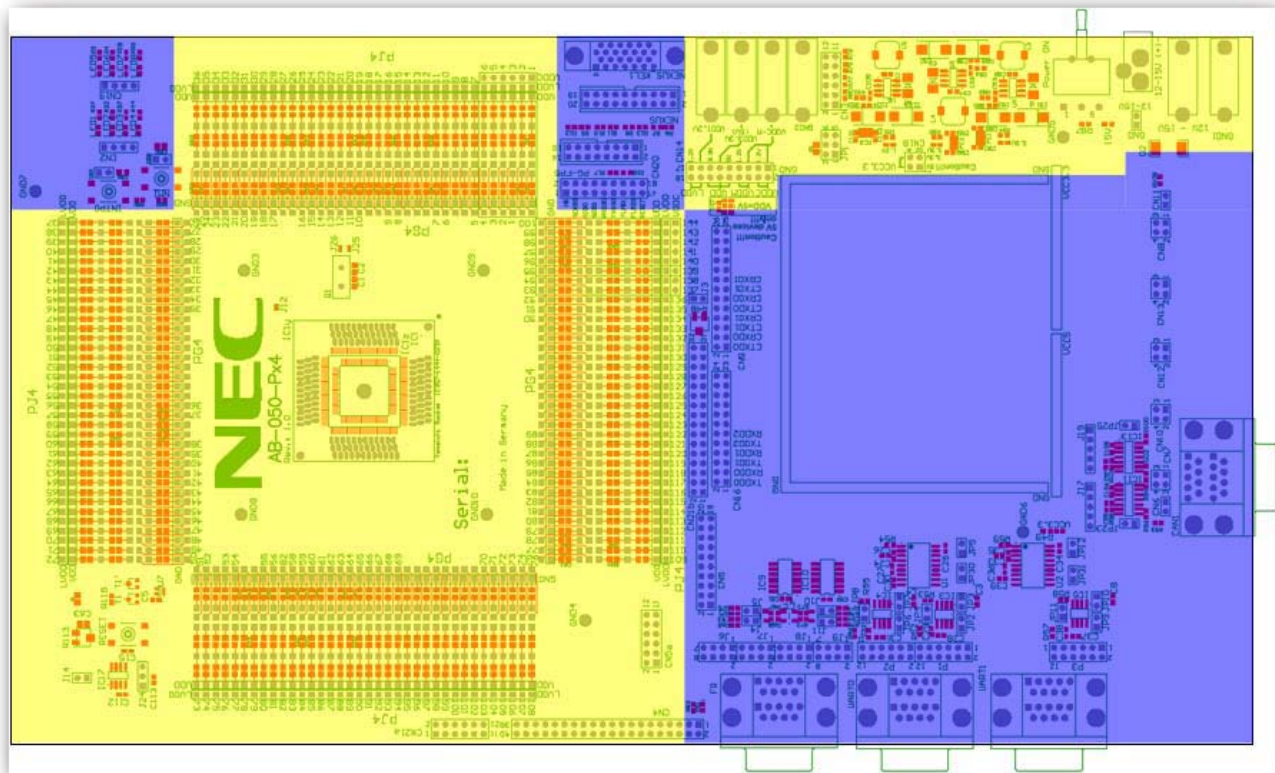


Figure 2. Board overview

2.1.1 Electrical Area

The yellow marked Electrical Area comprised the power supply, the reset circuit and the device socket with a surrounding Pin Patch Area. The core voltage supply is divided into a master and a checker domain, which is mandatory to fulfill the safety concept of the Px4 redundant core architecture.

In the centre of the Electrical Area the device socket is soldered either on a 100 pin or a 144 pin SMD pad field. On each side of the package/socket a "Pin Patch Area" is located.

In this patch area access is given to:

- each pin of the device ^(Note)
- VSS (GND)
- LVDD (1.2V)
- VDD (3.3V)

Further more SMD and through-hole components can directly be soldered onto the Pin Patch Area to allow simple networks to be easily built up.

Note:

The Board supports the 144pin PJ4 and the 100pin PG4 packaging. Inside pin labeling is for PG4, outside pin labeling for PJ4.

2.1.2 Functional Area

The blue marked Functional Area holds the drivers for RS-232, LIN bus, CAN and FlexRay. Additionally other patch areas are available as well to directly assembled LEDs, PowerDrivers and connectors to the board. Additional 2 EEPROM devices are available.

Note:

For detailed information about the operation of the used RS-232, LIN bus, CAN and FlexRay drivers refer to the related datasheets of those devices.

2.1.3 Connecting both areas

The Electrical and Functional Areas are not connected to each other except by a common VSS plane. Nevertheless by use of Jumpers a signal connection between the Electrical Area and the Functional Area is possible.

The following signals are available on the related jumper fields:

Signal	Jumper
FlexRay	CN5+CN5a
UART - URTHn (n=0..2)	CN16
CAN - FCNn (n=0..1)	CN9

Table 1. Overview of functional signals

2.1.4 Minimal configuration for quick start

To run the device without the Functional Area the following minimal configuration has to be done.

- select with CN14 the used power supply and VDD voltage
- assemble an 8MHz or an 16MHz oscillator to Q1
- set the required jumper setting to CN20

2.2 Reset

The V850E2/Px4 can be reset by asserting RESETZ input pin.

2.2.1 RESETZ input

The RESETZ input of the V850E2/Px4 is controlled via a pull-up resistor and transistor to GND. With J14 the connection to this circuit can be established.

2.3 Connecting the Power Supply

There are two different ways to supply the board with power:

a) Switching power supply

By supplying 12-15V to the 12-15V power connector jacket or to the 12-15V banana jacket. This will supply the on board voltage regulators for VCC5, VCC3.3 and VCC1.2 as well as directly supply VCC15.

b) Linear power supply

Optional the device voltages VDDC, VDDM, VDD and LVDD can be supplied separately by supplying the required voltages carefully to the corresponding banana jackets VDDC/M, VDD3.3V and VDD1.2V.

Use CN14 to select the device voltage supply source:

Supply voltage	Supply Source	CN14
VDDC	Extern	1-2
VDDC	Regulator	3-4
VDDM	Extern	5-6
VDDM	Regulator	7-8
VDD	Regulator 5V	9-10
VDD	Extern	11-12
LVDD	Extern	15-16
LVDD	Regulator	17-18

Table 2. Power Supply

VDDC and VDDM are the separated core voltage. VDDM supplies the Master Core and VDDC the Checker Core.

The board supports a voltage supply of 5V VDD. If the device should run with 5V, the voltage of the Functional Area and the Electrical Area has to be changed separately.

- With CN18 the voltage for the components of the Functional Area can be set to 5V.
- To switch the voltage of the device to 5V pin 9-10 of CN14 has to be connected.

Caution: Applying a voltage to the device outside the specified device operating voltage range may damage the device!

2.4 Nexus connection

The Nexus debug cable from a Renesas Debug Tool (e.g. MiniCube) can be connected to the Nexus Connector on the board.

KEL connector (Nexus_KEL1) is not supported by the AB-050-Px4 evaluation board.

The following jumpers must be closed in order to physically connect some of the Nexus signals from the Nexus Connector to the corresponding pins of the V850E2/Px4 device:

Jumper	Pin number
CN20	17-18
CN20	15-16

Table 3. Nexus

2.5 PG-FP5 connection

The programming cable of the PG-FP5 Flash programmer can be connected to 'PG-FP5' Connector.

To program the device via the CSI interface the following jumpers must be closed:

Connector	Pin number
CN20	3-4
CN20	5-6
CN20	7-8
CN20	13-14
CN20	15-16
CN20	17-18

Table 4. FP5 (CSI) Jumpers

To program the device via the UART interface the following jumpers must be closed:

Connector	Pin number
CN20	1-2
CN20	9-10
CN20	11-12
CN20	13-14
CN20	15-16
CN20	17-18

Table 5. FP5 (UART) Jumpers

Note:

For Flash programming, using the PG-FP5 device, power must be supplied by the AB-050-Px4. Please make sure to switch of power monitoring in PG-FP5 setup.

For Flash programming, using the PG-FP5, clock supply is done by the AB-050-Px4. Please make sure to enter the right crystal value in PG-FP5 setup.

2.6 RS-232 / LIN

2.6.1 RS-232 Transmission

V_{BAT} of the LIN bus driver is direct connected to the 12- 15V power supply jacket and the corresponding banana jackets. If the 12- 15V power supply is not used as power supply, a voltage in the range of 5V to 12V must be supplied to the jackets. For the exact specification refer to the Datasheet of the LIN Drivers.

Close the following jumpers on CN16 to physically connect the URTH signals from the Electrical Area to the Functional Area.

Signal		CN16
URTH0	TXD0	1-2
	RXD0	3-4
URTH1	TXD1	5-6
	RXD1	7-8
URTH2	TXD2	9-10
	RXD2	11-12

Table 6. URTHn signal jumpers

To connect the RS-232 bus driver signals to the RS-232 / LIN bus connectors close the following jumpers:

Signal		Connector	Pin #
URTH0	TXD0	P1	1-2
	RXD0		3-4
	GND		5-6
URTH1	TXD1	P2	1-2
	RXD1		3-4
	GND		5-6
URTH2	TXD2	P3	1-2
	RXD2		3-4
	GND		5-6

Table 7. RS-232 signal jumpers

To enable RS-232 transmission the disable Jumper must be removed from the corresponding RS232 transceiver. In addition the corresponding LIN-Transceiver must be send into SLEEP-Mode, otherwise it will disturb the transmission by limiting the level on RXD-Signal to 1,5V max. In most cases this high-level of 1,5V will not be recognized by the RS-232 controller.

To send LIN-Transceiver into SLEEP-Mode all 3 Jumpers must be removed from the LIN-Transceiver!

A falling edge must be generated on the NSLP-pin. This can either be done by setting and immediately removing the NSLP-Jumper after powering the board or by connecting both pins of the NSLP-Jumper via a 4,7nF capacity. By this the potential on the NSLP-Pin will follow the 5V power up and then it will be pulled down by the NSLP-Pin internal pull down resistor. This will generate the required falling edge.

2.6.2 LIN Transmission

To connect the LIN bus driver signals to the related RS-232/LIN bus connector close the following jumpers:

Signal		Connector	Pin #
LIN0	12V	P1	7-8
	LIN		9-10
	GND		11-12
		JP30	1-2
LIN1	12V	P2	7-8
	LIN		9-10
	GND		11-12
LIN2	12V	P3	7-8
	LIN		9-10
	GND		11-12
		JP31	1-2
LIN3	12V	P5	7-8
	LIN		9-10
	GND		11-12
LIN4	12V	P6	7-8
	LIN		9-10
	GND		11-12
LIN5	12V	P7	7-8
	LIN		9-10
	GND		11-12

Table 8. LIN bus signal jumpers

To enable the LIN drivers (IC3, IC4, IC5, IC6, IC7, IC8) the NSLP pin of the drivers must be pulled high. To do so a Jumper is available to connect the pin to VDD.

LIN channel	NLSP Jumper
0	JP3
1	JP7
2	JP10
3	JP14
4	JP17
5	JP21

Table 9. LIN NLSP Pin

At same time the RS232 Transceiver RX Pin must be disabled for the LIN-enabled channel. This must be done by the Disable Jumper connected to the EN-Pin of RS232 Transceiver.

LIN channel	RS232 Jumper
0	JP5
1	JP5
2	JP12
3	JP12
4	JP18
5	JP18

Table 10. LIN RS232 Jumper

Note: The Disable Jumper will disable 2 channels at same time!

The RxD pin of the LIN driver (pin #1) is an open drain output. The necessary pull-up resistor in order to interface to the Px4 device is not assembled on the board. To enable operation of the RxD signal user has either

- To connect an appropriate pull up resistor to the related RxD input pin of the LIN channel,

Or

- To enable the internal Pull-Up resistors available in the Px4 devices for each LIN input pin.

For additional information on the LIN driver refer to its User's Manual / Datasheet.

2.7 CAN

Power is permanently supplied to the CAN drivers by VCC5 and VCC3.3 and VCC15. These power lines are decoupled from Px4 power supply areas VDDC, VDDM, VDD, LVDD.

Close the following jumpers to physically connect the devices CAN signals to the CAN interface drivers located on the Functional Area of the board:

Signal		CN9
FCN0	CTXD0	1-2
	CRXD0	3-4
FCN1	CTXD1	5-6
	CRXD1	7-8
FCN2	CTXD2	9-10
	CRXD2	11-12
FCN3	CTXD3	13-14
	CRXD3	15-16
FCN4	CTXD4	17-18
	CRXD4	19-20
FCN5	CTXD5	21-22
	CRXD51	23-24
FCN6		25-26
	CRXD6	27-28 ^{Note}

Table 11. FCNn signal jumpers

Note: CAN6 of V850E2/Px4 is for diagnosis purpose and has only receive functionality. The physical interface on the Px4-Board is shared with the one for CAN5. Please make sure to jumper only one of them.

2.8 FlexRay

Power is permanently supplied to the FlexRay drivers by VCC5 and VCC3.3 and VCC15. These power lines are decoupled from Px4 power supply areas VDDC, VDDM, VDD, LVDD.

Close the following jumpers to physically connect the devices FlexRay signals to the FlexRay interface drivers located on the Functional Area of the board:

Signal		CN5a
FlexRay	FTXDA	1-2
	FRXDA	3-4
	FTXENA	5-6
	FTXDB	7-8
	FRXDB	9-10
	FTXENB	11-12

Table 12. FlexRay signal jumpers

Note: To control the operating mode of FlexRay interface drivers, the following jumpers have to be closed:

Signal	CN5
FR_EN1	1-2
FR_EN2	3-4
FR_STBN1	5-6
FR_STBN2	7-8
FR_WAKE1	9-10
FR_WAKE2	11-12
FR_RXEN1	13-14
FR_RXEN2	15-16
FR_ERRN1	17-18
FR_ERRN2	19-20

Table 13. FlexRay control jumpers

To connect the FlexRay bus driver signals to the related FlexRay bus connector close the following jumpers according to your requirements (refer to the AB-050-PJ4-Schematics for details):

Signal		Connector	Pin #
FlexRay	CH0_A	J6	x-y
	CH0_B	J7	x-y
	CH1_A	J8	x-y
	CH1_B	J9	x-y

Table 14. FlexRay bus jumpers

To terminate the FlexRay bus close the following jumpers:

Signal		Connector	Pin #
FlexRay	CH0_A	J4	1-2
	CH0_B	J5	1-2
	CH1_A	J10	1-2
	CH1_B	J11	1-2

Table 15. FlexRay bus termination jumpers

3. FlexRay / UART / LIN / CAN DSUB connectors

To physically connect the Starter Board to other UART / LIN / CAN devices DSUB type connectors are available.

3.1 UART / LIN connectors

To interface the AB-050-Px4 board to external to UART / LIN devices a 9 pin male D-SUB connector is supplied for each of the six available UART / LIN interfaces.

The signal layout of the UART/LIN DSUB connector can be seen in Table 16.

Male D-SUB, 9pin	Function
1	n/c
6	n/c
2	RS-232 TxD
7	LIN
3	RS-232 RxD or GND
8	n/c
4	n/c
9	+12V
5	GND

Table 16. UART / LIN DSUB connectors

3.2 FlexRay connectors

To interface the AB-050-Px4 board to external to FlexRay devices a 9 pin male D-SUB connector is supplied for each of the two available FlexRay interfaces.

The signal layout of the FlexRay D-SUB connector can be seen in Table 17.

Male D-SUB, 9pin	Function
1	n/c
6	n/c
2	CH0_A or CH1_A
7	CH0_B or CH1_A
4	CH0_A or CH1_A
8	CH0_B or CH1_A
3	n/c
9	n/c
5	n/c

Table 17. FlexRay DSUB connectors

Figure 3 displays the assignment of each DSUB connector to its related peripheral:

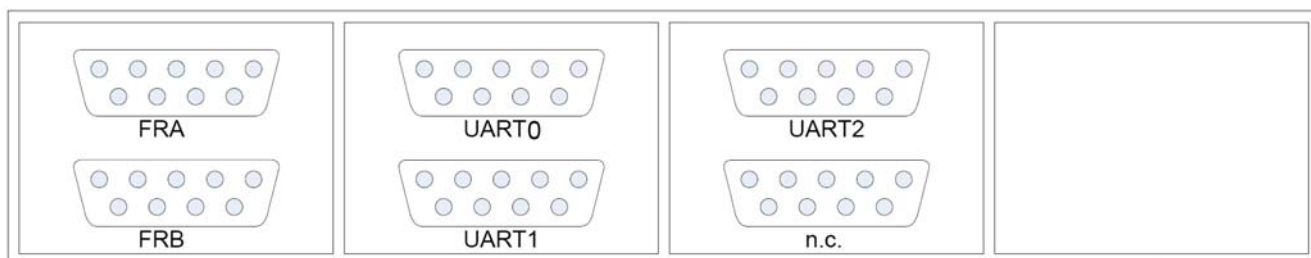


Figure 3. FlexRay / UART / LIN DSUB connectors

3.3 CAN connectors

To interface the AB-050-Px4 board to external CAN devices a 9 pin female D-SUB connector is supplied for each of the six available CAN interfaces.

The pin functions of the CAN DSUB connectors can be seen in Table 18.

Male D-SUB, 9pin	Function
1	n/c
6	GND
2	CANL
7	CANH
3	GND (if jumpered)
8	n/c
4	n/c
9	n/c
5	n/c

Table 18. CAN DSUB connectors

Figure 4 displays the assignment of each DSUB connector to its related peripheral:



Figure 4. CAN DSUB connectors

3.4 Pin connection

The pin connection, which is described below, is already done on the board.

3.4.1 Power supply pins

Connect the devices power supply pins to the related power lines using the available SMD pads in the Pin Patch Areas.

Refer to the V850E2/Px4 User's Manual and Electrical Target Specification for the location of the VDD and VSS pins on the different devices.

Connect the VDD and VSS pins in the Pin Patch Areas like this:

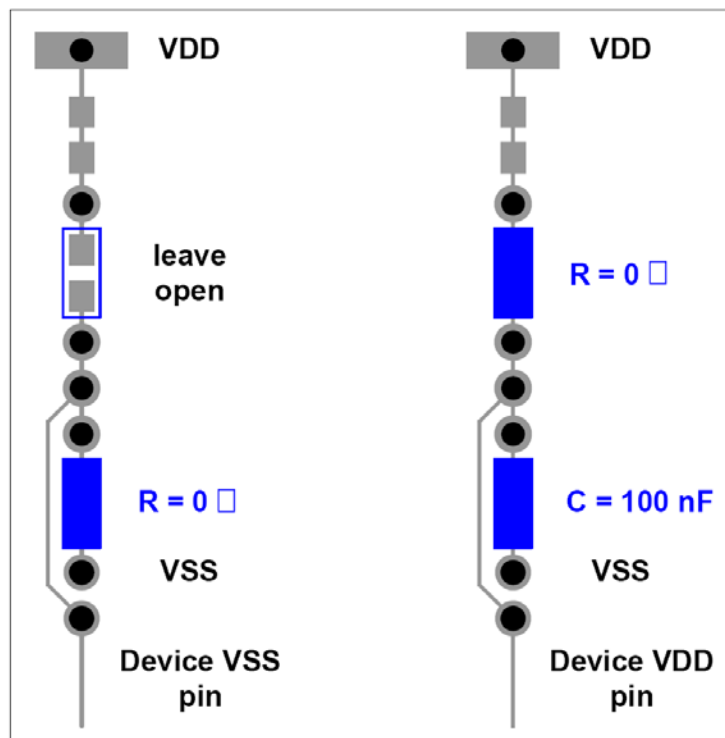


Figure 5. Device power supply

To connect the devices VSS pins to the VSS lane of the board place a 0 Ohm resistor on the SMD1 pad.

To connect the devices VDD pins to the VDD lane of the board place a 0 Ohm resistor on the SMD2 pad and place a 100 nF buffering capacitor on the SMD1 pad.

3.4.2 REGC pin

A buffering capacitor between the devices REGC pin(s) and VSS should be placed. Assemble the capacitor to the SMD1 pad field.

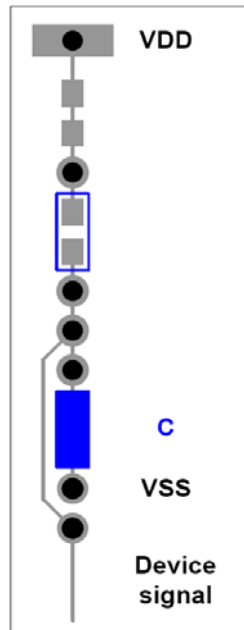


Figure 6. REGC pin components

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the REGC pin on the different devices.

3.4.3 X1, X2 pins

The external crystal can be connected to the socket Q1. Alternatively An external oscillator can be connected to the X1 and X2 pins of the device. Connect the oscillator between the X1 and X2 pins and place a small capacitor on the SMD1 areas of those pins. For size of the capacitor refer to the oscillator manufacturer specification / recommendation.

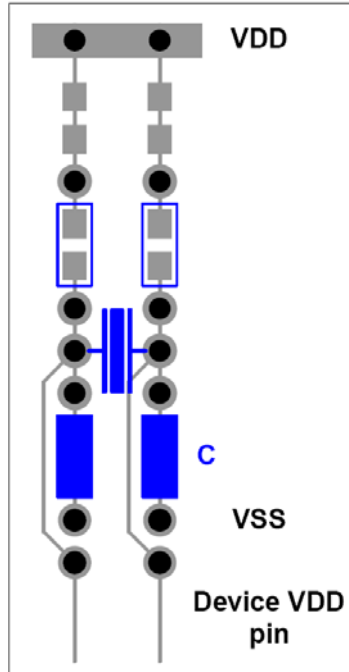


Figure 7. X1, X2 pin components

In this case you have to connect the J25 and J26 with solder.

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the X1 and X2 pins on the different devices.

3.4.4 XT1, FLMD0

A pull-down resistor should be connected to input pin FLMD0.

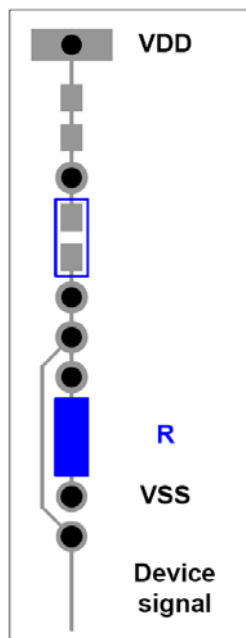


Figure 8. Pins with Pull-Down

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the FLMD0 pins on the different devices.

3.5 Functional pin connection

As the routing of the functional signals (Reset, UARTH_n, CAN_n, NWIRE and FP5) between the device SMD pad area and the Jumpers connecting the Electrical Area and Functional Area is based on the Px4 device, the routing of those signals for other Px4 devices must be place manually.

To do so, connect a wire between the device pin (e.g. from one of the through holes in the Pin Patch areas) and the functional side of the related signal jumper.

Caution: Do not close the related Jumpers of any of the newly routed signals as this can lead to a direct connection between different device pins. Be aware that no further disconnection by the use of jumpers between the Electrical Area and Functional Area is possible after wiring the signals for other than Px4 devices.

3.5.1 Jumper and connector overview

The location of all jumpers located on the board can be seen in the Figure 9.

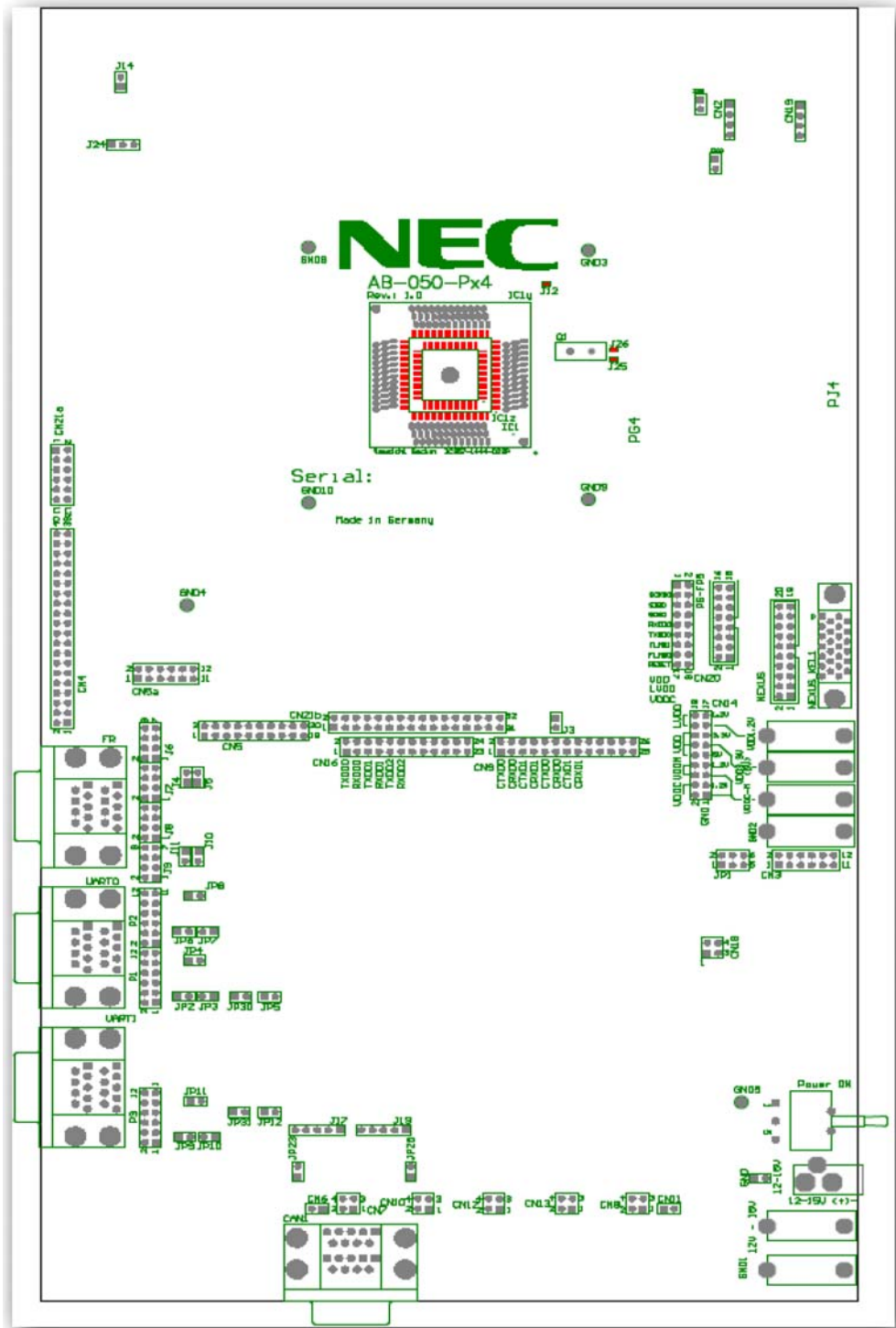


Figure 9. Jumper and connector location

4. Revision History

Version	Chapter	Comment
0.1-0.4		Initial releases incl. bug fixes
0.5-0.6		Modification due to merger of Renesas Technologies and NEC Electronics.
0.7		Socket board schematics attached.
0.8		Included information: KEL connector not supported.
0.09		Modified document template and document numbering format.

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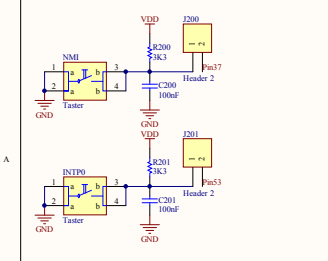
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Colophon 1.0

V850E2/Px4 Application Board

Device Footprint

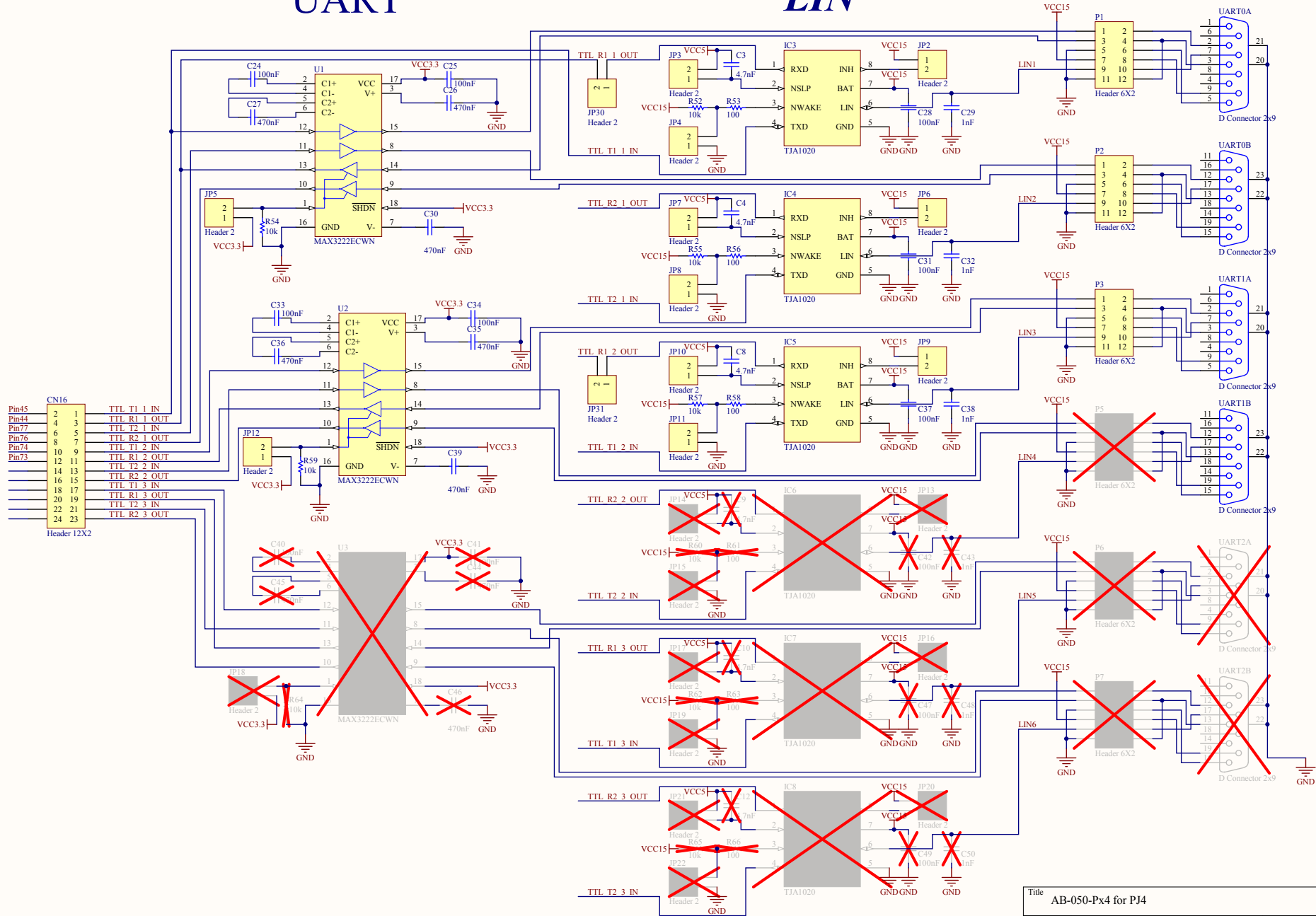
A



IC1A	IC1B	IC1V
<p>0129 Pin129 P5_1 UCSH1CS2URTHXKINTP1CSBHCS2CSHHRY4RTHX2ADCATRGINTP4CSHHRYO</p> <p>0130 Pin130 P5_2 CSBH1CS1URTHXKINTP2CSBHCS1URTHXSCADACATRGINTP4CSHHRYO</p> <p>0131 Pin131 P5_3 CSBH1CS2URTHXKINTP3CSBHCS2ADCATRGINTP4CSHHRYO</p> <p>0132 Pin132 P5_4 CSBH1CS3CSBHCS3CSHHRY4RTHX2</p> <p>0133 Pin133 P5_5 STALADRTXALADRTXCSHHRYO</p> <p>0134 Pin134 P5_6 CSBH1CS2URTHXKINTP1</p> <p>0135 Pin135 P5_7 CSBH1CS2URTHXKINTX</p> <p>0136 Pin136 P5_8 CSBH1CS2URTHXKINTX</p> <p>0137 Pin137 P5_9 CSBH1CS2URTHXKINTX</p> <p>0138 Pin138 P5_10 CSBH1CS2URTHXKINTX</p> <p>0139 Pin139 P5_11 CSBH1CS2URTHXKINTX</p>	<p>047 Pin47 P6_0 CSKGS2TSGI06TALIA0012TSG200</p> <p>048 Pin48 P6_1 UCSKGS2URTHXKINTXCSHHRYO</p> <p>049 Pin49 P6_2 UCSKGS2URTHXKINTXCSHHRYO</p> <p>050 Pin50 P6_3 UCSKGS2URTHXKINTXCSHHRYO</p> <p>051 Pin51 P6_4 UCSKGS2URTHXKINTXCSHHRYO</p> <p>052 Pin52 P6_5 UCSKGS2URTHXKINTXCSHHRYO</p> <p>053 Pin53 P6_6 UCSKGS2URTHXKINTXCSHHRYO</p> <p>054 Pin54 P6_7 UCSKGS2URTHXKINTXCSHHRYO</p> <p>055 Pin55 P6_8 UCSKGS2URTHXKINTXCSHHRYO</p>	<p>32 Pin32 P1_0 DCUTD0/P0_0</p> <p>33 Pin33 P1_1 DCUTD0/P0_1</p> <p>34 Pin34 P1_2 DCUTD0/P0_2</p> <p>35 Pin35 P1_3 DCUTD0/P0_3</p> <p>36 Pin36 P1_4 DCUTD0/P0_4</p> <p>37 Pin37 P1_5 DCUTD0/P0_5</p> <p>38 Pin38 P1_6 DCUTD0/P0_6</p> <p>39 Pin39 P1_7 DCUTD0/P0_7</p> <p>40 Pin40 P1_8 DCUTD0/P0_8</p> <p>41 Pin41 P1_9 DCUTD0/P0_9</p> <p>42 Pin42 P1_10 DCUTD0/P0_10</p> <p>43 Pin43 P1_11 DCUTD0/P0_11</p> <p>44 Pin44 P1_12 DCUTD0/P0_12</p> <p>45 Pin45 P1_13 DCUTD0/P0_13</p> <p>46 Pin46 P1_14 DCUTD0/P0_14</p> <p>47 Pin47 P1_15 DCUTD0/P0_15</p> <p>48 Pin48 P1_16 DCUTD0/P0_16</p> <p>49 Pin49 P1_17 DCUTD0/P0_17</p> <p>50 Pin50 P1_18 DCUTD0/P0_18</p> <p>51 Pin51 P1_19 DCUTD0/P0_19</p> <p>52 Pin52 P1_20 DCUTD0/P0_20</p> <p>53 Pin53 P1_21 DCUTD0/P0_21</p> <p>54 Pin54 P1_22 DCUTD0/P0_22</p> <p>55 Pin55 P1_23 DCUTD0/P0_23</p> <p>56 Pin56 P1_24 DCUTD0/P0_24</p> <p>57 Pin57 P1_25 DCUTD0/P0_25</p> <p>58 Pin58 P1_26 DCUTD0/P0_26</p> <p>59 Pin59 P1_27 DCUTD0/P0_27</p> <p>60 Pin60 P1_28 DCUTD0/P0_28</p> <p>61 Pin61 P1_29 DCUTD0/P0_29</p> <p>62 Pin62 P1_30 DCUTD0/P0_30</p> <p>63 Pin63 P1_31 DCUTD0/P0_31</p> <p>64 Pin64 P1_32 DCUTD0/P0_32</p> <p>65 Pin65 P1_33 DCUTD0/P0_33</p> <p>66 Pin66 P1_34 DCUTD0/P0_34</p> <p>67 Pin67 P1_35 DCUTD0/P0_35</p> <p>68 Pin68 P1_36 DCUTD0/P0_36</p> <p>69 Pin69 P1_37 DCUTD0/P0_37</p> <p>70 Pin70 P1_38 DCUTD0/P0_38</p> <p>71 Pin71 P1_39 DCUTD0/P0_39</p> <p>72 Pin72 P1_40 DCUTD0/P0_40</p> <p>73 Pin73 P1_41 DCUTD0/P0_41</p> <p>74 Pin74 P1_42 DCUTD0/P0_42</p> <p>75 Pin75 P1_43 DCUTD0/P0_43</p> <p>76 Pin76 P1_44 DCUTD0/P0_44</p> <p>77 Pin77 P1_45 DCUTD0/P0_45</p> <p>78 Pin78 P1_46 DCUTD0/P0_46</p> <p>79 Pin79 P1_47 DCUTD0/P0_47</p> <p>80 Pin80 P1_48 DCUTD0/P0_48</p> <p>81 Pin81 P1_49 DCUTD0/P0_49</p> <p>82 Pin82 P1_50 DCUTD0/P0_50</p> <p>83 Pin83 P1_51 DCUTD0/P0_51</p> <p>84 Pin84 P1_52 DCUTD0/P0_52</p> <p>85 Pin85 P1_53 DCUTD0/P0_53</p> <p>86 Pin86 P1_54 DCUTD0/P0_54</p> <p>87 Pin87 P1_55 DCUTD0/P0_55</p> <p>88 Pin88 P1_56 DCUTD0/P0_56</p> <p>89 Pin89 P1_57 DCUTD0/P0_57</p> <p>90 Pin90 P1_58 DCUTD0/P0_58</p> <p>91 Pin91 P1_59 DCUTD0/P0_59</p> <p>92 Pin92 P1_60 DCUTD0/P0_60</p> <p>93 Pin93 P1_61 DCUTD0/P0_61</p> <p>94 Pin94 P1_62 DCUTD0/P0_62</p> <p>95 Pin95 P1_63 DCUTD0/P0_63</p> <p>96 Pin96 P1_64 DCUTD0/P0_64</p> <p>97 Pin97 P1_65 DCUTD0/P0_65</p> <p>98 Pin98 P1_66 DCUTD0/P0_66</p> <p>99 Pin99 P1_67 DCUTD0/P0_67</p> <p>100 Pin100 P1_68 DCUTD0/P0_68</p> <p>101 Pin101 P1_69 DCUTD0/P0_69</p> <p>102 Pin102 P1_70 DCUTD0/P0_70</p> <p>103 Pin103 P1_71 DCUTD0/P0_71</p> <p>104 Pin104 P1_72 DCUTD0/P0_72</p> <p>105 Pin105 P1_73 DCUTD0/P0_73</p> <p>106 Pin106 P1_74 DCUTD0/P0_74</p> <p>107 Pin107 P1_75 DCUTD0/P0_75</p> <p>108 Pin108 P1_76 DCUTD0/P0_76</p> <p>109 Pin109 P1_77 DCUTD0/P0_77</p> <p>110 Pin110 P1_78 DCUTD0/P0_78</p> <p>111 Pin111 P1_79 DCUTD0/P0_79</p> <p>112 Pin112 P1_80 DCUTD0/P0_80</p> <p>113 Pin113 P1_81 DCUTD0/P0_81</p> <p>114 Pin114 P1_82 DCUTD0/P0_82</p> <p>115 Pin115 P1_83 DCUTD0/P0_83</p> <p>116 Pin116 P1_84 DCUTD0/P0_84</p> <p>117 Pin117 P1_85 DCUTD0/P0_85</p> <p>118 Pin118 P1_86 DCUTD0/P0_86</p> <p>119 Pin119 P1_87 DCUTD0/P0_87</p> <p>120 Pin120 P1_88 DCUTD0/P0_88</p> <p>121 Pin121 P1_89 DCUTD0/P0_89</p> <p>122 Pin122 P1_90 DCUTD0/P0_90</p> <p>123 Pin123 P1_91 DCUTD0/P0_91</p> <p>124 Pin124 P1_92 DCUTD0/P0_92</p> <p>125 Pin125 P1_93 DCUTD0/P0_93</p> <p>126 Pin126 P1_94 DCUTD0/P0_94</p> <p>127 Pin127 P1_95 DCUTD0/P0_95</p> <p>128 Pin128 P1_96 DCUTD0/P0_96</p> <p>129 Pin129 P1_97 DCUTD0/P0_97</p> <p>130 Pin130 P1_98 DCUTD0/P0_98</p> <p>131 Pin131 P1_99 DCUTD0/P0_99</p> <p>132 Pin132 P1_100 DCUTD0/P0_100</p> <p>133 Pin133 P1_101 DCUTD0/P0_101</p> <p>134 Pin134 P1_102 DCUTD0/P0_102</p> <p>135 Pin135 P1_103 DCUTD0/P0_103</p> <p>136 Pin136 P1_104 DCUTD0/P0_104</p> <p>137 Pin137 P1_105 DCUTD0/P0_105</p> <p>138 Pin138 P1_106 DCUTD0/P0_106</p> <p>139 Pin139 P1_107 DCUTD0/P0_107</p> <p>140 Pin140 P1_108 DCUTD0/P0_108</p> <p>141 Pin141 P1_109 DCUTD0/P0_109</p> <p>142 Pin142 P1_110 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DCUTD0/P0_212</p> <p>245 Pin245 P1_213 DCUTD0/P0_213</p> <p>246 Pin246 P1_214 DCUTD0/P0_214</p> <p>247 Pin247 P1_215 DCUTD0/P0_215</p> <p>248 Pin248 P1_216 DCUTD0/P0_216</p> <p>249 Pin249 P1_217 DCUTD0/P0_217</p> <p>250 Pin250 P1_218 DCUTD0/P0_218</p> <p>251 Pin251 P1_219 DCUTD0/P0_219</p> <p>252 Pin252 P1_220 DCUTD0/P0_220</p> <p>253 Pin253 P1_221 DCUTD0/P0_221</p> <p>254 Pin254 P1_222 DCUTD0/P0_222</p> <p>255 Pin255 P1_223 DCUTD0/P0_223</p> <p>256 Pin256 P1_224 DCUTD0/P0_224</p> <p>257 Pin257 P1_225 DCUTD0/P0_225</p> <p>258 Pin258 P1_226 DCUTD0/P0_226</p> <p>259 Pin259 P1_227 DCUTD0/P0_227</p> <p>260 Pin260 P1_228 DCUTD0/P0_228</p> <p>261 Pin261 P1_229 DCUTD0/P0_229</p> <p>262 Pin262 P1_230 DCUTD0/P0_230</p> <p>263 Pin263 P1_231 DCUTD0/P0_231</p> <p>264 Pin264 P1_232 DCUTD0/P0_232</p> <p>265 Pin265 P1_233 DCUTD0/P0_233</p> <p>266 Pin266 P1_234 DCUTD0/P0_234</p> <p>267 Pin267 P1_235 DCUTD0/P0_235</p> <p>268 Pin268 P1_236 DCUTD0/P0_236</p> <p>269 Pin269 P1_237 DCUTD0/P0_237</p> <p>270 Pin270 P1_238 DCUTD0/P0_238</p> <p>271 Pin271 P1_239 DCUTD0/P0_239</p> <p>272 Pin272 P1_240 DCUTD0/P0_240</p> <p>273 Pin273 P1_241 DCUTD0/P0_241</p> <p>274 Pin274 P1_242 DCUTD0/P0_242</p> <p>275 Pin275 P1_243 DCUTD0/P0_243</p> <p>276 Pin276 P1_244 DCUTD0/P0_244</p> <p>277 Pin277 P1_245 DCUTD0/P0_245</p> <p>278 Pin278 P1_246 DCUTD0/P0_246</p> <p>279 Pin279 P1_247 DCUTD0/P0_247</p> <p>280 Pin280 P1_248 DCUTD0/P0_248</p> <p>281 Pin281 P1_249 DCUTD0/P0_249</p> <p>282 Pin282 P1_250 DCUTD0/P0_250</p> <p>283 Pin283 P1_251 DCUTD0/P0_251</p> <p>284 Pin284 P1_252 DCUTD0/P0_252</p> <p>285 Pin285 P1_253 DCUTD0/P0_253</p> <p>286 Pin286 P1_254 DCUTD0/P0_254</p> <p>287 Pin287 P1_255 DCUTD0/P0_255</p> <p>288 Pin288 P1_256 DCUTD0/P0_256</p> <p>289 Pin289 P1_257 DCUTD0/P0_257</p> <p>290 Pin290 P1_258 DCUTD0/P0_258</p> <p>291 Pin291 P1_259 DCUTD0/P0_259</p> <p>292 Pin292 P1_260 DCUTD0/P0_260</p> <p>293 Pin293 P1_261 DCUTD0/P0_261</p> <p>294 Pin294 P1_262 DCUTD0/P0_262</p> <p>295 Pin295 P1_263 DCUTD0/P0_263</p> <p>296 Pin296 P1_264 DCUTD0/P0_264</p> <p>297 Pin297 P1_265 DCUTD0/P0_265</p> <p>298 Pin298 P1_266 DCUTD0/P0_266</p> <p>299 Pin299 P1_267 DCUTD0/P0_267</p> <p>300 Pin300 P1_268 DCUTD0/P0_268</p> <p>301 Pin301 P1_269 DCUTD0/P0_269</p> <p>302 Pin302 P1_270 DCUTD0/P0_270</p> <p>303 Pin303 P1_271 DCUTD0/P0_271</p> <p>304 Pin304 P1_272 DCUTD0/P0_272</p> <p>305 Pin305 P1_273 DCUTD0/P0_273</p> <p>306 Pin306 P1_274 DCUTD0/P0_274</p> <p>307 Pin307 P1_275 DCUTD0/P0_275</p> <p>308 Pin308 P1_276 DCUTD0/P0_276</p> <p>309 Pin309 P1_277 DCUTD0/P0_277</p> <p>310 Pin310 P1_278 DCUTD0/P0_278</p> <p>311 Pin311 P1_279 DCUTD0/P0_279</p> <p>312 Pin312 P1_280 DCUTD0/P0_280</p> <p>313 Pin313 P1_281 DCUTD0/P0_281</p> <p>314 Pin314 P1_282 DCUTD0/P0_282</p> <p>315 Pin315 P1_283 DCUTD0/P0_283</p> <p>316 Pin316 P1_284 DCUTD0/P0_284</p> <p>317 Pin317 P1_285 DCUTD0/P0_285</p> <p>318 Pin318 P1_286 DCUTD0/P0_286</p> <p>319 Pin319 P1_287 DCUTD0/P0_287</p> <p>320 Pin320 P1_288 DCUTD0/P0_288</p> <p>321 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DCUTD0/P0_314</p> <p>347 Pin347 P1_315 DCUTD0/P0_315</p> <p>348 Pin348 P1_316 DCUTD0/P0_316</p> <p>349 Pin349 P1_317 DCUTD0/P0_317</p> <p>350 Pin350 P1_318 DCUTD0/P0_318</p> <p>351 Pin351 P1_319 DCUTD0/P0_319</p> <p>352 Pin352 P1_320 DCUTD0/P0_320</p> <p>353 Pin353 P1_321 DCUTD0/P0_321</p> <p>354 Pin354 P1_322 DCUTD0/P0_322</p> <p>355 Pin355 P1_323 DCUTD0/P0_323</p> <p>356 Pin356 P1_324 DCUTD0/P0_324</p> <p>357 Pin357 P1_325 DCUTD0/P0_325</p> <p>358 Pin358 P1_326 DCUTD0/P0_326</p> <p>359 Pin359 P1_327 DCUTD0/P0_327</p> <p>360 Pin360 P1_328 DCUTD0/P0_328</p> <p>361 Pin361 P1_329 DCUTD0/P0_329</p> <p>362 Pin362 P1_330 DCUTD0/P0_330</p> <p>363 Pin363 P1_331 DCUTD0/P0_331</p> <p>364 Pin364 P1_332 DCUTD0/P0_332</p> <p>365 Pin365 P1_333 DCUTD0/P0_333</p> <p>366 Pin366 P1_334 DCUTD0/P0_334</p> <p>367 Pin367 P1_335 DCUTD0/P0_335</p> <p>368 Pin368 P1_336 DCUTD0/P0_336</p> <p>369 Pin369 P1_337 DCUTD0/P0_337</p> <p>370 Pin370 P1_338 DCUTD0/P0_338</p> <p>371 Pin371 P1_339 DCUTD0/P0_339</p> <p>372 Pin372 P1_340 DCUTD0/P0_340</p> <p>373 Pin373 P1_341 DCUTD0/P0_341</p> <p>374 Pin374 P1_342 DCUTD0/P0_342</p> <p>375 Pin375 P1_343 DCUTD0/P0_343</p> <p>376 Pin376 P1_344 DCUTD0/P0_344</p> <p>377 Pin377 P1_345 DCUTD0/P0_345</p> <p>378 Pin378 P1_346 DCUTD0/P0_346</p> <p>379 Pin379 P1_347 DCUTD0/P0_347</p> <p>380 Pin380 P1_348 DCUTD0/P0_348</p> <p>381 Pin381 P1_349 DCUTD0/P0_349</p> <p>382 Pin382 P1_350 DCUTD0/P0_350</p> <p>383 Pin383 P1_351 DCUTD0/P0_351</p> <p>384 Pin384 P1_352 DCUTD0/P0_352</p> <p>385 Pin385 P1_353 DCUTD0/P0_353</p> <p>386 Pin386 P1_354 DCUTD0/P0_354</p> <p>387 Pin387 P1_355 DCUTD0/P0_355</p> <p>388 Pin388 P1_356 DCUTD0/P0_356</p> <p>389 Pin389 P1_357 DCUTD0/P0_357</p> <p>390 Pin390 P1_358 DCUTD0/P0_358</p> <p>391 Pin391 P1_359 DCUTD0/P0_359</p> <p>392 Pin392 P1_360 DCUTD0/P0_360</p> <p>393 Pin393 P1_361 DCUTD0/P0_361</p> <p>394 Pin394 P1_362 DCUTD0/P0_362</p> <p>395 Pin395 P1_363 DCUTD0/P0_363</p> <p>396 Pin396 P1_364 DCUTD0/P0_364</p> <p>397 Pin397 P1_365 DCUTD0/P0_365</p> <p>398 Pin398 P1_366 DCUTD0/P0_366</p> <p>399 Pin399 P1_367 DCUTD0/P0_367</p> <p>400 Pin400 P1_368 DCUTD0/P0_368</p> <p>401 Pin401 P1_369 DCUTD0/P0_369</p> <p>402 Pin402 P1_370 DCUTD0/P0_370</p> <p>403 Pin403 P1_371 DCUTD0/P0_371</p> <p>404 Pin404 P1_372 DCUTD0/P0_372</p> <p>405 Pin405 P1_373 DCUTD0/P0_373</p> <p>406 Pin406 P1_374 DCUTD0/P0_374</p> <p>407 Pin407 P1_375 DCUTD0/P0_375</p> <p>408 Pin408 P1_376 DCUTD0/P0_376</p> <p>409 Pin409 P1_377 DCUTD0/P0_377</p> <p>410 Pin410 P1_378 DCUTD0/P0_378</p> <p>411 Pin411 P1_379 DCUTD0/P0_379</p> <p>412 Pin412 P1_380 DCUTD0/P0_380</p> <p>413 Pin413 P1_381 DCUTD0/P0_381</p> <p>414 Pin414 P1_382 DCUTD0/P0_382</p> <p>415 Pin415 P1_383 DCUTD0/P0_383</p> <p>416 Pin416 P1_384 DCUTD0/P0_384</p> <p>417 Pin417 P1_385 DCUTD0/P0_385</p> <p>418 Pin418 P1_386 DCUTD0/P0_386</p> <p>419 Pin419 P1_387 DCUTD0/P0_387</p> <p>420 Pin420 P1_388 DCUTD0/P0_388</p> <p>421 Pin421 P1_389 DCUTD0/P0_389</p> <p>422 Pin422 P1_390 DCUTD0/P0_390</p> <p>423 Pin423 P1_391 DCUTD0/P0_391</p> <p>424 Pin424 P1_392 DCUTD0/P0_392</p> <p>425 Pin425 P1_393 DCUTD0/P0_393</p> <p>426 Pin426 P1_394 DCUTD0/P0_394</p> <p>427 Pin427 P1_395 DCUTD0/P0_395</p> <p>428 Pin428 P1_396 DCUTD0/P0_396</p> <p>429 Pin429 P1_397 DCUTD0/P0_397</p> <p>430 Pin430 P1_398 DCUTD0/P0_398</p> <p>431 Pin431 P1_399 DCUTD0/P0_399</p> <p>432 Pin432 P1_400 DCUTD0/P0_400</p> <p>433 Pin433 P1_401 DCUTD0/P0_401</p> <p>434 Pin434 P1_402 DCUTD0/P0_402</p> <p>435 Pin435 P1_403 DCUTD0/P0_403</p> <p>436 Pin436 P1_404 DCUTD0/P0_404</p> <p>437 Pin437 P1_405 DCUTD0/P0_405</p> <p>438 Pin438 P1_406 DCUTD0/P0_406</p> <p>439 Pin439 P1_40</p>

UART

LIN



Header 12X2

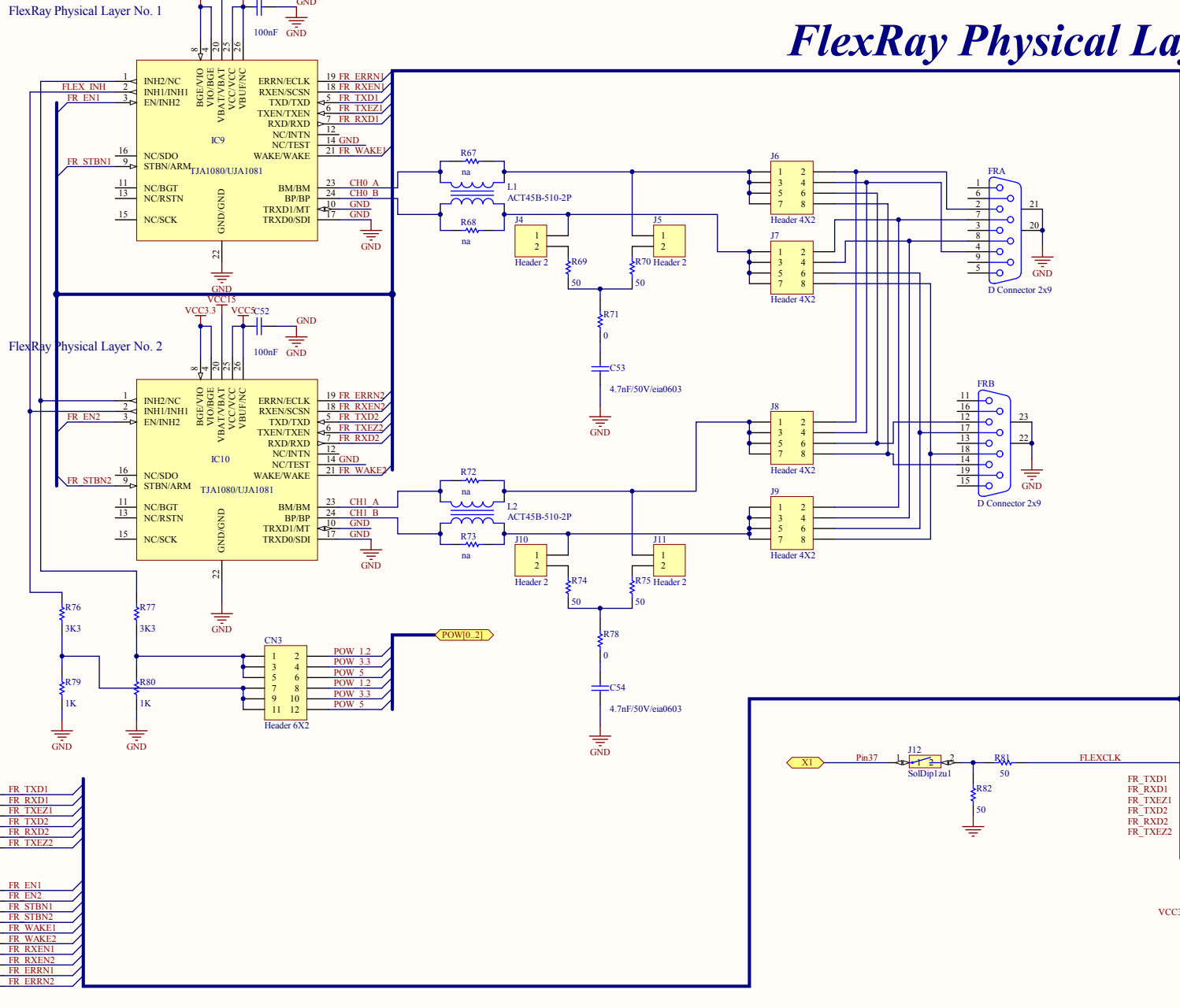
Pin	Signal
Pin45	TTL T1 1 IN
Pin44	TTL R1 1 OUT
Pin43	TTL T2 1 IN
Pin77	TTL R2 1 OUT
Pin76	TTL T1 2 IN
Pin74	TTL R2 1 OUT
Pin73	TTL T1 2 IN
Pin72	TTL R1 2 OUT
Pin71	TTL T2 2 IN
Pin70	TTL R2 2 OUT
Pin69	TTL T1 3 IN
Pin68	TTL R1 3 OUT
Pin67	TTL T2 3 IN
Pin66	TTL R2 3 OUT

Title AB-050-Px4 for PJ4		
Size A3	Number EASE-UM-0069-	Revision 0.6
Date: 29.10.2009	Sheet 2 of 5	
File: C:\Data\12 SCHDOC	Drawn By: NEC Electronics	

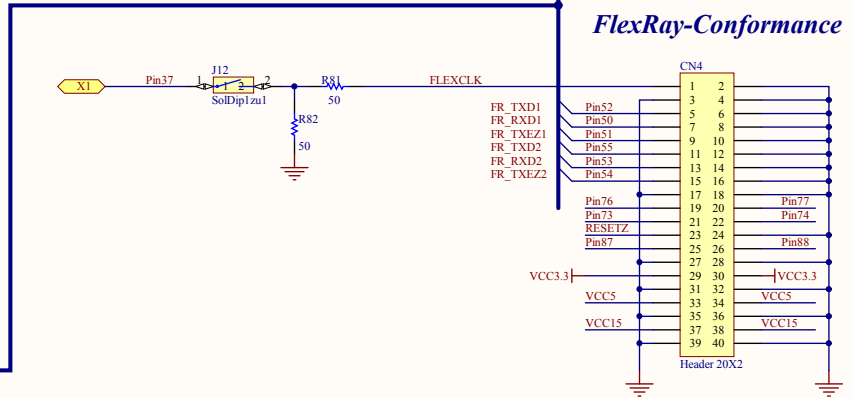
FlexRay Physical Layer

FlexRay Physical Layer No. 1

FlexRay Physical Layer No. 2



FlexRay-Conformance



CN5a

Pin52	2	1	FR_TXD1
Pin50	4	3	FR_RXD1
Pin51	6	5	FR_TXE2
Pin55	8	7	FR_RXE2
Pin53	10	9	FR_TXE2
Pin54	12	11	FR_TXE2

Header 6X2

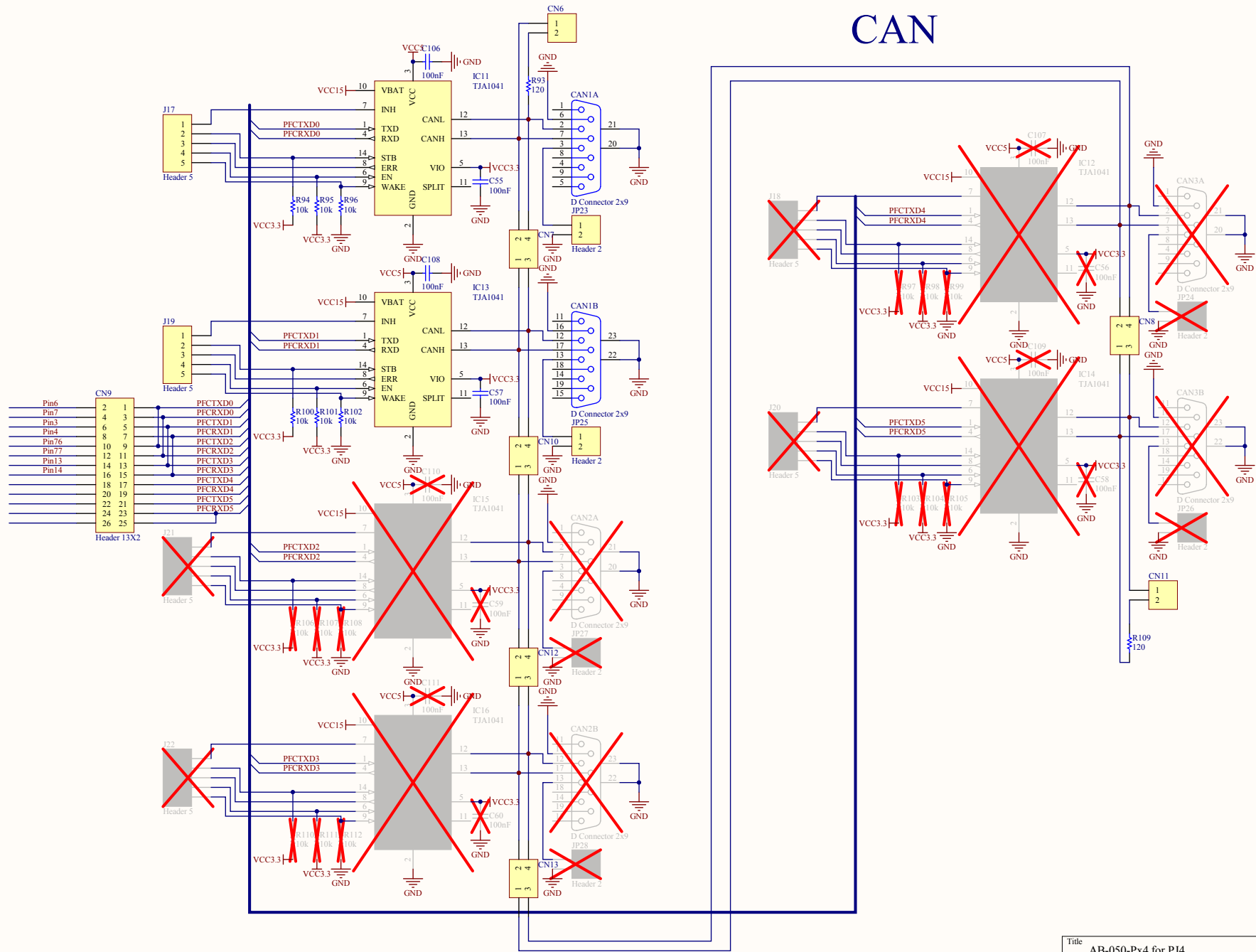
CN5

Pin95	2	1	FR_EN1
Pin96	4	3	FR_EN2
Pin97	6	5	FR_STBN1
Pin98	8	7	FR_STBN2
Pin99	10	9	FR_WAKE1
Pin100	12	11	FR_WAKE2
Pin101	14	13	FR_RXEN1
Pin102	16	15	FR_RXEN2
Pin66	18	17	FR_ERRN1
Pin67	20	19	FR_ERRN2

Header 10X2

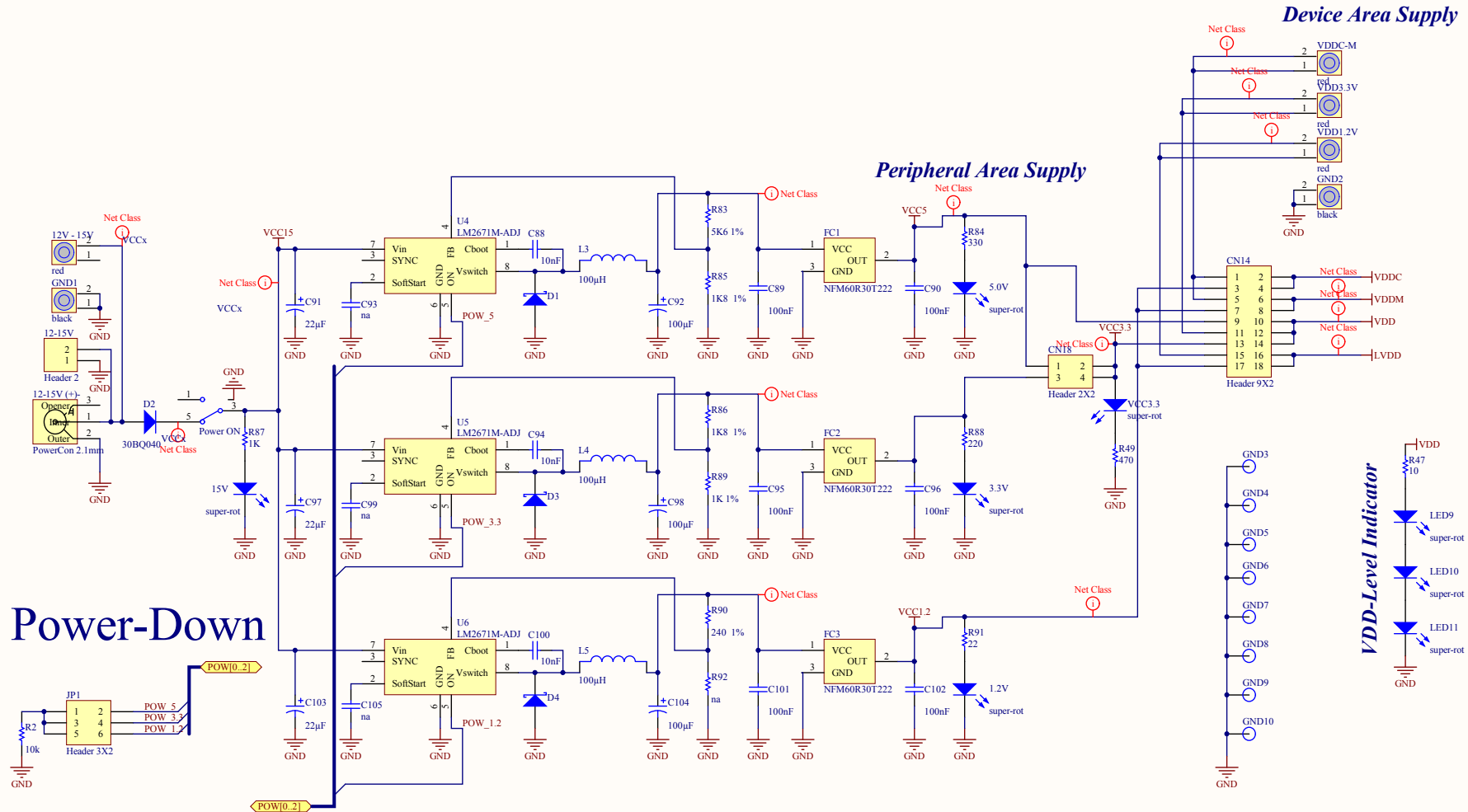
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AB-050-Px4 for PJ4			
Size	Number	Revision	
A3	EASE-UM-0069-	0.6	
Date:	29.10.2009	Sheet 3 of 5	
File:	C:\Data\...SCHDOC	Drawn By: NEC Electronics	

CAN



Title			AB-050-Px4 for PJ4
Size	Number	Revision	
A3	EASE-UM-0069-	0.6	
Date:	29.10.2009	Sheet 4 of 5	
File:	C:\Data\...4.SCHDOC	Drawn By: NEC Electronics	

Power Supply



Title			
AB-050-Px4 for PJ4			
Size	Number	Revision	
A3	EASE-UM-0069-	0.6	
Date:	29.10.2009	Sheet 5 of 5	
File:	C:\Data\55\SCHDOC	Drawn By: NEC Electronics	

