

V850E2/Px4 Application Board

User's Manual: Hardware

RENESAS MCU
V850 P Series

AB-050-PX4 Rev.: 1.0

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1. Introduction

The AB-050-Px4 is designed as a simple and easy to use Starter Board to support users with the first steps when starting with the V850E2/Px4.

The Starter Board is prepared to hold a V850E2/Px4 device (uPD70350x),

With the Nexus Debug interface and the Flash Programming interface for the Renesas PG-FP5 Flash Programmer the standard Renesas programming interfaces are directly available.

To enable further application development the board features drivers for 2 high speed CAN interfaces, 3 RS-232 interfaces, 3 LIN bus interfaces and 2 FlexRay interfaces.

With on-board voltage regulator and reset generator a simple external DC power supply is sufficient to operate the board.

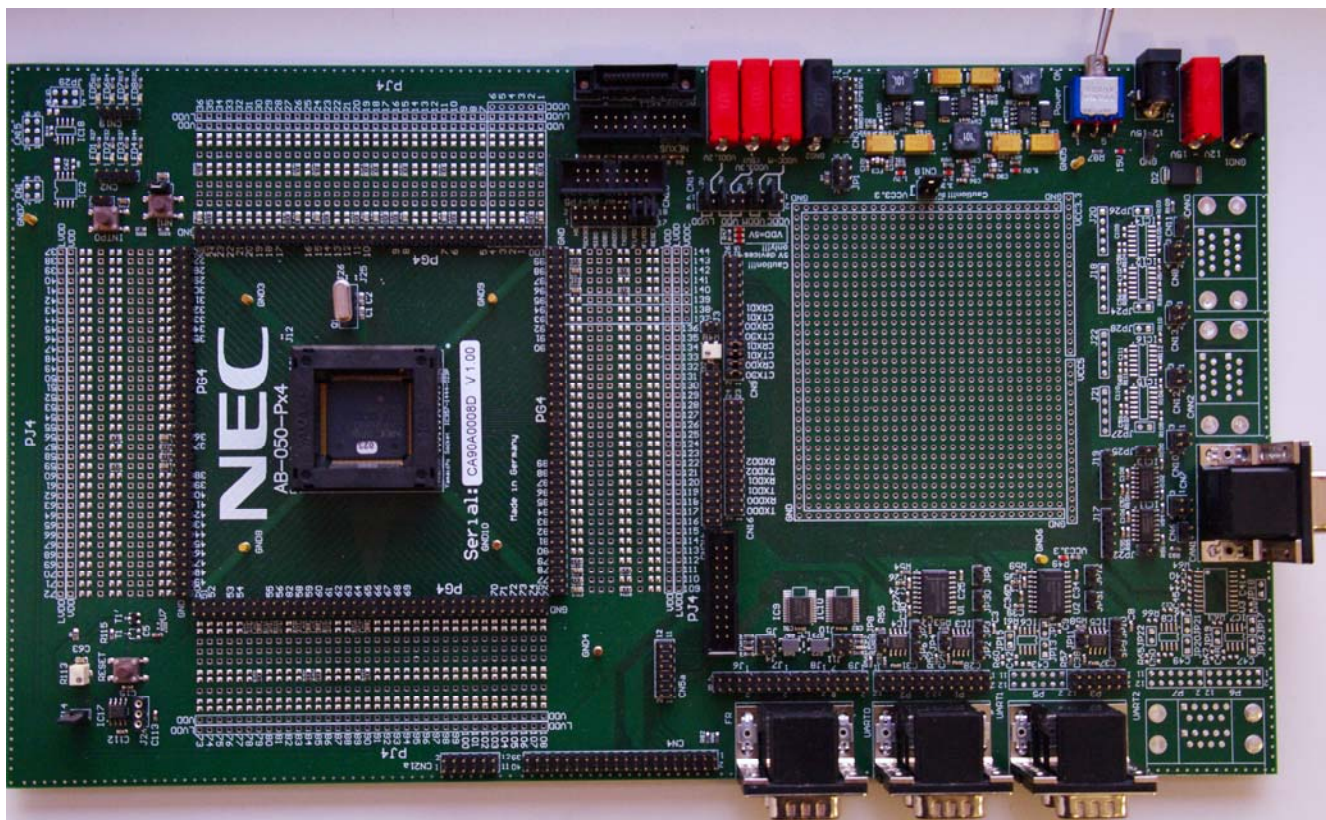


Figure 1. AB-050-Px4

2. Board description

2.1 Overview

Basically the board is divided into two areas, an 'Electrical Area' and a 'Functional Area'.

In Figure 2 the Electrical Area is marked yellow and the Functional Area is marked blue.

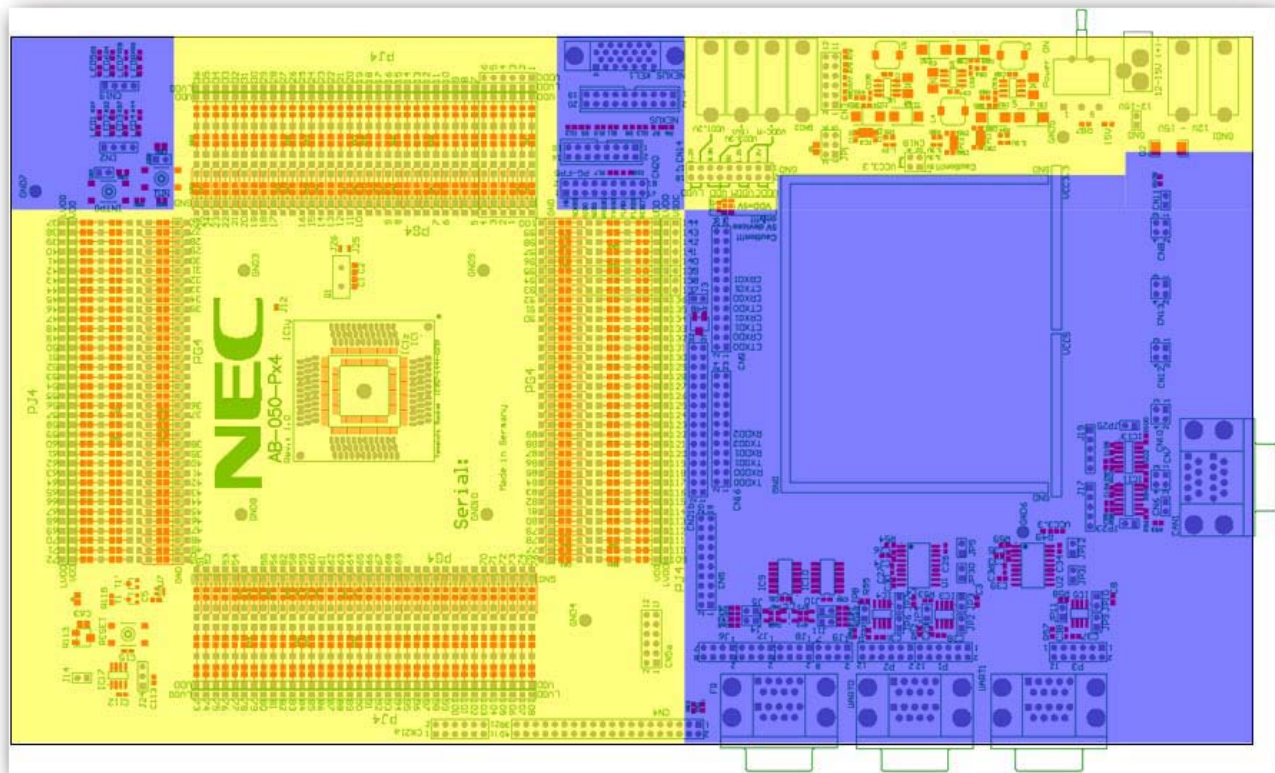


Figure 2. Board overview

2.1.1 Electrical Area

The yellow marked Electrical Area comprised the power supply, the reset circuit and the device socket with a surrounding Pin Patch Area. The core voltage supply is divided into a master and a checker domain, which is mandatory to fulfill the safety concept of the Px4 redundant core architecture.

In the centre of the Electrical Area the device socket is soldered either on a 100 pin or a 144 pin SMD pad field. On each side of the package/socket a "Pin Patch Area" is located.

In this patch area access is given to:

- each pin of the device ^(Note)
- VSS (GND)
- LVDD (1.2V)
- VDD (3.3V)

Further more SMD and through-hole components can directly be soldered onto the Pin Patch Area to allow simple networks to be easily built up.

Note:

The Board supports the 144pin PJ4 and the 100pin PG4 packaging. Inside pin labeling is for PG4, outside pin labeling for PJ4.

2.1.2 Functional Area

The blue marked Functional Area holds the drivers for RS-232, LIN bus, CAN and FlexRay. Additionally other patch areas are available as well to directly assembled LEDs, PowerDrivers and connectors to the board. Additional 2 EEPROM devices are available.

Note:

For detailed information about the operation of the used RS-232, LIN bus, CAN and FlexRay drivers refer to the related datasheets of those devices.

2.1.3 Connecting both areas

The Electrical and Functional Areas are not connected to each other except by a common VSS plane. Nevertheless by use of Jumpers a signal connection between the Electrical Area and the Functional Area is possible.

The following signals are available on the related jumper fields:

Signal	Jumper
FlexRay	CN5+CN5a
UART - URTHn (n=0..2)	CN16
CAN - FCNn (n=0..1)	CN9

Table 1. Overview of functional signals

2.1.4 Minimal configuration for quick start

To run the device without the Functional Area the following minimal configuration has to be done.

- select with CN14 the used power supply and VDD voltage
- assemble an 8MHz or an 16MHz oscillator to Q1
- set the required jumper setting to CN20

2.2 Reset

The V850E2/Px4 can be reset by asserting RESETZ input pin.

2.2.1 RESETZ input

The RESETZ input of the V850E2/Px4 is controlled via a pull-up resistor and transistor to GND. With J14 the connection to this circuit can be established.

2.3 Connecting the Power Supply

There are two different ways to supply the board with power:

a) Switching power supply

By supplying 12-15V to the 12-15V power connector jacket or to the 12-15V banana jacket. This will supply the on board voltage regulators for VCC5, VCC3.3 and VCC1.2 as well as directly supply VCC15.

b) Linear power supply

Optional the device voltages VDDC, VDDM, VDD and LVDD can be supplied separately by supplying the required voltages carefully to the corresponding banana jackets VDDC/M, VDD3.3V and VDD1.2V.

Use CN14 to select the device voltage supply source:

Supply voltage	Supply Source	CN14
VDDC	Extern	1-2
VDDC	Regulator	3-4
VDDM	Extern	5-6
VDDM	Regulator	7-8
VDD	Regulator 5V	9-10
VDD	Extern	11-12
LVDD	Extern	15-16
LVDD	Regulator	17-18

Table 2. Power Supply

VDDC and VDDM are the separated core voltage. VDDM supplies the Master Core and VDDC the Checker Core.

The board supports a voltage supply of 5V VDD. If the device should run with 5V, the voltage of the Functional Area and the Electrical Area has to be changed separately.

- With CN18 the voltage for the components of the Functional Area can be set to 5V.
- To switch the voltage of the device to 5V pin 9-10 of CN14 has to be connected.

Caution: Applying a voltage to the device outside the specified device operating voltage range may damage the device!

2.4 Nexus connection

The Nexus debug cable from a Renesas Debug Tool (e.g. MiniCube) can be connected to the Nexus Connector on the board.

KEL connector (Nexus_KEL1) is not supported by the AB-050-Px4 evaluation board.

The following jumpers must be closed in order to physically connect some of the Nexus signals from the Nexus Connector to the corresponding pins of the V850E2/Px4 device:

Jumper	Pin number
CN20	17-18
CN20	15-16

Table 3. Nexus

2.5 PG-FP5 connection

The programming cable of the PG-FP5 Flash programmer can be connected to 'PG-FP5' Connector.

To program the device via the CSI interface the following jumpers must be closed:

Connector	Pin number
CN20	3-4
CN20	5-6
CN20	7-8
CN20	13-14
CN20	15-16
CN20	17-18

Table 4. FP5 (CSI) Jumpers

To program the device via the UART interface the following jumpers must be closed:

Connector	Pin number
CN20	1-2
CN20	9-10
CN20	11-12
CN20	13-14
CN20	15-16
CN20	17-18

Table 5. FP5 (UART) Jumpers

Note:

For Flash programming, using the PG-FP5 device, power must be supplied by the AB-050-Px4. Please make sure to switch of power monitoring in PG-FP5 setup.

For Flash programming, using the PG-FP5, clock supply is done by the AB-050-Px4. Please make sure to enter the right crystal value in PG-FP5 setup.

2.6 RS-232 / LIN

2.6.1 RS-232 Transmission

V_{BAT} of the LIN bus driver is direct connected to the 12- 15V power supply jacket and the corresponding banana jackets. If the 12- 15V power supply is not used as power supply, a voltage in the range of 5V to 12V must be supplied to the jackets. For the exact specification refer to the Datasheet of the LIN Drivers.

Close the following jumpers on CN16 to physically connect the URTH signals from the Electrical Area to the Functional Area.

Signal		CN16
URTH0	TXD0	1-2
	RXD0	3-4
URTH1	TXD1	5-6
	RXD1	7-8
URTH2	TXD2	9-10
	RXD2	11-12

Table 6. URTHn signal jumpers

To connect the RS-232 bus driver signals to the RS-232 / LIN bus connectors close the following jumpers:

Signal		Connector	Pin #
URTH0	TXD0	P1	1-2
	RXD0		3-4
	GND		5-6
URTH1	TXD1	P2	1-2
	RXD1		3-4
	GND		5-6
URTH2	TXD2	P3	1-2
	RXD2		3-4
	GND		5-6

Table 7. RS-232 signal jumpers

To enable RS-232 transmission the disable Jumper must be removed from the corresponding RS232 transceiver. In addition the corresponding LIN-Transceiver must be send into SLEEP-Mode, otherwise it will disturb the transmission by limiting the level on RXD-Signal to 1,5V max. In most cases this high-level of 1,5V will not be recognized by the RS-232 controller.

To send LIN-Transceiver into SLEEP-Mode all 3 Jumpers must be removed from the LIN-Transceiver!

A falling edge must be generated on the NSLP-pin. This can either be done by setting and immediately removing the NSLP-Jumper after powering the board or by connecting both pins of the NSLP-Jumper via a 4,7nF capacity. By this the potential on the NSLP-Pin will follow the 5V power up and then it will be pulled down by the NSLP-Pin internal pull down resistor. This will generate the required falling edge.

2.6.2 LIN Transmission

To connect the LIN bus driver signals to the related RS-232/LIN bus connector close the following jumpers:

Signal		Connector	Pin #
LIN0	12V	P1	7-8
	LIN		9-10
	GND		11-12
		JP30	1-2
LIN1	12V	P2	7-8
	LIN		9-10
	GND		11-12
LIN2	12V	P3	7-8
	LIN		9-10
	GND		11-12
		JP31	1-2
LIN3	12V	P5	7-8
	LIN		9-10
	GND		11-12
LIN4	12V	P6	7-8
	LIN		9-10
	GND		11-12
LIN5	12V	P7	7-8
	LIN		9-10
	GND		11-12

Table 8. LIN bus signal jumpers

To enable the LIN drivers (IC3, IC4, IC5, IC6, IC7, IC8) the NSLP pin of the drivers must be pulled high. To do so a Jumper is available to connect the pin to VDD.

LIN channel	NLSP Jumper
0	JP3
1	JP7
2	JP10
3	JP14
4	JP17
5	JP21

Table 9. LIN NLSP Pin

At same time the RS232 Transceiver RX Pin must be disabled for the LIN-enabled channel. This must be done by the Disable Jumper connected to the EN-Pin of RS232 Transceiver.

LIN channel	RS232 Jumper
0	JP5
1	JP5
2	JP12
3	JP12
4	JP18
5	JP18

Table 10. LIN RS232 Jumper

Note: The Disable Jumper will disable 2 channels at same time!

The RxD pin of the LIN driver (pin #1) is an open drain output. The necessary pull-up resistor in order to interface to the Px4 device is not assembled on the board. To enable operation of the RxD signal user has either

- To connect an appropriate pull up resistor to the related RxD input pin of the LIN channel,

Or

- To enable the internal Pull-Up resistors available in the Px4 devices for each LIN input pin.

For additional information on the LIN driver refer to its User's Manual / Datasheet.

2.7 CAN

Power is permanently supplied to the CAN drivers by VCC5 and VCC3.3 and VCC15. These power lines are decoupled from Px4 power supply areas VDDC, VDDM, VDD, LVDD.

Close the following jumpers to physically connect the devices CAN signals to the CAN interface drivers located on the Functional Area of the board:

Signal		CN9
FCN0	CTXD0	1-2
	CRXD0	3-4
FCN1	CTXD1	5-6
	CRXD1	7-8
FCN2	CTXD2	9-10
	CRXD2	11-12
FCN3	CTXD3	13-14
	CRXD3	15-16
FCN4	CTXD4	17-18
	CRXD4	19-20
FCN5	CTXD5	21-22
	CRXD51	23-24
FCN6		25-26
	CRXD6	27-28 ^{Note}

Table 11. FCNn signal jumpers

Note: CAN6 of V850E2/Px4 is for diagnosis purpose and has only receive functionality. The physical interface on the Px4-Board is shared with the one for CAN5. Please make sure to jumper only one of them.

2.8 FlexRay

Power is permanently supplied to the FlexRay drivers by VCC5 and VCC3.3 and VCC15. These power lines are decoupled from Px4 power supply areas VDDC, VDDM, VDD, LVDD.

Close the following jumpers to physically connect the devices FlexRay signals to the FlexRay interface drivers located on the Functional Area of the board:

Signal		CN5a
FlexRay	FTXDA	1-2
	FRXDA	3-4
	FTXENA	5-6
	FTXDB	7-8
	FRXDB	9-10
	FTXENB	11-12

Table 12. FlexRay signal jumpers

Note: To control the operating mode of FlexRay interface drivers, the following jumpers have to be closed:

Signal	CN5
FR_EN1	1-2
FR_EN2	3-4
FR_STBN1	5-6
FR_STBN2	7-8
FR_WAKE1	9-10
FR_WAKE2	11-12
FR_RXEN1	13-14
FR_RXEN2	15-16
FR_ERRN1	17-18
FR_ERRN2	19-20

Table 13. FlexRay control jumpers

To connect the FlexRay bus driver signals to the related FlexRay bus connector close the following jumpers according to your requirements (refer to the AB-050-PJ4-Schematics for details):

Signal		Connector	Pin #
FlexRay	CH0_A	J6	x-y
	CH0_B	J7	x-y
	CH1_A	J8	x-y
	CH1_B	J9	x-y

Table 14. FlexRay bus jumpers

To terminate the FlexRay bus close the following jumpers:

Signal		Connector	Pin #
FlexRay	CH0_A	J4	1-2
	CH0_B	J5	1-2
	CH1_A	J10	1-2
	CH1_B	J11	1-2

Table 15. FlexRay bus termination jumpers

3. FlexRay / UART / LIN / CAN DSUB connectors

To physically connect the Starter Board to other UART / LIN / CAN devices DSUB type connectors are available.

3.1 UART / LIN connectors

To interface the AB-050-Px4 board to external to UART / LIN devices a 9 pin male D-SUB connector is supplied for each of the six available UART / LIN interfaces.

The signal layout of the UART/LIN DSUB connector can be seen in Table 16.

Male D-SUB, 9pin	Function
1	n/c
6	n/c
2	RS-232 TxD
7	LIN
3	RS-232 RxD or GND
8	n/c
4	n/c
9	+12V
5	GND

Table 16. UART / LIN DSUB connectors

3.2 FlexRay connectors

To interface the AB-050-Px4 board to external to FlexRay devices a 9 pin male D-SUB connector is supplied for each of the two available FlexRay interfaces.

The signal layout of the FlexRay D-SUB connector can be seen in Table 17.

Male D-SUB, 9pin	Function
1	n/c
6	n/c
2	CH0_A or CH1_A
7	CH0_B or CH1_A
4	CH0_A or CH1_A
8	CH0_B or CH1_A
3	n/c
9	n/c
5	n/c

Table 17. FlexRay DSUB connectors

Figure 3 displays the assignment of each DSUB connector to its related peripheral:

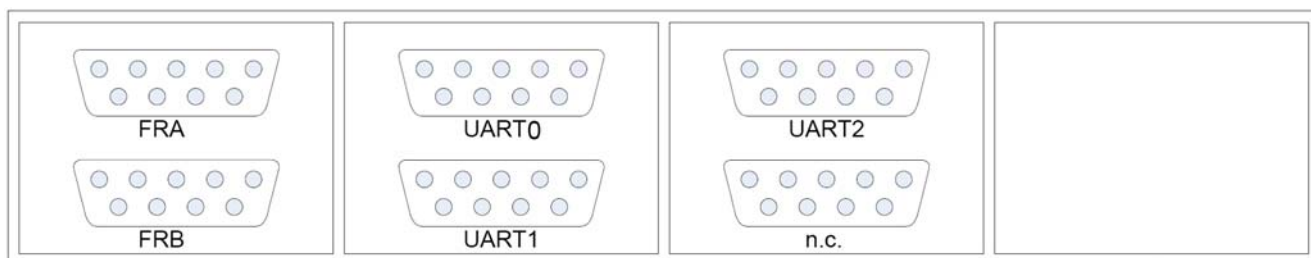


Figure 3. FlexRay / UART / LIN DSUB connectors

3.3 CAN connectors

To interface the AB-050-Px4 board to external CAN devices a 9 pin female D-SUB connector is supplied for each of the six available CAN interfaces.

The pin functions of the CAN DSUB connectors can be seen in Table 18.

Male D-SUB, 9pin	Function
1	n/c
6	GND
2	CANL
7	CANH
3	GND (if jumpered)
8	n/c
4	n/c
9	n/c
5	n/c

Table 18. CAN DSUB connectors

Figure 4 displays the assignment of each DSUB connector to its related peripheral:



Figure 4. CAN DSUB connectors

3.4 Pin connection

The pin connection, which is described below, is already done on the board.

3.4.1 Power supply pins

Connect the devices power supply pins to the related power lines using the available SMD pads in the Pin Patch Areas.

Refer to the V850E2/Px4 User's Manual and Electrical Target Specification for the location of the VDD and VSS pins on the different devices.

Connect the VDD and VSS pins in the Pin Patch Areas like this:

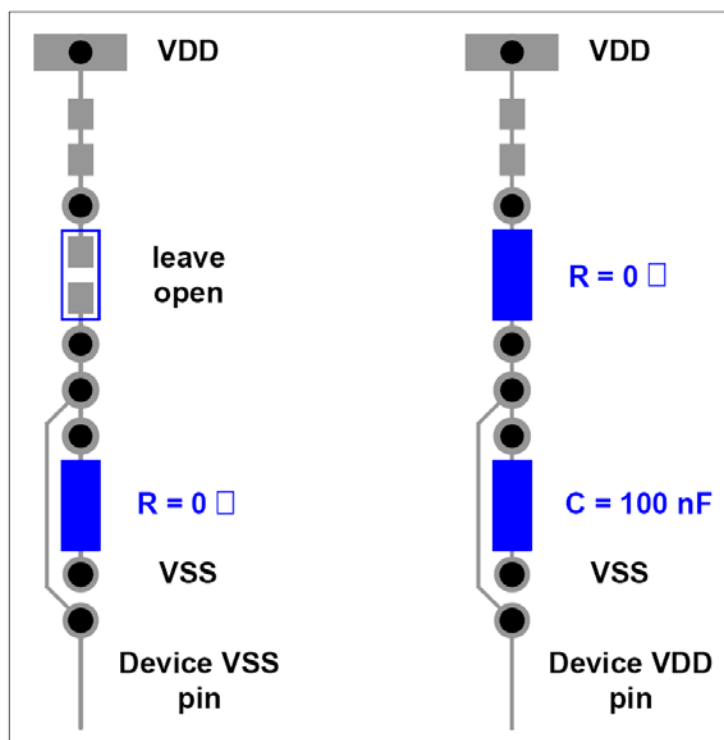


Figure 5. Device power supply

To connect the devices VSS pins to the VSS lane of the board place a 0 Ohm resistor on the SMD1 pad.

To connect the devices VDD pins to the VDD lane of the board place a 0 Ohm resistor on the SMD2 pad and place a 100 nF buffering capacitor on the SMD1 pad.

3.4.2 REGC pin

A buffering capacitor between the devices REGC pin(s) and VSS should be placed. Assemble the capacitor to the SMD1 pad field.

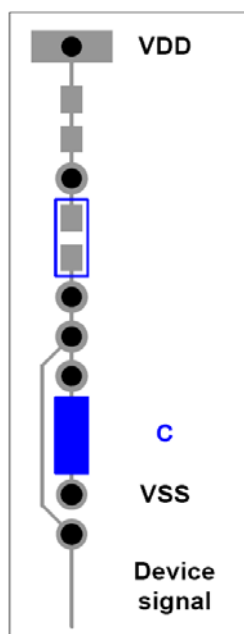


Figure 6. REGC pin components

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the REGC pin on the different devices.

3.4.3 X1, X2 pins

The external crystal can be connected to the socket Q1. Alternatively An external oscillator can be connected to the X1 and X2 pins of the device. Connect the oscillator between the X1 and X2 pins and place a small capacitor on the SMD1 areas of those pins. For size of the capacitor refer to the oscillator manufacturer specification / recommendation.

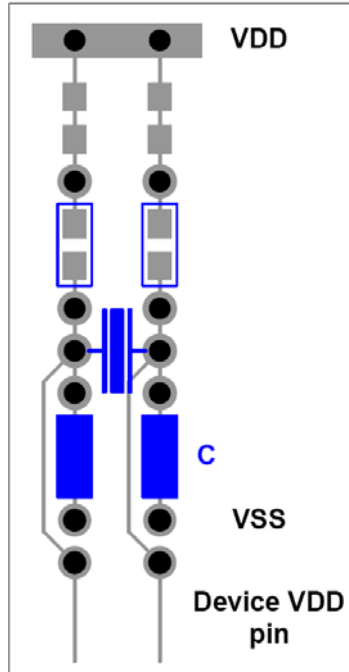


Figure 7. X1, X2 pin components

In this case you have to connect the J25 and J26 with solder.

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the X1 and X2 pins on the different devices.

3.4.4 XT1, FLMD0

A pull-down resistor should be connected to input pin FLMD0.

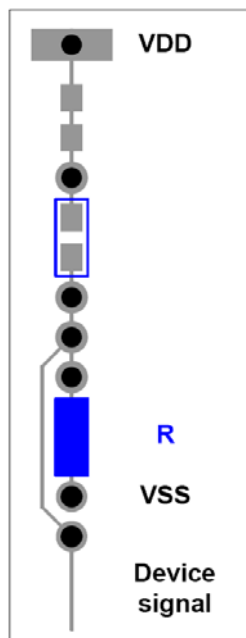


Figure 8. Pins with Pull-Down

Refer to the Px4 User's Manual and Electrical Target Specification for the location of the FLMD0 pins on the different devices.

3.5 Functional pin connection

As the routing of the functional signals (Reset, UARTH_n, CAN_n, NWIRE and FP5) between the device SMD pad area and the Jumpers connecting the Electrical Area and Functional Area is based on the Px4 device, the routing of those signals for other Px4 devices must be place manually.

To do so, connect a wire between the device pin (e.g. from one of the through holes in the Pin Patch areas) and the functional side of the related signal jumper.

Caution: Do not close the related Jumpers of any of the newly routed signals as this can lead to a direct connection between different device pins. Be aware that no further disconnection by the use of jumpers between the Electrical Area and Functional Area is possible after wiring the signals for other than Px4 devices.

3.5.1 Jumper and connector overview

The location of all jumpers located on the board can be seen in the Figure 9.

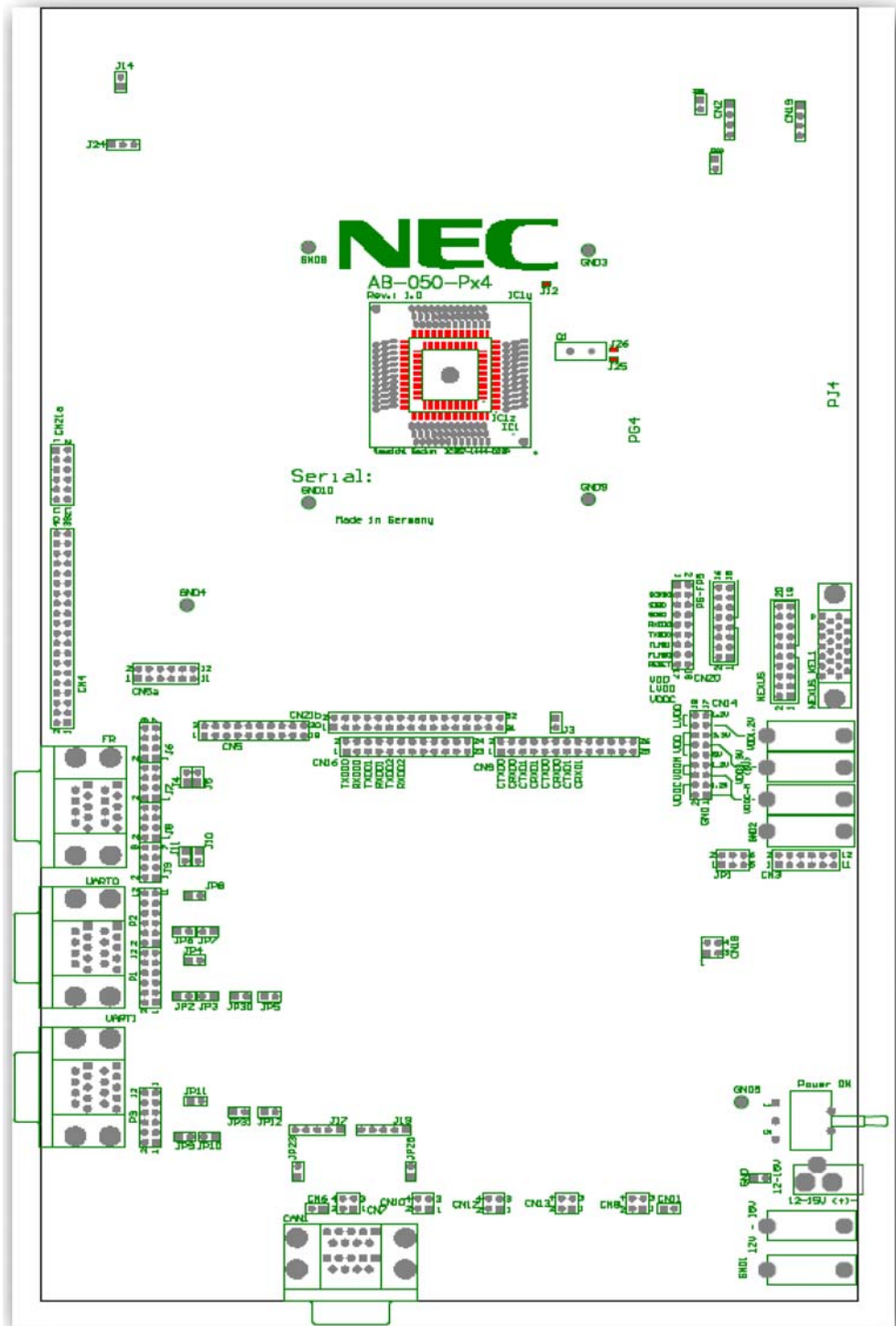


Figure 9. Jumper and connector location

4. Revision History

Version	Chapter	Comment
0.1-0.4		Initial releases incl. bug fixes
0.5-0.6		Modification due to merger of Renesas Technologies and NEC Electronics.
0.7		Socket board schematics attached.
0.8		Included information: KEL connector not supported.
0.09		Modified document template and document numbering format.

V850E2/Px4 Application Board User's Manual: Hardware

Publication Date: Rev.0.8 Jul, 2010
Rev.0.09 Apr 28, 2011

Published by: Renesas Electronics Europe



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Renesas Electronics Korea Co., Ltd.

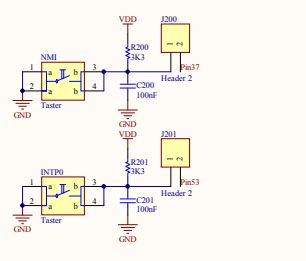
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Tel: +82-2-558-3737, Fax: +82-2-558-5141

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Colophon 1.0

V850E2/Px4 Application Board

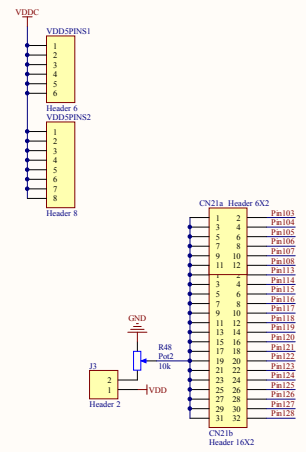
Device Footprint

A



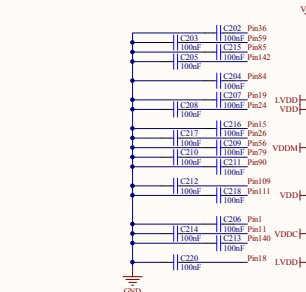
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<p>0129 Pin129 P5_1 UCSH1CS2URTHXKINTP1CSBHCS2CSBHRY4URTHXKINTP4ADCATRG0INTP3</p> <p>0130 Pin130 P5_2 CSBH1CS1URTHXKINTP2CSBHCS1URTHXSCADCATRG1INTP4CSBHRY0</p> <p>0131 Pin131 P5_3 CSBH1CS2URTHXKINTP3CSBHCS2ADCATRG0ADCATRG2INTP5</p> <p>0132 Pin132 P5_4 CSBH1CS2CSBHCS1CSBH1RYURTHXCS</p> <p>0133 Pin133 P5_5 STALDR1TALDR1CSBH1INTP1</p> <p>0134 Pin134 P5_6 CSBH1CS2URTHXKINTP1</p> <p>0135 Pin135 P5_7 CSBH1CS2URTHXKINTP1</p> <p>0136 Pin136 P5_8 CSBH1CS2URTHXKINTP1</p> <p>0137 Pin137 P5_9 CSBH1CS2URTHXKINTP1</p> <p>0138 Pin138 P5_10 CSBH1CS2URTHXKINTP1</p> <p>0139 Pin139 P5_11 CSBH1CS2URTHXKINTP1</p>	<p>0140 Pin140 P6_0 CSKGS2TSG06TALIA001TSG2000</p> <p>0141 Pin141 P6_1 CSKGS2URTHXKINTP1TSG2000</p> <p>0142 Pin142 P6_2 CSKGS2URTHXKINTP1TSG2000</p> <p>0143 Pin143 P6_3 CSKGS2URTHXKINTP1TSG2000</p> <p>0144 Pin144 P6_4 CSKGS2URTHXKINTP1TSG2000</p> <p>0145 Pin145 P6_5 CSKGS2URTHXKINTP1TSG2000</p> <p>0146 Pin146 P6_6 CSKGS2URTHXKINTP1TSG2000</p> <p>0147 Pin147 P6_7 CSKGS2URTHXKINTP1TSG2000</p> <p>0148 Pin148 P6_8 CSKGS2URTHXKINTP1TSG2000</p> <p>0149 Pin149 P6_9 CSKGS2URTHXKINTP1TSG2000</p> <p>0150 Pin150 P6_10 CSKGS2URTHXKINTP1TSG2000</p> <p>0151 Pin151 P6_11 CSKGS2URTHXKINTP1TSG2000</p> <p>0152 Pin152 P6_12 CSKGS2URTHXKINTP1TSG2000</p> <p>0153 Pin153 P6_13 CSKGS2URTHXKINTP1TSG2000</p> <p>0154 Pin154 P6_14 CSKGS2URTHXKINTP1TSG2000</p> <p>0155 Pin155 P6_15 CSKGS2URTHXKINTP1TSG2000</p> <p>0156 Pin156 P6_16 CSKGS2URTHXKINTP1TSG2000</p> <p>0157 Pin157 P6_17 CSKGS2URTHXKINTP1TSG2000</p> <p>0158 Pin158 P6_18 CSKGS2URTHXKINTP1TSG2000</p> <p>0159 Pin159 P6_19 CSKGS2URTHXKINTP1TSG2000</p> <p>0160 Pin160 P6_20 CSKGS2URTHXKINTP1TSG2000</p>

B



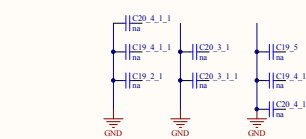
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<p>0103 Pin103 ADCAM1</p> <p>0104 Pin104 ADCAM2</p> <p>0105 Pin105 ADCAM3</p> <p>0106 Pin106 ADCAM4</p> <p>0107 Pin107 ADCAM5</p> <p>0108 Pin108 ADCAM6</p> <p>0109 Pin109 ADCAM7</p> <p>0110 Pin110 ADCAM8</p> <p>0111 Pin111 ADCAM9</p> <p>0112 Pin112 ADCAM10</p> <p>0113 Pin113 ADCAM11</p> <p>0114 Pin114 ADCAM12</p> <p>0115 Pin115 ADCAM13</p> <p>0116 Pin116 ADCAM14</p> <p>0117 Pin117 ADCAM15</p> <p>0118 Pin118 ADCAM16</p> <p>0119 Pin119 ADCAM17</p> <p>0120 Pin120 ADCAM18</p> <p>0121 Pin121 ADCAM19</p> <p>0122 Pin122 ADCAM20</p> <p>0123 Pin123 ADCAM21</p> <p>0124 Pin124 ADCAM22</p>	<p>P1_0 ADCATRG2INTP5CSKGSURTHXKINTP0FCN1TX</p> <p>P1_1 ADCATRG1INTP4CSKGSURTHXKINTP0FCN1TX</p> <p>P1_2 ADCATRG0INTP3CSKGSURTHXKINTP0FCN1TX</p> <p>P1_3 ADCATRG3INTP6CSKGSURTHXKINTP0FCN1TX</p> <p>P1_4 ADCATRG4INTP7CSKGSURTHXKINTP0FCN1TX</p> <p>P1_5 ADCATRG5INTP8CSKGSURTHXKINTP0FCN1TX</p> <p>P1_6 ADCATRG6INTP9CSKGSURTHXKINTP0FCN1TX</p> <p>P1_7 ADCATRG7INTP10CSKGSURTHXKINTP0FCN1TX</p> <p>P1_8 ADCATRG8INTP11CSKGSURTHXKINTP0FCN1TX</p> <p>P1_9 ADCATRG9INTP12CSKGSURTHXKINTP0FCN1TX</p> <p>P1_10 ADCATRG10INTP13CSKGSURTHXKINTP0FCN1TX</p> <p>P1_11 ADCATRG11INTP14CSKGSURTHXKINTP0FCN1TX</p> <p>P1_12 ADCATRG12INTP15CSKGSURTHXKINTP0FCN1TX</p> <p>P1_13 ADCATRG13INTP16CSKGSURTHXKINTP0FCN1TX</p> <p>P1_14 ADCATRG14INTP17CSKGSURTHXKINTP0FCN1TX</p> <p>P1_15 ADCATRG15INTP18CSKGSURTHXKINTP0FCN1TX</p> <p>P1_16 ADCATRG16INTP19CSKGSURTHXKINTP0FCN1TX</p> <p>P1_17 ADCATRG17INTP20CSKGSURTHXKINTP0FCN1TX</p> <p>P1_18 ADCATRG18INTP21CSKGSURTHXKINTP0FCN1TX</p> <p>P1_19 ADCATRG19INTP22CSKGSURTHXKINTP0FCN1TX</p> <p>P1_20 ADCATRG20INTP23CSKGSURTHXKINTP0FCN1TX</p>

C

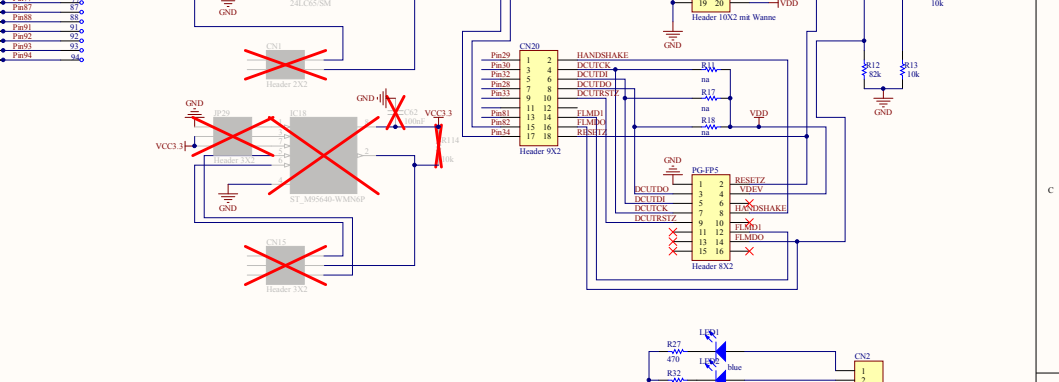
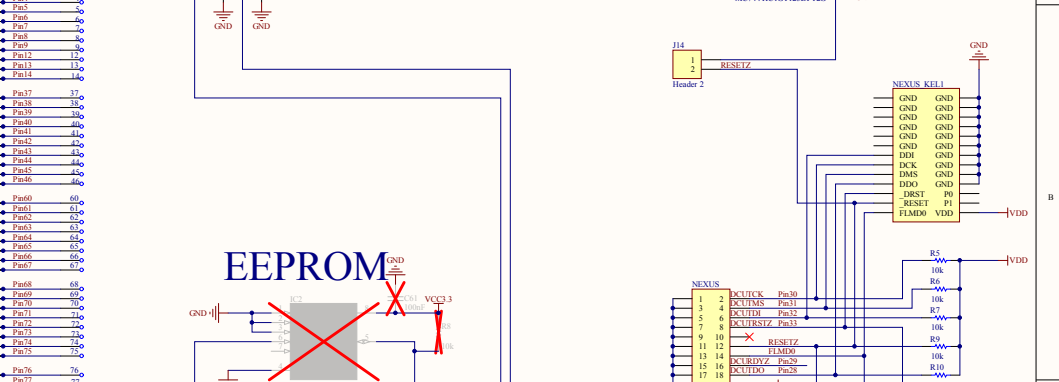
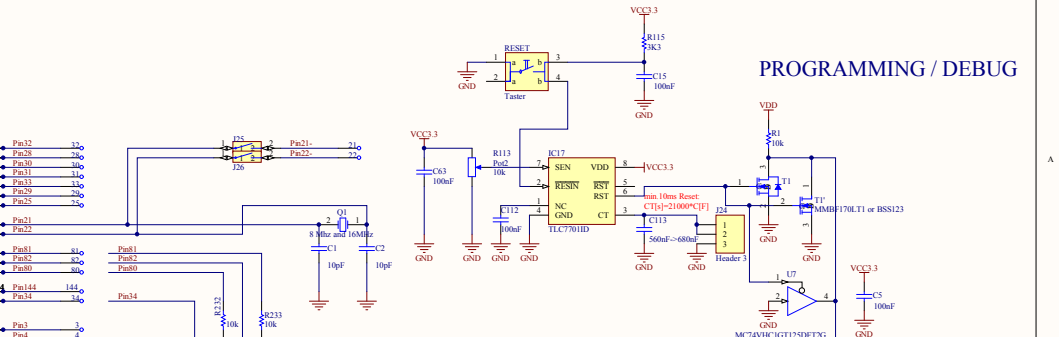


IC1B IC1d IC1e	IC1c
<p>0135 Pin135 EVVD</p> <p>0136 Pin136 EVVD</p> <p>0137 Pin137 EVVD</p> <p>0138 Pin138 EVVD</p> <p>0139 Pin139 EVVD</p> <p>0140 Pin140 EVVD</p> <p>0141 Pin141 EVVD</p> <p>0142 Pin142 EVVD</p> <p>0143 Pin143 EVVD</p> <p>0144 Pin144 EVVD</p> <p>0145 Pin145 EVVD</p> <p>0146 Pin146 EVVD</p> <p>0147 Pin147 EVVD</p> <p>0148 Pin148 EVVD</p> <p>0149 Pin149 EVVD</p> <p>0150 Pin150 EVVD</p> <p>0151 Pin151 EVVD</p> <p>0152 Pin152 EVVD</p> <p>0153 Pin153 EVVD</p> <p>0154 Pin154 EVVD</p> <p>0155 Pin155 EVVD</p> <p>0156 Pin156 EVVD</p> <p>0157 Pin157 EVVD</p> <p>0158 Pin158 EVVD</p> <p>0159 Pin159 EVVD</p> <p>0160 Pin160 EVVD</p>	<p>P2_0 TALIA001TALIA001TALIA001URTHXKINTP3TSG2100TALIA001CSBHCS0</p> <p>P2_1 TALIA002TALIA002TALIA002URTHXKINTP3TSG2100TALIA002CSBHCS0</p> <p>P2_2 TALIA003TALIA003TALIA003URTHXKINTP3TSG2100TALIA003CSBHCS0</p> <p>P2_3 TALIA004TALIA004TALIA004URTHXKINTP3TSG2100TALIA004CSBHCS0</p> <p>P2_4 TALIA005TALIA005TALIA005URTHXKINTP3TSG2100TALIA005CSBHCS0</p> <p>P2_5 TALIA006TALIA006TALIA006URTHXKINTP3TSG2100TALIA006CSBHCS0</p> <p>P2_6 TALIA007TALIA007TALIA007URTHXKINTP3TSG2100TALIA007CSBHCS0</p> <p>P2_7 TALIA008TALIA008TALIA008URTHXKINTP3TSG2100TALIA008CSBHCS0</p> <p>P2_8 TALIA009TALIA009TALIA009URTHXKINTP3TSG2100TALIA009CSBHCS0</p> <p>P2_9 TALIA010TALIA010TALIA010URTHXKINTP3TSG2100TALIA010CSBHCS0</p> <p>P2_10 TALIA011TALIA011TALIA011URTHXKINTP3TSG2100TALIA011CSBHCS0</p> <p>P2_11 TALIA012TALIA012TALIA012URTHXKINTP3TSG2100TALIA012CSBHCS0</p> <p>P2_12 TALIA013TALIA013TALIA013URTHXKINTP3TSG2100TALIA013CSBHCS0</p> <p>P2_13 TALIA014TALIA014TALIA014URTHXKINTP3TSG2100TALIA014CSBHCS0</p> <p>P2_14 TALIA015TALIA015TALIA015URTHXKINTP3TSG2100TALIA015CSBHCS0</p> <p>P2_15 TALIA016TALIA016TALIA016URTHXKINTP3TSG2100TALIA016CSBHCS0</p> <p>P2_16 TALIA017TALIA017TALIA017URTHXKINTP3TSG2100TALIA017CSBHCS0</p> <p>P2_17 TALIA018TALIA018TALIA018URTHXKINTP3TSG2100TALIA018CSBHCS0</p> <p>P2_18 TALIA019TALIA019TALIA019URTHXKINTP3TSG2100TALIA019CSBHCS0</p> <p>P2_19 TALIA020TALIA020TALIA020URTHXKINTP3TSG2100TALIA020CSBHCS0</p> <p>P2_20 TALIA021TALIA021TALIA021URTHXKINTP3TSG2100TALIA021CSBHCS0</p>

D



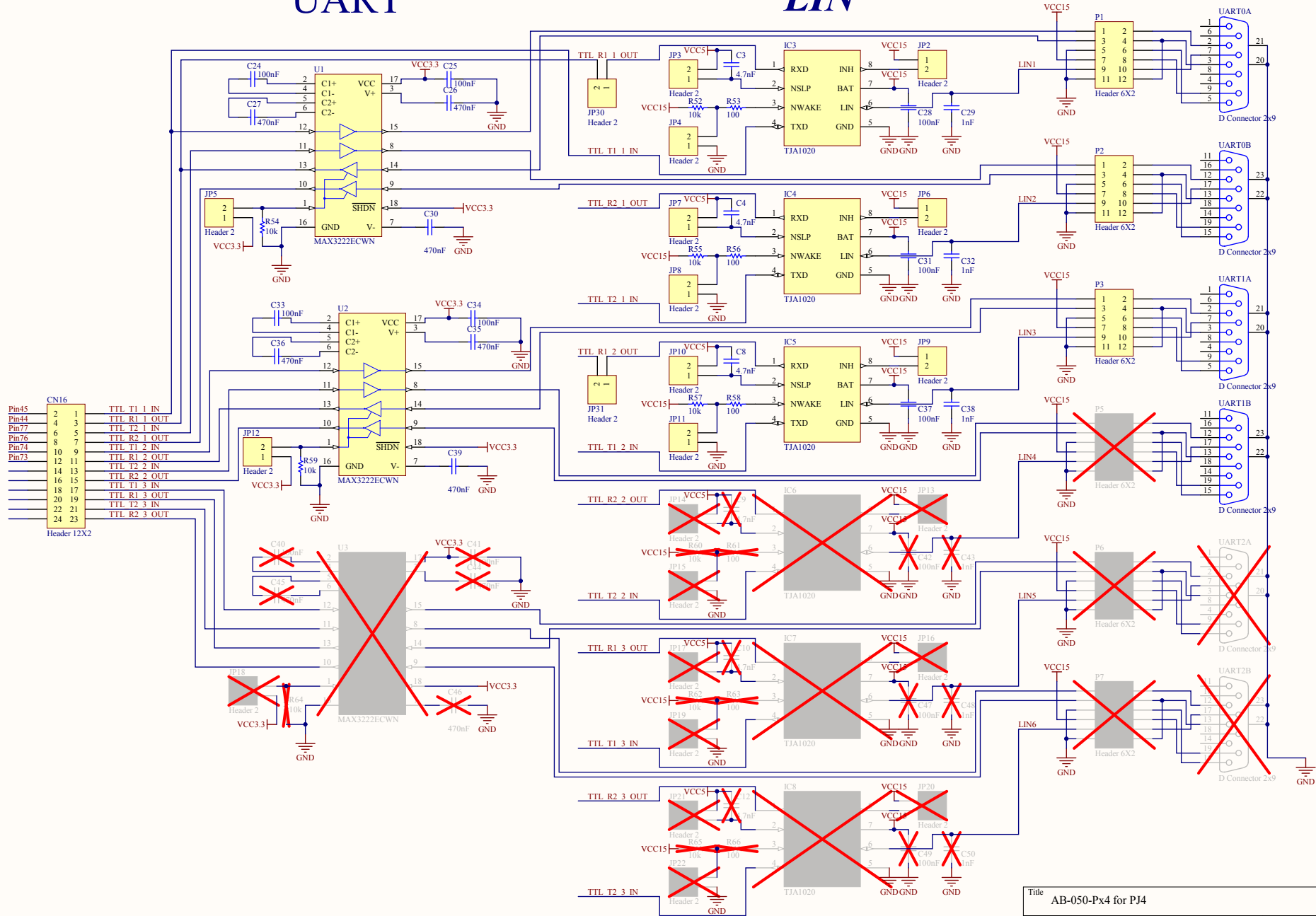
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0194	0195	0196	0197	0198	0199	0200	0201	0202	0203	0204	0205	0206



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	A2	EASE-UM-0069-	0.6
Date	20 10 2009	Sheet	1 of 5
File	C:\Users\N.SCHURK	Drawn by	N.C. Electronics

UART

LIN



CN16 Header 12X2

Pin45	2	1	TTL T1 1 IN
Pin44	4	3	TTL R1 1 OUT
Pin77	6	5	TTL T2 1 IN
Pin76	8	7	TTL R2 1 OUT
Pin74	10	9	TTL T1 2 IN
Pin73	12	11	TTL R1 2 OUT
	14	13	TTL T2 2 IN
	16	15	TTL R2 2 OUT
	18	17	TTL T1 3 IN
	20	19	TTL R1 3 OUT
	22	21	TTL T2 3 IN
	24	23	TTL R2 3 OUT

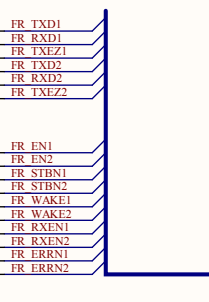
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Size A3	Number EASE-UM-0069-	Revision 0.6
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FlexRay Physical Layer

FlexRay Physical Layer No. 1

FlexRay Physical Layer No. 2

FlexRay-Conformance

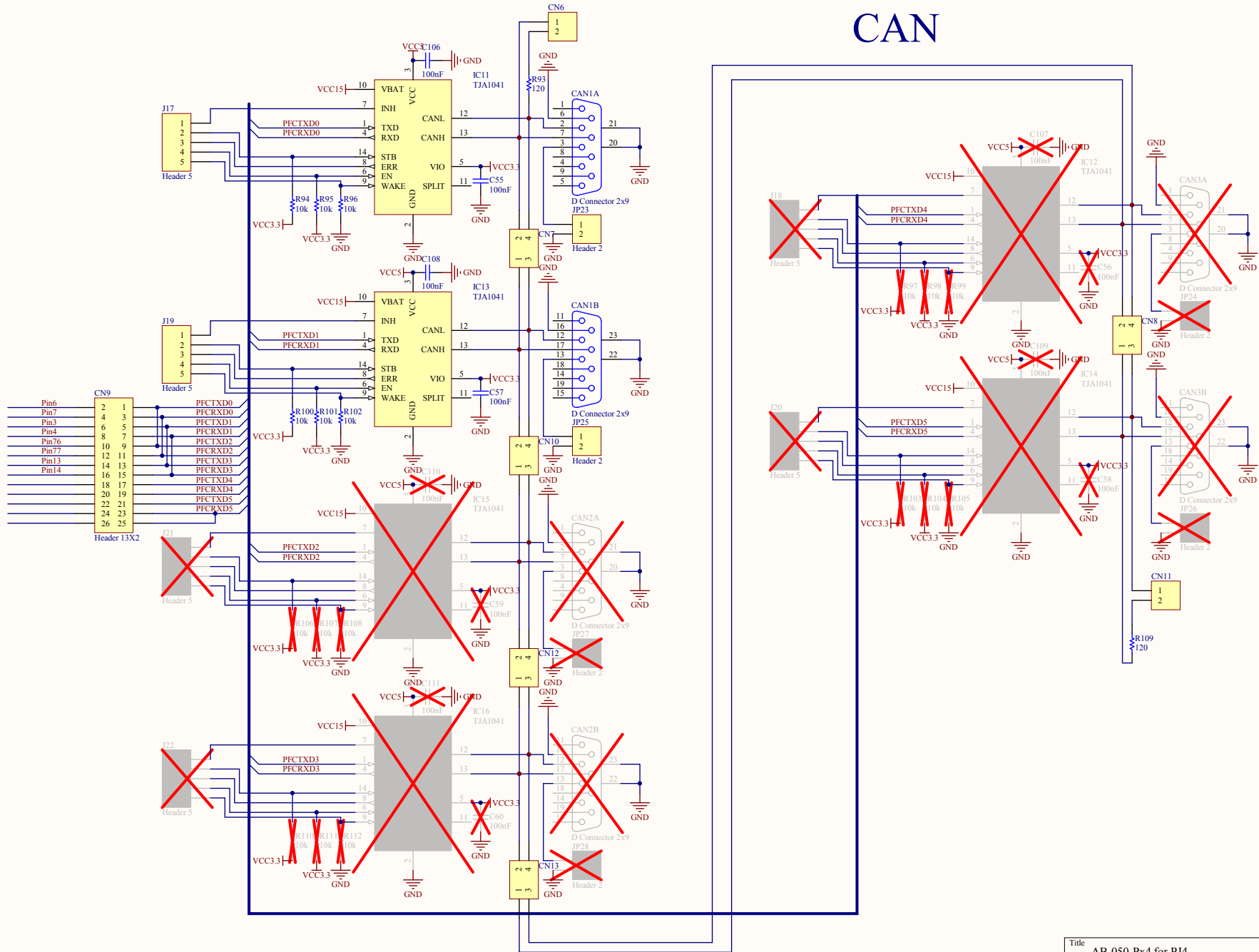


Pin	Signal
Pin52	FR_TXD1
Pin50	FR_RXD1
Pin51	FR_TXEZ1
Pin55	FR_TXD2
Pin53	FR_RXD2
Pin54	FR_TXEZ2
Pin95	FR_EN1
Pin96	FR_EN2
Pin97	FR_STBN1
Pin98	FR_STBN2
Pin99	FR_WAKE1
Pin100	FR_WAKE2
Pin101	FR_RXEN1
Pin102	FR_RXEN2
Pin66	FR_ERRN1
Pin67	FR_ERRN2

Pin	Signal
Pin52	FR_TXD1
Pin50	FR_RXD1
Pin51	FR_TXEZ1
Pin55	FR_TXD2
Pin53	FR_RXD2
Pin54	FR_TXEZ2
Pin76	
Pin73	RESETZ
Pin87	
Pin77	
Pin74	
Pin88	
Pin29	VCC3.3
Pin31	VCC5
Pin33	VCC5
Pin34	VCC5
Pin35	VCC15
Pin36	VCC15
Pin37	VCC15
Pin38	VCC15
Pin39	VCC15
Pin40	VCC15

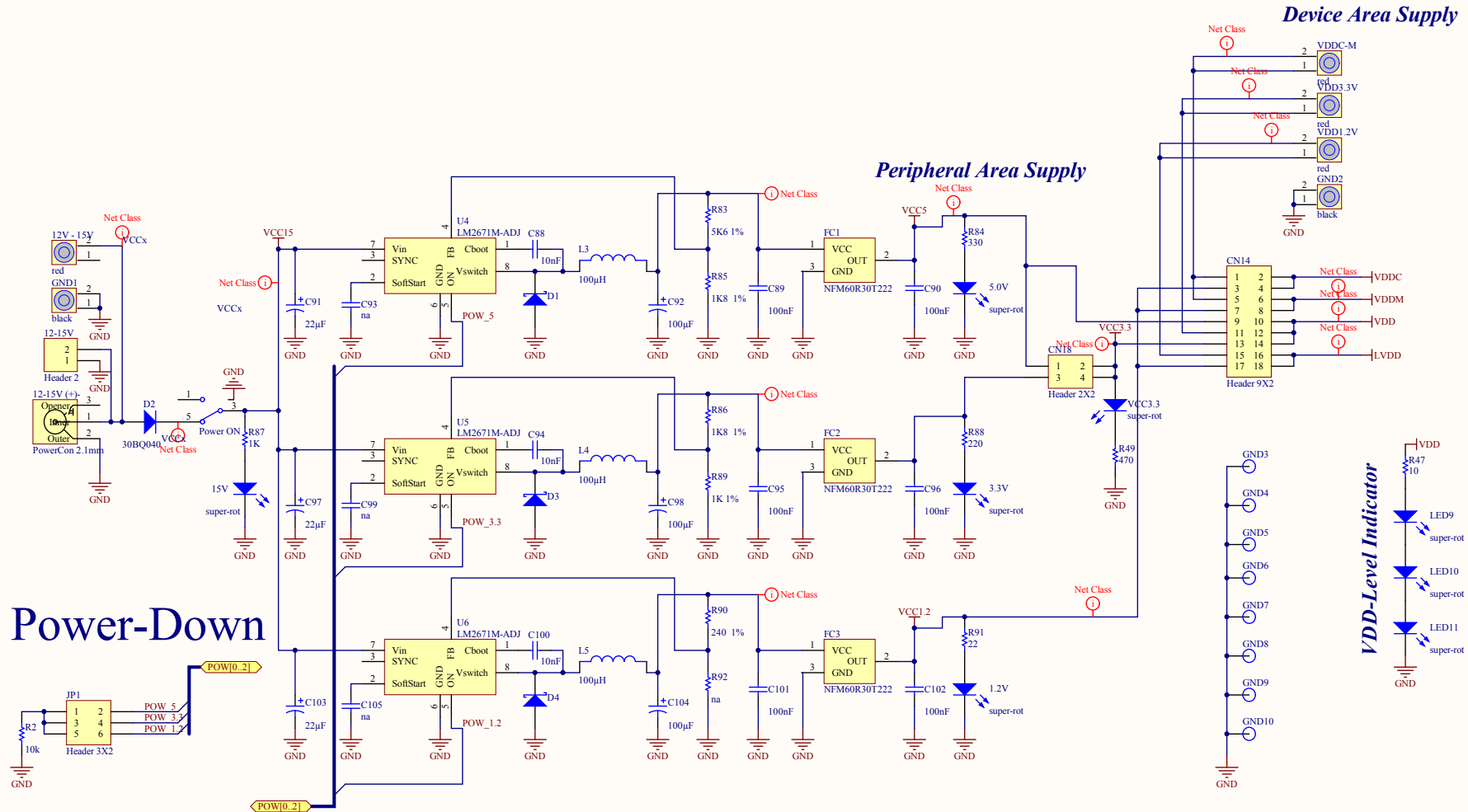
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Size	Number	Revision	
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Date:	29.10.2009	Sheet 3 of 5	
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CAN



Title		
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Size	Number	Revision
A3	EASE-UM-0069-	0.6
Date:	29.10.2009	Sheet 4 of 5
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Power Supply



Title			
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Size	Number	Revision	
A3	EASE-UM-0069-	0.6	
Date:	29.10.2009	Sheet 5 of 5	
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