Preliminary User's Manual

NEC

IE-780948-SL-EM1
IE-780948-SL-EM4

Emulation Board and Probe Board

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This equipment complies with the EMC protection requirements.

Warning

This is a ´Class A´ (EN 55022: 1994) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

Caution

This equipment should be handled like a CMOS semiconductor device. The user must take all precautions to avoid build-up of static electricity while working with this equipment. All test and measurement tools including the workbench must be grounded. The user/operator must be grounded using the wrist strap. The In-Circuit Emulator probe target connector plug and/or its adapter pins should not be touched with bare hands.

The related documents in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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Preface

Product Outline

The IE-780948-SL-EM1 and IE-780948-SL-EM4, in combination with the IE-78001-R-A, is used for debugging the following target devices of the 78K/0 series 8-bit single-chip microcontrollers.

- μPD780948 subseries: μPD780948, 78F0948[Note]

Note: Under development

Intended Readership

This manual is intended for engineers who perform system debugging using the IE-78001-R-A in combination with the IE-780948-SL-EM1 and IE-780948-SL-EM4.

Engineers reading this manual are assumed to have sufficient knowledge regarding functions and use of the above target devices and the debugger.

Organization

There are four manuals relating to use of the IE-78001-R-A: This manual, supplied with the IE-780948-SL-EM1, the manual supplied with the IE-78001-R-A and the manual supplied with the integrated debugger (Introduction and reference volumes).

IE-780948-SL-EM1 User's Manual	IE-780948-SL-EM4 User's Manual	IE-78001-R-A User's Manual
(Supplied with IE-780948-SL-EM1)	(Included in IE-780948-SL-EM1)	(Supplied with IE-78001-R-A)
Function Outline	Function Outline	Basic specifications
IE-780948-SL-EM1 Connection Method	IE-780948-SL-EM4 Connection Method	System Configuration
Emulation Board Connection Method	Emulation Probe Connection Method	External Interface Functions

ID78K0 Integrated Debugger User's Manual - Introduction	ID78K0 Integrated Debugger User's Manual - Reference

(Supplied with Integrated Debugger)

Simple Method of Use of IE-78001-R-A	Function Outline Command Descriptions Menu Descriptions

Purpose

The purpose of this manual is to explain the basic functions and proper connection method of the IE-780948-SL-EM1 and IE-780948-SL-EM4.

How to Read This Manual

For an understanding of the basic specification
→ Read **Chapter 1 "General"**.

When connecting the IE-780948-SL-EM1 and IE-780948-SL-EM4
→ Read **Chapter 2 "Installation Procedure"** and **IE-78001-R-A User's Manual**.

When setting the clock
→ Read **Chapter 4 "Clock Setting".**

Terminology

Terminology used in this manual is explained in the table below.

Term	Meaning
Emulation device	Generic term for the device performing target device emulation in the emulator. Includes the emulation CPU.
Emulation CPU	CPU section executing the user-written program in the emulator.
Target device	The device which is the object of emulation (real chip).
Target program	The program which is the object of debugging (user-written program).
Target system	The system which is the object of debugging (user-created system). Includes the target program and user-created hardware. In a narrower sense, designates the hardware only.

Note: Explanation of an item marked with Note in the text.
Caution: **Information to be particularly noted.**
Remark: Supplementary information.
Procedure: Procedure for connection, setting, etc.

Related Documents

The documents referred to in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document Number	
		Japanese	English
IE-78001-R-A user's manual		Planned	Planned
IE-78001-R-BK user's manual		Planned	Planned
IE-780948-SL-EM1, IE-780948-SL-EM4 user's manual		—	This manual
EP-100GF-SL user's manual		TEMPU-2093	TEMPU-2093
Flashpro programmer user's manual		—	—
ID78K0 integrated debugger user's manual	Introduction	U11649J	—
PC-9800 series (MS-DOS™) base	Reference	U11151J	—
ID78K0 integrated debugger user's manual	Introduction	U11649J	U11649E
IBM PC/AT™ (PC DOS™) base	Reference	U11539J	U11539E

Caution: These documents are subject to change without notice. Be sure to use the latest documents when you design your system.

Contents

1. General

The IE-780948-SL-EM1 is an emulation board for use with the IE-78001-R-A development system for 78K/0 series 8-bit single-chip microcontroller. Combination of this board with the separately available IE-78001-R-A and emulation probe allows efficient emulation of the subseries of μPD780948. The emulation probe with 100 pin GF package target adapter is connected to the probe board (IE-780948-SL-EM4), which is connected to the emulation board (IE-780948-SL-EM1).

1.1 Features

Connecting the IE-780948-SL-EM1 and IE-780948-SL-EM4 to the IE-78001-R-A offers the following features:

(1) Target device peripheral functions (I/O ports, etc.) can be emulated.
(2) I/O port statuses during emulation can be traced.

1.2 IE-780948-SL-EM1 Components

The IE-780948-SL-EM1 comprises the following components. Please check that all these items are included in the package.

(1)	IE-780948-SL-EM1	x 1
(2)	Part holders (with cover)	x 2
(3)	Screws	x 4
(4)	Registration Card	x 1
(5)	Readme First	x 1
(6)	Floppy Disk with Device File and FPGA Data	x 1
(7)	User's Manual (this manual)	x 1
(8)	List of Attachment	x 1

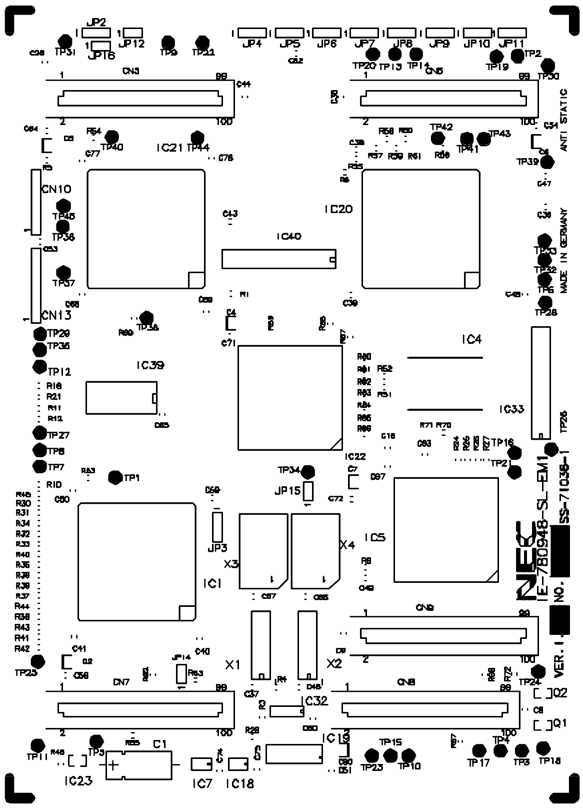
1.3 IE-780948-SL-EM4 Components

The IE-780948-SL-EM4 comprises the following components. Please check that all these items are included in the package.

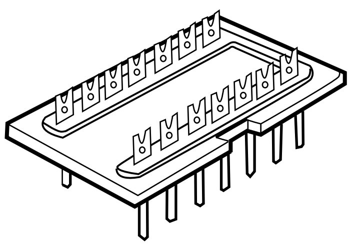
(1)	IE-780948-SL-EM4	x 4
(2)	Screws	x 4
(3)	Registration Card	x 1
(4)	Readme First	x 1
(5)	List of Attachment	x 1

Figure 1-1: IE-780948-SL-EM1 Components

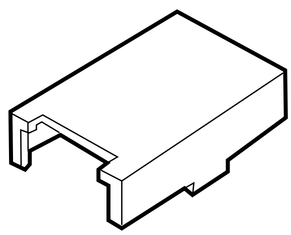
(1) IE-780948-SL-EM1



(2) Parts Holder Note

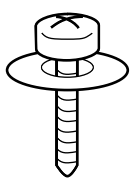


Parts Holder Cover



Note: The actual parts holder is supplied with the cover shown on the right fitted.

(3) Screw



(4) User's Manual (This Manual)

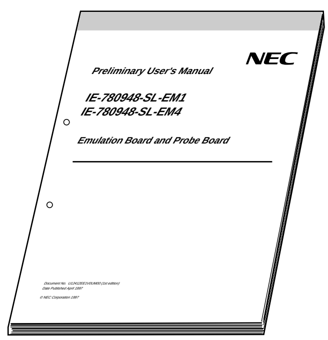
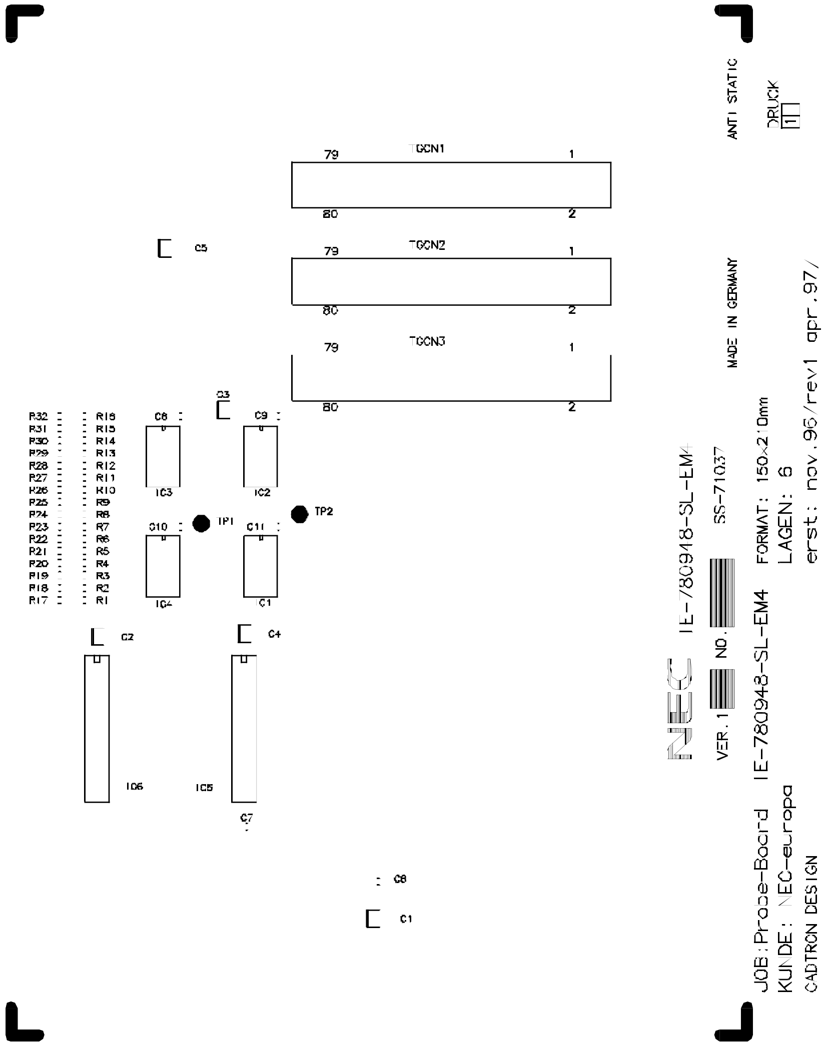
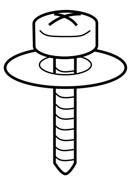


Figure 1-2: IE-780948-SL-EM4 Components

(1) IE-780948-SL-EM4



(2) Screw



1.4 External View and Part Names

Figure 1-3: IE-780948-SL-EM1 External View and Part Names

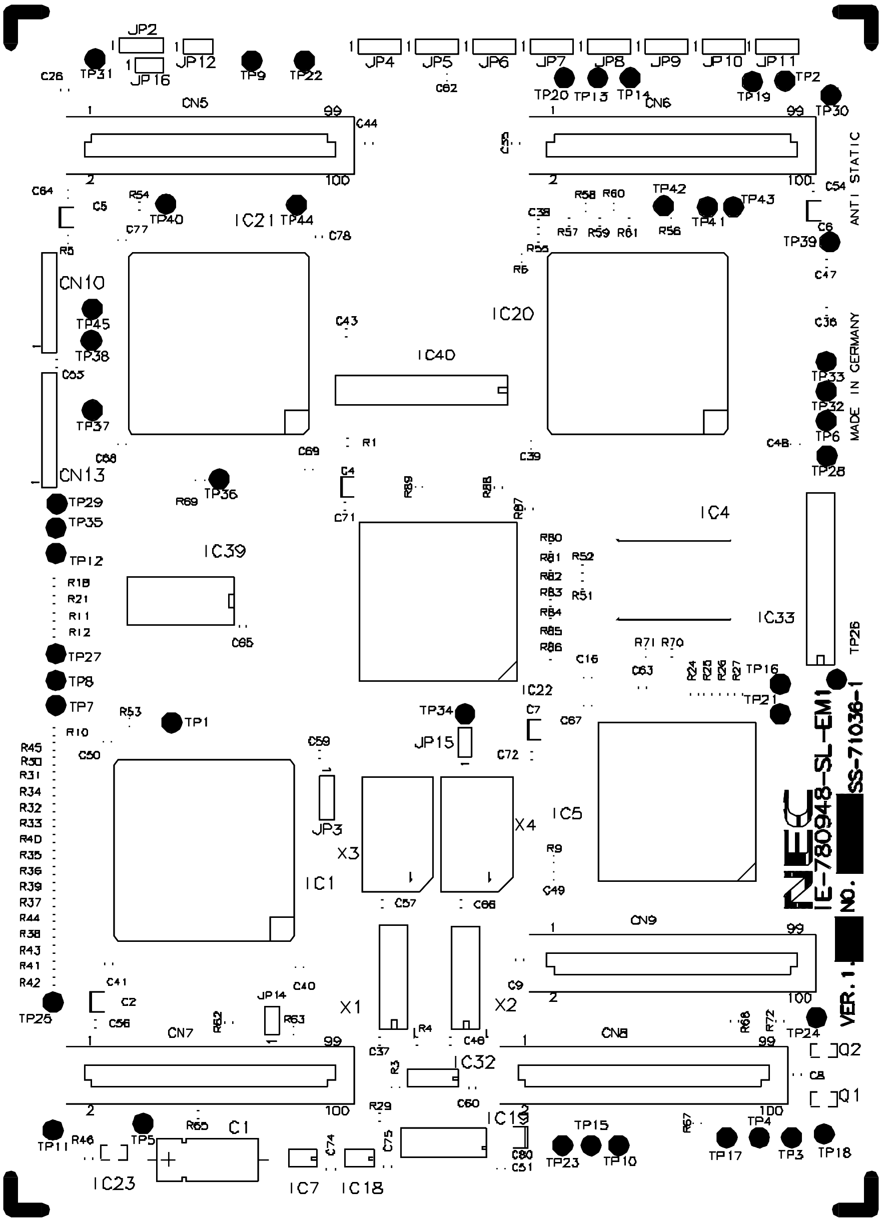


Figure 1-4: IE-780948-SL-EM4 External View and Part Names

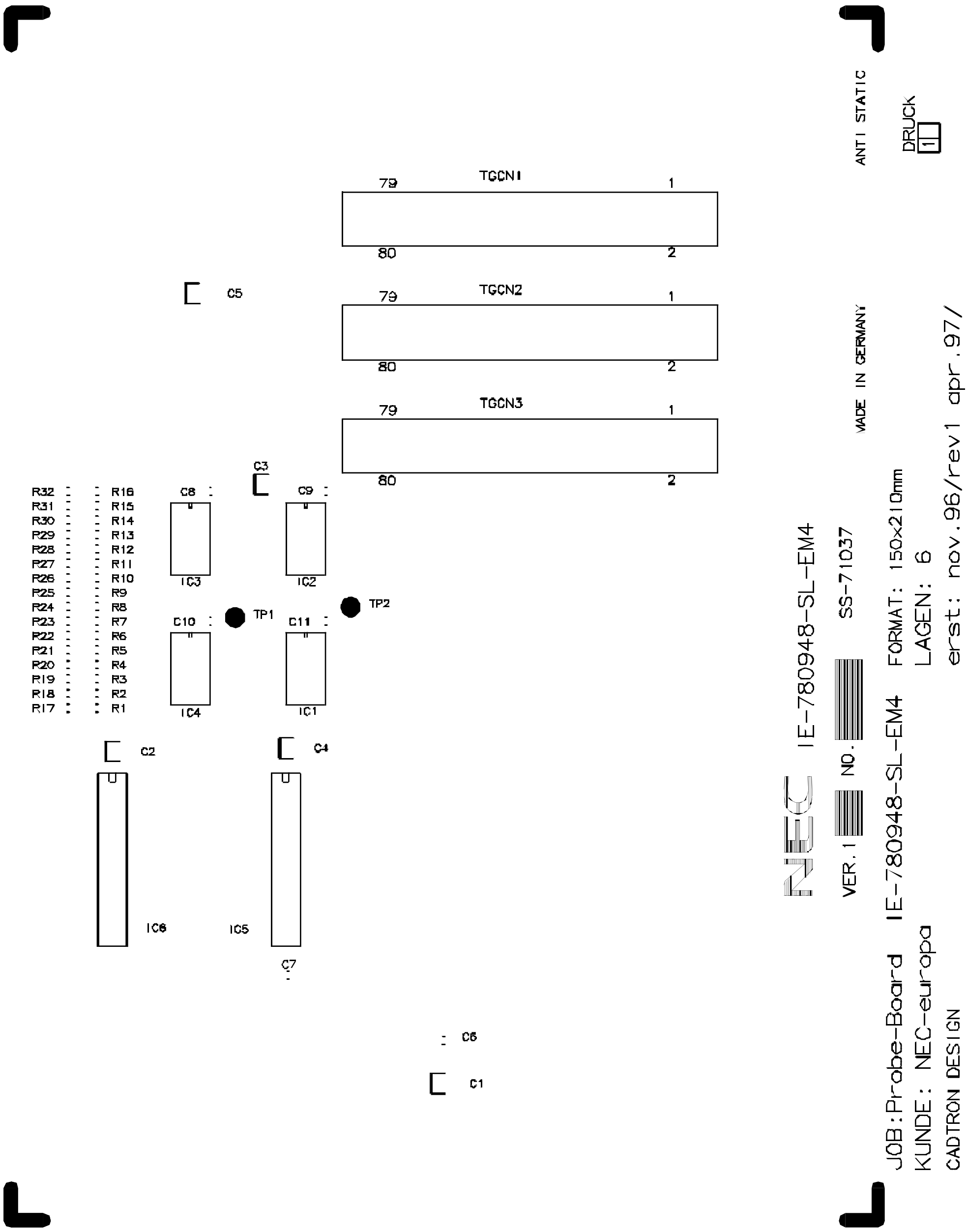


Table 1-1: Names of IE-780948-SL-EM1 and IE-780948-SL-EM4 Parts

Name	Description (IE-780948-SL-EM1)	Name	Description (IE-780948-SL-EM4)
CN1	Break board (IE-78001-R-BK) connectors	CN5	Emulation board connectors (IE-780948-SL-EM1)
CN2		CN6	
CN3		CN7	
CN4		CN8	
CN5	Probe board connectors (IE-780948-SL-EM4)	CN9	
CN6		TGCN1	Probe connector (EP-100GF-SL)
CN7		TGCN2	
CN8		TGCN3	
CN9			
CN10	FPGA download cable connector (only for internal use by NEC)		
CN13	JTAG connector of FPGA		
JP2	FPGA mode selection		
JP3	CAN clock selection		
JP12	GND-pin of A/D Converter		
JP16	VCC-pin of A/D Converter		
JP4...JP11	Port 5 connection		
JP14	LVREF1		
JP15	LVREF0		

1.5 Target Devices

Target devices for which emulation is possible using the IE-78001-R-A in conjunction with the IE-780948-SL-EM1 are shown below. The names of the device files to be installed in development of each product and the names of the CPU series to be input when starting the integrated debugger (ID78K0) are also shown.

Table 1-2: Target Device

Target Device		Device File[Note]	Series CPU Name
µPD780948 subseries	µPD780948, µPD78F0948	DF0948.78K	780948

Note: Sold separately.

1.6 Emulation Probes

Emulation probes are sold separately.
The appropriate probe should be used for the target device package.

Table 1-3: Emulation Probes and Target Devices

Emulation Probe	Package	Target Device
EP-100GF-SL	100-pin plastic QFP (14 x 20 mm)	µPD780948GF-xxx-3BA µPD78F0948GF-xxx-3BA

1.7 Notes on Use of IE-780948-SL-EM1 and IE-780948-SL-EM4

(1) Ensure that the power supply for the IE-78001-R-A and the target system is OFF before connecting or disconnecting to/from the IE-78001-R-A and the target device, or changing switch settings, etc.

(2) When carrying out target device emulation using the IE-780948-SL-EM1 and IE-780948-SL-EM4 in conjunction with the IE-78001-R-A, there are certain differences from the operation of the actual device (see **Chapter 3 Differences from Target Device**).

(3) The emulation probe earth clip must be connected to the signal ground line of the target system (please refer to TEMPU-2093).

(4) The target system V_{DD} must be between 4.5 V and 5.5 V.

(5) The power must be turned on for the IE-78001-R-A first, then target system, and turned off for the target system first, then IE-78001-R-A.

[Memo]

2. Installation Procedure

This chapter describes the procedure for connecting the following items to the IE-780948-SL-EM1 and IE-780948-SL-EM4 and setting up the 78K/0 series development system.

- The break board (IE-78001-R-BK) installed in the IE-78001-R-A
- The emulation board (IE-780948-SL-EM1) installed on the break board (IE-78001-R-BK)
- The probe board (IE-780948-SL-EM4) installed on the emulation board (IE-780948-SL-EM1)
- The emulation probe (EP-100GF-SL)

The power supply for the IE-78001-R-A and the target system must be OFF when connecting or disconnecting any item.

For the method of connecting the emulation probe and target system, see user’s manuals for each emulation probe.

This chapter includes a description which jumper has to be set for using special clocks.

The connection of the IE-780948-SL-EM1 and IE-780948-SL-EM4, break board, IE-78001-R-A, is described below.

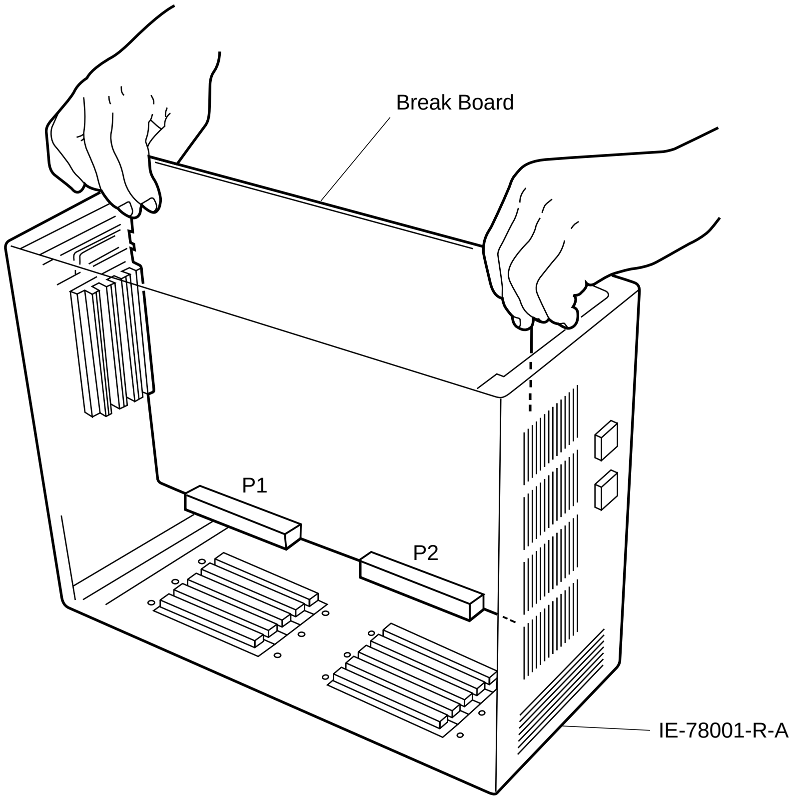
Procedure

<1> Remove the 6 screws in the top of the IE-78001-R-A and open the lid.

<2> Remove the J1 and J2 cables connecting the control/trace board (IE-78001-R-A) and the break board.

<3> Pull forward the card pullers on either side of the break board, and remove the break board from the slot.

Figure 2-1: Removal of Break Board



<4> Set up the break board.

It is necessary to set some jumper and switches on the **break board**. The following tables show the function of each jumper. An example for each jumper setting will be given in **Chapter 4 Clock Setting**.

Jumper JP2 Fixed Internal Main Oscillation Frequency

Table 2-1: Jumper JP2 Fixed Internal Main Oscillation Frequency

Jumper Position	Frequency	Function
(1-2)	20 MHz	Internal clock = 20 MHz
(3-4)	16.77 MHz	Internal clock = 16.77MHz
(5-6)	10 MHz	Internal clock = 10 MHz
(7-8)	8.38 MHz	Internal clock = 8.38 Mhz (**default**)
(9-10)	5 MHz	Internal clock = 5 MHz
(11-12)	4.19 MHz	Internal clock = 4.19 MHz
(13-14)	IOMCK	Fixed clock on IE-780948-SL-EM1 board is used
(15-16)	FLASHCK	Fixed clock on real chip board is used

Jumper JP3

Table 2-2: Usage of Clock Doubler

<table>
<tr><th>Jumper Position</th><th>MCLK</th><th>Usage of clock doubler</th><th>Function</th></tr>
<tr><td>(1-2)</td><td>IF</td><td>Clock doubler of µPD780009 used</td><td>Selection of JP4 (default)</td></tr>
<tr><td>(3-4)</td><td>FPGA</td><td rowspan="2">Clock doubler of µPD780009 not used</td><td>Clock doubler in FPGA (based board)</td></tr>
<tr><td>(5-6)</td><td>FLASH</td><td>Clock doubler in real chip (realchip based board)</td></tr>
</table>

Jumper JP4 Main Clock Selection

Table 2-3: Main Clock Selection

Jumper Position	Main Clock	Function
(1-2)	AUTO	Clock is selected by software (**default**)
(3-4)	CLK I	Clock is selected by JP2
(5-6)	CLK U	User clock is used (from target **or** parts holder on emulation board ref.Chapter 4)

Jumper JP5 Subclock Selection

Table 2-4: Subclock Selection

Jumper Position	Subclock	Function
(1-2)	IOSCK	Internal subclock (IOSCK)
(3-4)	URSCK	User clock is used (from target **or** parts holder on emulation board ref.Chapter 4)
(5-6)	32 kHz	32 kHz subclock (break board) (**default**)

Jumper JP24 FPGA Load Mode

Table 2-5: Downloading Selection

Jumper Position	Function
SERIAL LOAD	Loading FPGA data via serial connector on the BK-board (**default**)
SVLOD	Loading FPGA data via device file

For downloading see Appendix E Downloading Procedure.

Switch SW1 Voltage Selection

Table 2-6: Voltage Selection

Switch Position	Function
IE	Internal voltage from IE is used (only 5V from IE) (**default**)
USR	Target system power supply is used (variable voltage from target)

There are eight different ways to generate the main clock for the IE. The following table describes the settings of the BK board and the emulation board.

Table 2-7: Clock Selections

Main system clock frequency	Setting clock on ID configuration	IE-78001-R-BK	IE-780948-SL-EM1
4.19 Mhz: BK Board Clock	Internal	JP2: short11-12 JP3: short 1-2 JP4: short 1-2	Don’t care
5 Mhz: BK Board Clock	Internal	JP2: short 9-10 JP3: short 1-2 JP4: short 1-2	Don’t care
8.38 Mhz: BK Board Clock	Internal	JP2: short 7-8 JP3: short 1-2 JP4: short 1-2	Don’t care
10 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 5-6 JP3: short 1-2 JP4: short 1-2	Don’t care
16.77 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 3-4 JP3: short 1-2 JP4: short 1-2	Don’t care
20 Mhz: BK Board Clock (not allowed)	Internal	JP2: short 1-2 JP3: short 1-2 JP4: short 1-2	Don’t care
Clock on Emulation Board (parts holder)	External	JP2: don’t care JP3: short 1-2 JP4: short 5-6	Please refer to chapter 4
Clock on Target Board (user hardware)	External	JP2: don’t care JP3: short 1-2 JP4: short 5-6	Please refer to chapter 4

<5> When a user clock is used, mount the main system clock to the emulation board and the subsystem clock to the emulation board too, using a parts holder (See **Chapter 4 Clock Setting**).

<6> Setup the emulation board

It is necessary to set some jumper and switches on the **emulation board**. The following tables describe the function of each jumper.

FPGA Mode Selection

There are two ways of loading the FPGAs. In the normal condition (i.e. config. of FPGAs in IE emulation mode) the FPGAs get their data in the IE which is connected with a PC via RS-232C cable, parallel cable with PC Interface card or ethernet. For test operations it is possible to load the FPGAs via download cable from PC (only used by NEC). The Jumper JP2 selects one of these modes. The connector for the download cable is described in chapter 3.2.1 (connector CN10) (refer Appendix Downloading FPGA Data using IE-78001-R-A configuration).

Table 2-8: FPGA Mode Selection

Jumper JP2

Jumper Position	M_FPGA3(1)	Function
(1-2)	VCC	Reserved
(2-3)	GND	Asynchronous Peripheral Mode (FPGA's are loaded by IE) (**default**)

CAN Clock Selection

Normally the CAN CLK is driven by the main clock of the CPU. If it is necessary to reduce the frequency of the main clock you need an external 8 Mhz oscillator to guarantee the maximum speed on the CAN-Bus. The selection is made by Jumper JP3.

Table 2-9: CAN Clock Selection

Jumper JP3

Jumper Position	CAN-CLK (prs0)	Function
(1-2)	8 Mhz (ext.)	The dcan-module is connected to an external oscillator with 8 MHz
(2-3)	(int.)	The dcan-module is connected to the internal clock (**default**)

Ground Voltage Pin of AD-Converter

Table 2-10: Ground Voltage Pin of AD-Converter

Jumper JP12

Jumper Position	AAVSS	Function
open	target	Connected to selected ground base
closed	GND	Internal digital ground (**default**)

VCC Voltage Pin of AD-Converter

Table 2-11: VCC Voltage Pin of AD-Converter

Jumper JP16

Jumper Position	AAREF0	Function
open	target	Connected to selected ground base
closed	VCC	Internal digital VCC (**default**)

Special Features of Port 5

Port 4, 5 and some signals (4..7) from Port 6 are used for external Device Expansion. To avoid complication using external memory it is possible to connect the Port P5 directly to the I/O Pins. In the other way this pins are shared with the LCD-controller by using an external analog switch.

Table 2-12: Special Features of Port 5

Jumper JP(4..11)

Jumper Position	SW(32..39)	Function
(1-2)	P5(7..0)	Port 5 directly connected with the probe (without LCD and switch)
(2-3)	JSW(32..39)	Port 5 and LCD (switch) connected with probe (**default**)

JP14 Voltage Setting

Table 2-13: JP14 Voltage Setting

Jumper Position		Function
OPEN	LV_{REF1}	LV_{REF1} not connected with LV_{DD}
CLOSED	LV_{DD}	LV_{REF1} connected with LV_{DD} (**default**)

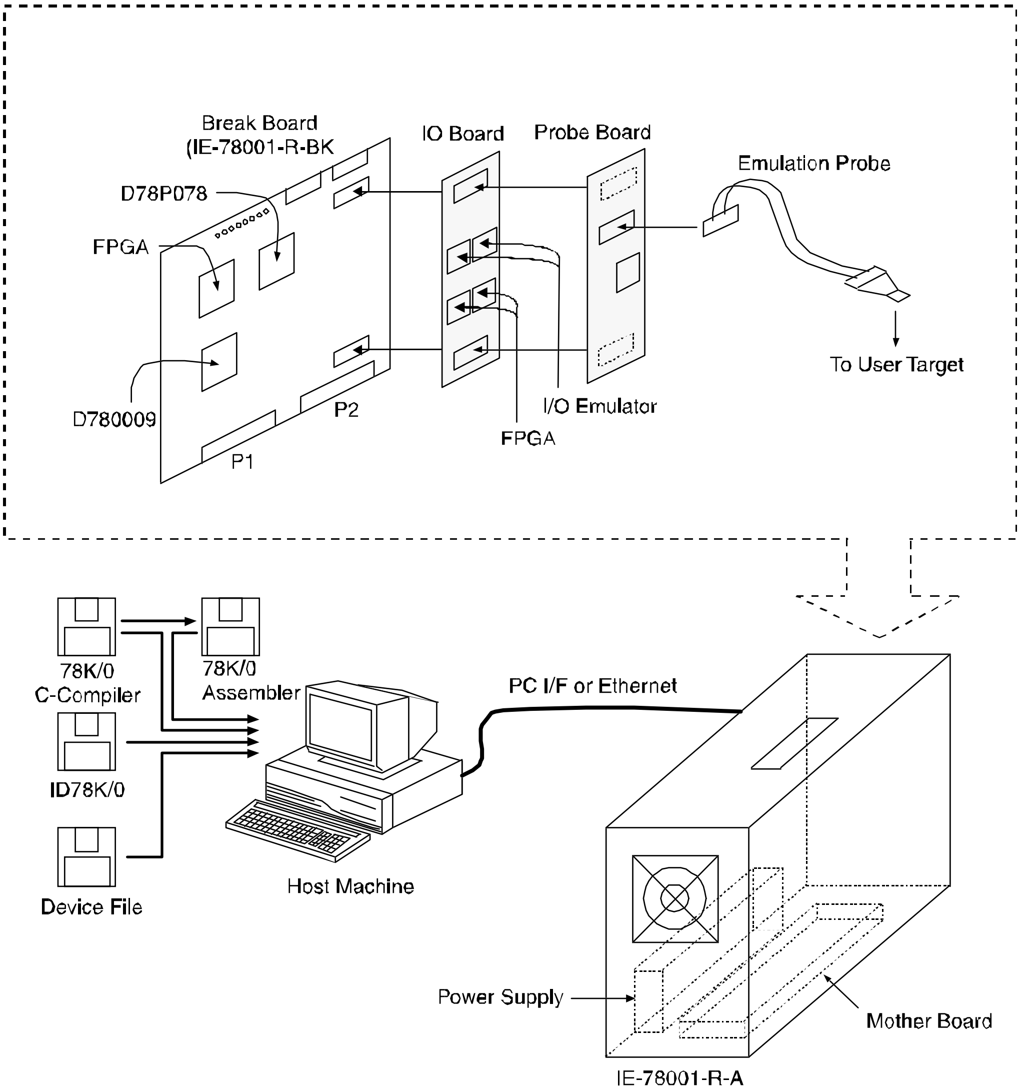
JP15 Voltage Setting

Table 2-14: JP15 Voltage Setting

Jumper Position		Function
OPEN	LV_{REF0}	LV_{REF0} not connected with LV_{DD}
CLOSED	LV_{DD}	LV_{REF0} connected with LV_{DD} (**default**)

<6> Connect all boards to the mother-board slots in the IE-78001-R-A housing (the break board in the 2nd slot from the right).
<7> Re-connect the J1 and J2 cables in their original positions.
<8> Check the position of the boards, then close the lid.

Figure 2-2: Connections of Boards



Break Board	IE-78001-R-BK
I/O Board	IE-780948-SL-EM1
Probe Board	IE-780948-SL-EM4
Emulation Probe	EP-100GF-SL
Device File	D0948.78K / DF0948.78K

[Memo]

3. Differences from Target Device

When target device emulation is performed using the IE-780948-SL-EM1 and IE-780948-SL-EM4 in conjunction with the IE-78001-R-A, there are certain differences from the operation of the actual target device. These differences are described in this chapter.

3.1 Differences in Port Functions

(1) Port 13 and 14 of the device are a normal CMOS inputs with no hysteresis. The emulator has pins with hysteresis.

(2) The LCD-segment signals S0-S39 are in/out ports of type 17A/17B at the device. The emulator drives these signals by an analog switch.

3.1.1 Port related Signals

Figure 3-1: Port 0, Port 1 (digital), Port 2, Port 3 (without 3.4), Port 4, Port 6

Figure 3-2: Port 3.4

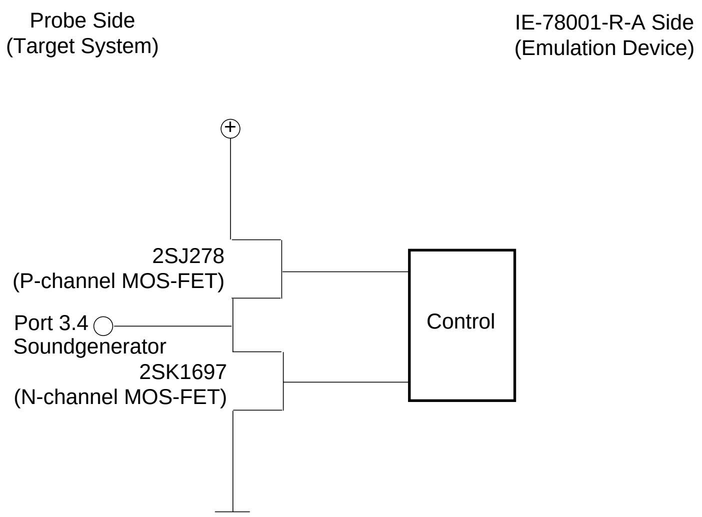


Figure 3-3: Port 5

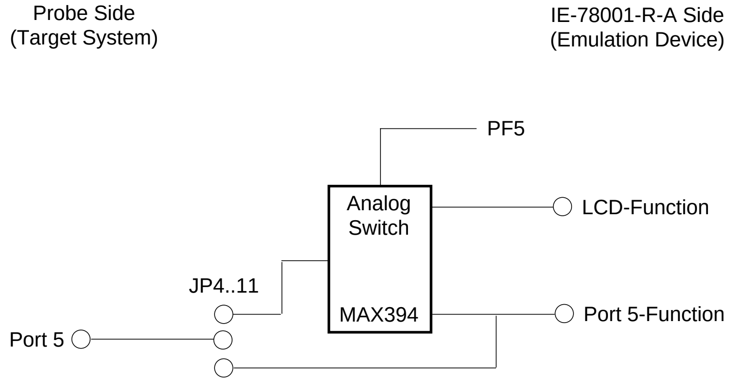
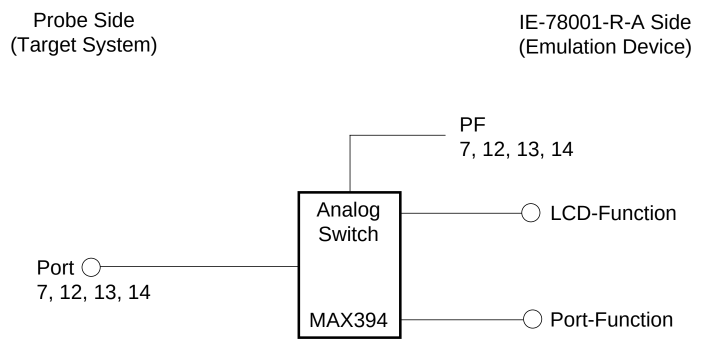
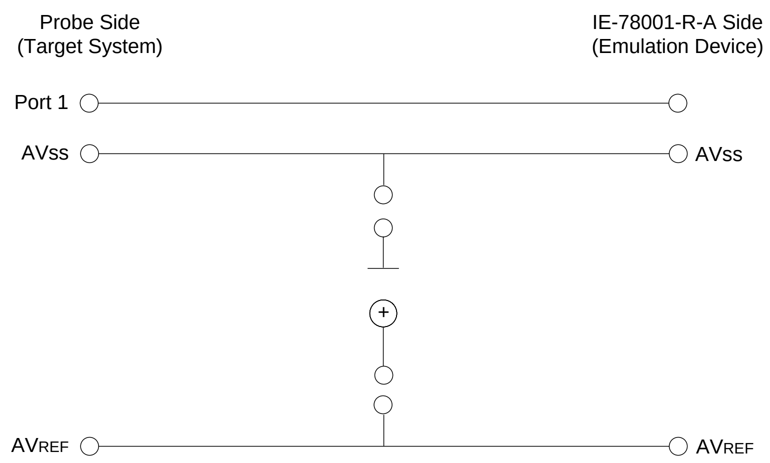


Figure 3-4: Port 7, 12, 13, 14



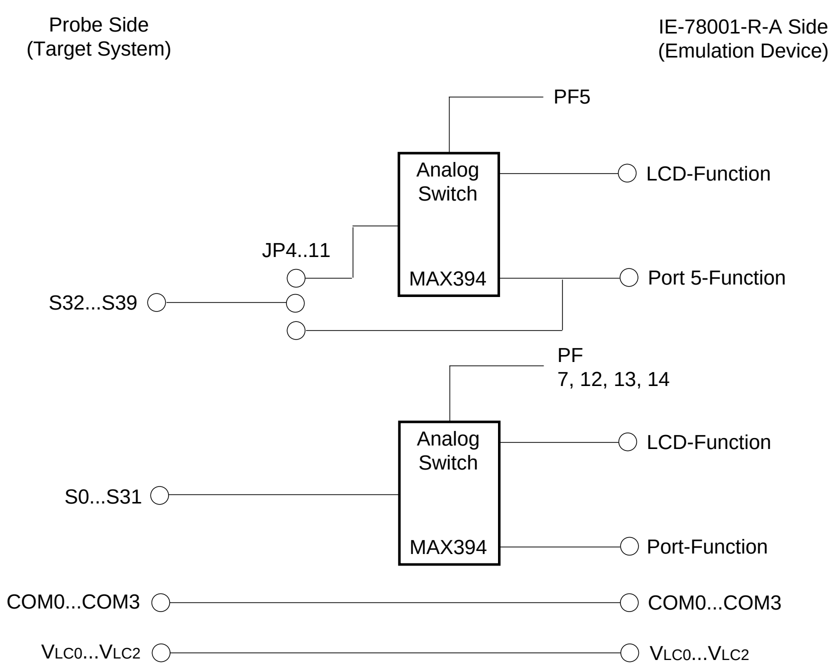
3.1.2 Analog related Signals

Figure 3-5: Analog related Signals



3.1.3 LCD related Signals

Figure 3-6: LCD related Signals

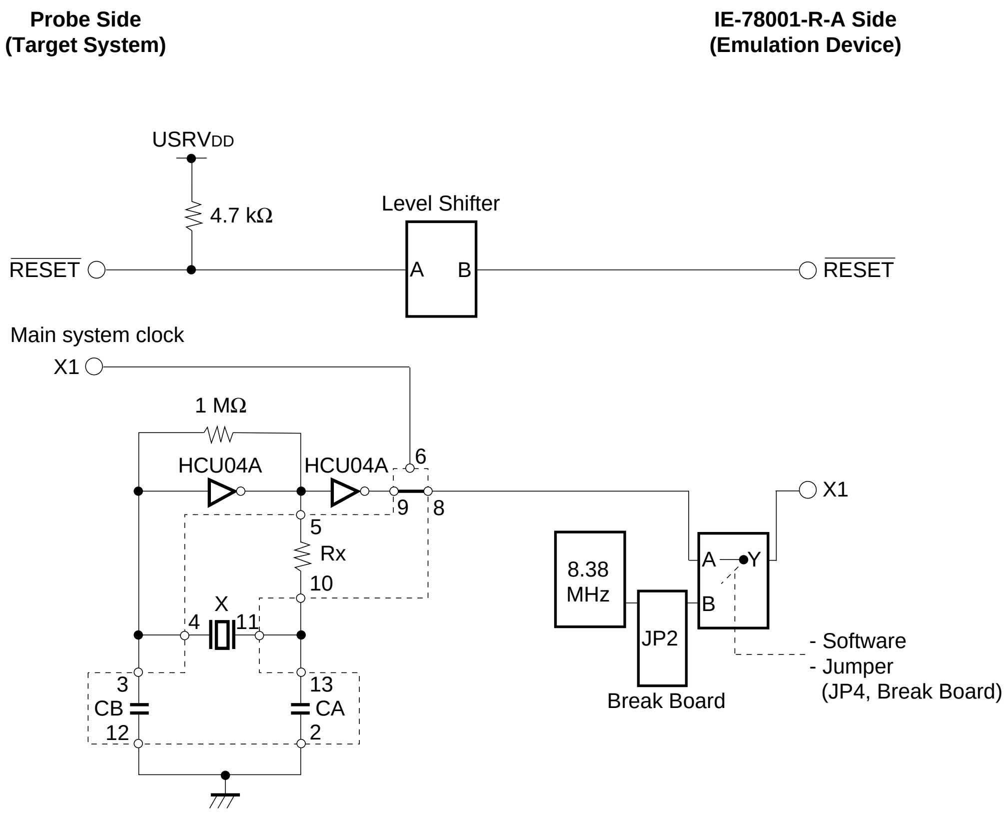


3.1.4 Circuits which input Signals to/from Emulation Device

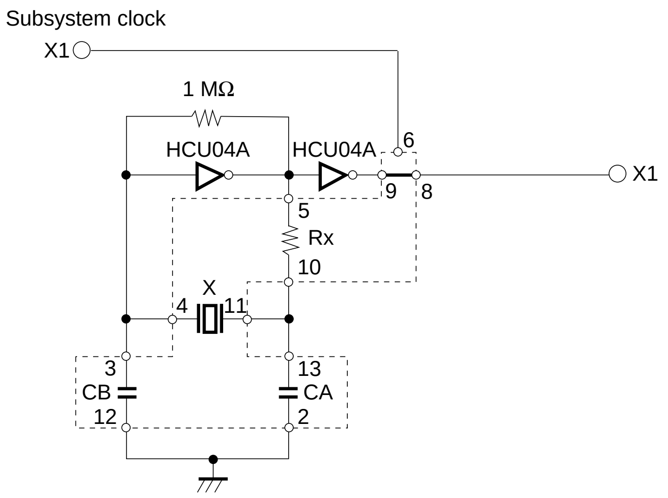
These circuits interface the following signals:

- $\overline{\text{RESET}}$ signal
- Clock input related signals

Figure 3-7: Emulation Circuit Equivalent Circuit Diagram



Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.



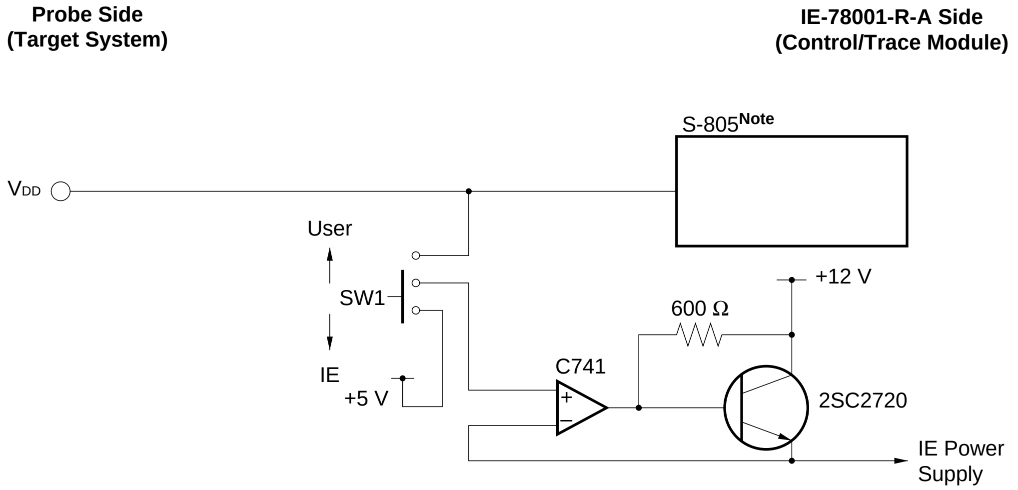
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

3.1.5 Circuits which input Signals to Control/Trace Module

These circuit interfaces the following signals:

- V_{DD} signal

Figure 3-8: Emulation Circuit Equivalent Circuit Diagram



Note: The S-805 is an IC manufactured by Seiko Electronics Industries, Inc.

3.2 Differences in SFR-Registers

Caution: **1. The emulator has a register to emulate the powerfail detection which is not existing at the real chip. The name of the register is DAM0 (SFR-Adr: 0xFF9C). This register has to be set to the value 0x01 by the user-program.**

2. The emulator has a register for the emulation of the LCD-function. The name of the register is LCDTM (SFR-Adr: 0xFF4A). This register has to be set to the value 0x02 by the user-program.

3.3 Target Interface Circuit

The purpose of the target interface circuit is to have the same operations as the target device performed in the IE-78001-R-A. It comprises the emulation device and various gates (CMOS, TTL and other ICs).

When debugging is performed with the target system connected to the IE-78001-R-A, the IE-78001-R-A target interface circuit performs emulation as though the actual target device were operating in the target system.

The target device has a CMOS LSI configuration. The target interface circuit emulation device also has a CMOS LSI configuration, and is virtually identical to the target device in terms of DC characteristics and AC characteristics (when operating on V_{DD} = 4.5 to 5.0 V).

However, where emulation device signal input/output is performed via gates in the target interface circuit, DC and AC characteristics differ from those of the target device.

In particular, regarding AC characteristics, there is a gate delay time (which differs from gate to gate) each time a gate is passed through.

The above points must be taken into consideration when designing the target system.

Caution: **When the IE-78001-R-A and IE-780948-SL-EM1 and IE-780948-SL-EM4 are connected to the target system, 4.5 to 5.5 V must be supplied as the target system power supply (V_{DD}).**

[Memo]

4. Clock Setting

This chapter describes the clock setting method.

4.1 Outline of Clock Setting

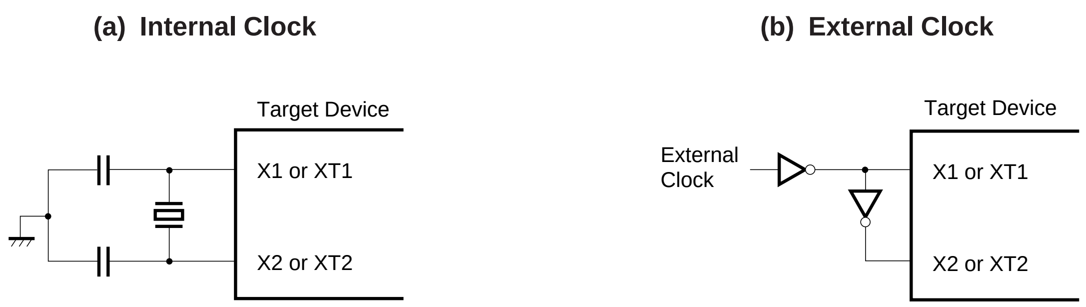
The main system clock for use in debugging can be selected from (1) to (3) below.
The subsystem clock can be selected from (1) to (3), too.

(1) Standard clock offered by the break board
(2) Clock mounted by the user on the emulation board
(3) External clock on the target hardware

If an internal clock is incorporated in the target system, (1) “Clock mounted on the break board” or (2) “Clock mounted by the user” should be selected. An internal clock means the use of an oscillator in the target device with a resonator connected to the target device. The external circuit is shown in Figure 4-1(a). The resonator mounted in the target system is not used during emulation. The clock mounted on the emulation board installed in the IE-78001-R-A is used.

If an external clock is incorporated in the target system, (3) “External clock” should be selected. An external clock means supplying a clock from outside the target device, and the oscillator in the target device is not used. The external circuit is shown in Figure 4-1(b).

Figure 4-1: System Clock Oscillator External Circuit

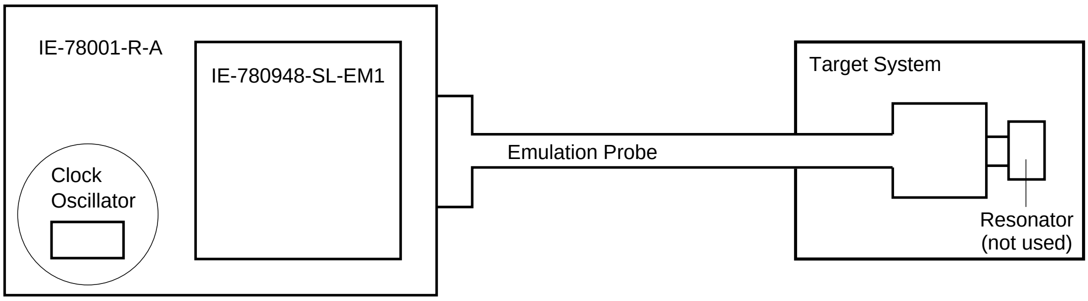


4.1.1 Main System Clock Selections

(1) Standard clock offered by the break board

A crystal oscillator is already mounted on the break board. The frequency is 8.38 MHz.

Figure 4-2: When Using Standard Clock Mounted on Break Board

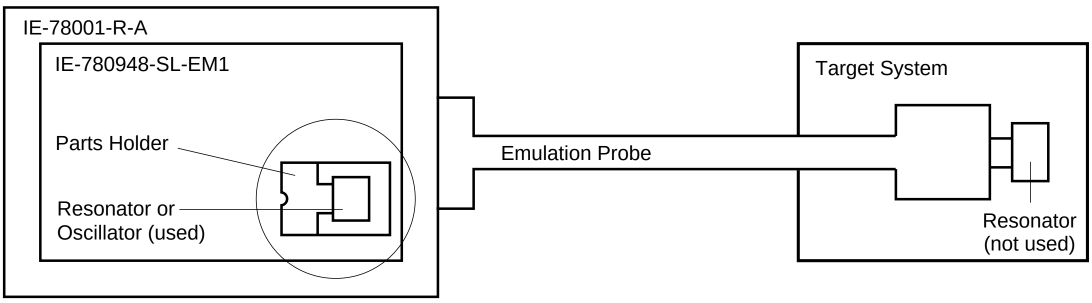


Remark: The clock supplied from the oscillator on the IE-78001-R-BK (circled) is used.

(2) Clock mounted by user on the emulation board

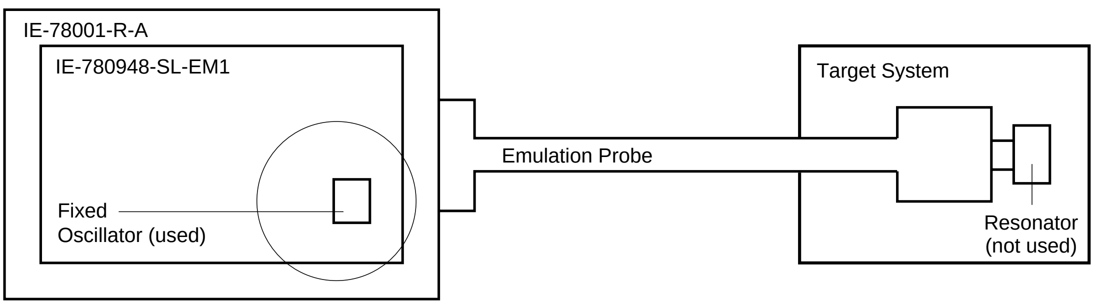
A clock that matches the specifications set by the user can be mounted on the IE-780948-SL-EM1. The resonator or oscillator to be used is mounted on a parts holder and that parts holder is installed on the IE-780948-SL-EM1. This is useful if you want to perform debugging at a different frequency from that of the clock mounted beforehand.

Figure 4-3: When Using Clock Mounted on the Emulation Board



Remark: The clock supplied from the resonator or oscillator on the IE-780948-SL-EM1 (circled) is used.

Figure 4-4: Using a fixed Clock mounted by the User on the Emulation Board

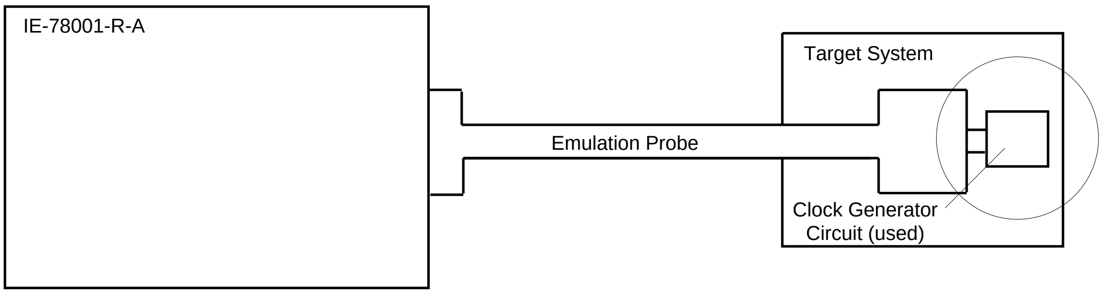


Remark: The clock supplied with the oscillator on the IE-780948 (circled in the above figure) is used.

(3) External clock on the target hardware

The external clock on the target system can be used via an emulation probe.

Figure 4-5: Using an External Clock mounted on the Target Hardware



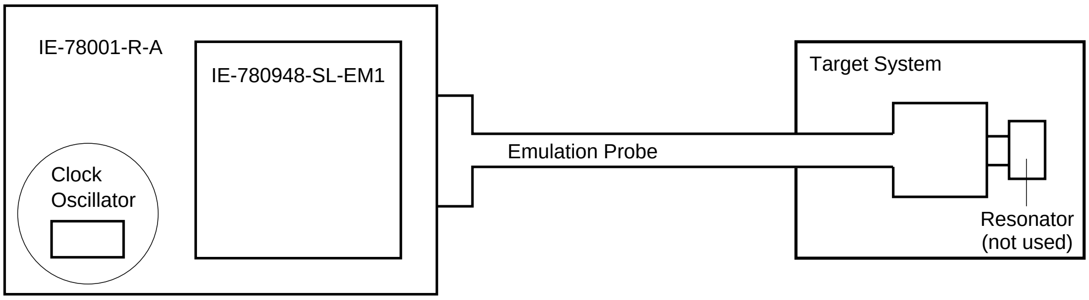
Remark: The clock supplied by the clock generator circuit (circled in the above figure) is used.

4.1.2 Subsystem Clock Selections

(1) Standard clock offered by the break board

A crystal oscillator is already mounted on the break board. The frequency is 32.768 kHz.

Figure 4-6: When Using Standard Clock Mounted on Break Board

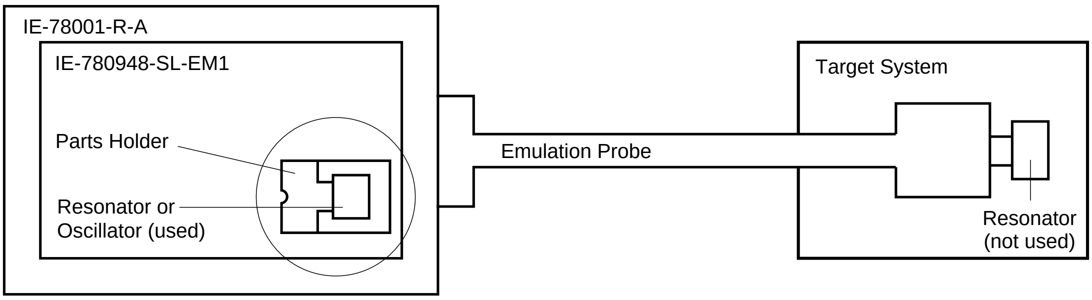


Remark: The clock supplied from the oscillator on the IE-78001-R-BK (circled) is used.

(2) Clock mounted by user on the emulation board

A clock that matches the specifications set by the user can be mounted on the IE-780948-SL-EM1. The resonator or oscillator to be used is mounted on a parts holder and that parts holder is installed on the IE-780948-SL-EM1. This is useful if you want to perform debugging at a different frequency from that of the clock mounted beforehand.

Figure 4-7: When Using Clock Mounted on the Emulation Board

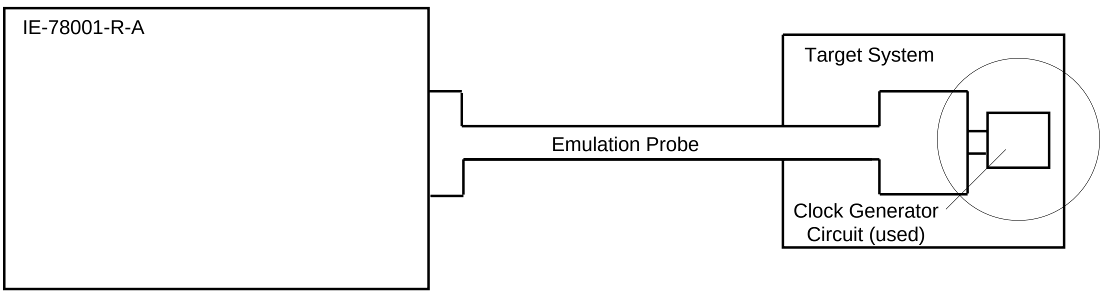


Remark: The clock supplied from the resonator or oscillator on the IE-780948-SL-EM1 (circled) is used.

(3) External clock on the target hardware

The external clock on the target system can be used via an emulation probe.

Figure 4-8: Using an External Clock mounted on the Target Hardware



Remark: The clock supplied by the clock generator circuit (circled in the above figure) is used.

4.2 Main System Clock Setting

It is not necessary to change the parts holder (IC29, X1 (MAIN)) on the breakboard IE-78001-R-BK.

4.2.1 When Using Standard Clock offered by the Break Board

A parts holder, wired as shown in Figure 4-9, is fitted in the X2 socket on the IE-780948-SL-EM1 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

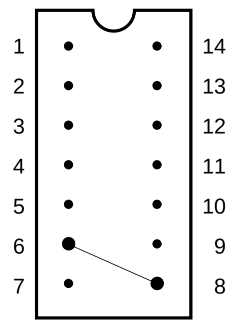
When the integrated debugger (ID78K0) is started, clock should be set to “INTERNAL” in the configuration window clock selection.

Items to be prepared

- Parts holder (IE-7800948-SL-EM1 accessory)
- Lead wire
- Set of soldering tools

Procedure

Figure 4-9: Lead Wiring Diagram (When Clock mounted on Break Board is used as Main System Clock)



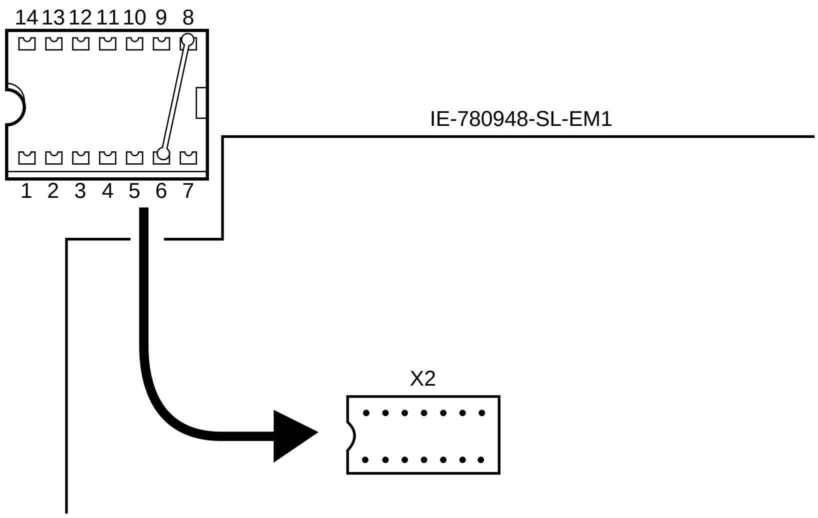
Parts Holder Inter-Pin Numbers
6-8

<1> Check the break board and the IE-780948-SL-EM1.

<2> Insert parts holder in the socket (marked “X2”) on the IE-780948-SL-EM1. Ensure that the pin <1> mark is correctly oriented when inserting the parts holder.

<3> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-9.

Figure 4-10: Parts Holder Mounting Location (When Clock mounted on the Break Board is used as Main System Clock)



<5> Install the IE-780948-SL-EM1 and the other boards in the IE-78001-R-A.

4.2.2 When using Clock mounted by User on the Emulation Board

The settings shown in (1) or (2) below must be performed depending on the type of clock used. When the integrated debugger ID78K0 is started, clock should be selected to “INTERNAL” in the configuration window (clock selection).

(1) When ceramic resonator/crystal resonator is used

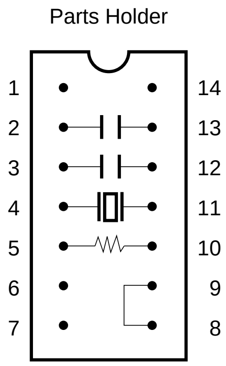
Items to be prepared

- Parts holder (IE-780948-SL-EM1 accessory)
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Set of soldering tools

Procedure

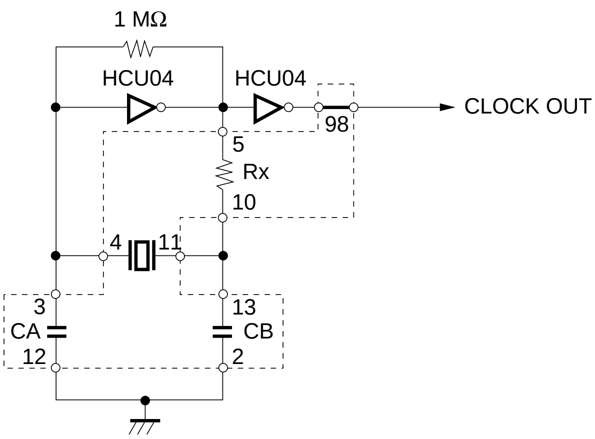
<1> Solder the ceramic resonator or crystal resonator to be used and resistor Rx, capacitor CA and capacitor CB appropriate to the oscillation frequency of the resonator to the parts holder provided as shown below.

Figure 4-11: Soldering of Parts to the Parts Holder



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator/crystal resonator
5-10	Resistor Rx
8-9	Shorted

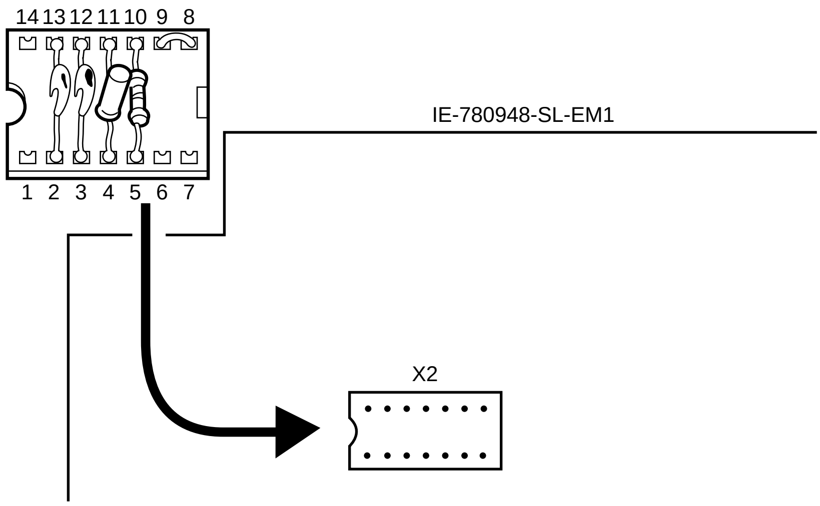
Figure 4-12: Circuit Diagram



Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

<2> Prepare the break board (jumper settings) and the IE-780948-SL-EM1.
<3> Remove the external clock parts holder inserted in the socket (marked "X2") on the IE-780948-SL-EM1.
<4> Insert parts holder <1> in the socket (X2) from which the external clock parts holder was removed in <3>. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

Figure 4-13: Parts Holder Mounting Location (When Clock mounted by User on the Emulation Board is used as Main System Clock)

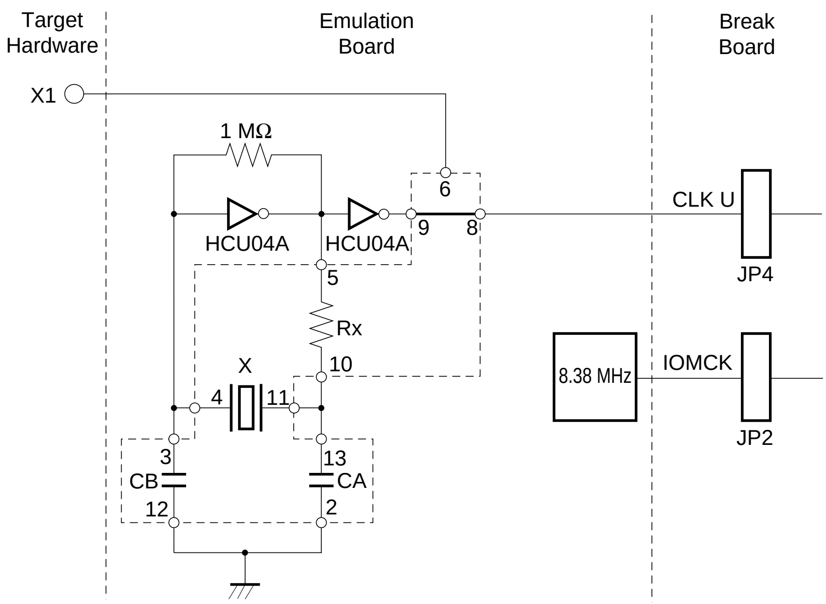


<5> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-5.

<6> Install the IE-780948-SL-EM1 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted resonator.

Figure 4-14: Clock Enabling



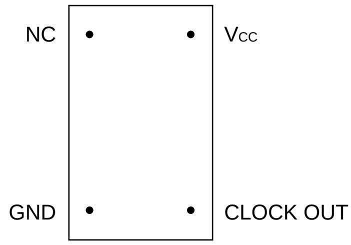
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

(2) When crystal oscillator is used

Items to be prepared

- Crystal oscillator (with pins as shown in Figure 4-15)

Figure 4-15: Crystal Oscillator (When Clock mounted by User on the Emulation Board is used as Main System Clock)



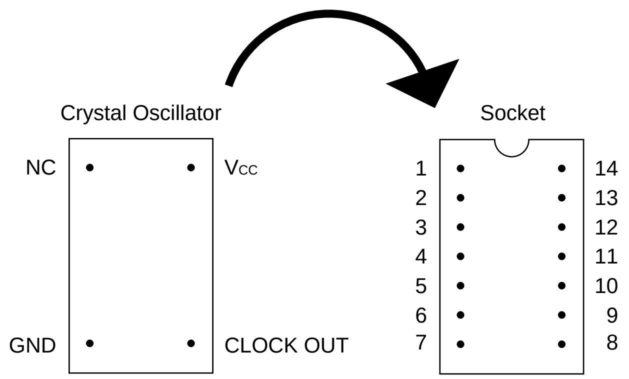
Procedure

<1> Prepare the break board (jumper settings) and the IE-780948-SL-EM1.

<2> Remove the external clock parts holder inserted in the socket (marked “X2”) on the IE-780948-SL-EM1.

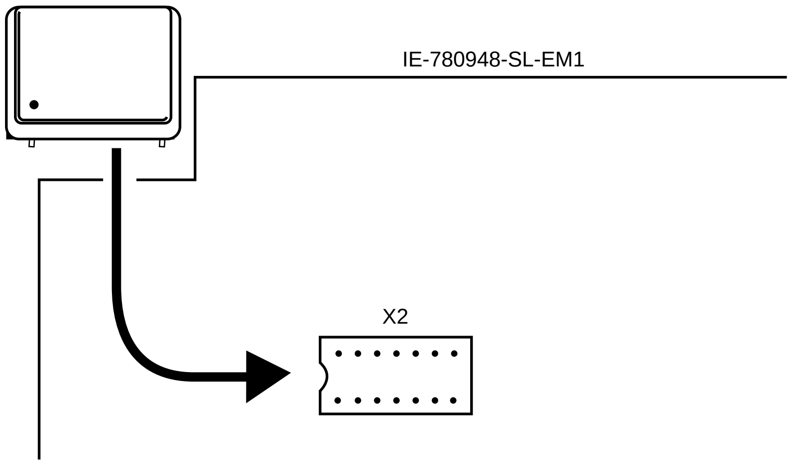
<3> Insert the crystal oscillator in the socket (marked "X2") from which the external clock parts holder was removed in <2>. The crystal oscillator pins should be inserted in the socket holes as shown in Figure 4-16.

Figure 4-16: Insertion of Crystal Oscillator in the Socket



Crystal Oscillator Pin	Socket Hole No.
NC	1
GND	7
CLOCK OUT	8
VCC	14

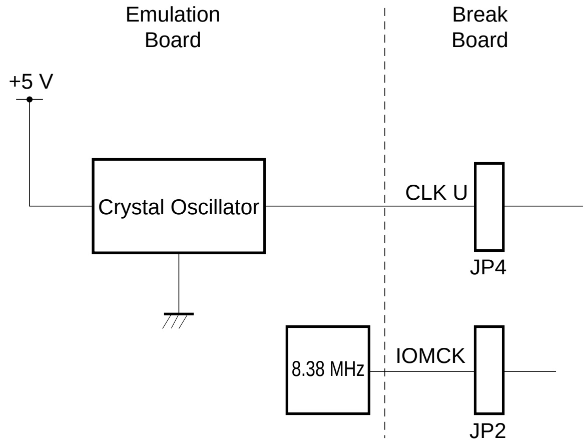
Figure 4-17: Crystal Oscillator Mounting Location (When Clock mounted by User on the Emulation Board is used as Main System Clock)



<4> Confirm that the component mounted on the X1 (MAIN) socket on the break board is wired as shown in Figure 4-5.
<5> Install the IE-780948-SL-EM1 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted oscillator.

Figure 4-18: Clock Enabling



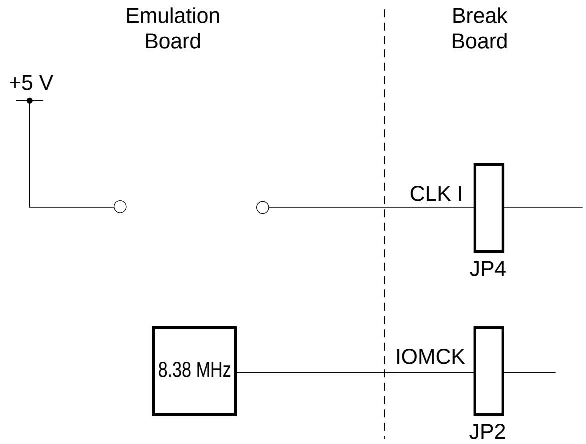
(3) When fixed oscillator on the emulation board is used

Procedure

<1> Prepare the break board (jumper settings).
<2> Confirm that the component mounted on the X1 (main) socket on the break board is wired as shown in Figure 4-5.
<3> Install the IE-780948-SL-EM1 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the oscillator mounted fixed on the emulation board.

Figure 4-19: Fixed Oscillator



4.2.3 When Using External Clock on the Target Hardware

A parts holder, wired as shown in Figure 4-20, is fitted in the X2 socket on the IE-780948-SL-EM1 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

When the integrated debugger ID78K0 is started, clock should be set to "EXTERNAL" in the configuration window (clock selection).

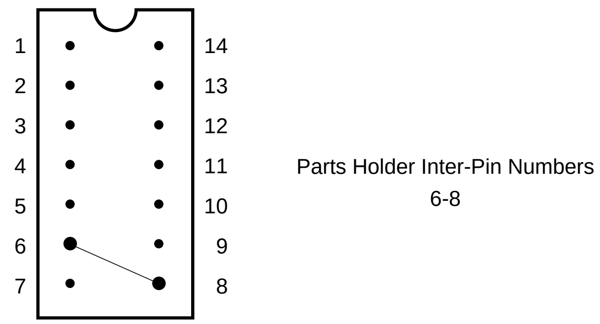
Items to be prepared

- Parts holder (IE-780948-SL-EM1 accessory)
- Lead wire
- Set of soldering tools

Procedure

<1> Solder and wire the parts holder provided with the lead wire.

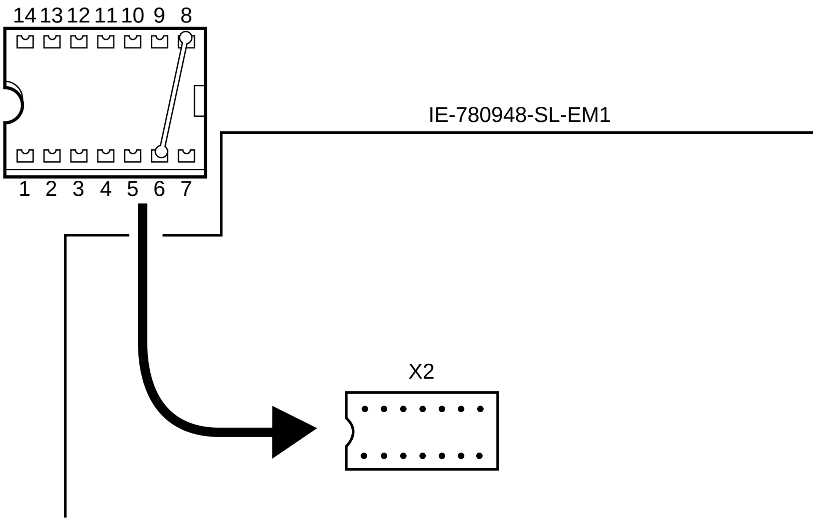
Figure 4-20: Lead Wiring Diagram (When External Clock on the Target Hardware is used as Main System Clock)



<2> Prepare the break board (jumper settings) and the IE-780948-SL-EM1.

<3> Insert parts holder <1> in the socket (marked "X2") on the IE-780948-SL-EM1. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

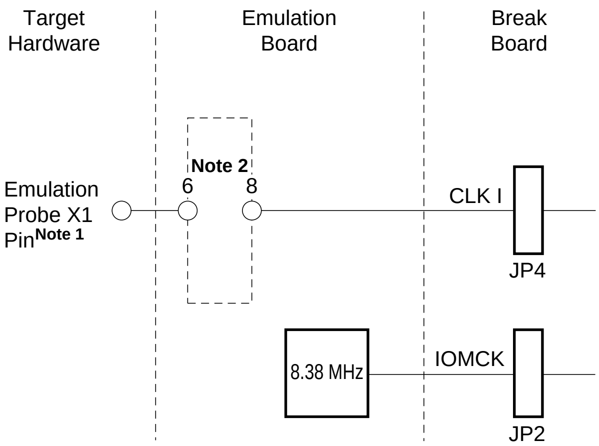
Figure 4-21: Parts Holder Mounting Location (When External Clock on theTarget Hardware is used as Main System Clock)



<4> Confirm that the component mounted on the X1 (MAIN) socket on the break board as well as the IE-780948-SL-EM1 are wired as shown in Figure 4-5.
<5> Install the IE-780948-SL-EM1 and the other boards in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock signal on the target system to be supplied to the emulation device.

Figure 4-22: Clock Enabling



Notes: **1.** Target device pin name
2. Parts holder pin numbers

Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

4.2.4 Examples of Main System Clock Setting

(1) Standard Clock offered by the Break Board

Break Board:	JP2 - Frequency selection
	JP4 - CLK I
Emulation Board:	X2 with shortcut between 6 - 8
ID78K0:	Internal

(2) Clock mounted by the User on the Emulation Board

- User related Clock

Break Board:	JP2 - don't care
	JP4 - CLK U
Emulation Board:	X2 with parts holder and crystal resonator, ceramic resonator or crystal oscillator
ID78K0:	External

- Fixed Clock

Break Board:	JP2 - IOMCK
	JP4 - CLK I
Emulation Board:	don't care
ID78K0:	Internal

(3) External Clock on the Target Hardware

Break Board:	JP2 - don't care
	JP4 - CLK U
Emulation Board:	X2 with shortcut between 6 - 8
ID78K0:	External

4.3 Subystem Clock Setting

It is not necessary to change the parts holder (IC30, X2 (SUB)) on the breakboard IE-78001-R-BK.

4.3.1 When Using Standard Clock offered by the Break Board

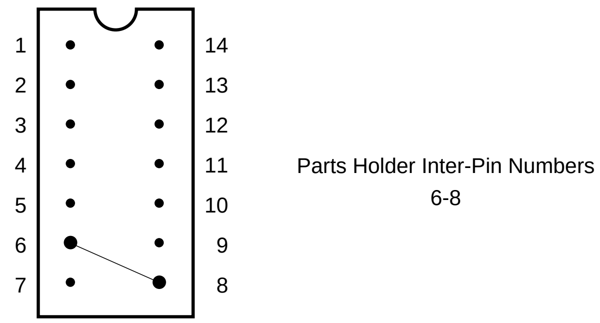
A parts holder, wired as shown in Figure 4-18, is fitted in the X1 (SUB) socket on the IE-780948-SL-EM1 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

Items to be prepared

- Parts holder (IE-7800948-SL-EM1 accessory)
- Lead wire
- Set of soldering tools

Procedure

Figure 4-23: LeadWiring Diagram (When Clock mounted on Break Board is used as Subystem Clock)



<1> Check the break board and the IE-780948-SL-EM1.
<2> Insert parts holder in the socket (marked "X1") on the IE-780948-SL-EM1. Ensure that the pin <1> mark is correctly oriented when inserting the parts holder.
<3> Confirm that the component mounted on the X2 (SUB) socket on the break board as well as the IE-780948-SL-EM1 are wired as shown in Figure 4-5.

4.3.2 When Using Clock Mounted by User on the Emulation Board

The settings shown in (1) or (2) below must be performed depending on the type of clock used.
No particular settings are required on the integrated debugger.

(1) When ceramic resonator/crystal resonator is used

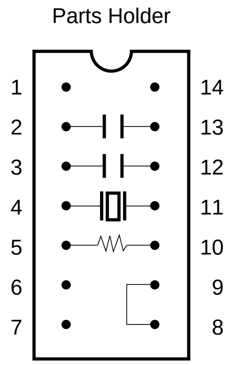
Items to be prepared

- Parts holder (IE-780948-SL-EM1 accessory)
- Ceramic resonator or crystal resonator
- Resistor Rx
- Capacitor CA
- Capacitor CB
- Set of soldering tools

Procedure

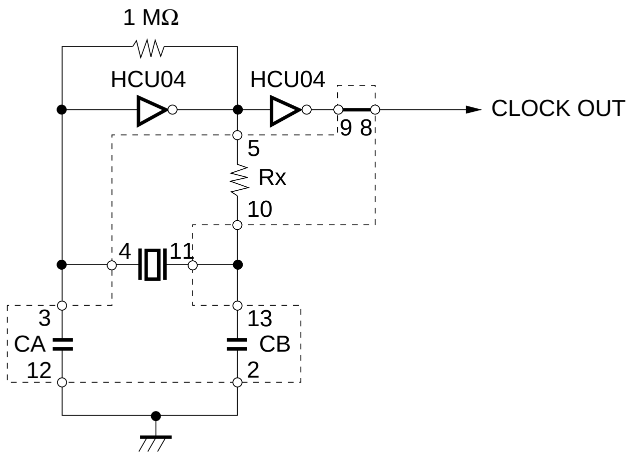
<1> Solder the ceramic resonator or crystal resonator to be used and resistor Rx, capacitor CA and capacitor CB appropriate to the oscillation frequency of the resonator to the parts holder provided as shown below.

Figure 4-24: Lead Wiring Diagram (When Clock mounted by User)



Pin No.	Connection
2-13	Capacitor CB
3-12	Capacitor CA
4-11	Ceramic resonator/crystal resonator
5-10	Resistor Rx
8-9	Shorted

Figure 4-25: Circuit Diagram

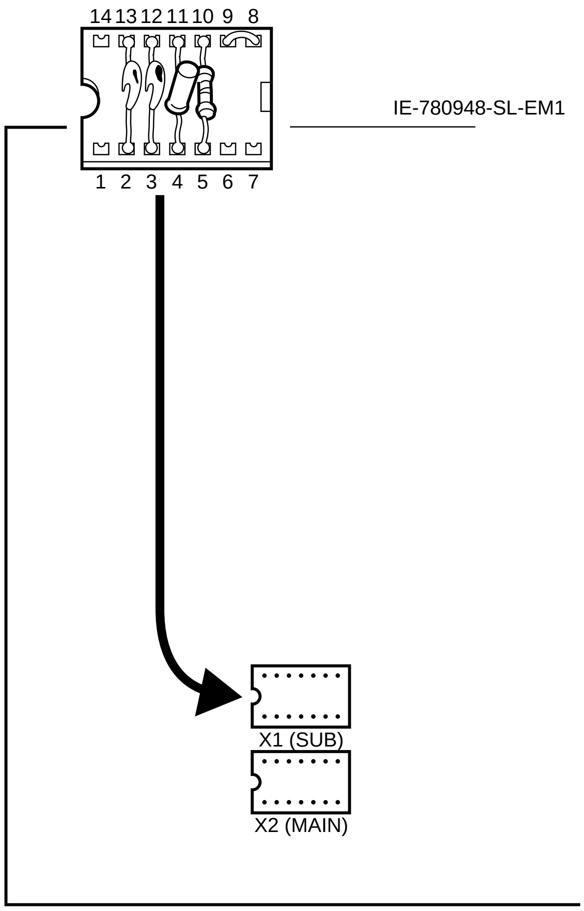


Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

<2> Prepare the break board (jumper settings) and the IE-780948-SL-EM1.

<3> Insert parts holder <1> in the socket X1 from which the external clock parts holder was removed in <3>. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

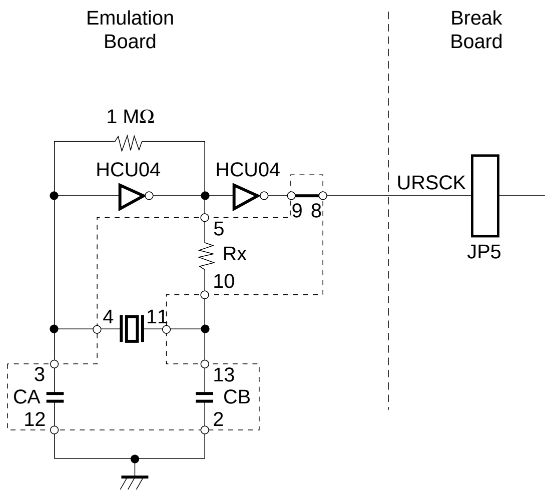
Figure 4-26: Parts Holder Mounting Location (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)



<4> Install the IE-780948-SL-EM1 and the other boards in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted resonator.

Figure 4-27: Clock Enabling



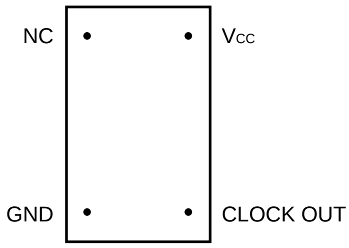
Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

(2) When crystal oscillator is used

Items to be prepared

- Crystal oscillator (with pins as shown in Figure 4-28)

Figure 4-28: Crystal Oscillator (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)

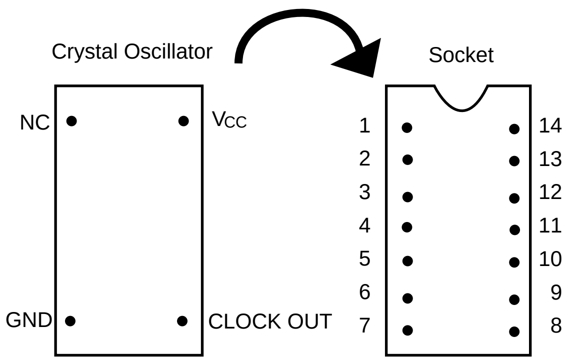


Procedure

<1> Prepare the break board (jumper setting) and the IIE-780948-SL-EM1.

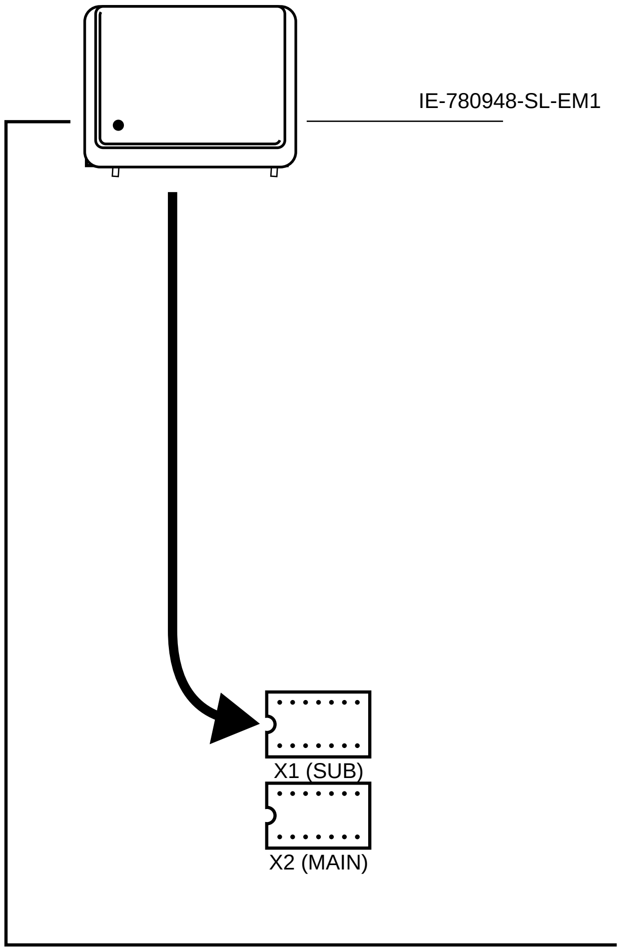
<2> Insert the crystal oscillator in the socket X1 from which the external clock parts holder was removed. The crystal oscillator pins should be inserted in the socket holes as shown in Figure 4-29.

Figure 4-29: Insertion of Crystal Oscillator in the Socket



Crystal Oscillator Pin	Socket Hole No.
NC	1
GND	7
CLOCK OUT	8
V_{CC}	14

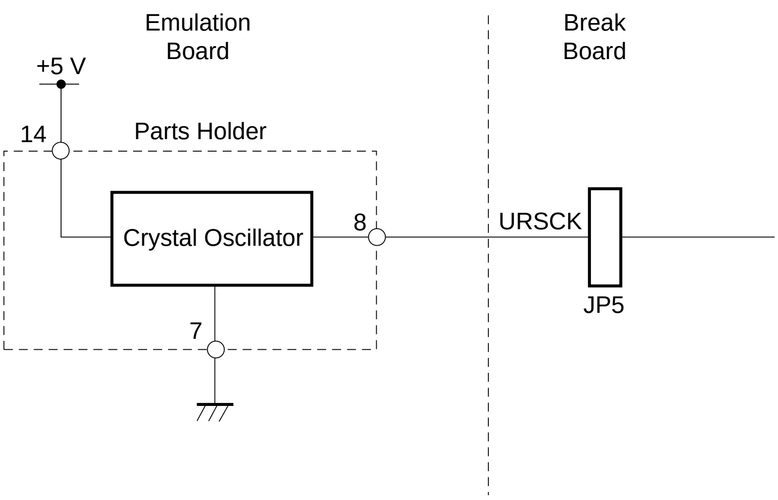
Figure 4-30: Crystal Oscillator Mounting Location (When Clock mounted by User on the Emulation Board is used as Subsystem Clock)



<4> Install the IE-780948-SL-EM1 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock to be supplied to the emulation device from the mounted oscillator.

Figure 4-31: Clock Enabling



4.3.3 When Using External Clock on the Target Hardware

A parts holder, wired as shown in Figure 4-32, is fitted in the X1 socket on the IE-780948-SL-EM1 when the product is shipped. If the parts holder state is the same as when the product was shipped, no particular hardware settings are necessary.

No particular settings are required on the integrated debugger.

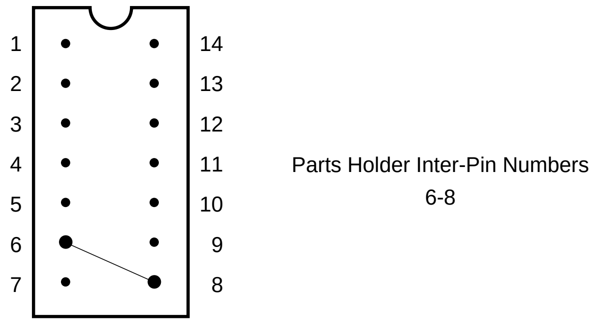
Items to be prepared

- Parts holder (IE-780948-SL-EM1 accessory)
- Lead wire
- Set of soldering tools

Procedure

<1> Solder and wire the parts holder provided with the lead wire.

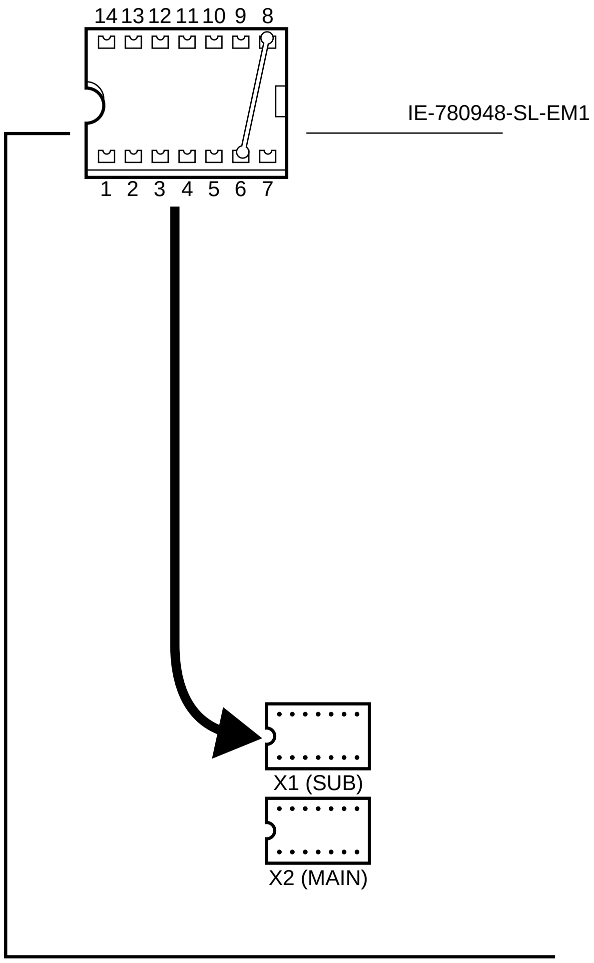
Figure 4-32: Lead Wiring Diagram (When External Clock on the Target Hardware is used as Subsystem Clock)



<2> Prepare the break board (jumper settings) and the IE-780948-SL-EM1.

<3> Insert parts holder <1> in the socket (marked “X1”) on the emulation board. Ensure that the pin 1 mark is correctly oriented when inserting the parts holder.

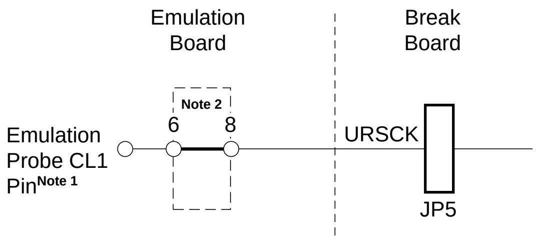
Figure 4-33: Parts Holder Mounting Location (When External Clock on the Target Hardware is used as Subsystem Clock)



<4> Install the IE-780948-SL-EM1 and the other board in the IE-78001-R-A.

The following circuit is configured by means of the above procedure, enabling the clock signal on the target system to be supplied to the emulation device.

Figure 4-34: IE-78001-R-A Side (Emulation Device)



Notes: **1.** Target device pin name
2. Parts holder pin numbers

Remark: The area enclosed by the dotted line is the part of the circuit mounted on the parts holder.

4.3.4 Examples of Subsystem Clock Setting

(1) Standard Clock offered by the Break Board

Break Board: JP5 - 32kHz
Emulation Board: X1 with shortcut between 6 - 8

(2) Clock mounted by the User on the Emulation Board

Break Board: JP5 - URSCK
Emulation Board: X1 with parts holder and crystal resonator, ceramic resonator or crystal oscillator

(3) External Clock on the Target Hardware

Break Board: JP5 - URSCK
Emulation Board: X2 with shortcut between 6 - 8

[Memo]

Appendix A IE-780948-SL-EM1, IE-780948-SL-EM4 Product Specifications

Product name	:	IE-780948-SL-EM1, IE-780948-SL-EM4
Peripheral emulation device	:	μPD780948, 78F0948
Operating temperature	:	0 to 50 °C
Humidity	:	10 to 80% RH (no condensation)
Storage temperature	:	–15 to +60 °C
Power supply	:	Power supply capacity : DC 200mA (MAX.) 1.0 W +5 V

Figure A-1: Printed Wiring Board Dimensions

Emulation Board

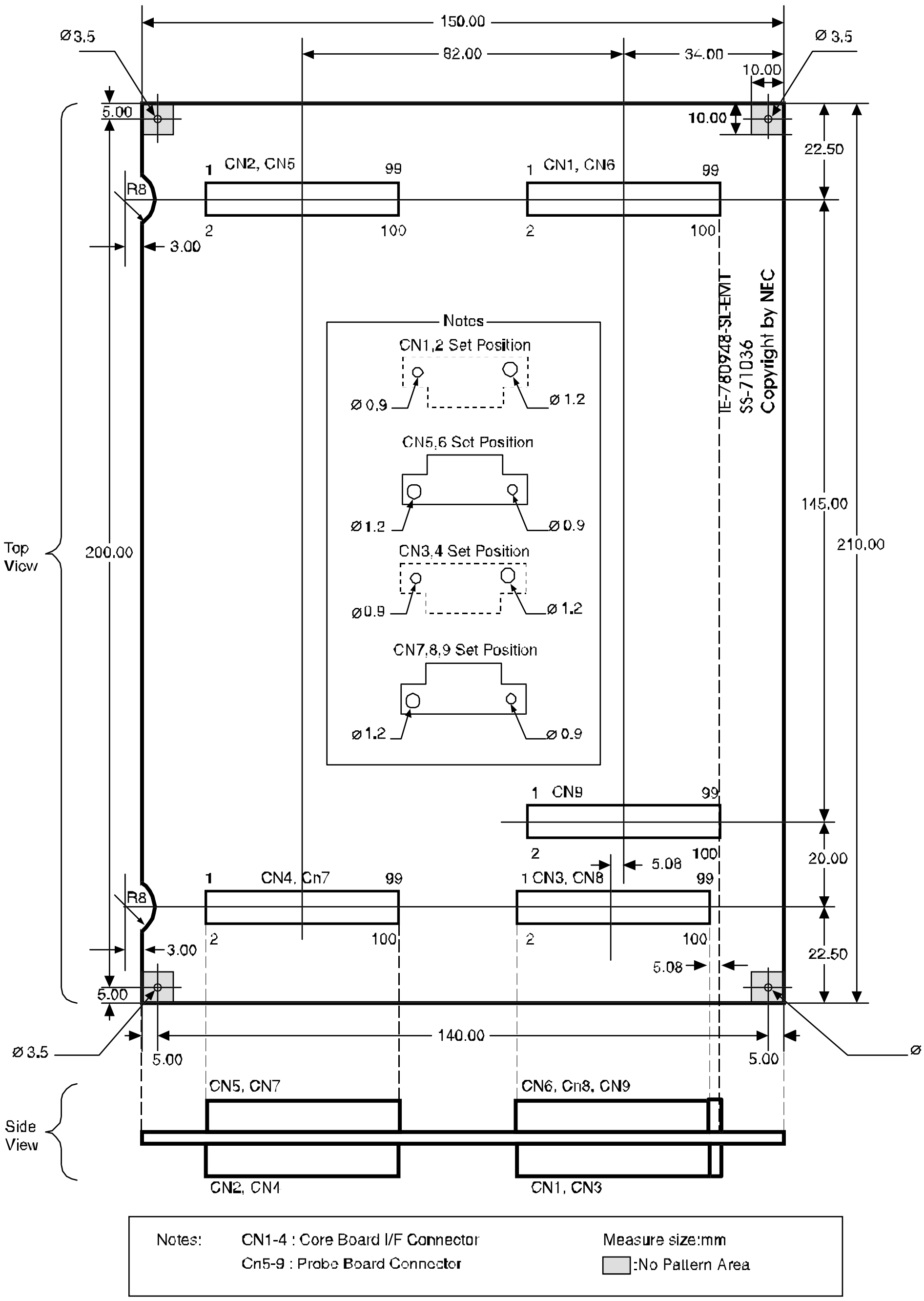
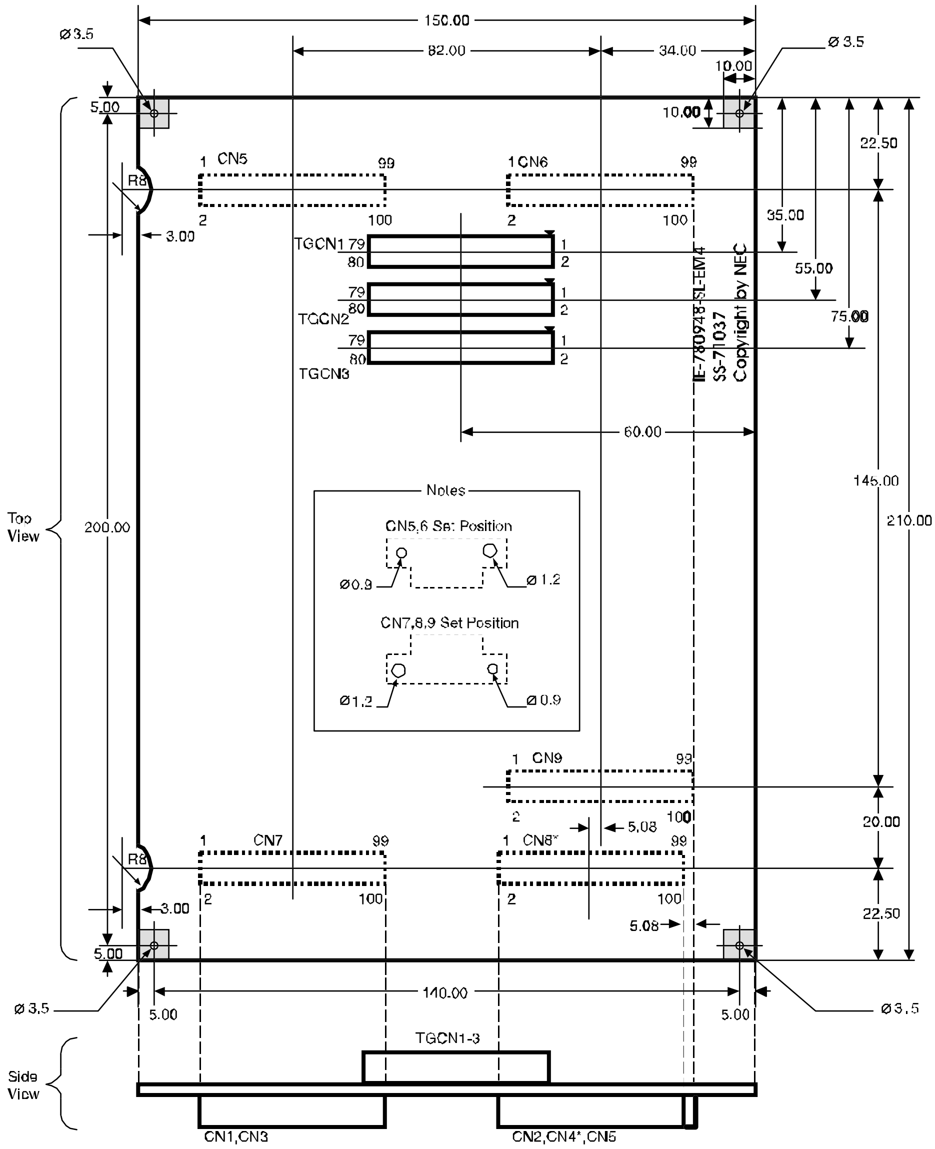


Figure A-2 Printed Wiring Board Dimensions

Probe Board



Notes:	CN5-9 : IO Board I/F Connector TGCN1-3 : Probe Connector *: ONLY CN8 shifted 5.08mm	Measure size:mm :No Pattern Area

Table A-1: Connectors on IE-780948-SL-EM1 Board (Emulation Board) and IE-780948-SL-EM4 Board (Probe Board).

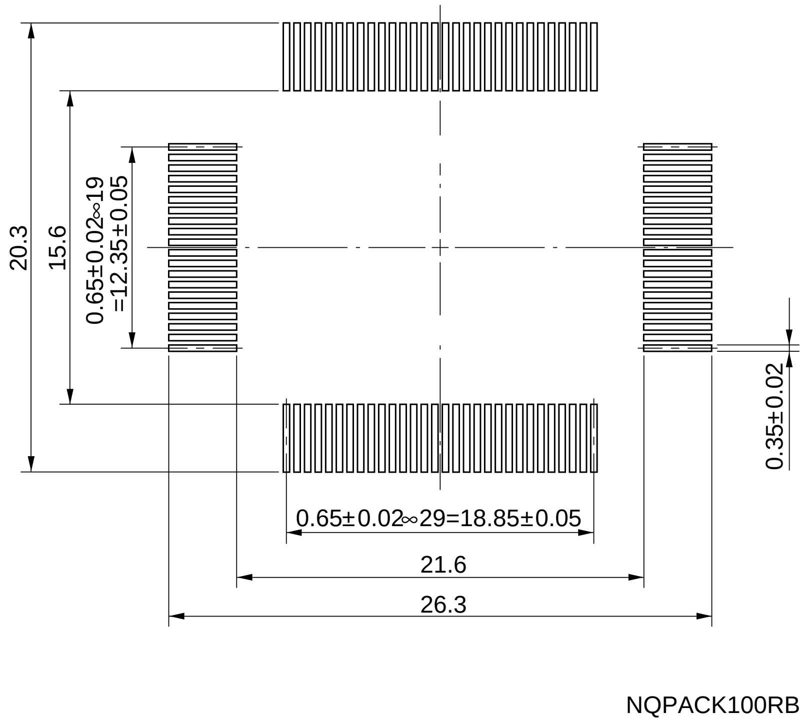
Name	Description (IE-780948-SL-EM1)
CN1	Break board (IE-78001-R-BK) connectors
CN2	
CN3	
CN4	
CN5	Probe board connectors (IE-780948-SL-EM4)
CN6	
CN7	
CN8	
CN9	
CN10	FPGA download cable connector (only for internal use by NEC)
CN13	JTAG connector of FPGA
JP2	FPGA mode selection
JP3	CAN clock selection
JP12	GND-pin of A/D Converter
JP16	VCC-pin of A/D Converter
JP4...JP11	Port 5 connection
JP14	LVREF1
JP15	LVREF0

Name	Description (IE-780948-SL-EM4)
CN5	Emulation board connectors (IE-780948-SL-EM1)
CN6	
CN7	
CN8	
CN9	
TGCN1	Probe connector (EP-100GF-SL)
TGCN2	
TGCN3	

[Memo]

Appendix B Conversion Socket/Conversion Adapter Package Drawings and recommended Board Mounting Pattern

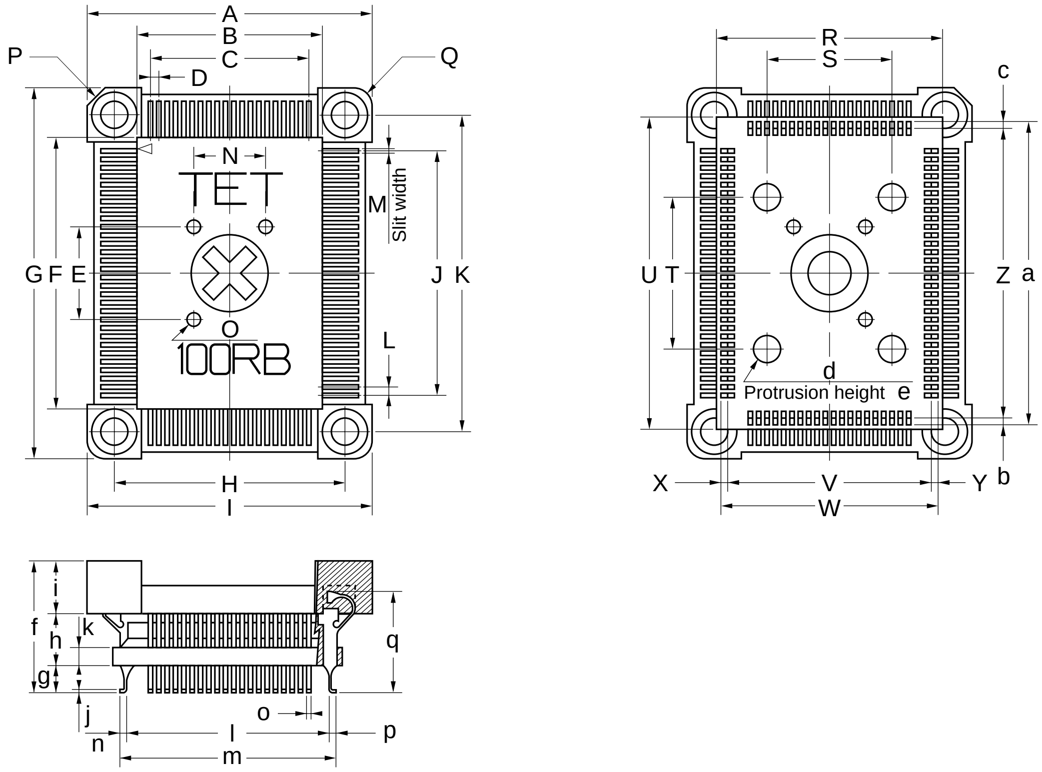
Figure B-1: NQPACK100RB Recommended Board Mount Pattern (Reference)



Caution: **Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "Semiconductor Device Mounting Technology Manual" (C10535E).**

Remark: Manufactured by Tokyo Eletech. Corp.

Figure B-2: NQPACK100RB (Target-Connected Side) Package Drawings (Reference)



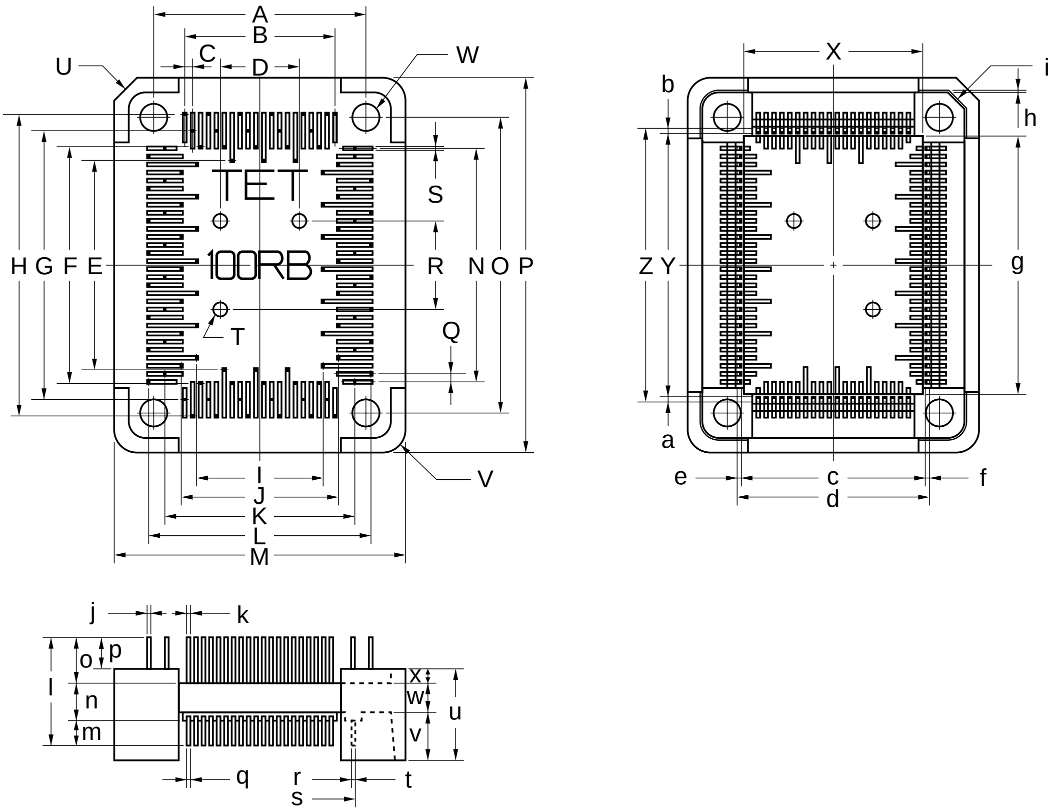
Item	Millimeters	Inches
A	21.75	0.856
B	14.25	0.561
C	0.65x19=12.35	0.026x0.748=0.486
D	0.65	0.026
E	7.0	0.276
F	20.75	0.817
G	28.25	1.112
H	17.4	0.685
I	21.75	0.856
J	0.65x29=18.85	0.026x1.142=0.742
K	23.9	0.941
L	0.65	0.026
M	0.4	0.016
N	6.0	0.236
O	3-ϕ1.0	3-ϕ0.039
P	C 1.5	C 0.059
Q	3-R 1.5	3-R 0.059
R	17.15	0.675
S	10.0	0.394
T	12.0	0.472
U	23.65	0.931
V	15.25	0.600
W	16.25	0.640
X	0.5	0.020
Y	0.5	0.020
Z	21.75	0.856

Item	Millimeters	Inches
a	22.75	0.896
b	0.5	0.020
c	0.5	0.020
d	4-ϕ2.0	4-ϕ0.079
e	1.8	0.071
f	9.45	0.372
g	1.85	0.073
h	3.7	0.146
i	3.9	0.154
j	0.2	0.008
k	1.2	0.047
l	15.25	0.600
m	16.25	0.640
n	0.5	0.020
o	0.25	0.010
p	0.5	0.020
q	6.95	0.274

NQPACK100RB-G1E

Remark: Manufactured by Tokyo Eletech. Corp.

Figure B-3: YQPACK100RB (Probe Side) Package Drawings (Reference)



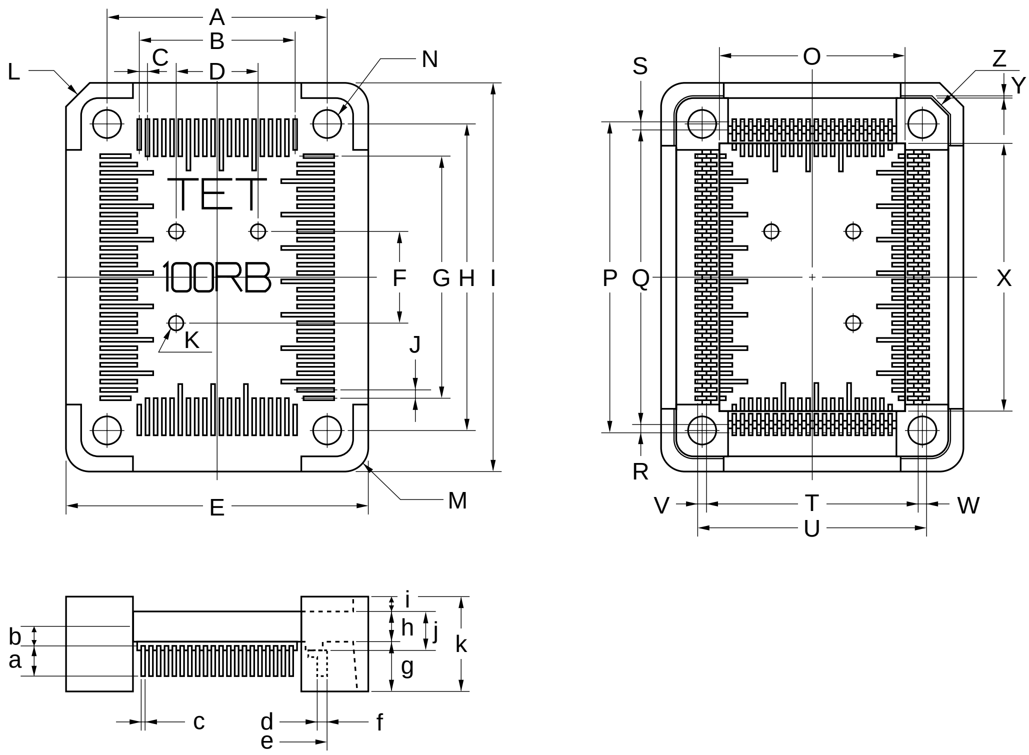
Item	Millimeters	Inches
A	17.4	0.685
B	0.65x19=12.35	0.026x0.748=0.486
C	0.65	0.026
D	6.0	0.236
E	16.85	0.663
F	19.25	0.758
G	21.65	0.852
H	24.05	0.947
I	10.35	0.407
J	12.75	0.502
K	15.15	0.596
L	17.55	0.691
M	23.75	0.935
N	0.65x29=18.85	0.026x1.142=0.742
O	23.9	0.941
P	30.25	1.191
Q	0.65	0.026
R	7.0	0.276
S	0.25	0.010
T	3-ϕ1.0	3-ϕ0.039
U	C 2.0	C 0.079
V	3-R 2.5	3-R 0.098
W	4-ϕ2.2	4-ϕ0.087
X	14.1	0.555
Y	21.25	0.837
Z	22.05	0.868

Item	Millimeters	Inches
a	0.4	0.685
b	0.4	0.026
c	14.75	0.748
d	15.55	0.486
e	0.4	0.016
f	0.4	0.016
g	20.1	0.791
h	0.2	0.008
i	C 1.5	C 0.059
j	0.3	0.012
k	0.25x0.3	0.010x0.012
l	9.0	0.354
m	2.2	0.087
n	3.1	0.122
o	3.7	0.146
p	2.5	0.098
q	0.25	0.010
r	14.75	0.581
s	15.55	0.612
t	0.4	0.016
u	7.4	0.291
v	3.9	0.154
w	2.3	0.091
x	1.2	0.047

YQPACK100RB-G0E

Remark: Manufactured by Tokyo Eletech. Corp.

Figure B-4: HQPACK100RB (Lid for Device Mounted) Package Drawings (Reference)



Item	Millimeters	Inches
A	17.4	0.685
B	0.65x19=12.35	0.026x0.748=0.486
C	0.65	0.026
D	6.0	0.236
E	23.75	0.935
F	7.0	0.276
G	0.65x29=18.85	0.026x1.142=0.742
H	23.9	0.941
I	30.25	1.191
J	0.65	0.026
K	3-ϕ1.0	3-ϕ0.039
L	C 2.0	C 0.079
M	3-R 2.5	3-R 0.098
N	4-ϕ2.2	4-ϕ0.087
O	14.1	0.555
P	24.07	0.948
Q	23.07	0.908
R	0.5	0.020
S	0.5	0.020
T	16.57	0.652
U	17.57	0.692
V	0.5	0.020
W	0.5	0.020
X	20.1	0.791
Y	0.2	0.008
Z	C 1.5	C 0.059

Item	Millimeters	Inches
a	2.25	0.089
b	1.6	0.063
c	0.25	0.010
d	16.57	0.652
e	17.57	0.692
f	0.5	0.020
g	3.9	0.154
h	2.3	0.091
i	1.2	0.047
j	3.1	0.122
k	7.4	0.291

HQPACK100RB-G0E

Remark: Manufactured by Tokyo Eletech. Corp.

[Memo]

Appendix C Pin Correspondence Tables of Emulation Probe

Table C-1: Connector TGCN1 to Emulation Probe

No.	Real-chip	Function	Port.Bit	No.	Signal
1	Pin 80	P7.0/ S31	P7.0	2	GND
3	Pin 79	P7.1/ S30	P7.1	4	GND
5	Pin 78	P7.2/ S29	P7.2	6	GND
7	Pin 77	P7.3/ S28	P7.3	8	GND
9	Pin 76	P7.4/ S27	P7.4	10	GND
11	Pin 75	P7.5/ S26	P7.5	12	GND
13	Pin 74	P7.6/ S25	P7.6	14	GND
15	Pin 73	P7.7/ S24	P7.7	16	GND
17	Pin 72	P12.0/ S23	P12.0	18	GND
19	Pin 71	P12.1/ S22	P12.1	20	GND
21	Pin 70	P12.2/ S21	P12.2	22	GND
23	Pin 69	P12.3/ S20	P12.3	24	GND
25	Pin 68	P12.4/ S19	P12.4	26	GND
27	Pin 67	P12.5/ S18	P12.5	28	GND
29	Pin 66	P12.6/ S17	P12.6	30	GND
31	Pin 65	P12.7/ S16	P12.7	32	GND
33	Pin 64	P13.0/ S15	P13.0	34	GND
35	Pin 63	P13.1/ S14	P13.1	36	GND
37	Pin 62	P13.2/ S13	P13.2	38	GND
39	Pin 61	P13.3/ S12	P13.3	40	GND
41	Pin 60	P13.4/ S11	P13.4	42	GND
43	Pin 59	P13.5/ S10	P13.5	44	GND
45	Pin 58	P13.6/ S9	P13.6	46	GND
47	Pin 57	P13.7/ S8	P13.7	48	GND
49	Pin 56	P14.0/ S7	P14.0	50	GND
51	Pin 55	P14.1/ S6	P14.1	52	GND
53	Pin 54	P14.2/ S5	P14.2	54	GND
55	Pin 53	P14.3/ S4	P14.3	56	GND
57	Pin 52	P14.4/ S3	P14.4	58	GND
59	Pin 51	P14.5/ S2	P14.5	60	GND
61	n.c.	n.c.	n.c.	62	GND
63	n.c.	n.c.	n.c.	64	GND
65	n.c.	n.c.	n.c.	66	GND
67	n.c.	n.c.	n.c.	68	GND
69	n.c.	n.c.	n.c.	70	GND
71	n.c.	n.c.	n.c.	72	GND
73	n.c.	n.c.	n.c.	74	GND
75	n.c.	n.c.	n.c.	76	GND
77	n.c.	n.c.	n.c.	78	GND
79	n.c.	n.c.	n.c.	80	GND

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
GND: Ground clip
1–80: Emulation probe tip pin numbers

Table C-2: Connector TGCN2 to Emulation Probe

No.	Real-chip	Function	Port.Bit	No.	Signal
1	Pin 81	P5.7/ S32 / A15	P5.7	2	GND
3	Pin 82	P5.6/ S33 / A14	P5.6	4	GND
5	Pin 83	P5.5/ S34 / A13	P5.5	6	GND
7	Pin 84	P5.4/ S35 / A12	P5.4	8	GND
9	Pin 85	P5.3/ S36 / A11	P5.3	10	GND
11	Pin 86	P5.2/ S37 / A10	P5.2	12	GND
13	Pin 87	P5.1 / S38 / A9	P5.1	14	GND
15	Pin 88	P5.0 / S39 / A8	P5.0	16	GND
17	Pin 89	P4.7 / AD7	P4.7	18	GND
19	Pin 90	P4.6 / AD6	P4.6	20	GND
21	Pin 91	P4.5 / AD5	P4.5	22	GND
23	Pin 92	P4.4 / AD4	P4.4	24	GND
25	Pin 93	P4.3 / AD3	P4.3	26	GND
27	Pin 94	P4.2 / AD2	P4.2	28	GND
29	Pin 95	P4.1 / AD1	P4.1	30	GND
31	Pin 96	P4.0 / AD0	P4.0	32	GND
33	Pin 97	P6.7 / ASTB	P6.7	34	GND
35	Pin 98	P6.5 / /WR	P6.5	36	GND
37	Pin 99	P6.4 / /RD	P6.4	38	GND
39	Pin 100	CRxD		40	GND
41	Pin 31	P1.5 / ANI5	P1.5	42	GND
43	Pin 32	P1.6 / ANI6	P1.6	44	GND
45	Pin 33	P1.7 / ANI7	P1.7	46	GND
47	Pin 34	AV_{SS}		48	GND
49	Pin 35	P3.0 / TI20	P3.0	50	GND
51	Pin 36	P3.1 / TI21	P3.1	52	GND
53	Pin 37	P3.2 / TI22	P3.2	54	GND
55	Pin 38	P3.3 / PCL / SGOA	P3.3	56	GND
57	Pin 39	P3.4 / SGO /SGOF	P3.4	58	GND
59	Pin 40	V_{SS}		60	GND
61	Pin 41	V_{DD}		62	GND
63	Pin 42	V_{LC0}		64	GND
65	Pin 43	V_{LC1}		66	GND
67	Pin 44	V_{LC2}		68	GND
69	Pin 45	COM0		70	GND
71	Pin 46	COM1		72	GND
73	Pin 47	COM2		74	GND
75	Pin 48	COM3		76	GND
77	Pin 49	P14.7 / S0	P14.7	78	GND
79	Pin 50	P14.6 / S1	P14.6	80	GND

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
GND: Ground clip
1–80: Emulation probe tip pin numbers

Table C-3: Connector TGCN3 to Emulation Probe

No.	Real-chip	Function	Port.Bit	No.	Signal
1	Pin 01	CTxD		2	GND
3	Pin 02	P0.0 / INTP0	P0.0	4	GND
5	Pin 03	P0.1 / INTP1	P0.1	6	GND
7	Pin 04	P0.2 / INTP2	P0.2	8	GND
9	Pin 05	P0.3 / INTP3 / T2PO	P0.3	10	GND
11	Pin 06	P0.4 / INTP4 / TI01	P0.4	12	GND
13	Pin 07	P0.5 / TI00 / TO0	P0.5	14	GND
15	Pin 08	P0.6 / TI50 / TO50	P0.6	16	GND
17	Pin 09	P0.7 / TI51 / TO51	P0.7	18	GND
19	Pin 10	P2.0 / SI0	P2.0	20	GND
21	Pin 11	P2.1 / SO0	P2.1	22	GND
23	Pin 12	P2.2 / SCK0	P2.2	24	GND
25	Pin 13	P2.3 / SI / SO1	P2.3	26	GND
27	Pin 14	P2.4 / SCK1	P2.4	28	GND
29	Pin 15	P2.5 / RxD	P2.5	30	GND
31	Pin 16	P2.6 / TxD	P2.6	32	GND
33	Pin 17	RESET		34	GND
35	Pin 18	X1		36	GND
37	Pin 19	X2		38	GND
39	Pin 20	IC/V_{PP}		40	GND
41	Pin 21	CL1/CCLK		42	GND
43	Pin 22	CL2		44	GND
45	Pin 23	V_{SS}		46	GND
47	Pin 24	V_{DD}		48	GND
49	Pin 25	AV_{REF}		50	GND
51	Pin 26	P1.0 / ANI0	P1.0	52	GND
53	Pin 27	P1.1 / ANI1	P1.1	54	GND
55	Pin 29	P1.2 / ANI2	P1.2	56	GND
57	Pin 29	P1.3 / ANI3	P1.3	58	GND
59	Pin 30	P1.4 / ANI4	P1.4	60	GND
61	n.c.	n.c.	n.c.	62	GND
63	n.c.	n.c.	n.c.	64	GND
65	n.c.	n.c.	n.c.	66	GND
67	n.c.	n.c.	n.c.	68	GND
69	n.c.	n.c.	n.c.	70	GND
71	n.c.	n.c.	n.c.	72	GND
73	n.c.	n.c.	n.c.	74	GND
75	n.c.	n.c.	n.c.	76	GND
77	n.c.	n.c.	n.c.	78	GND
79	n.c.	n.c.	n.c.	80	GND

Remark: The meaning of the symbols and figures in the Emulation Probe column is as follows:
GND: Ground clip
1–80: Emulation probe tip pin numbers
n.c.: No Connection

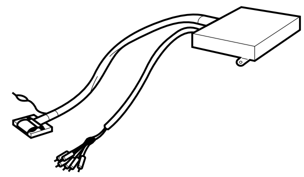
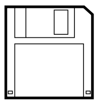
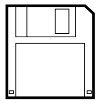
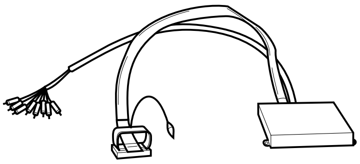
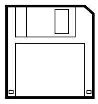
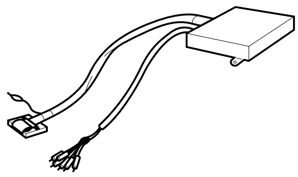
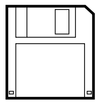
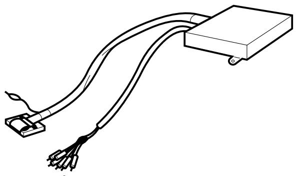
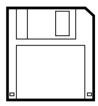
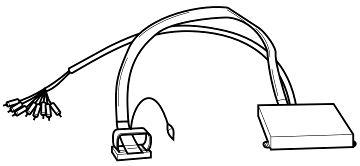
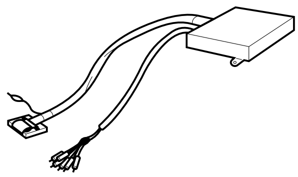
[Memo]

Appendix D System Configuration

Table D-1: IE-78001-R-A System Configuration (1/5)

Target Device	Housing and Control/Trace Board	Break Board
μPD78002 Subseries μPD78002Y Subseries		
μPD78014 Subseries μPD78014Y Subseries		
μPD78018F Subseries μPD78018FY Subseries	78K Series housing (w/power supply)	
μPD780001 Subseries		IE-78001-R-BK (78K/0 Series common break board)
μPD78044A Subseries	IE-78000-R-TR (78K Series trace board) IE-78000-R-SV2 (78K Series supervisor board)	

Table D-1: IE-78001-R-A System Configuration (2/5)

Emulation Board (Optional)	Emulation Probe (Optional)	Debugger (Optional)	Device File (Optional)
IE-78014-R-EM-A	 (Accessory: EV-9200GC-64 (1)) EP-78240GC-R	 ID78K/0	 D002
	 EP-78240CW-R		 D014
	 (Accessory: EV-9500GK-64 (1)) EP-78012GK-R Note 2		 D0001
IE-78044-R-EM	 (Accessory: EV-9200G-64 (1)) EP-78024GF-R		 D044
	 EP-78024CW-R		
	 (Accessory: EV-9200G-80 (1)) EP-78130GF-R		

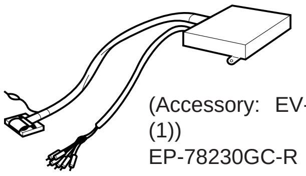
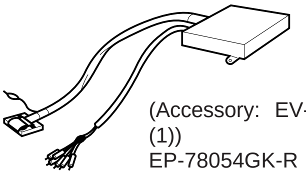
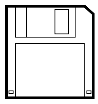
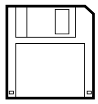
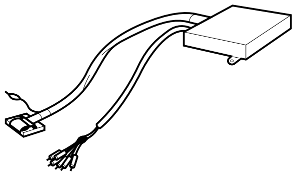
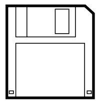
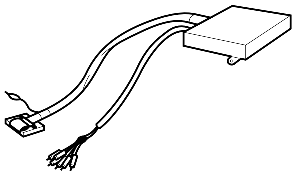
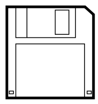
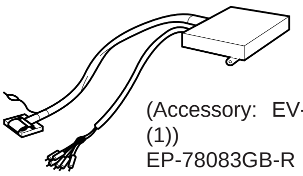
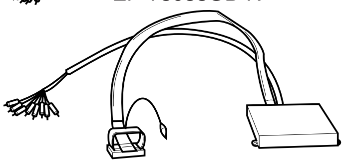
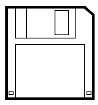
Notes: **1.** For μPD78002, 78002Y, 78014, and 78014Y Subseries only
2. For μPD78018F Subseries only

Table D-1: IE-78001-R-A System Configuration (3/5)

Target Device	Housing and Control/Trace Board	Break Board
μPD78054 Subseries μPD78054Y Subseries	 78K Series housing (w/power supply)	
μPD78064 Subseries		
μPD78078 Subseries	IE-78000-R-TR (78K Series trace board)	IE-78001-R-BK (78K/0 Series common break board)
μPD78083 Subseries	IE-78000-R-SV2 (78K Series supervisor board)	

Caution: μPD78058F and 78058FY Subseries are under development.

Table D-1: IE-78001-R-A System Configuration (4/5)

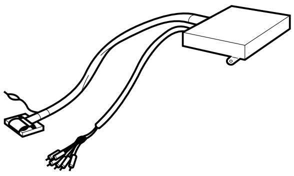
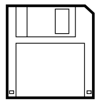
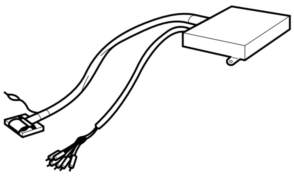
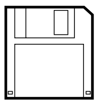
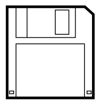
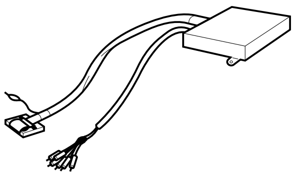
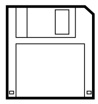
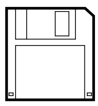
Emulation Board (Optional)	Emulation Probe (Optional)	Debugger (Optional)	Device File (Optional)
IE-78064-R-EM or IE-780308-R-EM	 (Accessory: EV-9200GC-80 (1)) EP-78230GC-R  (Accessory: EV-9500GK-80 (1)) EP-78054GK-R	 ID78K/0	 D054
	 (Accessory: EV-9500GC-100 (1)) EP-78064GC-R Note 2		 D064
IE-78078-R-EM	 (Accessory: EV-9200GF-100 (1)) EP-78064GF-R		 D078
	 (Accessory: EV-9200G-44 (1)) EP-78083GB-R  EP-78083CU-R		 D083

Notes:

1. Supports the μPD78052, 78053, 78054, 78058, 78058F, and 78058FY only.

2. Supports the μPD78064, 78064Y, 78064B, 78078 Subseries, μPD78070A, and 78070AY only.

Table D-1: IE-78001-R-A System Configuration (5/5)

Emulation Board (Optional)	Emulation Probe (Optional)		
IE-78098-R-EM	 (Accessory: EV-9200GC-80 (1)) EP-78230GC-R		 D098
IE-780208-R-EM	 (Accessory: EV-9500GC-100 (1)) EP-78064GC-R Note	 SD78K/0 (with ROM)	 D0208
	 (Accessory: EV-9200GF-100 (1)) EP-78064GF-R		 D0308
IE-780308-R-EM	EP-100GF-SL		 D0948

Note: Supports the μPD780308 Subseries only.

[Memo]

Appendix E Downloading Procedure

Caution: This is the preliminary version. The final version is t.b.d.

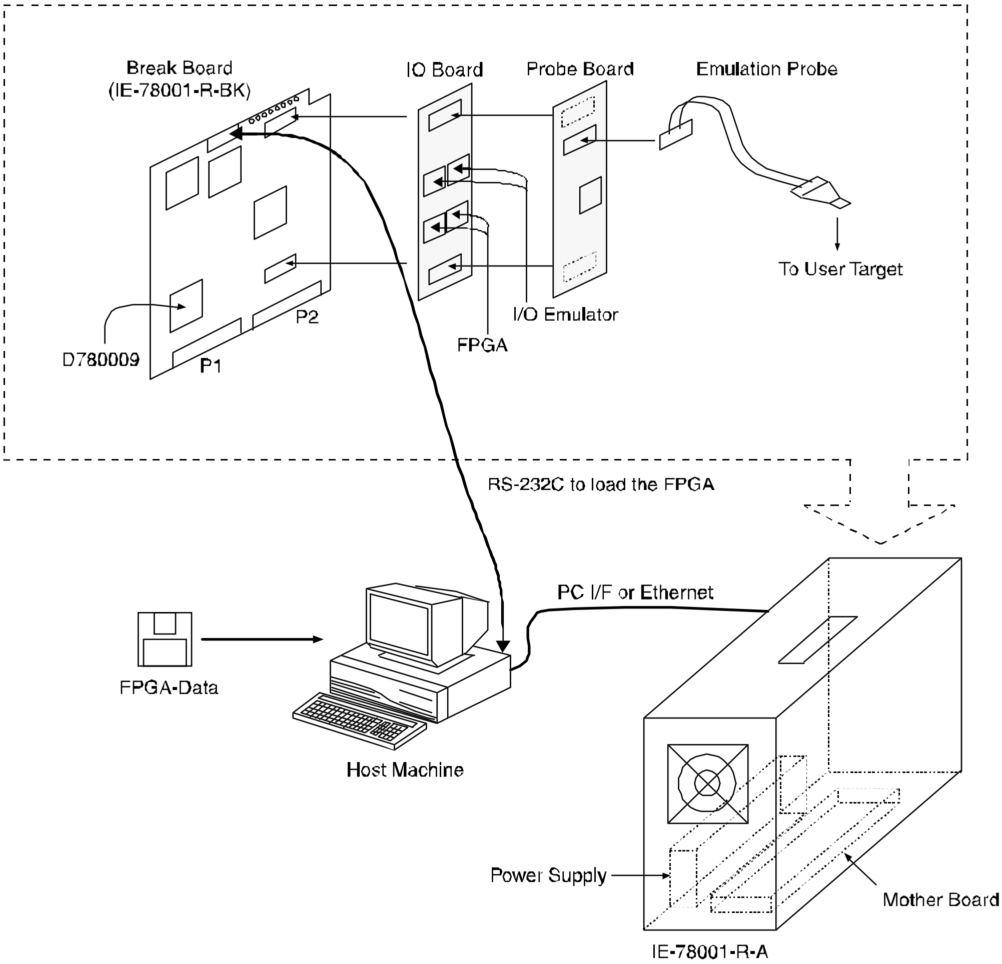
There are two ways of loading FPGA data:

- Download FPGA data via RS-232C by using a terminal program
- Download FPGA data via parallel interface during the IE-setup automatically.
  The FPGA data file is included in the device file.
  (exact description T.B.D.)

Steps for downloading FPGA Data via RS-232C by using a terminal program

1. Please connect D-SUB connector on break board with RS-232C ports of host machine with serial cable. This connection is only used for downloading the FPGA data and could be disconnected after downloading.

Figure E-1: Connections Used for Downloading



2. Power on IBM PC
3. Power on IE
4. Start Windows 3.11
5. Start terminal software in the program group “Accessories”

6. Setup the terminal software “Pulldown Menu: Settings -> Communications” with the following parameters on the host machine:

Parameter	Value
Baud Rate	9600
Data Bits	8
Stop Bits	1
Parity	No
Flow Control	XON / XOFF

7. Test the communication between the host machine and the IE by typing **help** in the terminal window. If the communication is OK you will see a list of commands to setup your IE.
The following commands are available at this moment:

ID:	Board ID display
VER:	Board version display
FPGA:	FPGA data download to the EM board
MASK:	Mask option data display
MASKC:	Mask option data clear
MASKL:	Mask option data download
MODE:	Change parameters of serial communication
HELP:	Display the help message

8. The first step is to setup the EM board. Therefore you type FPGA in the terminal window. Here you must also select the data file with the terminal program.

9. Before you can disconnect the communication to the control program of the IE you need to start the debug software ID78K0 on the host machine. When the software has finished setting up of the IE, it is ready for emulation. So long as you did not power down the IE it is possible to power down the host machine or reset the IE with the button in front of the IE.

Steps for downloading via parallel interface during the IE-setup automatically (t.b.d.).

[Memo]

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