NEC

Preliminary User's Manual

CAG4M-FP-FA

CAG4M-FP-FA User's Manual

Flash Programming Adapter for V850E/CAG4-M

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Notes for CMOS Devices

1. **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

2. **HANDLING OF UNUSED INPUT PINS**
   Unconnected CMOS device inputs can result in malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3. **PRECAUTION AGAINST ESD**
   A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and to quickly dissipate it should it occur. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4. **STATUS BEFORE INITIALIZATION**
   Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5. **POWER ON/OFF SEQUENCE**
   In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be

judged separately for each device and according to related specifications governing the device.

6. **INPUT OF SIGNAL DURING POWER OFF STATE**
Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Preface

Target Readers This manual is intended for users who design and develop application systems using the CAG4M-FP-FA User's Manual.

Purpose The purpose of this manual is to describe the proper operation of the CAG4M-FP-FA and its basic specifications.

Organization This manual is broadly divided into the following parts.

Overview

Setup procedure

Cautions

How to read this manual It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers. This manual explains the basic setup procedure, so read this document before using the CAG4M-FP-FA .

To learn about the basic specifications and operation methods:

Read this manual in the order of the Table of Contents.

To learn about software settings such as operation methods and command functions.

Read the user's manual of the debugger that is used:

Legend Symbols and notation are used as follows:

Weight in data notation : Left is high-order column, right is low order column

Active low notation : $\overline{xxx}$ (pin or signal name is over-scored) or

/xxx (slash before signal name)

Memory map address : High order at high stage and low order at low stage

Note Explanation of (Note) in the text

Caution Item deserving extra attention

Numeric notation :

Binary... XXXX or XXXB

Decimal... XXXX

Hexadecimal... XXXXH or 0x XXXX

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo): 210 = 1024

M (mega): 220 = 10242 = 1,048,576

G (giga): 230 = 10243 = 1,073,741,824

Further information For further information see http://www.eu.necel.com.

Table of Contents

Chapter 1 Introduction

1.1 Definitions and Abbreviations

Table 1-1 Terminology

Term	Description
CAG4M-FP-FA	Flash programming adapter for Cargate-M

1.2 Related Documents

Related Documents When using this manual, refer to the following manuals. The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Title	Document Number
V850E/CAG4-M Preliminary User's Manual	U18577EE1V1UM00
V850E/CAG4-M Electrical Target Specification	EASE-ES-0009-V03
PG-FP4 User's Manual	U15260EE3V1UM00
PG-FP5 User's Manual	U18865EJ1V0UM00
CAG4M-FP-FA schematics	EESS-0500-090-01

For documentation please refer to: **http://www.eu.necel.com/docuweb**/

Chapter 2 Overview

2.1 Hardware Specifications

The CAG4M-FP-FA flash programming adapter is supposed to ease the use of an external flash programmer like PG-FP4 or PG-FP5 and reduce the system cost for ECU's working with the V850E/CAG4-M.

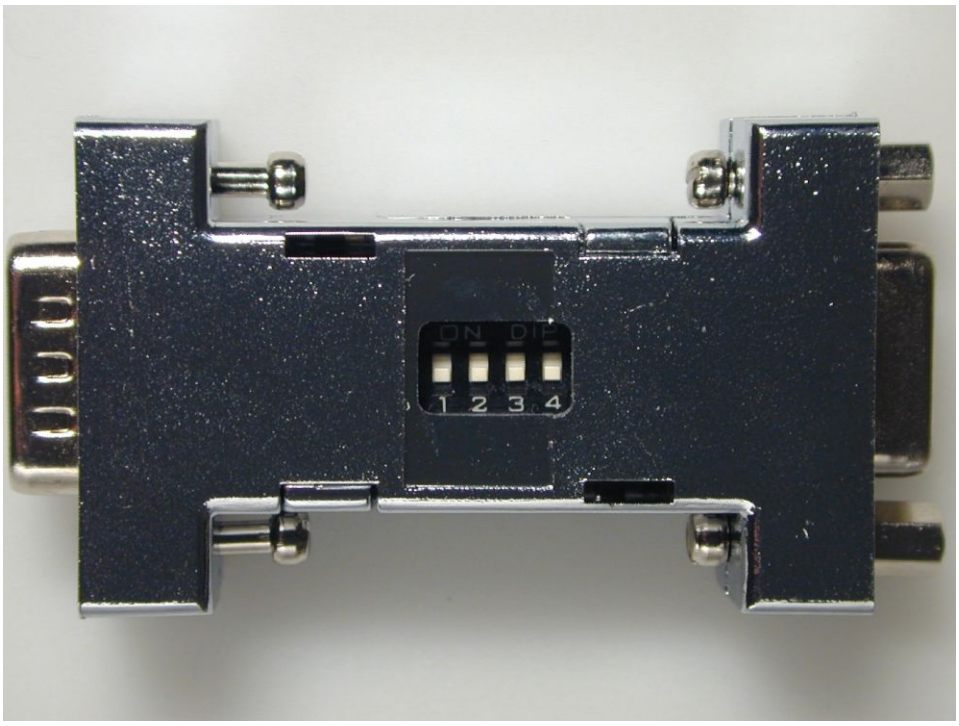

Figure 2-1 CAG4M-FP-FA

2.1.1 Level Shifting

Level Shifting

The V850E/CAG4-M can be used with 2 different voltage supplies:

- Main area: 3.3V
- Isolated Area: 5.0V

Therefore for programming necessary I/O pins might have a different voltage level, for details please refer to following table.

Table 2-1 V850E/CAG4-M Flash Programming IO Pins

Pin	Signal	Voltage Connection
143	RESET	VDD50
137	FLMD0	
128	MRESET	BVDD3x
115	FLMD1	
57	SIB0	
58	SOB0	
59	SCKB0	
60	TXDD0	
61	RXDD0	

As the programmers do not support different voltage levels for the I/O-pins a level shifting is necessary. This can be done with the CAG4M-FP-FA without additional components on the target PCB.

2.1.2 Generation REGON Signal

Generation of REGON Signal

The V850E/CAG4-M offers the possibility of low-power modes by using a dedicated pin on the isolated area, the REGON (pin 4). To support the flash programming it is necessary that all voltages for the V850E/CAG4-M are available and stable. Therefore it is not possible to program the device with an external programmer when the power down mode functionality of the isolated area is used.

The CAG4M-FP-FA supports the generation of an additional external REGON signal, which can be used to switch on the external regulators before the communication is started.

2.2 Dimensions

Note 1. Excluding programmer and target connector.

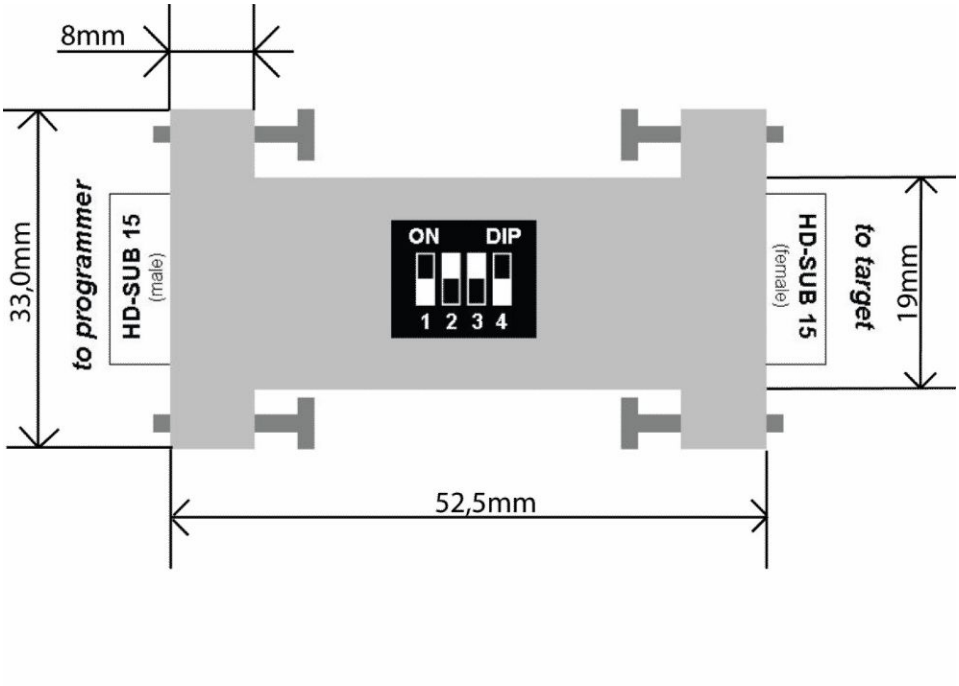

Figure 2-2 CAG4M-FP-FA Dimensions

Chapter 3 Setup Procedure

This chapter describes the procedure for setting up the CAG4M-FP-FA Perform setup using the following procedure described in the related chapter.

3.1 Hardware Description

3.1.1 DIP-Switch Setting

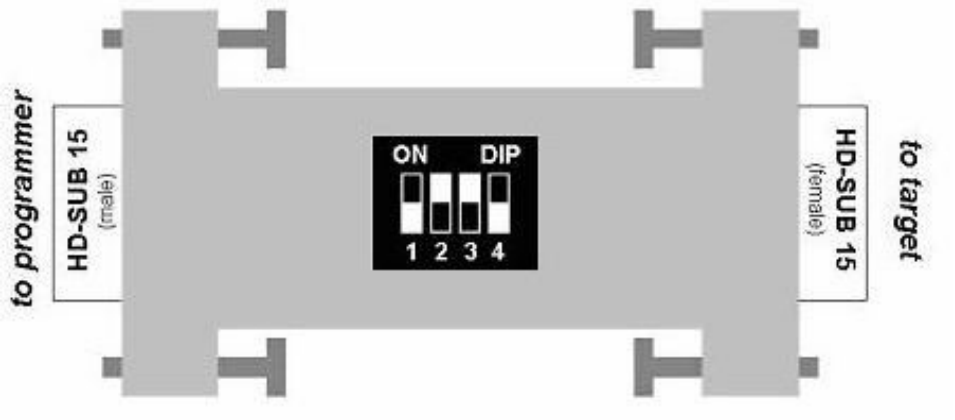

Figure 3-1 CAG4M-FP-FA

Table 3-1 Dip Switch Description

Switch	On	Off	Remark
SW1	HS signal of programmerPin 7 (HS) of programmer connected to Pin 7 for target.	No connection	Don’t switch both to ON at the same time!
SW2	Generated REGON signal connected to Pin 7 for target.		
SW3	Generated REGON signal connected to Pin 10 for target.		
SW4	Internal connection of power supply pinsPin 8 & 9 (VDD3) of programmer connector connected to pin 8 & 9 (VDD5) of target connector		Don’t switch on, if level shifting (3.3 <-> 5.0V) should be used

3.1.2 Connector Description

Table 3-2 HD-SUB15 (female) to Programmer

Pin	Signal	Remark
1	SO/TxD	
2	SI/RxD	
3	SCK	
4	RESET	
5	VDD2	
6	FLMD1	
7	H/S	
8	VDD3	3.3V voltage supply for the CAG4M-FP-FA.This voltage has to be supplied by the programmer
9	VDD3	
10	NC	
11	VPP	
12	FLMD0	
13	VDE	
14	CLK	
15	GND	

Table 3-3 HD-SUB15 (male) to Target

Pin	Signal	Remark
1	SO/TxD	3.3V level (supplied from programmer)
2	SI/RxD	
3	SCK	
4	RESET	5.0V level (supplied from target hardware)
5	VDD2	3.3V level (supplied from programmer)
6	FLMD1	
7	H/S	SW1 ON : 3.3V level (supplied from programmer)
	REGON	SW2 ON : 5.0V level (supplied from target hardware)
8	VDD5	5.0V voltage supply for the CAG4M-FP-FA.This voltage has to be supplied by the target hardwareIf SW4 ON direct connected to pin 8 & 9 of HD-SUB 15 (female) from programmer
9	VDD5	
10	REGON	SW3 ON : 5.0V level (supplied from target hardware)
	NC	
11	VPP	
12	FLMD0	5.0V level (supplied from target hardware)
13	VDE	
14	CLK	
15	GND	

3.1.3 Power Supply

Power Supply

For proper functionality the CAG4M-FP-FA needs 2 voltage supplies:

• 3.3V; supplied by the programmer

The programmer has to supply the 3.3V for the flash programming adapter. For the necessary settings please refer to the appropriate User's Manual

• 5.0V; supplied by the target hardware

The target hardware has to supply the 5.0V for the flash programming adapter. This supply enables the level shifting from 3.3V from programmer to 5.0V for the V850E/CAG4-M.

Additional to the output current, the CAG4M-FP-FA has an internal maximum consumption of 3 mA.

This current needs to be considered during design of the ECU and added to the supply for V850E/CAG4-M itself.

3.2 Connectors

Table 3-4 Target Cable Pinout

Signal	HD-SUB 15	16-PIN	10-PIN	Remark
SO/TxD	1	5	5	
SI/RxD	2	3	3	
SCK	3	7	7	
RESET	4	2	2	
VDD2	5	11	-	
FLMD1	6	12	-	
REGON	7	8	8	SW2 = ON
H/S				SW1 = ON
VDD3	8	4	4	SW4 = ON; same voltage for programmer and target
VDD5				SW4 = OFF; voltage supply from target necessary
VDD3	9	4	4	SW4 = ON; same voltage for programmer and target
VDD5				SW4 = OFF; voltage supply from target necessary
REGON	10	13	-	SW3 = ON
NC				SW3 = OFF
VPP	11	6	6	
FLMD0	12	14	-	
VDE	13	10	10	
CLK	14	9	9	
GND	15	1	1	

3.3 Target Settings

3.3.1 LevelShift for Reset and FLMD0

Table 3-5 Switch Setting

Switch	Setting
SW1	OFF
SW2	OFF
SW3	OFF
SW4	OFF

LevelShift for RESET and FLMD0

The level shifting is the bacic functionality of this adapter. RESET and FLMD0 are always shifted to the level of VDD5, which has to be supplied by the target hardware. The signals can be connected to the according V850E/CAG4- M pins.

3.3.2 REGON Generation with HS and LevelShift

Table 3-6 Switch Setting

Switch	Setting
SW1	ON
SW2	OFF
SW3	ON
SW4	OFF

REGON Generation with HS and LevelShift

Additional SW3 = ON enables the generation of a REGON signal on pin 10. This signal can be used to overrule the V850E/CAG4-M REGON output to enable the external voltage regulators on the target for flash programming.

With SW1 = ON the HS signal from the programmer is available on pin 7.

3.3.3 REGON Generation on HS signal Line and LevelShift

Table 3-7 Switch Setting

Switch	Setting
SW1	OFF
SW2	ON
SW3	OFF
SW4	OFF

REGON Generation on HS signal line and LevelShift

SW2 = ON enables the generation of a REGON signal on pin 7. This signal can be used to overrule the V850E/CAG4-M REGON output to enable the external voltage regulators on the target for flash programming. The use of handshake

signal for CSI programming is not possible with this configuration and SW1 must be OFF.

3.3.4 REGON Generation without LevelShift

Table 3-8 Switch Setting

Switch	Setting
SW1	OFF
SW2	OFF
SW3	ON
SW4	ON

REGON Generation without LevelShift

SW3 = ON enables the generation of a REGON signal on pin 10. This signal can be used to overrule the V850E/CAG4-M REGON output to enable the external voltage regulators on the target for flash programming.

With SW4 = ON, the VDD50 of V850E/CAG4-M should be on the same level as VDD3x. With this configuration the voltage sensing of the programmer can be used.

Chapter 4 Schematics