User's Manual

RA6T2 Group

MCB-RA6T2 User's Manual

Renesas RA Family
RA6 Series

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Renesas RA Family

MCB-RA6T2 User's Manual

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1. Overview

MCB-RA6T2 is a CPU board for motor control evaluation. By using this product in combination with an inverter board, motor control using RA6T2 can be easily performed.

There are two versions of the MCB-RA6T2 (Version 1 and Version 2), each with a different circuit diagram and terminal configuration. The model names for each are as follows:

Version 1 Model : RTK0EMA270C00000BJ
Version 2 Model : RTK0EMA270C00002BJ

1.1 Presupposition and precautions of this document

1. Experience of using tools: This document assumes that the user has used terminal emulation program of Integrated Development Environment (IDE) such as e^2 studio before.
2. Knowledge about the development subject: This document assumes that the user has a basic knowledge to modify the sample project regarding MCU and embedded system.
3. Before using this product, wear an antistatic wrist strap. If you touch this product with static charge on your body, a device failure may occur, or operation may become unstable
4. All screen shots provided in this document is for reference. Actual screen displays may differ depending on the software and development tool version which you use.

2. Product Contents

This kit consists of the following parts.

1. CPU Board x1
2. USB Cable x1
3. Screw x4
4. Standoff x4

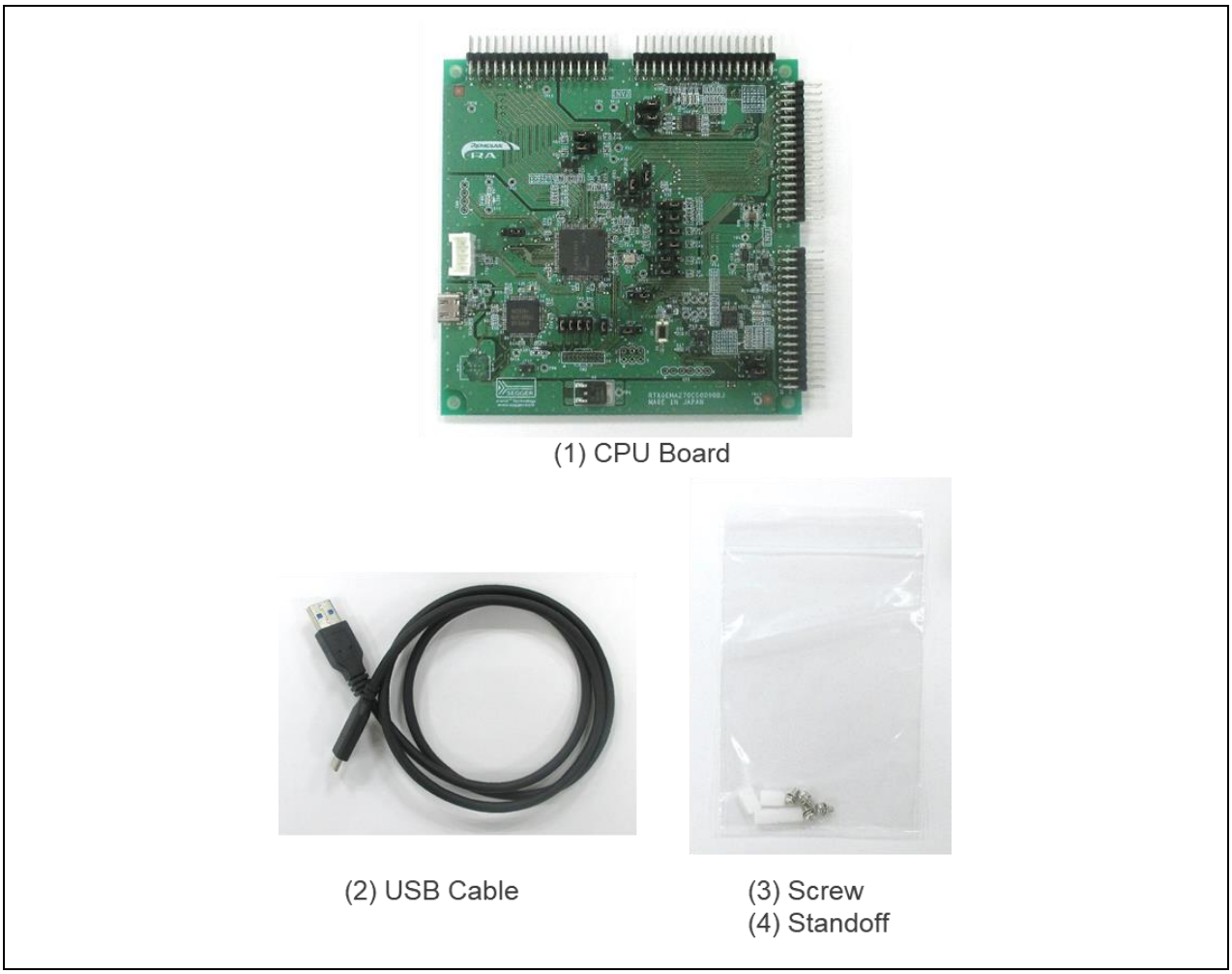

Figure 2-1 Product contents

3. Product Order Information

Product No. to order MCB-RA6T2 :
Version 1 Model : RTK0EMA270C00000BJ
Version 2 Model : RTK0EMA270C00002BJ

4. Hardware Configuration and Default Setting

4.1 Hardware configuration

The specifications of the CPU board are shown below.

Table 4-1 CPU Board Specification

item		Specification
Product name		CPU Board
Board part No.		Version 1 : RTK0EMA270C00000BJ Version 2 : RTK0EMA270C00002BJ
Compatible inverter board		RTK0EM0000B12020BJ
External view		 Note: The actual product may differ from this photo.
Mounted MCU	Product group	RA6T2 group
	Product No.	R7FA6T2BD3CFP
	CPU maximum operating frequency	240MHz
	Bit count	32 bit
	Package / Pin number	LFQFP / 100 pin
	RAM	64K byte
MCU input clock		10MHz (Generate with external crystal oscillator)
Input power supply voltage		DC 5V Select one from the below • Power is supplied from compatible inverter board • Power is supplied from USB connector
Debugger		J-Link On-Board (Onboard debugger circuit)
Connector		• Inverter board connector (2 sets) • USB connector for J-Link On-Board • SCI connector for Renesas Motor Workbench communication • Through hole for CAN communication • Through hole for SPI communication • 20 pin through hole for Arm debugger
Switch		MCU reset switch
LED		User-controllable LED x6, Power LED x1
Board size		109mm (W) x 109mm (L)
Operating temperature		Room temperature
Operating humidity		No condensation allowed
EMC Directive		EN61326-1 : 2021 EMI : Class A EMS : Basic Electromagnetic environment

4.2 Block diagram

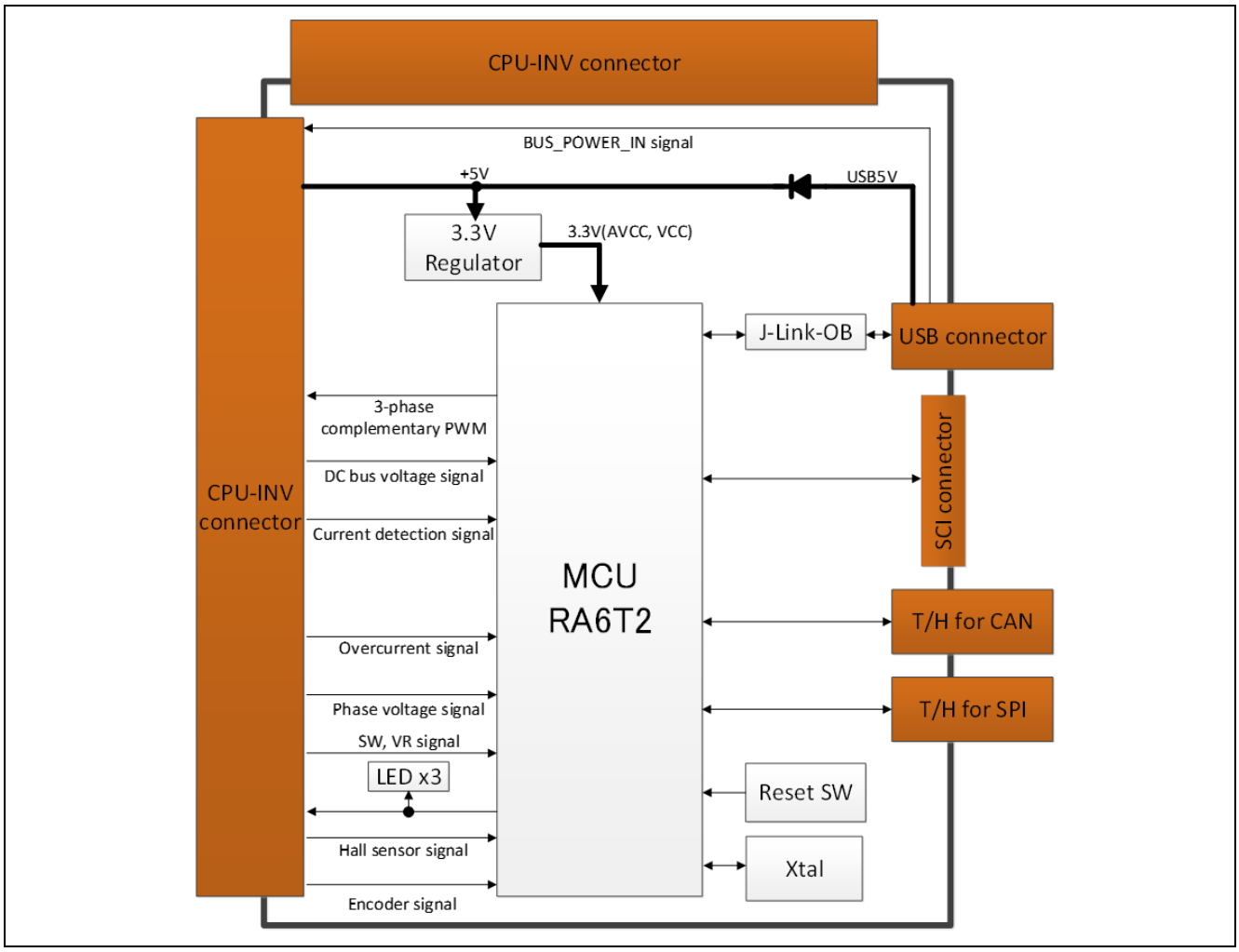

Figure 4-1 Block Diagram of CPU Board

4.3 Board Layout

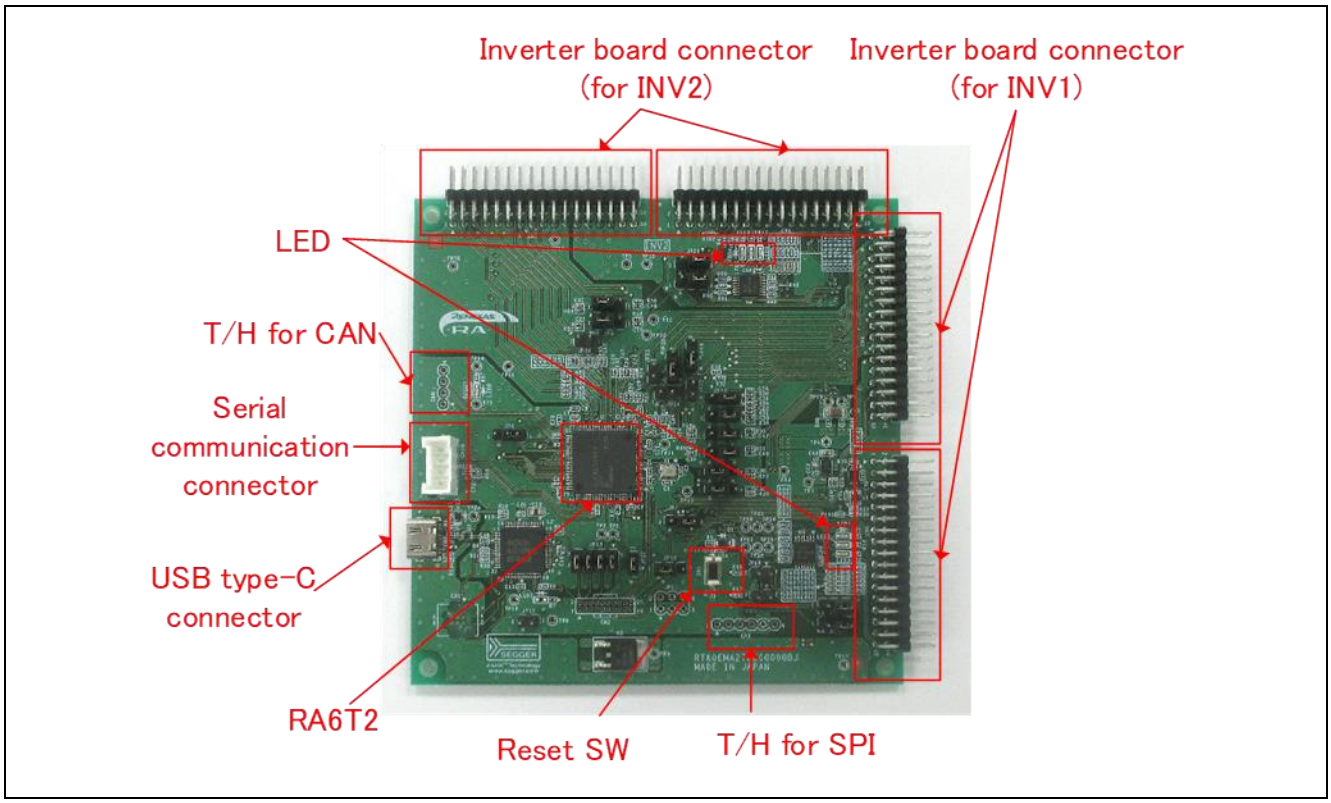

Figure 4-2 CPU Board Layout

4.4 Standoffs and Screws

Before using this product, assemble the included standoffs and screws as shown below.

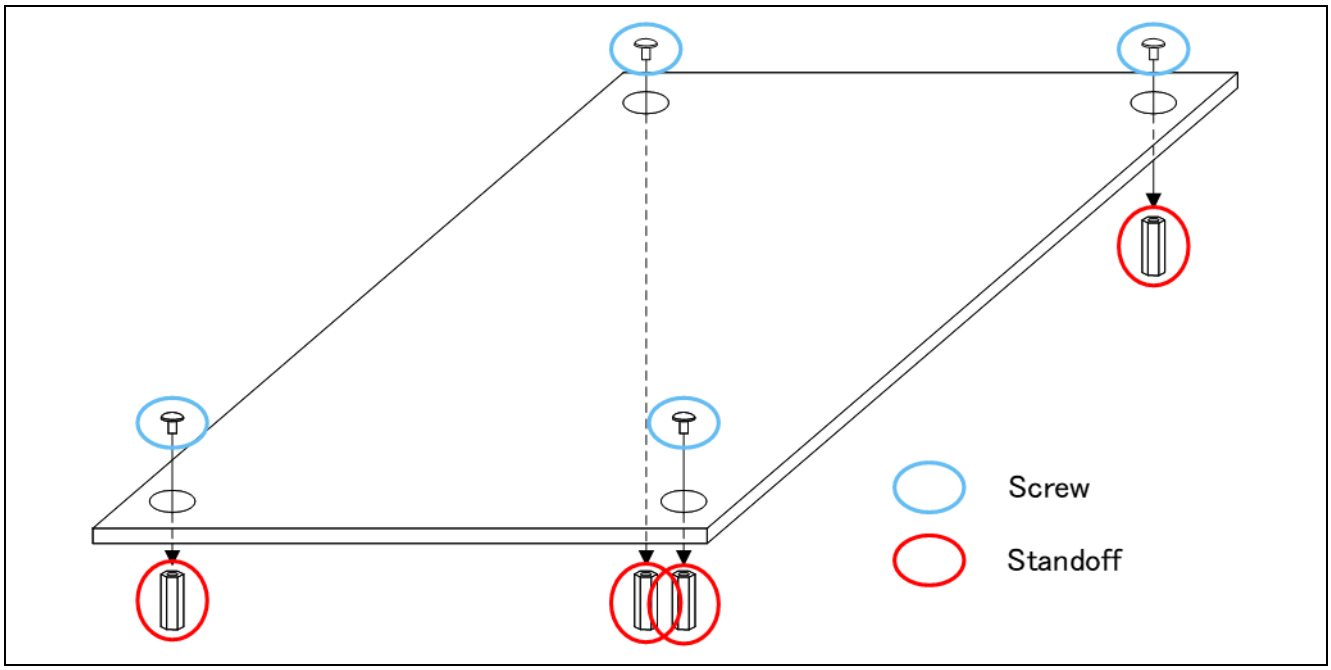

Figure 4-3 Standoffs and Screws assembly

4.5 Jumper pin setting

Default settings and functions of the jumper pins (JP1~JP25) are as follows.

Table 4-2 Jumper pin setting

Jumper pin	Default setting	Function
JP1	2-3pin short	1-2pin short : INV1 IPS CSNIRQN 2-3pin short : INV1 Encoder Z
JP2	2-3pin short	1-2pin short : INV2 PFC current detection (for HV INV) 2-3pin short : INV2 IPS A
JP3	2-3pin short	1-2pin short : INV2 AC input voltage detection (for HV INV) 2-3pin short : INV2 IPS A#/Encoder A#
JP4	1-2pin short	1-2pin short : INV1 HALL U 2-3pin short : INV1 IPS A
JP5	1-2pin short	1-2pin short : INV1 HALL V 2-3pin short : INV1 IPS A#/Encoder A#
JP6	1-2pin short	1-2pin short : INV2 V-phase voltage detection 2-3pin short : INV2 IPS B
JP7	2-3pin short	1-2pin short : INV1 PFC current detection (for HV INV) 2-3pin short : INV1 IPS B
JP8	2-3pin short	1-2pin short : INV2 IPS CSNIRQN 2-3pin short : INV2 Encoder Z
JP9	1-2pin short	1-2pin short : INV2 W-phase voltage detection 2-3pin short : INV2 IPS B#/Encoder B#
JP10	2-3pin short	1-2pin short : INV1 AC input voltage detection (for HV INV) 2-3pin short : INV1 IPS B#/Encoder B#
JP11	1-2pin open 3-4pin open 5-6pin open	Fix open
JP12	1-2pin open	1-2pin short : Disable J-Link On-Board 1-2pin open : Enable J-Link On-Board
JP13	1-2pin short 3-4pin short 5-6pin short 7-8pin short	Fix short
JP14	1-2pin short	1-2pin short : Enable RA6T2 2-3pin short : Disable RA6T2
JP15, JP16	1-2pin open	1-2pin short : Enable pull-up for I2C 1-2pin open : Disable pull-up for I2C
JP17	2-3pin short	1-2pin short : INV1 IPS A 2-3pin short : INV1 Encoder A
JP18	2-3pin short	1-2pin short : INV1 IPS B 2-3pin short : INV1 Encoder B
JP19	1-2pin short	1-2pin short : INV1 W-phase voltage detection 2-3pin short : INV1 W-phase current detection (PGAVSS)
JP20	1-2pin short	1-2pin short : INV1 V-phase voltage detection 2-3pin short : INV1 V-phase current detection (PGAVSS)
JP21	2-3pin short	1-2pin short : INV2 IPS A 2-3pin short : INV2 Encoder A
JP22	2-3pin short	1-2pin short : INV2 IPS B 2-3pin short : INV2 Encoder B
JP23, JP24, JP25	1-2pin open	1-2pin open : Enable LPF for current sensing 1-2pin short : Disable LPF for current sensing

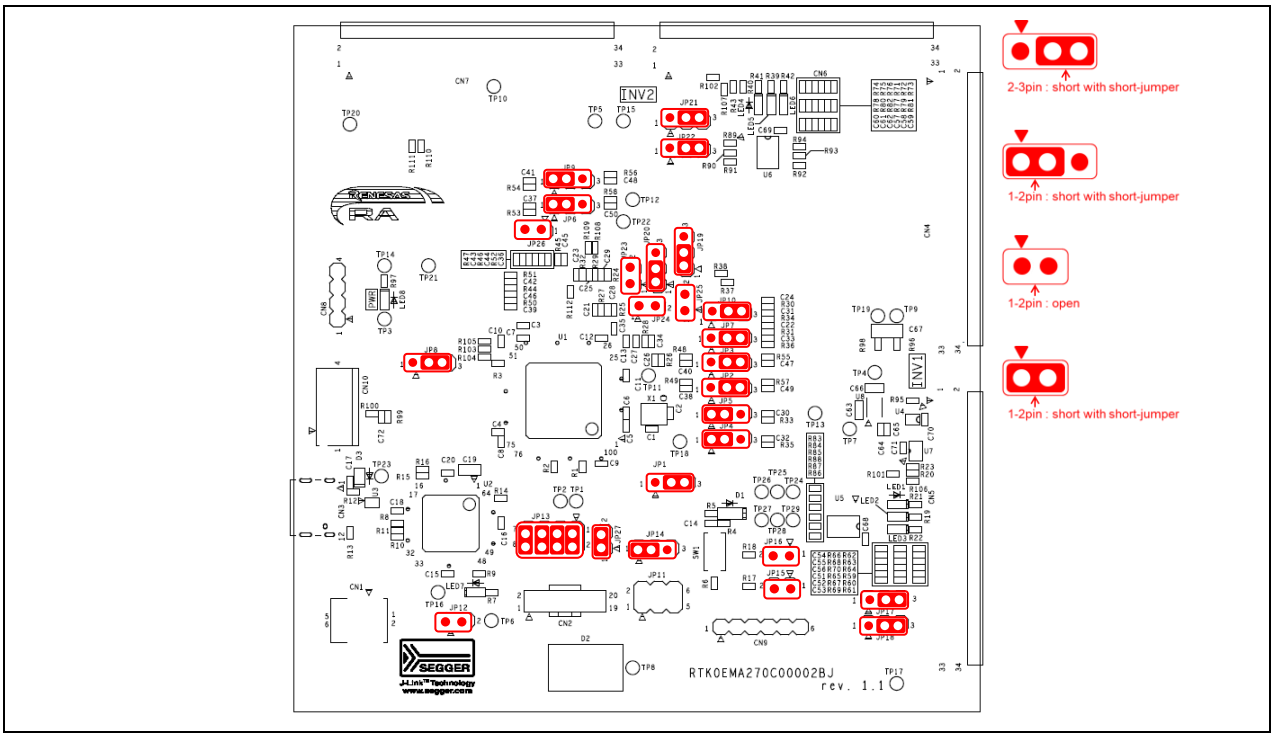

Figure 4-4 Default jumper pin setting

4.6 Jumper resistor setting(Only for RTK0EMA270C00002BJ)

Default settings and functions of the jumper resistor are as follows. This setting can only be changed for RTK0EMA270C00002BJ.

Table 4-3 Jumper resistor setting

Function	Default setting	Setting (function in use)
PFCPWM/CAN select (INV1,2)	R104,R105 mount, R3,R103 unmount	R104,R105 mount ,R3,R103 unmount: INV1 INV2 PFCPWM2 R104,R105 unmount,R3,R103 mount : CAN (CN8)
VU/HVtemp select (INV1)	R108 mount, R109 unmount	R108 mount ,R109 unmount: INV1 VU R108 unmount,R109 mount : INV1 HVtemp
VU/HVtemp select (INV2)	R110 mount, R111 unmount	R110 mount ,R111 unmount: INV2 VU R110 unmount,R111 mount : INV2 HVtemp
OC#/PFCERROR connect (INV1)	R106 unmount	R106 unmount: OC#, PFCERROR not connect R106 mount : OC#, PFCERROR connect
OC#/PFCERROR connect (INV2)	R107 unmount	R107 unmount: OC#, PFCERROR not connect R107 mount : OC#, PFCERROR connect
IU/IU(differential input) select (INV2)	R112 unmount (JP4 1-2pin short)	R112 unmount,JP4 1-2pin short: IU(single ended input AN006) R112 unmount,JP4 2-3pin short: IU(single ended input AN006) R112 mount ,JP4 Open : IU(differential input AN018-PGAVSS3)

4.7 Connection Example

Figure 4-5 shows a connection example when using this product in combination with a Renesas inverter board kit (MCI-LV-1, P/N: RTK0EM0000S04020BJ) and a communication board (MC-COM, P/N: RTK0EMXC90S00000BJ).

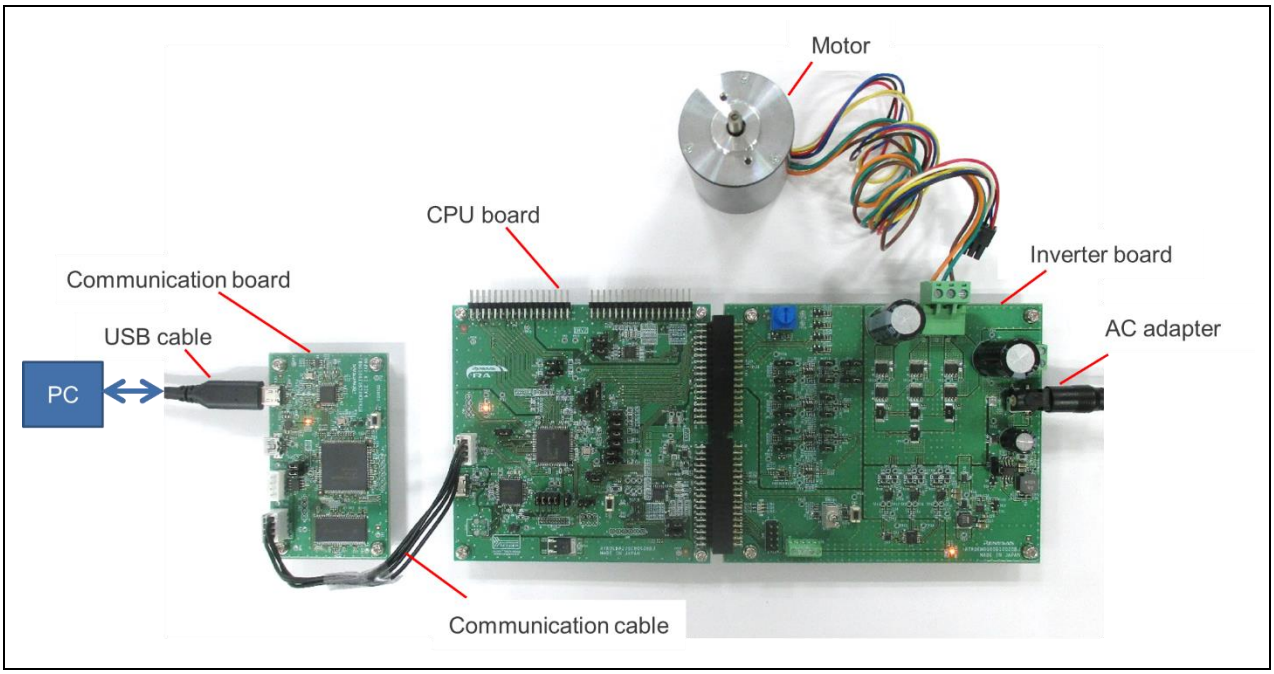

Figure 4-5 Connection Example

5. CPU Board Specification

This section describes the specification of the CPU Board.

5.1 Functions

5.1.1 Power supply

When not connected to the inverter board, power should be supplied from the USB connector. When connecting to the inverter board, power supply from the USB connector or from the inverter board will be automatically selected. USB power supply has priority.

5.1.2 Onboard debugger

This product has the onboard debugger circuit, J-Link On-Board (hereinafter called “J-Link-OB”). You can write a program (firmware) of RA6T2 with it. When you write a program, connect the CPU board to PC with USB cable. J-Link-OB operates as debugger equivalent to J-Link. If connecting from Integrated Development Environment or flash programming tool (e.g. J-Flash Lite by SEGGER), set the type of debugger (tool) to “J-Link”.

5.1.3 Inverter board connector

Two inverter boards can be connected to this board: the 1st inverter board is connected with CN4 and CN5, and the 2nd inverter board is connected with CN6 and CN7. The pin assignments of the connectors are shown in Table 5-1 to Table 5-8.

(1) The pin assignments (CN4 to CN7) of Version 1 (RTK0EMA270C00000BJ) are shown below.

Table 5-1 1st Inverter board connector (CN4) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	SPARE1	-	2	AGND	- (AVSS)
3	VPN	PA06/AN006	4	AGND	- (AVSS)
5	IU	PA04/AN004	6	PGAVSSU	PA05/PGAVSS2
7	IV	PA02/AN002	8	PGAVSSV	PA03/AN003
9	IW	PA00/AN000	10	PGAVSSW	PA01/AN001
11	VU	PA07/AN007	12	VV	PA03/AN003
13	VW	PA01/AN001	14	AGND	- (AVSS)
15	VAC	PB10/AN028	16	IPFC	PE15/AN027
17	VR	PB00/AN008	18	AGND	- (AVSS)
19	AVCC	- (AVCC)	20	AVCC	- (AVCC)
21	AGND	- (AVSS)	22	AGND	- (AVSS)
23	VCC	- (VCC)	24	VCC	- (VCC)
25	GND	- (VSS)	26	GND	- (VSS)
27	UN	PB05/GTIOC4B_B	28	GND	- (VSS)
29	UP	PB04/GTIOC4A_B	30	GND	- (VSS)
31	VN	PB07/GTIOC5B_B	32	GND	- (VSS)
33	VP	PB06/GTIOC5A_B	34	GND	- (VSS)

Table 5-2 1st Inverter board connector (CN5) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	WN	PB09/GTIOC6B_B	2	GND	- (VSS)
3	WP	PB08/GTIOC6A_B	4	GND	- (VSS)
5	SPARE2	-	6	SPARE3	-
7	SPARE4	-	8	SPARE5	-
9	BUS_POWER_IN	-	10	INV_CONNECTED	-
11	SAFE_LOCK	-	12	OC#	PC13/GTETRGD
13	PFCERROR	P001/IRQ2	14	PFCPWM	PB14/GTIOC1A
15	VRL	PE01	16	SW1	PD04
17	SW2	PD07	18	LED1	PD01
19	LED2	PD02	20	LED3	PD03
21	HALL_U	PC04/IRQ10_B	22	HALL_V	PC05/IRQ11_B
23	HALL_W	PB01/IRQ1_B	24	MISO0/SIO_SDA	PC11/MISOB_B
25	SCK0/SCK_SCL	PC10	26	CSN_IRQN/ENC_Z	PE00/GTETRGA
27	IPS_A ENC_A	PC04 PC14/GTIOC3A_D	28	IPS_A#/ENC_A#	PC05/IRQ11_B
29	IPS_B ENC_B	PE15 PC15/GTIOC3B_D	30	IPS_B#//ENC_B#	PB10/AN028
31	GND	- (VSS)	32	GND	- (VSS)
33	+5V	-	34	+5V	-

Table 5-3 2nd Inverter board connector (CN7) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	SPARE1	-	2	AGND	- (AVSS)
3	VPN	PE13/AN025	4	AGND	- (AVSS)
5	IU	PB02/AN018	6	PGAVSSU	P002/PGAVSS3
7	IV	PE08/AN020	8	PGAVSSV	-
9	IW	PE09/AN021	10	PGAVSSW	-
11	VU	PE10/AN022	12	VV	PE11/AN023
13	VW	PE12/AN024	14	AGND	- (AVSS)
15	VAC	PC03/AN015	16	IPFC	PC02/AN014
17	VR	PE14/AN026	18	AGND	- (AVSS)
19	AVCC	- (AVCC)	20	AVCC	- (AVCC)
21	AGND	- (AVSS)	22	AGND	- (AVSS)
23	VCC	- (VCC)	24	VCC	- (VCC)
25	GND	- (VSS)	26	GND	- (VSS)
27	UN	PC09/GTIOC7B_A	28	GND	- (VSS)
29	UP	PC08/GTIOC7A_A	30	GND	- (VSS)
31	VN	PA09/GTIOC8B_A	32	GND	- (VSS)
33	VP	PA08/GTIOC8A_A	34	GND	- (VSS)

Table 5-4 2nd Inverter board connector (CN6) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	WN	PA11/GTIOC9B_A	2	GND	- (VSS)
3	WP	PA10/GTIOC9A_A	4	GND	- (VSS)
5	SPARE2	-	6	SPARE3	-
7	SPARE4	-	8	SPARE5	-
9	BUS_POWER_IN	-	10	INV_CONNECTED	-
11	SAFE_LOCK	-	12	OC#	PA12/GTETRGB
13	PFCERROR	P000/IRQ0	14	PFCPWM	PB15/GTIOC1B_A
15	VRL	PD11	16	SW1	PC00
17	SW2	PC01	18	LED1	PD15
19	LED2	PC06	20	LED3	PC07
21	HALL_U	PD12/IRQ12_B	22	HALL_V	PD13/IRQ13_B
23	HALL_W	PD14/IRQ13_B	24	MISO0/SIO_SDA	PC11/MISOB_B
25	SCK0/SCK_SCL	PC10	26	CSN_IRQN/ENC_Z	PD10/GTETRGC
27	IPS_A ENC_A	PC02 PD08/GTIOC2A_A	28	IPS_A#/ENC_A#	PC03/AN015
29	IPS_B ENC_B	PE11 PD09/GTIOC2B_A	30	IPS_B#//ENC_B#	PE12/AN024
31	GND	- (VSS)	32	GND	- (VSS)
33	+5V	-	34	+5V	-

(2) The pin assignments (CN4 to CN7) of Version 2 (RTK0EMA270C00002BJ) are shown below.

Table 5-5 1st Inverter board connector (CN4) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	HVtemp	PE15/AN027(*)	2	AGND	- (AVSS)
3	VPN	PA07/AN007	4	AGND	- (AVSS)
5	IU	PA04/AN004	6	PGAVSSU	PA05/PGAVSS2
7	IV	PA02/AN002	8	PGAVSSV	PA03/AN003(*)
9	IW	PA00/AN000	10	PGAVSSW	PA01/AN001(*)
11	VU	PE15/AN027	12	VV	PA03/AN003
13	VW	PA01/AN001	14	AGND	- (AVSS)
15	VAC	PB01/AN009(*)	16	IPFC	PC05/AN011(*)
17	VR	P000/AN016	18	AGND	- (AVSS)
19	AVCC	- (AVCC)	20	AVCC	- (AVCC)
21	AGND	- (AVSS)	22	AGND	- (AVSS)
23	VCC	- (VCC)	24	VCC	- (VCC)
25	GND	- (VSS)	26	GND	- (VSS)
27	UN	PB05/GTIOC4B_B	28	GND	- (VSS)
29	UP	PB04/GTIOC4A_B	30	GND	- (VSS)
31	VN	PB07/GTIOC5B_B	32	GND	- (VSS)
33	VP	PB06/GTIOC5A_B	34	GND	- (VSS)

(*) Exclusively assigned by jumper pin and jumper register setting

Table 5-6 1st Inverter board connector (CN5) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	WN	PB09/GTIOC6B_B	2	GND	- (VSS)
3	WP	PB08/GTIOC6A_B	4	GND	- (VSS)
5	SPARE2	-	6	PFCPWM2_1	PB12/GTIOC0A
7	SPARE4	-	8	SPARE5	-
9	BUS_POWER_IN	-	10	INV_CONNECTED	-
11	SAFE_LOCK	-	12	OC#	PC13/GTETRGD
13	PFCERROR	P001/IRQ2	14	PFCPWM	PB14/GTIOC1A
15	VRL	PE01	16	SW1	PD04
17	SW2	PD07	18	LED1	PD01
19	LED2	PD02	20	LED3	PD03
21	HALL_U	PB02/IRQ15DS	22	HALL_V	PC00/IRQ11DS
23	HALL_W	PB10/IRQ10DS	24	MISO0/SIO_SDA	PC11/MISOB_B
25	SCK0/SCK_SCL	PC10	26	CSN_IRQN/ENC_Z	PE00/GTETRGA
27	IPS_A ENC_A	PB02/AN018(*) PC14/GTIOC3A_D	28	IPS_A#/ENC_A#	PC00/AN012/IRQ11DS (*)
29	IPS_B ENC_B	PC05/AN011(*) PC15/GTIOC3B_D	30	IPS_B#/ENC_B#	PB01/AN009
31	GND	- (VSS)	32	GND	- (VSS)
33	+5V	-	34	+5V	-

(*) Exclusively assigned by jumper pin and jumper register setting

Table 5-7 2nd Inverter board connector (CN7) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	HVtemp	PE10/AN022(*)	2	AGND	- (AVSS)
3	VPN	PE13/AN025	4	AGND	- (AVSS)
5	IU	PA06/AN006	6	PGAVSSU	P002/PGAVSS3
7	IV	PB00/AN008	8	PGAVSSV	-
9	IW	PC04/AN010	10	PGAVSSW	-
11	VU	PE10/AN022	12	VV	PE11/AN023
13	VW	PE12/AN024	14	AGND	- (AVSS)
15	VAC	PC03/AN015(*)	16	IPFC	PC02/AN014(*)
17	VR	PC01/AN013	18	AGND	- (AVSS)
19	AVCC	- (AVCC)	20	AVCC	- (AVCC)
21	AGND	- (AVSS)	22	AGND	- (AVSS)
23	VCC	- (VCC)	24	VCC	- (VCC)
25	GND	- (VSS)	26	GND	- (VSS)
27	UN	PC09/GTIOC7B_A	28	GND	- (VSS)
29	UP	PC08/GTIOC7A_A	30	GND	- (VSS)
31	VN	PA09/GTIOC8B_A	32	GND	- (VSS)
33	VP	PA08/GTIOC8A_A	34	GND	- (VSS)

(*) Exclusively assigned by jumper pin and jumper register setting

Table 5-8 2nd Inverter board connector (CN6) pin assignment

Pin No	Pin Function	RA6T2 Pin	Pin No	Pin Function	RA6T2 Pin
1	WN	PA11/GTIOC9B_A	2	GND	- (VSS)
3	WP	PA10/GTIOC9A_A	4	GND	- (VSS)
5	SPARE2	-	6	PFCPWM2_2	PB13/GTIOC0B
7	SPARE4	-	8	SPARE5	-
9	BUS_POWER_IN	-	10	INV_CONNECTED	-
11	SAFE_LOCK	-	12	OC#	PA12/GTETRGB
13	PFCERROR	PC07/IRQ7	14	PFCPWM1_2	PB15/GTIOC1B_A
15	VRL	PD11	16	SW1	PE08
17	SW2	PE09	18	LED1	PD15
19	LED2	PC06	20	LED3	PE14
21	HALL_U	PD12/IRQ12_B	22	HALL_V	PD13/IRQ13_B
23	HALL_W	PD14/IRQ13_B	24	MISO0/SIO_SDA	PC11/MISOB_B
25	SCK0/SCK_SCL	PC10	26	CSN_IRQN/ENC_Z	PD10/GTETRGC
27	IPS_A ENC_A	PC02/AN014(*) PD08/GTIOC2A_A	28	IPS_A#/ENC_A#	PC03/AN015
29	IPS_B ENC_B	PE11/AN023(*) PD09/GTIOC2B_A	30	IPS_B#/ENC_B#	PE12/AN024
31	GND	- (VSS)	32	GND	- (VSS)
33	+5V	-	34	+5V	-

(*) Exclusively assigned by jumper pin and jumper register setting

The connection for CPU board and inverter board is shown in Figure 5-1.

(1) CPU Board + INV Board (connected with CN4, CN5)

(2) CPU Board + INV Board (connected with CN6, CN7)

(3) CPU Board + INV Board x2

Figure 5-1 Connection for CPU board and inverter board

5.1.4 Serial communication

For serial communication using Renesas Motor Workbench, the CPU board has SCI connector. Pin assignment for SCI connector is listed in Table 5-9.

Table 5-9 SCI connector (CN10) pin assignment

Pin No.	Pin Function	RA6T2 Connection Pin
1	GND	-
2	MCU RXD	PD06/RXD9_A
3	MCU TXD	PD05/TXD9_A
4	VCC	-

5.1.5 Reset circuit

This product has a reset circuit to enable power-on reset or external reset on MCU. Push the tact switch (SW1) to externally reset MCU.

5.1.6 LED

This product has six ports and LEDs, so that they can be used for program debug and the system. LED switches on when output from the corresponding port is “LOW” and switches off when output is “HIGH”. Pin assignment for corresponding LEDs is listed in Table 5-10,Table 5-11.

(1) The pin assignments LED of Version 1 (RTK0EMA270C00000BJ) are shown below.

Table 5-10 LED pin assignment 1

RA6T2 port		LED1	LED2	LED3	LED4	LED5	LED6
PD01	Output HIGH	OFF	-	-	-	-	-
	Output LOW	ON	-	-	-	-	-
PD02	Output HIGH	-	OFF	-	-	-	-
	Output LOW	-	ON	-	-	-	-
PD03	Output HIGH	-	-	OFF	-	-	-
	Output LOW	-	-	ON	-	-	-
PD15	Output HIGH	-	-	-	OFF	-	-
	Output LOW	-	-	-	ON	-	-
PC06	Output HIGH	-	-	-	-	OFF	-
	Output LOW	-	-	-	-	ON	-
PC07	Output HIGH	-	-	-	-	-	OFF
	Output LOW	-	-	-	-	-	ON

(2) The pin assignments LED of Version 2 (RTK0EMA270C00002BJ) are shown below.

Table 5-11 LED pin assignment 2

RA6T2 port		LED1	LED2	LED3	LED4	LED5	LED6
PD01	Output HIGH	OFF	-	-	-	-	-
	Output LOW	ON	-	-	-	-	-
PD02	Output HIGH	-	OFF	-	-	-	-
	Output LOW	-	ON	-	-	-	-
PD03	Output HIGH	-	-	OFF	-	-	-
	Output LOW	-	-	ON	-	-	-
PD15	Output HIGH	-	-	-	OFF	-	-
	Output LOW	-	-	-	ON	-	-
PC06	Output HIGH	-	-	-	-	OFF	-
	Output LOW	-	-	-	-	ON	-
PE14	Output HIGH	-	-	-	-	-	OFF
	Output LOW	-	-	-	-	-	ON

5.1.7 CAN Communication

This product has through holes for CAN communication. Note that CAN driver is not mounted. When using CAN communication with RTK0EMA270C00002BJ, install jumper resistors R3 and R103 and remove R104 and R105. Pin assignment for CAN communication connector is listed in Table 5-12.

Table 5-12 CAN communication pin assignment (CN8)

Pin No	RA6T2 pin
1	VCC
2	PB13/CTX0_E
3	PB12/CRX0_E
4	VSS

5.1.8 SPI communication

This product has through holes for SPI communication. Pin Assignment for SPI communication connector is listed in Table 5-13.

Table 5-13 SPI communication pin assignment (CN9)

Pin No	RA6T2 pin
1	PD00_SS0
2	PC12_MOSI0
3	PC11_MISO0/SIO_SDA
4	PC10_SCK0/SCK_SCL
5	VSS
6	VCC

6. Regulatory information

This is a ‘Class A’ (EN 61326-1: 2021) equipment. This equipment can cause radio frequency noise when used in the residential area. In such cases, the user/operator of the equipment may be required to take appropriate countermeasures under his responsibility.

7. Design and Manufacture Information

You can obtain information on the design and manufacture of this product from renesas.com.

8. Website and Support

In order to learn, download tools and documents, apply technical support for RA family MCU and its kit, visit the below Web site.

· RA Product Information renesas.com/ra

· RA Product Support Forum renesas.com/ra/forum

· Renesas Support renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	August 3, 2021	-	First edition
1.10	March 31, 2022	12	Modified Table 5-5
1.20	June 8, 2023	11	Modified Table 5-2
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