NEC

User's Manual

MC-CPU-V850ES/IK1

Micro-Board for µPD70F3329 Microcontroller for Use with Motor Control I/O Interface Board

Document No. U17980EU1V1UME0
Date Published August 2006

Printed in Germany

CAUTION

This is a Test- and Measurement equipment with possibility to be significantly altered by user through hardware enhancements/modifications and/or test or application software. Thus, with respect to Council Directive 89/336/EEC (Directive on compliance with the EMC protection requirements), this equipment has no autonomous function. Consequently this equipment is not marked by the CE-symbol.

EEDT-ST-0005-10

Redemption of Waste Electrical and Electronic Equipment (WEEE) in accordance with legal regulations applicable in the European Union only: This equipment (including all accessories) is not intended for household use. After use the equipment cannot be disposed of as household waste. NEC Electronics (Europe) GmbH offers to take back the equipment. All you need to do is register at www.eu.necel.com/weee.

Product specifications are subject to change without notice. To ensure that you have the latest product data, please contact your local NEC Electronics sales office.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

- **The information in this document is current as of August, 2006. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

  The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

  "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

  "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

  "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).

M8E 02. 11-1

For further information,
please contact:

NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668,
Japan
Tel: 044-435-5111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554, U.S.A.
Tel: 408-588-6000
800-366-9782
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211-65030
http://www.eu.necel.com/

Hanover Office
Podbielskistrasse 166 B
30177 Hannover
Tel: 0 511 33 40 2-0

Munich Office
Werner-Eckert-Strasse 9
81829 München
Tel: 0 89 92 10 03-0

Stuttgart Office
Industriestrasse 3
70565 Stuttgart
Tel: 0 711 99 01 0-0

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908-691-133

Succursale Française
9, rue Paul Dautier, B.P. 52180
78142 Velizy-Villacoublay Cédex
France
Tel: 01-3067-5800

Sucursal en España
Juan Esplandiu, 15
28007 Madrid, Spain
Tel: 091-504-2787

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 638 72 00

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02-667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven
The Netherlands
Tel: 040 265 40 10

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27 ZhiChunLu Haidian
District, Beijing 100083, P.R.China
Tel: 010-8235-1155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2509-2510, Bank of China Tower,
200 Yincheng Road Central,
Pudong New Area, Shanghai P.R. China P.C:200120
Tel: 021-5888-5400
http://www.cn.necel.com/

NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
Tel: 2886-9318
http://www.hk.necel.com/

Seoul Branch
11F., Samik Lavied'or Bldg., 720-2,
Yeoksam-Dong, Kangnam-Ku,
Seoul, 135-080, Korea
Tel: 02-558-3737

NEC Electronics Taiwan Ltd.
7F, No. 363 Fu Shing North Road
Taipei, Taiwan, R. O. C.
Tel: 02-8175-9600
http://www.tw.necel.com/

NEC Electronics Singapore Pte. Ltd.
238A Thomson Road,
#12-08 Novena Square,
Singapore 307684
Tel: 6253-8311
http://www.sg.necel.com/

G06.8A

[MEMO]

Preface

Readers

This manual is intented for users who want to understand the functions of the MC-CPU-V850ES/IK1 micro-board for µPD70F3329 microcontroller for use with motor control I/O interface board.

Purpose

This manual presents the hardware manual of the MC-CPU-V850ES/IK1 micro-board for µPD70F3329 microcontroller for use with motor control I/O interface board.

Organization

This system specification describes the following sections:

- V850ES/IK1 micro-board system specifications
- Hardware
- Micro-board connections to the MC-IO board
- Schematics

Legend

Symbols and notation are used as follows:

Weight in data notation	:	Left is high-order column, right is low order column
Active low notation	:	$\overline{xxx}$ (pin or signal name is over-scored) or /xxx (slash before signal name)
Memory map address:	:	High order at high stage and low order at low stage
Note	:	Explanation of (Note) in the text
Caution	:	Item deserving extra attention
Remark	:	Supplementary explanation to the text
Numeric notation	:	Binary... xxxx or xxxB Decimal... xxxx Hexadecimal... xxxxH or 0x xxxx

Prefixes representing powers of 2 (address space, memory capacity)

K (kilo): $2^{10} = 1024$

M (mega): $2^{20} = 1024^2 = 1,048,576$

G (giga): $2^{30} = 1024^3 = 1,073,741,824$

Table of Contents

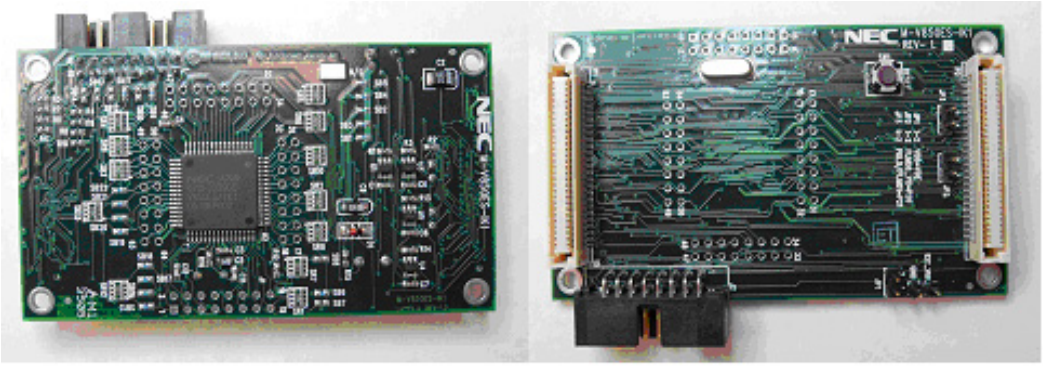
List of Figures

List of Tables

Chapter 1 Introduction

The MC-CPU-V850ES/IK1 micro-board is designed to demonstrate and evaluate CPU and on-chip peripheral functions of the NEC Electronics 32-bit μPD70F3329 microcontroller (MCU).
The MC-CPU-V850ES/IK1 micro-board can be operated as a stand-alone mode to evaluate the main features of the MCU or it can be connected through two 100-pin connectors to a separately sold motor control interface board (MC-IO-GENERAL) to evaluate the MCU's dedicated 3-phase motor control peripherals. The micro-board also may be used with a low-cost evaluation system called the M-Station (sold in the U.S. only). This manual only describes configuration and operation of the MC-CPU-V850ES/IK1 when used with the MC-IO board.

Figure 1-1: MC-CPU-V850ES/IK1 Micro-Board



Chapter 2 MC-CPU-V850ES/IK1 Micro-Board System Specifications

The MC-CPU-V850ES/IK1 micro-board has the µPD70F3329 microcontroller as its main controller. Specifications for the microcontroller and the board are listed below.

2.1 Microcontroller Features

- 128 KB flash program memory
- 6 KB high-speed data RAM
- 39 I/O ports
- Two units of 10-bit, 4-channel A/D converter
- Serial interfaces
  - Two-channel UARTA
  - One-channel, 3-wire variable-length serial I/O
- Timers
  - One-channel, 10-bit interval timer (TMM)
  - Two-channel, 16-bit timer event counter (TMQ)
  - Four-channel, 16-bit timer event counter (TMP)
  - One-channel, 16-bit motor control function (TMQ1)
  - One-channel, six-phase pulse-width modulator with 16-bit accuracy
  - One-channel watchdog timer
  - Timer output controls
  - High-impedance output control
  - Timer-tuning operation
- Arbitrary cycle-setting function
- Arbitrary dead time-setting function
- Vectored interrupts
  - Non-maskable interrupt: one source (internal NMI)
  - Maskable interrupts: 42 sources
  - Software exceptions: 32 sources
  - Exception traps: two sources
  - External NMI: none
- Power supply voltages
  - $V_{DD} = EV_{DD} = 3.5\ V_{DC}$ to $5.5\ V_{DC}$
  - AV_{DD0} and $AV_{DD1} = 4.5\ V_{DC}$ to $5.5\ V_{DC}$
- 64-pin plastic LQFP 14 × 14 mm (µPD70F3329GC-8BS)

Reference: µPD70F3329 User's Manual (U16910EJ2V0UD00, 2nd Edition, June 2004)

2.2 Micro-Board Features

- 4.0 MHz on-board crystal oscillator
- Connector that provides all I/O pins of the µPD70F3329 microcontroller
- Board size of 3.5 × 2 inches (W × L)
- 16-pin connector for debugging and flash programming interface.

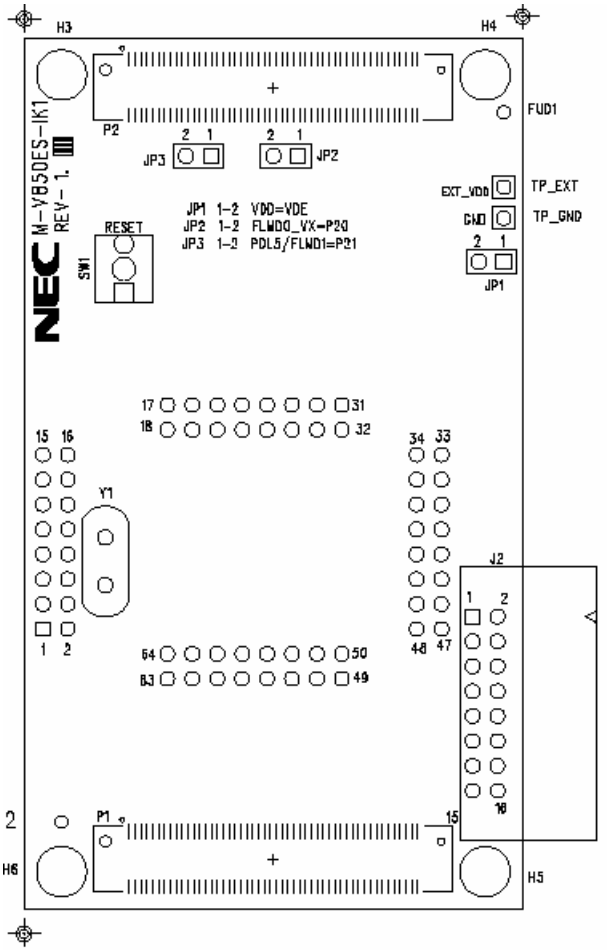
[MEMO]

Chapter 3 Hardware

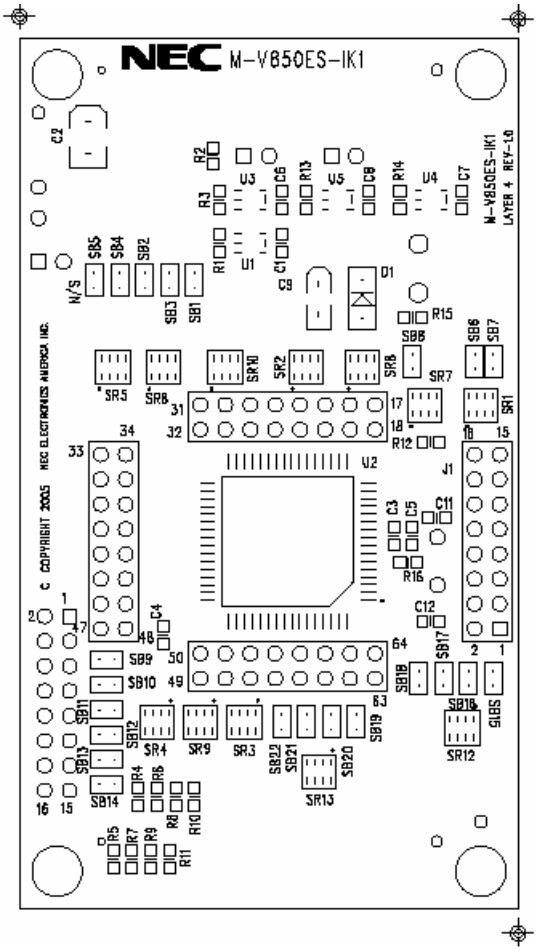
3.1 Physical Placement of Components

Figure 3-1: Component Placement on Micro-Board

Top



Bottom



3.2 Default Jumper Settings

Table 3-1: Micro-Board Jumper Settings

Jumper	Setting	Function	Description
JP1	1–2	V_{DD} to V_{DE}	µPD70F3329 V_{DD} coming from V_{DE} or External_V_{DD}
JP2	OPEN	FLMD0 for self-programming	Connect FLMD0 input to P20 for flash self-program mode set
JP3	OPEN	FLMD1 for self-programming	Connect FLMD1 input to P21 for flash self-program mode set

3.3 Operation

3.3.1 Demonstration configuration

You can use the MC-CPU-V850ES/IK1 micro-board to demonstrate the functions of the microcontroller and its on-chip peripherals in standalone mode by executing programs loaded into on-chip flash memory.

3.3.2 Debugging configuration

To debug an user program, you must remove the microcontroller from the MCU board and install a socket to accommodate an in-circuit emulator called the IECUBE. For IECUBE part numbers and availability, please contact your local NEC Electronics support representative.

3.4 Reprogramming the Flash Memory of the µPD70F3329

You can reprogram the on-chip flash memory at any time. To do so, use the PG-FP4-E or PG-FPL flash programmers. For programmer part numbers and availability, please contact your local NEC Electronics America support representative.

3.5 Measuring Power Consumption of the µPD70F3329

The JP1 power select jumper can provide a connection to an ampere meter for accurate measurement of the µPD70F3329's power consumption, regardless of which power source is selected. Use this procedure to measure power consumption for the µPD70F3329:

1. Remove the power select jumper on JP1.
2. Connect an ampere meter on JP1 terminals.

Table 3-2: 2JP1 Micro-Board Current Measurement Terminal

JP1 Setting	Selected Power Source	Remarks
1 to 2	Connect with jumper (V_{DD1} to V_{DE})	Default
1 to 2	Connect with ampere meter (CPU current measurement)	

Special Note on Power Measurement for the µPD70F3329:
Because JP1 is a dedicated terminal for measuring power to the µPD703329, the MC-CPU-V850ES/IK1 micro-board can remain connected to the MC-IO board during power measurement.

3.6 On-Board Components

3.6.1 J2 16-pin flash programming interface header

The J2 16-pin header provides a flash-programming interface for the MC-CPU-V850ES/IK1. To reprogram the on-chip flash memory, use either the PG-FP4-E or PG-FPL flash programmers. (For programmer part numbers and availability, please contact your local NEC Electronics America support representative.)

Figure 3-2: Layout of the J2 Debugging and Flash Programming Interface Connector

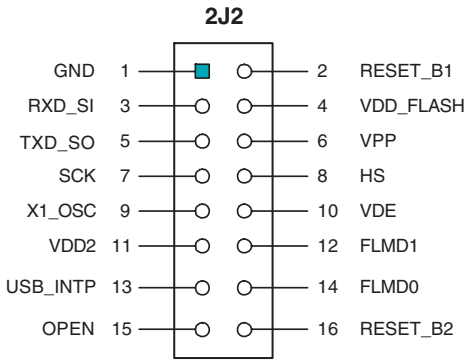


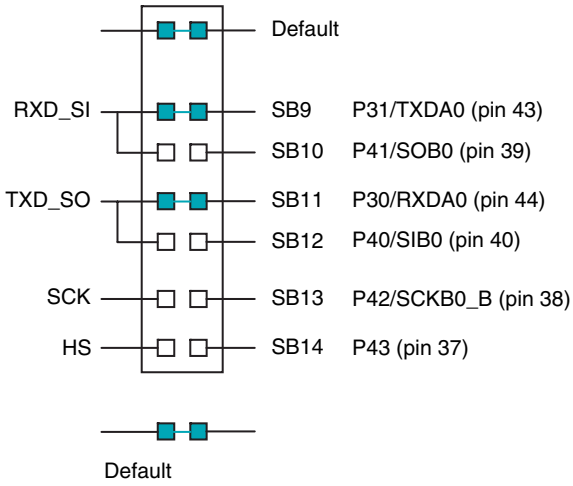
Table 3-3: Pin Assignments of the J2 Debugging and Flash Programming Interface Connector

Pin No.	MV850ES/IK1	PG-FP4-E Flash Programmer
1	GND	GND
2	RESET_B1	Reset to M-78F0714
3	RXD_SI	Serial I/O or UART data receive
4	VDD_FLASH	VDD from flash programmer
5	TXD_SO	Serial I/O or UART data transmit
6	V_{PP}	Not used
7	SCK	SCK
8	HS	Handshake
9	X1_OSC	Clock to M-78F0714
10	V_{DE}	V_{DD}
11	VDD2	Not used
12	FLMD1	Not used
13	USB_INTP	Not used
14	FLMD0	FLMD0
15	OPEN	
16	RESET_B2	Not used

3.6.2 Flash/debugging interface signal select

You can use the SBx array of solder blobs to select UARTA0 or the CSIB0 port on the µPD70F3329 for connection to the J2 (16-pin header) debugging and flash programming interface. (PG-FPL supports only the UARTA0 port.) The default settings shown in Figure 4 are configured to program the flash memory through UARTA0.

Figure 3-3: SBx Array



3.6.3 VDE and TP_EXTVDD1

The MC-CPU-V850ES/IK1 micro-board can obtain VDD from two sources. The first source is external power (EXT_VDD) supplied by the user. The external power should be 3.5 to 5.5 V_{DC}. The second power source is VDE from the MC-IO board when the MC-CPU-V850ES/IK1 is connected through the 100-pin connectors P1 and P2.

3.6.4 Main clock oscillator

A 4.0 MHz-crystal oscillator (Y1) is mounted on the micro-board to serve as the board's main clock. You can remove the 4.0 MHz crystal oscillator on the micro-board if you wish and mount a different crystal oscillator. Recommended quartz crystal oscillators include the Citizen HC49US Series. These oscillators use 18 pF biasing capacitors to set a range of frequencies. An 18 pF biasing capacitor is mounted on the MC-CPU-V850ES/IK1.

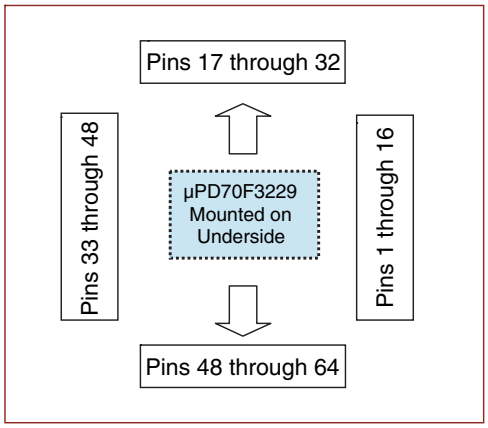
3.6.5 Sub-clock selection

The sub-clock is not supported for the µPD70F3229.

3.6.6 1 J1: µPD70F3229 I/O pin array

J1 is a pin array connecting to the µPD70F3229 I/O pins and provides an optional way to mount the MC-CPU-V850ES/IK1 micro-board directly onto your target system. J1 also allows easy access to all I/O pins. J1 is divided into four groups of 16 pins around the µPD70F3229.

Figure 3-4: J1 Pin Array Layout



3.6.7 Switch SW1

Pressing the SW1 push-button switch connects the RESET pin of the µPD70F3229 to GND, resetting the µPD70F3229.

3.6.8 Jumper settings for self flash programming

You can program the flash memory on the µPD70F3329 using the self-programming method. You can develop the self-programming code using libraries available from NEC Electronics America.

Table 3-4: JP2: FLMD0 Connection for Flash Self-Programming Mode

JP2 Setting	Selected Power Source	Remarks
1 to 2	Open: normal operation	Default
1 to 2	Connect P20 drives FLMD0 for flash programming mode	

Table 3-5: JP3: FLMD01 Connection for Flash Self-Programming Mode

JP3 Setting	Selected Power Source	Remarks
1 to 2	Open: normal operation	Default
1 to 2	Connect P21 drives FLMD1 for flash programming mode	

3.6.9 Solder blob select option

Several signals of the µPD70F3229 are connected to the SBx solder blobs. SBx is formed with two pads, making it easy to connect or disconnect with blobs of solder.

Figure 3-5: SBx Solder Blob Configuration

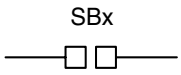


Table 3-6: SBx Connections

SBx	Description of Connection	Default
SB1	Optional connection for EV_{DD} to V_{DD}	Connected
SB2	Optional connection for AV_{REF0} to V_{DD}	Connected
SB3	Optional connection for AV_{REF1} to V_{DD}	Connected
SB4	Optional connection for AV_{DD0} to V_{DD}	Connected
SB5	Optional connection for AV_{DD1} to V_{DD}	Connected
SB6	Motor control application “speed measurement” input selection	Connected
SB7		Open
SB8		Open
SB9	Optional connection for RXD_SI to P31/TXDA0	Connected
SB10	Optional connection for RXD_SI to P41/SOB0	Open
SB11	Optional connection for TXD_SO to P30/RXDA0	Connected
SB12	Optional connection for TXD_SO to PP40/SIB0	Open
SB13	Optional connection for SCK to PP42/SCKB0_B	Open
SB14	Optional connection for HS to P43	Open
SB15–SB22	Optional termination with 1 MΩ for ANI0[3:0] and ANI1[3:0]	Connected

Note: Speed measurement input

INTP1_PX, INTP2_PY and INTP3_PZ are signals from the MC-IO board that provide sensor (HALL or back-EMF) inputs. The selected INTP_x signal is input to P12/TIQ03 (capture/compare register) of the on-chip timer for speed measurements.

Chapter 4 Micro-Board Connections to the MC-IO Board

Two 100-pin connectors connect all µPD70F3229 signals to the MC-IO board. The µPD70F3229 signals are arranged so that certain signals are connected to the motor control function signals on the MC-IO board, while the others can be used for prototyping. All signals are connected to pre-assigned positions of the P1 and P2 connectors.

The selected port signals are scrambled to connect to pre-assigned positions. These pins are duplicated, in most cases, to maintain contiguous 8-bit blocks. The P1 and P2 connectors also carry host communication and flash programming interface signals.

Table 4-1: P1 Connector Pin Assignments (1/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P1 Pin Number	Pin Name	CPU Pin Number	J1 Pin Number	Pin Name	
1	GND		1	GND_IS	CPU ground
2	GND		2	GND_IS	CPU ground
3	P32	42	3	RS232_RXD	RS-232 transceiver TXD output
4	P26	46	4	RS232_CTS	RS-232 transceiver CTS output
5	P33	41	5	RS232_TXD	RS-232 transceiver RXD input
6	P27	45	6	RS232_RTS	RS-232 transceiver RTS output
7	P03	14	7	J1007	
8	P04	13	8	J1008	
9	ANI00	1	9	J1009	
10			10	J1010	
11	P01	16	11	PX_ITRIP	Over-current detection
12	P00	17	12	J1012	
13			13	J1013	
14	P02	15	14	J1014	
15	P03	14	15	J1015	
16	P04	13	16	J1016	
17	P05	12	17	J1017	
18	P06	11	18	J1018	
19	ANI00	1	19	J1019	
20	ANI01	2	20	J1020	
21	ANI02	3	21	J1021	
22	ANI03	57	22	J1022	
23	ANI10	58	23	ANI4	
24	ANI11	4	24	ANI5_ISHUNT	Common current shunt
25	ANI12	56	25	ANI6_SPARE	Spare analog
26	ANI13	55	26	J1026	
27	P10	24	27	J1027	
28	P11	23	28	J1028	
29	P12	22	29	J1029	
30	P13	21	30	J1030	

Table 4-1: P1 Connector Pin Assignments (2/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P1 Pin Number	Pin Name	CPU Pin Number	J1 Pin Number	Pin Name	
31	P14	20	31	P54_TRIPB	
32	P16	19	32	J1032	
33	P17	18	33	J1033	
34			34	J1034	
35	PDL0	35	35	J1035	
36	PDL1	34	36	J1036	
37	PDL2	33	37	J1037	
38	PDL3	32	38	J1038	
39	PDL4	31	39	J1039	
40	PDL5	30	40	J1040	
41	PDL6	29	41	J1041	
42	PDL7	28	42	J1042	
43	P20	54	43	J1043	
44	P21	53	44	J1044	
45	P22	52	45	J1045	
46	P23	51	46	J1046	
47	P24	50	47	J1047	
48	P25	49	48	J1048	
49	P26	46	49	J1049	
50	P27	45	50	J1050	
51	P30	44	51	J1.051	
52	P31	43	52	J1.052	
53	P32	42	53	J1.053	
54	P33	41	54	J1.054	
55			55	J1.055	N/A
56			56	J1.056	N/A
57			57	J1.057	N/A
58			58	J1.058	
59	P40	40	59	J1059	
60	P41	39	60	J1060	
61	P42	38	61	J1061	
62	P43	37	62	J1062	
63	P44		63	J1063	
64			64	J1064	
65			65	J1065	
66			66	J1066	
67			67	J1067	
68			68	J1068	
69			69	J1069	
70			70	J1070	

Table 4-1: P1 Connector Pin Assignments (3/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P1 Pin Number	Pin Name	CPU Pin Number	J1 Pin Number	Pin Name	
71	EVDD	26	71	J1071	
72	EVDD	47	72	J1072	
73			73	J1073	
74			74	J1074	
75	RESET_B1		75		
76	RXD_SI		76		
77	TXD_SO		77		
78	VPP		78		
79	GND		79		
80	HS		80		
81	SCK		81		
82			82		
83	GND		83		
84	VDE		84		
85	X1_OSC		85		
86	VDE		86		
87	GND		87		
88	FLMD0		88		
89	BDID7		89		
90	FLMD1		90		
91	RESET_B2		91		
92	BDID0		92		
93	BDID1		93		
94	BDID2		94		
95	BDID3		95		
96	BDID4		96		
97	BDID5		97		
98	BDID6		98		
99	VDE		99	VCC_IS	Flash programmer V_{DD}
100	VDE		100	VCC_IS	Flash programmer V_{DD}

Table 4-2: P2 Connector Pin Assignments (1/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P2 Pin Number	Pin Name	CPU Pin Number	J2 Pin Number	Pin Name	
1	GND		1	GND_IS	CPU ground
2	GND		2	GND_IS	CPU ground
3	P30	44	3	J2003	
4	P26	46	4	J2004	
5	P31	43	5	J2005	
6	P27	45	6	J2006	
7	P05	12	7	J2007	
8	P06	11	8	J2008	
9	ANI13	55	9	J2009	
10	TG_RST		10	J2010	
11			11	J2011	
12			12	J2012	
13			13	J2013	
14			14	J2014	
15	P40	40	15	LED0	I/O board: LED data latch 0
16	P41	39	16	LED1	I/O board: LED data latch 1
17	P42	38	17	LED2	I/O board: LED data latch 2
18	P43	37	18	LED3	I/O board: LED data latch 3
19	PDL0	35	19	LED_A	I/O board: LED segment A
20	PDL1	34	20	LED_B	I/O board: LED segment B
21	PDL2	33	21	LED_C	I/O board: LED segment C
22	PDL3	32	22	LED_D	I/O board: LED segment D
23	PDL4	31	23	LED_E	I/O board: LED segment E
24	PDL5	30	24	LED_F	I/O board: LED segment F
25	PDL6	29	25	LED_G	I/O board: LED segment G
26	PDL7	28	26	LED_DP	I/O board: LED decimal point
27	GND		27	GND_IS	CPU ground
28	GND		28	GND_IS	CPU ground
29	P20	54	29	PWM_0	Phase U high
30	P21	53	30	PWM_1	Phase U low
31	GND		31	GND_IS	CPU ground
32	GND		32	GND_IS	CPU ground
33	P22	52	33	PWM_2	Phase V high
34	P23	51	34	PWM_3	Phase V low
35	GND		35	GND_IS	CPU ground
36	GND		36	GND_IS	CPU ground
37	P24	50	37	PWM_4	Phase W high
38	P25	49	38	PWM_5	Phase W low

Table 4-2: P2 Connector Pin Assignments (2/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P2 Pin Number	Pin Name	CPU Pin Number	J2 Pin Number	Pin Name	
39	GND		39	GND_IS	CPU ground
40	GND		40	GND_IS	CPU ground
41	P12	22	41	SPD_MSR	Speed measurement
42	GND		42	GND_IS	CPU ground
43	ANI12	56	43	J1043	Spare analog
44	ANI13	55	44	ANI7_TMP	Motor temperature
45	GND		45	GND_IS	CPU ground
46	GND		46	GND_IS	CPU ground
47	P02	15	47	INTP1_PX	To Hall 1/BEMF1 selector (2JP8)
48	P03	14	48	INTP_PY	To Hall 2/BEMF2 selector (2JP9)
49	GND		49	GND_IS	CPU ground
50	GND		50	GND_IS	CPU ground
51	P04	13	51	INTP3_PZ	To Hall 3/BEMF3 selector (2JP10)
52	ANI00	1	52	ANI0IU	Phase U current
53	GND		53	GND_IS	CPU ground
54	GND		54	GND_IS	CPU ground
55	ANI01	2	55	ANI1_IV	Phase V current
56	ANI02	3	56	ANI2_IW	Phase W current
57	GND		57	GND_IS	CPU ground
58	GND		58	GND_IS	CPU ground
59	ANI11	57	59	ANI3_TEMP	Power module temperature
60	P13	21	60	PX_ENCA	Motor shaft encoder
61	GND		61	GND_IS	CPU ground
62	GND		62	GND_IS	CPU ground
63	P10	24	63	PX_ENCB	Motor shaft encoder
64	P11	23	64	PX_ENCZ	Motor shaft encoder
65	GND		65	GND_IS	CPU ground
66	GND		66	GND_IS	CPU ground
67	P05	12	67	PX_START	START/STOP push button
68	P17	18	68	PX_FORWARD	FORWARD push button
69	GND		69	GND_IS	CPU ground
70	GND		70	GND_IS	CPU ground
71	P16	19	71	PX_REVERSE	REVERSE push button
72	P06	11	72	PX_MODE	MODE push button
73	GND		73	GND_IS	CPU ground
74	GND		74	GND_IS	CPU ground
75			75		
76			76		
77			77		

Table 4-2: P2 Connector Pin Assignments (3/3)

MC-CPU-V850ES/IK1 Micro-Board			MC-IO Board		Motor Control Function
P2 Pin Number	Pin Name	CPU Pin Number	J2 Pin Number	Pin Name	
78			78		
79	VDD	9	79	VDD_KX	External CPU V_{DD}
80	EVDD	26	80	VDD1	CPU EV_{DD}
81			81	J2081	
82	AVREF	64	82	AVREF	CPU AV_{REF}
83	AVDD0		83	AVDD	CPU AV_{DD}
84	TG_RST	63	84	J2084	
85	X1_OSC		85	TG_RST	CPU reset from target
86	FLMD0_VX	5	86	VPP_FLMD0	CPU FLMD0
87		25	87	J2087	
88			88	X1	CPU X1
89			89	X2	CPU X2
90			90	J2090	
91			91	J2091	
92			92	J2092	
93			93	J2093	
94			94	J2094	
95			95	J2095	
96			96	J2096	
97			97	J2097	
98			98	J2098	
99	VDE		99	VCC_IS	Flash programmer V_{DD}
100	VDE		100	VCC_IS	Flash programmer V_{DD}

Chapter 5 Schematics