NEC

LCE-789418-EM
Emulation Board for
LCE-K0S Development System

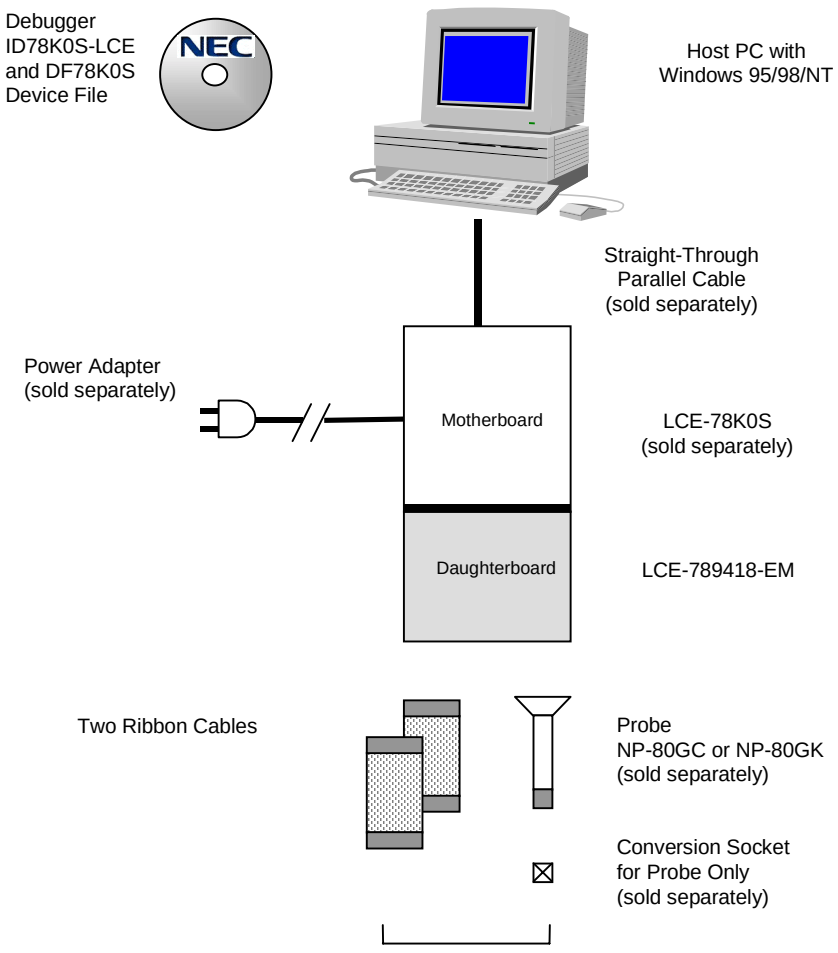
User's Manual ***July 2000***

Introduction

The LCE-789418-EM is an emulation board or daughterboard for the LCE-K0S development system for NEC's 8-bit μPD789418 subseries microcontrollers. Combining this board with the LCE-78K0S allows you to efficiently emulate any μPD789418 subseries device. The LCE-789418-EM is shipped with the following contents:

- LCE-789418-EM daughterboard
- User's manual
- Two 50-pin ribbon cables
- CD-ROM containing debugger, compiler, assembler, and documentation

Figure 1. System Configuration



Two Methods of Connecting the LCE-K0S to the User Target

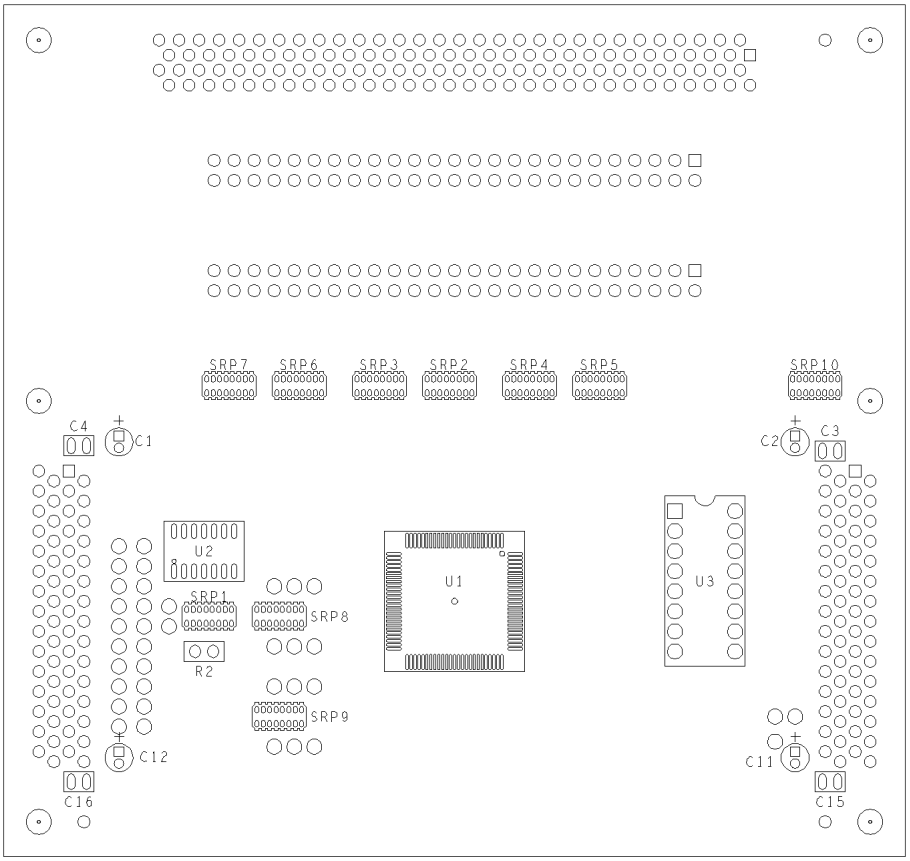
Table 1. Basic Specifications

Parameter	Description
Target device	µPD789405
	µPD789406
	µPD789407
	µPD789415
	µPD789416
	µPD789417
	µPD789418
Clock supply	Internal: installed on the motherboard
	External: pulse input via an emulation probe from target system
Low-voltage compatible	At least 2 volts

Components

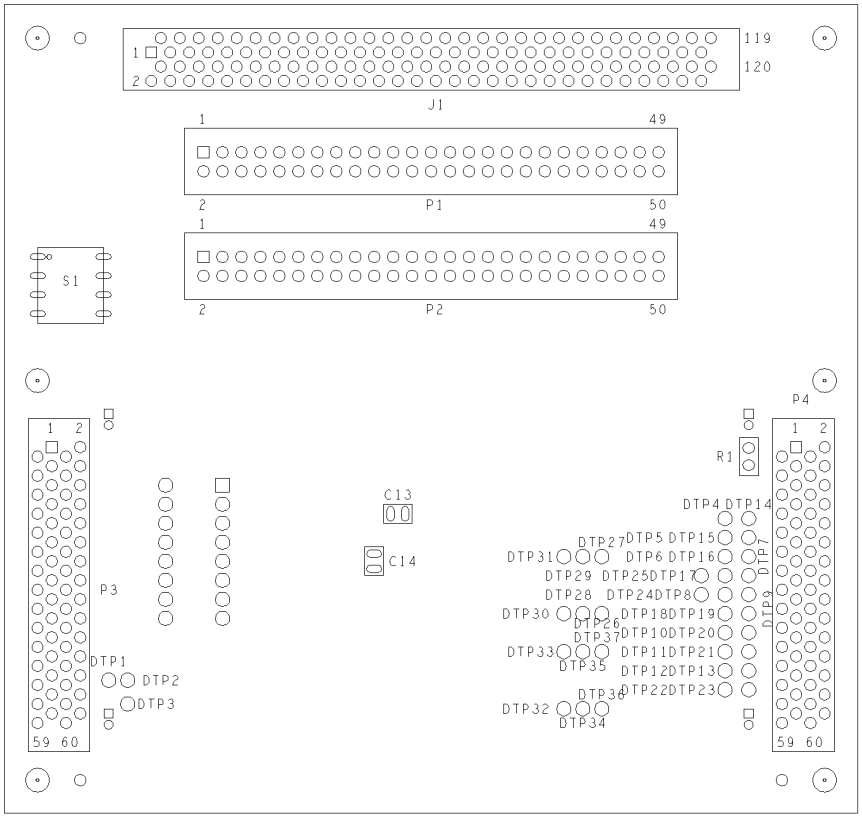
The LCE-789418-EM daughterboard mates with the LCE-78K0S motherboard. In other words, the top of the daughterboard faces down in the system. As shown in Figure 2, a bottom view of the daughterboard, U1 is the Realchip that provides peripherals unique to the µPD789418 devices. U3 is the user-defined LCD division resistor ladders.

Figure 2. Bottom View of Daughterboard



In the top view shown in Figure 3, J1, P1, and P2 are connectors to the user target. These connectors contain all of the pins available on the device. J1 is a KEL connector for the probe, while P1 and P2 are dual-row, male-shrouded headers with latching levers for the ribbon cables. See Tables 2-4 for pin assignments. S1 is a DIP switch for enabling or disabling pull-up resistors on the input pins for mask ROM. P3 and P4 are connectors for the motherboard, which attaches to the top of the daughterboard.

Figure 3. Top View of Daughterboard



Ribbon Cable

The ribbon cable is a 50-pin female-to-female cable that connects the LCE-K0S to the user target. Alternatively, an emulation probe may be used. One end of the ribbon cable connects to the daughterboard and the other to the target. Since all devices in this product group are 80-pin devices, two ribbon cables are shipped with the daughterboard. The side of the ribbon cable with a red stripe is pin 1.

Table 2. P1 Pin Assignments

P1 Connector	µPD7894xx Device Pin	Signal	Note
1			GND on probe cable
2			GND on probe cable
3			GND on probe cable
4			GND on probe cable
5	1	VDD1	PB_VDD is voltage sense; tied to pin 71, VDD0
6	2	BIAS	
7	3	VLC0	
8	4	VLC1	
9	5	VLC2	
10	6	VSS1	VSS1 is tied to GND
11	7	COM0	
12	8	COM1	
13	9	COM2	
14	10	COM3	
15	11	S0	
16	12	S1	
17	13	S2	
18	14	S3	
19	15	S4	
20	16	S5	
21	17	S6	
22	18	S7	
23	19	S8	
24	20	S9	
25	21	S10	
26	22	S11	
27	23	S12	
28	24	S13	
29	25	S14	
30	26	S15	
31	27	P93/S16	
32	28	P92/S17	
33	29	P91/S18	
34	30	P90/S19	
35	31	P87/S20	
36	32	P86/S21	
37	33	P85/S22	

Table 2. P1 Pin Assignments (continued)

P1 Connector	µPD7894xx Device Pin	Signal	Note
38	34	P84/S23	
39	35	P83/S24	
40	36	P82/S25	
41	37	P81/S26	
42	38	P80/S27	
43			GND on probe cable
44			GND on probe cable
45			GND on probe cable
46			GND on probe cable
47			GND on probe cable
48			GND on probe cable
49			GND on probe cable
50			GND on probe cable

Table 3. P2 Pin Assignments

P2 Connector	µPD7894xx Device Pin	Signal	Note
1			GND on probe cable
2			GND on probe cable
3			GND on probe cable
4			GND on probe cable
5	39	AVDD	
6	40	AVREF	
7	41	P66/ANI6	
8	42	P65/ANI5	
9	43	P64/ANI4	
10	44	P63/ANI3	
11	45	P62/ANI2	
12	46	P61/ANI1/ CMPREF0	
13	47	P60/ANI0/ CMPIN0	
14	48	AVSS	AVSS is tied to GND
15	49	P27/INTP3/CPT5	
16	50	P26/INTP2/TO5	
17	51	P25/INTP1/TI1	
18	52	P24/INTP0/TI0	
19	53	P23/CMPTOUT0/ TO2	
20	54	P22/SI/RXD	
21	55	P21/SO/TXD	
22	56	P20/SCK/ASCK	
23	57	P53	

Table 3. P2 Pin Assignments (continued)

P2 Connector	µPD7894xx Device Pin	Signal	Note
24	58	P52	
25	59	P51	
26	60	P50	
27	61	P03	
28	62	P02	
29	63	P01	
30	64	P00	
31	65	P47	
32	66	P46	
33	67	$\overline{\text{RESET}}$	Negative true
34	68	X2	Not connected in LCE-789418-EM
35	69	X1	External clock input for oscillator on target
36	70	VSS0	Tied to GND
37	71	VDD0	PB_VDD is used for voltage sense; tied to pin 1, VDD1
38	72	XT2	Not connected in LCE-789418-EM
39	73	XT1	External subclock input for oscillator on target
40	74	TEST/VPP	Not connected in LCE-789418-EM
41	75	P45/KR5	
42	76	P44/KR4	
43	77	P43/KR3	
44	78	P42/KR2	
45	79	P41/KR1	
46	80	P40/KR0	
47			GND on probe cable
48			GND on probe cable
49			GND on probe cable
50			GND on probe cable

Emulation Probe (Optional)

In place of ribbon cables, an emulation probe can be used to connect the LCE to the user target, provided the target has a conversion socket/adapter installed.

Table 4. Emulation Probe Pin Assignments

Emulation Device Pin No.	J1 Pin No.	Emulation Device Pin No.	J1 Pin No.
1	114	41	8
2	113	42	7
3	108	43	14
4	107	44	13
5	104	45	18
6	103	46	17
7	100	47	22
8	99	48	21
9	94	49	28
10	93	50	27
11	30	51	92
12	29	52	91
13	24	53	98
14	23	54	97
15	20	55	102
16	19	56	101
17	16	57	106
18	15	58	105
19	10	59	112
20	9	60	111
21	37	61	83
22	43	62	77
23	44	63	78
24	47	64	73
25	48	65	74
26	51	66	69
27	52	67	70
28	57	68	63
29	58	69	64
30	59	70	61
31	60	71	62
32	55	72	65
33	56	73	66
34	49	74	71
35	50	75	72
36	45	76	75
37	46	77	76
38	41	78	79
39	42	79	80
40	35	80	85

Table 5. Emulation Probe and Socket for µPD789418 Subseries

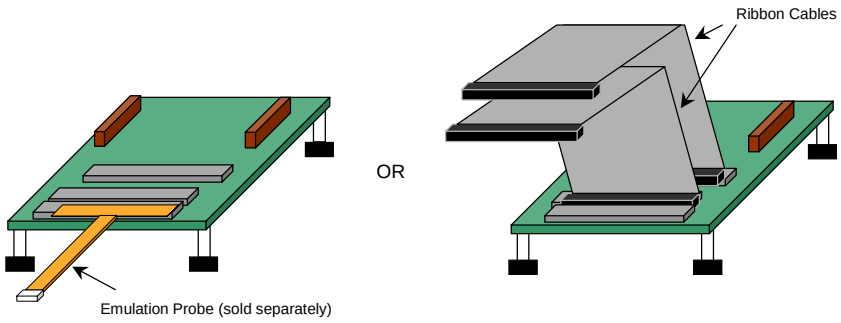
Target Device	Emulation Probe + Conversion Socket
µPD789405GC	NP-80GC + EV-9200G-C-80 or NP-80GC-TQ + EV-TGC-080SBP
µPD789406GC	
µPD789407GC	
µPD789415GC	
µPD789416GC	
µPD789417GC	
µPD78F9418GC	
µPD789405GK	NP-80GK + EV-TGK-080SDW
µPD789406GK	
µPD789407GK	
µPD789415GK	
µPD789416GK	
µPD789417GK	
µPD78F9418GK	

Assembly

This procedure explains how to connect the LCE-789418-EM to the LCE-78K0S motherboard.

1. Connect the probe or ribbon cables to their respective connectors on the LCE-789418-EM (Figure 4). Note that the number of KEL connectors, headers, and ribbon cables shown in Figure 4 may be different in other emulation boards.

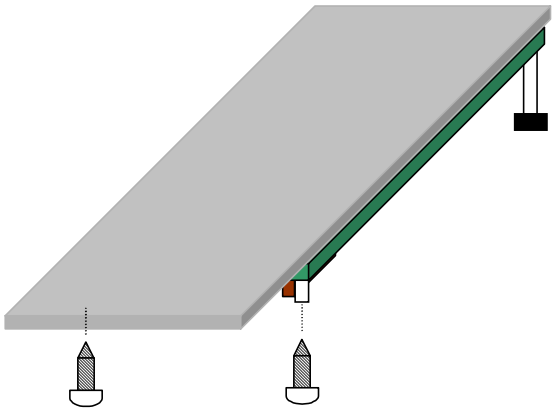
   Figure 4. Connections for Emulation Probe or Ribbon Cables



2. Make sure power is off from the LCE-78K0S motherboard.

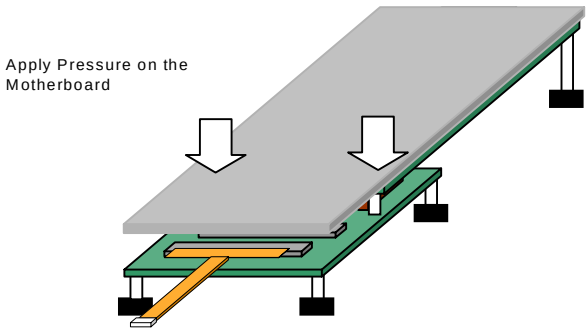
3. Remove the two screws at the bottom of the standoffs on the motherboard (Figure 5).

Figure 5. Screws on Bottom of Motherboard



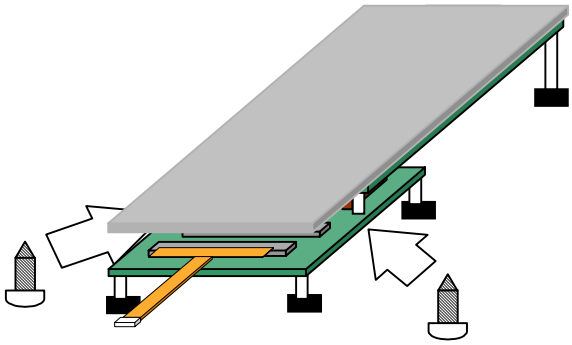
4. With the daughterboard on a stable surface, connect the motherboard on the daughterboard by gently applying pressure on the mating connectors. Avoid applying too much pressure on the plastic cover (Figure 6).

Figure 6. Daughterboard Mating Connectors



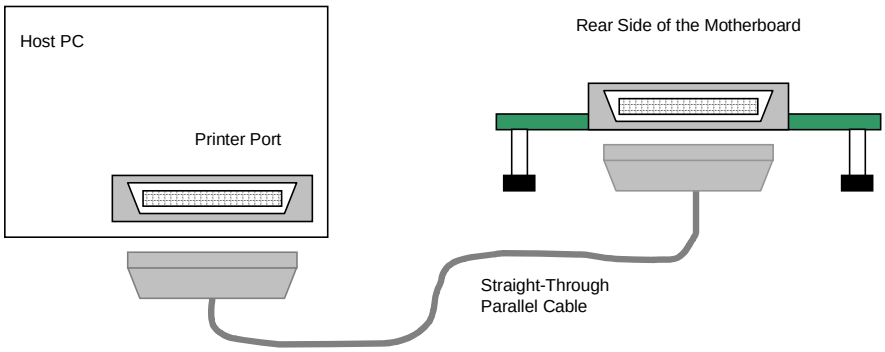
5. Replace the screws on the bottom of the daughterboard to securely connect it to the motherboard (Figure 7).

Figure 7. Connection to Motherboard



6. Connect the loose end of the probe or ribbon cables to the user target. Refer to Tables 2-4 for pin assignments.
7. With a 25-pin male-to-male parallel cable (not included), connect the LCE-K0S system to the host computer (Figure 8).

Figure 8. Connection to Host PC



8. With the power adapter connected, turn the switch to the ON position. The green LED turns on when power is supplied to the system.
9. Launch the debugger from your PC.

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