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Renesas Electronics Corporation

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User's Manual

LCE-780034-EM Emulation Board

Preliminary

1. GENERAL INFORMATION

The LCE-780034-EM emulation board, or daughterboard, for the LCE-K0 development system supports NEC's 8-bit μ PD780034 single-chip microcontrollers. By combining this daughterboard with the LCE-78K0 motherboard, you can efficiently emulate μ PD780034 subseries devices. The LCE-780034-EM is shipped with the following contents:

- Σ LCE-780034-EM daughterboard
- Σ User's manual
- Σ Two 50-pin ribbon cables
- Σ CD-ROM containing LCE debugger, device files, documentation, and evaluation copy of relocatable assembler and C compiler

1.1 System Configuration

The LCE-K0 system operates the ID78K0-LCE debugger on a host computer connected via a standard parallel cable from its LPT1 parallel port to the LCE-78K0 motherboard and LCE-780034-EM daughterboard. To connect the target system, use either a pair of 50-pin ribbon cables or an NEC probe and socket adapter.

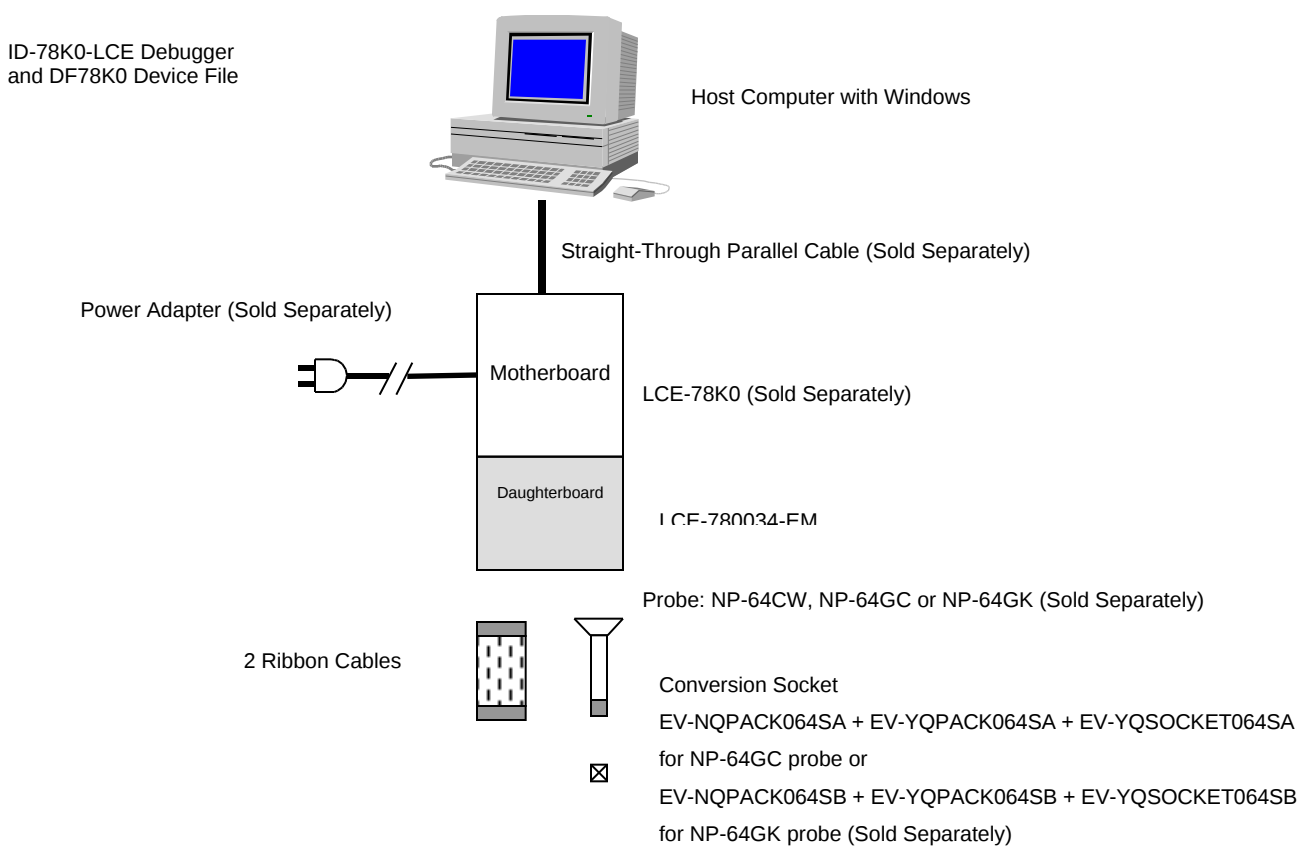


Table 1-1. Basic Configuration

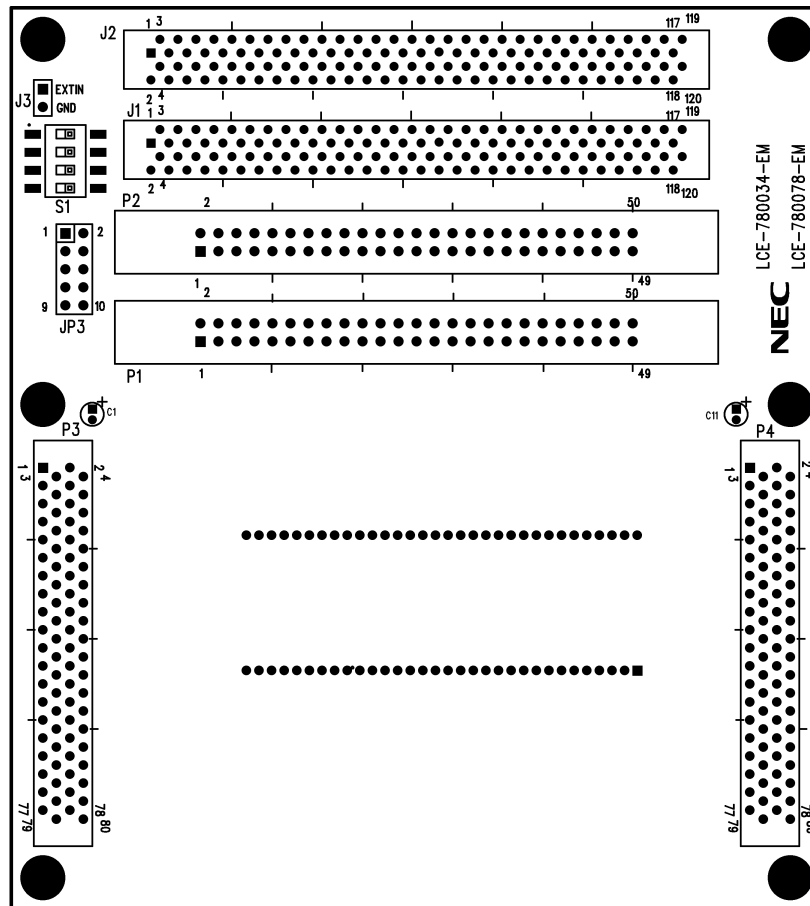
Parameter	Description
Target device	nPD780034 subseries: nPD780021A, nPD780022A, nPD780023A, nPD780024A, nPD780031A, nPD780032A, nPD780033A, nPD780034A, nPD78F0034A
Clock supply	Internal: installed on the motherboard
	External: pulse input
Low-voltage compatible	At least 2V

2. COMPONENTS

This section introduces the main components of the LCE-780034-EM daughterboard unit.

2.1 Daughterboard Layout

Figure 2-1. Top View

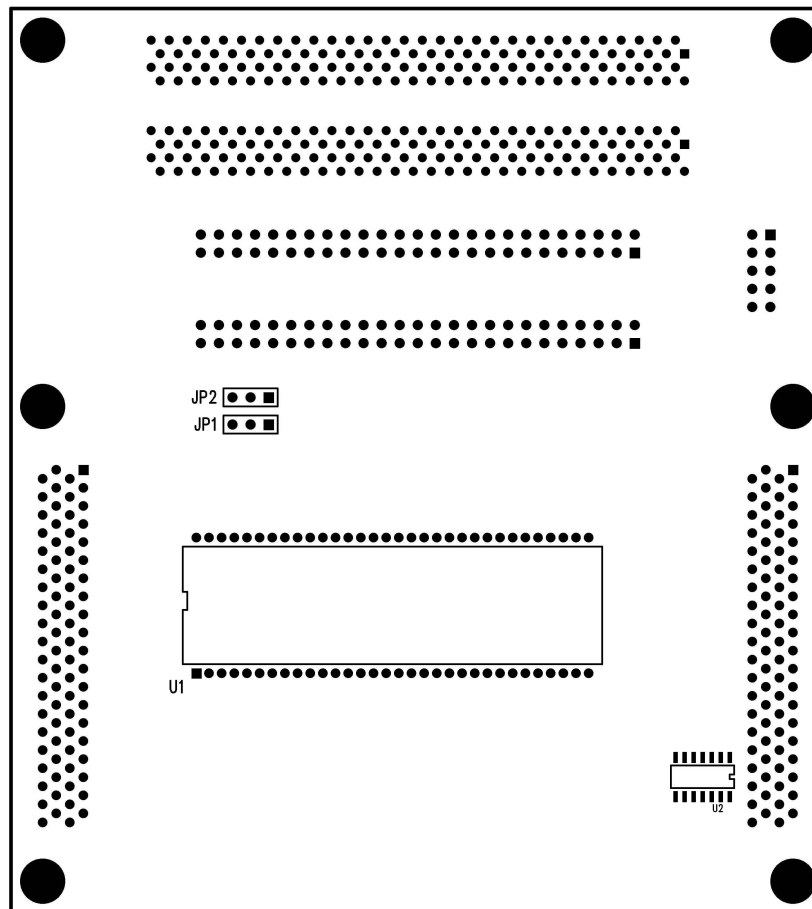


This side of the emulation board faces upward in the assembled system. Since the same printed circuit board is used for both the LCE-780034-EM and the LCE-780078-EM, the board name is labeled in the upper right corner.

J1, J2, P1 and P2 are connectors to the user target system. These connectors contain all the pins available on the emulated device. J1 and J2 are KEL connectors for device probes, while P1 and P2 are dual-row, male-shrouded headers with latching levers for the ribbon cables. Refer to Sections 2.2 and 2.3 for information about ribbon cables and probes, and to the Appendix for pin assignments of these connectors.

- Σ S1 is a dip switch for enabling or disabling pull-up resistors on the P30-P33 input pins to emulate mask options of the target device.
- Σ JP3 allows connection of analog input voltages of the Realchip to the available on-board chip voltages.
- Σ J3 is a connector for an external trigger input to the LCE-K0 system.
- Σ P3 and P4 are the connectors for the motherboard. The motherboard connects on top of the daughterboard.

Figure 2-2. Bottom View



The U1 device is the Realchip, which provides all the peripherals unique to the mPD780034 subseries microcontrollers.

Jumpers JP1 and JP2 are factory-set for configuration of the daughterboard with either a nPD78F0034ACW Realchip (for the LCE-780034-EM) or a nPD78F0078ACW Realchip (for the LCE-780078-EM). These jumper settings should not be changed.

Table 1. Jumper Settings

Board Type	Realchip Used	JP1 Setting	JP2 Setting
LCE-780034-EM	nPD78F0034ACW	JP1-1 to JP1-2	JP2-1 to JP2-2
LCE-780078-EM	nPD78F0078CW	JP1-2 to JP1-3	JP2-2 to JP2-3

2.2 Ribbon Cables

The ribbon cables are two 50-pin, female-to-female cables that connect the LCE-K0 system to the user target. One end of the ribbon cable connects to the dual-row, male-shrouded headers with latching levers on the daughterboard (P1 and P2), and the other connects to matching connectors on the user target.

Since all devices in the nPD780034 subseries are 64-pin devices, two ribbon cables are necessary to carry all signals of the target device. These ribbon cables are included with the daughterboard. The side of the ribbon cable that has a red stripe is pin 1. Please refer to the Appendix for the pin assignments of the P1 and P2 connectors.

2.3 Optional Emulation Probe

An emulation probe is optional. This is another method of connecting to the user target, provided a conversion socket/adaptor is installed on the target. Select the probe best suited for your target device package.

For target devices in the 64-pin plastic QFP package (GC suffix) or 64-pin plastic LQFP package (GK suffix), an appropriate probe and socket adapter to accept the probe should be used. These are the NP-64GC-TQ and NP-64GK probes. For connection of these probes to the LCE-780034-EM, connector J1 should be used.

For target devices in the 64-pin shrink DIP package (CW suffix), the NP-64CW probe should be used. No socket adapter is required for this probe, only an appropriate 64-pin SDIP socket on the target. For connection of this probe to the LCE-780034-EM, connector J2 should be used.

Table 2. Emulation Probe and Socket

Target Device	Emulation Probe	Conversion Socket/Adapter
mPD780021AGC mPD780022AGC mPD780023AGC mPD780024AGC mPD780031AGC mPD780032AGC mPD780033AGC mPD780034AGC mPD78F0034AGC	NP-64GC-TQ (connected to J1)	EV-NQPACK064SA + EV-YQPACK064SA + EV-YQSOCKET064SA
mPD780021AGK mPD780022AGK mPD780023AGK mPD780024AGK mPD780031AGK mPD780032AGK mPD780033AGK mPD780034AGK mPD78F0034AGK	NP-64GK (connected to J1)	EV-NQPACK064SB + EV-YQPACK064SB + EV-YQSOCKET064SB
mPD780021ACW mPD780022ACW mPD780023ACW mPD780024ACW mPD780031ACW mPD780032ACW mPD780033ACW mPD780034ACW mPD78F0034ACW	NP-64CW (connected to J2)	None required

Note: Refer to the Appendix for pin assignments.

2.4 S1 Settings for P30-P33 Mask Options

The target devices emulated by the LCE-780034-EM board have factory-programmable mask options, allowing pull-up resistors to be attached to the lower four bits of Port 3, P30 through P33. These ports are open-drain N-channel I/O ports, and can be configured as open-drain outputs by omitting the pull-up resistor mask option.

The factory-programmable mask options can be emulated by setting the appropriate bits of the S1 switch to connect or disconnect on-board pull-up resistors to P30- P33. These switches should be set for the mask options desired in the final target chip.

Table 3. S1 Settings for P30-P33 Mask Options

Port Bit	S1 Switch	Switch Setting	Port Setting
P30	S1-1	Off	P30 has no pull-up
		On	P30 has 33K pull-up to V _{DD}
P31	S1-2	Off	P31 has no pull-up
		On	P31 has 33K pull-up to V _{DD}
P32	S1-3	Off	P32 has no pull-up
		On	P32 has 33K pull-up to V _{DD}
P33	S1-4	Off	P33 has no pull-up
		On	P33 has 33K pull-up to V _{DD}

2.5 JP3 Settings for Analog Voltage Inputs

The target devices emulated by the LCE-780034-EM have analog voltage inputs to A/D converters, ANI₀ to ANI₇. These analog inputs require separate power (AV_{DD}), ground (AV_{SS}), and reference voltage (AV_{REF}) inputs.

Normally these analog voltage inputs are connected in the target system, with AV_{SS} connected to V_{SS} and AV_{DD} connected to V_{DD}, and with AV_{REF} connected to a voltage reference, which may also be V_{DD}.

JP3 allows for jumpering of these analog voltage inputs to V_{DD} or V_{SS} to provide these voltages when not connected in the target, or if no target is connected.

Table 4. JP3 Settings for Analog Voltage Inputs

Analog Voltage Input	Connected to	JP3 Setting
AV _{DD}	V _{DD}	JP3- 1 to JP3- 2, JP3- 4 open
	V _{SS}	JP3- 3 to JP3- 4, JP3- 2 open
	Not connected *	JP3- 2 and JP3- 4 open
AV _{REF}	V _{DD}	JP3- 5 to JP3- 6, JP3- 8 open
	V _{SS}	JP3- 7 to JP3- 8, JP3- 6 open
	Not connected *	JP3- 6 and JP3- 8 open
AV _{SS}	V _{SS}	JP3- 9 to JP3- 10
	Not connected *	JP3- 10 open

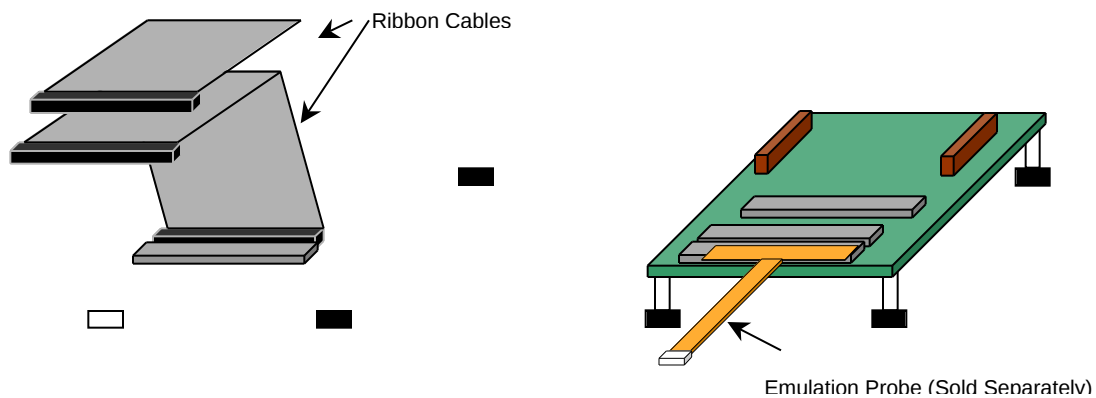
* Factory setting

Caution: To avoid shorting V_{DD} to V_{SS}, make sure only one of the possible jumper settings for AV_{DD} and AV_{REF} is selected.

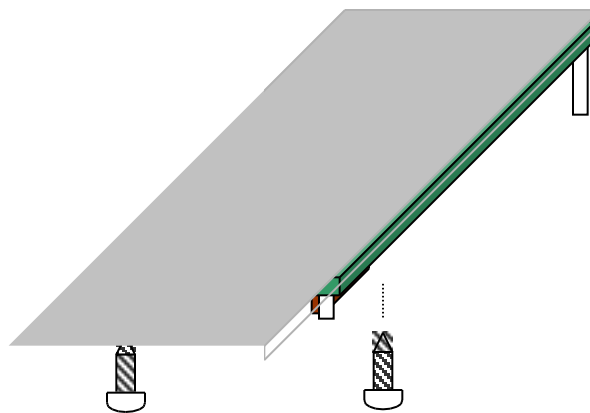
3. INSTALLATION

This chapter explains how to install and operate the LCE-K0 system.

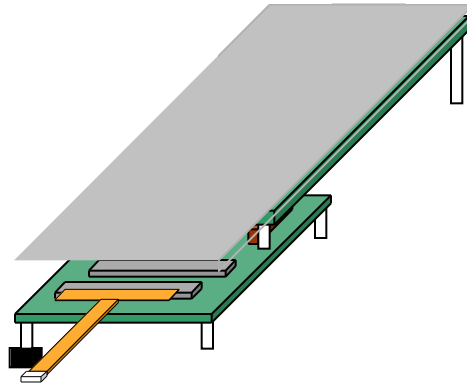
1. Connect the probe or ribbon cables to the respective connectors on the LCE-780034-EM.



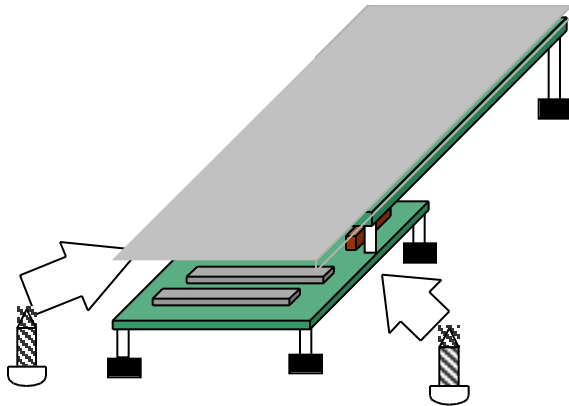
2. Turn off the power from the LCE-78K0 motherboard.
3. Remove the AC power adapter from the J1 power input on the motherboard.
4. Remove the two screws at the bottom of the stand-offs on the motherboard as shown.



5. With the daughterboard on a stable surface, connect the motherboard to the daughterboard by gently applying pressure on the mating connectors. Avoid applying pressure on the plastic cover.

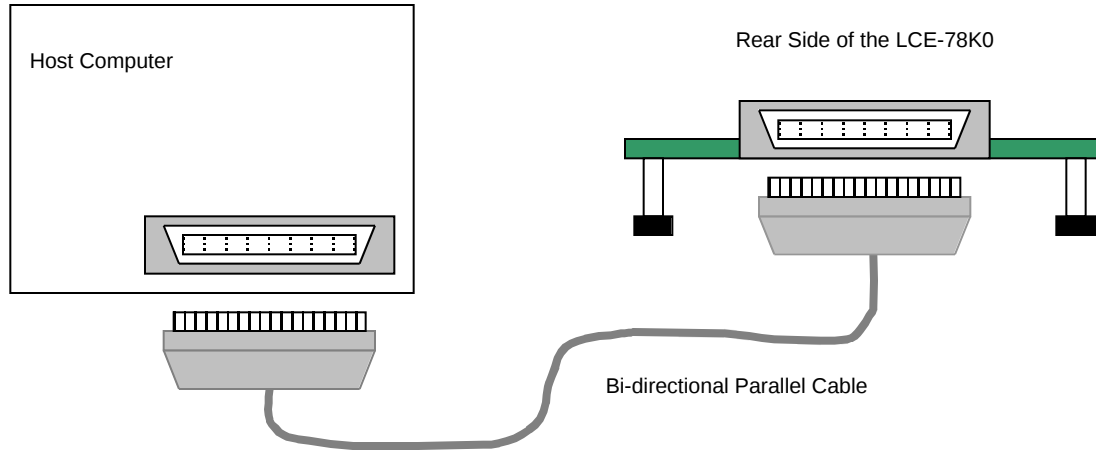


6. Tighten the screws back at the bottom of the daughterboard for a secure connection with the motherboards.



7. Make sure that power for the user target is off.
8. Connect the other end of the probe or ribbon cable to the user target.
9. Refer to Appendix A for pin assignments for both connectors.
10. Reconnect the AC power adapter to the LCE-78K0.

11. Connect the LCE-K0 system to the host computer with a 25-pin male-to-male parallel cable included with the motherboard.



12. Set the power switch on the LCE-78K0 motherboard to the ON position. The green LED should turn on indicating power is being supplied to the system.
13. Turn on power to the user target system.
14. Run the ID78K0-LCE debugger on the host computer.

When turning off power and disconnecting, follow the reverse sequence.

1. Turn power off to the user target system.
2. Turn the power switch on the LCE-78K0 motherboard off.
3. Disconnect the LCE-K0 system from the host computer.
4. Disconnect the AC adapter from the LCE-K0 system.
5. Disconnect the LCE-K0 system from the user target.

APPENDIX. CONNECTOR PIN ASSIGNMENTS

Table 5. Ribbon Cable Pin Assignments

P1 Pin	Target Pin Number	Target Signal	P2 Pin	Target Pin Number	Target Signal
1–10		(GND) ^(Note 3)	1–10		(GND) ^(Note 3)
11	1	P50	11	31	P12
12	2	P51	12	32	P11
13	3	P52	13	33	P10
14	4	P53	14	34	AVREF
15	5	P54	15	35	AVDD
16	6	P55	16	36	RESET_B
17	7	P56	17	37	XT2 ^(Note 2)
18	8	P57	18	38	XT1
19	9	VSS0 ^(Note 1)	19	39	VPP_TEST ^(Note 2)
20	10	VDD0 ^(Note 4)	20	40	X2 (Note 2)
21	11	P30	21	41	X1
22	12	P31	22	42	VSS1 ^(Note 2)
23	13	P32	23	43	P00
24	14	P33	24	44	P01
25	15	P34	25	45	P02
26	16	P35	26	46	P03
27	17	P36	27	47	P70
28	18	P20	28	48	P71
29	19	P21	29	49	P72
30	20	P22	30	50	P73
31	21	P23	31	51	P74
32	22	P24	32	52	P75
33	23	P25	33	53	P64
34	24	VDD1 ^(Note 4)	34	54	P65
35	25	AVSS	35	55	P66
36	26	P17	36	56	P67
37	27	P16	37	57	P40
38	28	P15	38	58	P41
39	29	P14	39	59	P42
40	30	P13	40	60	P43
41		(GND) ^(Note 3)	41	61	P44
42		(GND) ^(Note 3)	42	62	P45
43		(GND) ^(Note 3)	43	63	P46
44		(GND) ^(Note 3)	44	64	P47
45–50		(GND) ^(Note 3)	45–50		(GND) ^(Note 3)

1. VSS0 and VSS1 on the target pins are connected to GND on the LCE-780034-EM.
2. X2, XT2, and VPP/TEST on the target are not connected on the LCE-780034-EM.
3. P1 pins 1- 10 and 41- 50 and P2 pins 1- 10, 45-50 are connected to GND on the LCE-780034-EM.
4. VDD0 and VDD1 on the target are both connected to PB_VDD on the LCE-780034-EM; this signal is used for sensing target voltage, but it does not supply power to the target.

Table 6. NP-64GC-TQ/GK Pin Assignments (J1)

Target Pin Number	J1 Pin Number	Target Pin Number	J1 Pin Number
1	108	33	14
2	107	34	13
3	104	35	18
4	103	36	17
5	100	37	22
6	99	38	21
7	94	39	28
8	93	40	27
9	30	41	92
10	29	42	91
11	24	43	98
12	23	44	97
13	20	45	102
14	19	46	101
15	16	47	106
16	15	48	105
17	43	49	77
18	44	50	78
19	47	51	73
20	48	52	74
21	51	53	69
22	52	54	70
23	57	55	63
24	58	56	64
25	59	57	61
26	60	58	62
27	55	59	65
28	56	60	66
29	49	61	71
30	50	62	72
31	45	63	75
32	46	64	76

Table 7. NP-64CW Pin Assignments (J2)

Target Pin Number	J1 Pin Number	Target Pin Number	J1 Pin Number
1	29	33	91
2	24	34	98
3	23	35	97
4	20	36	102
5	19	37	101
6	16	38	106
7	15	39	105
8	43	40	77
9	44	41	78
10	47	42	73
11	48	43	74
12	51	44	69
13	52	45	70
14	57	46	63
15	58	47	64
16	59	48	61
17	60	49	62
18	55	50	65
19	56	51	66
20	49	52	71
21	50	53	72
22	45	54	75
23	46	55	76
24	14	56	108
25	13	57	107
26	18	58	104
27	17	59	103
28	22	60	100
29	21	61	99
30	28	62	94
31	27	63	93
32	92	64	30

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