ISL75055SLHEV1Z

Radiation Hardened 3A Source and Sink DDR Terminator/LDO Evaluation Board

Description

The ISL75055SLHEV1Z evaluation board features the ISL75055SLH 3A Source and Sink DDR Terminator/LDO. The board is designed for flexibility to evaluate the ISL75055SLH as a VTT termination rail in DDR memory applications using a buffered reference to set VDDQ/2 as the voltage reference, or as a standard LDO for general purpose applications using the internal 0.5V voltage reference. The board operates with a VIN power rail of 0.75V to 5.5V and a VCC bias supply of 2.7V to 5.5V. For standard LDO applications, the output voltage is jumper configurable between 0.5V to 4.2V. The ISL75055SLH features soft start, enable, output discharge, and OCP that can be adjusted by the user.

Features

- Configurable between DDR Mode, using buffered reference, and LDO Mode, using internal reference
- On-board load transient generator
- 3A Source/Sink capability
- Adjustable output voltage, soft start, output discharge, and overcurrent protection

Specifications

- Input supply (PVIN): 0.75V to 5.5V
- Bias supply (VCC): 2.7V to 5.5V
- DDR mode output voltage: DDR, DDR2, DDR3, and DDR4 VTT
- LDO mode output voltage: 0.5V to 4.2V (jumper selectable)
- Output current: 3A Sourcing or Sinking
- Number of board layers: 4
- PCB layer thickness: 2oz outer, 1oz inner

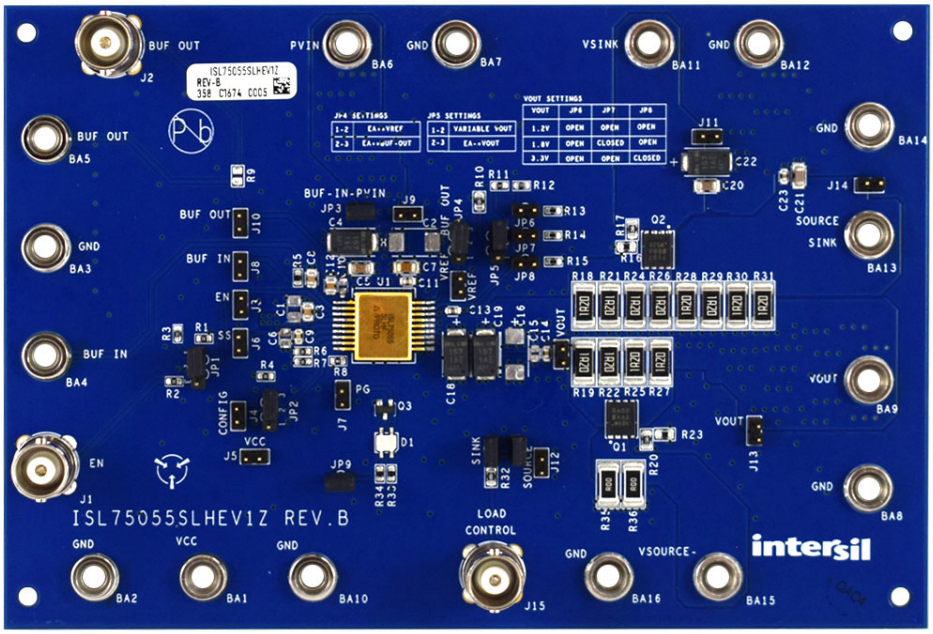

Figure 1. ISL75055SLHEV1Z Board

Contents

1. Functional Description . . . 3
1.1 Operational Characteristics . . . 3
1.2 Setup and Configuration . . . 3
1.2.1 DDR4 Application Configuration . . . 4
1.2.2 LDO Application Configuration . . . 4
1.2.3 Default Evaluation Board Configuration . . . 5
1.2.4 DDR Mode Description . . . 5
1.2.5 LDO Mode Description . . . 6
1.2.6 On-Board Load Transient Generator . . . 7
1.2.7 On-Board Static Load . . . 7
2. Board Design . . . 8
2.1 Schematic Diagrams . . . 8
2.2 Bill of Materials . . . 8
2.3 Board Layout . . . 10
3. Typical Performance Graphs . . . 11
4. Ordering Information . . . 16
5. Revision History . . . 16

1. Functional Description

The ISL75055SLHEV1Z evaluation board is designed to evaluate the ISL75055SLH 3A Source/Sink LDO as both a DDR VTT termination regulator and as a general purpose LDO. Configuration is handled by on-board jumpers to select either the internal buffer reference of BUF-IN/2 or the internal 0.5V voltage reference as the non-inverting input to the error amplifier. The board also features soft start, enable, output discharge, and OCP settings that can be adjusted by the user. An on-board load transient generator is provided to evaluate the sinking/sourcing transient performance.

1.1 Operational Characteristics

The ISL75055SLHEV1Z evaluation board requires a PVIN voltage source to supply VIN, the LDO input voltage of the IC. PVIN input voltage supports a range of 0.75V to 5.5V. A VCC voltage source for powering is also required for board operation. The VCC input supports a range of 2.7V to 5.5V and should be set to a minimum value of VOUT + 1.5V for proper output regulation.

- An optional voltage source can be placed on SOURCE/SINK to generate a static load across resistors R28 to R31.
- For sinking transient loads, a voltage source is required on VSINK.
- An optional voltage source can be placed on VSOURCE for the sourcing transient loads or the load can be terminated to GND by resistors R35 and R36.
- The EN pin can either be tied to VCC or an external enable signal through a BNC connector, J1.

1.2 Setup and Configuration

Figure 2 shows an overview of the evaluation board connections.

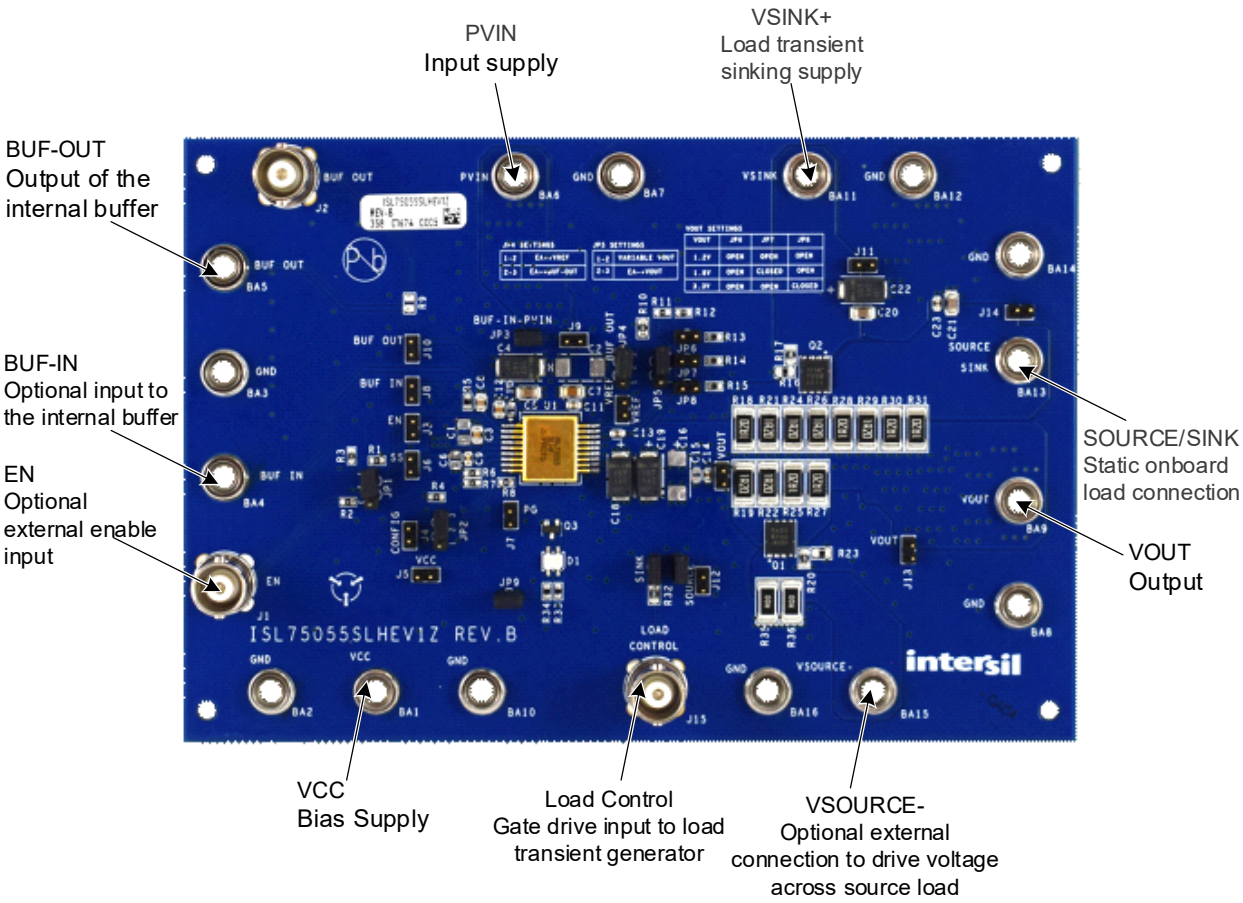

Figure 2. ISL75055SLHEV1Z Board Overview

1.2.1 DDR4 Application Configuration

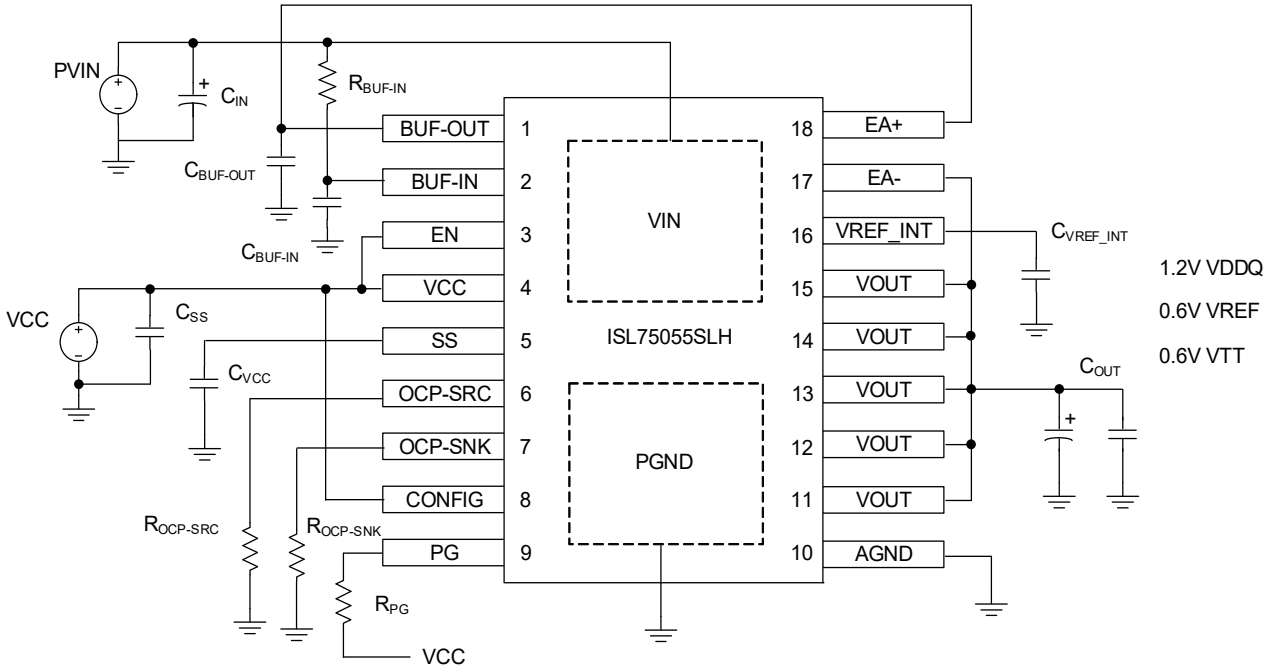

Figure 3. ISL75055SLH DDR4 Typical Application Circuit

1.2.2 LDO Application Configuration

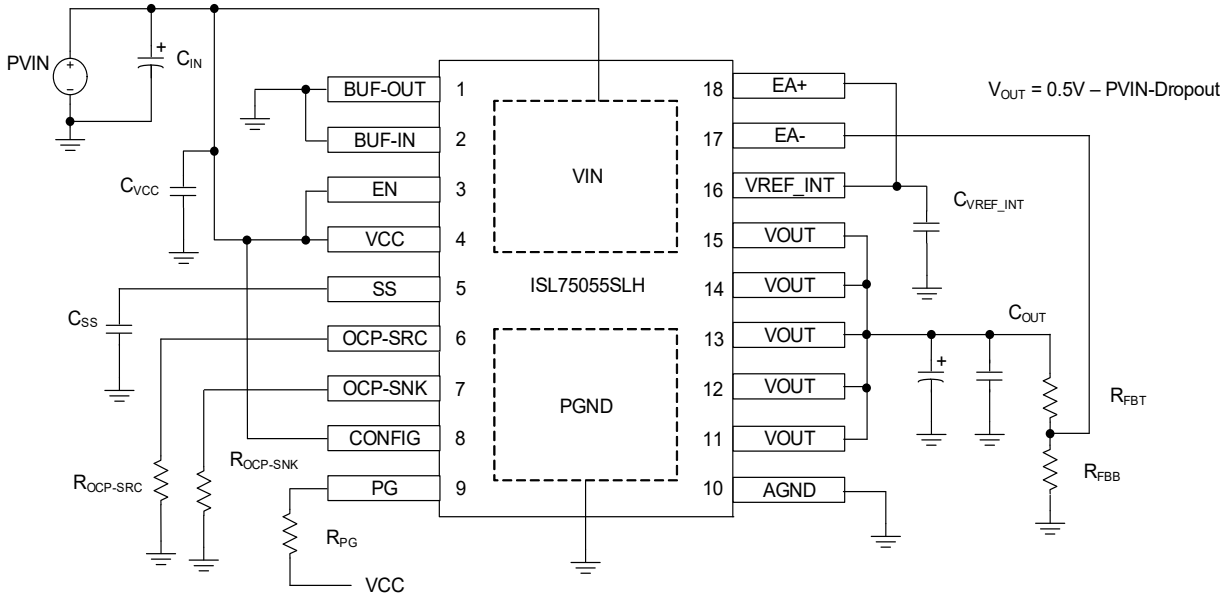

Figure 4. ISL75055SLH General LDO Typical Application Circuit

1.2.3 Default Evaluation Board Configuration

Table 1. Default Evaluation Board Jumper Configuration

Reference Designator	Description	Settings	Default Setting
JP1	Enable configuration jumper	1-2: EN = VCC 2-3: EN = External enable	1-2
JP2	V_{OUT} and BUF-OUT discharge configuration jumper	1-2: Output discharge disabled (CONFIG = GND) 2-3: Output discharge enabled (CONFIG = VCC)	2-3
JP3	Jumper between BUFIN and PVIN	OPEN: BUF-OUT = BUF-IN / 2 CLOSED: BUF-OUT = PVIN / 2	CLOSED
JP4	Error amplifier non-inverting input connection	1-2: Internal voltage reference for LDO Mode (EA+ = VREF_INT) 2-3: Buffered voltage reference for DDR Mode (EA+ = BUF-OUT)	2-3
JP5	Error amplifier inverting input connection	1-2: VOUT feedback divider (LDO Mode) 2-3: Direct connection to VOUT (DDR Mode)	2-3
JP6, JP7, JP8	Output voltage divider configuration	See Table 3 for setting the output voltage	OPEN
JP9	PG LED indicator enable/disable	OPEN: LED indicator disabled CLOSED: LED indicator enabled	CLOSED
SOURCE	Source transient enable	OPEN: Source transient disabled CLOSED: Source transient enabled (with driving source)	OPEN
SINK	Sink transient enable	OPEN: Sink transient disabled CLOSED: Sink transient enabled (with driving source)	OPEN

1.2.4 DDR Mode Description

In DDR systems, the VDDQ source must be supplied as an input to BUF-IN. The on-chip internal reference buffer generates a voltage equal to ½ VDDQ, which is used as the voltage reference, VREF. The device regulates VTT voltage on VOUT at the VREF voltage.

1. Evaluate DDR mode by first populating the jumpers to meet the required testing configuration. Refer to Table 1 and Table 3 for more details on jumper connections.
   a. JP3 – Populate to tie VIN to the input of the internal buffer, BUF-IN.
   b. JP4 – Must be set to position 2-3 to tie EA+ to the output of the internal buffer, BUF-OUT.
   c. JP5 – Must be set to position 2-3 to tie EA- directly to VOUT.
2. Apply power supplies to PVIN and VCC.
3. If EN is driven externally, set high to enable the device.
4. The output voltage should now be regulating at the target voltage, and the LED should turn to green.
5. A static load can be applied through an electronic or resistive load connected between the VOUT terminal BA9 and the GND terminal BA10.
   a. Alternatively, a voltage can be applied to the SOURCE/SINK terminal BA13 to use resistors R28 to R31 as a static load. This is described in more detail in On-Board Static Load.
   Note: Each 2512 resistor is rated for 2W.
6. A transient load can be applied by following the instructions in On-Board Load Transient Generator.

The *ISL75055SLH Datasheet* (see ISL75055SLH) recommends using an RC filter between VOUT and EA-. This filter optimizes loop response for the maximum phase margin, but is not required for LDO evaluation. To evaluate loop response with this RC filter, replace R11 with a 4.99kΩ resistor and depopulate R12. No jumper should be placed on JP5, and R10 is used as the signal injection resistor.

Table 2. DDR Jumper Connections

JP3	JP4	JP5	BUF-IN
OPEN	2-3	2-3	Externally supplied
CLOSED	2-3	2-3	Tied to PVIN

1.2.5 LDO Mode Description

The ISL75055SLH features an internal voltage reference that is connected to the error amplifier non-inverting input when the device is used in general purpose LDO application. Refer to Table 2 and Table 3 for more details about jumper connections output voltage.

1. Evaluate LDO Mode by first populating the jumpers to meet the required testing configuration. Refer to Table 2 and Table 3 for more details on jumper connections.
   a. JP3 – Remove to disconnect VIN from BUF-IN, as the buffered reference is not required in standard LDO applications.
   b. JP4 – Must be set to position 1-2 to tie EA+ to the 0.5V internal voltage reference, VREF_INT.
   c. JP5 – Set to position 1-2 to tie EA- to the scaled down output voltage set by the feedback divider resistors R11 - R15.
   d. JP6 to JP8 – Set according to the desired output voltage as outlined in Table 3.
2. Continue with board power up and evaluation as described in DDR Mode Description steps 2 - 6.

The *ISL75055SLH Datasheet* recommends using a single 330µF Tantalum Polymer capacitor for LDO mode configurations. This capacitance/ESR is the optimal combination tests for maximum phase margin, but is not required for LDO evaluation.

Table 3. LDO Jumper Connections

JP5	JP6	JP7	JP8	VOUT
2-3	N/A	N/A	N/A	0.5V
1-2	OPEN	OPEN	OPEN	1.2V
1-2	CLOSED	OPEN	OPEN	1.5V
1-2	OPEN	CLOSED	OPEN	1.8V
1-2	OPEN	OPEN	CLOSED	3.3V
1-2	CLOSED	CLOSED	OPEN	2.1V
1-2	CLOSED	OPEN	CLOSED	3.6V
1-2	OPEN	CLOSED	CLOSED	3.9V
1-2	CLOSED	CLOSED	CLOSED	4.2V

1.2.6 On-Board Load Transient Generator

The ISL75055SLHEV1Z includes an on-board transient load generator that accepts a single gate drive signal to control the NFET for sourcing load and PFET for sinking load.
Note: The load resistor values may require adjustment depending on target output voltage and current.

The following is the load transient test procedure:

1. Populate SOURCE and SINK jumpers to enable the load transient functionality.
2. Apply a voltage to VSINK+ terminal BA11 to generate the sinking load. This voltage is determined by calculating the current generated by the voltage drop from VSINK+ to VOUT across resistors R18, R21, R24, and R26.
3. The sourcing current is determined by the drop from VOUT to GND across R19, R22, R25, and R27.
4. Alternatively, R35 and R36 can be depopulated to drive the VSOURCE- voltage from an external power supply. Common lab power supplies can only source current and cannot sink current from an ISL75055SLH that is sourcing the current. However, with floating lab supplies, by reversing the polarity to provide negative voltage on VSOURCE-, the power supply is sinking through the reverse polarity the current that is sourced from the ISL75055SLH. When R35 and R36 are depopulated, the external voltage supply negative terminal should connect to VSOURCE- and positive terminal should connect to GND on the evaluation board. The sourcing current is determined by the drop from VOUT to VSOURCE- across R19, R22, R25, and R27.
5. Apply a ±5V square wave to BNC connector J15 (VOUT LOAD CONTROL) using a function generator to drive FETs Q1 and Q2 creating a sourcing/sinking load transient.

   Note: That the PMOS FET (Q2) Source is at the VSINK+ voltage and requires sufficient V_{SG} drive to turn it on/off. Conversely, the NMOS FET (Q1) Source is at GND (or VSOURCE-) and requires sufficient V_{GS} drive to turn it on/off.
6. The transient response can be measured with an oscilloscope on the VOUT header, or through the tip and barrel method across one of the output caps.

1.2.7 On-Board Static Load

Resistors R28 to R31 can be used as an on-board load by connecting an external supply to the SOURCE/SINK terminal. Use Equation 1 to calculate the load current.

- The device operates as a sourcing supply when SOURCE/SINK < V_{OUT}
- The device operates as a sinking supply when SOURCE/SINK > V_{OUT}

(EQ. 1) $$I_{LOAD} = \frac{V_{OUT} - V_{SOURCE/SINK}}{R_{LOAD}}$$

- Where R_{LOAD} is the equivalent resistance of R28-R31.

Note: Each 2512 resistor is rated for 2W.

2. Board Design

2.1 Schematic Diagrams

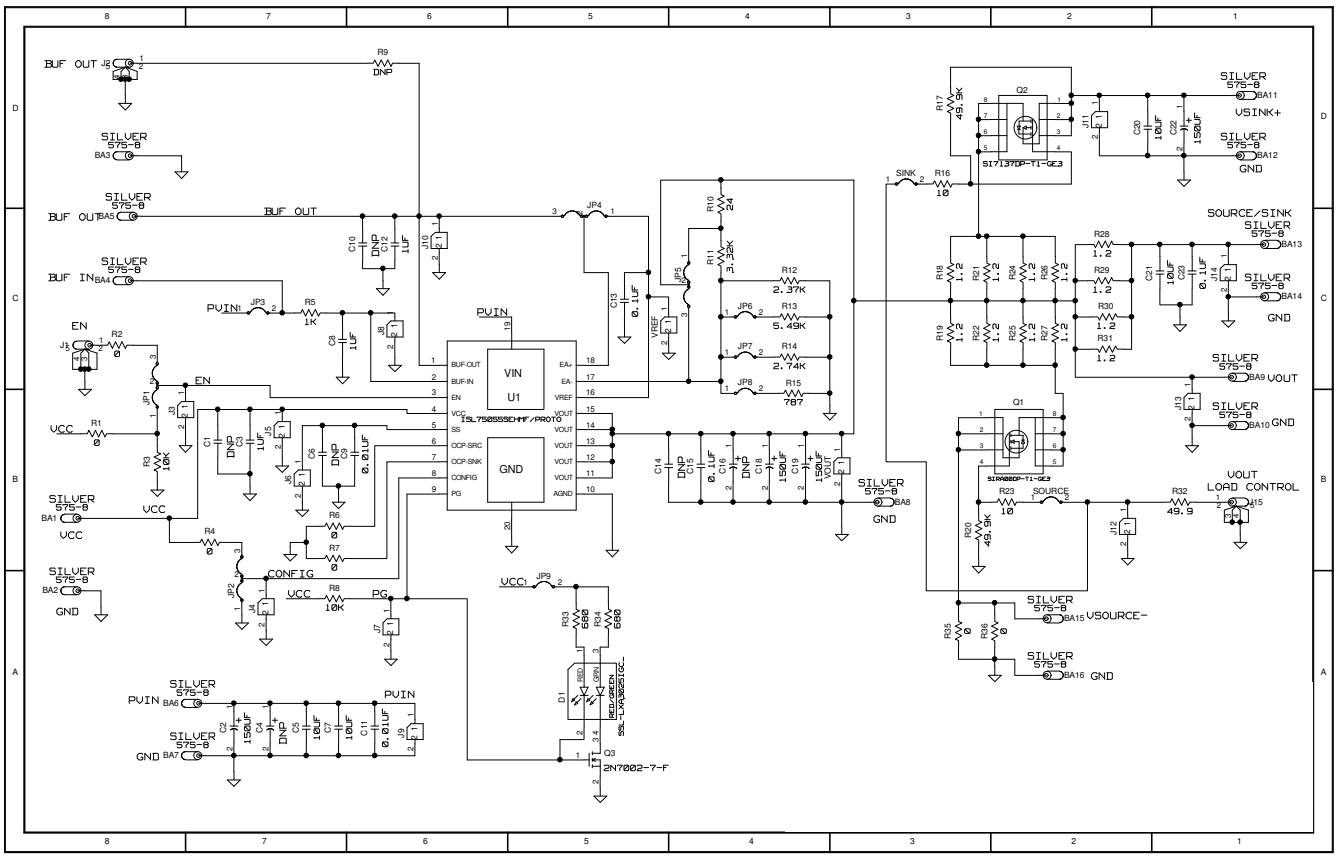

Figure 5. ISL75055SLHEV1Z Schematic

2.2 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	Q3	MOSFET N-CH 60V 115MA SOT23-3	Diodes Incorporated	2N7002-7-F
3	J1, J2, J15	CONN BNC RCPT STR 50Ω PCB	Amphenol	31-5329-51RFX
16	BA1, BA2, BA3, BA4, BA5, BA6, BA7, BA8, BA9, BA10, BA11, BA12, BA13, BA14, BA15, BA16	CONN Banana Jack Solder	Keystone	575-8
14	J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, VOUT, VREF	CONN HEADER VERT 2POS 2.54MM	FCI	69190-202HLF
2	R33, R34	RES SMD 680Ω 1% 1/8W 0603	Vishay	CRCW0603680RFKEA
1	R14	RES SMD 2.74kΩ 0.1% 1/10W 0603	Panasonic	ERA-3AEB2741V
1	R13	RES SMD 5.49kΩ 0.1% 1/10W 0603	Panasonic	ERA-3AEB5491V
1	R15	RES SMD 787Ω 0.1% 1/10W 0603	Panasonic	ERA-3AEB7870V
2	R16, R23	RES SMD 10Ω 1% 1/2W 0805	Panasonic	ERJ-P6WF10R0V
2	C9, C11	CAP CER 10000PF 16V X7R 0603	Yageo	CC0603KRX7R7BB103

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part Number
3	C13, C15, C23	CAP CER 0.1µF 16V X7R 0603	Yageo	CC0603KRX7R7BB104
3	C3, C8, C12	CAP CER 1µF 25V X7R 0805	Samsung Electro-mechanics	CL21B105KAFNNNE
4	C5, C7, C20, C21	CAP CER 10µF 16V X7R 1206	Samsung Electro-mechanics	CL31B106MOHNNNE
5	R1, R2, R4, R6, R7	RES 0Ω JUMPER 1/10W 0603	Yageo	RC0603JR-070RL
2	R3, R8	RES 10kΩ 5% 1/10W 0603	Stackpole Electronics Inc	RMCF0603JT10K0
1	R11	RES 3.32kΩ 1% 1/10W 0603	Stackpole Electronics Inc	RMCF0603FT3K32
1	R10	RES 24Ω 1% 1/8W 0805	Stackpole Electronics Inc	RMCF0805FT24R0
2	R17, R20	RES 49.9kΩ 1% 1/8W 0805	YAGEO	RC0805FR-0749K9L
1	R32	RES 49.9Ω 1% 1/8W 0805	YAGEO	RC0805FR-0749R9L
1	U1	5V 3A Source and Sink LDO Regulator (Non-Standard Footprint)	Renesas	ISL75055SLHMF/PROTO
4	JP1, JP2, JP4, JP5	CONN HEADER VERT 3POS 2.54MM	Harwin Inc.	M20-9990345
7	JP3, JP6, JP7, JP8, JP9, SINK, SOURCE	CONN HEADER VERT 2POS 2.54MM	Amphenol ICC (FCI)	69190-202HLF
1	R5	RES SMD 1kΩ 1% 1/8W 0603	Rohm	CRCW06031K00FKEA
12	R18, R19, R21, R22, R24, R25, R26, R27, R28, R29, R30, R31	RES 1.2Ω 1% 2W 2512	Stackpole	RC2512FK-7W1R2L
2	R35, R36	RES 0Ω JUMPER 1W 2512	Stackpole	RMCF2512ZT0R00
1	R12	RES SMD 2.37kΩ 0.1% 1/10W 0603	Yageo	RT0603BRD072K37L
1	Q2	MOSFET P-CH 20V 60A PPAK SO-8	Vishay	SI7137DP-T1-GE3
1	Q1	MOSFET N-CH 30V 100A PPAK SO-8	Vishay	SIRA00DP-T1-GE3
1	D1	3x2.5mm Surface Mount RED/GREEN LED	LUMEX	SSL-LXA3025IGC_
4	C2, C18, C19, C22	CAP TANT POLY 150µF 16V 2917	KEMET	T530X157M016ATE015
DNP	C1	CAP CER 10µF 16V X7R 1206	Samsung Electro-Mechanics	CL31B106MOHNNNE
DNP	C4, C16	CAP TANT POLY 150µF 16V 2917	Kemet	T530X157M016ATE015
DNP	C6	CAP CER 1µF 25V X7R 0805	Samsung Electro-mechanics	CL21B105KAFNNNE
DNP	C10, C14	CAP CER 0.1µF 16V X7R 0603	Yageo	CC0603KRX7R7BB104
DNP	R9	Thick Film Chip Resistor	-	H2506-DNP-DNP-1

2.3 Board Layout

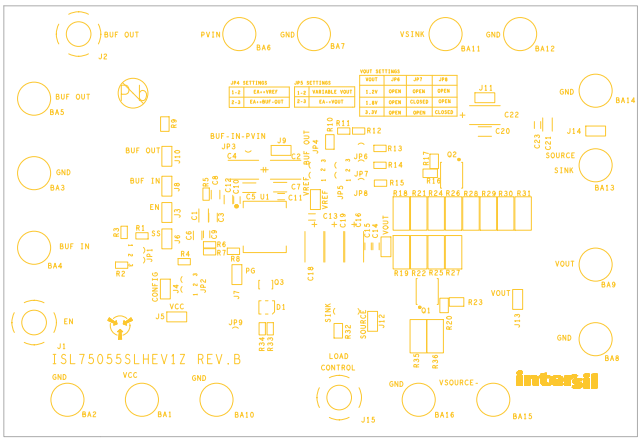

Figure 6. Silkscreen Top

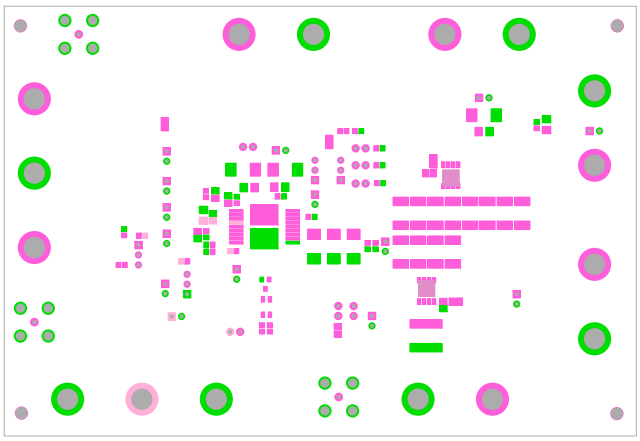

Figure 7. Solder Mask Top

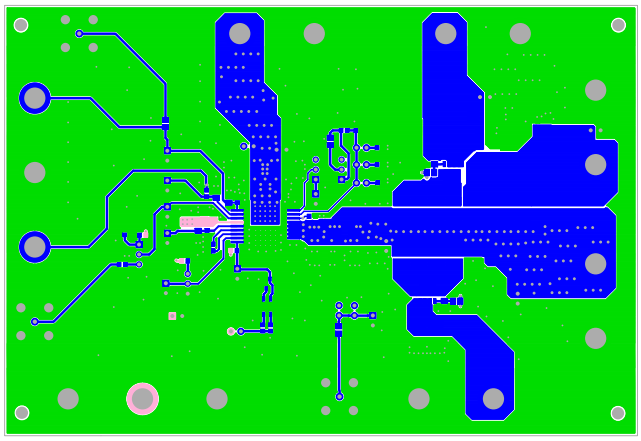

Figure 8. Top Layer

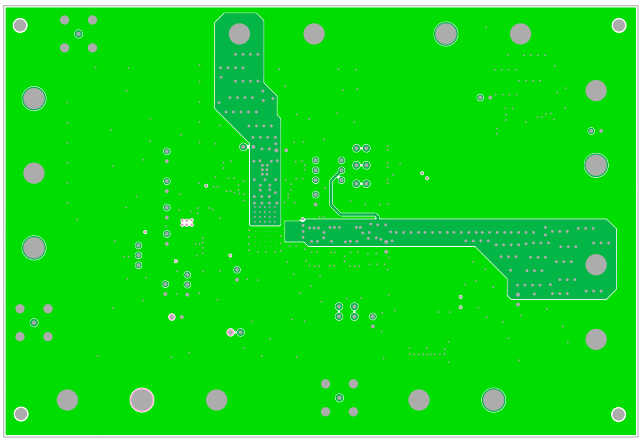

Figure 9. Layer 2

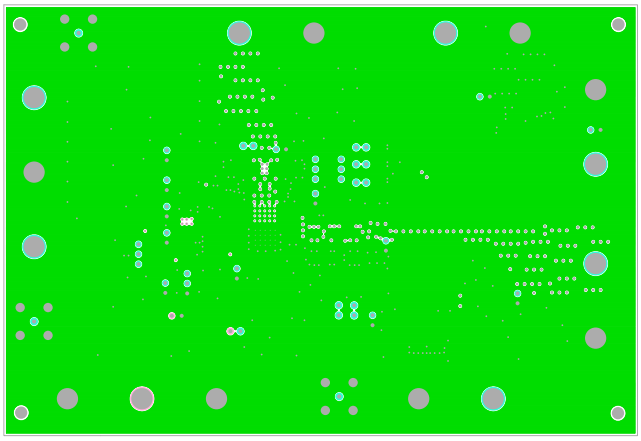

Figure 10. Layer 3

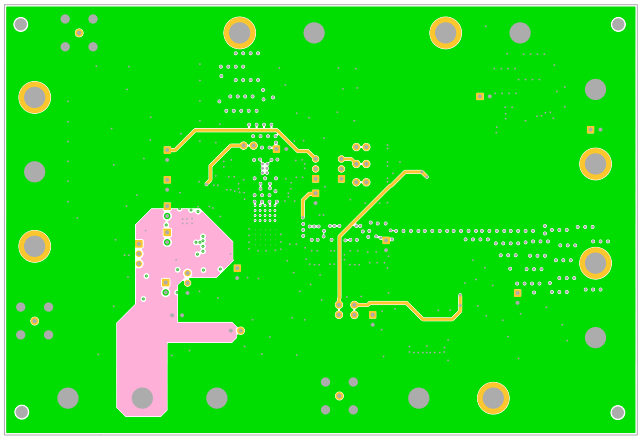

Figure 11. Bottom Layer

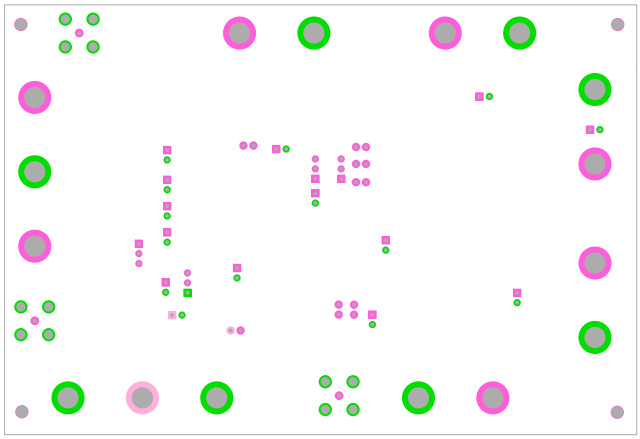

Figure 12. Solder Mask Bottom

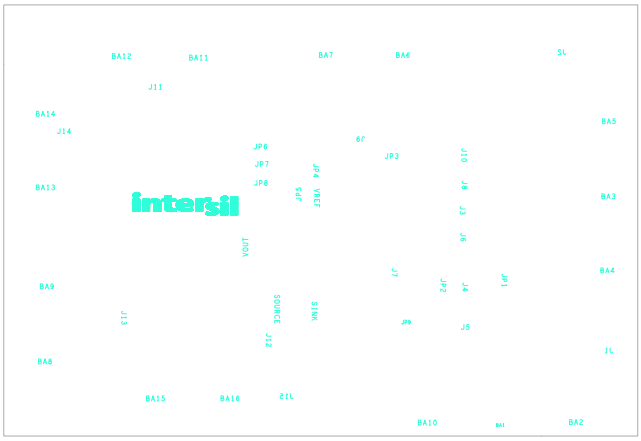

Figure 13. Silkscreen Bottom

3. Typical Performance Graphs

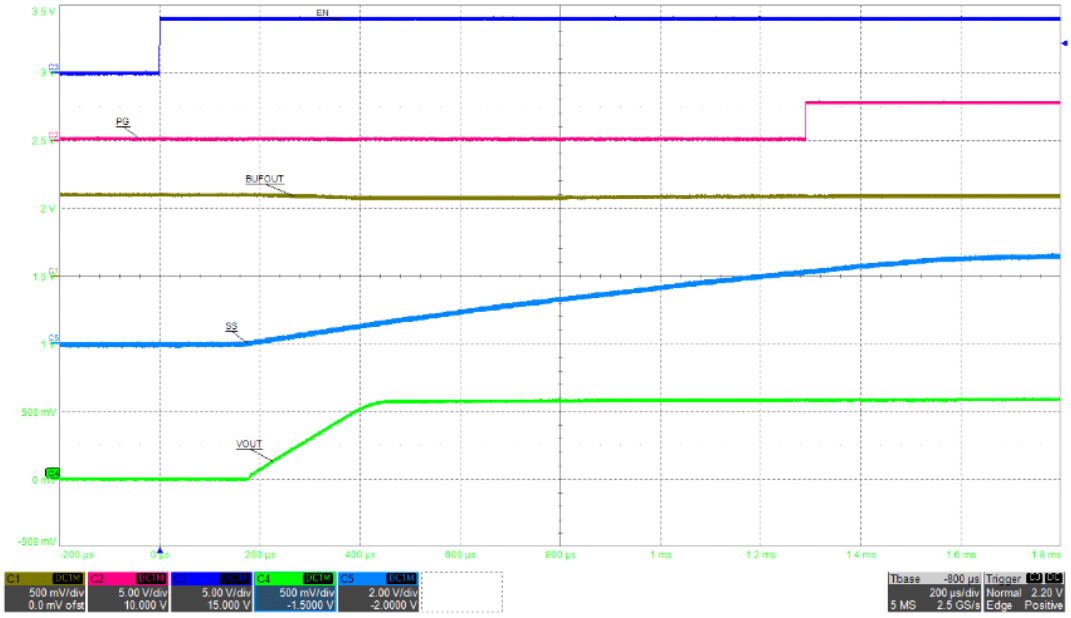

Figure 14. Startup with Soft-Start; DDR Mode
(V_{IN} = BUF - IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF - OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

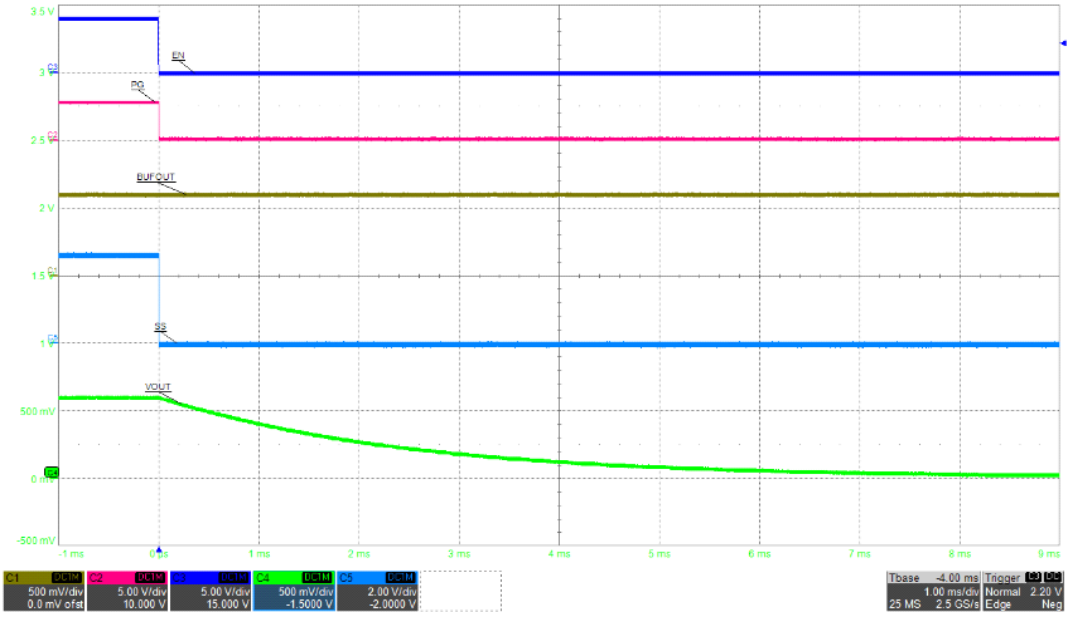

Figure 15. Shutdown; DDR Mode, Config High
(V_{IN} = BUF - IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF - OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

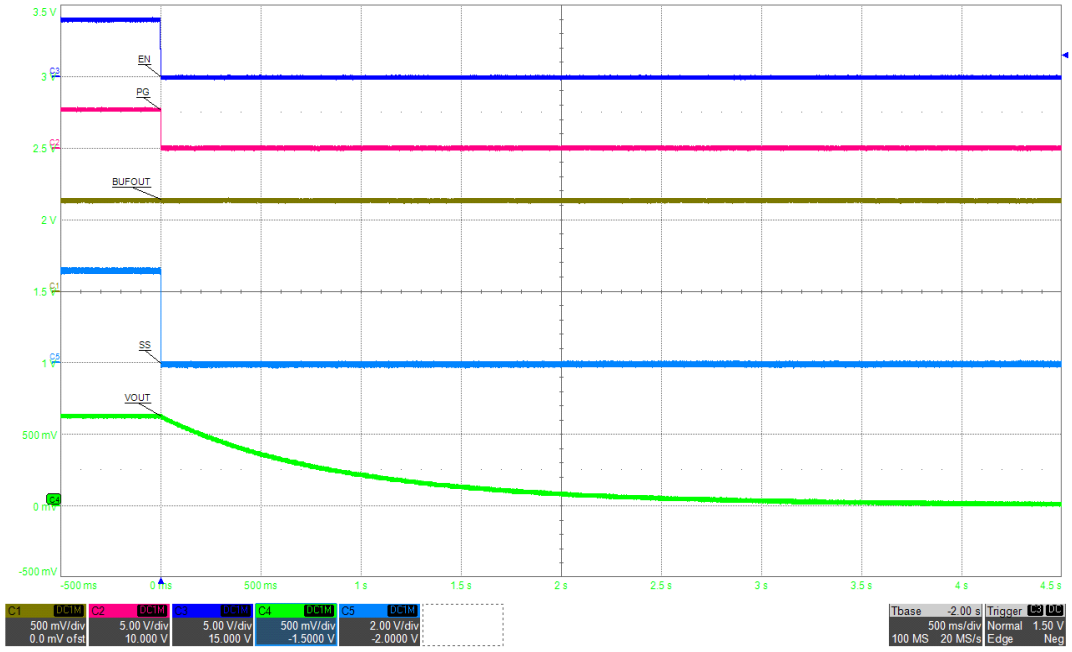

Figure 16. Shutdown; DDR Mode, Config Low
(V_{IN} = BUF - IN = 1.2V, V_{CC} = 2.7V, EA+ = BUF - OUT, V_{OUT} = 0.6V, I_{OUT} = 0A)

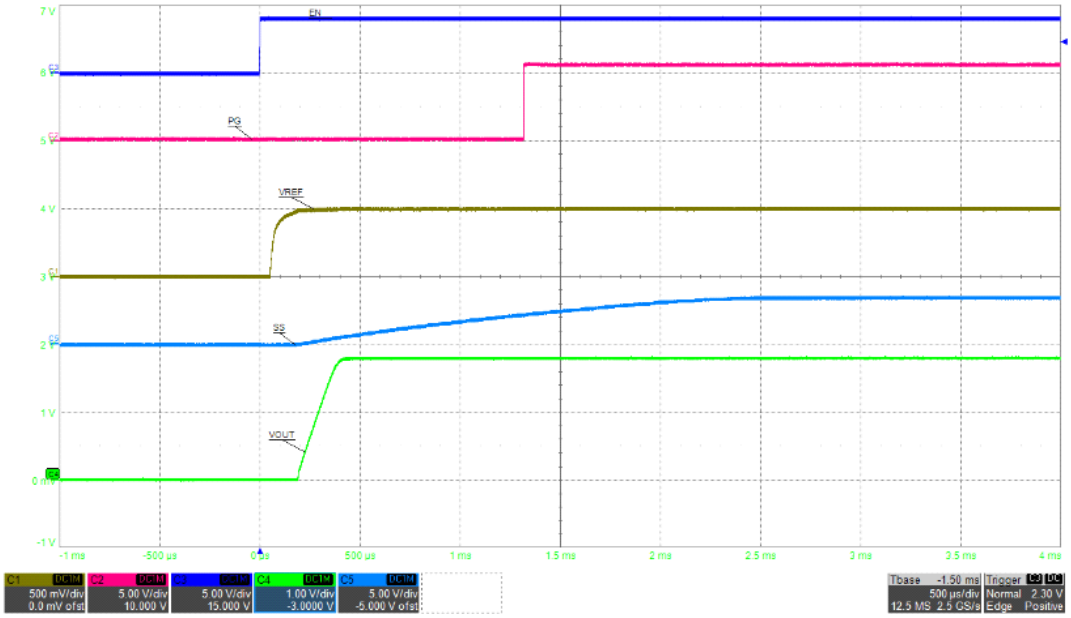

Figure 17. Startup with Soft-Start; LDO Mode
(V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = V_{REF_INT}, V_{OUT} = 1.8V, I_{OUT} = 0A)

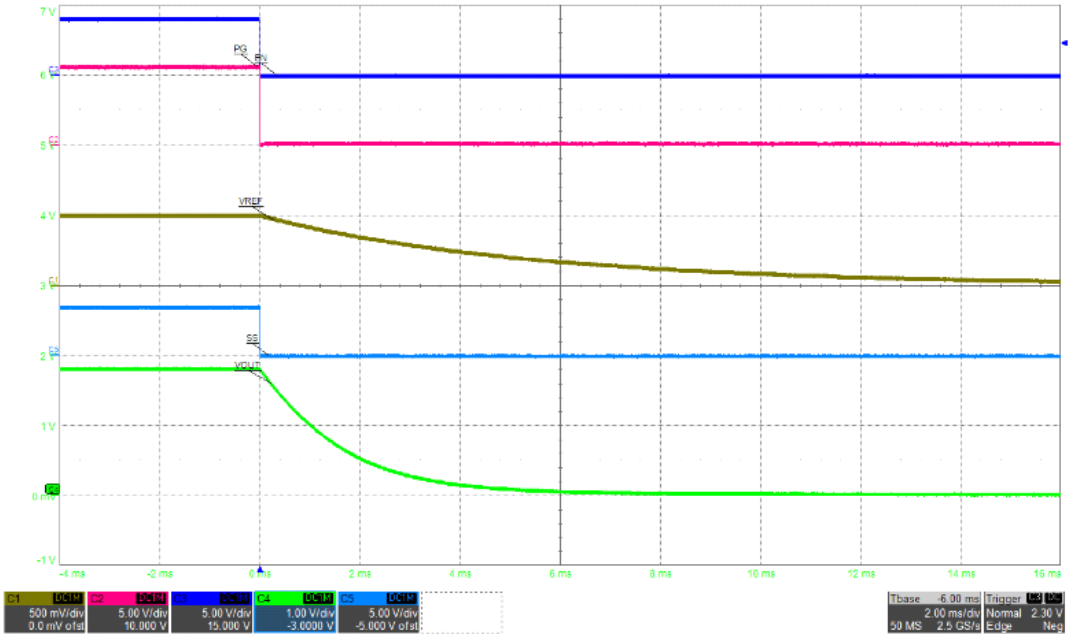

Figure 18. Shutdown; LDO Mode, Config High
(V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = V_{REF_INT}, V_{OUT} = 1.8V, I_{OUT} = 0A)

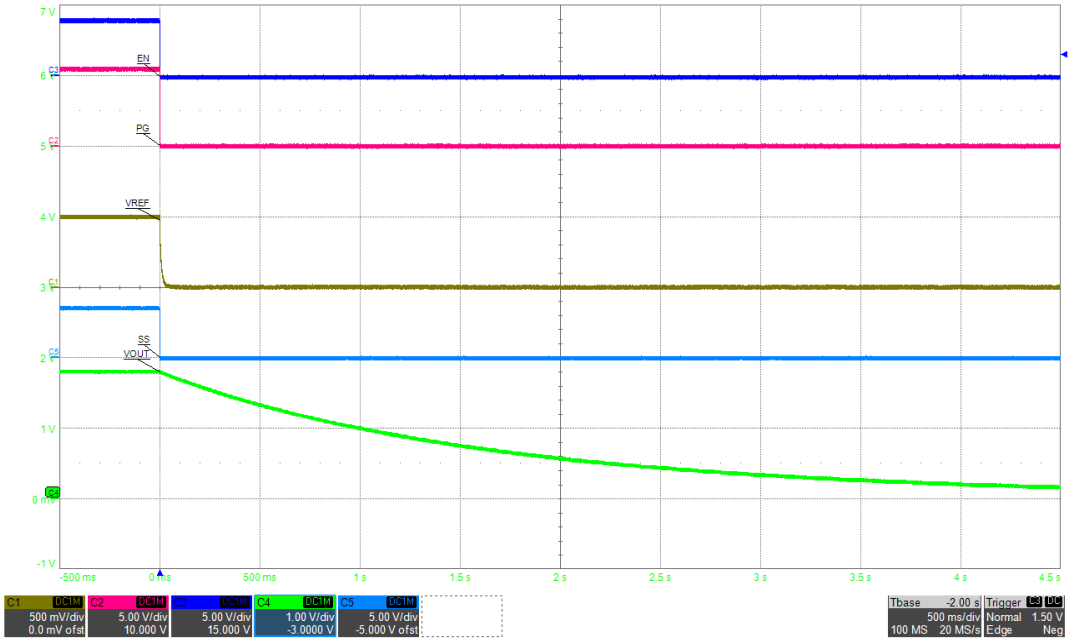

Figure 19. Shutdown; LDO Mode, Config Low
(V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = V_{REF_INT}, V_{OUT} = 1.8V, I_{OUT} = 0A)

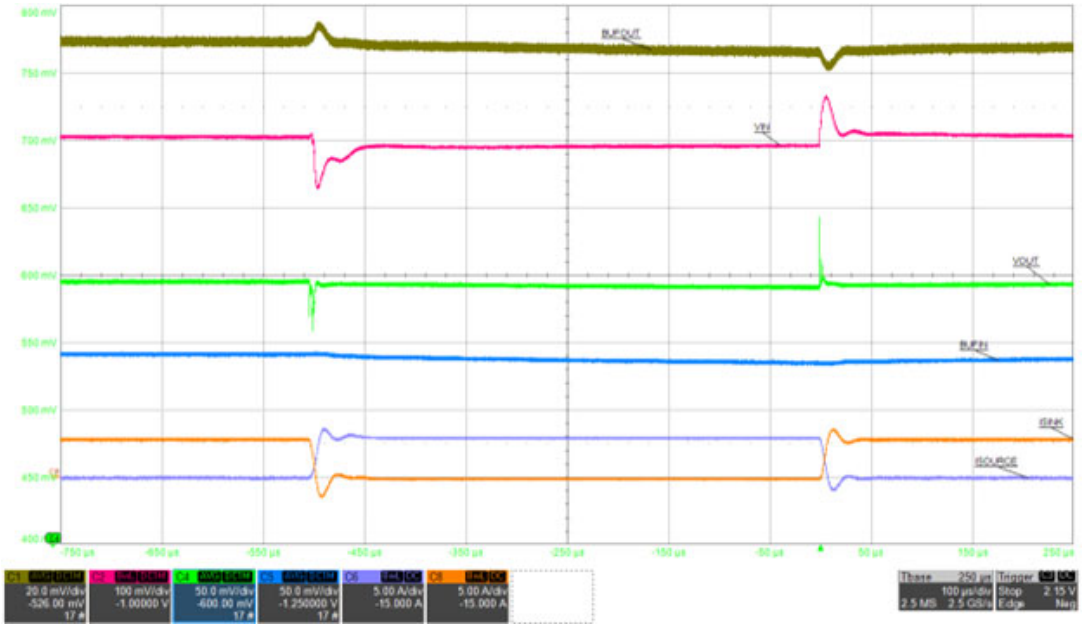

Figure 20. Load Transient Response; DDR4
(V_{IN} = BUF - IN = 1.2V, V_{CC} = 2.7V, Load Step = -3A to +3A)

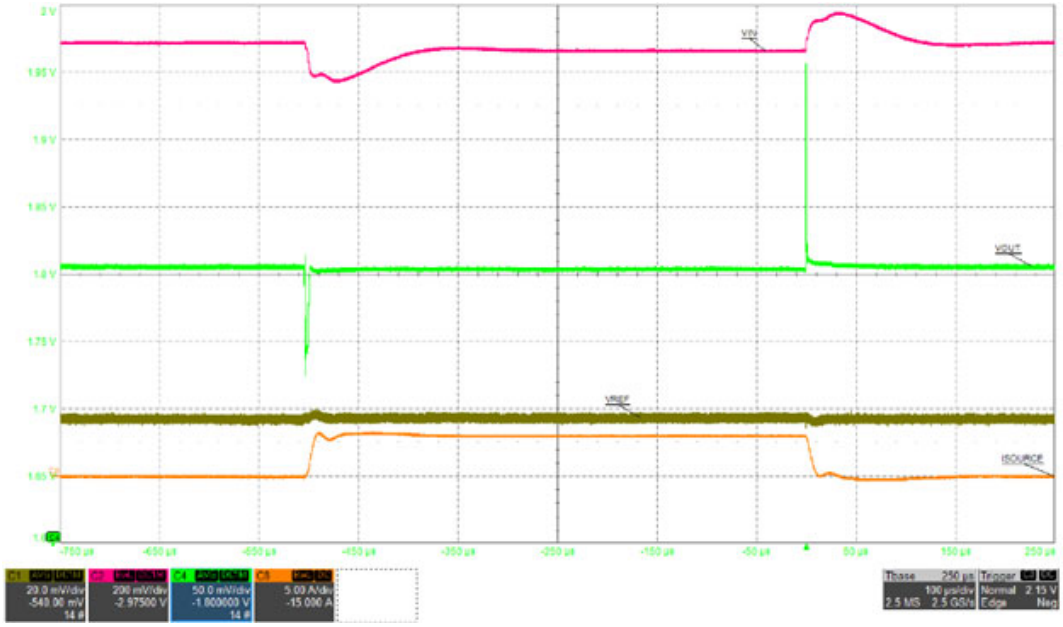

Figure 21. Load Transient Response; 1.8V LDO
(V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = V_{REF_INT}, Load Step = 0 to +3A)

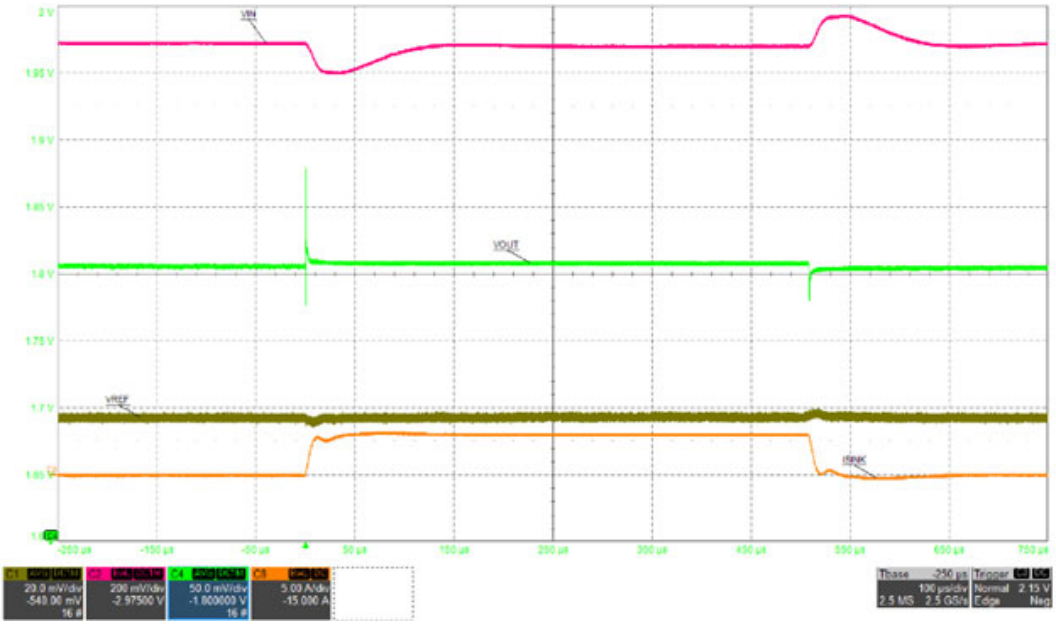

Figure 22. Load Transient Response; 1.8V LDO
(V_{IN} = 3.6V, V_{CC} = 5.5V, EA+ = V_{REF_INT}, Load Step = 0 to -3A)

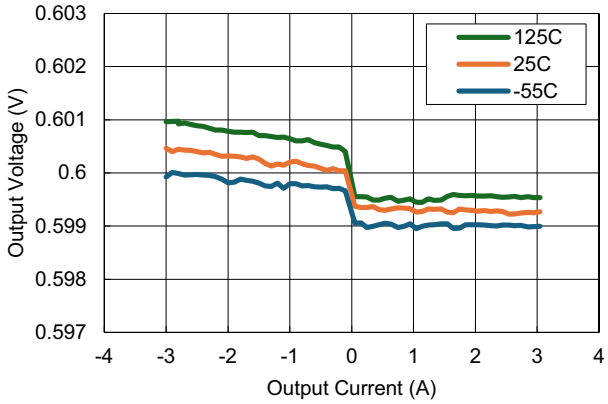

Figure 23. DDR4 Load Regulation (V_{CC} = 2.7V, V_{IN} = 1.2V, BUF - IN = 1.2V, EA+ = BUF - OUT, V_{OUT} = 0.6V)

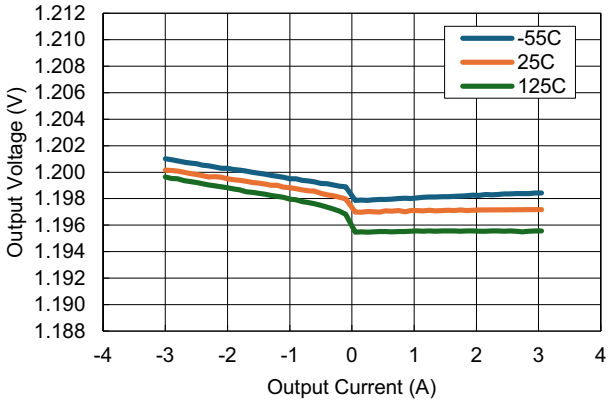

Figure 24. LDO Load Regulation (V_{CC} = 2.7V, V_{IN} = 1.8V, EA+ = V_{REF_INT}, V_{OUT} = 1.2V)

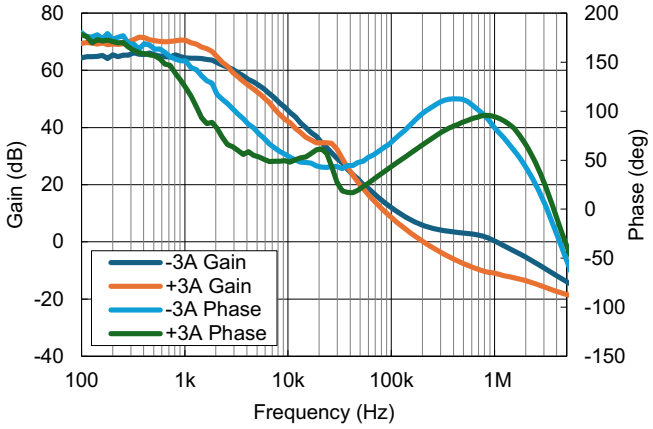

Figure 25. Bode Plot; DDR4 (V_{IN} = 1.2V, BUF = IN = 1.2V, V_{CC} = 3.3V, EA+ = BUF - OUT)

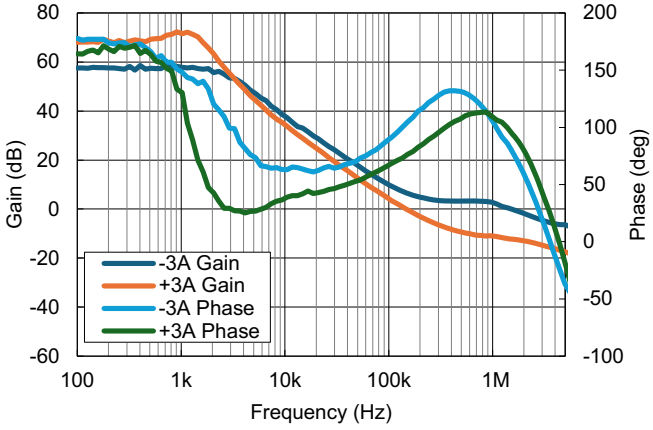

Figure 26. Bode Plot; 1.2 LDO (V_{IN} = 3.3V, V_{CC} = 3.3V, EA+ = V_{REF_INT})

4. Ordering Information

Part Number	Description
ISL75055SLHEV1Z	Radiation Hardened 3A Source and Sink DDR Terminator/LDO Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Jan 22, 2026	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.