ISL73040SEHEV4Z

The ISL73040SEHEV4Z evaluation board demonstrates how to build a half bridge power stage with the ISL73040SEH low-side GaN driver and the ISL73024SEH 200V GaN FET. The same board can be used to evaluate the ISL70040SEH alongside the ISL70024SEH, which are the same die offered with different radiation assurance screening. The ISL73040SEH has a 4.5V gate drive voltage (VDRV) generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of the ISL73024SEH GaN FET. The ISL73024SEH is a 200V GaN FET capable of 7.5A drain current.

Key Features

▪ Single PWM input to drive a half bridge configuration

▪ Adjustable dead time control

▪ Wide openings to support various inductor footprints

▪ >95% peak efficiency with high switching frequencies

▪ Enable/disable functions

Specifications

▪ V_{DD} = 4.5V to 13.2V

▪ V_{BUS} = up to 100V (limited by VDS of the GaN FET)

▪ PWM input: 40kHz to 1MHz, duty cycle = 2% to 97%

Related Literature

For a full list of related documents, visit our website:

▪ ISL73040SEH, ISL73024SEH, ISL70040SEH, ISL70024SEH device pages

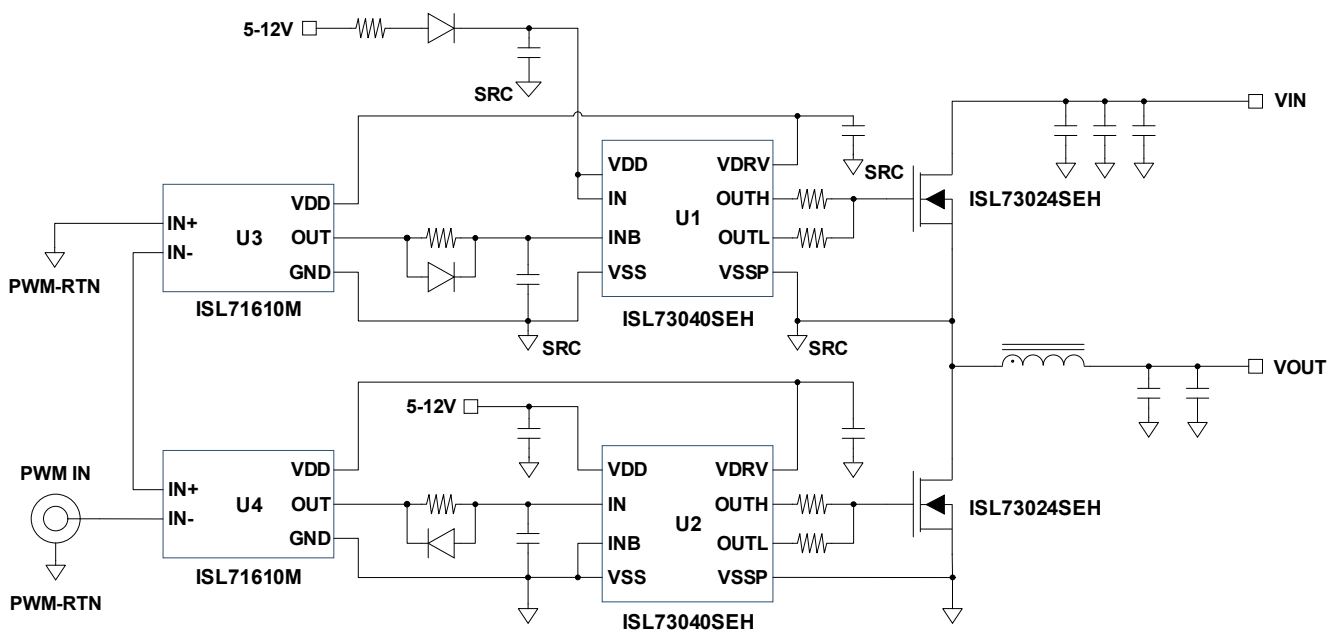Figure 1. ISL73040SEHEV4Z Block Diagram

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1. Functional Description

The ISL73040SEHEV4Z demonstrates how to use the ISL73040SEH and ISL73024SEH in a half bridge configuration. The following sections describe how to tune the evaluation board for a given application.

1.1 PWM Input

The input signal frequency is limited to 40kHz to 1MHz with a duty cycle between 2% and 97%, and is fed into J_7. The input is designed to accommodate voltages between 3.3V and 10V to be compatible with readily available PWM controllers on the market. The input signal is fed into two ISL71610M front ends in series, which can be simplified into coils with a coil resistance of 128Ω each. R_{20} and C_{55} control the current going into the input coils of the ISL71610M. Assuming the input voltage is 3.3V, R_{20} is set to 150Ω, which limits the current into the ISL71610M front end to 8mA (steady state), and C_{55} provides the instantaneous current for quicker rise and fall times. R_{22} (1MΩ) and C_{56} (100pF) are optional, but provide the ability to isolate the incoming signal from power ground.

1.2 Dead Time Control Adjustment

The dead time control is adjusted based on the RC charge and discharge times of R_6/C_{54} and R_5/C_{22}. The ISL73040SEH has inverting and non-inverting inputs that provide complimentary drive for the upper and lower GaN FETs. D_3 and D_4 ensure that the turn-on time is delayed only for the high-side and low-side by providing a lower resistance path during turn-off.

Dead time is controlled by turning off the active GaN FET quickly and delaying the turn-on of the inactive FET. Select the R and C values so that the charge and discharge times to the logic thresholds of the ISL73040SEH are equal to the desired dead time. The ideal RC charge and discharge profiles are shown in Figure 2 and Figure 3, respectively:
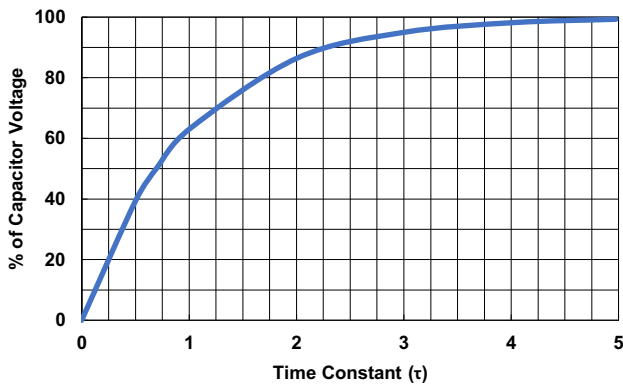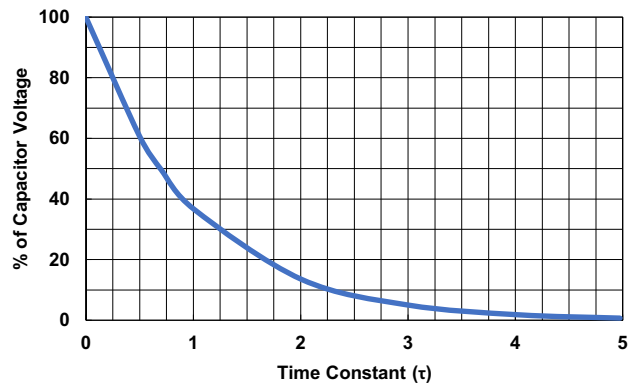

Figure 2. RC Charge Profile

Figure 3. RC Discharge Profile

The final capacitor voltage is 4.5V because the V_{DD} of the ISL71610M is tied to the VDRV of its respective gate driver. As the high side GaN FET is driven with an inverted logic signal, the dead time for turning on the high-side is determined by how long the RC filter takes to discharge from 4.5V down to the V_{IL} of the ISL73040SEH, which is 31.1% of 4.5V (V_{IL} = 1.4V). The dead time for turning on the low-side is gated by the RC filter's charging time up to the V_{IH} of the ISL73040SEH, which is 37.8% of 4.5V (V_{IH} =1.7V). These percentages yield time constant multiples of 1.1668τ for the high-side dead time, and 0.4721τ for the low-side dead time (where τ is the time constant). The dead time can be calculated using Equation 1 (where t_{don} is the high-side dead time, in seconds)

and Equation 2 (where t_{doff} is the low-side dead time, in seconds) by choosing a capacitor value (100pF is used in this design) and calculating the needed resistance.

(EQ. 1) $\quad R_6 = \dfrac{(t_{don} / 1.1668)}{100 \times 10^{-12} F}$

(EQ. 2) $\quad R_5 = \dfrac{(t_{doff} / 0.4721)}{100 \times 10^{-12} F}$

For example, a t_{don} (high side dead time) of 16ns and a t_{doff} (low side dead time) of 30ns yields $R_5 = 635\Omega$ and $R_6 = 137\Omega$. Use common resistor values to round $R_5 = 620\Omega$ and $R_6 = 140\Omega$. These calculations do not account for propagation delay mismatches between the high-side and low-side drivers (U_1/U_2) and the high-side and low-side isolators (U_3/U_4), so the final value on the board may need to be adjusted to achieve the desired results. Figure 15 shows the actual dead times that result from using $R_5 = 620\Omega$ and $R_6 = 140\Omega$.

1.3 Quick Start Guide

The following equipment is needed to evaluate the board:

- Bus power supply: a power supply capable of 100V with 5A current capability
- Bias power supply: a power supply capable of 5V to 12V with 1A current capability
- Function generator capable of producing a square wave up to 1MHz with duty cycle control
- Electronic load capable of 7A
- Digital multimeter to measure V_{OUT}

1.3.1 Operation Procedure

1. Connect the bus power supply between VBUS and GND (J_3/J_4).
2. Connect the bias power supply between J_1 and J_2.
3. Connect the function generator the BNC jack (J_7) on the board.
4. Connect the electronic load to VOUT and GND (J_5/J_6).
5. Connect the digital multimeter between VOUT and GND (J_5/J_6).
6. Set the bias power supply to any voltage between 5V and 12V. In this example it is set to 5V.
7. Set the bus power supply to 100V.
8. Set the electronic load anywhere up to 7A. The inductor on the evaluation platform is rated for 10.5A with a 20°C rise in temperature, so 7A provides enough margin.
9. Set the function generator to output a square wave with 28% duty cycle at 500kHz.
10. Set the function generator output voltage levels to $V_{OL} = 0.0V$ and $V_{OH} = 3.3V$. The PWM voltage is limited 10V, because of a 25mA coil rating. The input coils of U_3 and U_4 are specified at 128Ω (max) each.
11. Turn on the bias power supply.
12. Turn on the bus power supply.
13. Turn on the function generator output.
14. V_{OUT} should be roughly 28% of the bus supply voltage (100V in this example).
15. Turn on the electronic load.
16. V_{OUT} drops below 28V. The duty cycle of the function generator can be modified to return V_{OUT} to 28V.

2. Single Events Effects Testing

The ISL73040SEHEV4Z, which uses the ISL71610M isolators and the ISL73040SEH drivers was evaluated for shoot-through under heavy ions. The following is the test setup:

- VDD = 12V
- VBUS = 28V
- L1 was depopulated
- A 1Ω current-sense resistor was placed in line with the drain of Q1
- A 1MHz, 0V-5V signal was provided to J7
- LET = 86MeV•cm^2/mg
- Fluence = $1x10^7$ions/cm^2

The voltage at the drain of Q1 was monitored on an oscilloscope for events with a trigger window of ±50mV around the nominal voltage at the drain. A shoot-through event under heavy ions turned on Q1 and Q2, pulling the Q1 drain significantly below VBUS. A 50mV trigger window across 1Ω represents 50mA of shoot-through current. For the first test, both isolators (ISL71610M) were simultaneously exposed to heavy ions, no events were captured. For the second test, both drivers (ISL73040SEH) were simultaneously exposed to heavy ions with no events captures. In conclusion, there were no shoot-through events recorded for the half-bridge configuration used in the ISL73040SEHEV4Z evaluation board up to an LET of 86MeV•cm^2/mg.
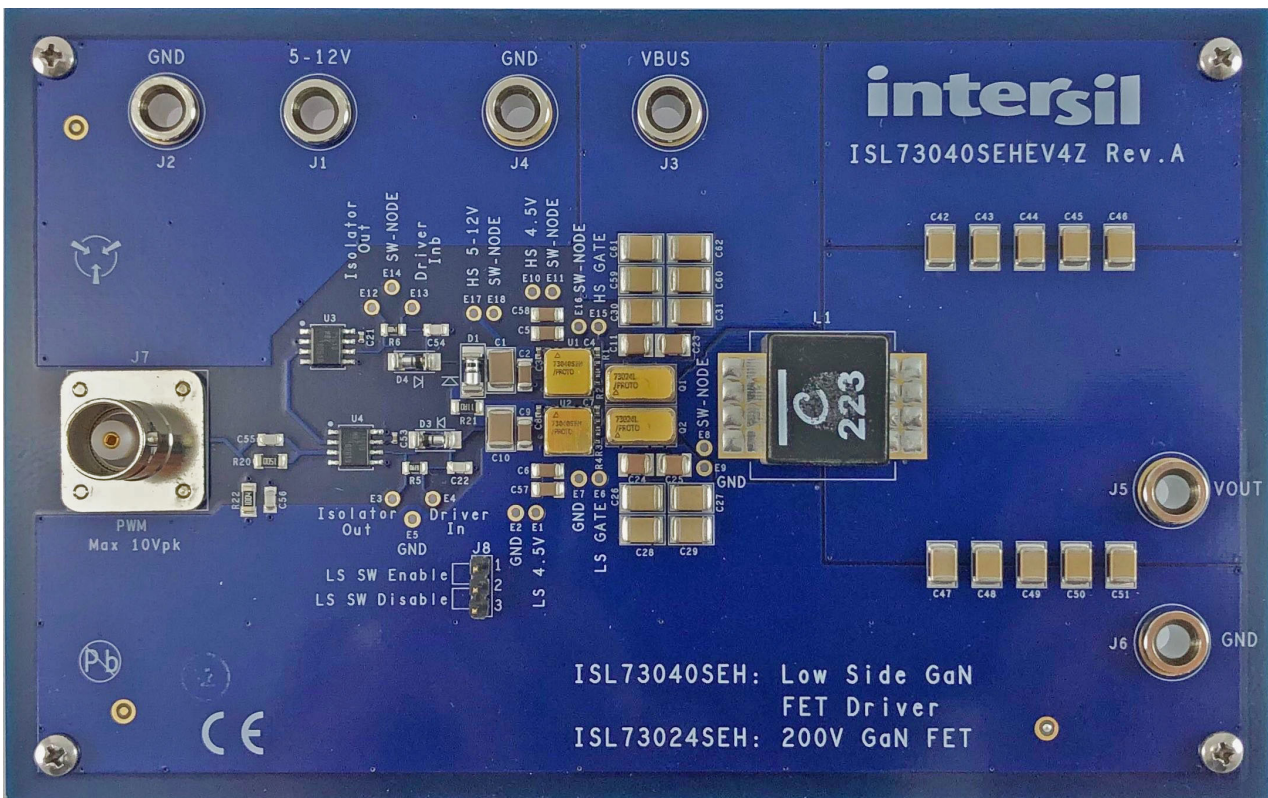
3. Board Design

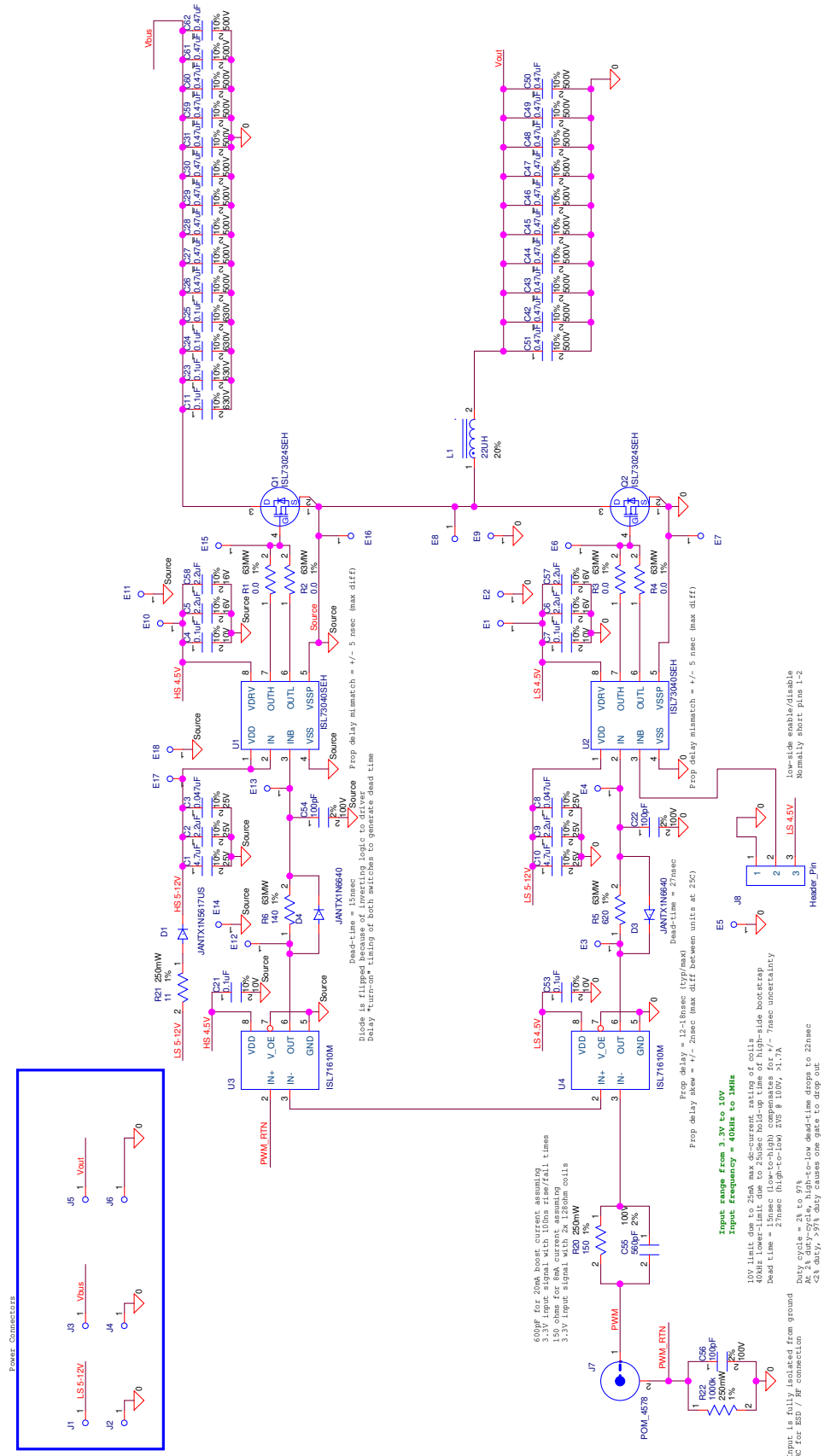**Figure 4. ISL73040SEHEV4Z Evaluation Board (Top)**

3.1   Schematic Diagrams

Figure 5. ISL73040SEHEV4Z Board Schematic

3.2   Bill of Materials

Qty	Reference Designator	Description	EDM Mfg.	EDM Mfg. Part Number	Flight Mfg.	Flight Mfg. Part Number
2	C1, C10	4.7µF Capacitor, X7R, 25V, 1812	KEMET	C1812F475K5RAC7800	AVX	G311P838-A-FX475K1R1
6	C2, C5, C6, C9, C57, C58	2.2µF Capacitor, X7R, 25V, 1206	KEMET	C1206C225K3RACTU	AVX	G311P838-A-DX225K1R1
2	C3, C8	0.047µF Capacitor, X7R, 25V, 0402	KEMET	C0402C473K3RACAUTO	Presidio	G311P829-A-AX473K1N1
4	C4, C7, C21, C53	0.1µF Capacitor, X7R, 10V, 0402	KEMET	C0402C104K4RALTU	Presidio	G311P829-A-AX104K1N1
4	C11, C23, C24, C25	0.1µF Capacitor, X7R, 250V, 1210	KEMET	C1210C104KBRACAUTO	KEMET	C1210T104KARAL
3	C22, C54, C56	100pF Capacitor, NP0, 100V, 0805	AVX	08051A101GAT2A	Presidio	SR0805NP0101G3NT9
20	C26, C27, C28, C29, C30, C31, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C59, C60, C61, C62	0.47µF Capacitor, X7R, 250V, 1812	KEMET	1812PC474KAT2A	KEMET	C1812T474KARAL
1	C55	560pF Capacitor, NP0, 100V, 0805	AVX	08051A561GAT2A	Presidio	SR0805NP0561G3NT9
1	D1	Diode 400V 1A, D5A	Microsemi	1N5617US	Microsemi	JANS1N5617US
2	D3, D4	Diode 50V 300mA, D5D	Microsemi	1N6640US	Microsemi	JANS1N6640
18	E1, E2, E3, E4, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, E17, E18	Test point E20AWG	N/A	N/A	N/A	N/A
6	J1, J2, J3, J4, J5, J6	Banana Jack	Keystone Electronics	575-8	N/A	N/A
1	J7	BNC Jack	Pomona	4578	N/A	N/A
1	J8	Header Pin	Samtec	TSW-103-07-F-S	N/A	N/A
1	L1	Inductor 22µH Note: Flight Inductor DCR >> EDM DCR	Coilcraft	XAL1510-223	Coilcraft	AE612PNB223MSZ
2	Q1, Q2	GaN FET 200V 45mΩ 7.5A	Renesas	ISL73024SEHL/PROTO	Renesas	ISL73024SEH

Qty	Reference Designator	Description	EDM Mfg.	EDM Mfg. Part Number	Flight Mfg.	Flight Mfg. Part Number
4	R1, R2, R3, R4	Resistor 0Ω Jumper, 0402	Vishay Beyschlag	MCS04020Z0000ZE000	Vishay	M32159B11T
1	R5	Resistor 619Ω 1%, 0805	Vishay Dale	CRCW0805619RFKEA	Vishay	M55342K06B619DS
1	R6	Resistor 140Ω 1%, 0805	Vishay Dale	CRCW0805140RFKEA	Vishay	M55342K06B140DS
1	R20	Resistor 150Ω 1%, 1206	Vishay Dale	CRCW1206150RFKEA	Vishay	D55342K07B150DS
1	R21	Resistor 11Ω 1%, 1206	Vishay Dale	CRCW120611R0FKEA	Vishay	D55342K07B11D0S
1	R22	Resistor 1000kΩ 1%, 1206	Vishay Dale	CRCW12061M00FKEA	Vishay	D55342K07B1F00S
2	U1, U2	RH Low-Side GaN FET Driver	Renesas	ISL73040SEHL/PROTO	Renesas	ISL73040SEH
2	U3, U4	RT Digital Isolator	Renesas	ISL71610M	Renesas	ISL71610M

3.3   Board Layout
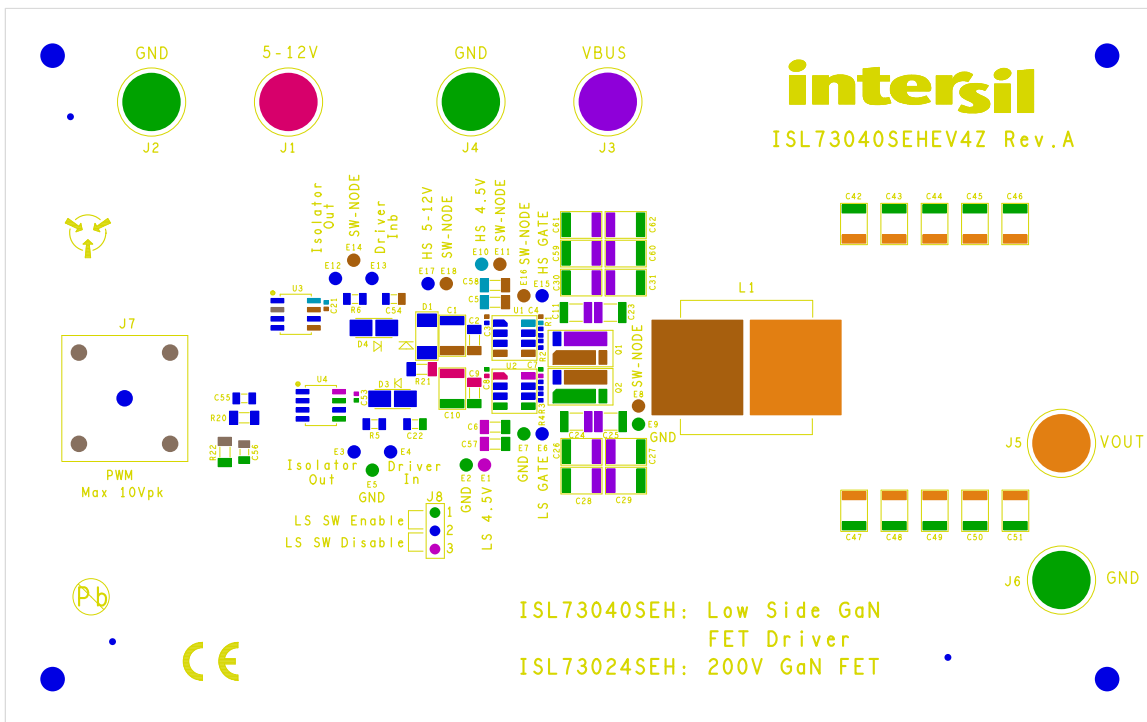
Figure 6. Silkscreen Top
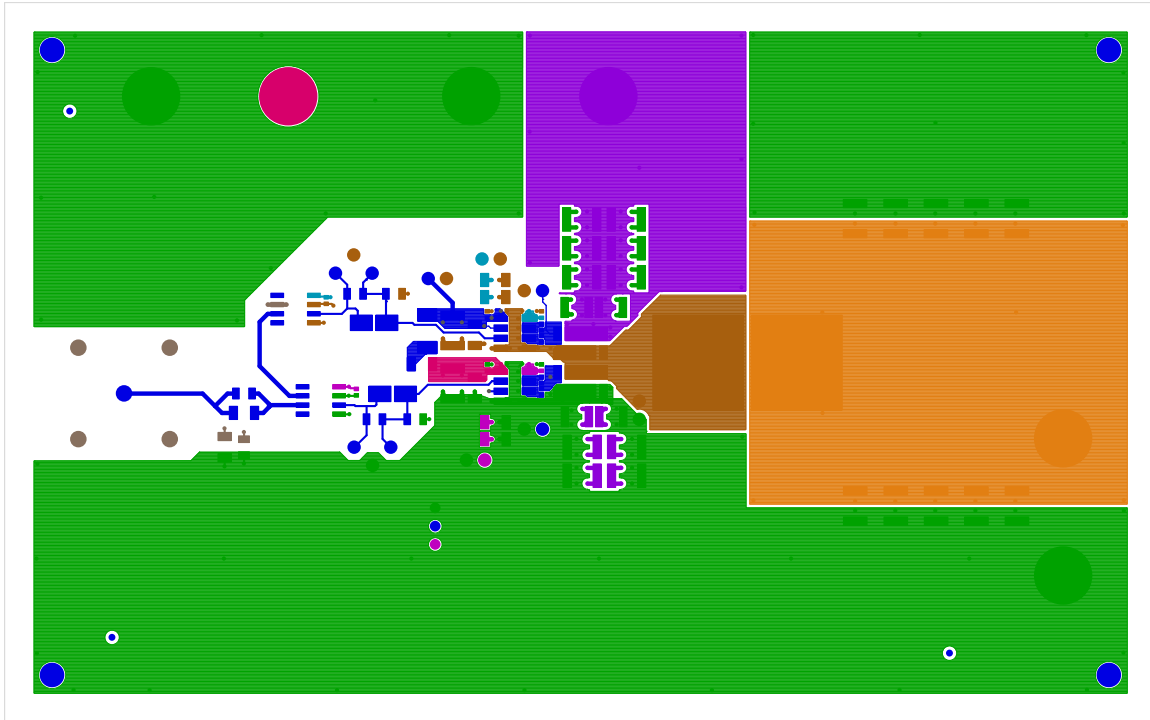
Figure 7. Layer 1 (Component Side)
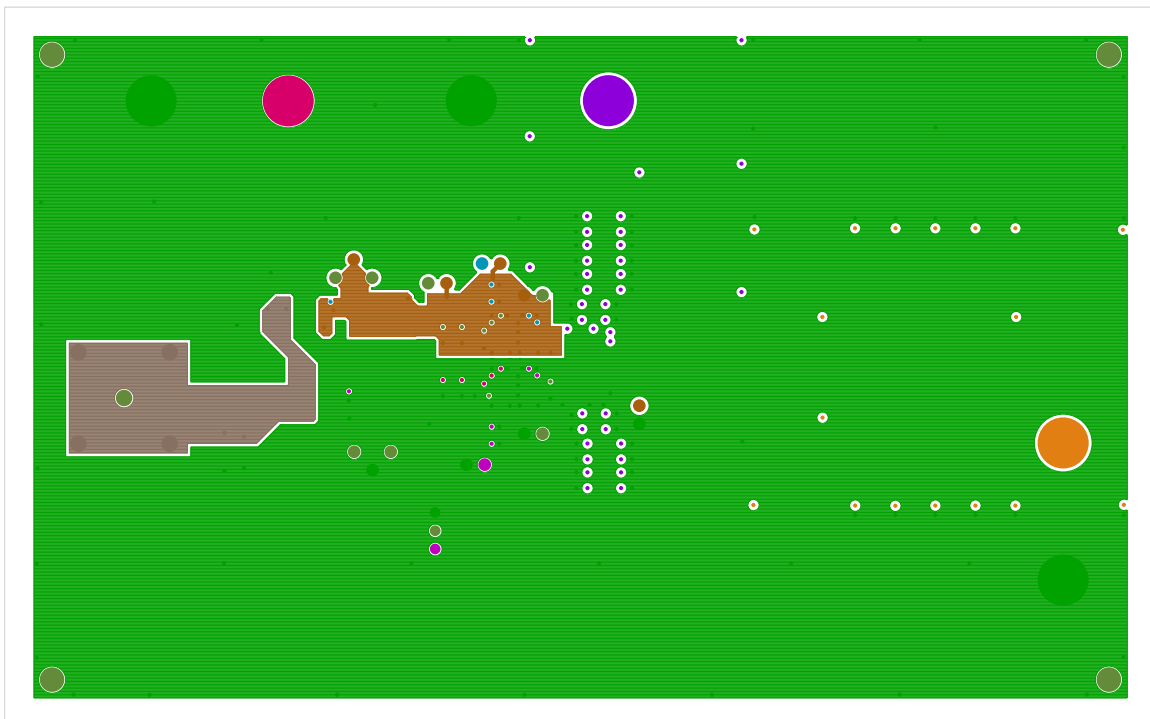
Figure 8. Layer 2
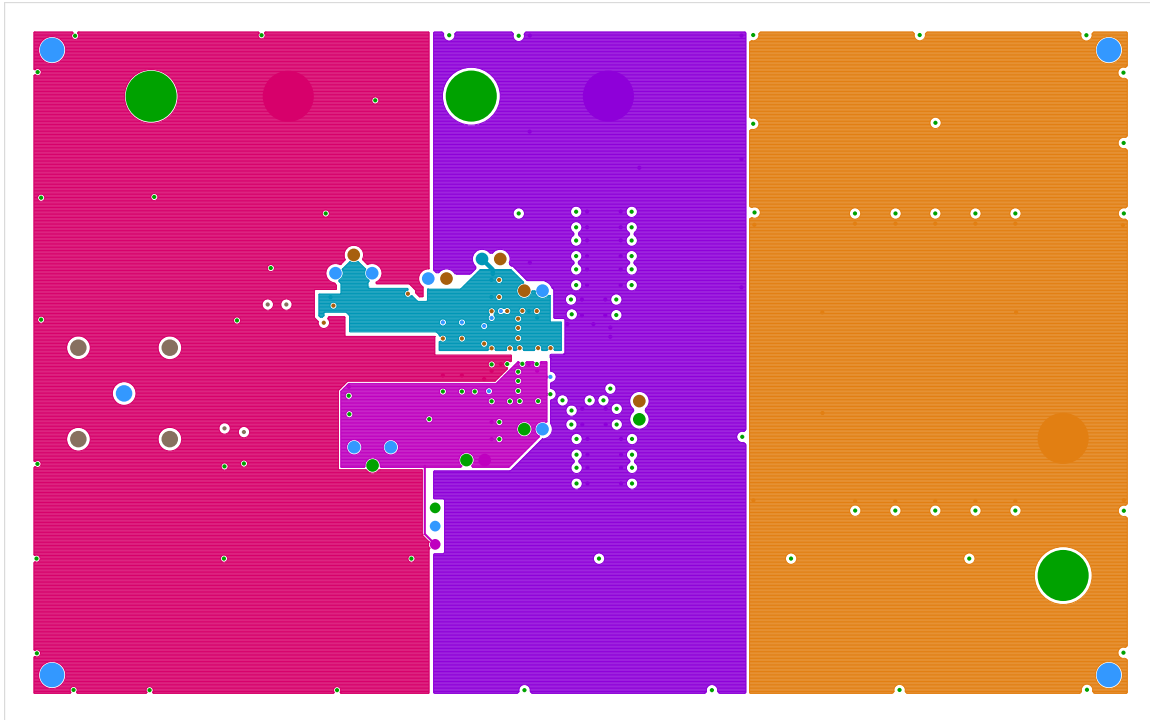
Figure 9. Layer 3
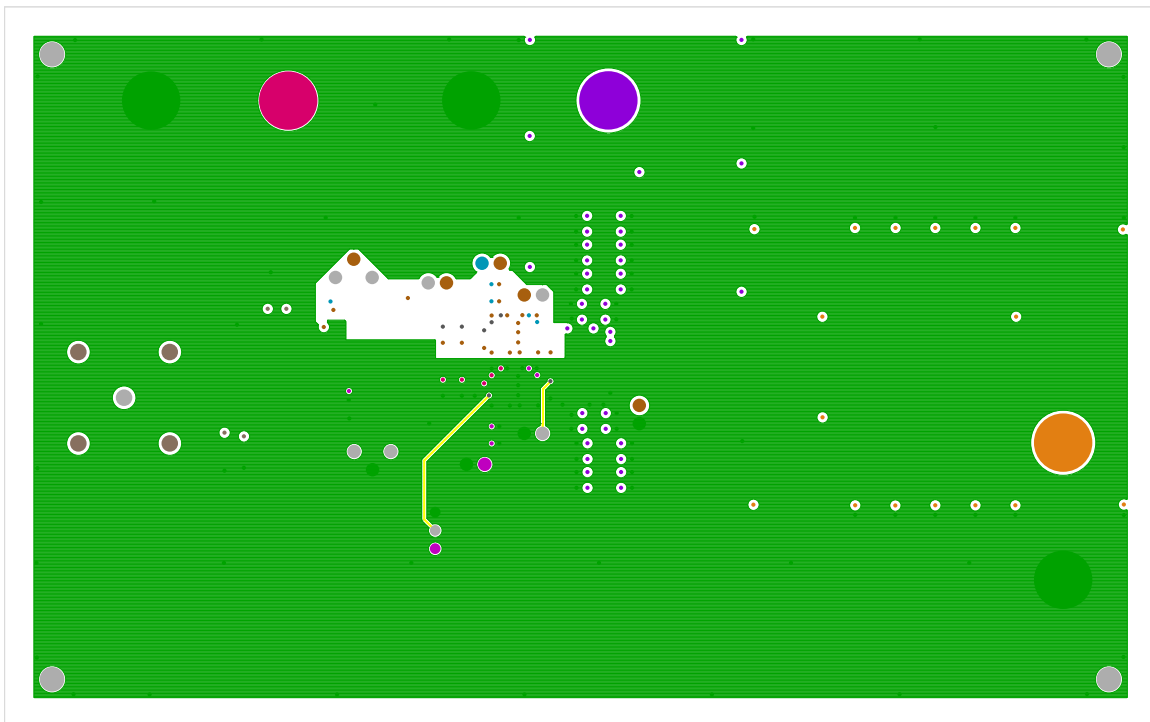
Figure 10. Layer 4

3.4 PCB Layout Guidelines

When replicating this layout in a system, pay attention to the following guidelines:

▪ Place the driver as close as possible to the driven power FET.

▪ Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induce significant voltage transients on the associated traces.

▪ Keep power loops as short as possible by paralleling the source and return traces.

▪ Use planes where practical; they are usually more effective than parallel traces.

▪ Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines.

▪ When practical, minimize impedances in low level signal circuits. The noise that is magnetically induced on a 10kΩ resistor is 10 times larger than the noise on a 1kΩ resistor.

▪ Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures emit lots of flux.

▪ If you must place traces close to magnetic devices, align the traces parallel to the flux lines to minimize coupling. The use of low inductance components such as chip resistors and chip capacitors is highly recommended.

▪ Use decoupling capacitors to reduce the influence of parasitic inductance in the V_{DRV}, V_{DD}, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If using vias, connect several paralleled vias to reduce the inductance of the vias.

▪ It may be necessary to add resistance to dampen resonating parasitic circuits, especially on OUTH. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance.

▪ Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL73040SEH.

▪ Avoid placing signal ground planes under high amplitude dv/dt circuits. This injects di/dt currents into the signal ground paths.

▪ Calculate power dissipation and voltage drop for the power traces. Many PCB/CAD programs have built-in tools for calculating trace resistance.

▪ Large power components (such as power FETs, electrolytic caps, and power resistors) have internal parasitic inductance which cannot be eliminated. Account for this in the PCB layout and circuit design.

▪ If the circuits are simulated, consider including parasitic components, especially parasitic inductance.

▪ The GaN FETs have a separate substrate connection that is internally tied to the source pin. Source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and thick as possible.

4.   Typical Performance Curves
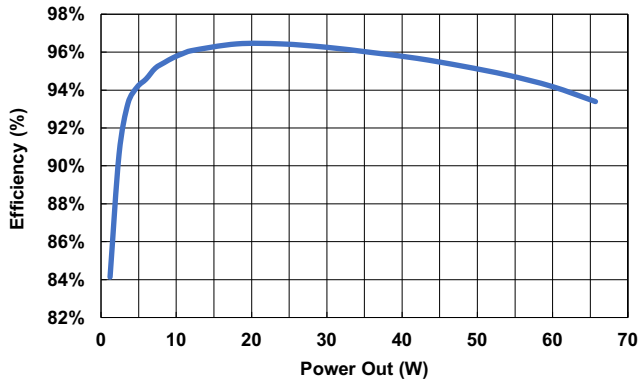
Unless noted: f_{SW} = 500kHz, T_A = +25°C

Figure 11. V_{BUS} = 28V, V_{OUT} = 12V
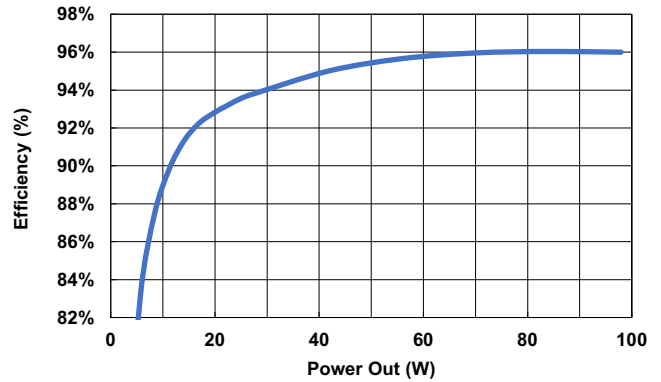
Figure 12. V_{BUS} = 70V, V_{OUT} = 28V
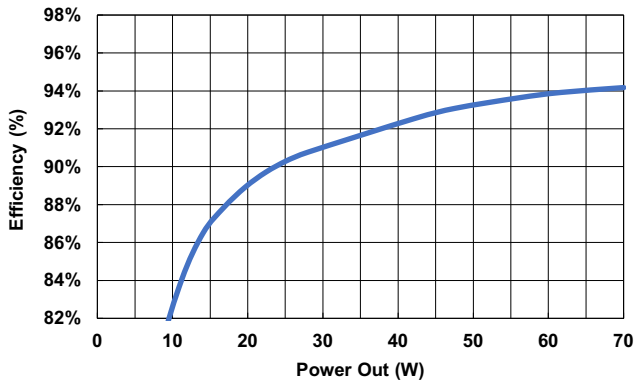

Figure 13. V_{BUS} = 100V, V_{OUT} = 28V
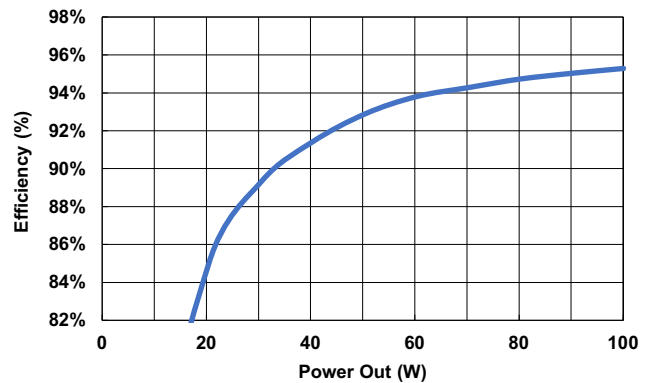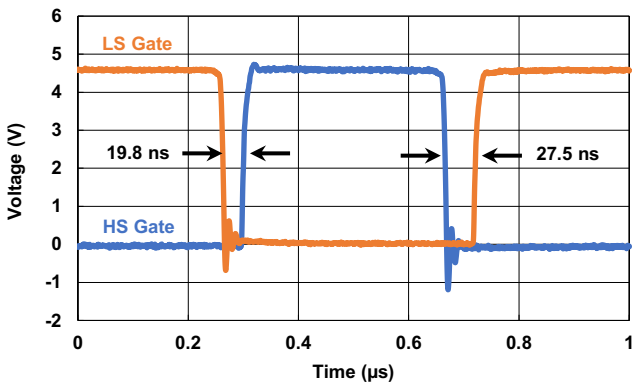

Figure 14. V_{BUS} = 120V, V_{OUT} = 100V
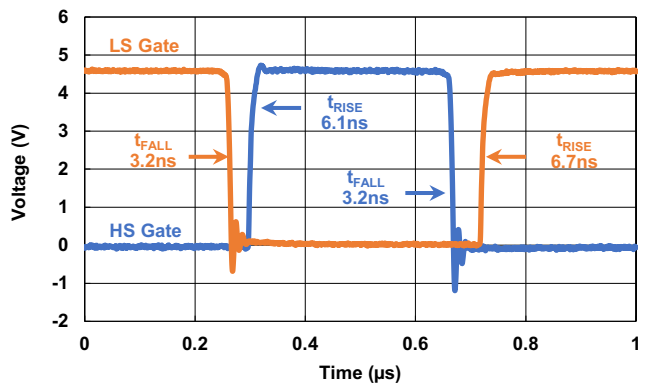

Figure 15. Dead Time Between HS and LS Gate

Figure 16. Rise and Fall Times

5.　Ordering Information

Part Number	Description
ISL73040SEHEV4Z	100V half bridge power stage evaluation board

6.　Revision History

Rev.	Date	Description
3.00	Jan 9, 2023	Applied new template. Updated Page 1 description and related literature.
2.00	Mar 24, 2021	Removed Front and Back Covers Added TOC. Added the SEE Testing section.
1.00	Feb 26, 2019	Updated Figures 2, 3, and 16.
0.00	Nov 20, 2018	Initial release

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